# BlackParrot FPGA Simulation Guide

Please visit the latest BP FPGA User Guide for the latest guide. Current version: 01/10/2021

# Vivado Setup

Before you run Vivado on KK9 (or other similar machine), make sure you source the settings file by running:

```
source /gro/cad/Xilinx/Vivado/2019.1/.settings64-Vivado.sh
```

To launch vivado, simply run the following command in the terminal

```
vivado &
```

(Optional) If you're planning to use VCS as the default vivado simulator, make sure you set the VCS_HOME and LM_LICENSE_FILE environment variables before launching Vivado. Note: you can also do it after you've launched Vivado by setting those two variables in the TCL console in Vivado.

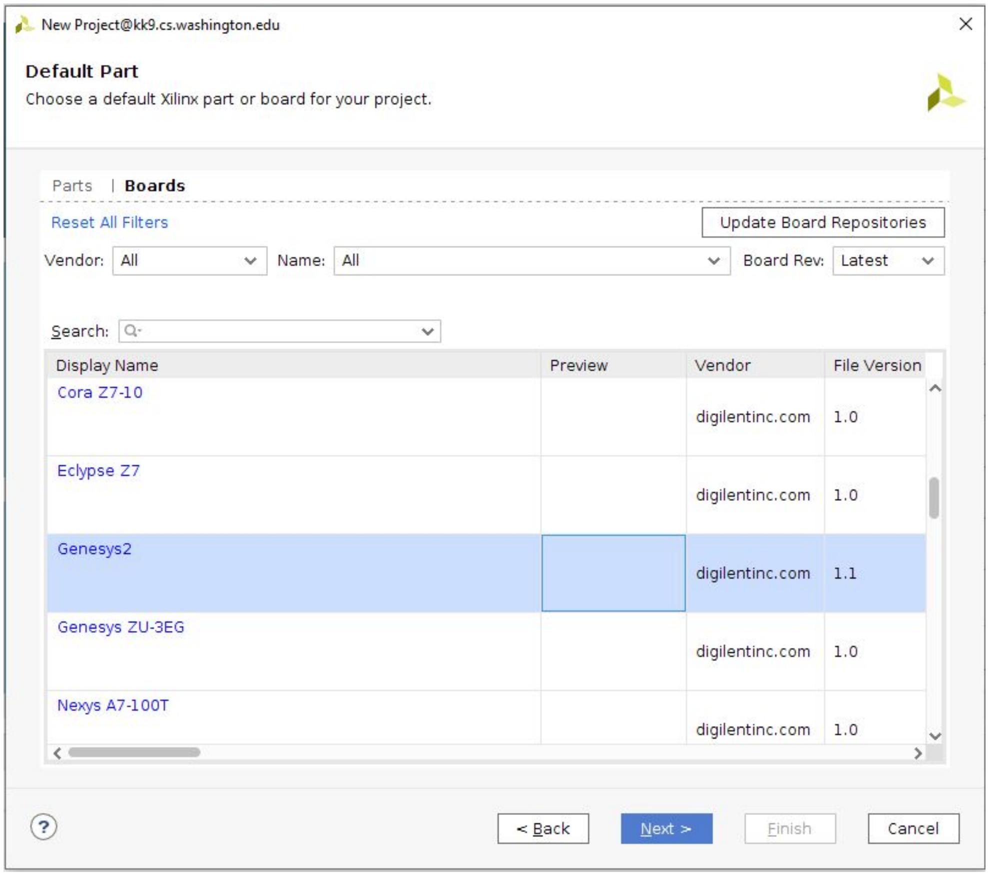
```
export VCS_HOME=<path to vcs-mx/O-2018.09-SP2-6>
export LM_LICENSE_FILE=<your license file>
```

# Packaging BlackParrot as a custom IP in Vivado

Add design sources to a project:

1) Check the reference documents below on how to start the basic steps
2) While selecting the default part of your project, you may select **Boards** and select **Genesys2** (Fig. 1) if you're working with Genesys2 boards. Hit **Next** and **Finish**.
3) Under the **Sources** window, you can add all of the BlackParrot related files to generate a BlackParrot IP. Right-click anywhere in the **Sources** window and select **Add Sources..**
4) Select **Add or Create Design Sources -> Add Files** and add all the files you need. Note: Be careful while adding a ton of files as it would take the Vivado tool a long time to Update the Hierarchy and Compile Order
5) Vivado tool automatically detects file hierarchy, for example, bp_be has many submodules and Vivado will automatically add those files under bp_be once they're added as design sources.

6) Notice how adding a design file may cause a syntax error in Vivado (Fig. 2). That is because the file is written in SystemVerilog but has a file extension of .v. Vivado thinks that this is a Verilog file and doesn't understand the syntax. To resolve this issue, go to the **Source File Properties** window and change the file type from Verilog to SystemVerilog.



New Project@kk9.cs.washington.edu

**Default Part**

Choose a default Xilinx part or board for your project.

Vendor: All Name: All Board Rev: Latest

Search:

| Display Name | Preview | Vendor | File Version |
|---|---|---|---|
| Cora Z7-10 | | digilentinc.com | 1.0 |
| Eclypse Z7 | | digilentinc.com | 1.0 |
| Genesys2 | | digilentinc.com | 1.1 |
| Genesys ZU-3EG | | digilentinc.com | 1.0 |
| Nexys A7-100T | | digilentinc.com | 1.0 |

Fig. 1 Selecting Parts/Boards when creating a project

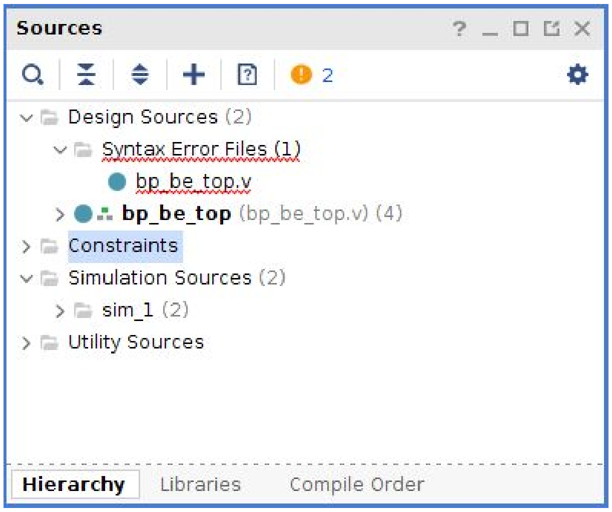


Fig. 2 Syntax error due to incorrect file type

7) You may still see some syntax error but that is ok because we have not yet added the dependent packages.
8) Now go ahead and add all of the files

Creating an IP with design source files:

1) Once you've added all the files, go to **Tools** on the top and select **Create and Package New IP**
2) Choose **Package your current directory** and select the correct directory for your IP to be packaged
3) A new window will open up, on the left hand side, select **Edit Packaged IP**
4) Go through the packaging steps and modify the parameters accordingly
5) For port interface, start by right clicking anywhere in the Ports and Interface window and choose **Add Bus Interface…** This allows you to better pack all the relevant IOs into a nicely packed bus format for the GUI
6) The Interface Definition allows you to select what kind of interface your signal is. Figure 3 shows a clock signal interface definition.
7) Next, map the correct interface's logic ports to IP physical ports (Fig. 4)
8) Once you're done with the other interfaces, make sure you associate those interfaces with a clock if needed. To do so, right click on the interface and select associate to clock.
9) As of now, there isn't a need for memory address mapping. But in the future, if multiple IO devices are supported, then it's necessary to segment the address so that the AXI interconnect IP will know where to direct the traffic
10) Once everything is done, go ahead and package the IP.

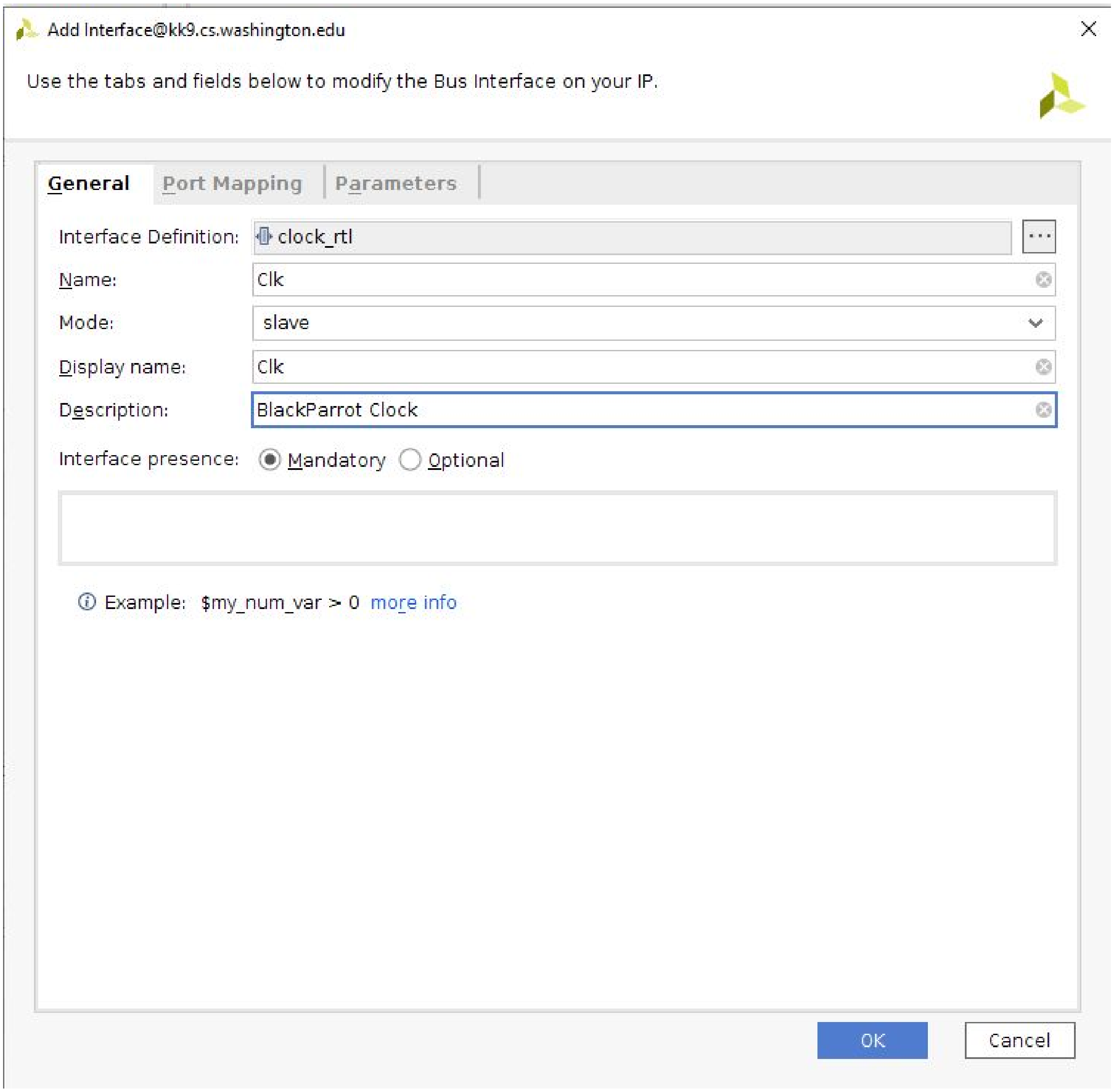
Reference documents:

ug1118-vivado-creating-packaging-custom-ip
ug1119-vivado-creating-packaging-ip-tutorial

# Adding BlackParrot to Vivado block design

Import the newly created IP into Vivado IP Catalog

1) When you have your new Vivado project open somewhere and you would like to add your new IP, you must first add a new repository where you've created your IP catalog.
2) Click **IP Catalog** in the Flow Navigator on the left side
3) Once the IP catalog is open, right click anywhere within and select **Add Repository…**
4) Navigate to where the IP is located and hit **Select**
5) The IP should now be added and should be visible in the IP list.



Add Interface@kk9.cs.washington.edu

Use the tabs and fields below to modify the Bus Interface on your IP.

Interface Definition: clock_rtl

Name: Clk

Mode: slave

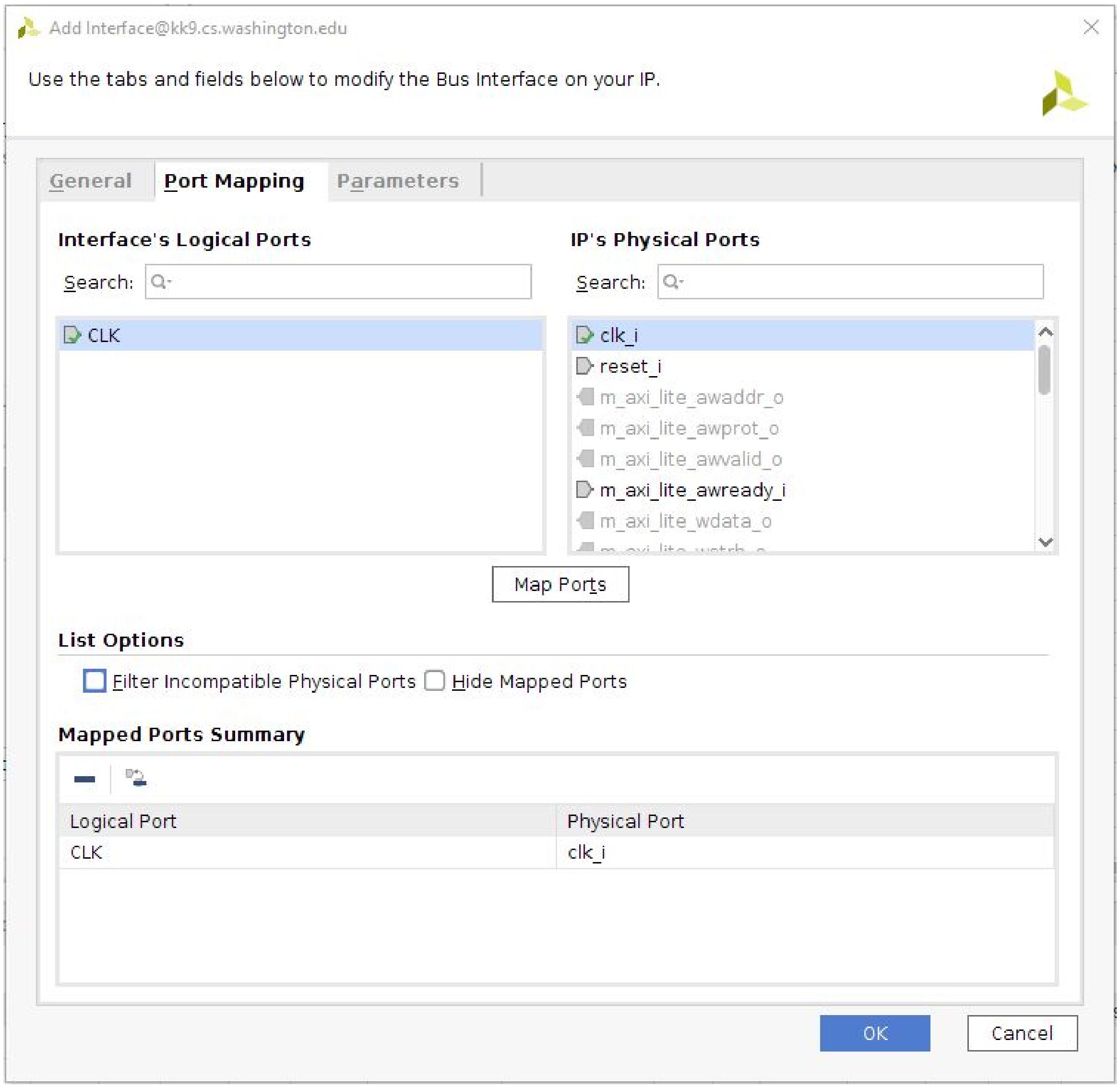
Display name: Clk

Description: BlackParrot Clock

Interface presence: ● Mandatory ○ Optional

ⓘ Example: $my_num_var > 0 more info

Fig. 3 Clock interface setup



Use the tabs and fields below to modify the Bus Interface on your IP.

**Interface's Logical Ports**

- CLK

**IP's Physical Ports**

- clk_i
- reset_i
- m_axi_lite_awaddr_o
- m_axi_lite_awprot_o
- m_axi_lite_awvalid_o
- m_axi_lite_awready_i
- m_axi_lite_wdata_o
- m_axi_lite_wstrb_o

**List Options**

☐ Filter Incompatible Physical Ports ☐ Hide Mapped Ports

**Mapped Ports Summary**

| Logical Port | Physical Port |
|---|---|
| CLK | clk_i |

Fig. 4 Clock port mapping

Adding BP as an IP:

1) Create a new block design
2) In the block design window, right click and search for BlackParrot as your design
3) Select the BlackParrot IP and it should now be added to your block design
4) To edit its parameters, double click the BlackParrot IP
5) To edit the files within the IP, right click and select **Edit In Packager**
6) A pop-up window should now appear and you can edit the IP mentioned in the earlier section

Reference documents:
ug994-vivado-ip-subsystems

# Block Design Description

Functionality of each IP in the block design:

1) See Fig. 5 - 7for the block design
2) **clk_wiz_100MHz**: use the system differential clock as a source to generate the a 100MHz clock
3) **rst_clk_wiz_100MHz:** generates a 100MHz active high/low synchronous reset
4) **axi_interconnect_0:** an asynchronous FIFO that converts the data from a 100MHz BlackParrot to a 225MHz Memory Interface Generator
5) **Mig_7series_0 (MIG):** a memory interface generator that converts AXI interface signals to DDR3 DRAM controller signals. This IP needs to be manually changed and the values should follow genesys2 board guidelines. Also, check the MIS (Memory Interface Solution) document for more Vivado DDR3 details..
6) **BlackParrot_0:** BlackParrot_V0_2020_12_22 which currently supports all simulation for all unicore configuration
7) For future designs, connect BP IOs to board supported communication IOs (such as UARTLITE or other switches). The UART communication IO can be used to load in programs

Reference documents:
https://reference.digilentinc.com/reference/programmable-logic/genesys-2/reference-manual
ug586_7Seriies_MIS

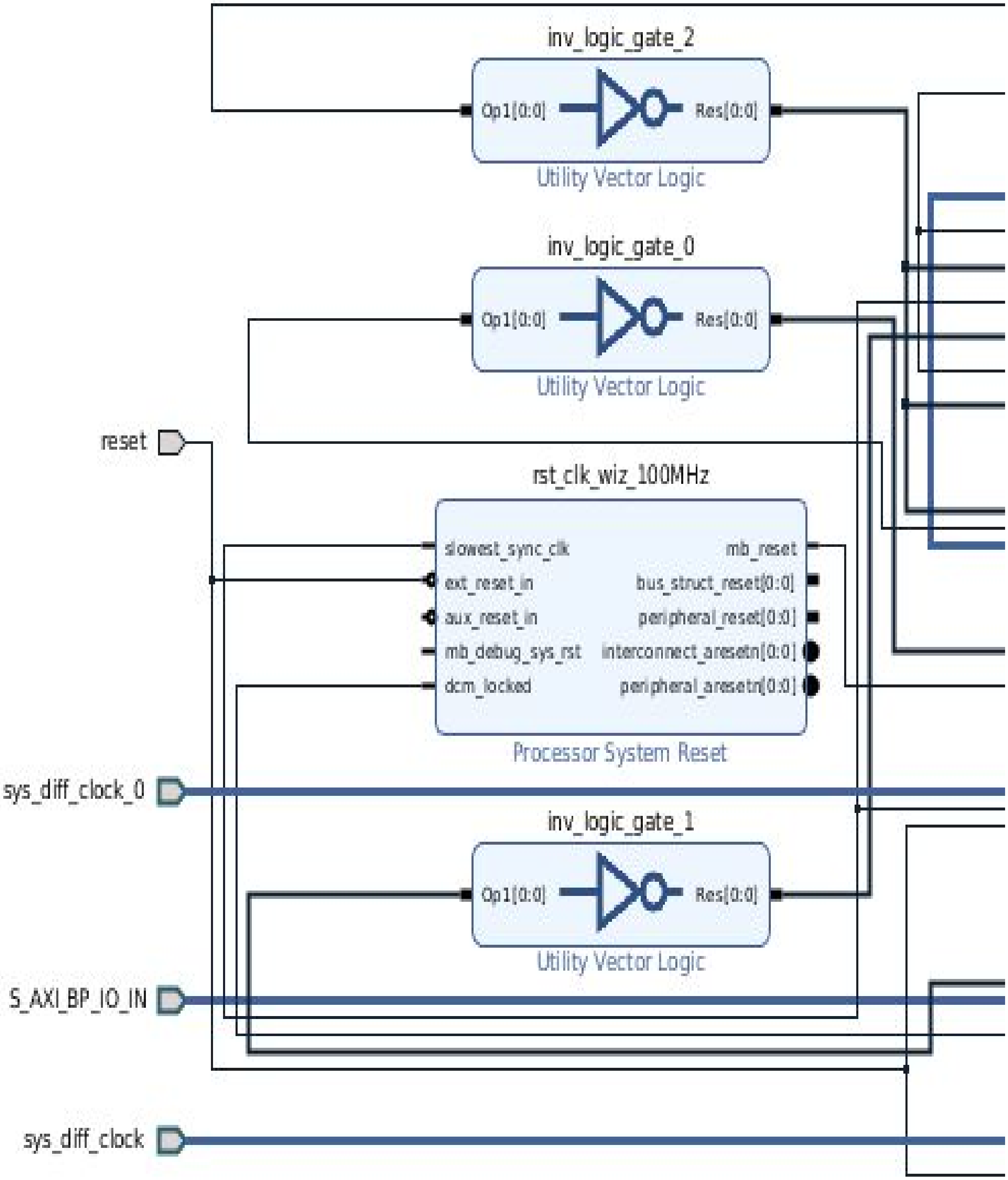


Fig. 5 Block design (left)

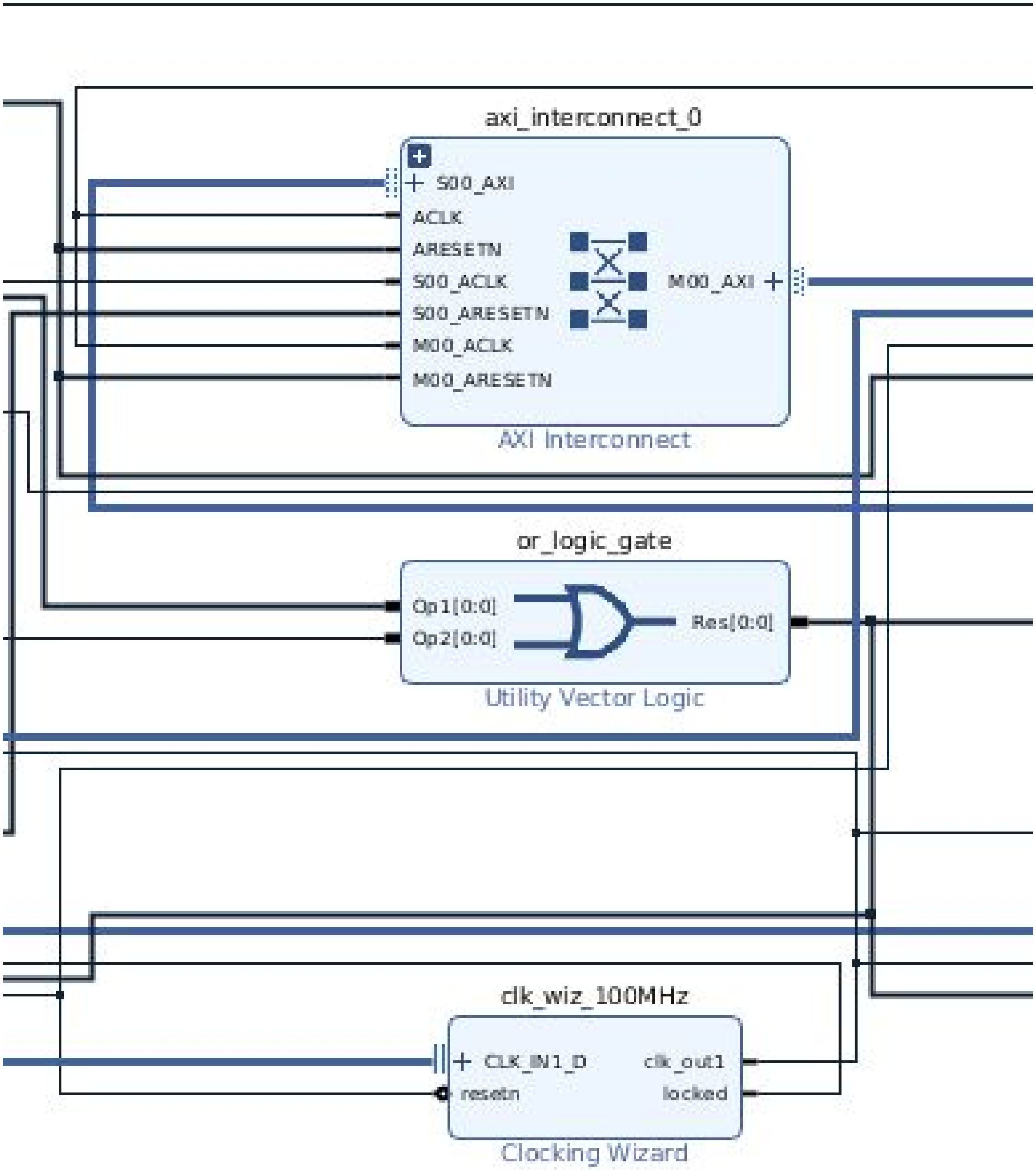


Fig. 6 Block design (middle)

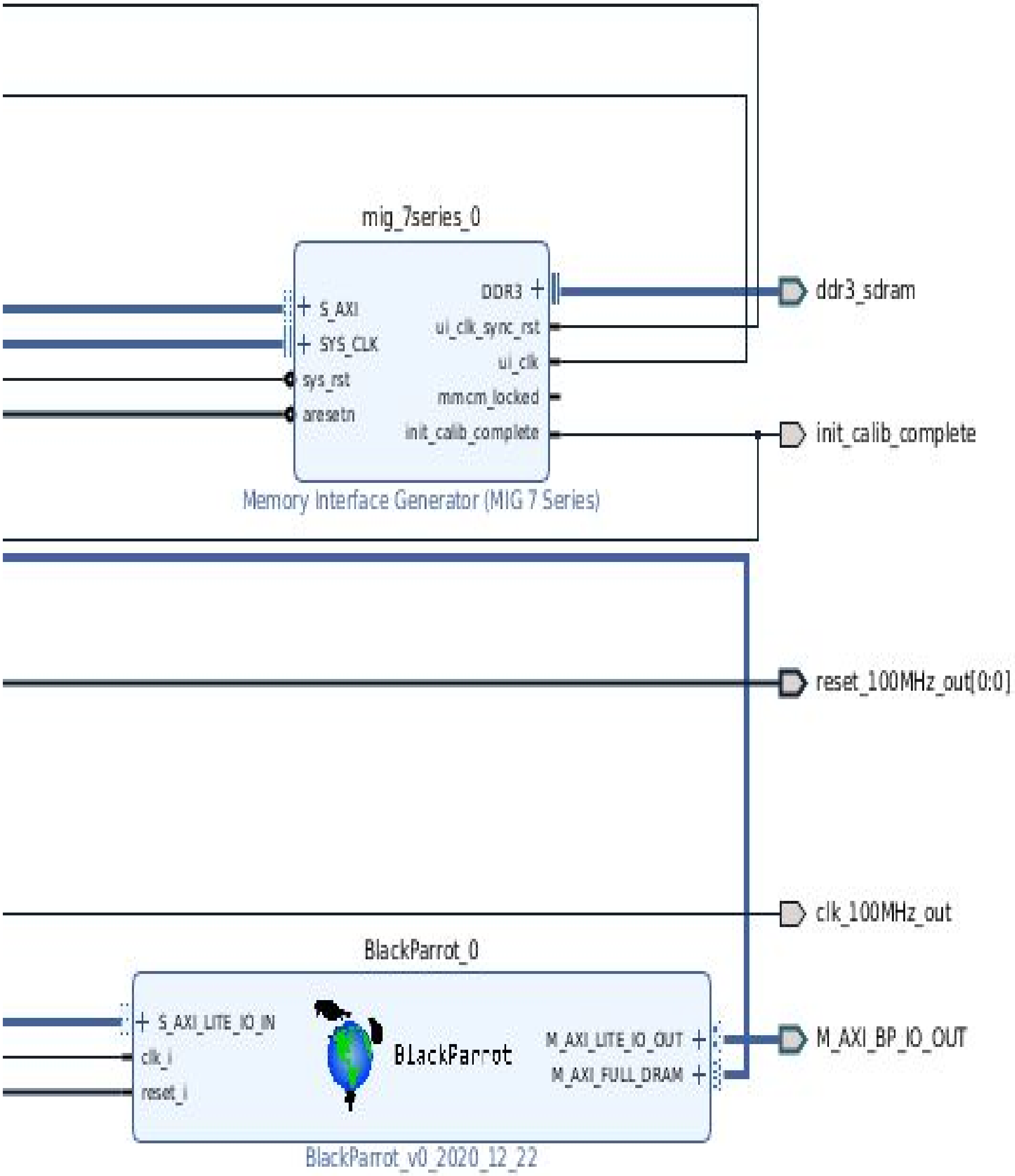


Fig. 7 Block design (right)

# Simulation

Simulation model:

1) Check Fig. 8 for simulation testbench setup
2) The simulation consists of a top level testbench that connects BP with a DDR3 model (provided by Xilinx and Micron), a block diagram design (BP + clk/rst + axi interconnect), and a program loader (that is the host + nbf_loader from BP).
3) With the provided scripts, VCS will be chosen as the default simulator with the simulation time set to 1ms. The proj_setup.tcl will set up the compilation, elaboration, and simulation flags
4) To add more VCS flags, click **Tools -> Setting -> Simulation**
5) Fig. 9 whos all the tabs in the simulation settings window
6) After the block diagram is design and all the ip files are generated, we have to add all of the simulation sources located in the bp_packaged_ip/tb
7) Vivado should automatically identify the hierarchy of the files
8) Make sure you set "sim_tb_top.v" as your top

Simulation breakdown:

1) BP waits for the MIG to be calibrated before doing anything. The calibration usually takes about 50,000,000ps to complete. Once the calibration is completed, BP will come out of reset
2) The DRAM's memory in the region of 0x0 - 0xffff is initialized to 0 through a file called "mem_init.txt"
3) The nbf files are loaded into BP through the bp_nonsynth_tb_top (host + nbf_loader). Prog.nbf and bootrom.mem are located in the bp_packaged_IP/tb
4) Once the simulation is launched, it will go through compilation, elaboration, and finally simulation.

Simulation hints/tips:

1) Simulation may be slow so be patient. Try out the smaller programs first to ensure it is working
2) Many components in the original blackparrot non-synth tb are commented out, like importing C functions. Thus you may not see many of the printouts from black-parrot RTL simulation. Don't freak out, you should still be able to see PASS/FAIL when the test is done.
3) You may also increase the BP operating frequency to higher than 100MHz, though that has led to other problems that you need to solve such as available FIFO slots in the AXI interconnect IP.

4) Sequences such as 5555, 9999, AAAA, 6666 are written into the DRAM during its initial calibration process. So don’t be afraid about seeing those values initially in the simulation printout.

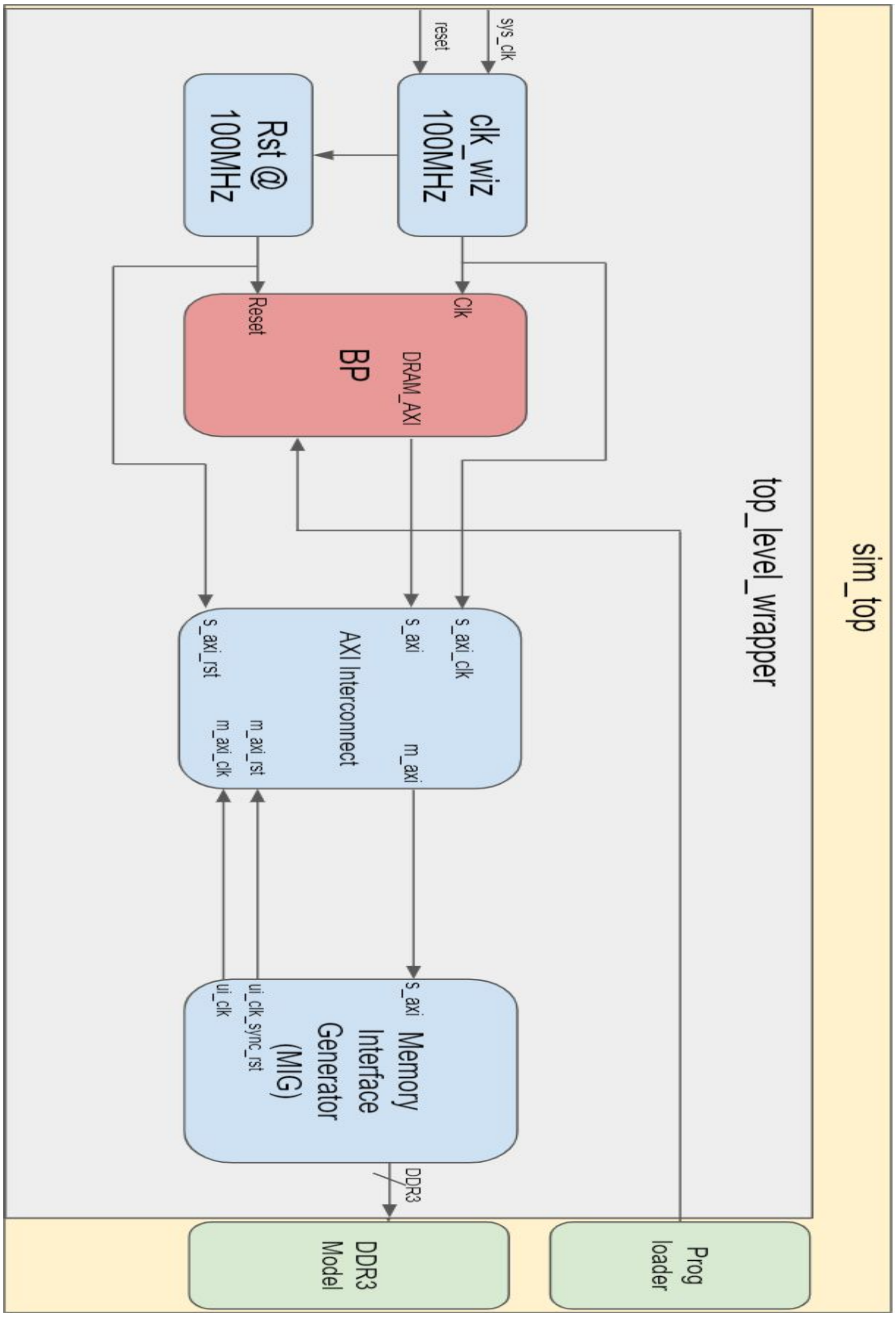
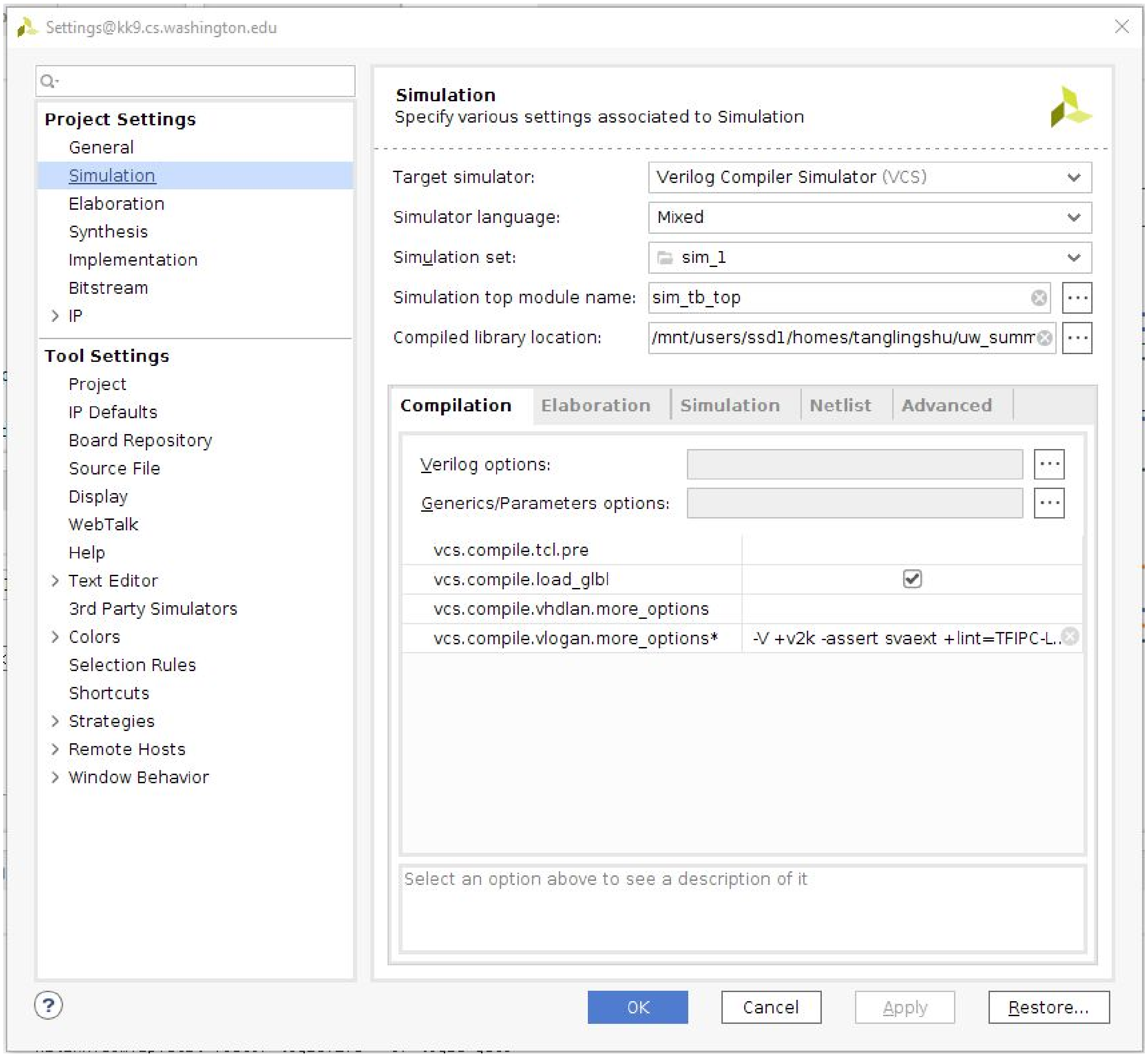


Fig. 8 BlackParrot simulation setup



**Simulation**
Specify various settings associated to Simulation

Target simulator: Verilog Compiler Simulator (VCS)
Simulator language: Mixed
Simulation set: sim_1
Simulation top module name: sim_tb_top
Compiled library location: /mnt/users/ssd1/homes/tanglingshu/uw_summ

Verilog options:
Generics/Parameters options:

| | |
|---|---|
| vcs.compile.tcl.pre | |
| vcs.compile.load_glbl | ☑ |
| vcs.compile.vhdlan.more_options | |
| vcs.compile.vlogan.more_options* | -V +v2k -assert svaext +lint=TFIPC-L.. |

Fig. 9 Simulation settings window

Other reference documents:

IHI0022E_amba_axi_and_ace_protocol_spec
pg267-axi-vip

# TCL Script Draft

```
# set your paths and variables
set bp_ip_path  <path_to_your_bp_ip_location>/bp_packaged_IP
set vcs_bin_path <path_to_vcs_bin>
set vcs_lib_path <path_to_where_you_want_your_compiled_vcs_lib>
set ::env(VCS_HOME) <path_to_your_vcs_home>
set ::env(LM_LICENSE_FILE) <your_license_key>
set proj_name <proj_name_of_your_choice>
set proj_path <path_to_your_proj>

# compile vcs library to use vcs as a simulator in Vivado
compile_simlib -simulator vcs -simulator_exec_path $vcs_bin_path -family all -language
all -library all -dir $vcs_lib_path -no_ip_compile

# project creation
create_project $proj_name $proj_path -part xc7k325tffg900-2
set_property board_part digilentinc.com:genesys2:part0:1.1 [current_project]

# create block diagram design
create_bd_design "design_1"

# 100 MHz Clock
startgroup
create_bd_cell -type ip -vlnv xilinx.com:ip:clk_wiz:6.0 clk_wiz_0
set_property name clk_wiz_100MHz [get_bd_cells clk_wiz_0]
set_property -dict [list CONFIG.CLK_IN1_BOARD_INTERFACE {sys_diff_clock}
CONFIG.RESET_BOARD_INTERFACE {reset} CONFIG.RESET_TYPE
{ACTIVE_LOW} CONFIG.PRIM_SOURCE {Differential_clock_capable_pin}
CONFIG.CLKIN1_JITTER_PS {50.0} CONFIG.MMCM_CLKFBOUT_MULT_F {5.000}
CONFIG.MMCM_CLKIN1_PERIOD {5.000} CONFIG.MMCM_CLKIN2_PERIOD {10.0}
CONFIG.RESET_PORT {resetn} CONFIG.CLKOUT1_JITTER {112.316}
CONFIG.CLKOUT1_PHASE_ERROR {89.971}] [get_bd_cells clk_wiz_100MHz]
apply_bd_automation -rule xilinx.com:bd_rule:board -config { Board_Interface
{sys_diff_clock ( System differential clock ) } Manual_Source {Auto}}  [get_bd_intf_pins
clk_wiz_100MHz/CLK_IN1_D]
apply_bd_automation -rule xilinx.com:bd_rule:board -config { Board_Interface {reset (
Reset ) } Manual_Source {New External Port (ACTIVE_LOW)}}  [get_bd_pins
clk_wiz_100MHz/resetn]
endgroup
```

```
# 100 MHz Processor Reset
startgroup
create_bd_cell -type ip -vlnv xilinx.com:ip:proc_sys_reset:5.0 proc_sys_reset_0
set_property name rst_clk_wiz_100MHz [get_bd_cells proc_sys_reset_0]
set_property -dict [list CONFIG.RESET_BOARD_INTERFACE {reset}] [get_bd_cells
rst_clk_wiz_100MHz]
apply_bd_automation -rule xilinx.com:bd_rule:clkrst -config {Clk
"/clk_wiz_100MHz/clk_out1 (100 MHz)" }  [get_bd_pins
rst_clk_wiz_100MHz/slowest_sync_clk]
apply_bd_automation -rule xilinx.com:bd_rule:board -config { Board_Interface {reset (
Reset ) } Manual_Source {Auto}}  [get_bd_pins rst_clk_wiz_100MHz/ext_reset_in]
connect_bd_net [get_bd_pins clk_wiz_100MHz/locked] [get_bd_pins
rst_clk_wiz_100MHz/dcm_locked]
endgroup

# BlackParrot
set_property  ip_repo_paths  $bp_ip_path [current_project]
update_ip_catalog

startgroup
create_bd_cell -type ip -vlnv bjump.org:user:BlackParrot:0.2020.12.22 BlackParrot_0
set_property -dict [list CONFIG.axi_lite_data_width_p {64}] [get_bd_cells BlackParrot_0]
connect_bd_net [get_bd_pins BlackParrot_0/clk_i] [get_bd_pins
clk_wiz_100MHz/clk_out1]
endgroup

# AXI Interconnect
startgroup
create_bd_cell -type ip -vlnv xilinx.com:ip:axi_interconnect:2.1 axi_interconnect_0
set_property -dict [list CONFIG.NUM_MI {1} CONFIG.ENABLE_ADVANCED_OPTIONS
{1}] [get_bd_cells axi_interconnect_0]
connect_bd_net [get_bd_pins clk_wiz_100MHz/clk_out1] [get_bd_pins
axi_interconnect_0/S00_ACLK]
connect_bd_intf_net [get_bd_intf_pins BlackParrot_0/M_AXI_FULL_DRAM]
-boundary_type upper [get_bd_intf_pins axi_interconnect_0/S00_AXI]
endgroup

# Memory Interface Generator (MIG)
startgroup
```

```
create_bd_cell -type ip -vlnv xilinx.com:ip:mig_7series:4.2 mig_7series_0
apply_board_connection -board_interface "ddr3_sdram" -ip_intf
"mig_7series_0/mig_ddr_interface" -diagram "design_1"
#set_property -name {CONFIG.XML_INPUT_FILE} -value  {mig_a.prj} -objects
[get_bd_cells mig_7series_0]
#set_property -name {CONFIG.RESET_BOARD_INTERFACE} -value  {Custom}
-objects [get_bd_cells mig_7series_0]
#set_property -name {CONFIG.MIG_DONT_TOUCH_PARAM} -value  {Custom}
-objects [get_bd_cells mig_7series_0]
#set_property -name {CONFIG.BOARD_MIG_PARAM} -value  {ddr3_sdram} -objects
[get_bd_cells mig_7series_0]
connect_bd_intf_net -boundary_type upper [get_bd_intf_pins
axi_interconnect_0/M00_AXI] [get_bd_intf_pins mig_7series_0/S_AXI]
connect_bd_net [get_bd_ports reset] [get_bd_pins mig_7series_0/sys_rst]
connect_bd_net [get_bd_pins mig_7series_0/ui_clk] [get_bd_pins
axi_interconnect_0/ACLK]
connect_bd_net [get_bd_pins mig_7series_0/ui_clk] [get_bd_pins
axi_interconnect_0/M00_ACLK]
connect_bd_net [get_bd_pins mig_7series_0/aresetn] [get_bd_pins
inv_logic_gate_2/Res]
endgroup

# Other logic gates and net connection
startgroup
create_bd_cell -type ip -vlnv xilinx.com:ip:util_vector_logic:2.0 util_vector_logic_0
set_property name inv_logic_gate_0 [get_bd_cells util_vector_logic_0]
set_property -dict [list CONFIG.C_SIZE {1} CONFIG.C_OPERATION {not}
CONFIG.LOGO_FILE {data/sym_notgate.png}] [get_bd_cells inv_logic_gate_0]
copy_bd_objs /  [get_bd_cells {inv_logic_gate_0}]
copy_bd_objs /  [get_bd_cells {inv_logic_gate_0}]
create_bd_cell -type ip -vlnv xilinx.com:ip:util_vector_logic:2.0 util_vector_logic_0
set_property name or_logic_gate [get_bd_cells util_vector_logic_0]
set_property -dict [list CONFIG.C_SIZE {1} CONFIG.C_OPERATION {or}
CONFIG.LOGO_FILE {data/sym_orgate.png}] [get_bd_cells or_logic_gate]
connect_bd_net [get_bd_pins mig_7series_0/init_calib_complete] [get_bd_pins
inv_logic_gate_0/Op1]
connect_bd_net [get_bd_pins inv_logic_gate_0/Res] [get_bd_pins or_logic_gate/Op1]
connect_bd_net [get_bd_pins rst_clk_wiz_100MHz/mb_reset] [get_bd_pins
or_logic_gate/Op2]
connect_bd_net [get_bd_pins or_logic_gate/Res] [get_bd_pins BlackParrot_0/reset_i]
connect_bd_net [get_bd_pins inv_logic_gate_1/Op1] [get_bd_pins or_logic_gate/Res]
connect_bd_net [get_bd_pins inv_logic_gate_1/Res] [get_bd_pins
axi_interconnect_0/S00_ARESETN]
connect_bd_net [get_bd_pins mig_7series_0/ui_clk_sync_rst] [get_bd_pins
inv_logic_gate_2/Op1]
connect_bd_net [get_bd_pins inv_logic_gate_2/Res] [get_bd_pins
axi_interconnect_0/ARESETN]
connect_bd_net [get_bd_pins axi_interconnect_0/M00_ARESETN] [get_bd_pins
inv_logic_gate_2/Res]
set_property CONFIG.ASSOCIATED_BUSIF {S_AXI_BP_IO_IN} [get_bd_ports
/clk_100MHz_out]
set_property CONFIG.ASSOCIATED_BUSIF {S_AXI_BP_IO_IN:M_AXI_BP_IO_OUT}
[get_bd_ports /clk_100MHz_out]

endgroup

# IO interface
startgroup
create_bd_intf_port -mode Slave -vlnv xilinx.com:interface:aximm_rtl:1.0
S_AXI_BP_IO_IN
set_property -dict [list CONFIG.CLK_DOMAIN {design_1_clk_wiz_0_0_clk_out1}
CONFIG.PROTOCOL {AXI4LITE} CONFIG.DATA_WIDTH {64} CONFIG.HAS_BURST
{0} CONFIG.HAS_CACHE {0} CONFIG.HAS_LOCK {0} CONFIG.HAS_QOS {0}
CONFIG.HAS_REGION {0}] [get_bd_intf_ports S_AXI_BP_IO_IN]
connect_bd_intf_net [get_bd_intf_ports S_AXI_BP_IO_IN] [get_bd_intf_pins
BlackParrot_0/S_AXI_LITE_IO_IN]
create_bd_intf_port -mode Master -vlnv xilinx.com:interface:aximm_rtl:1.0
M_AXI_BP_IO_OUT
set_property -dict [list CONFIG.CLK_DOMAIN {design_1_clk_wiz_0_0_clk_out1}
CONFIG.PROTOCOL {AXI4LITE} CONFIG.DATA_WIDTH {64} CONFIG.HAS_BURST
{0} CONFIG.HAS_CACHE {0} CONFIG.HAS_LOCK {0} CONFIG.HAS_QOS {0}
CONFIG.HAS_REGION {0}] [get_bd_intf_ports M_AXI_BP_IO_OUT]
connect_bd_intf_net [get_bd_intf_ports M_AXI_BP_IO_OUT] [get_bd_intf_pins
BlackParrot_0/M_AXI_LITE_IO_OUT]
create_bd_port -dir O init_calib_complete
connect_bd_net [get_bd_ports init_calib_complete] [get_bd_pins
mig_7series_0/init_calib_complete]
create_bd_port -dir O -type rst reset_100MHz_out
connect_bd_net [get_bd_ports reset_100MHz_out] [get_bd_pins or_logic_gate/Res]
create_bd_port -dir O -type clk clk_100MHz_out
```

```
connect_bd_net [get_bd_ports clk_100MHz_out] [get_bd_pins
clk_wiz_100MHz/clk_out1]
endgroup

# Excluding memory segment
exclude_bd_addr_seg [get_bd_addr_segs BlackParrot_0/S_AXI_LITE_IO_IN/Reg]
-target_address_space [get_bd_addr_spaces S_AXI_BP_IO_IN]

# Block design cleanup and validation
regenerate_bd_layout
save_bd_design
validate_bd_design

# Create HDL wrapper
startgroup
set dir [get_property DIRECTORY [current_project]]
set name [get_property NAME [current_project]]
set bdFile [get_files ${dir}/${name}.srcs/sources_1/bd/*.bd]
make_wrapper -files [get_files $bdFile] -top
add_files -norecurse [get_files
${dir}/${name}.srcs/sources_1/bd/design_1/hdl/design_1_wrapper.v]
endgroup

# Generate Output Products
export_ip_user_files -of_objects [get_ips design_1_BlackParrot_0_0] -no_script -sync
-force -quiet
generate_target all [get_files $bdFile]
export_simulation -of_objects [get_files
${dir}/project_4.srcs/sources_1/bd/design_1/design_1.bd] -directory
${dir}/project_4.ip_user_files/sim_scripts -ip_user_files_dir ${dir}/project_4.ip_user_files
-ipstatic_source_dir ${dir}/project_4.ip_user_files/ipstatic -lib_map_path [list
{modelsim=${dir}/project_4.cache/compile_simlib/modelsim}
{questa=${dir}/project_4.cache/compile_simlib/questa}
{ies=${dir}/project_4.cache/compile_simlib/ies}
{xcelium=${dir}/project_4.cache/compile_simlib/xcelium} {vcs=${vcs_lib_path}}
{riviera=${dir}/project_4.cache/compile_simlib/riviera}] -use_ip_compiled_libs -force
-quiet

-use_ip_compiled_libs -force -quiet
report_ip_status -name ip_status
```

```
launch_runs -jobs 72 design_1_synth_1

# Setting VCS as default simulator
set_property target_simulator VCS [current_project]
set_property compxlib.vcs_compiled_library_dir $vcs_lib_path [current_project]

# Adding simulation files
set_property SOURCE_SET sources_1 [get_filesets sim_1]
add_files -fileset sim_1 -norecurse [join “
  $bp_ip_path/tb/axi_lite_to_bp_lite_client.sv
  $bp_ip_path/tb/bp_be_pkg.sv
  $bp_ip_path/tb/bp_common_aviary_defines.svh
  $bp_ip_path/tb/bp_common_aviary_pkg.sv
  $bp_ip_path/tb/bp_common_bedrock_if.svh
  $bp_ip_path/tb/bp_common_cache_engine_if.svh
  $bp_ip_path/tb/bp_common_core_if.svh
  $bp_ip_path/tb/bp_common_csr_defines.svh
  $bp_ip_path/tb/bp_common_defines.svh
  $bp_ip_path/tb/bp_common_pkg.sv
  $bp_ip_path/tb/bp_common_rv64_defines.svh
  $bp_ip_path/tb/bp_lite_to_axi_lite_master.sv
  $bp_ip_path/tb/bp_me_pkg.sv
  $bp_ip_path/tb/bp_nonsynth_host.sv
  $bp_ip_path/tb/bp_nonsynth_if_verif.sv
  $bp_ip_path/tb/bp_nonsynth_nbf_loader.sv
  $bp_ip_path/tb/bp_nonsynth_tb_top.sv
  $bp_ip_path/tb/bp_nonsynth_tb_top_wrapper.v
  $bp_ip_path/tb/bsg_buf.sv
  $bp_ip_path/tb/bsg_bus_pack.sv
  $bp_ip_path/tb/bsg_circular_ptr.sv
  $bp_ip_path/tb/bsg_clkgate_optional.sv
  $bp_ip_path/tb/bsg_counter_up_down.sv
  $bp_ip_path/tb/bsg_decode.sv
  $bp_ip_path/tb/bsg_decode_with_v.sv
  $bp_ip_path/tb/bsg_defines.v
  $bp_ip_path/tb/bsg_dff_en.sv
  $bp_ip_path/tb/bsg_dff_reset_en.sv
  $bp_ip_path/tb/bsg_dff_reset.sv
  $bp_ip_path/tb/bsg_dff.sv
  $bp_ip_path/tb/bsg_dlatch.sv
  $bp_ip_path/tb/bsg_fifo_1r1w_small_hardened.sv
  $bp_ip_path/tb/bsg_fifo_1r1w_small.sv
  $bp_ip_path/tb/bsg_fifo_1r1w_small_unhardened.sv
  $bp_ip_path/tb/bsg_fifo_tracker.sv
  $bp_ip_path/tb/bsg_flow_counter.sv
  $bp_ip_path/tb/bsg_mem_1r1w.sv
  $bp_ip_path/tb/bsg_mem_1r1w_sync.sv
  $bp_ip_path/tb/bsg_mem_1r1w_sync_synth.sv
  $bp_ip_path/tb/bsg_mem_1r1w_synth.sv
  $bp_ip_path/tb/bsg_muxi2_gatestack.sv
  $bp_ip_path/tb/bsg_mux.sv
  $bp_ip_path/tb/bsg_nand.sv
  $bp_ip_path/tb/bsg_noc_links.vh
  $bp_ip_path/tb/bsg_noc_pkg.v
  $bp_ip_path/tb/bsg_nonsynth_test_rom.sv
  $bp_ip_path/tb/bsg_nor3.sv
  $bp_ip_path/tb/bsg_reduce.sv
  $bp_ip_path/tb/bsg_rotate_right.sv
  $bp_ip_path/tb/bsg_strobe.sv
  $bp_ip_path/tb/bsg_two_fifo.sv
  $bp_ip_path/tb/bsg_xnor.sv
  $bp_ip_path/tb/ddr3_model_parameters.vh
  $bp_ip_path/tb/ddr3_model.sv
  $bp_ip_path/tb/sim_tb_top.v
  $bp_ip_path/tb/wiredly.v
  $bp_ip_path/tb/bootrom.mem
  $bp_ip_path/tb/mem_init.txt
  $bp_ip_path/tb/prog.nbf
“]
set_property file_type SystemVerilog [get_files  $bp_ip_path/tb/bsg_noc_pkg.v]
set_property file_type SystemVerilog [get_files  $bp_ip_path/tb/sim_tb_top.v]
set_property file_type {Verilog Header} [get_files  $bp_ip_path/tb/bsg_defines.v]
update_compile_order -fileset sim_1

# Setting VCS simulation flags
set_property -name {vcs.compile.vlogan.more_options} -value {-V +v2k -sverilog -assert
svaext +lint=TFIPC-L} -objects [get_filesets sim_1]
set_property -name {vcs.elaborate.vcs.more_options} -value {-sverilog -assert svaext
-lca +lint=TFIPC-L +noportcoerce} -objects [get_filesets sim_1]
set_property -name {vcs.simulate.runtime} -value {1ms} -objects [get_filesets sim_1]
set_property -name {vcs.simulate.log_all_signals} -value {true} -objects [get_filesets sim_1]

# Launch simulation
launch_simulation -install_path $vcs_bin_path

########################################################################
############################## IP generation ##############################
########################################################################

# Create project
set ip_proj_name <ip_proj_name_of_your_choice>
set ip_proj_path <path_to_your_ip_proj>
set bp_ip_path  <path_to_your_bp_ip_location>
create_project $ip_proj_name $ip_proj_path -part xc7k325tffg900-2
set_property board_part digilentinc.com:genesys2:part0:1.1 [current_project]

# Turn off automatic hierarchy updates and automatic compilation order update
# If adding all the source file causes Vivado to freeze, it is suggested that you use the
# following command and perform manual hierarchy and compilation order update after
# adding all of the design sources
# set_property source_mgmt_mode None [current_project]

# Add design sources
startgroup
add_files -norecurse [join “
  $bp_ip_path/src/axi_lite_to_bp_lite_client.sv
  $bp_ip_path/src/bp_be_bypass.sv
  $bp_ip_path/src/bp_be_calculator_top.sv
  $bp_ip_path/src/bp_be_csr.sv
  $bp_ip_path/src/bp_be_ctl_defines.svh
  $bp_ip_path/src/bp_be_dcache_decoder.sv
  $bp_ip_path/src/bp_be_dcache_pipeline.svh
  $bp_ip_path/src/bp_be_dcache_pkt.svh
  $bp_ip_path/src/bp_be_dcache.sv
  $bp_ip_path/src/bp_be_dcache_tag_info.svh
  $bp_ip_path/src/bp_be_dcache_wbuf_entry.svh
  $bp_ip_path/src/bp_be_dcache_wbuf_queue.sv
  $bp_ip_path/src/bp_be_dcache_wbuf.sv
  $bp_ip_path/src/bp_be_detector.sv
```

```
$bp_ip_path/src/bp_be_director.sv
$bp_ip_path/src/bp_be_fp_to_rec.sv
$bp_ip_path/src/bp_be_instr_decoder.sv
$bp_ip_path/src/bp_be_internal_if_defines.svh
$bp_ip_path/src/bp_be_issue_queue.sv
$bp_ip_path/src/bp_be_mem_defines.svh
$bp_ip_path/src/bp_be_pipe_aux.sv
$bp_ip_path/src/bp_be_pipe_ctl.sv
$bp_ip_path/src/bp_be_pipe_fma.sv
$bp_ip_path/src/bp_be_pipe_int.sv
$bp_ip_path/src/bp_be_pipe_long.sv
$bp_ip_path/src/bp_be_pipe_mem.sv
$bp_ip_path/src/bp_be_pipe_sys.sv
$bp_ip_path/src/bp_be_pkg.sv
$bp_ip_path/src/bp_be_ptw.sv
$bp_ip_path/src/bp_be_rec_to_fp.sv
$bp_ip_path/src/bp_be_regfile.sv
$bp_ip_path/src/bp_be_scheduler.sv
$bp_ip_path/src/bp_be_top.sv
$bp_ip_path/src/bp_burst_to_lite.sv
$bp_ip_path/src/bp_cce_inst.svh
$bp_ip_path/src/bp_cce_loopback.sv
$bp_ip_path/src/bp_cfg.sv
$bp_ip_path/src/bp_clint_slice.sv
$bp_ip_path/src/bp_common_aviary_defines.svh
$bp_ip_path/src/bp_common_aviary_pkg.sv
$bp_ip_path/src/bp_common_bedrock_if.svh
$bp_ip_path/src/bp_common_cache_engine_if.svh
$bp_ip_path/src/bp_common_core_if.svh
$bp_ip_path/src/bp_common_csr_defines.svh
$bp_ip_path/src/bp_common_defines.svh
$bp_ip_path/src/bp_common_pkg.sv
$bp_ip_path/src/bp_common_rv64_defines.svh
$bp_ip_path/src/bp_core_minimal.sv
$bp_ip_path/src/bp_fe_bht.sv
$bp_ip_path/src/bp_fe_btb.sv
$bp_ip_path/src/bp_fe_defines.svh
$bp_ip_path/src/bp_fe_icache.sv
$bp_ip_path/src/bp_fe_icache.svh
$bp_ip_path/src/bp_fe_instr_scan.sv
```

```
$bp_ip_path/src/bp_fe_pc_gen.sv
$bp_ip_path/src/bp_fe_pkg.sv
$bp_ip_path/src/bp_fe_top.sv
$bp_ip_path/src/bp_lite_to_axi_lite_master.sv
$bp_ip_path/src/bp_lite_to_burst.sv
$bp_ip_path/src/bp_logo.png
$bp_ip_path/src/bp_me_cache_slice.sv
$bp_ip_path/src/bp_me_cce_to_cache.sv
$bp_ip_path/src/bp_me_cord_to_id.sv
$bp_ip_path/src/bp_mem_to_axi_master.sv
$bp_ip_path/src/bp_mem_wormhole.svh
$bp_ip_path/src/bp_me_pkg.sv
$bp_ip_path/src/bp_mmu.sv
$bp_ip_path/src/bp_pma.sv
$bp_ip_path/src/bp_tlb.sv
$bp_ip_path/src/bp_uce.sv
$bp_ip_path/src/bp_unicore_axi_wrapper_top_timing_ooc.xdc
$bp_ip_path/src/bp_unicore_axi_wrapper_top_timing.xdc
$bp_ip_path/src/bp_unicore.sv
$bp_ip_path/src/bp_unicore_with_axi_wrapper.sv
$bp_ip_path/src/bp_unicore_with_axi_wrapper_top.v
$bp_ip_path/src/compareRecFN.v
$bp_ip_path/src/divSqrtRecFN_small.v
$bp_ip_path/src/fNToRecFN.v
$bp_ip_path/src/HardFloat_consts.vi
$bp_ip_path/src/HardFloat_localFuncs.vi
$bp_ip_path/src/HardFloat_primitives.v
$bp_ip_path/src/HardFloat_rawFN.v
$bp_ip_path/src/HardFloat_specialize.v
$bp_ip_path/src/HardFloat_specialize.vi
$bp_ip_path/src/iNToRecFN.v
$bp_ip_path/src/isSigNaNRecFN.v
$bp_ip_path/src/mulAddRecFN.v
$bp_ip_path/src/recFNToFN.v
$bp_ip_path/src/recFNToIN.v
$bp_ip_path/src/recFNToRecFN.v
$bp_ip_path/src/bsg_adder_cin.sv
$bp_ip_path/src/bsg_adder_one_hot.sv
$bp_ip_path/src/bsg_arb_fixed.sv
$bp_ip_path/src/bsg_buf.sv
```

```
$bp_ip_path/src/bsg_bus_pack.sv
$bp_ip_path/src/bsg_cache_decode.sv
$bp_ip_path/src/bsg_cache_dma.sv
$bp_ip_path/src/bsg_cache_miss.sv
$bp_ip_path/src/bsg_cache_pkg.sv
$bp_ip_path/src/bsg_cache_sbuf_queue.sv
$bp_ip_path/src/bsg_cache_sbuf.sv
$bp_ip_path/src/bsg_cache.sv
$bp_ip_path/src/bsg_cam_1r1w_replacement.sv
$bp_ip_path/src/bsg_cam_1r1w.sv
$bp_ip_path/src/bsg_cam_1r1w_sync.sv
$bp_ip_path/src/bsg_cam_1r1w_tag_array.sv
$bp_ip_path/src/bsg_circular_ptr.sv
$bp_ip_path/src/bsg_clkgate_optional.sv
$bp_ip_path/src/bsg_counter_clear_up.sv
$bp_ip_path/src/bsg_counter_set_en.sv
$bp_ip_path/src/bsg_counter_up_down.sv
$bp_ip_path/src/bsg_crossbar_o_by_i.sv
$bp_ip_path/src/bsg_decode.sv
$bp_ip_path/src/bsg_decode_with_v.sv
$bp_ip_path/src/bsg_defines.v
$bp_ip_path/src/bsg_dff_chain.sv
$bp_ip_path/src/bsg_dff_en_bypass.sv
$bp_ip_path/src/bsg_dff_en.sv
$bp_ip_path/src/bsg_dff_reset_en_bypass.sv
$bp_ip_path/src/bsg_dff_reset_en.sv
$bp_ip_path/src/bsg_dff_reset_set_clear.sv
$bp_ip_path/src/bsg_dff_reset.sv
$bp_ip_path/src/bsg_dff.sv
$bp_ip_path/src/bsg_dlatch.sv
$bp_ip_path/src/bsg_encode_one_hot.sv
$bp_ip_path/src/bsg_expand_bitmask.sv
$bp_ip_path/src/bsg_fifo_1r1w_small_hardened.sv
$bp_ip_path/src/bsg_fifo_1r1w_small.sv
$bp_ip_path/src/bsg_fifo_1r1w_small_unhardened.sv
$bp_ip_path/src/bsg_fifo_tracker.sv
$bp_ip_path/src/bsg_flow_counter.sv
$bp_ip_path/src/bsg_idiv_iterative_controller.sv
$bp_ip_path/src/bsg_idiv_iterative.sv
$bp_ip_path/src/bsg_lru_pseudo_tree_decode.sv
```

```
$bp_ip_path/src/bsg_lru_pseudo_tree_encode.sv
$bp_ip_path/src/bsg_mem_1r1w_one_hot.sv
$bp_ip_path/src/bsg_mem_1r1w.sv
$bp_ip_path/src/bsg_mem_1r1w_sync.sv
$bp_ip_path/src/bsg_mem_1r1w_sync_synth.sv
$bp_ip_path/src/bsg_mem_1r1w_synth.sv
$bp_ip_path/src/bsg_mem_1rw_sync_mask_write_bit.sv
$bp_ip_path/src/bsg_mem_1rw_sync_mask_write_bit_synth.sv
$bp_ip_path/src/bsg_mem_1rw_sync_mask_write_byte.sv
$bp_ip_path/src/bsg_mem_1rw_sync_mask_write_byte_synth.sv
$bp_ip_path/src/bsg_mem_1rw_sync.sv
$bp_ip_path/src/bsg_mem_1rw_sync_synth.sv
$bp_ip_path/src/bsg_mem_2r1w_sync.sv
$bp_ip_path/src/bsg_mem_2r1w_sync_synth.sv
$bp_ip_path/src/bsg_mem_3r1w_sync.sv
$bp_ip_path/src/bsg_mem_3r1w_sync_synth.sv
$bp_ip_path/src/bsg_mux_bitwise.sv
$bp_ip_path/src/bsg_muxi2_gatestack.sv
$bp_ip_path/src/bsg_mux_one_hot.sv
$bp_ip_path/src/bsg_mux_segmented.sv
$bp_ip_path/src/bsg_mux.sv
$bp_ip_path/src/bsg_nand.sv
$bp_ip_path/src/bsg_noc_links.vh
$bp_ip_path/src/bsg_noc_pkg.v
$bp_ip_path/src/bsg_nor2.sv
$bp_ip_path/src/bsg_nor3.sv
$bp_ip_path/src/bsg_one_fifo.sv
$bp_ip_path/src/bsg_parallel_in_serial_out_dynamic.sv
$bp_ip_path/src/bsg_priority_encode_one_hot_out.sv
$bp_ip_path/src/bsg_priority_encode.sv
$bp_ip_path/src/bsg_reduce.sv
$bp_ip_path/src/bsg_rotate_left.sv
$bp_ip_path/src/bsg_rotate_right.sv
$bp_ip_path/src/bsg_scan.sv
$bp_ip_path/src/bsg_serial_in_parallel_out_dynamic.sv
$bp_ip_path/src/bsg_shift_reg.sv
$bp_ip_path/src/bsg_strobe.sv
$bp_ip_path/src/bsg_two_fifo.sv
$bp_ip_path/src/bsg_wormhole_router_pkg.sv
$bp_ip_path/src/bsg_wormhole_router.vh
```

```
  $bp_ip_path/src/bsg_xnor.sv
”]

set_property file_type SystemVerilog [get_files [join “
  $bp_ip_path/src/bsg_noc_pkg.v
  $bp_ip_path/src/divSqrtRecFN_small.v
“]]

set_property top bp_unicore_with_axi_wrapper_top [current_fileset]
set_property top bp_unicore_with_axi_wrapper_top [get_filesets sim_1]
set_property top_lib xil_defaultlib [get_filesets sim_1]
endgroup

# run the following if you turned off the automatic hierarchy update and compilation
# order update
# set_property source_mgmt_mode All [current_project]
# update_compile_order -fileset sources_1
# update_compile_order -fileset sources_1

ipx::package_project -root_dir $bp_ip_path -vendor user.org -library user -taxonomy /UserIP -force

# IP package identification
startgroup
set_property vendor bjump.org [ipx::current_core]
set_property name BlackParrot [ipx::current_core]
set_property version 0.1 [ipx::current_core]
set_property display_name BlackParrot [ipx::current_core]
set_property description BlackParrot_v0_1_11d0890 [ipx::current_core]
set_property vendor_display_name {Bespoke Silicon Group} [ipx::current_core]
set_property company_url {https://github.com/black-parrot/black-parrot} [ipx::current_core]
set_property taxonomy {/Embedded_Processing/Processor /UserIP} [ipx::current_core]
endgroup

# IP package file groups (adding logo and product guide)
startgroup
ipx::add_file_group -type product_guide {} [ipx::current_core]
ipx::add_file $bp_ip_path/doc/BP_Unicore_Xilinx_IP_Product_Guide.pdf [ipx::get_file_groups xilinx_productguide -of_objects [ipx::current_core]]
```

```
set_property type pdf [ipx::get_files doc/BP_Unicore_Xilinx_IP_Product_Guide.pdf
-of_objects [ipx::get_file_groups xilinx_productguide -of_objects [ipx::current_core]]]
ipx::add_file_group -type utility {} [ipx::current_core]
ipx::add_file doc/bp_logo_small.png [ipx::get_file_groups xilinx_utilityxitfiles -of_objects
[ipx::current_core]]
set_property type image [ipx::get_files doc/bp_logo_small.png -of_objects
[ipx::get_file_groups xilinx_utilityxitfiles -of_objects [ipx::current_core]]]
endgroup

# IP package parameter customization
startgroup
set_property display_name {BP_PARAMS_P} [ipgui::get_guiparamspec -name
"bp_params_p" -component [ipx::current_core] ]
set_property tooltip {BlackParrot Configuration} [ipgui::get_guiparamspec -name
"bp_params_p" -component [ipx::current_core] ]
set_property widget {textEdit} [ipgui::get_guiparamspec -name "bp_params_p"
-component [ipx::current_core] ]
set_property value_validation_type range_long [ipx::get_user_parameters
bp_params_p -of_objects [ipx::current_core]]
set_property value_validation_range_minimum 0 [ipx::get_user_parameters
bp_params_p -of_objects [ipx::current_core]]
set_property value_validation_range_maximum 9 [ipx::get_user_parameters
bp_params_p -of_objects [ipx::current_core]]

set_property display_name {AXI_LITE_ADDR_WIDTH_P} [ipgui::get_guiparamspec
-name "axi_lite_addr_width_p" -component [ipx::current_core] ]
set_property tooltip {Address has to be 32 or 64} [ipgui::get_guiparamspec -name
"axi_lite_addr_width_p" -component [ipx::current_core] ]
set_property widget {comboBox} [ipgui::get_guiparamspec -name
"axi_lite_addr_width_p" -component [ipx::current_core] ]
set_property value 64 [ipx::get_user_parameters axi_lite_addr_width_p -of_objects
[ipx::current_core]]
set_property value 64 [ipx::get_hdl_parameters axi_lite_addr_width_p -of_objects
[ipx::current_core]]
set_property value_validation_type list [ipx::get_user_parameters axi_lite_addr_width_p
-of_objects [ipx::current_core]]
set_property value_validation_list {32 64} [ipx::get_user_parameters
axi_lite_addr_width_p -of_objects [ipx::current_core]]
```

```
set_property display_name {AXI_LITE_DATA_WIDTH_P} [ipgui::get_guiparamspec -name "axi_lite_data_width_p" -component [ipx::current_core] ]
set_property tooltip {AXI_LITE_DATA_WIDTH_P} [ipgui::get_guiparamspec -name "axi_lite_data_width_p" -component [ipx::current_core] ]
set_property widget {textEdit} [ipgui::get_guiparamspec -name "axi_lite_data_width_p" -component [ipx::current_core] ]

set_property enablement_value false [ipx::get_user_parameters axi_lite_strb_width_lp -of_objects [ipx::current_core]]
set_property value_tcl_expr {$axi_lite_data_width_p/8} [ipx::get_user_parameters axi_lite_strb_width_lp -of_objects [ipx::current_core]]
ipgui::remove_param -component [ipx::current_core] [ipgui::get_guiparamspec -name "axi_lite_strb_width_lp" -component [ipx::current_core]]

set_property display_name {AXI_FULL_ADDR_WIDTH_P} [ipgui::get_guiparamspec -name "axi_full_addr_width_p" -component [ipx::current_core] ]
set_property tooltip {Address width for DRAM, up to 64-bits} [ipgui::get_guiparamspec -name "axi_full_addr_width_p" -component [ipx::current_core] ]
set_property widget {textEdit} [ipgui::get_guiparamspec -name "axi_full_addr_width_p" -component [ipx::current_core] ]

set_property display_name {AXI_FULL_DATA_WIDTH_P} [ipgui::get_guiparamspec -name "axi_full_data_width_p" -component [ipx::current_core] ]
set_property tooltip {Data width for DRAM} [ipgui::get_guiparamspec -name "axi_full_data_width_p" -component [ipx::current_core] ]
set_property widget {comboBox} [ipgui::get_guiparamspec -name "axi_full_data_width_p" -component [ipx::current_core] ]
set_property value 64 [ipx::get_user_parameters axi_full_data_width_p -of_objects [ipx::current_core]]
set_property value 64 [ipx::get_hdl_parameters axi_full_data_width_p -of_objects [ipx::current_core]]
set_property value_validation_type list [ipx::get_user_parameters axi_full_data_width_p -of_objects [ipx::current_core]]
set_property value_validation_list {32 64 128 256 512 1024} [ipx::get_user_parameters axi_full_data_width_p -of_objects [ipx::current_core]]

set_property display_name {AXI_FULL_ID_WIDTH_P} [ipgui::get_guiparamspec -name "axi_full_id_width_p" -component [ipx::current_core] ]
set_property tooltip {number of devices supported} [ipgui::get_guiparamspec -name "axi_full_id_width_p" -component [ipx::current_core] ]
set_property widget {textEdit} [ipgui::get_guiparamspec -name "axi_full_id_width_p"
-component [ipx::current_core] ]

set_property display_name {AXI_FULL_BURST_TYPE_P} [ipgui::get_guiparamspec
-name "axi_full_burst_type_p" -component [ipx::current_core] ]
set_property tooltip {Various AXI Burst Type} [ipgui::get_guiparamspec -name
"axi_full_burst_type_p" -component [ipx::current_core] ]
set_property widget {comboBox} [ipgui::get_guiparamspec -name
"axi_full_burst_type_p" -component [ipx::current_core] ]
set_property value_validation_type list [ipx::get_user_parameters axi_full_burst_type_p
-of_objects [ipx::current_core]]
set_property value_validation_list {00 01 10 11} [ipx::get_user_parameters
axi_full_burst_type_p -of_objects [ipx::current_core]]

set_property enablement_value false [ipx::get_user_parameters axi_full_strb_width_lp
-of_objects [ipx::current_core]]
set_property value_tcl_expr {$axi_full_data_width_p/8} [ipx::get_user_parameters
axi_full_strb_width_lp -of_objects [ipx::current_core]]
ipgui::remove_param -component [ipx::current_core] [ipgui::get_guiparamspec -name
"axi_full_strb_width_lp" -component [ipx::current_core]]
endgroup

# IP ports and interface
startgroup
ipx::add_bus_interface Clk [ipx::current_core]
set_property abstraction_type_vlnv xilinx.com:signal:clock_rtl:1.0
[ipx::get_bus_interfaces Clk -of_objects [ipx::current_core]]
set_property bus_type_vlnv xilinx.com:signal:clock:1.0 [ipx::get_bus_interfaces Clk
-of_objects [ipx::current_core]]
set_property display_name Clk [ipx::get_bus_interfaces Clk -of_objects
[ipx::current_core]]
set_property description {Main processor clock} [ipx::get_bus_interfaces Clk -of_objects
[ipx::current_core]]
ipx::add_bus_parameter FREQ_HZ [ipx::get_bus_interfaces Clk -of_objects
[ipx::current_core]]
ipx::add_port_map CLK [ipx::get_bus_interfaces Clk -of_objects [ipx::current_core]]
set_property physical_name clk_i [ipx::get_port_maps CLK -of_objects
[ipx::get_bus_interfaces Clk -of_objects [ipx::current_core]]]

ipx::add_bus_interface M_AXI_FULL_DRAM [ipx::current_core]
```

```
set_property abstraction_type_vlnv xilinx.com:interface:aximm_rtl:1.0
[ipx::get_bus_interfaces M_AXI_FULL_DRAM -of_objects [ipx::current_core]]
set_property bus_type_vlnv xilinx.com:interface:aximm:1.0 [ipx::get_bus_interfaces
M_AXI_FULL_DRAM -of_objects [ipx::current_core]]
set_property interface_mode master [ipx::get_bus_interfaces M_AXI_FULL_DRAM
-of_objects [ipx::current_core]]
set_property display_name M_AXI_FULL_DRAM [ipx::get_bus_interfaces
M_AXI_FULL_DRAM -of_objects [ipx::current_core]]
set_property description {AXI DRAM} [ipx::get_bus_interfaces M_AXI_FULL_DRAM
-of_objects [ipx::current_core]]
ipx::add_bus_parameter NUM_READ_OUTSTANDING [ipx::get_bus_interfaces
M_AXI_FULL_DRAM -of_objects [ipx::current_core]]
ipx::add_bus_parameter NUM_WRITE_OUTSTANDING [ipx::get_bus_interfaces
M_AXI_FULL_DRAM -of_objects [ipx::current_core]]
ipx::add_port_map WLAST [ipx::get_bus_interfaces M_AXI_FULL_DRAM -of_objects
[ipx::current_core]]
set_property physical_name m_axi_wlast_o [ipx::get_port_maps WLAST -of_objects
[ipx::get_bus_interfaces M_AXI_FULL_DRAM -of_objects [ipx::current_core]]]
ipx::add_port_map BREADY [ipx::get_bus_interfaces M_AXI_FULL_DRAM -of_objects
[ipx::current_core]]
set_property physical_name m_axi_bready_o [ipx::get_port_maps BREADY -of_objects
[ipx::get_bus_interfaces M_AXI_FULL_DRAM -of_objects [ipx::current_core]]]
ipx::add_port_map AWLEN [ipx::get_bus_interfaces M_AXI_FULL_DRAM -of_objects
[ipx::current_core]]
set_property physical_name m_axi_awlen_o [ipx::get_port_maps AWLEN -of_objects
[ipx::get_bus_interfaces M_AXI_FULL_DRAM -of_objects [ipx::current_core]]]
ipx::add_port_map AWQOS [ipx::get_bus_interfaces M_AXI_FULL_DRAM -of_objects
[ipx::current_core]]
set_property physical_name m_axi_awqos_o [ipx::get_port_maps AWQOS -of_objects
[ipx::get_bus_interfaces M_AXI_FULL_DRAM -of_objects [ipx::current_core]]]
ipx::add_port_map AWREADY [ipx::get_bus_interfaces M_AXI_FULL_DRAM
-of_objects [ipx::current_core]]
set_property physical_name m_axi_awready_i [ipx::get_port_maps AWREADY
-of_objects [ipx::get_bus_interfaces M_AXI_FULL_DRAM -of_objects
[ipx::current_core]]]
ipx::add_port_map ARBURST [ipx::get_bus_interfaces M_AXI_FULL_DRAM
-of_objects [ipx::current_core]]
set_property physical_name m_axi_arburst_o [ipx::get_port_maps ARBURST
-of_objects [ipx::get_bus_interfaces M_AXI_FULL_DRAM -of_objects
[ipx::current_core]]]
```

```
ipx::add_port_map AWPROT [ipx::get_bus_interfaces M_AXI_FULL_DRAM -of_objects
[ipx::current_core]]
set_property physical_name m_axi_awprot_o [ipx::get_port_maps AWPROT
-of_objects [ipx::get_bus_interfaces M_AXI_FULL_DRAM -of_objects
[ipx::current_core]]]
ipx::add_port_map RRESP [ipx::get_bus_interfaces M_AXI_FULL_DRAM -of_objects
[ipx::current_core]]
set_property physical_name m_axi_rresp_i [ipx::get_port_maps RRESP -of_objects
[ipx::get_bus_interfaces M_AXI_FULL_DRAM -of_objects [ipx::current_core]]]
ipx::add_port_map ARPROT [ipx::get_bus_interfaces M_AXI_FULL_DRAM -of_objects
[ipx::current_core]]
set_property physical_name m_axi_arprot_o [ipx::get_port_maps ARPROT -of_objects
[ipx::get_bus_interfaces M_AXI_FULL_DRAM -of_objects [ipx::current_core]]]
ipx::add_port_map RVALID [ipx::get_bus_interfaces M_AXI_FULL_DRAM -of_objects
[ipx::current_core]]
set_property physical_name m_axi_rvalid_i [ipx::get_port_maps RVALID -of_objects
[ipx::get_bus_interfaces M_AXI_FULL_DRAM -of_objects [ipx::current_core]]]
ipx::add_port_map AWID [ipx::get_bus_interfaces M_AXI_FULL_DRAM -of_objects
[ipx::current_core]]
set_property physical_name m_axi_awid_o [ipx::get_port_maps AWID -of_objects
[ipx::get_bus_interfaces M_AXI_FULL_DRAM -of_objects [ipx::current_core]]]
ipx::add_port_map RLAST [ipx::get_bus_interfaces M_AXI_FULL_DRAM -of_objects
[ipx::current_core]]
set_property physical_name m_axi_rlast_i [ipx::get_port_maps RLAST -of_objects
[ipx::get_bus_interfaces M_AXI_FULL_DRAM -of_objects [ipx::current_core]]]
ipx::add_port_map ARID [ipx::get_bus_interfaces M_AXI_FULL_DRAM -of_objects
[ipx::current_core]]
set_property physical_name m_axi_arid_o [ipx::get_port_maps ARID -of_objects
[ipx::get_bus_interfaces M_AXI_FULL_DRAM -of_objects [ipx::current_core]]]
ipx::add_port_map AWCACHE [ipx::get_bus_interfaces M_AXI_FULL_DRAM
-of_objects [ipx::current_core]]
set_property physical_name m_axi_awcache_o [ipx::get_port_maps AWCACHE
-of_objects [ipx::get_bus_interfaces M_AXI_FULL_DRAM -of_objects
[ipx::current_core]]]
ipx::add_port_map WREADY [ipx::get_bus_interfaces M_AXI_FULL_DRAM -of_objects
[ipx::current_core]]
set_property physical_name m_axi_wready_i [ipx::get_port_maps WREADY -of_objects
[ipx::get_bus_interfaces M_AXI_FULL_DRAM -of_objects [ipx::current_core]]]
ipx::add_port_map WSTRB [ipx::get_bus_interfaces M_AXI_FULL_DRAM -of_objects
[ipx::current_core]]
```

```
set_property physical_name m_axi_wstrb_o [ipx::get_port_maps WSTRB -of_objects
[ipx::get_bus_interfaces M_AXI_FULL_DRAM -of_objects [ipx::current_core]]]
ipx::add_port_map BRESP [ipx::get_bus_interfaces M_AXI_FULL_DRAM -of_objects
[ipx::current_core]]
set_property physical_name m_axi_bresp_i [ipx::get_port_maps BRESP -of_objects
[ipx::get_bus_interfaces M_AXI_FULL_DRAM -of_objects [ipx::current_core]]]
ipx::add_port_map BID [ipx::get_bus_interfaces M_AXI_FULL_DRAM -of_objects
[ipx::current_core]]
set_property physical_name m_axi_bid_i [ipx::get_port_maps BID -of_objects
[ipx::get_bus_interfaces M_AXI_FULL_DRAM -of_objects [ipx::current_core]]]
ipx::add_port_map ARLEN [ipx::get_bus_interfaces M_AXI_FULL_DRAM -of_objects
[ipx::current_core]]
set_property physical_name m_axi_arlen_o [ipx::get_port_maps ARLEN -of_objects
[ipx::get_bus_interfaces M_AXI_FULL_DRAM -of_objects [ipx::current_core]]]
ipx::add_port_map ARQOS [ipx::get_bus_interfaces M_AXI_FULL_DRAM -of_objects
[ipx::current_core]]
set_property physical_name m_axi_arqos_o [ipx::get_port_maps ARQOS -of_objects
[ipx::get_bus_interfaces M_AXI_FULL_DRAM -of_objects [ipx::current_core]]]
ipx::add_port_map RDATA [ipx::get_bus_interfaces M_AXI_FULL_DRAM -of_objects
[ipx::current_core]]
set_property physical_name m_axi_rdata_i [ipx::get_port_maps RDATA -of_objects
[ipx::get_bus_interfaces M_AXI_FULL_DRAM -of_objects [ipx::current_core]]]
ipx::add_port_map ARCACHE [ipx::get_bus_interfaces M_AXI_FULL_DRAM
-of_objects [ipx::current_core]]
set_property physical_name m_axi_arcache_o [ipx::get_port_maps ARCACHE
-of_objects [ipx::get_bus_interfaces M_AXI_FULL_DRAM -of_objects
[ipx::current_core]]]
ipx::add_port_map BVALID [ipx::get_bus_interfaces M_AXI_FULL_DRAM -of_objects
[ipx::current_core]]
set_property physical_name m_axi_bvalid_i [ipx::get_port_maps BVALID -of_objects
[ipx::get_bus_interfaces M_AXI_FULL_DRAM -of_objects [ipx::current_core]]]
ipx::add_port_map RREADY [ipx::get_bus_interfaces M_AXI_FULL_DRAM -of_objects
[ipx::current_core]]
set_property physical_name m_axi_rready_o [ipx::get_port_maps RREADY -of_objects
[ipx::get_bus_interfaces M_AXI_FULL_DRAM -of_objects [ipx::current_core]]]
ipx::add_port_map AWVALID [ipx::get_bus_interfaces M_AXI_FULL_DRAM -of_objects
[ipx::current_core]]
set_property physical_name m_axi_awvalid_o [ipx::get_port_maps AWVALID
-of_objects [ipx::get_bus_interfaces M_AXI_FULL_DRAM -of_objects
[ipx::current_core]]]
```

```
ipx::add_port_map ARSIZE [ipx::get_bus_interfaces M_AXI_FULL_DRAM -of_objects
[ipx::current_core]]
set_property physical_name m_axi_arsize_o [ipx::get_port_maps ARSIZE -of_objects
[ipx::get_bus_interfaces M_AXI_FULL_DRAM -of_objects [ipx::current_core]]]
ipx::add_port_map WDATA [ipx::get_bus_interfaces M_AXI_FULL_DRAM -of_objects
[ipx::current_core]]
set_property physical_name m_axi_wdata_o [ipx::get_port_maps WDATA -of_objects
[ipx::get_bus_interfaces M_AXI_FULL_DRAM -of_objects [ipx::current_core]]]
ipx::add_port_map AWSIZE [ipx::get_bus_interfaces M_AXI_FULL_DRAM -of_objects
[ipx::current_core]]
set_property physical_name m_axi_awsize_o [ipx::get_port_maps AWSIZE -of_objects
[ipx::get_bus_interfaces M_AXI_FULL_DRAM -of_objects [ipx::current_core]]]
ipx::add_port_map RID [ipx::get_bus_interfaces M_AXI_FULL_DRAM -of_objects
[ipx::current_core]]
set_property physical_name m_axi_rid_i [ipx::get_port_maps RID -of_objects
[ipx::get_bus_interfaces M_AXI_FULL_DRAM -of_objects [ipx::current_core]]]
ipx::add_port_map ARADDR [ipx::get_bus_interfaces M_AXI_FULL_DRAM -of_objects
[ipx::current_core]]
set_property physical_name m_axi_araddr_o [ipx::get_port_maps ARADDR -of_objects
[ipx::get_bus_interfaces M_AXI_FULL_DRAM -of_objects [ipx::current_core]]]
ipx::add_port_map WID [ipx::get_bus_interfaces M_AXI_FULL_DRAM -of_objects
[ipx::current_core]]
set_property physical_name m_axi_wid_o [ipx::get_port_maps WID -of_objects
[ipx::get_bus_interfaces M_AXI_FULL_DRAM -of_objects [ipx::current_core]]]
ipx::add_port_map AWADDR [ipx::get_bus_interfaces M_AXI_FULL_DRAM -of_objects
[ipx::current_core]]
set_property physical_name m_axi_awaddr_o [ipx::get_port_maps AWADDR
-of_objects [ipx::get_bus_interfaces M_AXI_FULL_DRAM -of_objects
[ipx::current_core]]]
ipx::add_port_map ARREADY [ipx::get_bus_interfaces M_AXI_FULL_DRAM
-of_objects [ipx::current_core]]
set_property physical_name m_axi_arready_i [ipx::get_port_maps ARREADY
-of_objects [ipx::get_bus_interfaces M_AXI_FULL_DRAM -of_objects
[ipx::current_core]]]
ipx::add_port_map WVALID [ipx::get_bus_interfaces M_AXI_FULL_DRAM -of_objects
[ipx::current_core]]
set_property physical_name m_axi_wvalid_o [ipx::get_port_maps WVALID -of_objects
[ipx::get_bus_interfaces M_AXI_FULL_DRAM -of_objects [ipx::current_core]]]
ipx::add_port_map ARVALID [ipx::get_bus_interfaces M_AXI_FULL_DRAM -of_objects
[ipx::current_core]]
```

```
set_property physical_name m_axi_arvalid_o [ipx::get_port_maps ARVALID -of_objects
[ipx::get_bus_interfaces M_AXI_FULL_DRAM -of_objects [ipx::current_core]]]
ipx::add_port_map AWBURST [ipx::get_bus_interfaces M_AXI_FULL_DRAM
-of_objects [ipx::current_core]]
set_property physical_name m_axi_awburst_o [ipx::get_port_maps AWBURST
-of_objects [ipx::get_bus_interfaces M_AXI_FULL_DRAM -of_objects
[ipx::current_core]]]

ipx::add_bus_interface M_AXI_LITE_IO_OUT [ipx::current_core]
set_property abstraction_type_vlnv xilinx.com:interface:aximm_rtl:1.0
[ipx::get_bus_interfaces M_AXI_LITE_IO_OUT -of_objects [ipx::current_core]]
set_property bus_type_vlnv xilinx.com:interface:aximm:1.0 [ipx::get_bus_interfaces
M_AXI_LITE_IO_OUT -of_objects [ipx::current_core]]
set_property interface_mode master [ipx::get_bus_interfaces M_AXI_LITE_IO_OUT
-of_objects [ipx::current_core]]
set_property display_name M_AXI_LITE_IO_OUT [ipx::get_bus_interfaces
M_AXI_LITE_IO_OUT -of_objects [ipx::current_core]]
set_property description {AXI4-LITE IO connection} [ipx::get_bus_interfaces
M_AXI_LITE_IO_OUT -of_objects [ipx::current_core]]
ipx::add_bus_parameter NUM_READ_OUTSTANDING [ipx::get_bus_interfaces
M_AXI_LITE_IO_OUT -of_objects [ipx::current_core]]
ipx::add_bus_parameter NUM_WRITE_OUTSTANDING [ipx::get_bus_interfaces
M_AXI_LITE_IO_OUT -of_objects [ipx::current_core]]
ipx::add_port_map BVALID [ipx::get_bus_interfaces M_AXI_LITE_IO_OUT -of_objects
[ipx::current_core]]
set_property physical_name m_axi_lite_bvalid_i [ipx::get_port_maps BVALID
-of_objects [ipx::get_bus_interfaces M_AXI_LITE_IO_OUT -of_objects
[ipx::current_core]]]
ipx::add_port_map RREADY [ipx::get_bus_interfaces M_AXI_LITE_IO_OUT -of_objects
[ipx::current_core]]
set_property physical_name m_axi_lite_rready_o [ipx::get_port_maps RREADY
-of_objects [ipx::get_bus_interfaces M_AXI_LITE_IO_OUT -of_objects
[ipx::current_core]]]
ipx::add_port_map BREADY [ipx::get_bus_interfaces M_AXI_LITE_IO_OUT -of_objects
[ipx::current_core]]
set_property physical_name m_axi_lite_bready_o [ipx::get_port_maps BREADY
-of_objects [ipx::get_bus_interfaces M_AXI_LITE_IO_OUT -of_objects
[ipx::current_core]]]
ipx::add_port_map AWVALID [ipx::get_bus_interfaces M_AXI_LITE_IO_OUT
-of_objects [ipx::current_core]]
```

```
set_property physical_name m_axi_lite_awvalid_o [ipx::get_port_maps AWVALID
-of_objects [ipx::get_bus_interfaces M_AXI_LITE_IO_OUT -of_objects
[ipx::current_core]]]
ipx::add_port_map AWREADY [ipx::get_bus_interfaces M_AXI_LITE_IO_OUT
-of_objects [ipx::current_core]]
set_property physical_name m_axi_lite_awready_i [ipx::get_port_maps AWREADY
-of_objects [ipx::get_bus_interfaces M_AXI_LITE_IO_OUT -of_objects
[ipx::current_core]]]
ipx::add_port_map AWPROT [ipx::get_bus_interfaces M_AXI_LITE_IO_OUT
-of_objects [ipx::current_core]]
set_property physical_name m_axi_lite_awprot_o [ipx::get_port_maps AWPROT
-of_objects [ipx::get_bus_interfaces M_AXI_LITE_IO_OUT -of_objects
[ipx::current_core]]]
ipx::add_port_map WDATA [ipx::get_bus_interfaces M_AXI_LITE_IO_OUT -of_objects
[ipx::current_core]]
set_property physical_name m_axi_lite_wdata_o [ipx::get_port_maps WDATA
-of_objects [ipx::get_bus_interfaces M_AXI_LITE_IO_OUT -of_objects
[ipx::current_core]]]
ipx::add_port_map RRESP [ipx::get_bus_interfaces M_AXI_LITE_IO_OUT -of_objects
[ipx::current_core]]
set_property physical_name m_axi_lite_rresp_i [ipx::get_port_maps RRESP -of_objects
[ipx::get_bus_interfaces M_AXI_LITE_IO_OUT -of_objects [ipx::current_core]]]
ipx::add_port_map ARPROT [ipx::get_bus_interfaces M_AXI_LITE_IO_OUT -of_objects
[ipx::current_core]]
set_property physical_name m_axi_lite_arprot_o [ipx::get_port_maps ARPROT
-of_objects [ipx::get_bus_interfaces M_AXI_LITE_IO_OUT -of_objects
[ipx::current_core]]]
ipx::add_port_map RVALID [ipx::get_bus_interfaces M_AXI_LITE_IO_OUT -of_objects
[ipx::current_core]]
set_property physical_name m_axi_lite_rvalid_i [ipx::get_port_maps RVALID
-of_objects [ipx::get_bus_interfaces M_AXI_LITE_IO_OUT -of_objects
[ipx::current_core]]]
ipx::add_port_map ARADDR [ipx::get_bus_interfaces M_AXI_LITE_IO_OUT
-of_objects [ipx::current_core]]
set_property physical_name m_axi_lite_araddr_o [ipx::get_port_maps ARADDR
-of_objects [ipx::get_bus_interfaces M_AXI_LITE_IO_OUT -of_objects
[ipx::current_core]]]
ipx::add_port_map AWADDR [ipx::get_bus_interfaces M_AXI_LITE_IO_OUT
-of_objects [ipx::current_core]]
```

```
set_property physical_name m_axi_lite_awaddr_o [ipx::get_port_maps AWADDR
-of_objects [ipx::get_bus_interfaces M_AXI_LITE_IO_OUT -of_objects
[ipx::current_core]]]
ipx::add_port_map ARREADY [ipx::get_bus_interfaces M_AXI_LITE_IO_OUT
-of_objects [ipx::current_core]]
set_property physical_name m_axi_lite_arready_i [ipx::get_port_maps ARREADY
-of_objects [ipx::get_bus_interfaces M_AXI_LITE_IO_OUT -of_objects
[ipx::current_core]]]
ipx::add_port_map WVALID [ipx::get_bus_interfaces M_AXI_LITE_IO_OUT -of_objects
[ipx::current_core]]
set_property physical_name m_axi_lite_wvalid_o [ipx::get_port_maps WVALID
-of_objects [ipx::get_bus_interfaces M_AXI_LITE_IO_OUT -of_objects
[ipx::current_core]]]
ipx::add_port_map WREADY [ipx::get_bus_interfaces M_AXI_LITE_IO_OUT
-of_objects [ipx::current_core]]
set_property physical_name m_axi_lite_wready_i [ipx::get_port_maps WREADY
-of_objects [ipx::get_bus_interfaces M_AXI_LITE_IO_OUT -of_objects
[ipx::current_core]]]
ipx::add_port_map ARVALID [ipx::get_bus_interfaces M_AXI_LITE_IO_OUT
-of_objects [ipx::current_core]]
set_property physical_name m_axi_lite_arvalid_o [ipx::get_port_maps ARVALID
-of_objects [ipx::get_bus_interfaces M_AXI_LITE_IO_OUT -of_objects
[ipx::current_core]]]
ipx::add_port_map WSTRB [ipx::get_bus_interfaces M_AXI_LITE_IO_OUT -of_objects
[ipx::current_core]]
set_property physical_name m_axi_lite_wstrb_o [ipx::get_port_maps WSTRB
-of_objects [ipx::get_bus_interfaces M_AXI_LITE_IO_OUT -of_objects
[ipx::current_core]]]
ipx::add_port_map BRESP [ipx::get_bus_interfaces M_AXI_LITE_IO_OUT -of_objects
[ipx::current_core]]
set_property physical_name m_axi_lite_bresp_i [ipx::get_port_maps BRESP
-of_objects [ipx::get_bus_interfaces M_AXI_LITE_IO_OUT -of_objects
[ipx::current_core]]]
ipx::add_port_map RDATA [ipx::get_bus_interfaces M_AXI_LITE_IO_OUT -of_objects
[ipx::current_core]]
set_property physical_name m_axi_lite_rdata_i [ipx::get_port_maps RDATA -of_objects
[ipx::get_bus_interfaces M_AXI_LITE_IO_OUT -of_objects [ipx::current_core]]]

ipx::add_bus_interface S_AXI_LITE_IO_IN [ipx::current_core]
```

```
set_property abstraction_type_vlnv xilinx.com:interface:aximm_rtl:1.0
[ipx::get_bus_interfaces S_AXI_LITE_IO_IN -of_objects [ipx::current_core]]
set_property bus_type_vlnv xilinx.com:interface:aximm:1.0 [ipx::get_bus_interfaces
S_AXI_LITE_IO_IN -of_objects [ipx::current_core]]
set_property display_name S_AXI_LITE_IO_IN [ipx::get_bus_interfaces
S_AXI_LITE_IO_IN -of_objects [ipx::current_core]]
set_property description {AXI4-LITE IO in} [ipx::get_bus_interfaces S_AXI_LITE_IO_IN
-of_objects [ipx::current_core]]
ipx::add_bus_parameter NUM_READ_OUTSTANDING [ipx::get_bus_interfaces
S_AXI_LITE_IO_IN -of_objects [ipx::current_core]]
ipx::add_bus_parameter NUM_WRITE_OUTSTANDING [ipx::get_bus_interfaces
S_AXI_LITE_IO_IN -of_objects [ipx::current_core]]
ipx::add_port_map BVALID [ipx::get_bus_interfaces S_AXI_LITE_IO_IN -of_objects
[ipx::current_core]]
set_property physical_name s_axi_lite_bvalid_o [ipx::get_port_maps BVALID
-of_objects [ipx::get_bus_interfaces S_AXI_LITE_IO_IN -of_objects [ipx::current_core]]]
ipx::add_port_map RREADY [ipx::get_bus_interfaces S_AXI_LITE_IO_IN -of_objects
[ipx::current_core]]
set_property physical_name s_axi_lite_rready_i [ipx::get_port_maps RREADY
-of_objects [ipx::get_bus_interfaces S_AXI_LITE_IO_IN -of_objects [ipx::current_core]]]
ipx::add_port_map BREADY [ipx::get_bus_interfaces S_AXI_LITE_IO_IN -of_objects
[ipx::current_core]]
set_property physical_name s_axi_lite_bready_i [ipx::get_port_maps BREADY
-of_objects [ipx::get_bus_interfaces S_AXI_LITE_IO_IN -of_objects [ipx::current_core]]]
ipx::add_port_map AWVALID [ipx::get_bus_interfaces S_AXI_LITE_IO_IN -of_objects
[ipx::current_core]]
set_property physical_name s_axi_lite_awvalid_i [ipx::get_port_maps AWVALID
-of_objects [ipx::get_bus_interfaces S_AXI_LITE_IO_IN -of_objects [ipx::current_core]]]
ipx::add_port_map AWREADY [ipx::get_bus_interfaces S_AXI_LITE_IO_IN -of_objects
[ipx::current_core]]
set_property physical_name s_axi_lite_awready_o [ipx::get_port_maps AWREADY
-of_objects [ipx::get_bus_interfaces S_AXI_LITE_IO_IN -of_objects [ipx::current_core]]]
ipx::add_port_map AWPROT [ipx::get_bus_interfaces S_AXI_LITE_IO_IN -of_objects
[ipx::current_core]]
set_property physical_name s_axi_lite_awprot_i [ipx::get_port_maps AWPROT
-of_objects [ipx::get_bus_interfaces S_AXI_LITE_IO_IN -of_objects [ipx::current_core]]]
ipx::add_port_map WDATA [ipx::get_bus_interfaces S_AXI_LITE_IO_IN -of_objects
[ipx::current_core]]
set_property physical_name s_axi_lite_wdata_i [ipx::get_port_maps WDATA
-of_objects [ipx::get_bus_interfaces S_AXI_LITE_IO_IN -of_objects [ipx::current_core]]]
```

```
ipx::add_port_map RRESP [ipx::get_bus_interfaces S_AXI_LITE_IO_IN -of_objects
[ipx::current_core]]
set_property physical_name s_axi_lite_rresp_o [ipx::get_port_maps RRESP -of_objects
[ipx::get_bus_interfaces S_AXI_LITE_IO_IN -of_objects [ipx::current_core]]]
ipx::add_port_map ARPROT [ipx::get_bus_interfaces S_AXI_LITE_IO_IN -of_objects
[ipx::current_core]]
set_property physical_name s_axi_lite_arprot_i [ipx::get_port_maps ARPROT
-of_objects [ipx::get_bus_interfaces S_AXI_LITE_IO_IN -of_objects [ipx::current_core]]]
ipx::add_port_map RVALID [ipx::get_bus_interfaces S_AXI_LITE_IO_IN -of_objects
[ipx::current_core]]
set_property physical_name s_axi_lite_rvalid_o [ipx::get_port_maps RVALID
-of_objects [ipx::get_bus_interfaces S_AXI_LITE_IO_IN -of_objects [ipx::current_core]]]
ipx::add_port_map ARADDR [ipx::get_bus_interfaces S_AXI_LITE_IO_IN -of_objects
[ipx::current_core]]
set_property physical_name s_axi_lite_araddr_i [ipx::get_port_maps ARADDR
-of_objects [ipx::get_bus_interfaces S_AXI_LITE_IO_IN -of_objects [ipx::current_core]]]
ipx::add_port_map AWADDR [ipx::get_bus_interfaces S_AXI_LITE_IO_IN -of_objects
[ipx::current_core]]
set_property physical_name s_axi_lite_awaddr_i [ipx::get_port_maps AWADDR
-of_objects [ipx::get_bus_interfaces S_AXI_LITE_IO_IN -of_objects [ipx::current_core]]]
ipx::add_port_map ARREADY [ipx::get_bus_interfaces S_AXI_LITE_IO_IN -of_objects
[ipx::current_core]]
set_property physical_name s_axi_lite_arready_o [ipx::get_port_maps ARREADY
-of_objects [ipx::get_bus_interfaces S_AXI_LITE_IO_IN -of_objects [ipx::current_core]]]
ipx::add_port_map WVALID [ipx::get_bus_interfaces S_AXI_LITE_IO_IN -of_objects
[ipx::current_core]]
set_property physical_name s_axi_lite_wvalid_i [ipx::get_port_maps WVALID
-of_objects [ipx::get_bus_interfaces S_AXI_LITE_IO_IN -of_objects [ipx::current_core]]]
ipx::add_port_map WREADY [ipx::get_bus_interfaces S_AXI_LITE_IO_IN -of_objects
[ipx::current_core]]
set_property physical_name s_axi_lite_wready_o [ipx::get_port_maps WREADY
-of_objects [ipx::get_bus_interfaces S_AXI_LITE_IO_IN -of_objects [ipx::current_core]]]
ipx::add_port_map ARVALID [ipx::get_bus_interfaces S_AXI_LITE_IO_IN -of_objects
[ipx::current_core]]
set_property physical_name s_axi_lite_arvalid_i [ipx::get_port_maps ARVALID
-of_objects [ipx::get_bus_interfaces S_AXI_LITE_IO_IN -of_objects [ipx::current_core]]]
ipx::add_port_map WSTRB [ipx::get_bus_interfaces S_AXI_LITE_IO_IN -of_objects
[ipx::current_core]]
set_property physical_name s_axi_lite_wstrb_i [ipx::get_port_maps WSTRB -of_objects
[ipx::get_bus_interfaces S_AXI_LITE_IO_IN -of_objects [ipx::current_core]]]
```

```
ipx::add_port_map BRESP [ipx::get_bus_interfaces S_AXI_LITE_IO_IN -of_objects [ipx::current_core]]
set_property physical_name s_axi_lite_bresp_o [ipx::get_port_maps BRESP -of_objects [ipx::get_bus_interfaces S_AXI_LITE_IO_IN -of_objects [ipx::current_core]]]
ipx::add_port_map RDATA [ipx::get_bus_interfaces S_AXI_LITE_IO_IN -of_objects [ipx::current_core]]
set_property physical_name s_axi_lite_rdata_o [ipx::get_port_maps RDATA -of_objects [ipx::get_bus_interfaces S_AXI_LITE_IO_IN -of_objects [ipx::current_core]]]

ipx::associate_bus_interfaces -busif M_AXI_FULL_DRAM -clock Clk [ipx::current_core]
ipx::associate_bus_interfaces -busif M_AXI_LITE_IO_OUT -clock Clk [ipx::current_core]
ipx::associate_bus_interfaces -busif S_AXI_LITE_IO_IN -clock Clk [ipx::current_core]
ipx::associate_bus_interfaces -clock Clk -reset reset_i [ipx::current_core]

endgroup

# Package Core
ipx::update_checksums [ipx::current_core]
ipx::save_core [ipx::current_core]
set_property core_revision 2 [ipx::current_core]
ipx::create_xgui_files [ipx::current_core]
ipx::update_checksums [ipx::current_core]
ipx::save_core [ipx::current_core]
set_property  ip_repo_paths  $bp_ip_path [current_project]
update_ip_catalog
```