JUN CAO

Tel:(+46)760182341 | Email: junca@chalmers.se | Orcid

Education

Chalmers University of Technology **Gothenburg, Sweden**
Master Students in Information and Communication Technology *Sep.2024-Present*
Southeast University, Chien-shiung Wu College (Honors College) **Nanjing, Jiangsu, China**
Bachelor of Science, major in Information Science and Engineering *Sep.2020-Jun.2024*

- **GPA and Average Score:** 3.93/4.0 | 92.3/100
- **Honors:** *National Scholarship* (Top 1%) in 2020-2021**;** *Tong Ren Ding Scholarship* (Corporate-sponsored) in 2021-2022.

Research Experience

Digital predistortion linearization technology of power amplifiers and FPGA implementation
(Verilog, MATLAB, Python, 2023-2024)
Advised by *Prof. Chao Yu*, *State Key Laboratory of Millimeter Waves, Southeast University, Nanjing*

- Learned the basics of power amplifiers and read relevant pieces of literature concerning digital predistortion technology and modern power amplifiers.
- Completed Verilog implementation of GMP and MP models of digital predistortion with *Xilinx Zynq UltraScale+ ZCU102 Evaluation Kit*.
- Finished the overall simulation of digital predistortion in MATLAB using various models and expanded the test scenario to broadband test signals(200MHz 5GNR).

Design of 5G millimeter wave massive MIMO beam measurement system (C++, MATLAB, 2022)
Advised by *Prof. Chao Yu*, *State Key Laboratory of Millimeter Waves, Southeast University, Nanjing*

- **Contribution**: Developed and tested a software platform suitable for joint simulation of turntables, antennas and various measuring instruments based on MATLAB.
- Learned the use of relevant instruments in the RF laboratory and the measurement methods of antennas in dynamic environments.
- Learned the basic knowledge of antennas and important parameters for measuring antenna performance and gained experience in laboratory measurement.

Publication

Wei Xue, Yixiang Huang, **Jun Cao**, YuCheng Yu, FeiFei Hui, Chao Yu, "Dynamic Matching Power Amplification Technique for Transmitting Time-Varied Signals With Large Modulated Bandwidth and Frequency Range," in *IEEE Transactions on Microwave Theory and Techniques*, 2024.

Contribution:

- Implement the LMS-based adaptive FIR filter to generate the control signal for power amplifier dynamic matching control.
- Draw most of the figures and block diagrams in the paper to illustrate related ideas.
- Laboratory testing and real-time system calibration.

Course Projects

RF Circuit Modeling and CAD with *Systemvue* (MATLAB, Python)

Keysight & SEU joint course, Sep.2022-Jan.2023

- Schools and enterprises jointly offer courses to learn today's cutting-edge RF circuit research directions from the industry's top company *Keysight*.
- Learn the joint simulation of *Systemvue* software and *MATLAB* and implement digital predistortion of balanced power amplifiers using various models like MP, GMP and DNN.
- The group I led won second place among 12 groups in the final project assessment.

Digital system integrated design with FPGA (Verilog)

Texas Instruments & SEU joint course, May.2022-Jun.2022

- Selected project: Implementation of a simple voltmeter with *Xilinx Artix-7 Series*.
- Learned the basics of FPGA design, finite state machine theory, etc., and conducted a series of programming practices. Wide range(200mV–5V), multi-channel, interactive, high-precision(< 0.5%) voltage measurement is achieved.
- Assessment result: A (Top 10%).

Comprehensive circuit system design: Phase-locked loop circuit simulation implemented in Cadence Virtuoso (Verilog A, C++, Python) *May.2022-Jun.2022*

- Learn the basic knowledge of phase-locked loop circuits and implement basic signal simulation in *MATLAB Simulink*.
- Implemented the phase-locked loop circuit in ADS, combined components such as VCO and Frequency Detector in the form of a circuit and completed the simulation and optimization goals.
- The code of most modules was written using Verilog AMS language, and the signal simulation was implemented in Cadence Virtuoso.

Extracurricular Activities

- Content Ambassador of International Students, Chalmers *Sep.2024-Present*
- Programme Ambassador of *MPICT*, Chalmers *Sep.2024-Present*
- Chairman of Student Union of Chien-shiung Wu College, Southeast University *Sep.2022-Sep.2023*

Skills & Interests

Programming Languages: MATLAB (fluent), Verilog (fluent), Python(fluent), C/C++, Java,
Engineering Software: Vivado, Quartus, Multisim, ADS, Systemvue, Cadence Virtuoso
Systems: Linux, Mac, Windows
Interests: Flim, Music, Jogging