

CECS 346 Lab 4 – SysTick

Preparation:

You will need a TI TM4C LaunchPad.

Book Reading: Textbook Sections 4.4

Starter Project: CECS346_Lab4_SysTick

Reference Code: Textbook Program 4.7a (in Lecture 5 slides), TExaSware\C10_SysTick

Purpose:

The purpose of this lab is to learn how to use SysTick to generate accurate timing for an embedded system, and learn how to use logic analyzer in Keil uVision simulator.

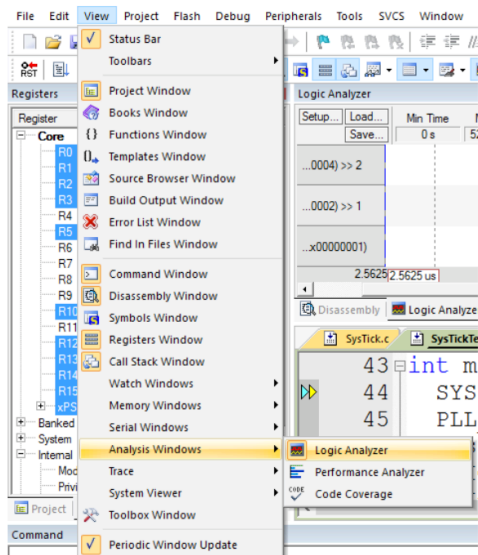
System Requirements:

In this lab you will implement the same features as Lab 1. Instead of using a software `for` loop to generate 0.1s delay, you will use SysTick timer busy waiting approach to generate the same time delay.

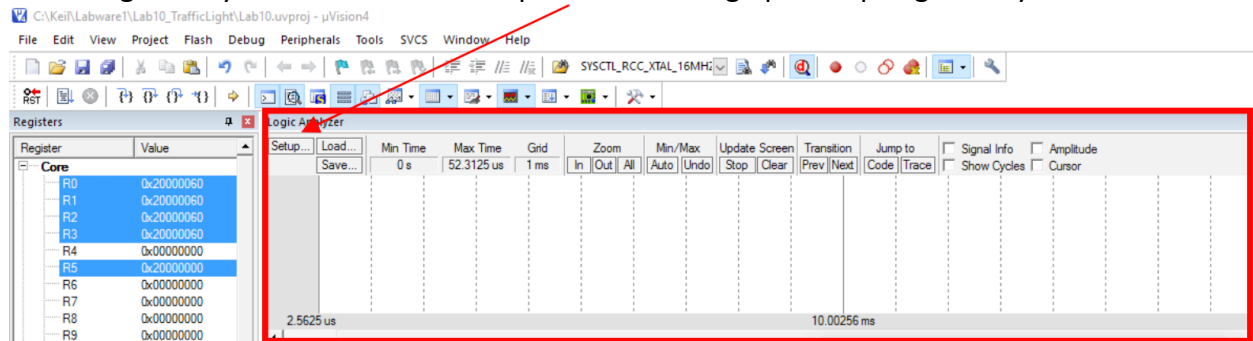
Procedure:

1. Download CECS346_Lab4_SysTick.zip and unzip into Keil\Labware folder.
2. Study Lecture 5 sample code / TExaSware\C10_SysTick, specifically `SysTick_Init()` and `SysTick_Wait()`.
3. Create a `SysTick_Init()` function in main.c and call it from main().
4. Update the `Delay()` function in main.c based on the contents of `SysTick_Wait()` to wait 0.1 seconds, assuming the board has a clock speed of 16 MHz.
5. Compile and simulate it: First, set up the logic analyzer to observe bits PB0, PB1, and PB2. After start debug session, you should see a Logic Analyzer window. If you do not see the Logic Analyzer window after you start debugging, click View menu -> Analysis Windows ->

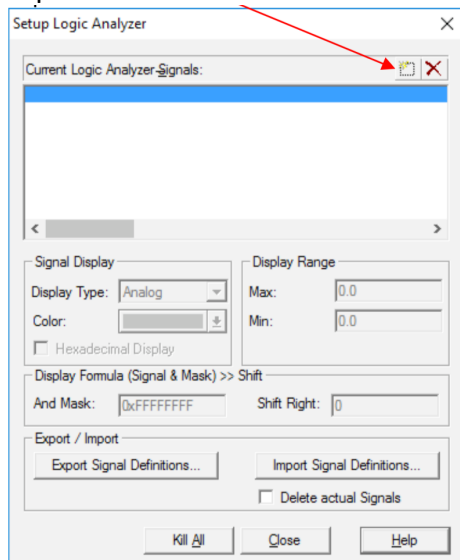
Logic Analyzer to open the Logic Analyzer. See figure below.



6. In the Logic Analyzer window Click Setup button to bring up "Setup Logic Analyzer" window.

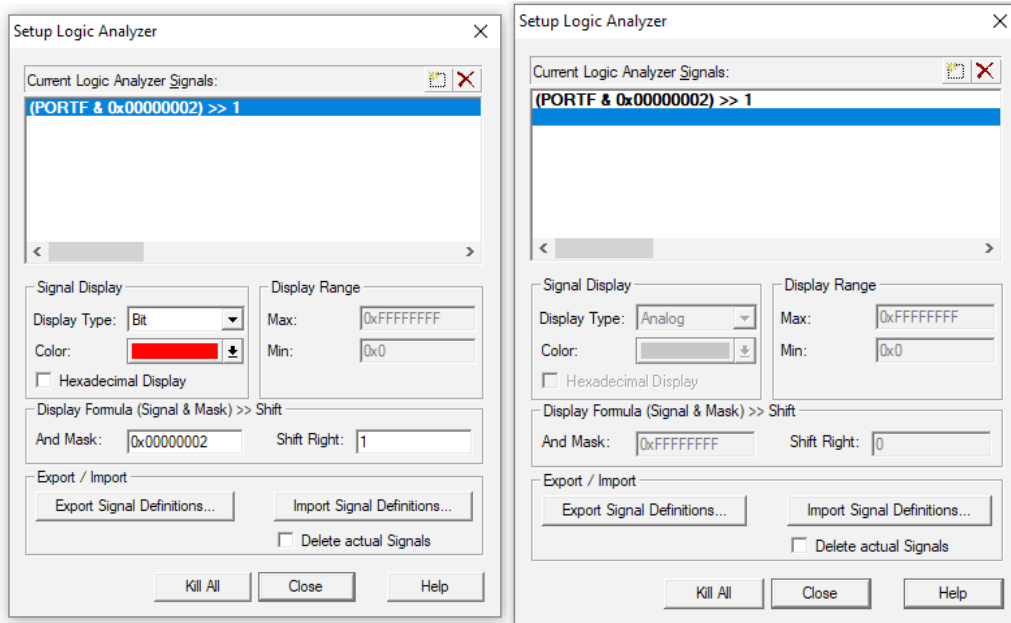


7. Then click New (Insert) button on the "Setup Logic Analyzer" window to add signals to be captured.



8. We want to visualize 4 signals: PF1, PF2, PF3, and PF4. To capture PF1 (LaunchPad Red LED), enter "(PORTB & 0x02) >> 2" or "PORTB.1" in the "setup Logic Analyzer" window and hit

Enter when done. Then select the setting just entered and make sure Display Type is “Bit” and pick a color the matches the LED color.



Close the window to finish current signal setup.

9. Open Peripherals -> TExaS Port F window and toggle SW1 and watch the Logic Analyzer.
10. Create a screenshot of the Logic Analyzer simulation results showing that 5 flashes (10 delays) takes a little over 1 second (slightly longer than expected due to code before and after the delay).

Deliverable:

- 1) Demonstrate your lab
 - a. In simulator – Show 4 signals in Logic Analyzer. Show that delay is 0.1s.
 - b. On board – Show board flashing
- 2) Submit to the Beachboard Dropbox
 - a. Software source code (main.c)
 - b. Logic Analyzer screenshot