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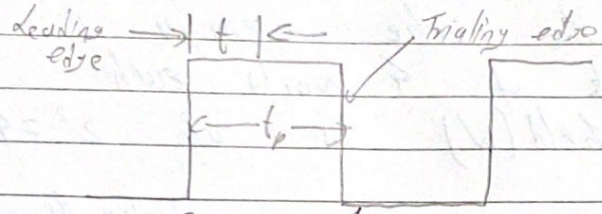
4) Consider for example the inputs are J=K=1 & Q=0 & pulse as shown in figure below is applied at clock input



After a time interval Δt equal to propagation delay in 2 Nand gates in series, the output will change to Q=1. Now we have J=K=1 & Q=1 & after another time interval of Δt, the output will change back to 0. Hence we conclude that the value of Q will oscillate between 1 & 0. This is called race around condition.

This condition can be avoided if $t_p < \Delta t < T$. However, it may be difficult to satisfy this inequality bcoz of very small propagation delay in IC. To overcome this we use Master-Slave JK flip flop.

A Master slave J-K flipflop is cascade of 2 S-R flipflop with feedback from the output of the second to inputs of first. Positive clock pulse are applied to the first flip flop & the clock pulses are inverted before being applied to the second.

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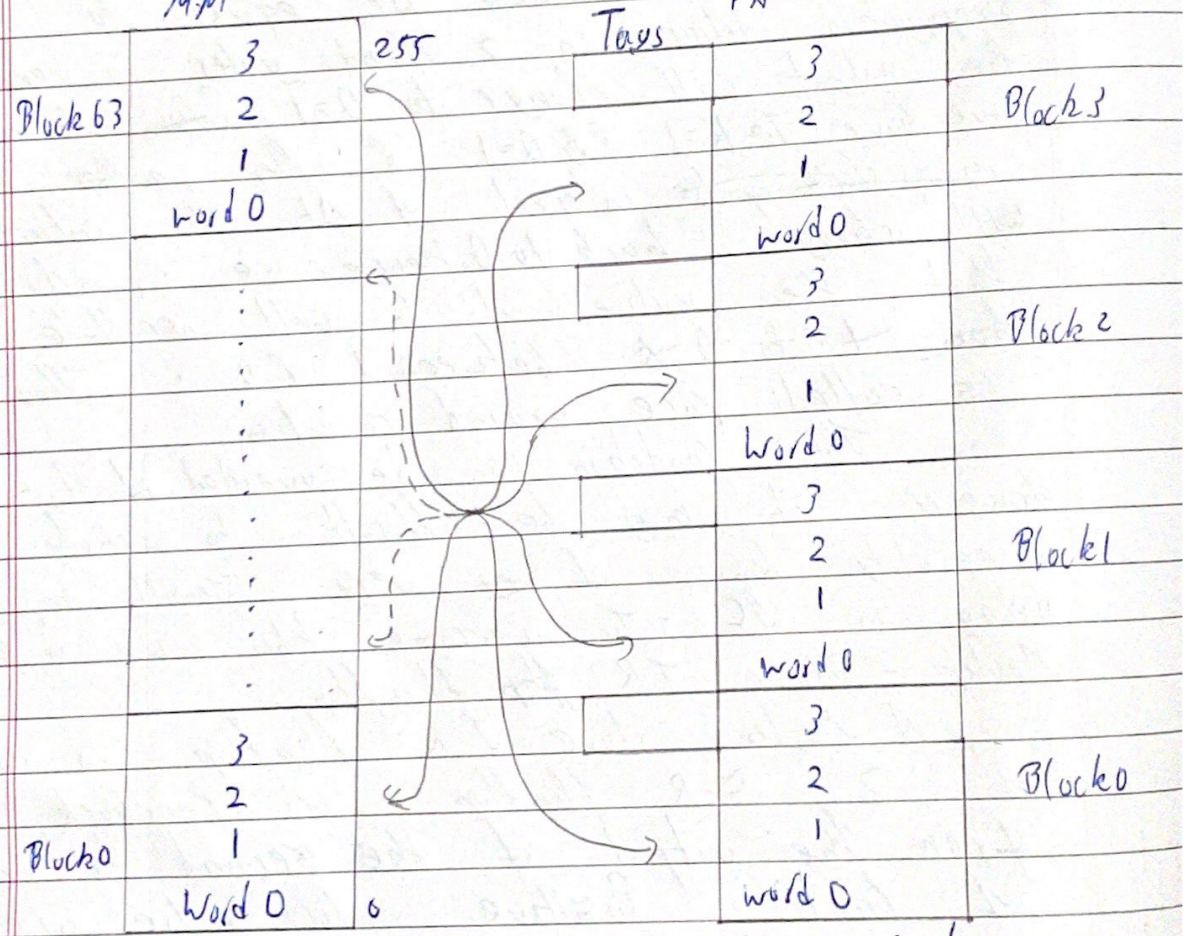
3) Cache Memory of 16 words - Each block consists of 4 words

Therefore, the cache memory is organized as 4 block of 4 words each

∴ word field (W) is of $2^2 = 4 \rightarrow 2$ bits in width



T	W
Tag Field	Word Field
6 bit	2 bit

The ~~Main~~ Main Memory is of 256 bytes.

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Total address field is of 8 bits.

However, Address field (A) = Tag field (T) + Word field (W) from associative

∴ Tag field is

$$T = A - W = 8 - 2 = 6 \text{ bit}$$

The Main Memory is divided into 64 block and cache would be organised as 4 word of 4 block each. Any cache block can be populated to/from any block in MM