4)	Consider for example the inputs one J=K=1
	& 4=0 6 huse as shown in fure below is applied
10	Leading of the Finaling edge at clock input
	ege de la companya della companya della companya de la companya della companya de
1/4	Standard Control
	After a fine inferval At equal to
	propagation delay in 2 Nand gates in series
	we have J=K=1 & Q=1 & after another pino
	in clock pute interval of Dt, the output
	will charge buck to la Hence we condude
	that the value of a will oscillate
5 6	from + to Do between 1 60. This
	15 called face around condition
	This condition can be avoided if to < AT <t.< th=""></t.<>
	However, it may be difficult to sapisfy this
1.0	in equality to stee very small propagation
	delay in IC : to overcome this we use
	Auster - Slave TK pap flip fly
	A Muster slave J-R flipflyp is corcade
	of 2 5-R glipflop with feedback
	of 2 5-R flipfly with feedback  From the output of the second to inputs of first . Positive clock pulse are
	of mist " cositive clock pulse are
	clock pulses are inverted before being
	applied to the second . then the
	applied to 125 selona
	when it I is a proper down the set
	STATE OF THE STATE

3)	Cacho	Memory	01 1	6 Word	s - Ea	ch block	Longists	
-7	Cache Memory of 16 Words - Each block consists							
	Therefore, the cache memory is organized  Therefore, the cache memory is organized							
	1 2 - 4 h/6/2							
	word field (W)							
	in width lathe Memory							
		MM	1	730/1/	Toys	FA	1	
100	0.4	3	255	-	10,93	3	2/ / )	
B	luck 63	2 \ =	1	1 1 1 1		2	B(och3	
Sec. Sec. Sec.		1			>			
	A. A.	roid 0		1	N. A.	mordo		
	V. 1.	9.1	6	3/2	1	3		
	321			1	A-1	2	Plock 2	
	XX	1 1 1	1		7	1/1/2		
				1		Wordo		
A5  2	1000	10 2 10 21 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1			3	N. A. A. A.	
			1			2	Blockl	
		•				21 1	2-3-73-11	
	4.1	an en	6		7	word 0		
						3		
		3				2	Blocko	
		2	2	-		l l		
	Blucho	16/0	and the second	A A		wold o		
	Vin 1 s	Word O	6	3.46.			0/1	
	Addron Field							
	The state of the same of the s							
	T Warmen							
	Tay Word							
	Gield field							
	6 bit 2 bit							
	The Main Memory is of 256 bytes.							

	Total address field is of 8 bits.
	However, Address field (A) = Tag field (T) + Word field (W) from
	Toy field is associatise
	T= A- W= 8-2= 6 bit
	The Main Memory is divided into 64 block up to cache would be organised as 4
	word of 4 block ouch a Any cache block  can be populated to/from one block in
4, 3,	