SIES Graduate School of Technology

Subject : DLCOA

Roll No.: 114A1076

Assignment No. 3

Date : 25/11/20

Q1) What is bus arbitration? Explain any 2 techniques of bus arbitration

a) The device that is allowed to initiate data ~~transfers~~ transfers on the bus at any given time is called bus master. In a computer system, there may be more than one bus master such as processor, DMA controller, etc

b) They share the system bus when current master relinquishes control of the bus, another bus master can aquire control of bus

c) Bus arbitration is the process by which the next device to become the bus master is selected & bus ~~mas~~ mastership is transferred to it. The selection of bus master usually done on the priority basis.

d) There are 2 ~~appro~~ approaches to bus arbitration: Centralized & distributed

i) Centralized Arbitration

ii) In centralized bus arbitration, a single bus arbiter ~~are~~ performs the required arbitration. The bus arbiter may be the processor or a separate controller connected to the bus

iii) There are 3 different arbitration scheme that use the centralized bus arbitration approach. The schemes are

i) Daisy chaining

ii) Polling method

iii) Independent request

c) Daisy chaining

It is simple & cheaper method. All masters make use of same line for bus request

In response to the bus request, the controller sends a bus grant if the bus is free

d) Polling method

In this, the controller is used to generate the addresses for ~~the~~ the master. Number of address line required depends on the number of master

connected in the system.
For example, if there are 8 masters connected in the system, at least 3 ~~addr~~ address lines are required

e) ~~Ind~~ Independent request:
In distributed arbitration, all devices participate in the selection of next bus master.
In this scheme each device on the bus is assigned a 4-bit identification number

2) The Main memory size is = 4096 blocks $= 2^{12}$
Each block has 128 word $= 2^7$ word
∴ Total size of main memory in word length
$= 2^{12} \times 2^7 = 2^{19}$
Hence, there will be 19 bit in MM
ii) The MM size = 4096 blocks $= 2^{12}$
∴ TAG + SET = 12

Cache is divided into $16 = 2^4$ set
∴ SET $= 2^4$
TAG = $12 - 4 = 8$
Each word consist of 128 words $= 2^7$ word

∴ Word field length = 7 bits
∴ There are 8, 4, 7 bit in tag set and word field respectively

3) Addressing mode types
i) Implied mode:- In implied addressing the operand is specified in the instructions itself. Data is 8 bit or 16 bit long & data is part of instruction. Zero address instructions are designed with implied addressing mode
Example:- CLC

ii) Immediate addressing mode:-
In this mode, data is present in address field of instruction. Designed like one address instruction format
Eg:- MOV AL, 35H

iii) Register mode:-
In register addressing, the operand is placed in one of 8 bit or 16 bit general purpose registers. The data is in the register that is ~~specifically~~ specified by the instructions.
Eg:- MOV AX, CX

iv) Register Indirect Mode: In this addressing, the operand's offset is placed in any one of the registers BX, BP, SI, DI as specified in the instruction. The effective address of data is in the base register or an index register
Eg:- MOV AX, [BX]

4) i) Pipeline hazards are situation that prevents the next instruction in instruction stream from executing during designated clock cycle

ii) Any condition that causes a stall in the pipeline operations can be called as hazard.

iii) There are primarily 3 types of hazard

a) Data Hazards:
A data Hazard is any condition in which either the source or the destination operand of an instruction are not available at the time expected in the pipeline. As a result of which some operation has to be ~~delayed~~ delayed & the pipeline stalls. Whenever there are 2 instructions one of which depends on the data obtained from the other.
A = 3 + A
B = A * 4

ii) Structural Hazard

This ~~situ~~ situation arises mainly when 2 instruction require a given hardware resource at same time & hence for one of the instructions the pipeline need to be stalled.

The most common case is when memory is accessed at the same time by 2 instructions.

One instruction may need to access the memory as part of the Execute or Write back phase while other instruction is being fetched.

iii) Control hazards

The instruction fetch unit of the CPU is responsible for providing a stream of instructions to execute unit.

The instruction fetched by fetch unit are in consecutive memory location and they are executed

However, problem arises when one of the instructions is a branching instruction to some other memory location