Evaluation II-SE CE- DLCOA-MCQ - Part 1

Note:1) All questions are compulsory
2) Each question carries 1 Mark

Points: 10/10

1. Access type of memory that enables one to make a comparison of desired bit locations within a word for a specified match- *
(1/1 Point)

- 1. Random
- 2. Sequential
- 3. Direct
- 4. Associative ✓

2. Roll No. *

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3. How many times does the processor need to refer to memory when it fetches and executes an indirect-address-mode instruction if the instruction is a computation requiring a single operand? *
(1/1 Point)

- (●) 1. 2 ✓
- ( ) 2. 4
- ( ) 3. 1
- ( ) 4. 6

4. Identify the micro operations for the indirect cycle- *
(1/1 Point)

- (●) 1. t1: MAR = (IR(Address)) t2: MBR = Memory t3: IR(Address) = (MBR(Address)) ✓
- ( ) 2. t1: MBR =(PC) t2: MAR = Save_Address PC = Routine_Address t3: Memory = (MBR)
- ( ) 3. t1: MAR = (IR(Address)) t2: MAR = Memory t3: IR(Address) = (MBR(Address))
- ( ) 4. t1: MBR =(PC) t2: MAR = Save_Address PC = Routine_Address

5. Segment registers holds *
(1/1 Point)

- ( ) 1. Address of the data to be fetched
- (●) 2. Base Address of the segment ✓
- ( ) 3. Offset in the segment
- ( ) 4. EA of the segment

6. Which of the following is a read-write memory- *
(1/1 Point)

- 1. PROM
- 2. EPROM
- 3. RAM ✓
- 4. Flash memory

7. Which of the following is false w.r.t hardwired control unit- *
(1/1 Point)

- 1. Implemented in hardware
- 2. Flexible ✓
- 3. Very difficult
- 4. Design is complex

8. There is no change in state of the flip flop when both the inputs are low in: *
(1/1 Point)

- 1. D flip flop
- 2. JK flip flop ✓
- 3. SR flip flop
- 4. T flip flop

9. Which of the following is correct for a gated D-type flip-flop? *
(1/1 Point)

- (●) 1. The Q output is either SET or RESET as soon as the D input goes HIGH or LOW. ✓
- ( ) 2. The output complement follows the input when enabled
- ( ) 3. Only one of the inputs can be HIGH at a time
- ( ) 4. The output toggles if one of the inputs is held HIGH

10. Number of half adders needed to implement full adder: *
(1/1 Point)

- (●) 1. 2 ✓
- ( ) 2. 1
- ( ) 3. 3
- ( ) 4. Cannot be implemented

11. A combinational circuit that converts binary information in the form of a 2N input lines into N output lines is : *
(1/1 Point)

- ( ) 1. Decoder
- (●) 2. Encoder ✓
- ( ) 3. MUX
- ( ) 4. Full adder

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