1,082,426

PATENT SPECIFICATION

DRAWINGS ATTACHED

Inventor: DANIEL MATTHEW TAUB

1,082,426

Date of Application and filing Complete Specification: May 5, 1966.

No. 19903/66.

Complete Specification Published: Sept. 6, 1967.

Index at acceptance: —**H3** T(1M2, 1M3, 2A, 2B2, 2B3, 2F, 2J, 2T3J, 2X, 3N, 4C, 4E1, 4EX, 4M); **B6** F(6B8D1, 6B8DY, 6B8G2, 6B8GY); **G4** H(1A, 3B, 3C, 6E, 7B, 9E, 13D)

Int. Cl.: —**H 03 k 17/00**//B 41 j, G 08 d

COMPLETE SPECIFICATION

Interlock Circuit

We, INTERNATIONAL BUSINESS MACHINES CORPORATION, a Corporation organized and existing under the laws of the State of New York in the United States of America, of Armonk, New York 10504, United States of America (assignees of DANIEL MATTHEW TAUB), do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement: —

The present invention relates to an interlock circuit employing bistable circuits.

The invention can advantageously be employed to control keyboards the keys of which are arranged in groups, each group being concerned with a particular item of information to be entered and in any group one and only one key being required to be pressed to set up valid information. If initially the operator makes a mistake and presses the wrong key in a group, this key must be restored or its effect cancelled in some way either before or when the correct one is pressed.

One way of making such a keyboard is to use latching keys, the keys within a group being mechanically interlocked so that when one is pressed it releases any that were previously pressed. In keyboards of which the keys are operated by touch and the keys are stationary, the interlock must be arranged electrically.

According to the present invention there is provided an interlock circuit having a plurality of bistable circuits each switchable between two stable states, a plurality of input circuits corresponding respectively to the bistable circuits, each input circuit being operable to apply to the corresponding bistable circuit a set signal effective to switch the bistable circuit to one of its stable states if in the other, and a negative feedback circuit connected to receive as input the set signal applied to any one of the bistable circuits, the negative feedback circuit being connected and arranged to feed back to its input and to each bistable circuit a reset signal, the reset signal being nullified by the set signal at every bistable circuit which simultaneously receives both set and reset signals, the reset signal being effective at each bistable circuit not simultaneously receiving a set signal to switch the bistable circuit to the said other stable state if in the said one stable state.

Preferably each input circuit is key operated and the bistable circuits are associated respectively with a plurality of indicators, the stable state occupied by each bistable circuit being indicated by the associated indicator.

An example of the present invention will now be described with reference to the accompanying drawings in which: —

Fig. 1 is a block circuit diagram of a keyboard incorporating an interlock circuit according to the present invention and

Fig. 2 is a circuit diagram of portions of the keyboard of Fig. 1.

Referring to Fig. 1, a plurality of keys K_a to K_k are respectively connected to associated input circuits A_a to A_k. Each input circuit in response to the touching of the associated key produces a set signal which is applied to an associated bistable circuit, the bistable circuits B_a to B_k respectively receiving the set signals from the input circuits A_a to A_k.

An OR gate G is connected to all the input circuits A_a to A_k so that a set signal from any one of the input circuits A_a to A_k is applied to a reset circuit R. The reset circuit R responds to the set signal from any

[*Price*

one of the input circuits A_a to A_k by generating a reset signal which is applied to all the bistable circuits B_a to B_k.

The bistable circuits B_a to B_k are associated respectively with indicator lamps L_a to L_k. The lamp associated with any one bistable circuit is arranged to light whenever the associated bistable circuit is in one of its two stable states but to be extinguished whenever the associated bistable circuit is in the other of its two stable states.

When any one of the bistable circuits receives a set signal the bistable circuit is switched to the state in which the associated lamp lights. The reset signal switches each bistable circuit to the state in which the associated lamp is extinguished. When a bistable circuit receives both a set and a reset signal simultaneously, the set signal predominates and the associated lamp lights. Also if an input circuit is operated by the associated key to produce a set signal and, as a consequence, a reset signal, and subsequently the operation of the input circuit ends, the reset signal terminates before the set signal.

In operation when a key such as K_j is touched, the bistable circuit B_j receives a set and a reset signal simultaneously, but as the former predominates, lamp L_j lights. When the operator no longer touches the key K_j, first the reset signal ceases, and then the set signal. Thus B_j remains set. If a second key such as K_k is now touched, lamp L_k lights and the output from R resets B_j since this is no longer receiving a set signal.

If two keys are touched at the same time, both associated lamps light. Then, when the operator leaves one key, that key no longer produces a set signal, but the one still being touched continues to activate R and produce a reset signal. The result is that the only lamp that remains alight is the one associated with the last key to be touched. Information is cleared by touching a key K_r which has no associated bistable circuit and lamp but only operates the reset circuit through an associated input circuit A_r.

The keys K_a to K_k constitute one group of a number of such groups of keys. Each group of keys has its own associated input circuits, bistable circuits, lamps and a reset circuit all as shown in Fig. 1. A complete message is first set up by pressing one key in each of the several groups and the message is transmitted after having been set up correctly.

If the wrong key is touched in any one group, the mistake can be corrected in any one of several ways, (i) The operator may remove his finger from the wrong key and then touch the correct one. (ii) He may slide his finger from the incorrect one to the correct one touching the intervening ones on the way. With the keys closely spaced, there will be times when his finger will touch two keys at once. (iii) Leaving one finger on the wrong key he may touch the correct one with another finger, then take away the first finger and finally the second finger.

It is possible, but unlikely, for the operator to take his fingers from both keys at the same instant, in which case two lamps could remain alight. Misoperation from this cause can be prevented by arranging that simultaneous signals from two bistable circuits within the same group represents valid information.

Referring now to Fig. 2, one of the input circuits A is shown connected to its associated bistable circuit B and lamp L. There is also shown the OR gate G and the reset circuit R. The remaining input circuits A_a to A_k and bistable circuits B_a to B_k are identical to the circuits A and B shown.

The input circuit A includes a bridge circuit consisting of a capacitor C_1, stray capacitance C_{s1} and resistors R_1 and R_2. The bridge circuit is fed with negative-going pulses at a supply terminal 10 and is normally balanced. When the corresponding key K is touched, an addition capacitance C_{in} is introduced which unbalances the bridge circuit causing pulses to be applied between the base of a transistor T_1 and the emitter of a transistor T_2 connected as a Darlington pair. The pulse output from across the Darlington pair causes an output capacitor C_2 to be charged through a diode D_1, the junction between the diode D_1 and capacitor C_2 being caused to become progressively more negative as the capacitor C_2 charges. The set signal from the input circuit A consists of the negative excursion of potential across the capacitor C_2.

The bistable circuit B consists of a pair of transistors T_3 and T_4 one of which has a load resistor R_3 and the other of which has the lamp L associated with the bistable circuit as its load. The transistors T_3 and T_4 are cross-coupled, collector to base, so as to be alternately conducting. The emitters of the transistors T_3 and T_4 are connected through a diode D_4 which holds the emitters at about 0.6 volts above earth potential. The transistor T_3 is initially conducting whereby the lamp L is extinguished and the base of the transistor T_3 is at about 1.2 volts above earth potential allowing for a 0.6 volt drop between the base and emitter of the transistor T_3. The set signal from the input circuit A is applied at the junction of resistors R_5 and R_4 to the bistable circuit B.

The OR gate G consists of a group of diodes D_2 (only 3 of which are shown).

Each diode D_2 applies the set signal from an individual one of the input circuits A_a to A_k to the reset circuit. Only the connection for the input circuit A of Fig. 2 is shown.

The reset circuit R has three cascade connected transistors T_5, T_6 and T_7, the set

signal input to the reset circuit being applied to the base of the transistor T_5 and the reset output from the reset circuit being taken from the emitter of the transistor T_7 and applied to the base of transistor T_3 of each bistable circuit B. The connection for applying the reset signal from the reset circuit R is shown only in the case of the bistable circuit B of Fig. 2 and includes a diode D_3 and the resistor R_4.

In the reset circuit R, T_5 is initially saturated and so its base is at about 0.6 volts above earth potential. D_2 and the other diodes in the OR-gate G are, therefore, reverse-biased because the base of the transistor T_3 is at about 1.2 volts above earth potential. T_6 and T_7 are cut off and the output voltage from R is about 0.2 volts above earth potential, reverse-biasing D_3 and the corresponding diodes in the other bistable circuits.

When K is touched, current which previously flowed through R_3 into the base of T_3 is diverted into A. When this current is sufficient to bring T_3 out of saturation B switches and the lamp L lights. The base voltage of transistor T_3 therefore falls, D_2 conducts and the reset circuit R operates, causing the output from the reset circuit R to rise. Since the reset signal is connected through D_3 and R_4 back to the input of the OR gate G, the OR gate G, reset circuit R, diode D_3 and resistor R_1 behave as a negative-feedback amplifier. The current fed back through R_4 is therefore less than the current drawn by A. The requirement that the set signal should predominate over the reset signal is, therefore, met. All the bistable circuits receive a reset signal and this will be effective on any bistable circuit not simultaneously receiving a set signal. The circuit is so designed that if the current drawn by A is sufficient to set B, it is also sufficient to make R give its full output. While the operator's finger remains on the key K, the base voltage of the transistor T_3 will be negative with respect to ground. When he removes it, this base voltage rises, and as it goes above ground potential T_5 conducts again and the reset output falls.

B could not reset unless the base of the transistor T_3 rose to at least 1 volt, and once the set output from the input circuit A has fallen there is no longer any possibility of this happening. The requirement that the reset signal must terminate before the set signal is thus met.

The input circuits may each be limited to a single transistor in which case the resulting diminution of each set signal would cause the output from each bistable circuit to be insufficient to operate the lamps L. This deficiency may be made up by providing each bistable circuit with an additional amplifying transistor. An advantage of such an arrangement is that since the set signal is diminished, the reset signal may be diminished correspondingly. The reset circuit may thus be provided with two instead of three transistors.

WHAT WE CLAIM IS:—

1. An interlock circuit having a plurality of bistable circuits each switchable between two stable states, a plurality of input circuits corresponding respectively to the bistable circuits, each input circuit being operable to apply to the corresponding bistable circuit a set signal effective to switch the bistable circuit to one of its stable states if in the other, and a negative feedback circuit connected to receive as input the set signal applied to any one of the bistable circuits, the negative feedback circuit being connected and arranged to feed back to its input and to each bistable circuit a reset signal, the reset signal being nullified by the set signal at every bistable circuit which simultaneously receives both set and reset signals, the reset signal being effective at each bistable circuit not simultaneously receiving a set signal to switch the bistable circuit to the said other stable state if in the said one stable state.

2. A circuit according to claim 1, wherein each input circuit has a key by means of which the input circuit can be operated.

3. A circuit according to claim 2, wherein each input circuit comprises a bridge which is normally balanced but which can be unbalanced by means of the key, the bridge producing an unbalance signal from which the set signal of the input circuit is derived.

4. A circuit according to claim 3, wherein the unbalance of the bridge can be effected by a human operator touching the key and so introducing capacitance into the bridge circuit.

5. A circuit according to claim 3 or 4, wherein the bridge circuit is supplied with pulses which, upon unbalance of the bridge cause a capacitor to be charged through a rectifying circuit, the change of potential across the capacitor resulting from unbalance of the bridge constituting the set signal of the input circuit.

6. A circuit according to any one of the preceding claims, wherein the negative feedback circuit comprises an OR gate having one gating path for each bistable circuit, and an amplifier connected to receive the set signal from each bistable circuit through the gating path thereof, biassing means being provided to reverse bias all the gating paths to be non conductive in the absence of a set signal.

7. A circuit according to claim 6, wherein the gating paths of the OR gate are each constituted by a rectifying circuit.

8. A circuit according to claim 8, wherein a plurality of further rectifying circuits are provided, one for each bistable circuit, each further rectifying circuit being arranged to

derive the reset signal for the bistable circuit thereof from the amplified output, the further rectifying circuits being reverse-biased by the biassing means in the absence of a set signal.

9. A circuit according to claim 6, 7 or 8, wherein each bistable circuit includes a pair of transistors cross-coupled from collector to base, the biassing means including the base-emitter junction of one of the transistors from each bistable circuit.

10. A circuit according to claim 9, wherein the transistors of each bistable circuit have their emitters connected to a point of fixed reference potential through a normally conductive diode.

11. A circuit according to any one of the preceding claims, wherein the bistable circuits are associated respectively with a plurality of indicators, the state occupied by any one bistable circuit being indicated by the associated indicator.

12. A circuit according to claim 11, wherein each indicator is a lamp.

13. An interlock circuit substantially as hereinbefore described with reference to and consturcted in accordance with the circuit diagrams of Figs. 1 and 2.

For the Applicants,
F. N. BLAKEMORE,
Chartered Patent Agent.

Leamington Spa: Printed for Her Majesty's Stationery Office by the Courier Press.—1967.
Published at The Patent Office, 25, Southampton Buildings, London, W.C.2, from which copies may be obtained.

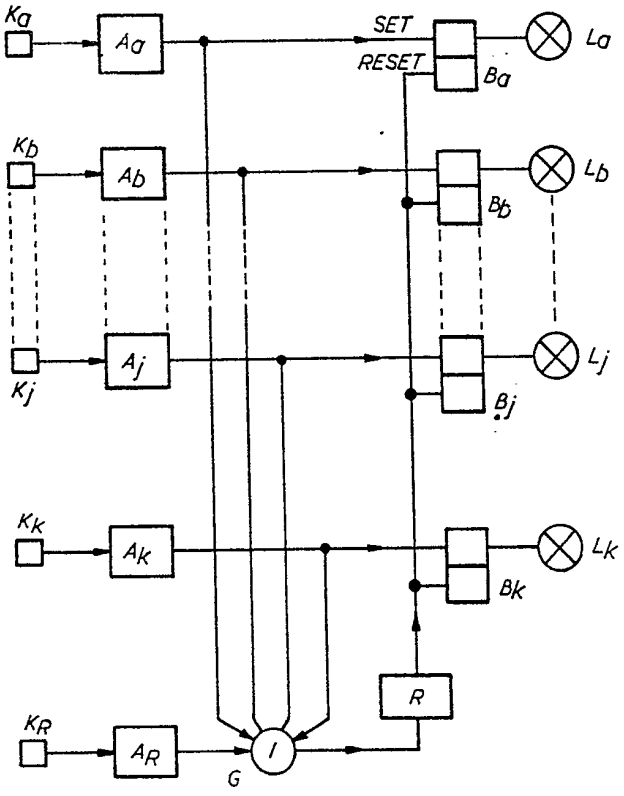

FIG. 1

1082426 COMPLETE SPECIFICATION
2 SHEETS *This drawing is a reproduction of the Original on a reduced scale*
Sheets 1 & 2

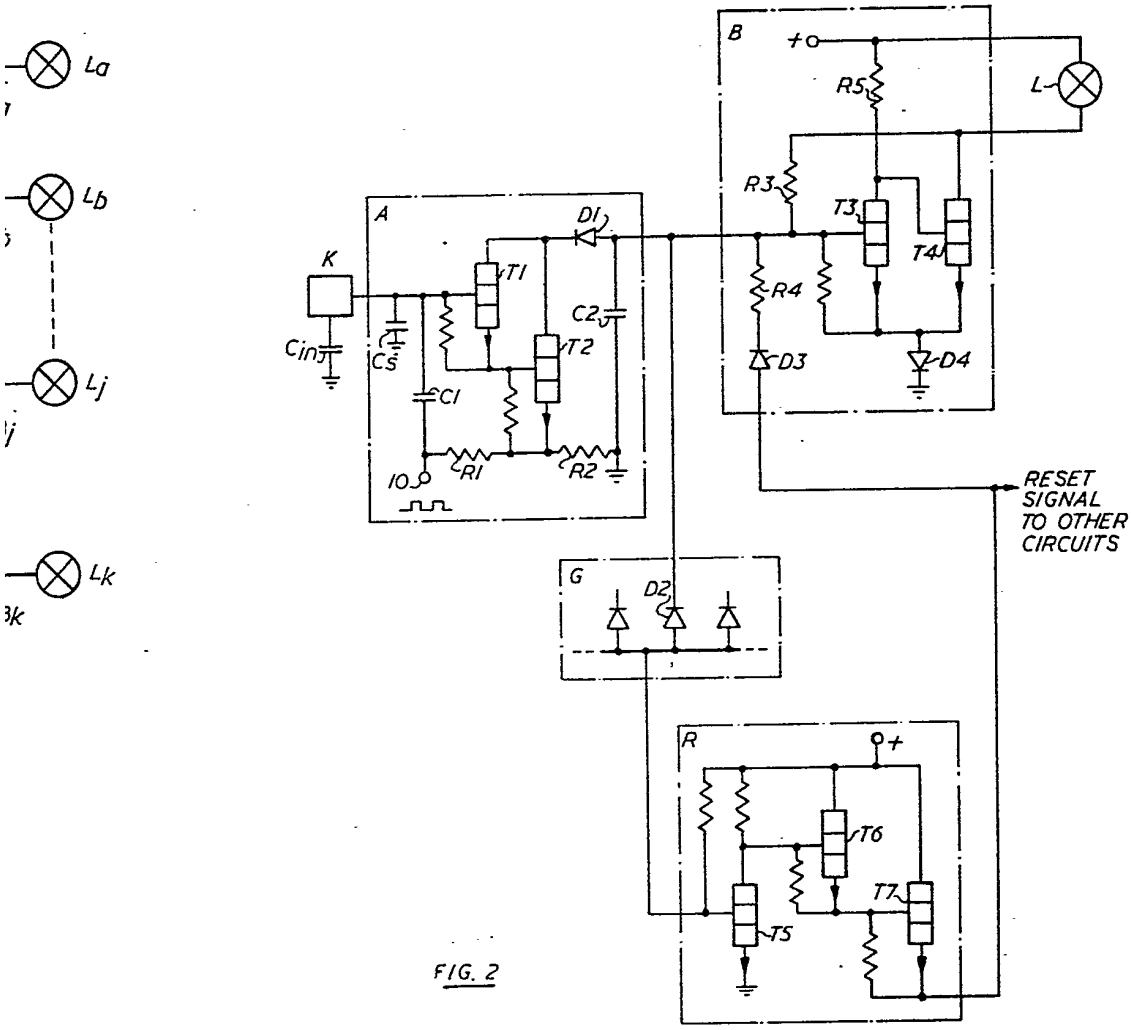

FIG. 2

1082426 COMPLETE SPECIFICATION
2 SHEETS This drawing is a reproduction of the Original on a reduced scale
Sheets 1 & 2

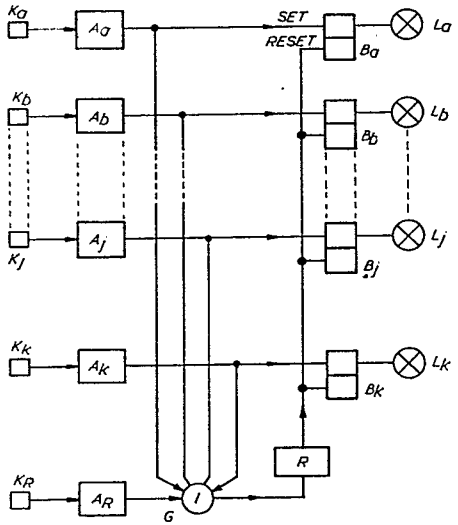

FIG. 1

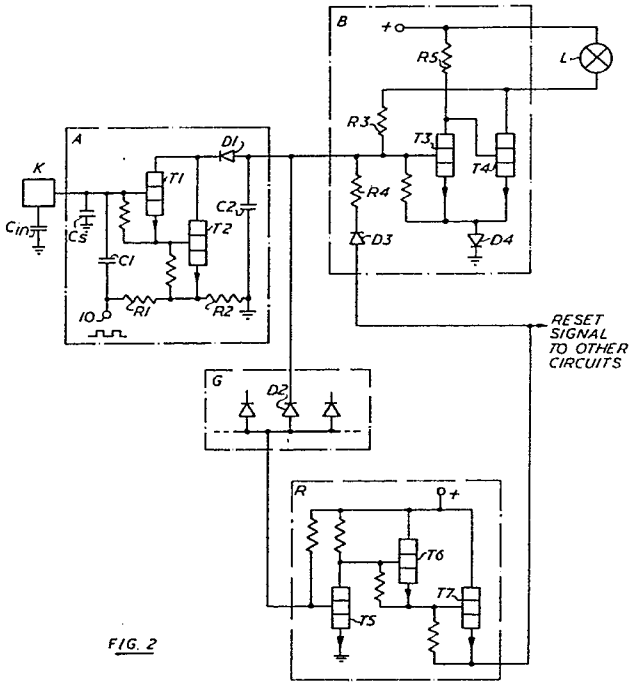

FIG. 2