PATENT SPECIFICATION

999,752

DRAWINGS ATTACHED

999,752

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Int. Cl.:—G 06 f

COMPLETE SPECIFICATION

Improvements in Control Systems for Electronic Calculators and the like

We, INTERNATIONAL BUSINESS MACHINES CORPORATION, a Corporation organised and existing under the laws of the State of New York, United States of America, of Armonk, New York 10504, United States of America do hereby declare the invention for which we pray that a patent may be granted to us, and the method by which it is performed, to be particularly described in and by the following statement:—

This invention relates generally to digital electric calculating apparatus and particularly to such apparatus embodying a matrix for controlling arithmetic and other operations.

The technique of controlling a calculator by a matrix is well known and has been shown to be very powerful. A typical control matrix comprises an array of magnetic cores containing a number of multi-digit words, any one of which can be selected by coincident current techniques by specifying a particular address. The arrangement is such that the selection of a word generates a number of control pulses, certain of which specify the address of the next word and the remainder specify the function to be performed. Thus, by selecting one word at a particular address a sequence of words can be specified. Such a sequence defines a succession of basic machine operations known as a microprogram. Other forms of control matrix employ arrays of diodes or resistors, usually arranged to form the type of store known in the art as a "read-only" store.

It often happens that in the execution of a microprogram certain machine conditions occur which require a different sequence to be followed from that currently in use. In other words, facilities for conditional branching are desirable.

According to the invention we provide a control system for an electronic calculator or the like comprising a storage array having a plurality of address means each adapted when energised to cause an associated control pattern to be developed on a plurality of sense lines in which said address means are divided into two or more groups which may be separately selected for energisation under the control of signals emitted by said calculator whereby different parts of said array may be caused to develop control patterns according to calculator conditions manifested by such signals.

A preferred form of control system embodying the invention comprises a matrix of bistable elements, driving means coupled to said elements and selectively operable to change their state, and gating means responsive to a change in state of an element to condition said driving means to change the state of another element, in which said driving means are divided into groups, each group being associated with a separate sub-matrix of elements within said matrix, and said gating means are operable under the control of conditional control signals to select a group of driving means and thus a sub-matrix within which the next element to be changed in state occurs.

The bistable elements may be magnetic cores, in which case the driving means would typically include an array of row and column drive conductors, and each group of driving means would include a set of row and a set of column conductors. Each element may be threaded by a number of sense wires connected to control the selection of the next element to be changed in state.

In a preferred embodiment of the invention, to be described in detail hereinafter, the matrix has four sub-matrices, each having an associated group of row and column drive conductors. Selection of a sub-matrix is accomplished by simple binary switches, one arranged to select one of two sets of row conductors and the other arranged to select one of two sets of column conductors.

[P

In order that the invention may be fully understood, a preferred embodiment thereof will now be particularly described with reference to the drawing accompanying the provisional specification which is a schematic diagram of a control matrix embodying the invention, having provision for four-way conditional branching.

Referring to the drawing, there is shown a control matrix 1 adapted to deliver a 46-bit output each time a core is changed in state. The matrix 1 contains 576 cores arranged in 24 rows and 24 columns, and is threaded by 46 sense windings 2, each of which threads only those cores whose change in state is required to produce an output pulse on the associated winding. The average number of sense windings on each core is about 4, i.e. only 4 out of the 46 available control matrix bits are in the " one " state for any particular microinstruction. The microprogram of a particular operation, such as an add instruction, consists of a sequence of control matrix cores, threaded with their appropriate control signal windings.

In order to achieve a sequence of signals from the control matrix, 8 additional sense windings 3a, 3b are provided so that each core can supply the address of the next in the sequence. 4 of these windings (3a) specify one of the 12 row addresses of the matrix, the other 4 (3b) one of the column addresses. These windings are taken to two core decoders 4a, 4b each arranged to produce an output on one of 12 lines. The column outputs may be switched at a binary switch 8 to drive the left or right hand halves of the matrix depending on the output from a column conditional gate 5. Similarly the row outputs can be switched at a switch 9 to drive the top or bottom half of the matrix depending on the output of a row conditional gate 6.

It will be observed that this addressing system is not unique, as a single address may select one of four cores in equivalent positions in each quarter of the matrix, depending on the outputs of the conditional gates. This is the method by which the control matrix takes decisions (i.e. branches in the microprogram) on the basis of signals from the computer (such as a carry), the operator, or an input unit. There are in all 25 of these conditional signals, 13 of which may switch the row address and 12 the column address. Flexibility is significantly increased by the provision that any core may select one row condition and one column condition for the next cycle by means of 8 further wires 7a, 7b which are threaded through the control matrix, 4 to specify the row condition and 4 the column condition. These signals are taken to their respective conditional gates and decoded for comparison with conditional signals manifested by the computer so that the effect of the system is to switch the address from left to right if the specified column condition is satisfied and from top to bottom if the specified row condition is satisfied. This makes possible a 2-way or 4-way branch in the microprogram. To increase the flexibility of the system, one of the cores in both the column and row decision windings is arranged to produce an unconditional branch.

The addition of the addressing and conditional system increases the total number of sense windings threading the matrix to 62, and the average number of sense windings per core to about 8.

It is seen, therefore, that a microprogram is executed as a sequence of steps, each of which may specify a condition or conditions which are to be tested. If the specified condition is present, a branch will occur to another portion of the control matrix, depending on the type of condition specified. Otherwise the microprogram will proceed without branching. A special case of conditional branching occurs when a microprogram is to be ended. A typical example is in a division routine where a signal will be developed indicating that the final quotient digit has been extracted. This signal, which will be a negative balance signal, is applied to the conditional gates of the control matrix so that when a microinstruction calls for a test for negative balance, a branch will occur into a routine which controls the replacement of the program instruction which has now been completed by the next program instruction to be executed. This program instruction will select another address in the control matrix, and the appropriate routine will be followed.

WHAT WE CLAIM IS:—

1. A control system for an electronic calculator or the like comprising a storage array having a plurality of address means each adapted when energised to cause an associated control pattern to be developed on a plurality of sense lines in which said address means are divided into two or more groups which may be separately selected for energisation under the control of signals emitted by said calculator whereby different parts of said array may be caused to develop control patterns according to calculator conditions manifested by such signals.

2. A system as claimed in claim 1 comprising a matrix of bistable elements, driving means coupled to said elements and selectively operable to change their state, and gating means responsive to a change in state of an element to condition said driving means to change the state of another element, in which said driving means are divided into groups, each group being associated with a separate sub-matrix of elements within said matrix, and said gating means are operable under the control of conditional control signals to select a group of driving means and thus a sub-

matrix within which the next element to be changed in state occurs.

3. A system as claimed in claim 2 in which said bistable elements are cores of magnetisable material exhibiting a substantially rectangular hysteresis loop.

4. A system as claimed in claim 3 in which said driving means include an array of row and column drive conductors arranged for coincident current selection, said drive conductors being arranged in two or more sets.

5. A system as claimed in any of the preceding claims in which each control pattern includes a group of condition testing signals and means are provided for comparing said condition testing signals with condition manifesting signals emitted by said calculator whereby a part of said array is selected for subsequent energisation in accordance with the result of the comparison.

6. A control system for an electronic calculator or the like substantially as described with reference to the drawing accompanying the provisional specification.

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Chartered Patent Agent,
Agent for the Applicant.

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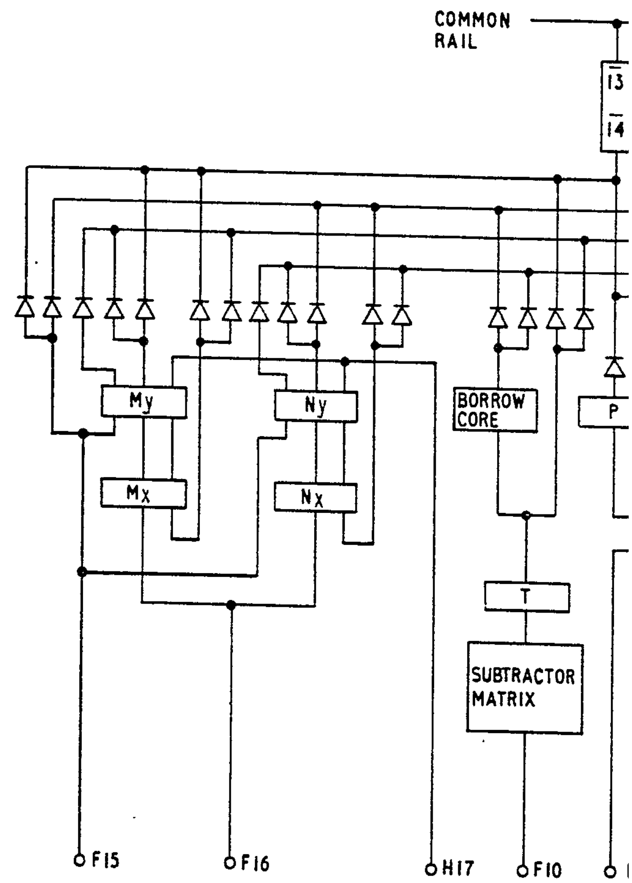

COMMON
RAIL
13
14
My
Ny
Mx
Nx
BORROW
CORE
P
T
SUBTRACTOR
MATRIX
F15
F16
H17
F10

FIG. 1

999752 COMPLETE SPECIFICATION

9 SHEETS *This drawing is a reproduction of the Original on a reduced scale*

Sheet 1

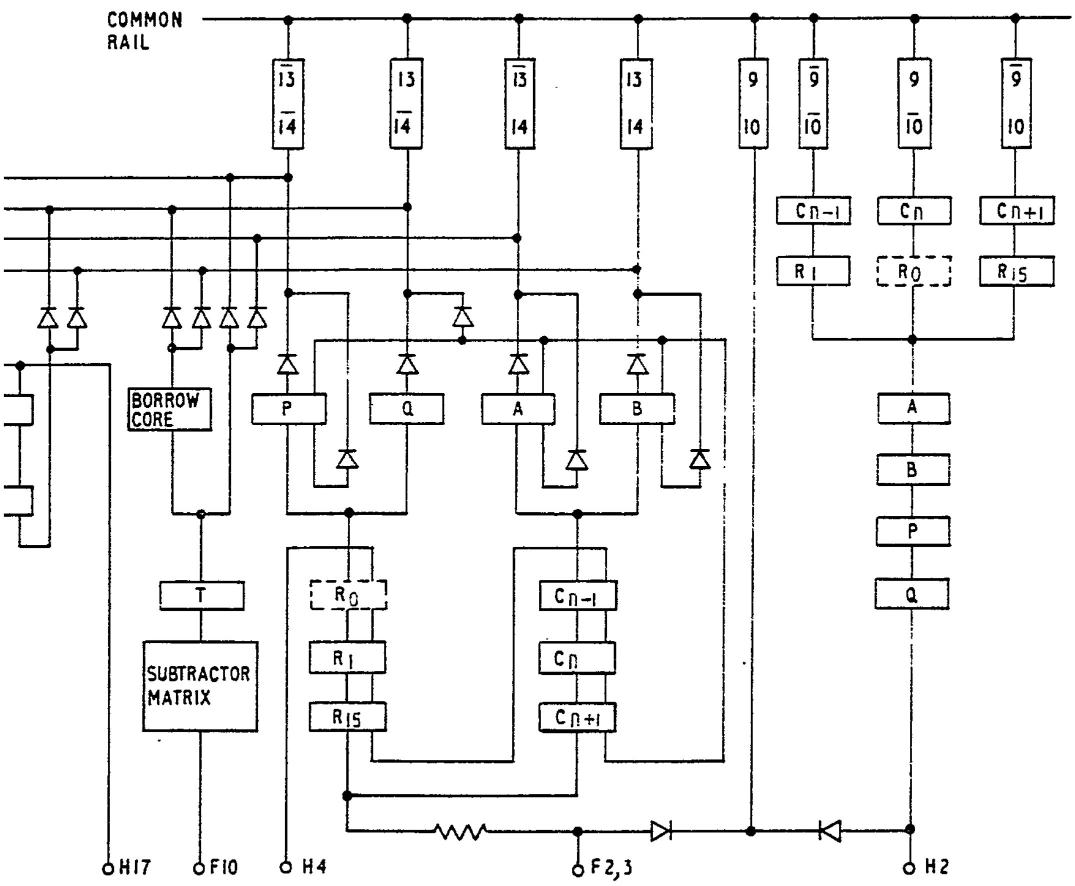


FIG. 1

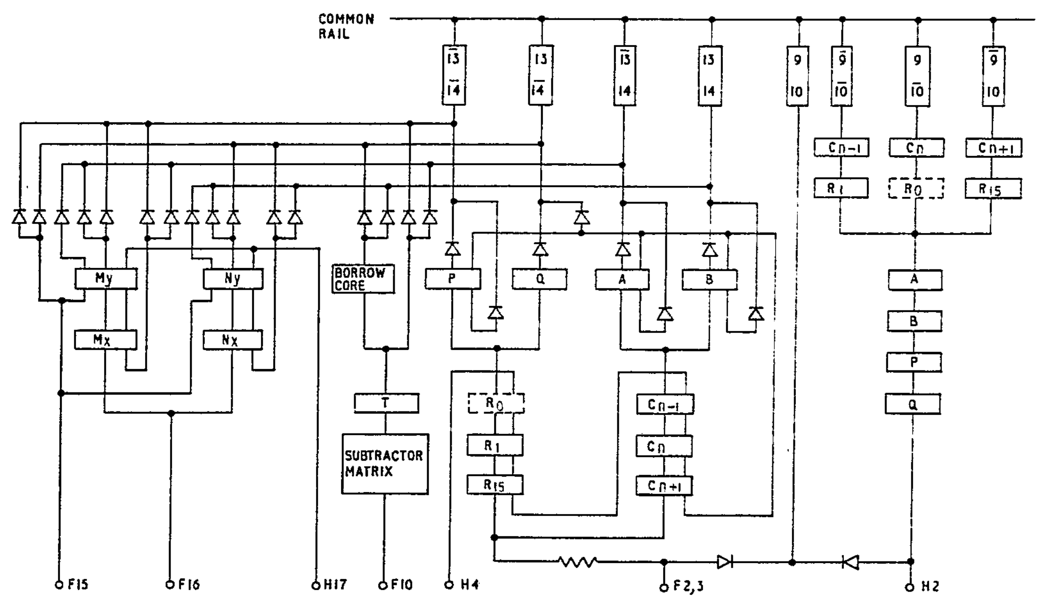
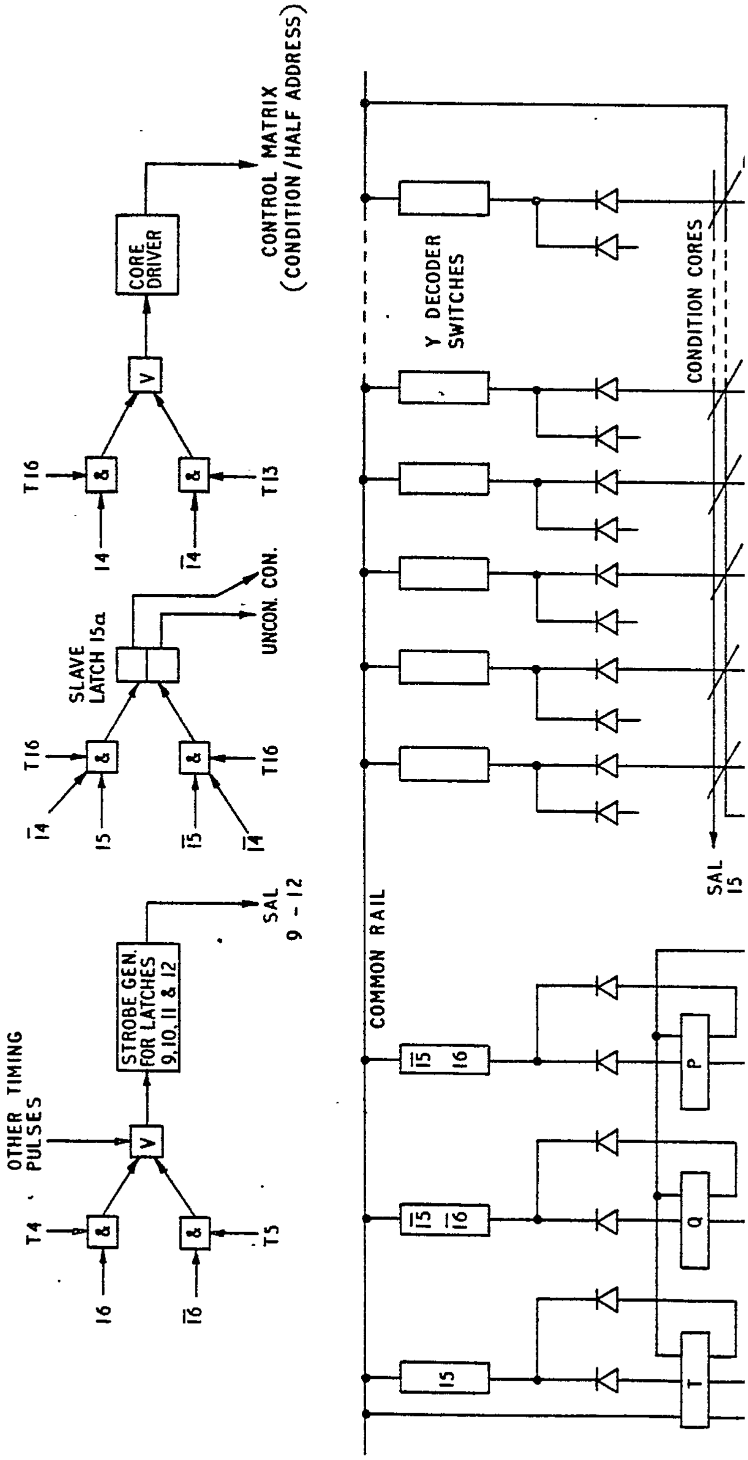

COMMON RAIL
BORROW CORE
SUBTRACTOR MATRIX
T
My
Mx
Ny
Nx
P
Q
A
B
R_0
R_1
R_{15}
C_{n-1}
C_n
C_{n+1}
R_i
F15
F16
H17
F10
H4
F2,3
H2

FIG. 1



CONTROL MATRIX (CONDITION / HALF ADDRESS)
CORE DRIVER
T16
T13
SLAVE LATCH 15a
UNCON. CON.
STROBE GEN. FOR LATCHES 9, 10, 11 & 12
SAL 9 - 12
OTHER TIMING PULSES
T4
T5
Y DECODER SWITCHES
CONDITION CORES
SAL 15
COMMON RAIL
P
Q
T

FIGURE 2

999752 COMPLETE SPECIFICATION

9 SHEETS *This drawing is a reproduction of the Original on a reduced scale*

Sheets 2 & 3

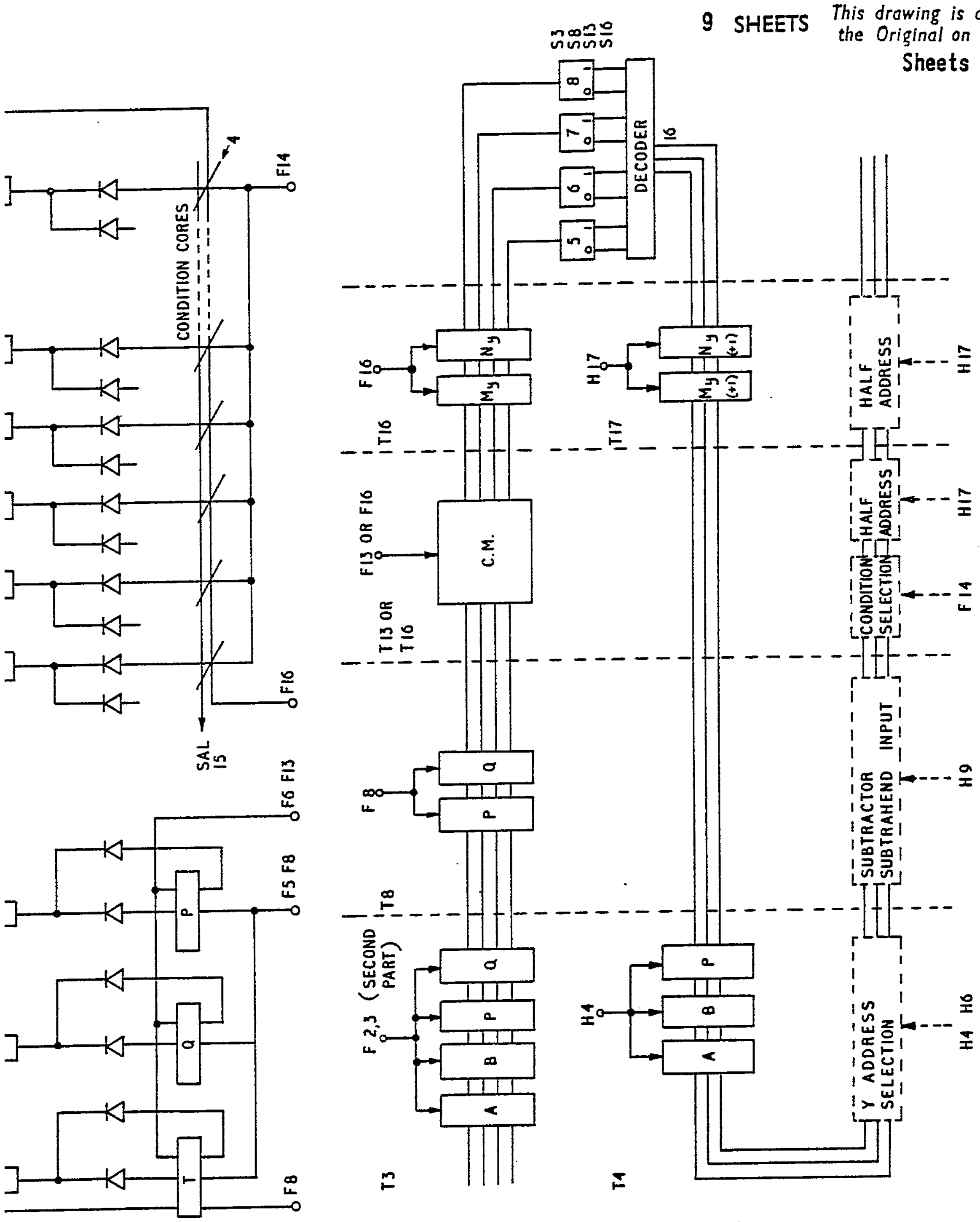


FIGURE 3

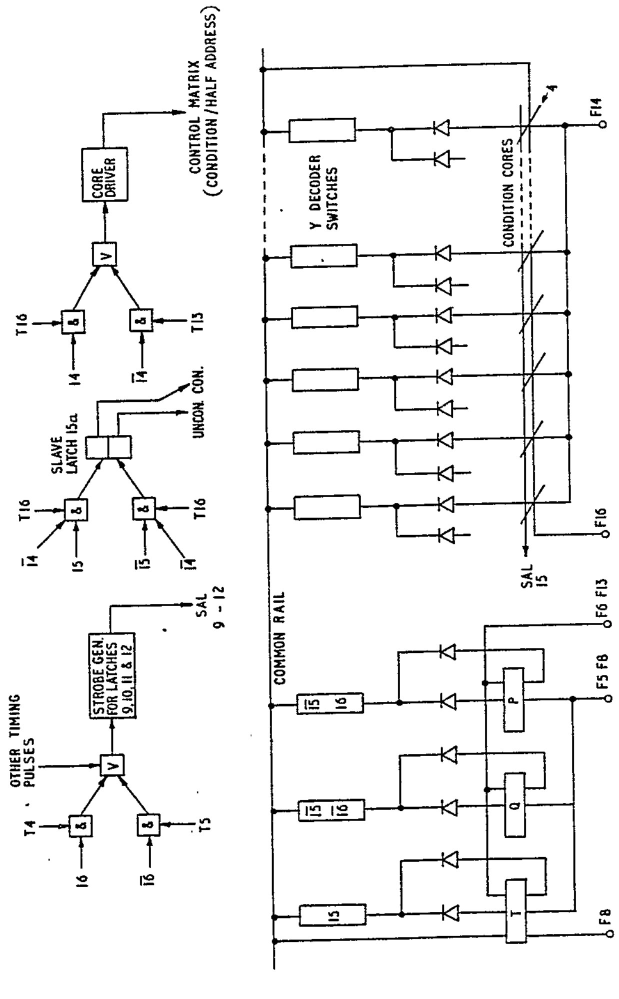


FIGURE 2

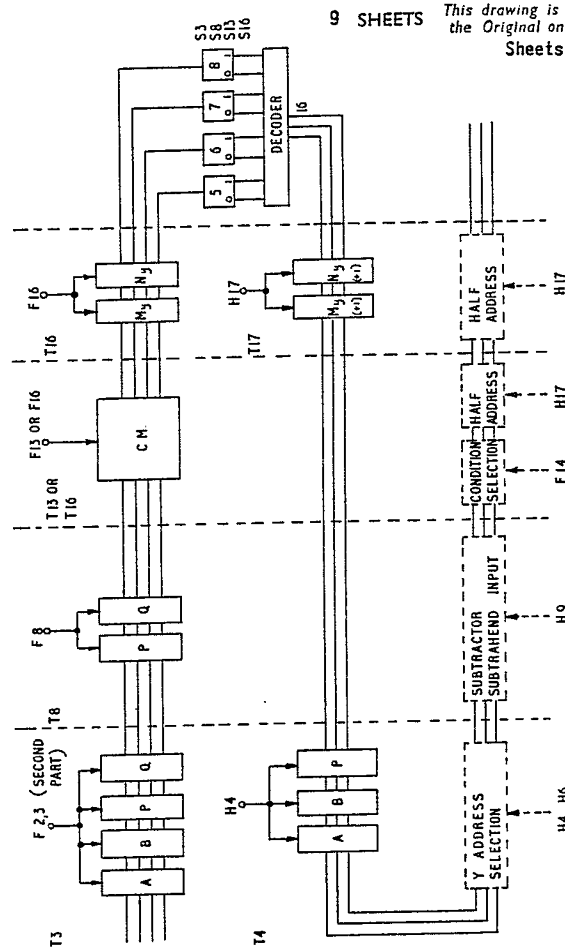


FIGURE 3

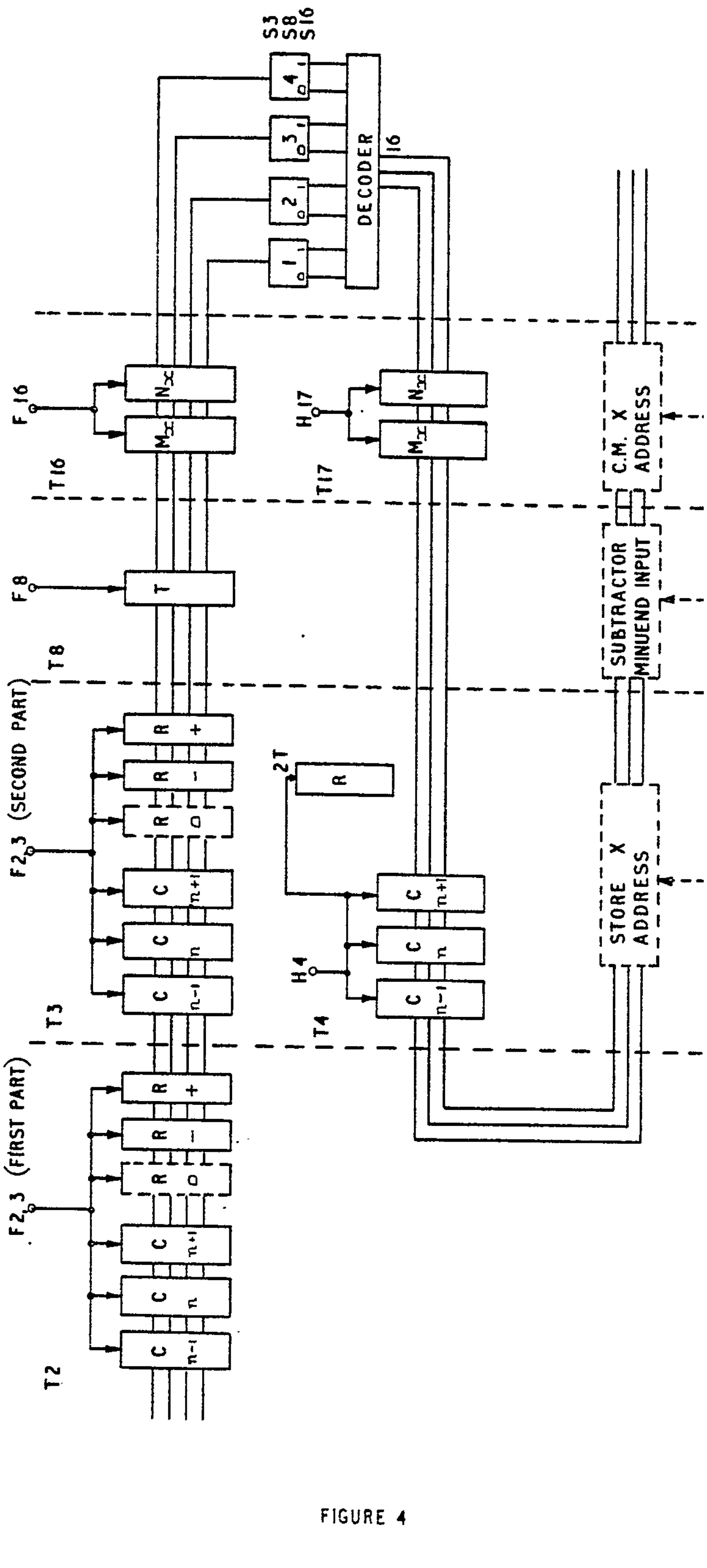

S3
S8
S16
DECODER
16
F16
T16
H17
T17
F8
T8
(SECOND PART)
(FIRST PART)
T3
T4
T2
H4
2T
STORE X
ADDRESS
SUBTRACTOR
MINUEND INPUT
C.M. X
ADDRESS

FIGURE 4

999752 COMPLETE SPECIFICATION

9 SHEETS *This drawing is a reproduction of the Original on a reduced scale*

Sheets 4 & 5

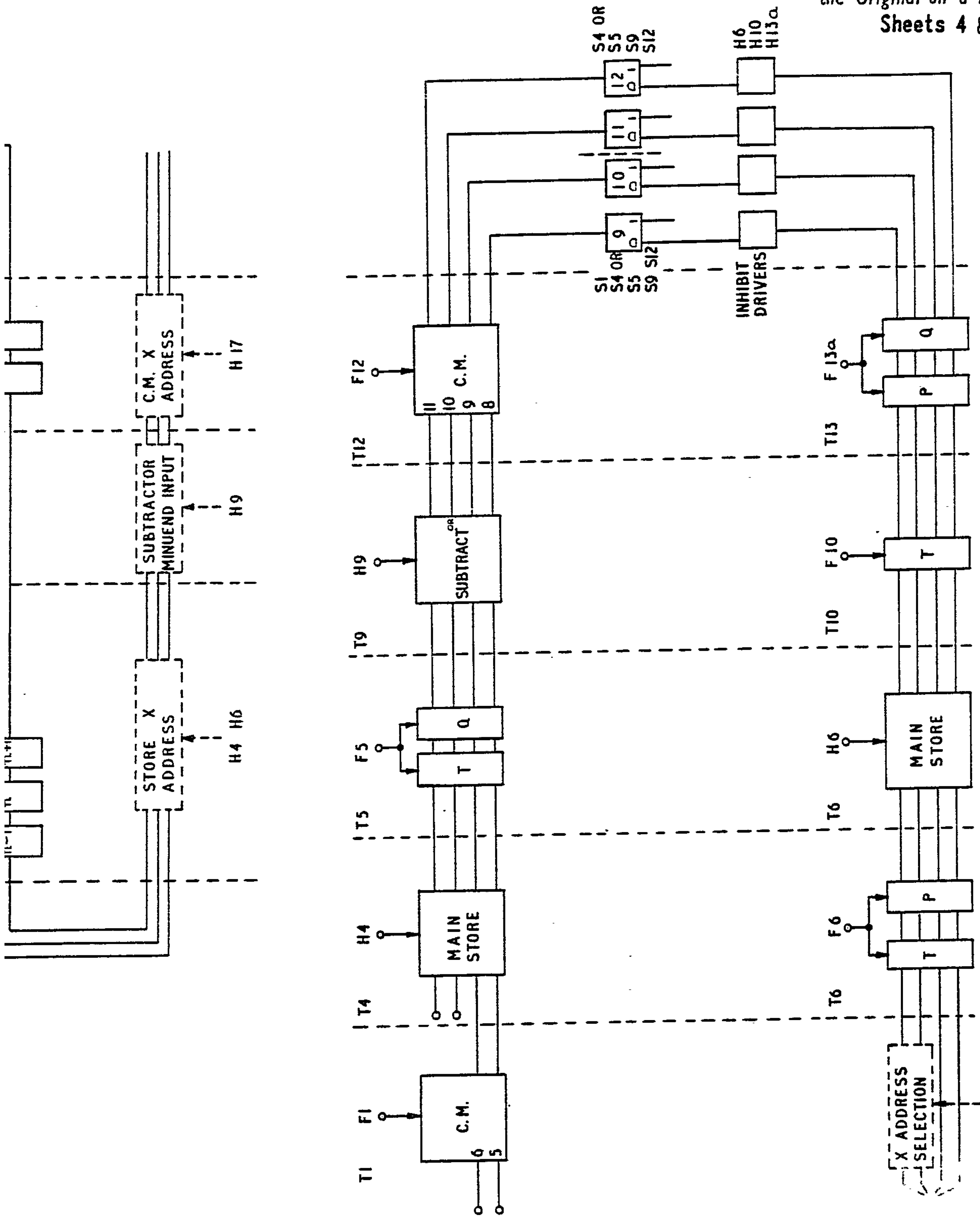


FIGURE 5

999752 COMPLETE SPECIFICATION

9 SHEETS *This drawing is a reproduction of the Original on a reduced scale*

Sheets 4 & 5

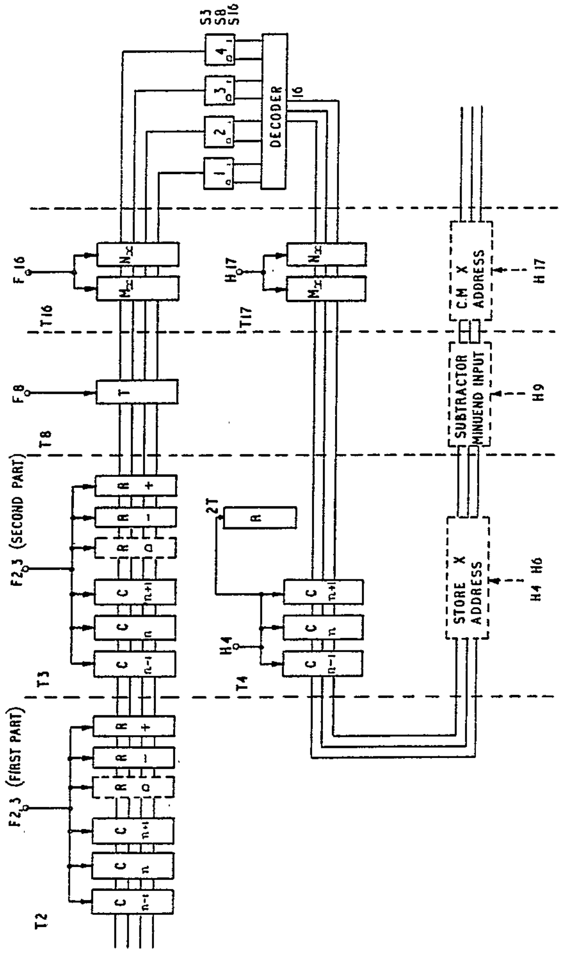


FIGURE 4

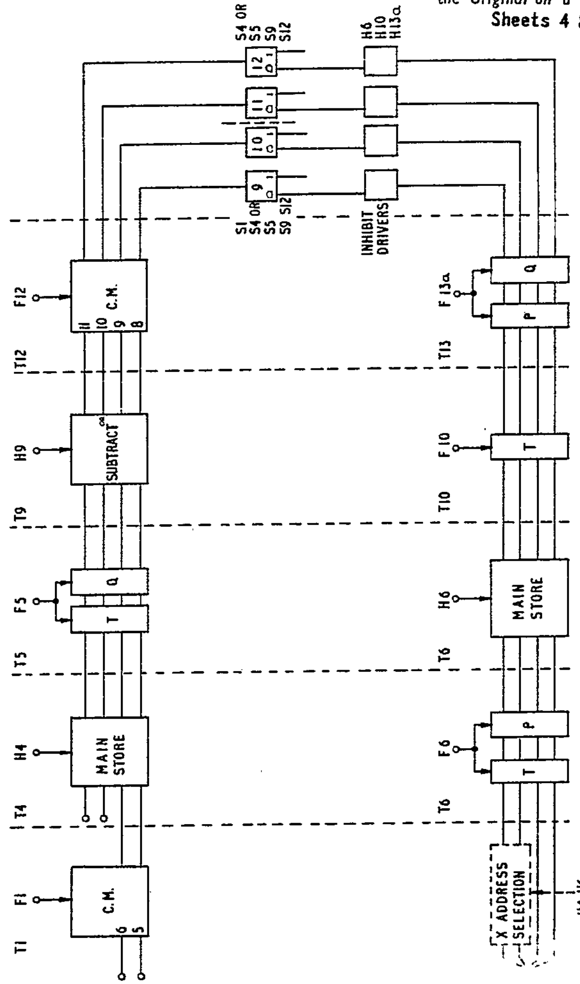
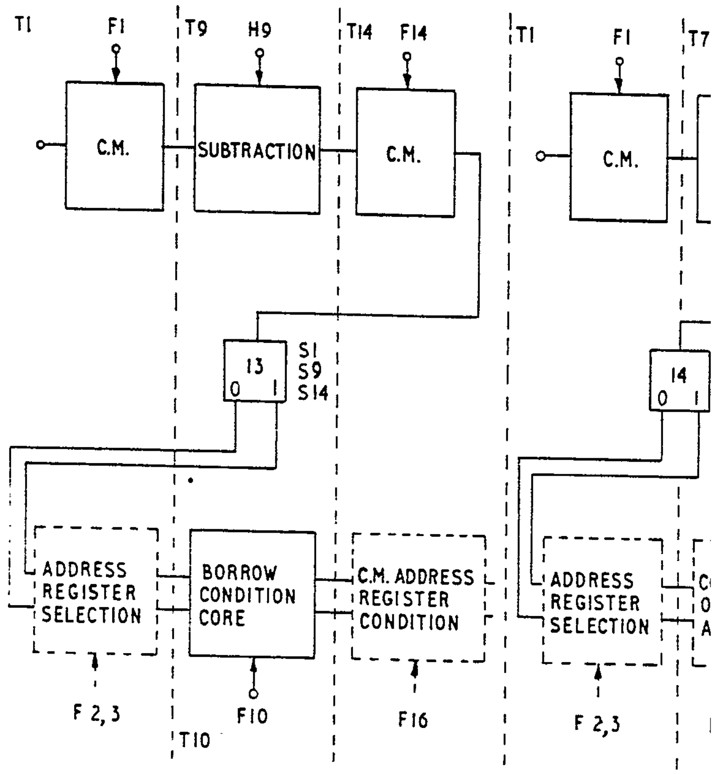


FIGURE 5


T1
F1
T9
H9
T14
F14
T1
F1
T7
C.M.
SUBTRACTION
C.M.
C.M.
13
0
1
S1
S9
S14
14
0
1
ADDRESS REGISTER SELECTION
BORROW CONDITION CORE
C.M. ADDRESS REGISTER CONDITION
ADDRESS REGISTER SELECTION
F 2,3
F10
F16
F 2,3
T10

999752 COMPLETE SPECIFICATION

9 SHEETS *This drawing is a reproduction of the Original on a reduced scale*

Sheet 6

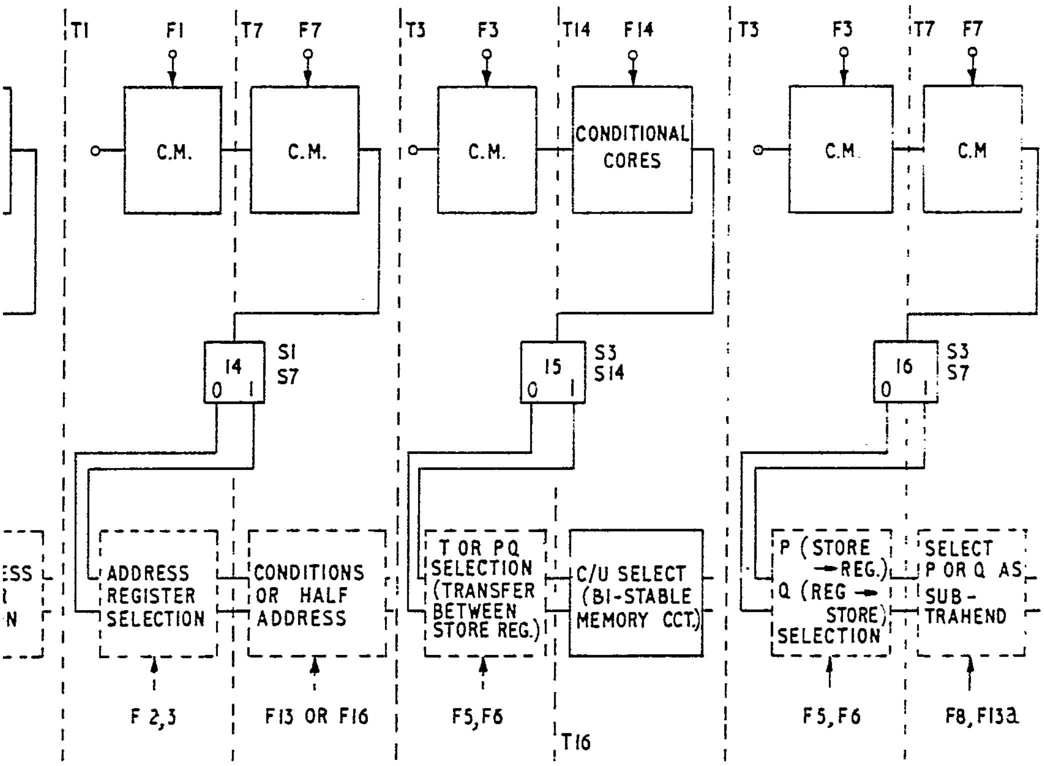


FIG. 6

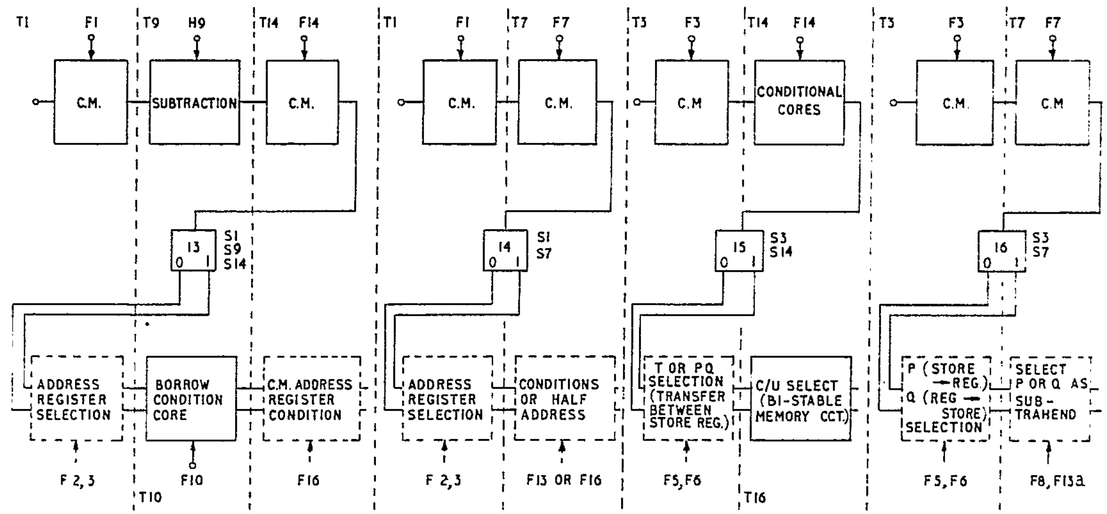

T1
F1
C.M.
T9
H9
SUBTRACTION
T14
F14
C.M.
13
S1
S9
S14
ADDRESS REGISTER SELECTION
F 2,3
BORROW CONDITION CORE
F10
T10
C.M. ADDRESS REGISTER CONDITION
F16
T1
F1
C.M.
T7
F7
C.M.
14
S1
S7
ADDRESS REGISTER SELECTION
F 2,3
CONDITIONS OR HALF ADDRESS
F13 OR F16
T3
F3
C.M
T14
F14
CONDITIONAL CORES
15
S3
S14
T OR PQ SELECTION (TRANSFER BETWEEN STORE REG.)
F5,F6
C/U SELECT (BI-STABLE MEMORY CCT.)
T16
T3
F3
C.M.
T7
F7
C.M
16
S3
S7
P (STORE → REG.)
Q (REG → STORE)
SELECTION
F5,F6
SELECT P OR Q AS SUB-TRAHEND
F8, F13a

FIG 6

15	15	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
14	14	8	9	10	11	0	1	2	3	4	0	8	0	0	0	0
13	5	5	6	6	7	7	8	8	9	9	0	0	0	0	0	0
12	0	0	1	1	2	2	3	3	4	4	5	5	6	6	7	7
11	1	2	3	4	5	6	7	8	9	10	11	0	0	0	0	0
10	2	3	4	5	6	7	8	9	10	11	0	1	0	0	0	0
9	3	4	5	6	7	8	9	10	11	0	1	2	0	0	0	0
P OR Q 8	4	5	6	7	8	9	10	11	0	1	2	3	0	0	0	0
7	5	6	7	8	9	10	11	0	1	2	3	4	0	0	0	0
6	6	7	8	9	10	11	0	1	2	3	4	5	0	0	0	0
5	7	8	9	10	11	0	1	2	3	4	5	6	0	0	0	0
4	8	9	10	11	0	1	2	3	4	5	6	7	0	0	0	0
3	9	10	11	0	1	2	3	4	5	6	7	8	0	0	0	0
2	10	11	0	1	2	3	4	5	6	7	8	9	0	0	0	0
1	11	0	1	2	3	4	5	6	7	8	9	10	0	0	0	0
0	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

T

FIGURE 7

999752 COMPLETE SPECIFICATION

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Sheets 7 & 9

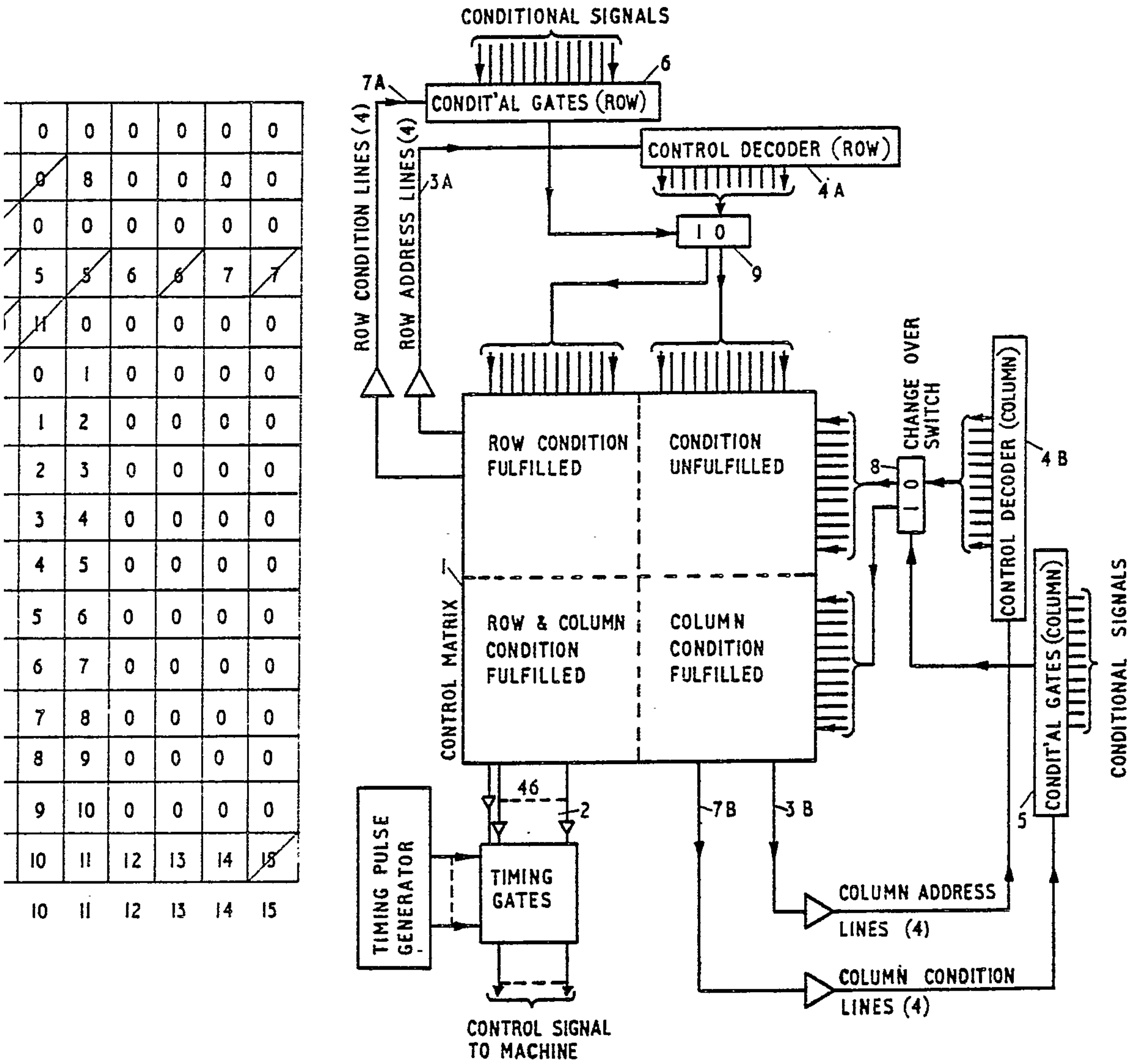


FIGURE 9

P OR Q \ T	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
15	15	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
14	14	8	9	10	11	0	1	2	3	4	0	8	0	0	0	0
13	5	5	6	6	7	7	8	8	9	9	0	0	0	0	0	0
12	0	0	1	1	2	2	3	3	4	4	5	5	6	6	7	7
11	1	2	3	4	5	6	7	8	9	10	11	0	0	0	0	0
10	2	3	4	5	6	7	8	9	10	11	0	1	0	0	0	0
9	3	4	5	6	7	8	9	10	11	0	1	2	0	0	0	0
8	4	5	6	7	8	9	10	11	0	1	2	3	0	0	0	0
7	5	6	7	8	9	10	11	0	1	2	3	4	0	0	0	0
6	6	7	8	9	10	11	0	1	2	3	4	5	0	0	0	0
5	7	8	9	10	11	0	1	2	3	4	5	6	0	0	0	0
4	8	9	10	11	0	1	2	3	4	5	6	7	0	0	0	0
3	9	10	11	0	1	2	3	4	5	6	7	8	0	0	0	0
2	10	11	0	1	2	3	4	5	6	7	8	9	0	0	0	0
1	11	0	1	2	3	4	5	6	7	8	9	10	0	0	0	0
0	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

FIGURE 7

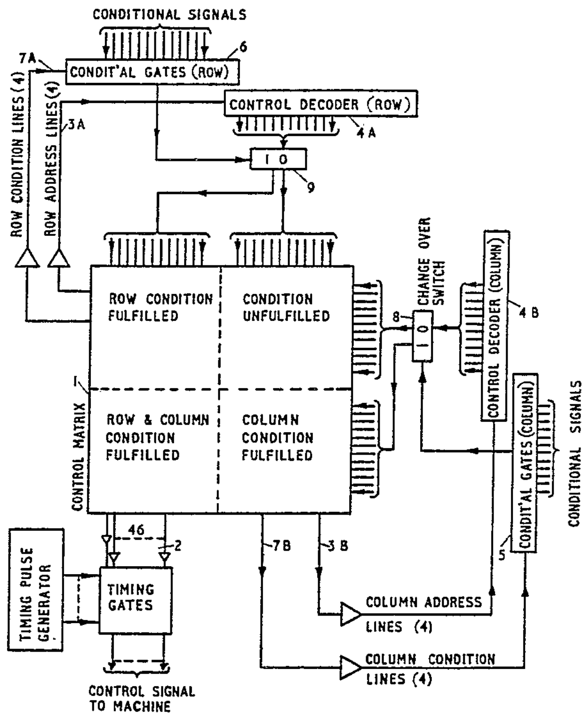
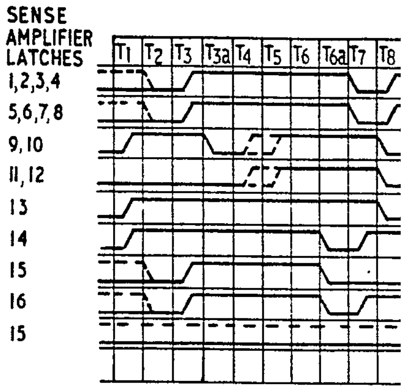


FIGURE 9


SENSE
AMPLIFIER
LATCHES
T1 T2 T3 T3a T4 T5 T6 T6a T7 T8
1,2,3,4
5,6,7,8
9,10
11,12
13
14
15
16
15

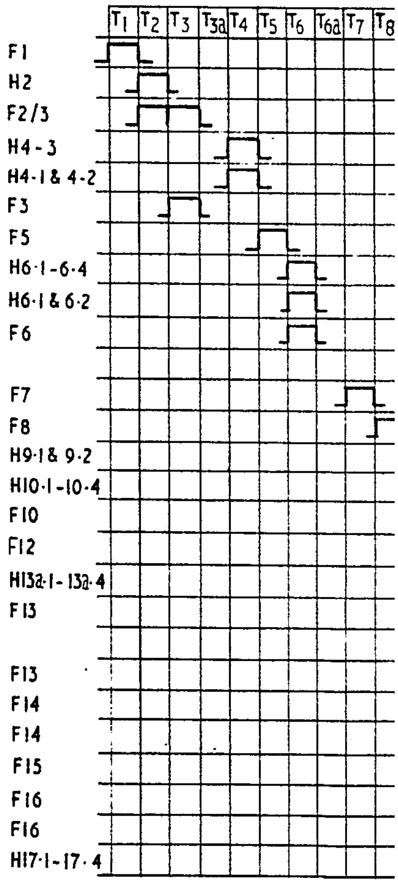
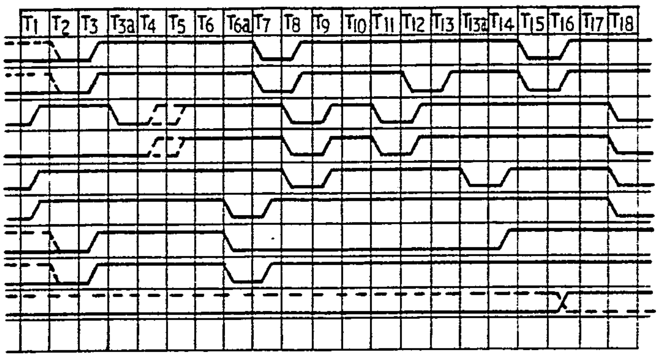

T1 T2 T3 T3a T4 T5 T6 T6a T7 T8
F1
H2
F2/3
H4-3
H4·1 & 4·2
F3
F5
H6·1-6·4
H6·1 & 6·2
F6
F7
F8
H9·1 & 9·2
H10·1-10·4
F10
F12
H13a·1-13a·4
F13
F13
F14
F14
F15
F16
F16
H17·1-17·4

FIG 8

999752 COMPLETE SPECIFICATION

9 SHEETS *This drawing is a reproduction of the Original on a reduced scale*

Sheet 8



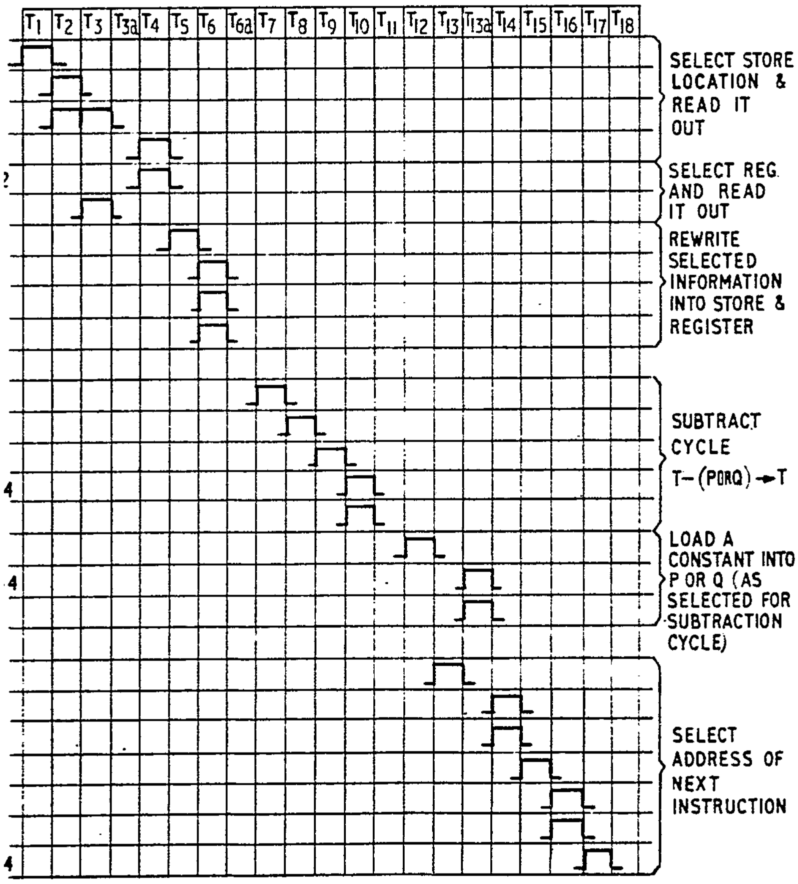


FIG 8

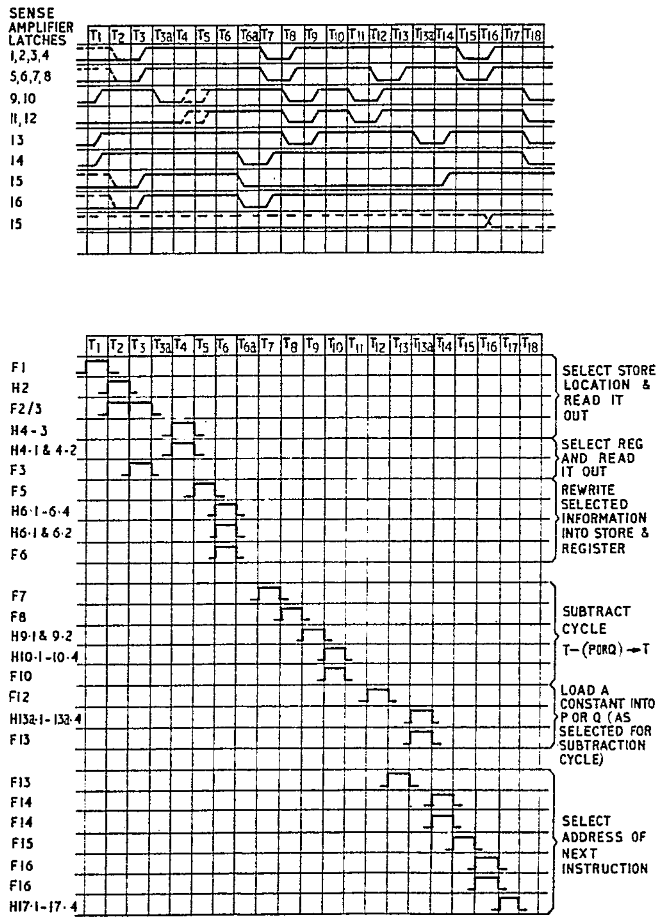
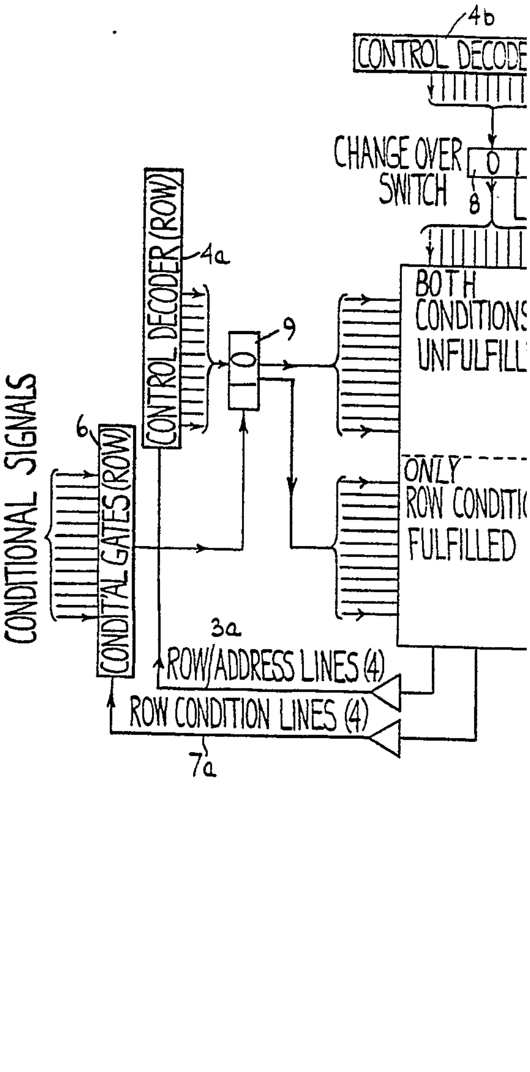
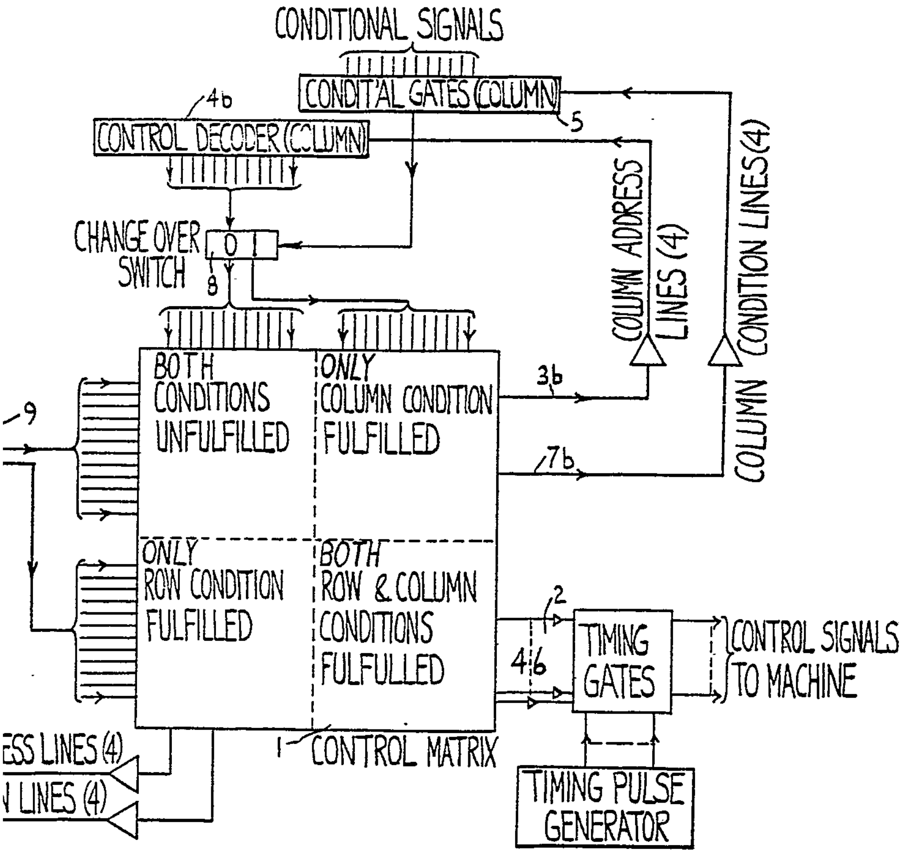

SENSE AMPLIFIER LATCHES
1,2,3,4
5,6,7,8
9.10
11,12
13
14
15
16
15
T1 T2 T3 T3a T4 T5 T6 T6a T7 T8 T9 T10 T11 T12 T13 T13a T14 T15 T16 T17 T18
F1
H2
F2/3
H4-3
H4·1 & 4·2
F3
F5
H6·1-6·4
H6·1 & 6·2
F6
F7
F8
H9·1 & 9·2
H10·1-10·4
F10
F12
H13a·1-13a·4
F13
F13
F14
F14
F15
F16
F16
H17·1-17·4
SELECT STORE LOCATION & READ IT OUT
SELECT REG AND READ IT OUT
REWRITE SELECTED INFORMATION INTO STORE & REGISTER
SUBTRACT CYCLE
T−(P OR Q) → T
LOAD A CONSTANT INTO P OR Q (AS SELECTED FOR SUBTRACTION CYCLE)
SELECT ADDRESS OF NEXT INSTRUCTION

FIG 8



4b
CONTROL DECODE
CHANGE OVER SWITCH
0
8
CONTROL DECODER (ROW)
4a
9
0
1
BOTH CONDITIONS UNFULFILL
CONDITIONAL SIGNALS
6
CONDIT'AL GATES (ROW)
ONLY ROW CONDITI
FULFILLED
3a
ROW/ADDRESS LINES (4)
ROW CONDITION LINES (4)
7a

999752 PROVISIONAL SPECIFICATION
1 SHEET *This drawing is a reproduction of the Original on a reduced scale*



999752 PROVISIONAL SPECIFICATION
1 SHEET *This drawing is a reproduction of the Original on a reduced scale*