PATENT SPECIFICATION

DRAWINGS ATTACHED

Inventors: DANIEL MATTHEW TAUB and CHARLES EDWARD OWEN

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Int. Cl.:—G 06 f 3/14

COMPLETE SPECIFICATION

Improvements in Electronic Digital Computers

We, INTERNATIONAL BUSINESS MACHINES CORPORATION, a Corporation organized and existing under the laws of the State of New York in the United States of America, of Armonk, New York 10504, United States of America do hereby declare the invention for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to electronic digital computers.

It is an object of the invention to provide an electronic digital computer which is particularly suitable for demonstrating the operation of computers and for instructing potential users in the skills of programming.

According to the invention we provide an electronic digital computer comprising a processing unit adapted to operate on data in the form of digital operands in accordance with instructions supplied to the computer and a display control circuit connected to said processing unit and adapted in response to signals indicating that different classes of instructions are being performed by said processing unit to produce display control signals defining different display formats, said display control circuit also including an oscillator modulator unit adapted to impress said display control signals on a radio frequency carrier wave for application as a modulated input to a television receiver.

Where multiple address macroinstructions are provided in a machine embodying the invention the display control circuit may include means responsive to the occurrence of such a macroinstruction to cause the display to present selected stages in the execution of the macroinstruction and to suppress the display of information pertaining to the basic instructions constituting the macroinstruction.

In order that the invention may be well understood a preferred embodiment thereof will now be described with reference to the accompanying drawings, in which:—

FIGURE 1 is a general view of a computer embodying the invention;

FIGURE 2 is a schematic diagram showing the major components of the computer of FIGURE 1;

FIGURE 3 is a schematic diagram of the display circuitry,

FIGURE 4 is a data flow diagram showing the manner in which information is handled in the computer of FIGURE 1;

FIGURE 5 shows the display format;

FIGURES 6, 10 and 11 show examples of displays which are produced with different classes of instructions;

FIGURE 7 shows the keyboard layout in detail;

FIGURE 8 shows the format of data as it is handled by the computer of FIGURE 1, and

FIGURE 9 shows the format of instructions of the different classes which are obeyed by the computer.

Referring first to FIGURE 1, the computer is seen to comprise two basic units, an input/processing module 1 and a display device 2 interconnected by a cable 3. The input/processing module 1 has on its top surface a keyboard 4 which in the preferred embodiment is a capacitive touch keyboard of the type disclosed in our copending applications Nos. 6315/66 (Serial No. 1134704) and 19903/66 (Serial No. 1082426), the keys of which are grouped into different sets 5, 6, 7, 8 according to the function which they

perform. As shown in detail in FIGURE 7 certain keys are used for entering numbers whilst other keys are used for causing specific processing operations to be performed and particular items of data to be displayed.

In the preferred embodiment, the display device is a conventional television receiver, the cable 3 being a coaxial cable arranged to convey signals at VHF from a modulator unit in the module 1 which is adapted to impress a display pattern on a carrier frequency.

FIGURES 2 and 3 show the main components of the input/processor module 1. Referring to FIGURE 2, a magnetic core memory 9 has a capacity of 222 words, each of eight binary coded decimal characters, the individual characters being separately addressable by means of addresses applied to an address bus 10. The construction of the memory 9 is entirely conventional employing well established coincident current access techniques and since it forms no part of the present invention will not be described further.

An adder-subtracter 11 is connected to receive data from the two registers 12 and 13 each having a capacity of 1 character, the register 13 being connected to receive data from the memory 9 by way of register 12. A data path 14 is arranged to return the results of operations performed in the adder-subtracter 11 to the memory 9 and to the register 12. Data from the keyboard 4 can be applied directly to the register 12 and can be entered into the memory 9 by causing it to pass through the adder-subtracter 11 and the data path 14. It will thus be seen that operands can be directed from the memory 9 to the registers 12 and 13 in response to addresses supplied serially on address bus 10, operated on by the unit 11 and returned to the memory 9 for subsequent display or for participation in subsequent operations.

The development of addresses for the memory 9 is performed by two address register systems 15 and 16. As mentioned above there are 222 words of storage in memory unit 9 occupying addresses 000 to 221. Of these addresses those from 00 to 99 are available for the user to store data and instructions, the remaining addresses 100 to 221 being reserved for general purpose registers and sub-routines. The addresses are expressed in binary coded decimal form and since data is accessible on a character basis, there being 8 characters in each word, it is necessary, not only to specify hundreds, tens and units digits, but also to identify the character which is currently being accessed. There is therefore provided a three binary digit character address. The arrangement of address registers is designed to provide for operations on pairs of operands derived as follows: (a) both from registers in the machine (Register-Register operations) or (b) one from a register and one from the memory 9 (Register-Memory operations). The case where both operands are derived from memory is not provided for. This stipulation simplifies the address register system enabling register 15 to consist merely of a units position 17 and a character position 18 with one digit of a tens position 19 whose purpose will be described hereinafter. Address register 16 which is used to specify operands and instructions under the control of the operator requires in addition a tens position 20 together with two digits of hundreds position 21.

The contents of the address registers 15 and 16 are supplied respectively to an A address bus and a B address bus, either one of which may be rendered effective to address the memory 9 by appropriate energisation of one of a pair of AND circuits 22 and 23, which permits the address developed by the associated register to be applied to address bus 10. The three least significant binary digits on address bus 10 are applied to an incrementing/decrementing circuit 24 which is adapted to change the address applied to bus 10 by one character at a time and to return the changed address to the character position of the appropriate register 15 or 16 thereby enabling the characters of a word specified by one of the address registers to be scanned in sequence into the registers 12 and 13.

Addresses for entry into the address registers 15 and 16 can be obtained from the memory unit 9 over the bus 25 which is fed one character at a time from register 12. Alternatively the address may be furnished by a control unit 26 over output lines designated OC. This control unit which in the preferred embodiment of the machine is an assembly of logic gates driven by a timing circuit, is arranged in a conventional manner to produce sequences of control patterns for controlling the flow of data in accordance with the operations required to be performed by the machine and the stage in an operating cycle reached by the machine. It will be appreciated by those skilled in the art that this unit may take other forms, for example a read only store.

In the present arrangement characters specifying the operation to be performed, designated function characters F1 and F2, are entered over the bus 25 into a pair of registers 27 and 28, the contents of which are decoded to specify the pattern which a control unit develops on the lines OC which control the gating of data at various points in the machine. The development of this pattern is also controlled by signals representing the state of the machine applied to the control unit 26 over input lines IC.

Characters for display are supplied over bus 25 to the display circuitry which will be described below with reference to FIGURE 3. First, however, will be given a description

of the format in which information of various types is expressed in the machine, and the registers which take the form of reserved locations in the memory 9 which are employed to handle this information.

When storing a number as distinct from an instruction, the eight digit positions in a word are used as shown in FIGURE 8a. Digit position number 1 stores the sign of the number. Position 2 stores the number of decimal places, i.e. the negative of the exponent; it can have any value from 0 to 6. Positions 3 to 8 store the significant digits, the most significant digit being in position 3 and the least significant in position 8. The numbers can thus range from 0.000001 to 999999, positive or negative. Negative numbers are always handled in 'sign and modulus' form.

Although stored as an integer and exponent, numbers are entered on the keyboard and appear on the display in conventional form, with the decimal point in the appropriate place. Any negative sign is keyed-in after the least-significant digit and is displayed at the right-hand end (see FIGURES 6b and 6c). Positive signs are not keyed-in and do not appear on the display.

General Purpose Registers

Referring to FIGURE 4 there are ten general purpose registers, designated R0 to R9. R0 to R7 are single length registers each storing a sign and six decimal digits and occupying addresses 200 to 207 in memory 9. R8 and R9 are double-length registers, each storing a sign and twelve decimal digits and occupying addresses 208, 218 and 209, 219 in memory 9. When the double length registers are in use the existence of a first carry out of the incrementer/decrementer 24 (FIGURE 2) indicates that half the register has been scanned. Such a carry is applied to the tens position 19 of the address register 15, thereby effecting a change in address by 10, automatically selecting the other half of the register.

In order to access any of these registers, the control unit supplies the appropriate addresses to the registers 15, 16 over the lines OC.

All transfers of data from store to registers and vice versa take place via R0 to R1. The basic 'read store' instruction causes the integer and sign from the appropriate word to be transferred to R1 and the exponent digit to R0. Thereafter they are manipulated separately using the basic instruction set. When a number is to be written back into store, the integer is first set up in R1 and the exponent in R0. The basic 'write into store' instruction combines the contents of these registers and arranges them in the required storage location according to the format of FIGURE 8.

Special-Purpose Registers

R3, R4 and R5, besides serving as general-purpose registers, also serve as Modifier Registers.

In addition the following special purpose registers are provided:—

Keyboard Register in which all information entered on the keyboard is initially stored.

Instruction Address Register (IAR) which holds the address of the next instruction to be carried out.

Instruction Register in which an instruction is held while being executed.

Several True Address Registers (TAR) which hold the true addresses of operands used in basic and macroinstructions.

Link Register used for temporary storage of the link address in "Branch and Link" instructions.

Instruction Format

The instructions for this machine can be divided into three categories:

(i) Basic instructions operating only on the contents of registers (register instructions).

(ii) Basic instructions requiring access to the store (single-address instructions).

(iii) Three-address macroinstructions, each of which is implemented by a routine of basic instructions.

The instructions in categories (i) and (ii) each consist of four decimal digits and are stored two to a word. The macroinstructions each have eight digits and are stored one to a word.

The way in which the various instruction digits are interpreted is given in FIGURE 9. It should be noted that in single address instructions c and d are the tens and units digits of the base address, the hundreds digit being taken from the hundreds digit position of the instruction address register. The user's program is confined to store locations 00 to 99, and so far as he is concerned c and d represent the entire base address. Obtaining the hundreds digit from the IAR is a convenient way of providing 'scratch-pad' storage in locations 100 upwards for the use of the macroinstruction subroutines which reside in that part of the store.

As will be discussed below with particular reference to the display circuitry, the control unit 26 includes a decoder which produces signals indicating that a particular class of instruction is being processed. If the instruction is a basic instruction the operation of the machine is quite straightforward, the instructions being processed one by one in sequence. If the instruction is a macroinstruction, the following action takes place:

(1) The operand addresses are formed and stored at certain of the scratchpad locations specified by the Control Unit.

(2) A latch in the Control Unit is set and

remains so until the routine by which the macroinstruction is implemented is completed. This latch causes the various stages of the macroinstruction to be displayed as if it were a basic instruction. That is to say, the A, B and C stages referred to hereinafter, do not refer to the basic instructions in the routine.

(3) The link address (from the IAR) is stored in the Link Register, and branching takes place to the beginning of the appropriate routine.

Early in the routine, the link address and the operand addresses are stored in the scratchpad area associated with that routine.

Display Formats

The display format is shown in FIGURE 5. It consists of six rows each containing 14 character positions. Rows 1 and 2 are permanently assigned as shown. The remaining four rows display the contents of storage locations or registers, depending on the instruction being carried out and the stage that has been reached.

Row 1

Positions 1 through 4 carry the Instruction Address Register Positions 1, 2 and 3 carry the hundreds, tens and units digits respectively, though, as the user's program is confined to addresses 00 to 99, the hundreds digit will normally be zero. Position 4 is blank if the next instruction starts at the left-hand end of a word; if it is a 4-digit instruction occupying the right-hand half of a word, position 4 carries the letter A. Thus, if for example, the next instruction is to be taken from the right-hand half of the word No. 27, the IAR will be displayed as shown in FIGURE 6a.

Position 5 is always blank.

Positions 6 through 14 are allocated to the Keyboard Register. If this contains an 8-digit instruction the digits appear in positions 6 through 13; if it contains a 6-digit floating-point number, the digits appear in positions 8 through 13 with the decimal point at the appropriate place, and any negative sign in position 14. Positive signs are suppressed, but all zeros entered on the keyboard are displayed.

Row 2

Position 1 is used to indicate an error, caused, for example, by overflow or an invalid instruction. An error is indicated by a dark rectangle appearing in this position; in the absence of any error it remains blank.

Position 2 carries an alphabetic character N, K or I indicating the mode in which the machine is operating. This is determined by keys on the keyboard.

N indicates normal mode, in which the instructions are fetched from a store location as specified by the IAR.

K indicates keyboard mode, in which the instructions are fetched from the keyboard register.

I indicates input mode, used for entering data from the keyboard directly into store without the use of "Store" instructions.

Position 3 is always blank.

Position 4 carries an alphabetic character A, B or C, indicating the stage reached in handling an instruction.

A indicates that the instruction has been fetched and placed in the instruction register. If it calls for address modification the appropriate modifier register or registers will be displayed on rows 4 through 6. If it calls for indirect addressing these rows will display the addresses of the relevant storage locations and their contents, i.e. the true addresses. In the case of normal addressing these rows remain blank (see below for details of this part of the display).

B indicates that the true address or addresses have been obtained and that rows 3 through 6 now display the relevant operands, before the instruction has been executed.

C indicates that execution of the instruction is complete. Rows 3 through 6 still show the relevant operands.

Position 5 is always blank.

Positions 6 through 13 display the contents of the Instruction Register. If it is an 8-digit instruction, i.e. 3-address, all the positions are used. If it is a 4-digit instruction (single address or register) the instruction appears in positions 6 through 9 and positions 10 through 13 are blank.

Position 14 is always blank.

Rows 3 through 6

These display the contents of storage locations or registers as explained above. When a row displays the contents of a store location, the address of that location (hundreds, tens and units digits) appears in positions 1 through 3. (As in the case of the instruction address register, the hundreds digit will normally be zero).

The contents appear in positions 6 through 14, the positions being allocated exactly as in the keyboard register (Row 1). However, certain zero-suppression arrangements are made, as follows. If the word in store represents numerical data (i.e. not an instruction) indicated by a + or − sign in the sign position, non-significant zeros are suppressed in all positions except the least significant one. That is to say, if the location contains all zeros apart from the sign, a single zero is displayed in position 13. If a word represents an instruction (or instruction pair), indicated by a decimal digit in the sign position, there is no zero suppression.

When a row displays the contents of a

single-length register, the letter R appears in position 2 and the register number in position 3. Positions 8 through 14 display the contents exactly as in the case of numerical data in a storage location. Two examples showing the appearance of the display are given in FIGURE 6.

Displaying the contents of a double-length register requires two rows. The letter R and the register number appear in positions 2 and 3 respectively of the upper row. The upper half of the register is displayed in positions 8 through 13 of the upper row, and the lower half and sign in positions 8 through 14 of the lower row as shown in FIGURE 10a.

Two additional items that have to be displayed during certain instructions are (a) the Link Register and (b) the Control Latch. The Link Register is displayed like any single-length register except that in position 3 the letter L appears in place of a register number. When the Control Latch is displayed the letters C L appears in positions 2 and 3 of the appropriate row and a 1 or 0 indicating whether the latch is set or reset in position 13. A typical display which includes the Link Register and Control Latch is shown in FIGURE 11.

In order to develop the various display formats described above, the control unit 26 (FIGURE 2) includes circuitry arranged to recognize the different classes of instructions. As has already been described with reference to FIGURE 2, one function of the unit 26 is to generate addresses of the various registers so as to make their contents available at appropriate times in the operation of the machine. Referring to FIGURE 3a, this function is performed by an address generator, which is shown to supply addresses to registers 15 and 16. These addresses may be generated in response to a number of different stimuli, but for the purpose of the present description it is only necessary to show the arrangement for causing the display to adopt different formats according to the class of instruction being performed.

The contents of registers 27 and 28, which identify the class of instruction being performed, are applied to a decoder 31, which energises one of three output lines RM, RR and 3A according to whether the instruction is a register-memory, register-register, or three address instruction. These lines are connected to the address generator 30, which responds to the signals on the lines, together with other signals originating in the control unit identifying, for example, the stage reached in an instruction, to enable the recovery of addresses specifying registers and store locations associated with the corresponding instruction.

Characters are displayed in the form shown in FIGURE 3b as a matrix of five by seven elements leaving three elements spacing between characters in a row. A character is read out of memory 9 each time a pulse is received by a memory read out control circuit 32 from divider stage 2 of a divider chain 37. The address of the character read from memory 9 is supplied by the address generator 30 under control of signals on digit column line 33 from divider 3 and the digit row line 34 from divider 6.

The output from memory 9 activates a decoder 35 to energize one of a number of lines, according to which character is to be displayed, to access a corresponding character in a pattern generator 36 stored in 5×7 dot matrix form.

The character is scanned by pulses on the five character column element line 38 from divider stage 2 under control of the coincidently energized appropriate one of seven character row element lines 39 from divider stage 5. The information thus received is combined in a combiner 40 with synchronizing 42 from divider stages 3 and 6 respectively to provide a signal. This modulates the output of RF oscillator 43 to supply modulated RF input signals to the television receiver.

For the arrangement to be suitable for display on different television systems the division ratios of the divider 37 are adjusted as shown in the table in FIGURE 3c. The divider chain is supplied with an input from 6 Mc/s oscillator 44.

Keyboard

The keyboard layout is shown in FIGURE 7. The keys are divided into four groups separated by dividing lines as shown.

At the bottom of groups 1, 3 and 4 are the 'mode' keys that place the machine in the 'Input', 'Keyboard', 'Normal' or 'Recorder' modes. The first three of these modes have already been explained. 'Recorder' mode is used when dumping the store contents into a tape recorder or when reloading. The other keys in groups 1, 3 and 4 are used when the machine is in the relevant mode.

Group 2 contains the numerical, decimal point, sign and 'Clear Keyboard Register' keys. These are used in 'Input', 'Normal', and 'Keyboard' modes.

Group 1

The keys in group 1 are used when one wishes to display or replace the contents of any store location without using the normal machine instructions. They are particularly useful for entering a program into the store.

To do this, the operator first touches the 'Input Mode' key, clears the keyboard register, and then keys-in the address at which the first instruction is to be stored. This is held in the keyboard register and appears at the top right-hand corner of the display. He then touches 'Load Address Register' whereupon

the digits are copied into an address register and displayed at the left-hand end of line 4. The existing contents of the selected location (left over from a previous program) are displayed at the right-hand end of the same line.

The operator then clears the keyboard register and keys-in the first instruction word. This may be a single 3-address instruction or a pair of single-address or register instructions. Touching the 'Load Store' key, now causes the instruction word to replace the previous contents of the selected location.

The next step is to touch the 'Increment Address' key. This adds 1 to the contents of the address register (displayed at the left-hand end of display line 4), and causes the next word in the store to be displayed at the right-hand end. The keyboard register is cleared and the second instruction word keyed-in and transferred to the store in the same manner. The process is continued until all the instructions and initial data have been entered.

The above method of loading a program is the most straightforward and therefore the most useful in the initial stages of teaching. However, it is not the only method, e.g. a load routine could be used, containing a single-address 'input' instruction with address modification.

Group 3

The keys in group 3 are used in the 'Normal' mode when instructions are fetched from the store, and in the 'Keyboard' mode when they are fetched from the keyboard register. Having entered a program as described above, the machine is brought into the correct initial state in the following way. It is put into 'Keyboard' mode, the keyboard register cleared and a single-address 'unconditional branch' instruction (code 27) keyed in. The address portion of this instruction (digits c and d) is the address of the first instruction in the program; for example, if the program starts at address 00, the instruction to be keyed in is 2700. Touching the 'Run' or 'C' key causes 00 to be entered into the instruction address register. The machine is then put into 'Normal' mode and the program is ready to run.

On touching the 'Run' key, instructions are obeyed in succession until one is encountered which requires some action on the part of the operator. Such instructions are: 'Input', which calls for new data to be entered into the keyboard register, and 'Output', in which the result must be noted.

The machine will also stop if an error is detected. If 'Run' is touched when the machine is in 'Keyboard' mode the machine fetches its instruction from the keyboard register, executes it and then stops.

When the 'Stop' key is touched, the machine completes the instruction on which it is currently engaged, and then stops and displays the result. Normally this key would only be used if owing to some error the machine is unable to branch out of a program loop.

The A, B and C keys are used when the operation of the machine is to be demonstrated in detail. The three letters represent stages in the processing of an instruction. At stage A, the instruction has been fetched and entered into the Instruction Register (line 2 of the display). At stage B the true addresses of the operands have been determined, and at stage C the instruction has been executed and the Instruction Address Register incremented.

The information displayed at each of these stages is shown earlier in this specification. Touching any of these keys causes an instruction to be processed up to the relevant stage. Thus, to follow the operation of the machine in the greatest detail, the keys are touched in succession, A, B, C, A, B, C . . . etc. Often, however, this degree of detail will be unnecessary and the operator will touch only the B and C keys, or if he wishes to display conditions only at the completion of each instruction, he will touch only the C key. Having touched the A or B keys the operator must complete the instruction by touching the C key; otherwise, further operation of the A or B keys will have no effect.

Group 4

The keys in group 4 control the dumping and reloading of the store when the machine is used with a tape recorder. To dump the contents of the store the machine is first put into 'Recorder' mode, the tape recorder started and the 'Dump' key touched. When dumping is complete the tape is rewound, the 'Check' key touched and the recorder started again. This causes the recorded information to be read back into the computer where it is compared digit by digit with the store contents to check that it has been recorded correctly. If not, the computer stops and displays an error condition. To reload the store the 'Reload' key is touched and the recorder started.

WHAT WE CLAIM IS:—

1. An electronic digital computer comprising a processing unit adapted to operate on data in the form of digital operands in accordance with instructions supplied to the computer and a display control circuit connected to said processing unit and adapted in response to signals indicating that different classes of instructions are being performed by said processing unit to produce display control signals defining different display formats, said display control circuit also including an oscillator modulator unit adapted to impress said display control signals on a radio fre-

quency carrier wave for application as a modulated input to a television receiver.

2. An electronic digital computer as claimed in claim 1, in which the display control circuit includes means responsive to the occurrence of a multiple address macroinstruction to cause the display to present selected stages in the execution of the macroinstruction and to suppress the display of information pertaining to the basic instructions constituting the macroinstruction which would otherwise be displayed.

3. An electronic digital computer substantially as hereinbefore described with reference to the accompanying drawings.

Agent for the Applicants.
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Chartered Patent Agent,

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Published by the Patent Office, 25, Southampton Buildings, London, W.C.2, from which copies may be obtained.

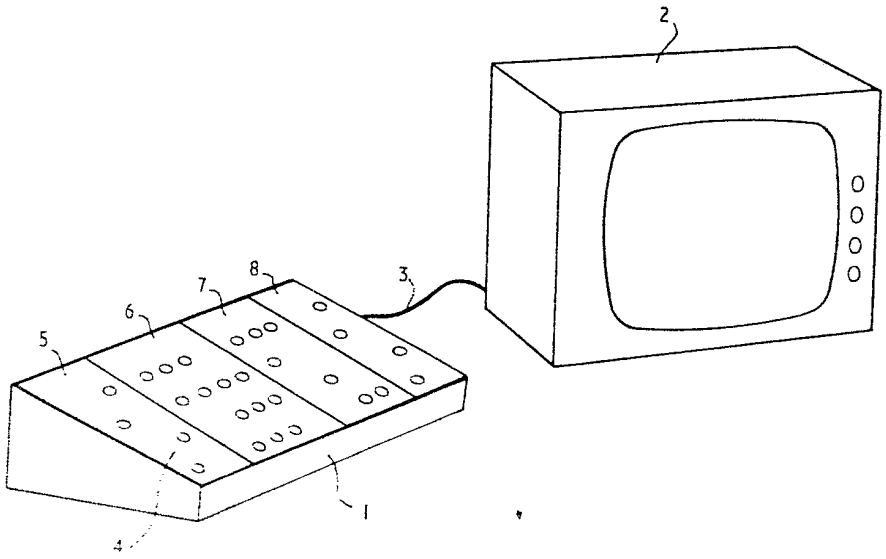

FIG 1

1143327 COMPLETE SPECIFICATION

10 SHEETS *This drawing is a reproduction of the Original on a reduced scale*

Sheets 1 & 2

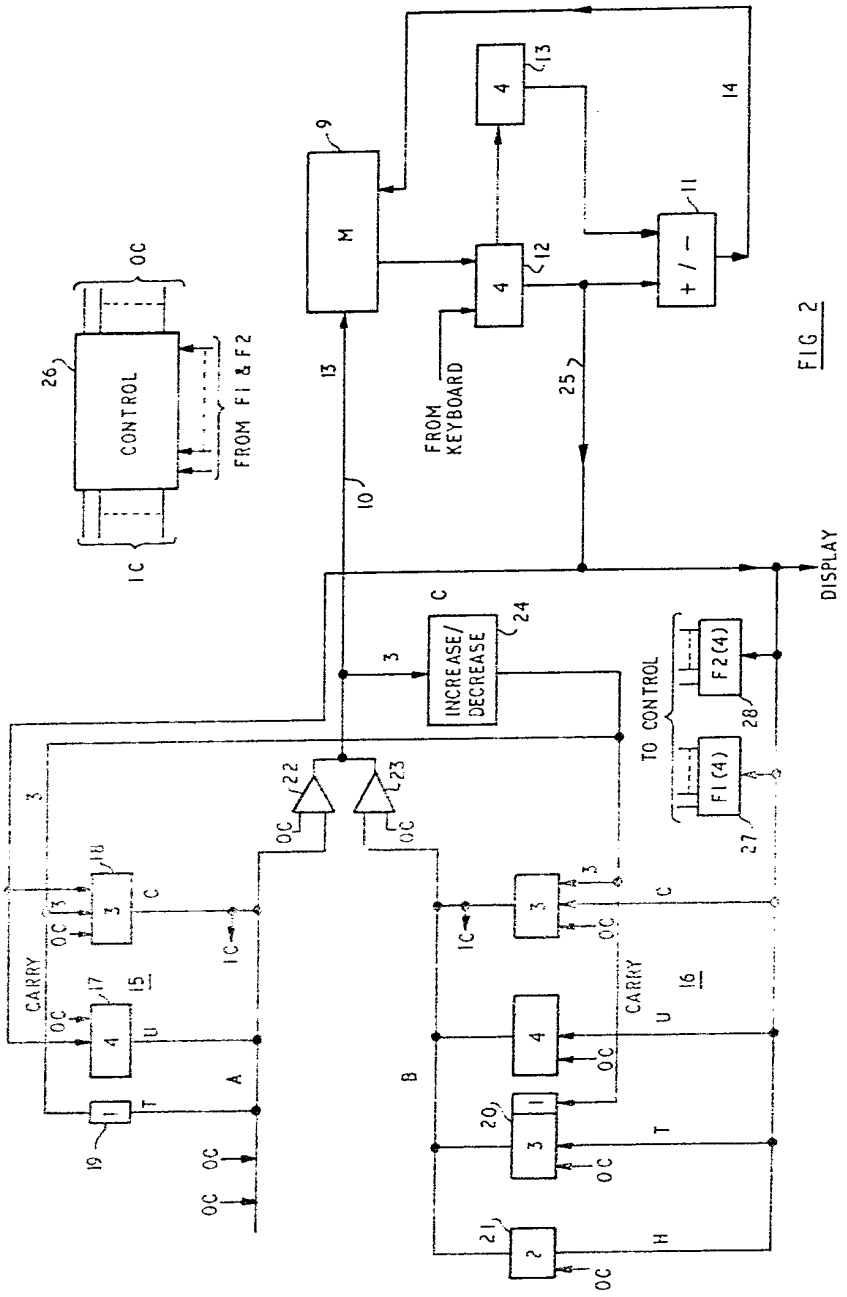

FIG 2

1143327 COMPLETE SPECIFICATION
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Sheets 1 & 2

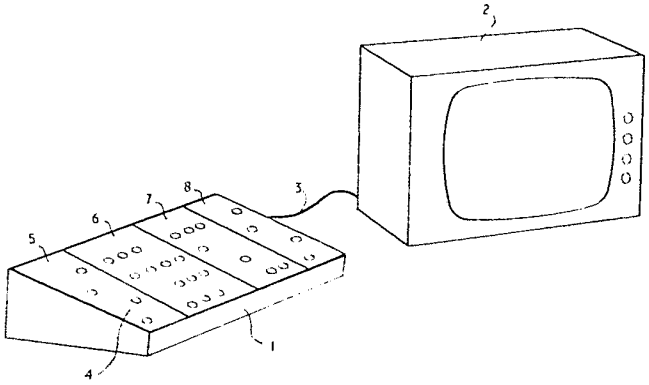

FIG 1

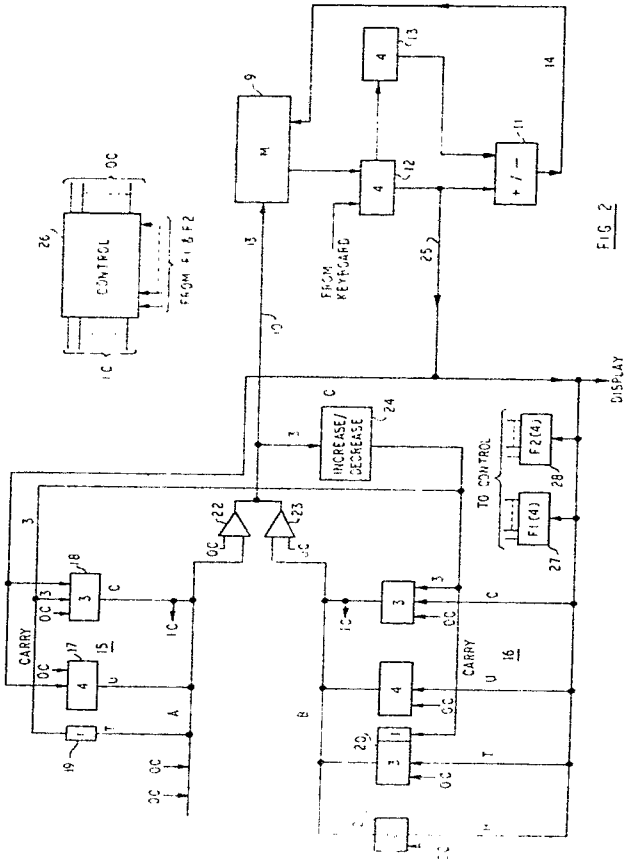

FIG 2

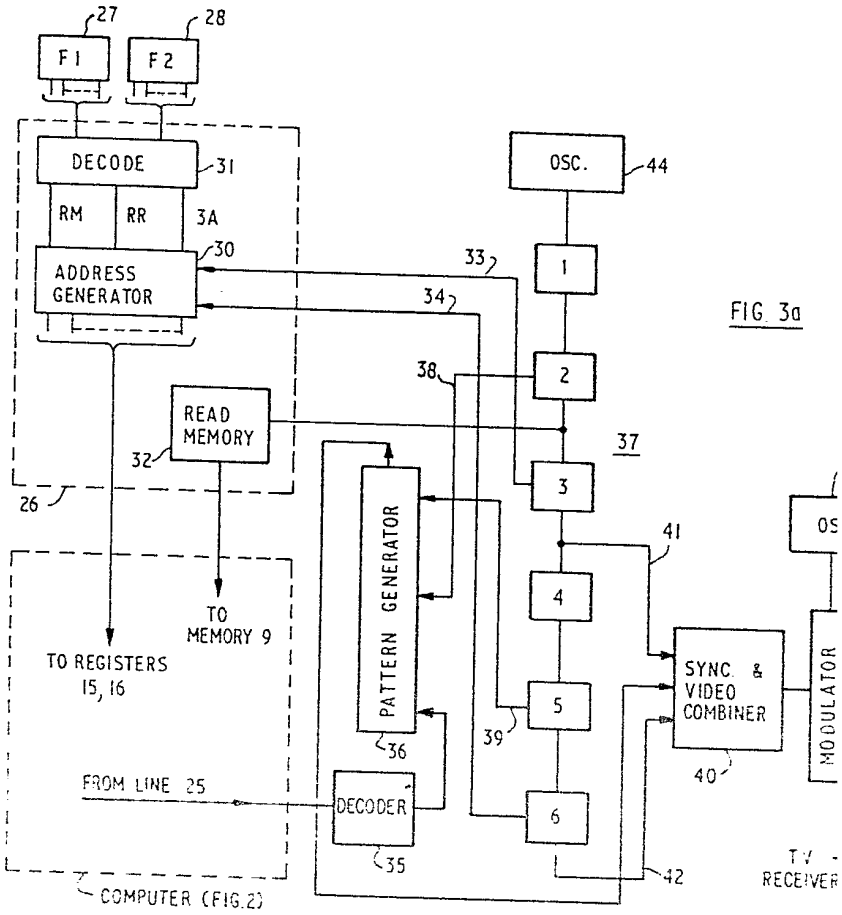

FIG. 3a

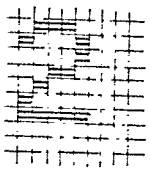

FIG. 3b

DIVIDER CHAIN						LINE/ FRAME
1	2	3	4	5	6	
6	8	12	2	13	8	405/50
4	8	12	3	13	8	625/50
4	8	12	3	11	8	525/60
3	8	12	4	13	8	819/50

FIG. 3c

1143327 COMPLETE SPECIFICATION

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Sheets 3 & 4

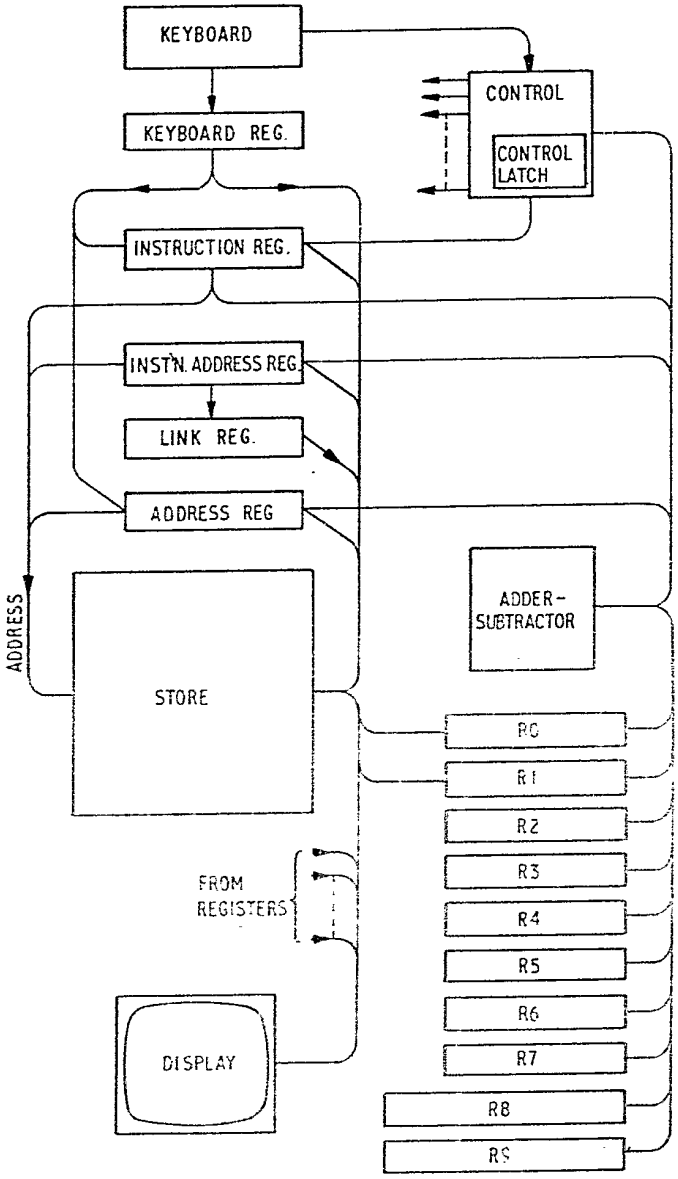

FIG. 4

1143327 COMPLETE SPECIFICATION
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Sheets 3 & 4

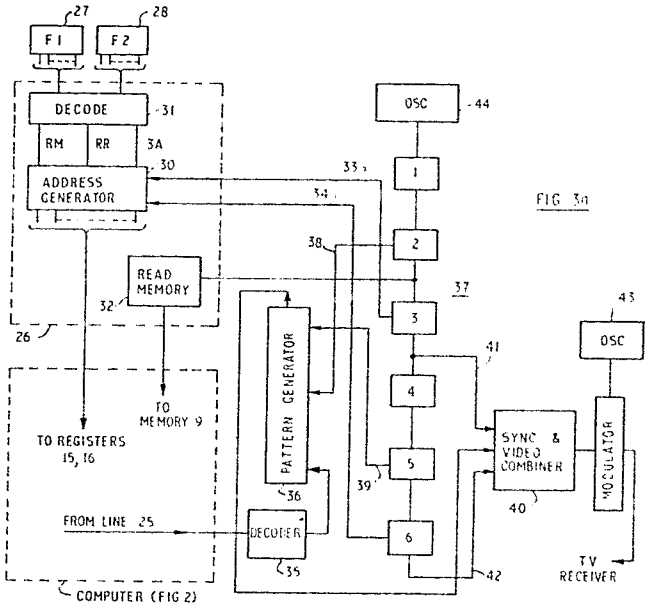


FIG 3a

FIG 3b

DIVIDER CHAIN						LINE/ FRAME
1	2	3	4	5	6	
6	8	12	2	13	8	405/50
4	8	12	3	13	8	625/50
4	8	12	3	11	8	525/60
3	8	12	4	13	8	819/50

FIG 3c

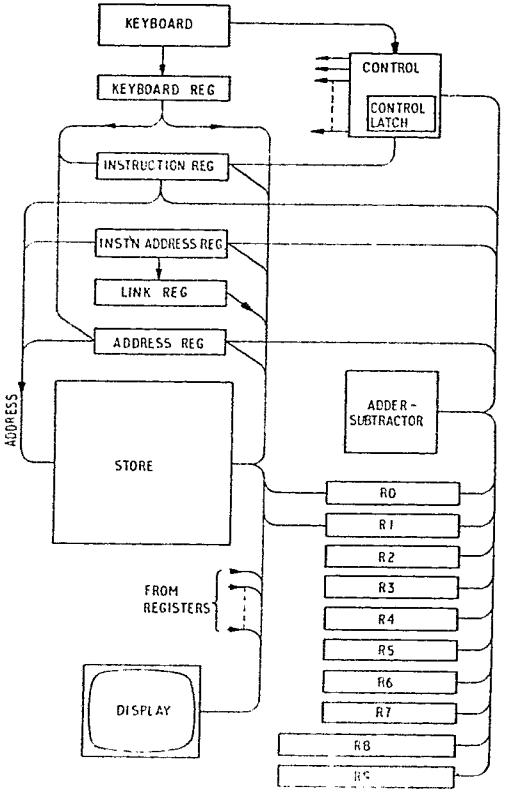
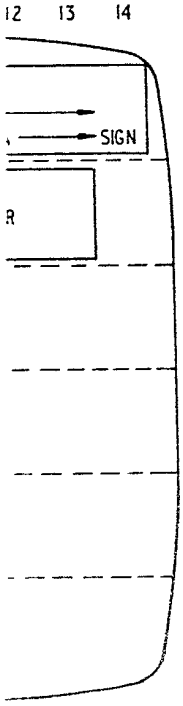
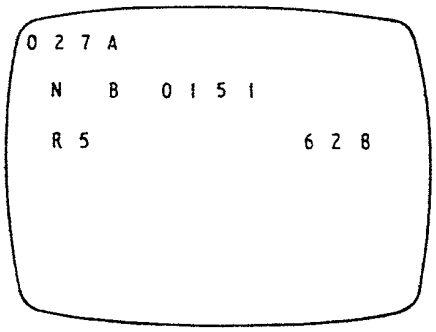


FIG 4

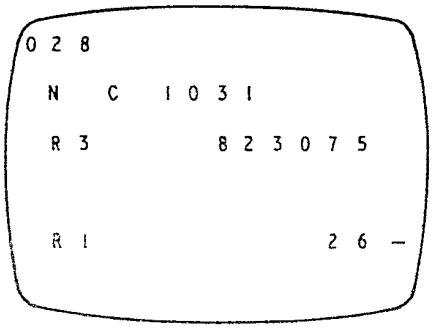
1143327 COMPLETE SPECIFICATION
10 SHEETS *This drawing is a reproduction of the Original on a reduced scale*
Sheets 5 & 6



a



b



c

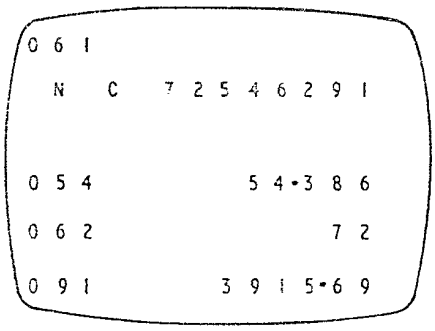


FIG 6

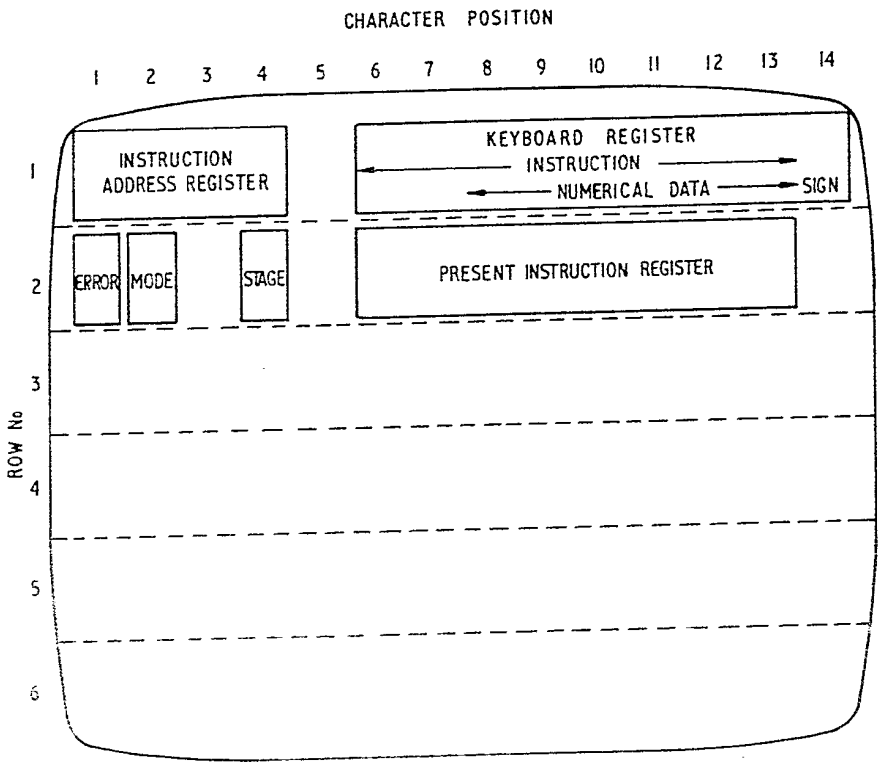

CHARACTER POSITION
1 2 3 4 5 6 7 8 9 10 11 12 13 14
ROW No
1
2
3
4
5
6
INSTRUCTION ADDRESS REGISTER
KEYBOARD REGISTER
INSTRUCTION
NUMERICAL DATA
SIGN
ERROR
MODE
STAGE
PRESENT INSTRUCTION REGISTER

FIG. 5

1143327 COMPLETE SPECIFICATION
10 SHEETS *This drawing is a reproduction of the Original on a reduced scale*
Sheets 5 & 6

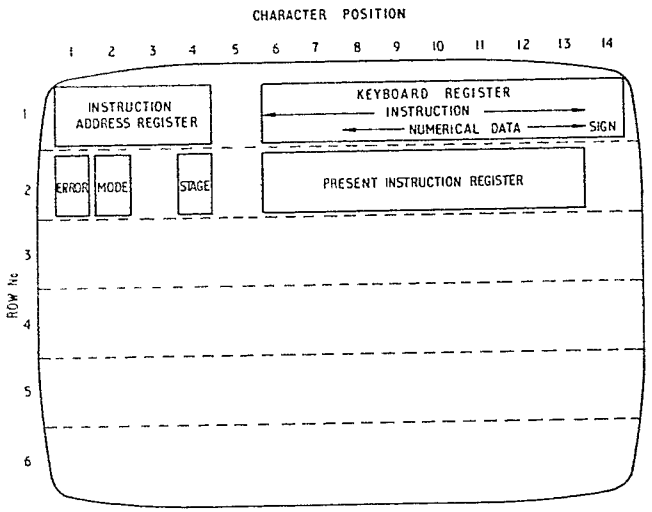


FIG 5

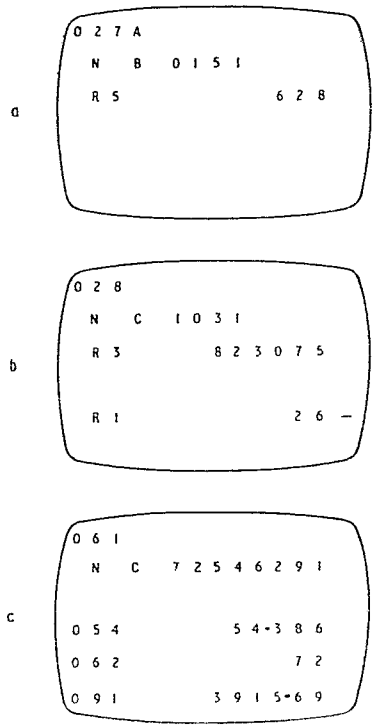
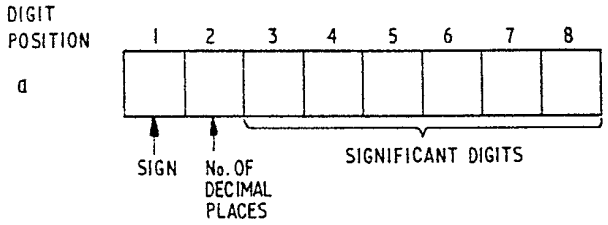


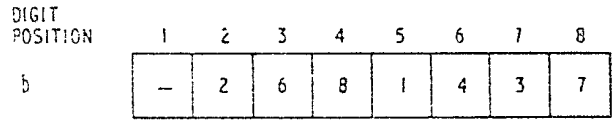
FIG 6

1143327 COMPLETE SPECIFICATION
10 SHEETS *This drawing is a reproduction of the Original on a reduced scale*
Sheets 7 & 8



EXAMPLE

IN STORE



AS DISPLAYED:

c 6 8 1 4 · 3 7 –

FIG 8

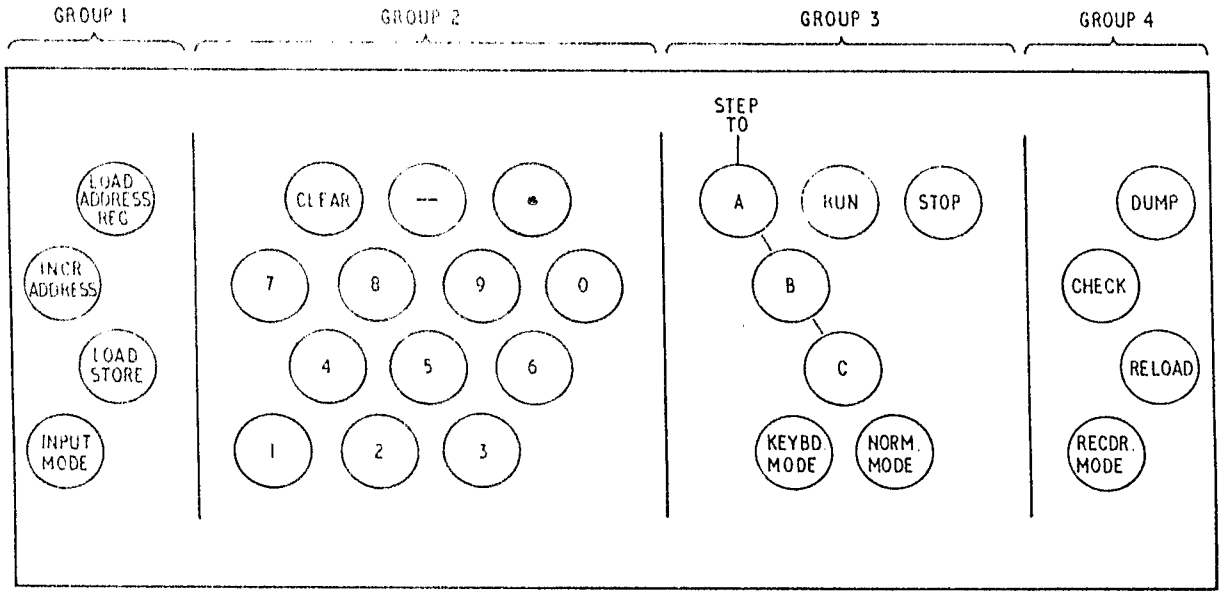


FIG 7

EXAMPLE

IN STORE

DIGIT POSITION

a

b

DIGIT POSITION

c

AS DISPLAYED

1143327 COMPLETE SPECIFICATION
10 SHEETS *This drawing is a reproduction of the Original on a reduced scale*
Sheets 7 & 8

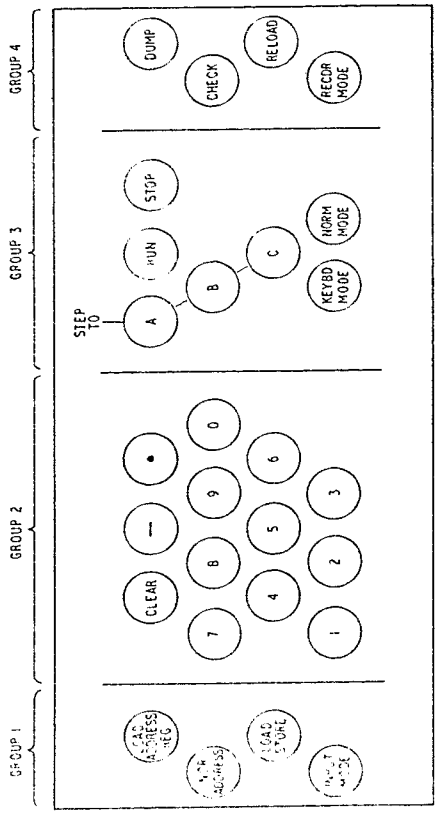
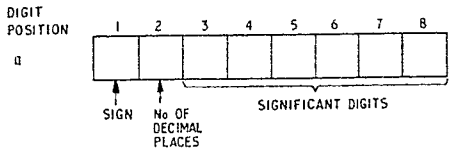
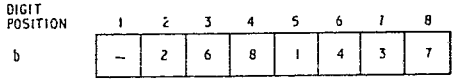


FIG 7



EXAMPLE

IN STORE

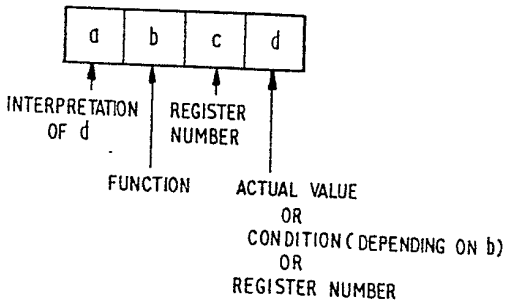


AS DISPLAYED

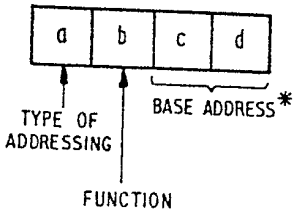
c 6 8 1 4·3 7 —

FIG 8

REGISTER INSTRUCTIONS:



SINGLE ADDRESS INSTRUCTIONS:



THREE ADDRESS INSTRUCTIONS:

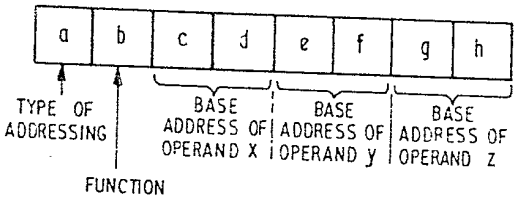


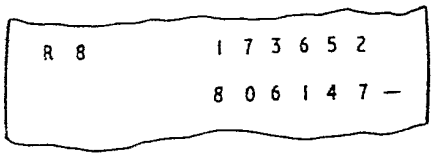
FIG. 9

1143327 COMPLETE SPECIFICATION

10 SHEETS *This drawing is a reproduction of the Original on a reduced scale*

Sheets 9 & 10

a



b

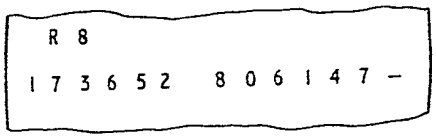
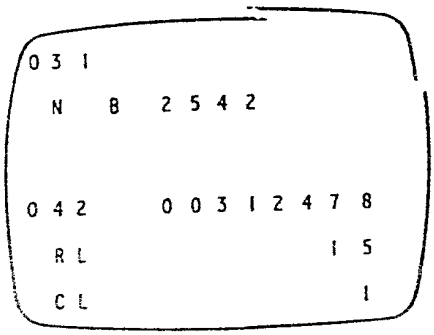


FIG. 10



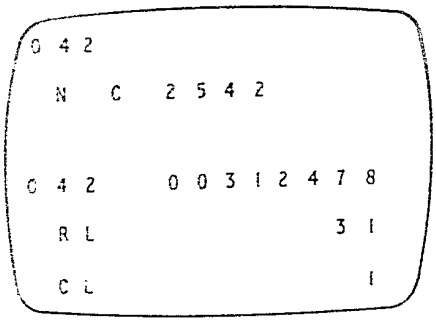
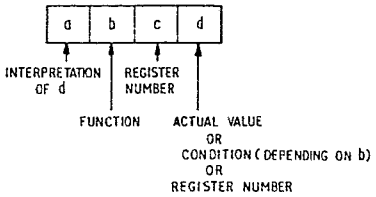


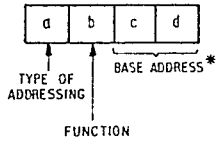
FIG 11

1143327 COMPLETE SPECIFICATION
10 SHEETS *This drawing is a reproduction of the Original on a reduced scale*
Sheets 9 & 10

REGISTER INSTRUCTIONS



SINGLE ADDRESS INSTRUCTIONS



THREE ADDRESS INSTRUCTIONS.

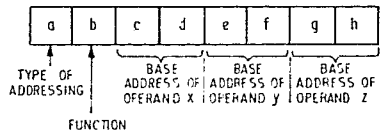


FIG 9

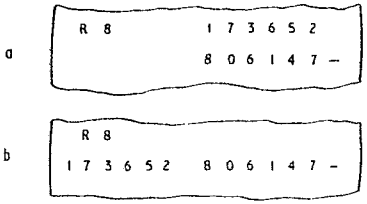


FIG 10

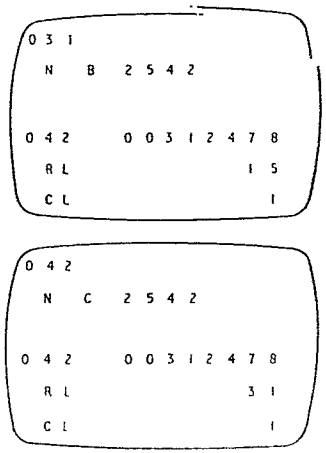


FIG 11