

PARALLEL PROCESSING SYSTEM (PPS) DATA SHEET

GENERAL PURPOSE INPUT/OUTPUT (GPI/O)

DESCRIPTION

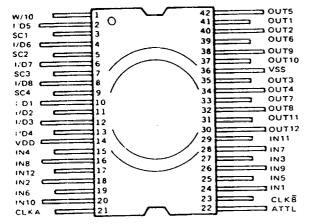
The General Purpose Input/Output device P/N 10696, provides 12 discrete inputs and 12 discrete static outputs. This device is used for direct data exchange or status and control function exchange with an external peripheral device. The GPI/O lines directly interface with TTL circuitry. Direct addressing for up to sixteen of these circuits is possible by the use of four chip address straps that can be terminated, by the user, to create each chip address. The I/O is accessed with an I/O enable signal from the CPU and a simultaneous 8-bit instruction from ROM. Four bits of the instruction are used to address the particular I/O chip; the other four bits define the I/O operation.

The 4-bit operation code is interpreted by the GPI/O to either copy the contents of the accumulator into one of the three 4-bit parallel output registers (A, B or C) or transfer data from one of the 4-bit parallel input receivers (A, B or C) into the accumulator of the CPU. The input lines are static and are sampled at instruction execution time. The output drivers are latched and data remains in the output registers until altered. Bits 1 through 4 of the instruction word are commands to the I/O while bits 5 through 8 are used to address one of 16 possible I/O chips. The four I/O chip select strap inputs terminated by the user, create the addresses for each I/O circuit.

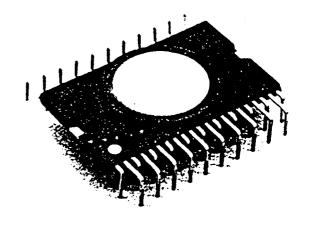
Data is transferred through the GPI/O from input groups A, B, or C to I/D 1 through 4 and from I/D 5 through 8 to output groups A, B or C, to most significant to most significant and least significant to least significant. A TTL level A clock (ATTL) is provided for external system use.

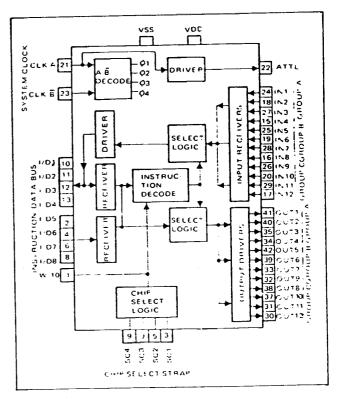
FEATURES

- 12 Discrete Inputs
- 12 Discrete Outputs
- Direct TTL Compatibility
- Individual Strappable Addresses for Up to 16 GPI/Os
- Latched Output Drivers
- PPS-4 and PPS-8 Direct Compatibility



General Purpose Input/Output Pin Configuration





GPI/O Block Diagram

Specifications subject to change without notice Revision 1, March 1976

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OPERATING CHARACTERISTICS

Supply Voltage:

VDD = .17 Volts $\pm 5\%$ (Logic "1" = most negative voltage V_{IL} and V_{OL} .)

VSS = 0 Volts (Gnd.)

(Logic "0" = most positive voltage V_{IH} and V_{OH} .)

System Operating Frequencies:

199 kHz or 256 kHz.

Device Power Consumption:

330 mw

Input Capacitance:

<5 pf

Input Leakage:

<10 ua

Operating Temperature (TA):

0°C to 70°C. (TA = 25°C unless otherwise specified.)

Storage Temperature:

-55°C to 120°C.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage

VDD-VSS = 27 volts maximum.

Input Voltage with respect to VSS

-27 votts maximum.

CHIP SELECT STRAPS				C B A	COMMAND
CHIP NO.	ł	HEX	READ		
0	10000		1010	x	, Read Group A
1	0001	9	1001] - × -	Read Group 8
2	0010	3	0011	×	Read Group C
3	0011	0	0000.	[If two or three groups are
4	0100	1	0001	× × -	selected the accumulator w
5	0101	2	0010	x - x	copy the logical "Off," wall of the selected groups
6	0110	8	1000	-××	St the selected groups
7	0111	1	Ì	1 1	
8	1000	1	——SET	1 1	
9	1001	1] †	i 1	
10	1010	E	1110	×	Set Group A
11	1011	0	1101	- × -	Set Group 8
12	1100	7	0111	× .	Set Group C
13	1101	4	0100	XXX	If two or three groups are
14	11110	5	0101	x x -	selected the accumulator
15	11111	6	0110	x - x	contents will be copied to each group selected
		c	1100	-××	each group selected
	1 1	•	•	•	

GPI/O Instruction Format

	Maximum positive voltage on			LIMITS (VSS = 0V)		LIMITS (VSS = +5V)			TEST		
	Eu.	INCTION	SYMBOL	MIN TYP N	MAX	MIN	TYP	MAX	UNIT	CONDITIONS	
	Supply Curre		100		8.5	18.5		8.5	18.5	mA	VDD = 17.85V VSS = 0V F = 256 kHz T _A = 25°C
_			Bus	l			<u> </u>				VDD = -17V ±5%
	Input and Ou	1/D5.8	VIH	-1.5 -6.5		+0.3 -17.85	+3.5 -1.5		+5.3 -12.85	v v	VSS = 0V
		William	V _{OH}	-1.0 -7.5		+0.3 -17.85	+4.0 -2.5		+5.3 -12.85	v	
	CLKA CLKB		V _I H V _I L	-0.5 -10.0		+0.3 -17.85	+4.5 -5.0		+5.3 -12.85	V	OR
_	Input and Output Characteristics — External Interface and Straps										
H	SC _{1.4}		VIH VIL	-1.5 -13.0		+0.3 -17.85	+3.5 -8.0		+5.3 -12.85	v	5
	IN ₁₋₁₂		VIH VIL	-1.5 -4.2		+0.3 -17.85	+3.5 +0.8		+5.3 -12.85	v	
<u> </u>	OUT ₁₋₁₂ A(TTL)		VOH VOL	1	NOTE loating (≥			NOTE loating (Ω	VDD = -12V ±5% VSS = +5V ±5%

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