Data Sheet | February 25, 2008 | FN6435.0

High Input Voltage Charger With Power Path Management

The ISL9301 is a fully integrated high input voltage single-cell Li-ion battery charger with power path management function. This charger performs the CC/CV charge function required by Li-ion batteries. The charger accepts an input voltage up to 28V but is disabled when the input voltage exceeds 10.5V OVP threshold. The 28V rating eliminates the overvoltage protection circuit required in a low-voltage charger. The charge current and the end-of-charge (EOC) current are programmable with external resistors. When the battery voltage is lower than 2.8V, the charger preconditions the battery with 16% of the programmed charge current. When the charge current reduces to the programmable EOC current level during the CV charge phase, the EOC indicator ($\overline{CHG}$) will toggle to logic LOW to indicate the end-of-charge condition. The charger will continue to charge until the user programmed timeout interval has elapsed, then the charger is terminated.

The ISL9301 uses separate power paths to supply the system load and charge the battery. This feature allows the system to immediately operate with a completely discharged battery. This feature also allows the charge to terminate when the battery is full while continuing to supply the system with the input source, thus minimizing unnecessary charge/discharge cycles and improving the battery life.

Two indication pins ($\overline{PPR}$ and $\overline{CHG}$) allow simple interface to a microprocessor or LEDs.

Ordering Information

PART NUMBER (Note)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL9301IRZ	9301	-40 to +85	10 Ld 3X3 DFN	L10.3X3C
ISL9301IRZ-T	9301	-40 to +85	10 Ld 3X3 DFN	L10.3X3C

* Please refer to TB347 for details on reel specifications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate PLUS ANNEAL - e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

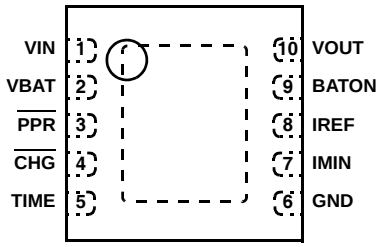
- Complete Charger for Single-Cell Li-ion/Polymer Batteries
- Power Path Management Optimize Charge and System Currents
- Intelligent Timeout Interval Based on Actual Charge Current
- Integrated Disconnect Switch to Disconnect the Battery
- 1% Charger Output Voltage Accuracy
- Programmable Charge Current
- Programmable End-of-Charge Current
- Charge Current Thermal Foldback for Thermal Protection
- Trickle Charge for Fully Discharged Batteries
- 28V Maximum Voltage at VIN pin
- Power Presence and Charge Indications
- Ambient Temperature Range: -40°C to +85°C
- 10 Ld 3x3 DFN Package
- Pb-Free (RoHS Compliant)

Applications

- Mobile Phones
- Blue-Tooth Devices
- PDAs
- MP3 Players
- Stand-Alone Chargers
- Other Handheld Devices

Pinout

ISL9301
(10 LD DFN)
TOP VIEW



Absolute Maximum Ratings (Reference to GND)

VIN . . . . . -0.3V to 30V
All other pins . . . . . -0.3V to 7V

Recommended Operating Conditions

Ambient Temperature Range . . . . . -40°C to +85°C
Maximum Supply Voltage (VIN Pin) 28V
Operating Supply Voltage (VIN Pin) . . . . . 4.3V to 10V
Programmed Charge Current . . . . . 50mA to 450mA
Output Current . . . . . 0mA to 800mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
DFN Package (Notes 1, 2)	40	2.5

Maximum Junction Temperature (Plastic Package) . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-free reflow profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

1. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
2. For theta θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Typical values are tested at VIN = 5V and the ambient temperature at +25°C. All maximum and minimum values are established under the recommended operating supply voltage range and ambient temperature range, unless otherwise noted.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
POWER-ON RESET						
Rising POR Threshold	V_{POR}	VBAT = 3.0V, use $\overline{PPR}$ to indicate the comparator output.	3.3	3.9	4.3	V
Falling POR Threshold	V_{POR}		3.1	3.6	4.15	V
VOUT-BAT OFFSET VOLTAGE						
Rising Edge	V_{OS}	V_{BAT} = 4.0V, use $\overline{CHG}$ pin to indicate the comparator output (Note 3)	-	110	250	mV
Falling Edge	V_{OS}		10	100	-	mV
VIN OVERVOLTAGE PROTECTION						
Over Voltage Protection Threshold	V_{OVP}	Use $\overline{PPR}$ to indicate the comparator output	10	10.5	13	V
OVP Threshold Hysteresis			200	400	500	mV
STANDBY CURRENT						
BAT Pin Sink Current	$I_{STANDBY}$	Charger disabled or the input is floating	-	-	1.0	µA
BAT Pin Supply Current	I_{VBAT}	No supply at VIN, BATON = HI	-	10	-	µA
VIN Pin Supply Current	I_{VIN}	Charger enabled	-	1	-	mA
VOLTAGE REGULATION						
Output Voltage	V_{OUT}	System current + charge current = 15mA	4.40	4.50	4.62	V
Output PPM Threshold Voltage	V_{DPPM}		4.22	4.35	4.45	V
Charger Output Voltage	V_{BAT}	Charge current = 10mA	4.158	4.20	4.242	V
IREF PIN Voltage	V_{IREF}	VBAT = 3.8V	1.165	1.20	1.245	V
MOSFET ON-RESISTANCE						
Regulator MOSFET $r_{DS(ON)}$	$r_{DS(ON)}$	V_{OUT} = 4.4V, Total current = 0.3A	-	0.8	1.2	Ω
Charger MOSFET $r_{DS(ON)}$	$r_{DS(ON)}$	V_{BAT} = 3.8V, charge current = 0.2A	-	0.1	0.15	Ω
RECHARGE THRESHOLD						
Recharge Voltage Threshold	V_{RECHG}	Relative to V_{BAT}	-200	-150	-100	mV
CURRENT REGULATION (Note 4)						
Input Current Limit	I_{LIM}	V_{OUT} = 4.5V	600	800	1200	mA
Constant Charge Current	I_{CHG}	R_{IREF} = 26.7kΩ, V_{BAT} = 2.8V - 4.0V	130	145	160	mA

Electrical Specifications

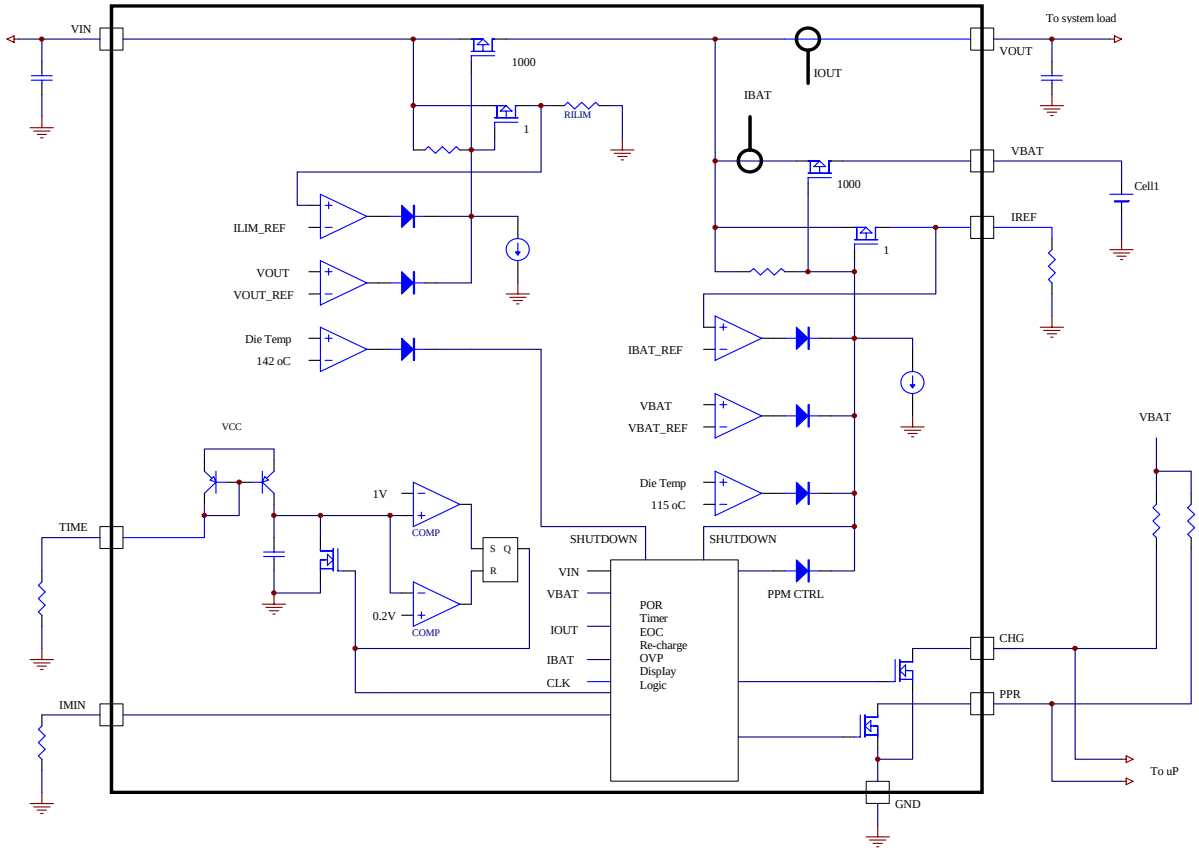
Typical values are tested at VIN = 5V and the ambient temperature at +25°C. All maximum and minimum values are established under the recommended operating supply voltage range and ambient temperature range, unless otherwise noted. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Trickle Charge Current	I_{TRK}	R_{IREF} = 26.7kΩ, V_{BAT} = 2.4V	17	23	30	mA
End-of-Charge Current	I_{MIN}	R_{IMIN} = 137kΩ	18	23	28	mA
PRECONDITIONING CHARGE THRESHOLD						
Preconditioning Charge Threshold Voltage	V_{MIN}		2.7	2.8	3.0	V
Preconditioning Voltage Hysteresis	V_{MINHYS}		40	100	150	mV
INTERNAL TEMPERATURE MONITORING (Note 5)						
Charger Current Thermal Foldback Threshold	T_{FOLD}		-	115	-	°C
OVER-TEMPERATURE PROTECTION (Note 5)						
Shutdown Rising Threshold	T_R		-	142	-	°C
Shutdown Falling Threshold	T_F		-	110	-	°C
OSCILLATOR PERIOD						
Oscillator Period	t_{OSC}	R_{TIME} = 1MΩ	60	75	90	µs
LOGIC INPUT AND OUTPUTS						
BATON Pin Logic Input High		V_{BAT} < 4.5V	1.1	-	-	V
BATON Pin Logic Input Low		V_{BAT} > 2V	-	-	0.4	V
BAT Pin Internal Pull-Down Resistance			800	1000	1200	kΩ
$\overline{PPR}$, $\overline{CHG}$						
Driving Capability when LOW		Pin Voltage = 1V	10	-	-	mA
Leakage Current When HIGH		Pin Voltage = 6.5V	-	-	1	µA

NOTES:

3. The 4.0V V_{BAT} is selected so that the CHG output can be used as the indication for the offset comparator output indication. If the V_{BAT} is lower than the POR threshold, no output pin can be used for indication.
4. The input current charge current can be affected by the thermal foldback function if the IC under the test setup cannot dissipate the heat.
5. Limits established by characterization and are not production tested.

Block Diagram



Pin Descriptions

VIN - Power input. The absolute maximum input voltage is 28V. A 10µF or larger value capacitor is recommended to be placed very close to the input pin for decoupling purposes. Additional capacitance may be required to provide a stable input voltage.

VBAT - Charger output pin. Connect this pin to the battery. A 1µF or larger X5R ceramic capacitor is recommended for decoupling and stability purposes. When the BATON pin is pulled to logic LOW or left floating, the VBAT pin is disconnected from the IC.

TIME - Timing resistor pin. The TIME pin determines the oscillation period by connecting a timing resistor between this pin and GND. The oscillator also provides a time reference for the charger calculated in Equation 1.

$$t_{OSC} = 75 \times R_{TIME} \quad (\mu s) \quad \text{(EQ. 1)}$$

Where R_{TIME} is in MΩ. The nominal timeout interval is given by Equation 2:

$$t_{TIMEOUT} = \frac{2^{28} \times t_{OSC}}{3600} \quad (Hour) \quad \text{(EQ. 2)}$$

Where t_{OSC} is in seconds. For an 1MΩ R_{TIME}, the nominal timeout interval is approximately 5.6 hours.

$\overline{PPR}$ - Open-drain power presence indication. The open-drain MOSFET turns on when the input voltage is above the POR threshold but below the OVP threshold and off otherwise. This pin is capable to sink 10mA (minimum) current to drive a LED. The maximum voltage rating for this pin is 7V.

$\overline{CHG}$ - Open-drain charge indication pin. This pin outputs a logic LOW when a charge cycle starts and turns to HIGH when the end-of-charge (EOC) condition is qualified. This pin is capable to sink 10mA min. current to drive an LED. When the charger is disabled, the $\overline{CHG}$ outputs high impedance.

IMIN - End-of-charge (EOC) current program pin. Connect a resistor between this pin and the GND pin to set the EOC current. The EOC current IMIN can be programmed by Equation 3:

$$I_{MIN} = \frac{3151}{R_{IMIN}} \quad (mA) \quad \text{(EQ. 3)}$$

Where R_{IMIN} is in kΩ. The programmable range covers 5% (or 10mA, whichever is higher) to 50% of IREF when programmed to less than 5% or 10mA.

IREF - Charge-current program and monitoring pin. Connect a resistor between this pin and the GND pin to set the charge current limit determined by Equation 4:

$$I_{REF} = \frac{3886}{R_{IREF}} \quad (mA) \qquad \text{(EQ. 4)}$$

Where R_{IREF} is in kΩ. The IREF pin voltage also monitors the actual charge current during the entire charge cycle, including the trickle, constant-current, and constant-voltage phases. When disabled, V_{IREF} = 0V.

BATON - Battery disconnect pin. The BATON pin is a logic input pin to allow the disconnection of the battery from the system to eliminate the unwanted drainage current from the battery. There is an internal 1MΩ pull-down resistor at this pin. Drive to HIGH to connect the battery to the system. When this pin is driven to LOW or left floating, the battery is disconnected from the system.

VOUT - Output connection to the system. This pin provides a 4.5V regulated voltage for the system when a valid input power is present. If no valid input is present, and BATON is driven HI, the VOUT pin is connected to VBAT through an internal MOSFET. If no valid input is present and BATON is LOW, the voltage at VOUT pin is zero. A 4.7µF or larger X5R ceramic capacitor is recommended for decoupling and stability purposes.

EPAD - Exposed pad. Connect as much copper as possible to this pad either on the component layer or other layers through thermal vias to enhance the thermal performance.

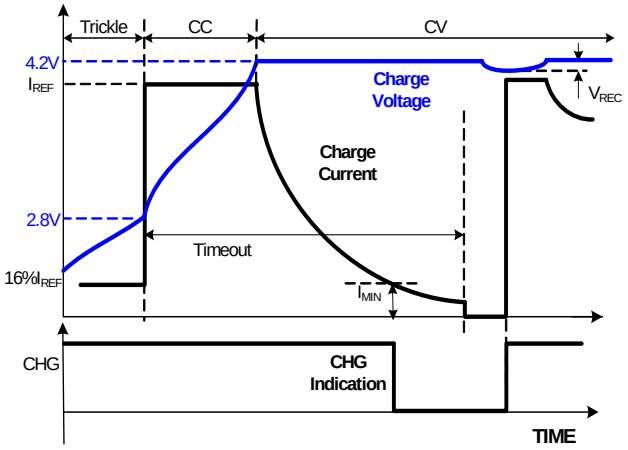
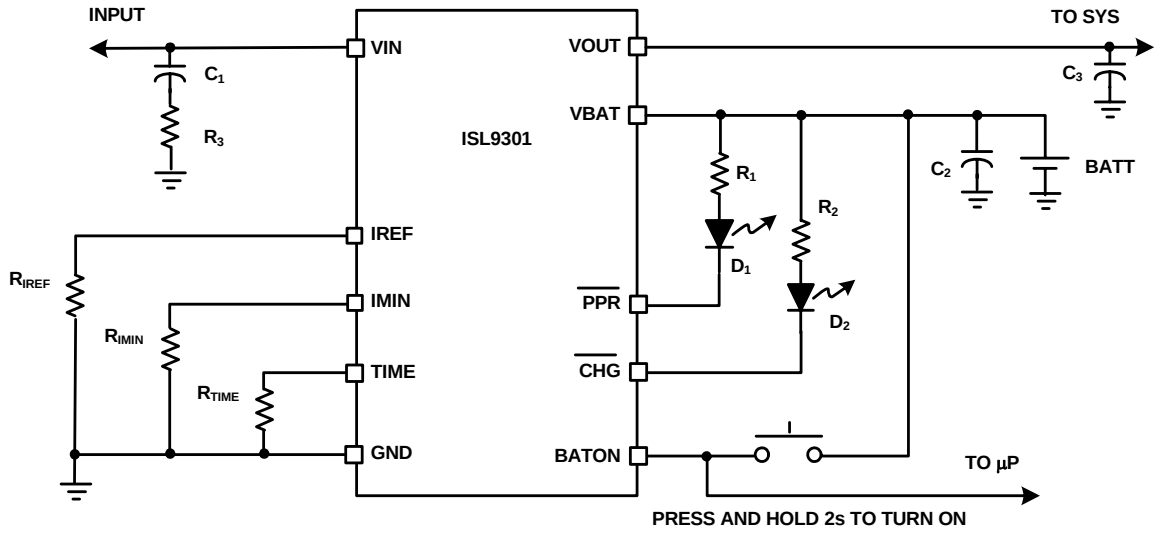


FIGURE 1. TYPICAL CHARGING CYCLE

Typical Application Circuit



PART	DESCRIPTION
C_1	10µF X5R ceramic cap
C_2	1µF X5R ceramic cap
C3	4.7µF X5R ceramic cap
R_3	1Ω, 5% resistor
R_{IREF}	26.7kΩ, 1%, for 150mA charge current
R_{IMIN}	137kΩ, 1%, for 23mA EOC current
R_{TIME}	1MΩ, 1% resistor for 75µs clock period
R_1, R_2	470Ω, 5% resistor
D_1, D_2	LEDs for indication

Theory of Operation

When a valid input voltage is applied at VIN, the ISL9301 first regulates VOUT at 4.5V for system power need. In the mean time, if the battery is attached, the ISL9301 also charges the battery while supplying current to the system. When the system exceeds the maximum available current, either limited by the IC or by the input power supply, the charger FET is operated in a reverse mode, i.e. it discharges current to the system instead of charging.

The charger function is similar to other Li-ion battery chargers, i.e. it charges the battery at a constant current (CC) or a constant voltage (CV) depending on the battery terminal voltage. The constant current I_{REF} is set with the external resistor R_{IREF}, as shown in the "Typical Application Circuit" on page 6. The constant voltage is fixed at 4.2V. If the battery voltage is below a typical 2.8V trickle charge threshold, the ISL9301 charges the battery with a trickle current (~16% of the programmed constant current) until the battery voltage rises above the trickle charge threshold. When the battery voltage reaches the final voltage of 4.2V, the charger enters the CV mode and regulates the battery voltage at 4.2V to fully charge the battery without the risk of overcharging. Upon reaching an end-of-charge (EOC) current, the charger indicates the charge completion with the $\overline{CHG}$ pin, but the charger continues to deliver 4.2V at the VBAT pin until the timeout limit has reached. Figure 1 shows the typical charge profile with the EOC/reset events.

The EOC current level IMIN is programmable with the external resistor R_{IMIN}. The $\overline{CHG}$ signal turns to LO when the trickle charge starts and rises to HIGH at an EOC event. After the EOC is reached, the $\overline{CHG}$ status is latched at HI. The $\overline{CHG}$ status will be reset to logic LO when the VBAT voltage drops to below the recharge threshold (4.05V), as shown in Figure 1.

A thermal foldback function reduces the charge current anytime when the die temperature reaches typically +115°C. This function guarantees safe operation when the printed-circuit board (PCB) is not capable of dissipating the heat generated by the linear charger.

The ISL9301 accepts an input voltage up to 28V but will be disabled when the input voltage exceeds the OVP threshold, minimum 10V, to protect against unqualified or faulty AC adapters.

$\overline{PPR}$ Indication

The $\overline{PPR}$ pin is an open-drain output to indicate the presence of the AC adapter. Whenever the input voltage is higher than the POR threshold, the $\overline{PPR}$ pin turns on the internal open-drain MOSFET to indicate a logic LOW signal. When the internal open-drain FET is turned off, the $\overline{PPR}$ pin should leak less than 1µA current. When turned on, the $\overline{PPR}$ pin should be able to sink at least 10mA current under all operating conditions.

The $\overline{PPR}$ pin can be used to drive an LED (see “Typical Application Circuit” on page 6) or to interface with a microprocessor.

Power-Good Range

The power-good range is defined by the following three conditions:

1. VIN > VPOR
2. VIN - VOUT > VOS
3. VIN < VOVP

where VOS is the offset voltage for the input and output voltage comparator and the VOVP is the overvoltage protection threshold given in the "Electrical Specifications" starting on page 2. All V_{POR}, V_{OS}, and V_{OVP} have hysteresis. The IC will not deliver any output if the input voltage is not in the power-good range.

$\overline{CHG}$ Indication

The $\overline{CHG}$ is an open-drain output. The open drain FET turns on when the charger starts to charge and turns off when the EOC condition is qualified. Once the EOC condition is qualified, the $\overline{CHG}$ signal is latched in off state. The EOC condition is qualified when both of the following conditions are satisfied:

1. $V_{BAT} > V_{RECHG}$
2. $I_{CHG} < I_{MIN}$

The $\overline{CHG}$ indication will not be turned on again until a recharge condition is qualified. A recharge condition is reached under one of the three conditions:

1. Input power being re-cycled
2. Enable signal being toggled
3. A recharge cycle starts when the battery voltage drops below the recharge threshold

The $\overline{CHG}$ signal can be interfaced either with a micro-processor GPIO or a LED for indication. A de-glitch delay of 1ms for both edges is required to prevent nuisance triggering due to some transient conditions.

Charge Termination, Recharge and Timeout

When an EOC condition is reached, the $\overline{CHG}$ pin changes to logic HI to indicate the end-of-charge. However the charger continues to deliver current to the battery until the timeout interval has elapsed, then the charging will be terminated. The setting of the timeout interval is described in “Intelligent Timer” on page 8. When a recharge condition is met after a timeout event, the timer will be reset to zero and the charging re-starts.

In the event when the timeout interval has elapsed before the EOC condition is reached, a timeout fault condition is triggered. The timeout fault condition is indicated by the $\overline{CHG}$ pin being toggled between HI and LO every 3s (R_{TIME} = 1MΩ). The timeout fault condition can be cleared by removing and reapplying the input power to the IC.

Under the EOC, timeout and timeout fault conditions, the power delivery to VOUT is not impacted. The battery continues to supply current to VOUT if needed, as described in “Dynamic Power Path Management” on page 8.

Battery Disconnection

The BATON pin provides an option for disconnection of the battery from the system if battery power is not needed and no power source is applied at VIN. The disconnection will prevent the IC leakage current from draining the battery for an extended period of time. To reconnect the battery, pull the BATON pin to logic HI for 2s. Once the system is powered on, the host micro process will send a logic signal to keep BATON at logic HI level. The BATON pin has a 1MΩ internal pull-down resistor thus, when left floating, the input is equivalent to a logic LOW state. The logic threshold levels are given in the "Electrical Specifications" table starting on page 2.

BATON Interlock

When a valid voltage source is applied at VIN, the BATON function is disabled. This prevents the battery from being connected to a 4.5V regulated voltage source and generating a large circulating current. If the VIN supply is removed, the BATON function will resume immediately to allow the battery to supply the system.

IREF Pin Function

The IREF pin has the two functions as described in “Pin Descriptions” on page 4. When setting the fast charge current, the charge current is trimmed to have 10% accuracy at 145mA, excluding the programming resistor error. The percent error decreases as the set charge current is higher but increases as the set charge current is lower than 145mA. The trickle charge current is 16% of the programmed fast charge current.

When monitoring the charge current, the accuracy of the IREF pin voltage vs the actual charge current has the same accuracy as the gain from the IREF pin current to the actual charge current. The IREF pin voltage vs the charge current

when I_{REF} is set to 145mA is shown in Figure 2. Figure 3 shows a typical time domain charge current curve vs time and its accuracy limits for a complete cycle. The accuracy is compared against the voltage on the IREF pin. Thermal foldback may affect the charge current curve as well as the accuracy.

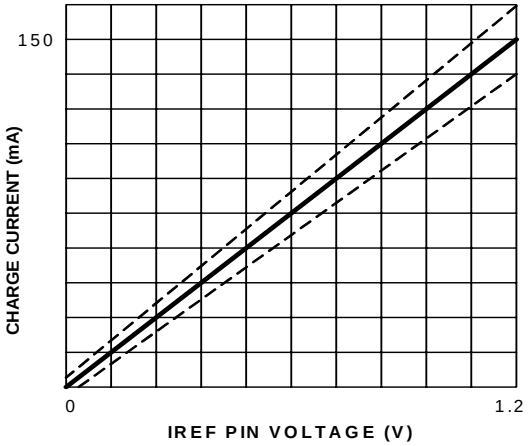


FIGURE 2. IREF PIN VOLTAGE vs CHARGE CURRERNT (IREF IS SET TO 150mA. THE DOTTED LINES SHOW THE UPPER AND LOWER LIMITS OF THE TOLERANCE)

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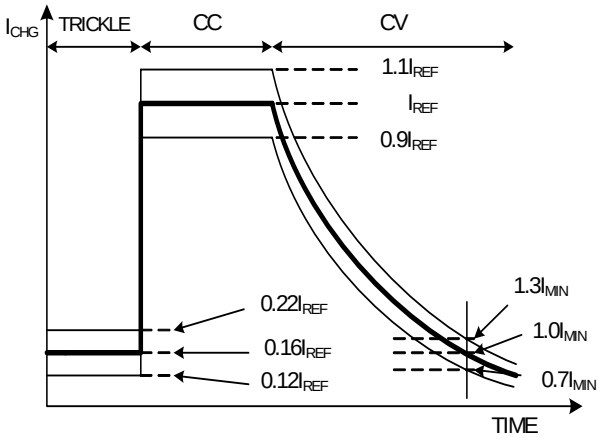


FIGURE 3. CHARGE CURRENT ACCURACY WHEN I_{REF} = 145mA

Dynamic Power Path Management

The power path management function of the ISL9301 controls the charge current and the system current when charging with system load. This is based on the available input current, which is either limited by the IC (800mA) or by the input power source, whichever is smaller. When the output voltage drops to the DPPM threshold (4.35V typical), the dynamic power path management starts to function. The DPPM control will first allocate the available current to the system load, using the remaining current to charge the battery. This is achieved by dynamically reducing the charge current until VOUT is regulated. In the event that the system needs more than the available current, VOUT will continue to drop. When VOUT drops to below the battery voltage, the DPPM control will turn on the charge control FET, allowing the battery to supply current to the system load. Thus the battery may be charged at a current smaller than the programmed constant current.

Intelligent Timer

The internal timer in the ISL9301 provides a time reference for the maximum charge time limit. The nominal clock cycle for the reference time is set by the external resistor connected between the TIME pin and GND and is given by Equation 1.

The nominal maximum charge time interval is calculated based on the assumption that the programmed charge current is always available during the entire charging cycle. However, due to the PPM control or due to the current limit of the input source, or thermal foldback, the actual charge current maybe reduced during the constant current charge period. Under such conditions, the Intelligent Timer control will increase the timeout interval accordingly to allow approximately the same mAh product as the original timeout interval at the programmed current.

Thermal Foldback

The thermal foldback function starts to reduce the charge current when the internal temperature reaches a typical value of +115°C. When thermal foldback is encountered, the charge current will be reduced to a value where the die temperature stops rising.

Figure 5 shows the thermal foldback operation whereas the current signals at the summing node of the current error amplifier CA are shown in Figure 4. I_R is the reference. I_T is the temperature tracking current generated from the Temperature Monitoring block. The I_T has no impact on the charge current until the internal temperature reaches approximately +115°C; then I_T starts to rise. In the mean time, as I_T rises, I_{SEN} will fall at the same rate (as the sum is a constant current IR). As a result, the charging current, which is proportional to I_{SEN}, also decreases, keeping the die temperature constant at +115°C.

The system output current, however, is not impacted by the thermal foldback. Thus, when the charge current is reduced to zero, if the die temperature still rises, the IC will shut down to prevent damage to the IC.

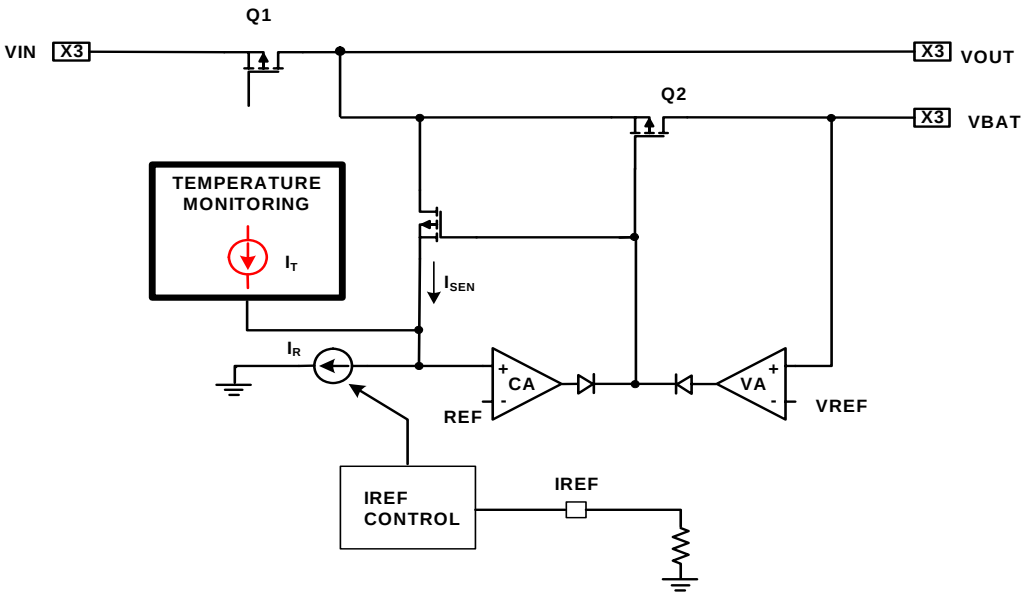


FIGURE 4. CHARGE CURRENT THERMAL FOLDBACK CIRCUIT

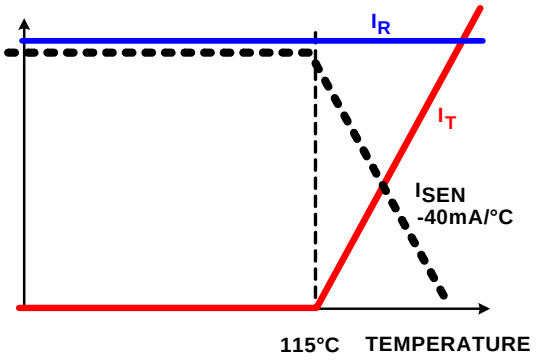


FIGURE 5. CHARGE CURRENT FOLDBACK

Applications Information

Input Bypass Capacitor

The input capacitor is required to suppress the power supply transient response during transitions. Typically, a 10µF or larger capacitor should be sufficient to suppress the power supply noise.

Due to the inductance of the power leads of the wall adapter or USB source, the input capacitor type must be properly selected to prevent high voltage transient during a hot-plug event. A tantalum capacitor is a good choice for its high ESR, providing damping to the voltage transient. Multi-layer ceramic capacitors, however, have a very low ESR and hence when chosen as input capacitor, a 1Ω series resistor must be used (as shown in the “Typical Application Circuit” on page 6) to provide adequate damping.

VOUT and VBAT Capacitor Selection

The criteria for selecting the capacitor at the VOUT and VBAT pins is to maintain the stability as well as to bypass any transient load current. The recommended capacitance is a 4.7µF X5R ceramic capacitor for VOUT and 1µF for VBAT. The actual capacitance connected to the output is dependent on the actual application requirement.

Layout Guidance

The ISL9301 uses a thermally-enhanced DFN package that has an exposed thermal pad at the bottom side of the package. The layout should connect as much as possible to copper on the exposed pad. Typically, the component layer is more effective in dissipating heat. The thermal impedance can be further reduced by using other layers of copper connecting to the exposed pad through a thermal via array. Each thermal via is recommended to have 0.3mm diameter and 1mm distance from other thermal vias.

Input Power Sources

The input power source is typically a well-regulated wall cube with 1m length wire or a USB port. The input voltage ranges from 4.3V to 10V. The ISL9301 can withstand up to 28V on the input without damaging the IC. If the input voltage is higher than the OVP threshold, the IC is disabled.

State Diagram

The state diagram is shown in Figure 6. There are 8 states to cover all the operation modes, including the Trickle Charge, Batt Discharge, PPM, CV Charge, Charge Fault, Charge Complete, Disabled and OTP states.

The IC starts with a trickle charge or constant current charge state depending on VBAT when input power is applied. In the Trickle Charge state, the $\overline{PPR}$ is LO and the $\overline{CHG}$ is LO,

VOUT is regulated at 4.5V, the charger is ON, delivering a trickle charge current.

The IC moves to a fast charge constant current mode when VBAT reaches the VMIN threshold. There are 3 possible states in this mode depending on the output current. When the sum of the output current and the fast charge current is smaller than the input current limit, the IC enters the Fast Charge state with the charge current set by R_{IREF}. When the output current and the fast charge current are greater than the input current limit, the IC will enter the PPM mode, where the charging current is reduced to a point such that the sum of output current and the charging current equals to the input current limit. If the output current by itself is greater than the input current limit, the IC enters the Battery Discharge state, where the battery is discharged to the system to supply a part of the output demand.

When the battery voltage reaches 4.2V, the IC enters the CV Charge state, where $\overline{PPR}$ is LO, $\overline{CHG}$ is LO and VOUT is regulated at 4.5V. The battery is being charged at a constant voltage while the charging current decreases.

When the charging current is reduced to the IMIN threshold, the IC enters a Charge Complete state, where $\overline{PPR}$ is LO, $\overline{CHG}$ is HI, VOUT is regulated at 4.5V and the charger continues to charge the battery.

When the timeout interval has elapsed after the Charge Complete state, the IC will enter the Disabled state, where the $\overline{PPR}$ is LO, $\overline{CHG}$ is HI, VOUT is regulated at 4.5V and the charger is OFF. After the Charge Complete state, if VBAT is below the re-charge threshold, the IC will re-initialize and start a new cycle.

If the timeout limit is reached before the Charge Complete state, the IC enters the Charger Fault state, where $\overline{PPR}$ is LO, $\overline{CHG}$ is blinking, VOUT is regulated at 4.5V and the charger is OFF. This state is latched until the input power is removed and re-applied to start a new cycle.

Any time during the operation, if the die temperature reaches the OTP threshold, the IC will enter the OTP state, where $\overline{PPR}$ is LO, $\overline{CHG}$ is HI, and the charger is OFF. VOUT is disconnected from VIN and connected to VBAT internally to maintain system power need.

Summary of Output States

The output states under various fault conditions are summarized in Table 1.

TABLE 1. OUTPUT STATES UNDER FAULT CONDITIONS

OTP	OVP	BATON	M1	M2
Y	Y	H	OFF	ON
Y	N	H	OFF	ON
N	Y	H	OFF	ON
Y	Y	L	OFF	OFF
Y	N	L	OFF	OFF
N	Y	L	OFF	OFF
N	N	X	Regulating	Charging

NOTES:

BATON: BATON Pin

OVP: Input Over Voltage Protection

OTP: Over Temperature Protection

M1: Output Path MOSFET

M2: Battery Path MOSFET

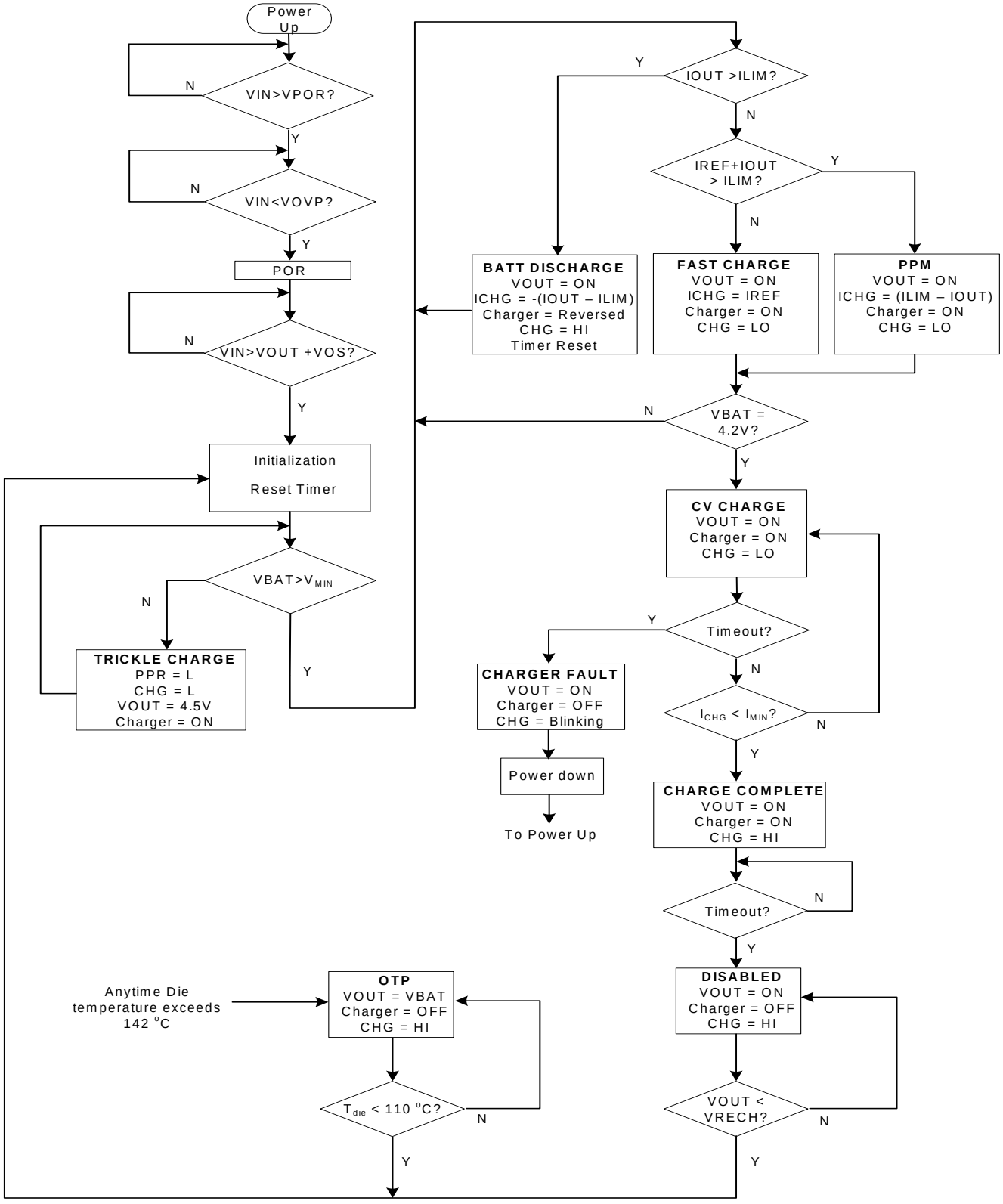
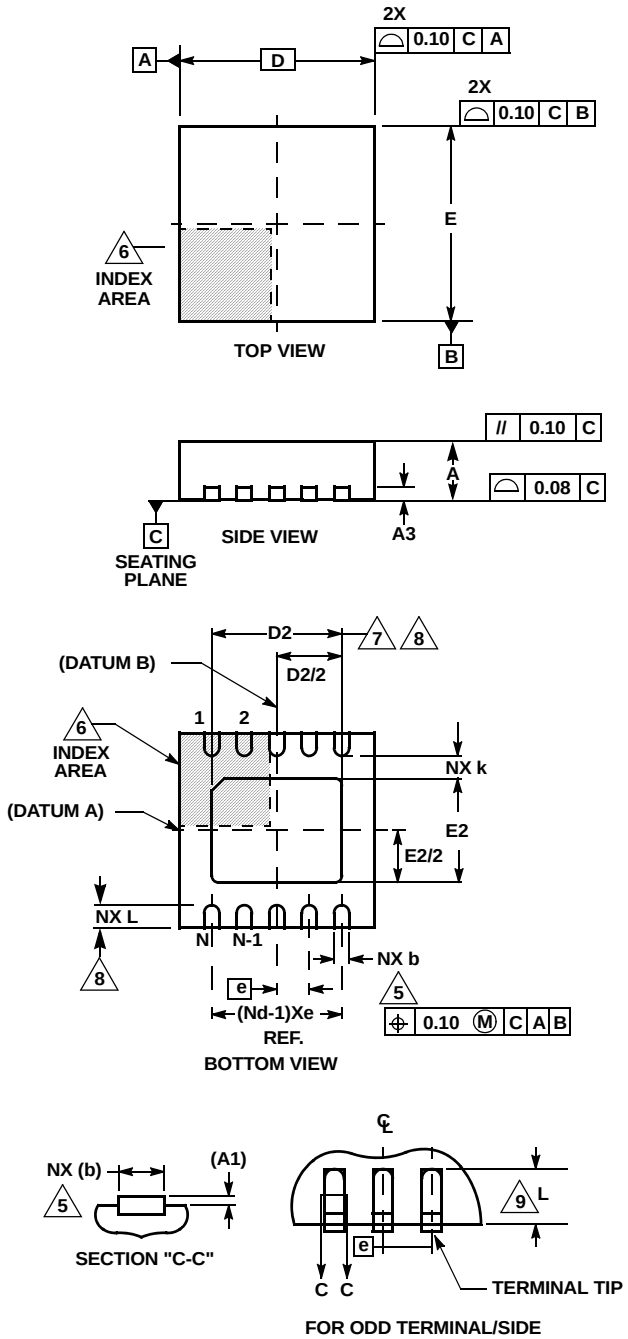


FIGURE 6. STATE DIAGRAM

Dual Flat No-Lead Plastic Package (DFN)



L10.3x3C

10 LEAD DUAL FLAT NO-LEAD PLASTIC PACKAGE

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.85	0.90	0.95	-
A1	-	-	0.05	-
A3		0.20 REF		-
b	0.20	0.25	0.30	5, 8
D		3.00 BSC		-
D2	2.33	2.38	2.43	7, 8
E		3.00 BSC		-
E2	1.59	1.64	1.69	7, 8
e		0.50 BSC		-
k	0.20	-	-	-
L	0.35	0.40	0.45	8
N		10		2
Nd		5		3

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NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd refers to the number of terminals on D.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. COMPLIANT TO JEDEC MO-229-WEED-3 except for dimensions E2 & D2.