ALL SHORE INDUSTRIES

ASI-T-300EA3AN/D

Item	Contents	Unit
Size	3.0	inch
Resolution	320(RGB)x240	/
Interface	8-bit RGB /8-bit Dummy RGB / CCIR656 / 601	/
Technology type	a-Si TFT	/
Pixel pitch	0.1875x0.1875	mm
Pixel Configuration	RGB Delta	
Outline Dimension (W x H x D)	70.20 x 51.40 x 2.65	mm
Active Area	60.00 x 45.00	mm
Display Mode	Transmissive Normally White,	/
Backlight Type	LED	/
Driver IC	HX8268C	/

Record of Revision

Date	Revision No.	Summary

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1. Scope

This data sheet introduces the specification of ASI-T-300EA3AN/D active matrix TFT module. It is composed of a color TFT-LCD panel, driver ICs, FPC and a backlight unit. The 3.0″ display area contains 320 (RGB) x 240 pixels.

2. Application

Digital equipments which need color display, DSC, mobile navigator/video systems.

3. General Information

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Backlight Type	LED	/
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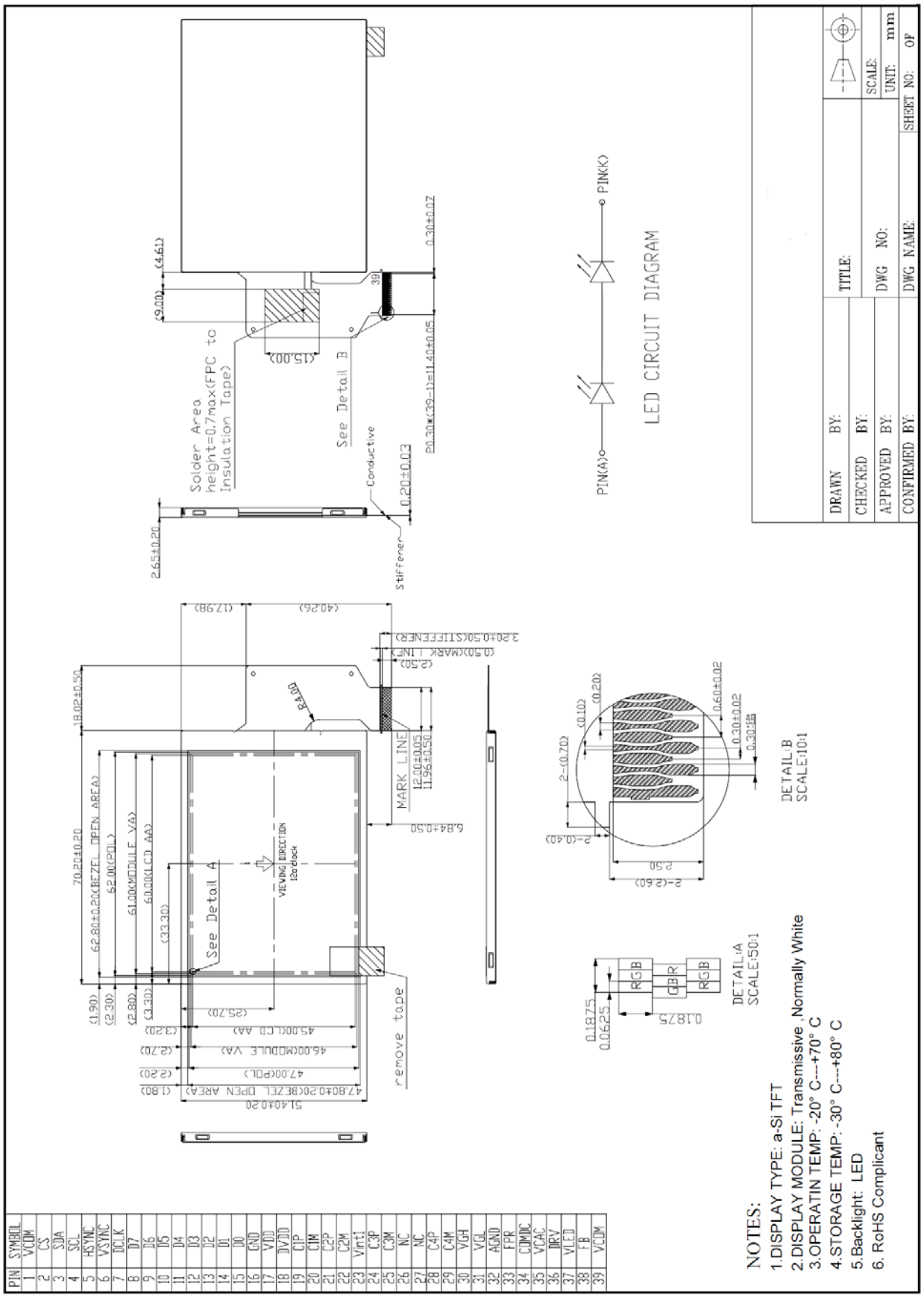
4. Outline Drawing



PIN	SYMBOL
1	VCOM
2	CS
3	SDA
4	SCL
5	HSYNC
6	VSYNC
7	DCLK
8	D7
9	D6
10	D5
11	D4
12	D3
13	D2
14	D1
15	D0
16	GND
17	VDD
18	DVDD
19	C1P
20	C1M
21	C2P
22	C2M
23	Vint
24	C3P
25	C3M
26	NC
27	NC
28	C4P
29	C4M
30	VGH
31	VGL
32	AGND
33	FPR
34	COMDC
35	VCAC
36	DRV
37	VLED
38	FB
39	VCOM

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5. Interface signals

No	Symbol	I/O	Description	Remarks
1	VCOM	I	Panel common voltage	
2	CS	I	SPI enable	
3	SDA	I/O	SPI data input/output	
4	SCL	I	SPI clock input	
5	HSYNC	I	Horizontal sync input.(HSD)	
6	VSYNC	I	Vertical sync input.(VSD)	
7	DCLK	I	Data clock input.(CLKIN)	
8	DB7	I	Data input; MSB	
9	DB6	I	Data input	
10	DB5	I	Data input	
11	DB4	I	Data input	
12	DB3	I	Data input	
13	DB2	I	Data input	
14	DB1	I	Data input	
15	DB0	I	Data input; LSB	
16	DGND	P	Power ground	
17	VDD	P	Supple power	
18	DVDD	C	Power setting capacitor connect pin	
19	C1P	C	Capacitor for charge pump	
20	C1M	C	Capacitor for charge pump	
21	C2P	C	Capacitor for charge pump	
22	C2M	C	Capacitor for charge pump	
23	VINT1	C	Power setting capacitor connect pin	
24	C3P	C	Capacitor for charge pump	
25	C3M	C	Capacitor for charge pump	
26	NC	--	No connect	
27	NC	--	No connect	
28	V4P	C	Capacitor for charge pump	
29	V4M	C	Capacitor for charge pump	
30	VGH	C	Power setting capacitor connect pin	
31	VGL	C	Power setting capacitor connect pin	
32	AGND	P	Power ground	
33	FRP	O	Frame Polarity output for VCOM	
34	COMDC	O	VCOM DC output in	
35	VCAC	C	Power setting capacitor connect pin	
36	CRV	--	No connect	
37	LED+	P	LED power anode	
38	FB	P	LED power cathode	
39	VCOM	I	Panel common voltage	

Recommend connector:FH26-39S-0.3 SHW(0.5)

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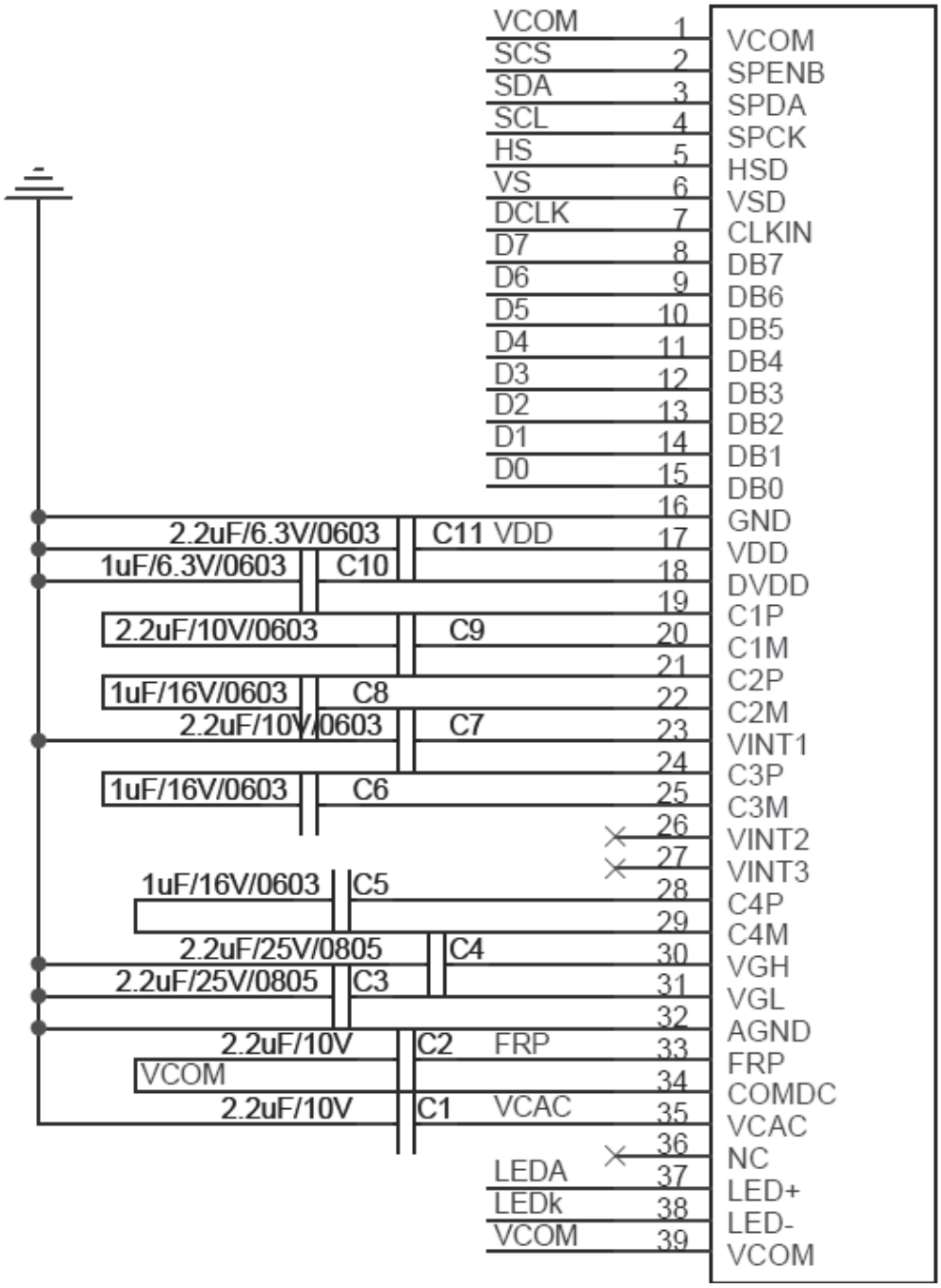
Application Circuit



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6. Absolute maximum Ratings

6.1. Electrical Absolute max. ratings

Parameter	Symbol	MIN	MAX	Unit	Remark
Logic Supply Voltage	VDD	-0.3	5	V	
Analog Supply Voltage	VDD	-0.3	5	V	
Input Signal Voltage	DB0~DB7,VCOM,CS,SDA,SCL,HSYNC,VSYNC,DCLK	-0.3	VDD+0.3	V	

6.2. Environment Conditions

Item	Symbol	MIN	MAX	Unit	Remark
Operating Temperature	TOPR	-20	70	℃	
Storage Temperature	TSTG	-30	80	℃	

6.3. LED Backlight Absolute max. ratings

Item	Symbol	MIN	MAX	Unit	Remark
LED Forward Current	ILED	--	25	mA	For each LED

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7. Electrical Specifications

7.1 Electrical characteristics

GND=0V, Ta=25℃

Item	Symbol	MIN	TYP	MAX	Unit	Remark
Logic Supply Voltage	VDD	3.0	3.3	3.6	V	
Analog Supply Voltage	VDD	3.0	3.3	3.6	V	
Input Signal Voltage	VIL	GND	--	0.3 x VDD	V	VDD = 2.7V~3.6V
		GND	--	0.2 x VDD	V	VDD = 1.65V~2.7V
	VIH	0.7 x VDD		VDD	V	VDD = 2.7V~3.6V
		0.8 x VDD	--	VDD	V	VDD = 1.65V~2.7V
Output Signal Voltage	VOL	GND	--	0.4	V	
	VOH	VDDIO -0.4	--	VDDIO	V	

7.2 LED Backlight

Ta=25℃

Item	Symbol	MIN	TYP	MAX	Unit	Remark
Forward Current	IF		20		mA	For each LED
Forward Voltage	VF		3.2		V	
Power Consumption	--		128		mW	

Note 1: The figure below shows the connection of backlight LED.

Note 2: One LED: IF =25mA, VF =3.2V.

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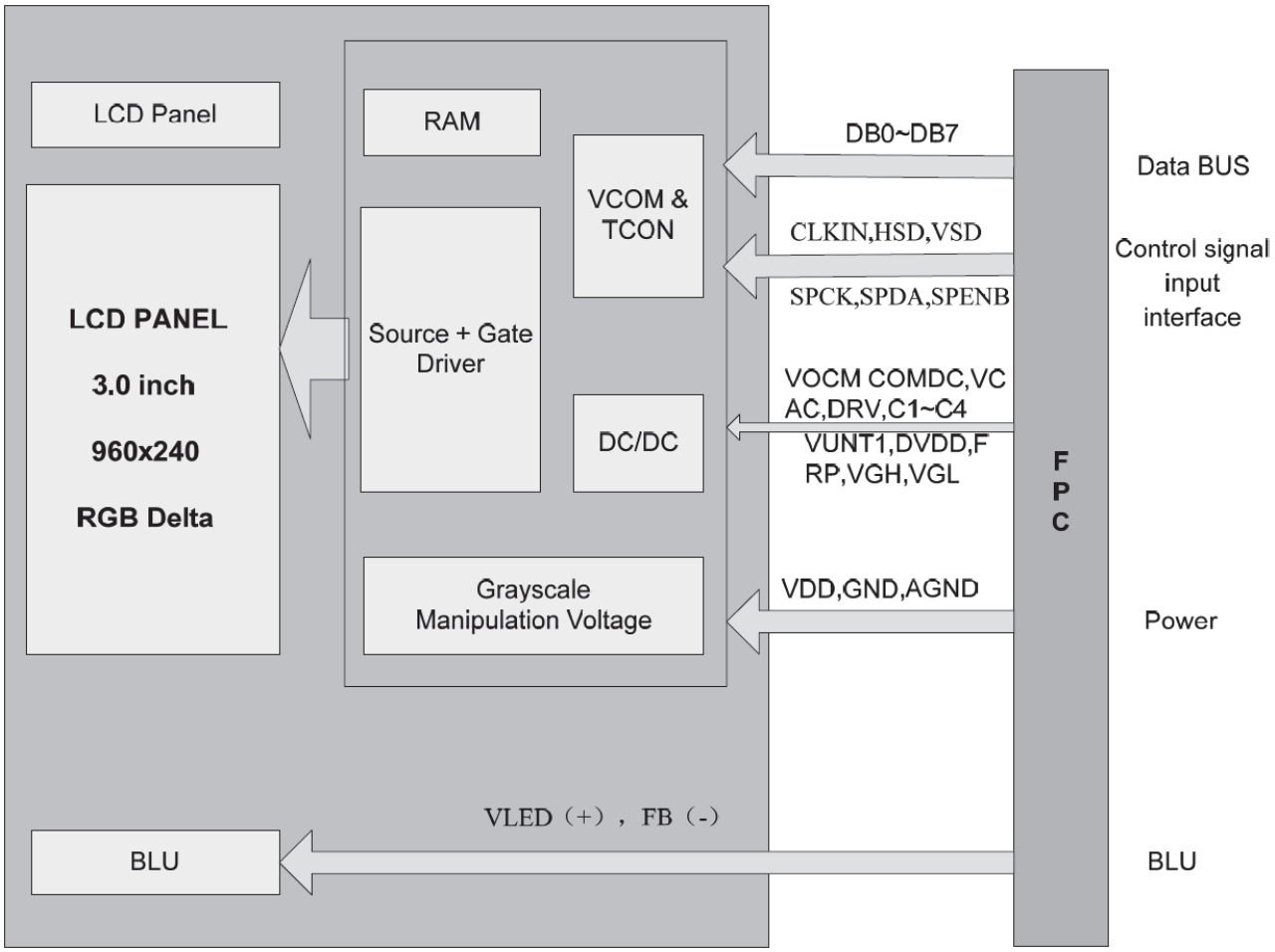
7.3 Block Diagram



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8. Command/AC Timing

8.13-WIRE SERIAL CONTROL INTERFACE

8.2 3-WIRE REGISTER TABLE

Register	Register address								Register data (Default)							
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R00h	0	0	0	0	0	0	0	0	Y_CbCr	CCIR601	x	Fine_AC	VCOM_AC			
									0	0		0	1	0	1	1
R01h	0	0	0	0	0	0	0	1	VCDCEN	x	VCOM_DC					
									1		0	1	1	0	0	0
R03h	0	0	0	0	0	0	1	1	Brightness							
									0	1	0	0	0	0	0	0
R04h	0	0	0	0	0	1	0	0	Narrow	YUV	SEL		NTSC/PAL		VDIR	HDIR
									0	0	0	0	1	0	1	1
R05h	0	0	0	0	0	1	0	1	DRV_FREQ	GRB	PWM_DUTY			VGH/L_EN	LED_EN	x
									0	1	0	1	1	1	1	
R06h	0	0	0	0	0	1	1	0	HBLK_EN	LED_Current		VBLK				
									0	0	0	1	0	1	0	1
R07h	0	0	0	0	0	1	1	1	HBLK							
									0	1	0	0	0	1	1	0
R08h	0	0	0	0	1	0	0	0	BL_DRV		x					
									0	0						
R09h	0	0	0	0	1	0	0	1	x				RGBW	x		
													0			
R0Bh	0	0	0	0	1	0	1	1	REGSEL	x		Sync_DE	x			Soften_Edge
									0			0				1
R0Ch	0	0	0	0	1	1	0	0	PAIR		DESEL	CbCr	DEpol	VDpol	HDpol	CLKINpol
									0	0	0	0	0	1	1	0
R0Dh	0	0	0	0	1	1	0	1	CONTRAST							
									0	1	0	0	0	0	0	0
R0Eh	0	0	0	0	1	1	1	0	×	SUB-CONTRAST_R						
										1	0	0	0	0	0	0
R0Fh	0	0	0	0	1	1	1	1	×	SUB-BRIGHTNESS_R						
										1	0	0	0	0	0	0
R10h	0	0	0	1	0	0	0	0	×	SUB-CONTRAST_B						
										1	0	0	0	0	0	0
R11h	0	0	0	1	0	0	0	1	×	SUB- BRIGHTNESS _B						
										1	0	0	0	0	0	0
R12h	0	0	0	1	0	0	1	0	TRMEN							
									0	0	0	0	0	0	0	0
R13h	0	0	0	1	0	0	1	1	x							ENTRY_EN
																0
R16h	0	0	0	1	0	1	1	0	×					GAMMA2.2		×
														1		
R2Bh	0	0	1	0	1	0	1	1	×							STB
																0
R2Fh	0	0	1	0	1	1	1	1	VGH_SEL			CF_SEL	LC_TYPE			SOPC
									0	1	1	0	0	0	0	1
R30h	0	0	1	1	0	0	0	0	5GammaNP_sel	x		L00P_SEL				
									1			1	1	0	0	1
R31h	0	0	1	1	0	0	0	1	x			L02P_SEL				
												1	0	1	0	0
R32h	0	0	1	1	0	0	1	0	x			L08P_SEL				
												0	1	0	0	0
R33h	0	0	1	1	0	0	1	1	x			L16P_SEL				
												0	1	0	0	0
R34h	0	0	1	1	0	1	0	0	x			L32P_SEL				
												0	1	0	0	0
R35h	0	0	1	1	0	1	0	1	x			L50P_SEL				
												0	1	0	0	0
R36h	0	0	1	1	0	1	1	0	x			L72P_SEL				

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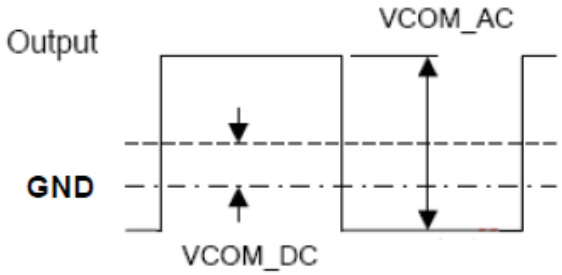
R55h	1	0	0	1	0	1	0	1	×	INV_SEL 0	NBW 0	x
R57h	1	0	0	1	0	1	1	1	VGHL_ENB 0	x		
R5Ah	1	0	0	1	1	0	1	0	x			VGL_SEL 0 1 0

Note:
1. When RSTB is low, all registers reset to default values.
2. Serial commands are executed at next VSYNC signal.

8.33-WIRE REGISTER DESCRIPTION

VCOM_AC: Common voltage AC level selection

D3	D2	D1	D0	LV LC (V)	NV LC-1 (V)	NV LC-2 (V)
0	0	0	0	3.7	4.0	5.0
0	0	0	1	3.8	4.1	5.1
0	0	1	0	3.9	4.2	5.2
0	0	1	1	4.0	4.3	5.3
0	1	0	0	4.1	4.4	5.4
0	1	0	1	4.2	4.5	5.5
0	1	1	0	4.3	4.6	5.6
0	1	1	1	4.4	4.7	5.7
1	0	0	0	4.5	4.8	5.8
1	0	0	1	4.6	4.9	5.9
1	0	1	0	4.7	5.0	6.0
1	0	1	1	4.8 (Default)	5.1 (Default)	6.1 (Default)
1	1	0	0	4.9	5.2	6.2
1	1	0	1	5.0	5.2	6.2
1	1	1	0	5.1	5.2	6.2
1	1	1	1	5.2	5.2	6.2



Fine_AC: Set Fine_AC=1 to increase VCOM_AC 0.05V. Set Fine_AC=0, VCOM_AC will keep setting voltage.

CCIR601: CCIR601 input timing selection

CCIR601	Function
0	Disable CCIR601. (Default)
1	Enable CCIR601. (Please refer to the table of R4(SEL) for detail description)

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Y_CbCr: Y & CbCr exchange position (only valid for 8-bit input YUV640 / YUV720)

Y_CbCr	CbCr (R12[4])															
	0								1							
0	Cb0	Y0	Cr0	Y1	Cb2	Y2	Cr2	Y3	Cr0	Y0	Cb0	Y1	Cr2	Y2	Cb2	Y3
1	Y0	Cb0	Y1	Cr0	Y2	Cb2	Y3	Cr2	Y0	Cr0	Y1	Cb0	Y2	Cr2	Y3	Cb2

R01h：VCOM DC setting

Address								Data setting							
A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	1	VCDCEN	-	VCOM_DC					
Initial setting value (Default)								1	-	0	1	1	1	0	0

VCOM_DC: Common voltage DC level selection (20mV/step)

D[5:0]	VCOM DC offset
00h	0.24
:	:
1Ch	0.8 (Default)
3Fh	1.5

VCDCEN: VCOM DC enable control

VCDCE	Function
0	VCOM_DC function disabled. The VCOMDC pin is disabled (Connection with GND)
1	VCOM_DC function enabled. The VCOMDC voltage follows VCOM_DC setting. (Default)

R03h：Whole brightness adjustment

Address								Data setting							
A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	1	1	Brightness							
Initial setting value (Default)								0	1	0	0	0	0	0	0

Brightness: Adjust RGB brightness

D[7:0]	Brightness gain
00h	Dark(-64)
40h	Center(0)(Default)
FFh	Bright(+191)

Setting accuracy 1bit/step

R04h：

Address								Data setting							
A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	1	0	0	Narrow	YUV	SEL		NTSC/PAL		VDIR	HDIR
Initial setting value (Default)								0	0	0	0	1	0	1	1

HDIR: Shift registers of source driver direction selection

D0	HDIR function
0	Shift from right to left. Y1 Y2 ← Y959 Y960
1	Shift from left to right. Y1 Y2 → Y959 Y960 (Default)

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NTSC/ PAL: NTSC or PAL input mode selection

D3	D2	NTSC/PAL mode
0	0	PAL.
0	1	NTSC.
1	x	Auto detection. (Default)

SEL: Input data timing format selection

CCIR601 R00[D6]	YUV R04[D6]	SEL		Input timing format
		R04 [D5]	R04[D4]	
0	0	0	0	8-bit RGB. (Default)
0	0	0	1	8-bit Dummy RGB 320 x 240.
0	0	1	x	8-bit Dummy RGB 360 x 240.
0	1	x	x	CCIR656.
1	1	0	x	YUV 640.
1	1	1	0	YUV 720.

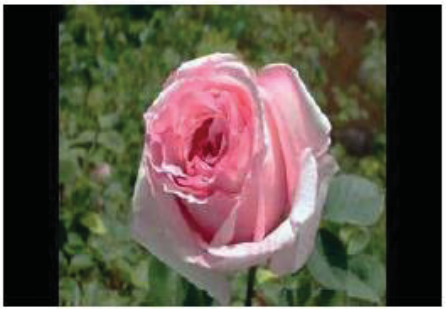
YUV: CCIR601/CCIR656 or RGB/RGB-Dummy input selection

D6	Data format
0	RGB/RGB-Dummy input. (Default)
1	CCIR656/YUV640/YUV720 input.

Narrow: Normal display and Narrow display selection

D7	Narrow function
0	Normal display. (Default)
1	Narrow display

Note: Narrow function was not supporting 8-bit RGB and 24-bit RGB input mode.



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VGH/L_EN : Shut down for VGH/VGL charge pump

D1	VGH/L_EN function
0	VGH/VGL charge pump is off.
1	VGH/VGL charge pump is controlled by STB's power on/off sequence. (Default)

PWM_DUTY: PWM duty cycle selection for back light power convert

PWM_DUTY			Function
D5	D4	D3	PWM duty cycle
0	0	0	20%
0	0	1	26%
0	1	0	32%
0	1	1	38% (Default)
1	0	0	44%
1	0	1	50%
1	1	0	56%
1	1	1	62%

GRB : Global reset

D6	GRB function
0	Reset all registers to default value.
1	Normal operation. (Default)

DRV_FREQ : DRV signal frequency setting

D7	GRB function
0	High frequency (Default)
1	Low frequency

R06h :

Address								Data setting							
A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	1	1	0	HBLK_EN	LED_Current		VBLK				
Initial setting value (Default)								0	0	0	1	0	1	0	1

VBLK : Vertical blanking setting for 8-bit RGB , 8-bit dummy RGB & CCIR656

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For 8-bit dummy RGB, CCIR656, YUV640 and YUV720 PAL mode. (Vertical blanking+3)

D[4:0]	Function	Unit
00h	3	H(Line)
04h	7	
15h	24(Default)	
1Fh	34	

LED_CURRENT : LED current adjustable for DC-DC feedback threshold voltage

D[6:5]	Feedback threshold voltage
00	0.6 V. (Default)
01	0.75V.
10	0.45V.
11	0.3V.

HBLK_EN : HBLK function enable

D[7]	HBLK EN function
0	Disable(Default)
1	Enable

R07h : Horizontal blanking setting

Address								Data setting							
A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	1	1	1	HBLK							
Initial setting value (Default)								0	1	0	0	0	1	1	0

HBLK : Horizontal blanking setting

HBLK_EN	D7~D0	HBLK	Unit	NTSC/PAL mode
X	32h~45h	50~69	CLKIN	8-bit RGB.
X	46h	70		
X	47h~FFh	71~255		
0	X	241		8-bit dummy RGB.
1	00h~03h	3		
	04h~FFh	4~255		
0	XXh	240		YUV640, YUV720.
1	00h~03h	3		
	04h~FFh	4~255		
0	X	61		Parallel RGB
1	04h~3Fh~	4~63		

R08h : Backlight driving capacity setting

Address								Data setting							
A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	0	0	0	BL_DRV		-	-	-	-	-	-
Initial setting value (Default)								0	0	-	-	-	-	-	-

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BL_DRV: Backlight driving capability setting

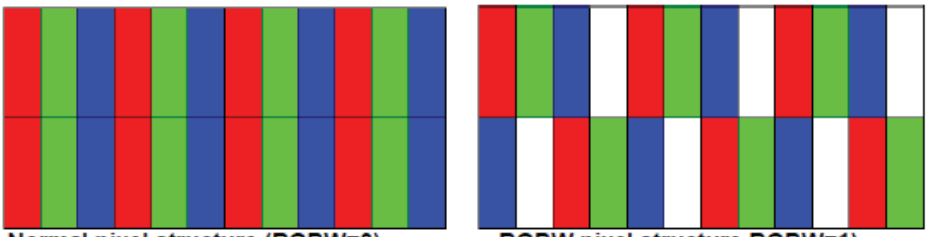
D7	D6	BL_DRV capability
0	0	Normal capability. (Default)
0	1	2 times the Normal capability.
1	0	4 times the Normal capability.
1	1	8 times the Normal capability.

R09h：RGBW function

Address								Data setting							
A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	0	0	1	-	-	-	-	RGBW	-	-	-
Initial setting value (Default)								-	-	-	-	0	-	-	-

D3: RGBW color filter mapping selection

D3	RGBW color filter mapping selection
0	Normal pixel structure
1	RGBW pixel structure



Normal pixel structure (RGBW=0) RGBW pixel structure RGBW=1)

Figure 6.2: RGBW color filter mapping

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R0Bh：

Address								Data setting							
A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	0	1	1	REGSEL	-	-	SYNCSEL	-	-	-	Soften Edge
Initial setting value (Default)								0	-	-	0	-	-	-	1

Soften Edge:

D1	Soften Edge function
0	Disable
1	Enable

Note: This function only for 320RGBx240 entry mode.

SYNCSEL: HV+DE mode selection

D4	SYNCSEL function
0	Select by R0Ch DESEL register
1	HV+DE mode

REGSEL：MTP function control register

D7	REGSEL function
0	VCOM_DC[5:0] is read from MTP memory. (Default)
1	VCOM_DC[5:0] is switch to the 3-wire register memory when user want to adjust the VCOMDC level for test propose. Refer to the "TRMEN" control register for the proper MPT write operation.

R0Ch：

Address								Data setting							
A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	1	0	0	PAIR		DESEL	CbCr	DEpol	VDpol	HDpol	CLKINpol
Initial setting value (Default)								0	0	0	0	0	1	1	0

CLKINpol：CLKIN polarity selection

D0	CLKINpol function
0	Positive polarity. (Default)
1	Negative polarity

HDpol：HSD polarity selection

D1	HDpol function
0	Positive polarity.
1	Negative polarity. (Default)

VDpol：VSD polarity selection

D2	VDpol function
0	Positive polarity.
1	Negative polarity. (Default)

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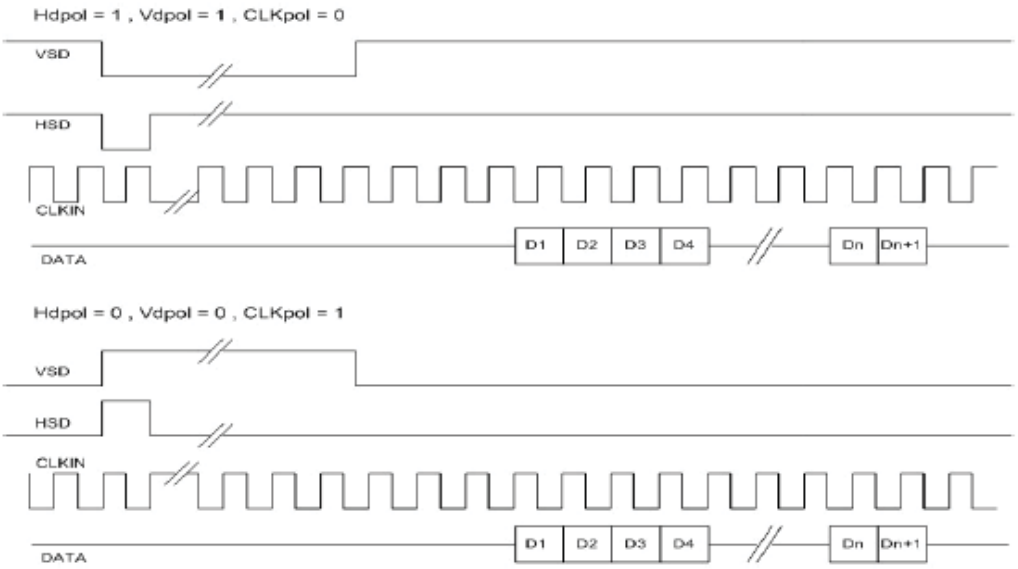

DEpol：DEN polarity selection

D3	DEpol function
0	Positive polarity (Default)
1	Negative polarity

CbCr：Cb & Cr exchange position (valid for CCIR656 and YUV640/YUV720)

D4	CbCr function
0	Cb→Y→Cr. (Default)
1	Cr→Y→Cb

DESEL：DE Mode selection

D5	DESEL function
0	HV mode selected. (Default)
1	DE mode selected.

DESEL only controls the HV and DE mode at 8-bit RGB, 8-bit dummy RGB and parallel mode.

PAIR：Vertical start time of Odd/Even frame

PAIR		VBLK	Unit
D7	D6	ODD/EVEN	
-	0	21/21. (Default)	H (Line)
-	1	21/20.	

For 8-bit RGB / 8-bit dummy RGB NTSC / 8-bit dummy RGB PAL, parallel RGB mode(PSEL=0).
The typical value of VBLK of 8-bit Dummy RGB PAL(24 H) is different than 8-bit RGB/8-bit dummy RGB NTSC(21H).

PAIR		VBLK	Unit
D7	D6	ODD/EVEN	
0	0	21/21. (Default)	H (Line)
0	1	21/22.	
1	0	22/21.	
1	1	22/22.	

For CCIR656/YUV640/YUV720 NTSC/PAL.
The typical value of VBLK of CCIR656 PAL(24 H) is different than CCIR656 NTSC(21H).

Note：Vertical blanking must be adjusted base on the input data.

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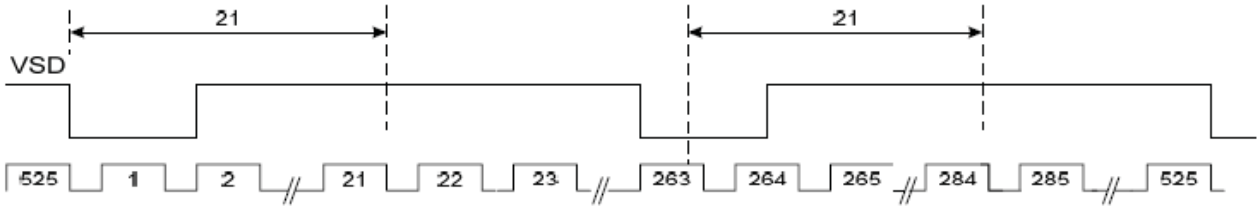
For example:



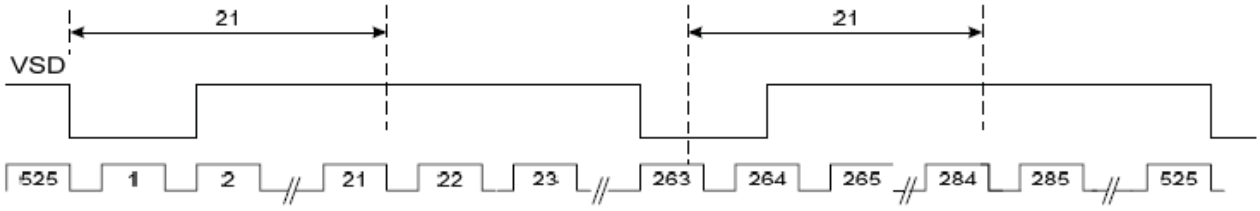
R0Dh：Whole contrast adjustment

Address								Data setting							
A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	1	0	1	CONTRAST							
Initial setting value (Default)								0	1	0	0	0	0	0	0

CONTRAST : RGB contrast level setting , the gain changes (1/64) / bit

D[7:0]	Contrast gain
00h	0
40h	1 (Default)
FFh	3.984

For example:



R0Dh：Whole contrast adjustment

Address								Data setting							
A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	1	0	1	CONTRAST							
Initial setting value (Default)								0	1	0	0	0	0	0	0

CONTRAST : RGB contrast level setting , the gain changes (1/64) / bit

D[7:0]	Contrast gain
00h	0
40h	1 (Default)
FFh	3.984

R10h：B contrast adjustment

Address								Data setting							
A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	0	0	0	-	SUB-CONTRAST_B						
Initial setting value (Default)								-	1	0	0	0	0	0	0

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SUB-CONTRAST_B：Blue sub-pixel contrast level setting, the gain changes (1/256)/bit

D[6:0]	B Contrast gain
00h	0.75
40h	1 (Default)
7Fh	1.246

R11h：B brightness adjustment

Address								Data setting							
A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	0	0	1	-	SUB-BRIGHTNESS_B						
Initial setting value (Default)								-	1	0	0	0	0	0	0

SUB-BRIGHTNESS_B：Blue sub-pixel brightness level setting, setting accuracy: 1 step/bit

D[6:0]	B Brightness gain
00h	DARK (-64)
40h	Center(0) (Default)
7Fh	Bright (+63)

R12h：Instruction for MTP

Address								Data setting							
A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	0	1	0	TRMEN							
Initial setting value (Default)								0	0	0	0	0	0	0	0

TRMEN：VCOM DC Trim Function Control Register

VCOMDC Trim function control register, this IC have build-in MTP memory, at Power-on, IC will auto load the MTP memory to set the VCOMDC level to prevent flick issue.

Operation condition:
1. CLKIN frequency range 26Mhz~30Mhz
2. Apply 7.5V to VPPMTP pin.

Programming procedure:
1. Set REGSEL=1
2. Adjustment VCOM_DC(R1[5:0]) value, select proper VCOM_DC value
3. Set TRMEN[7:0] as following sequence : **A0h →5Fh →EEh →00h**.
4. Hold 1s for MTP control block operation.
5. Set REGSEL=0 and restart the display operation.
6. Check the VCOMDC value.

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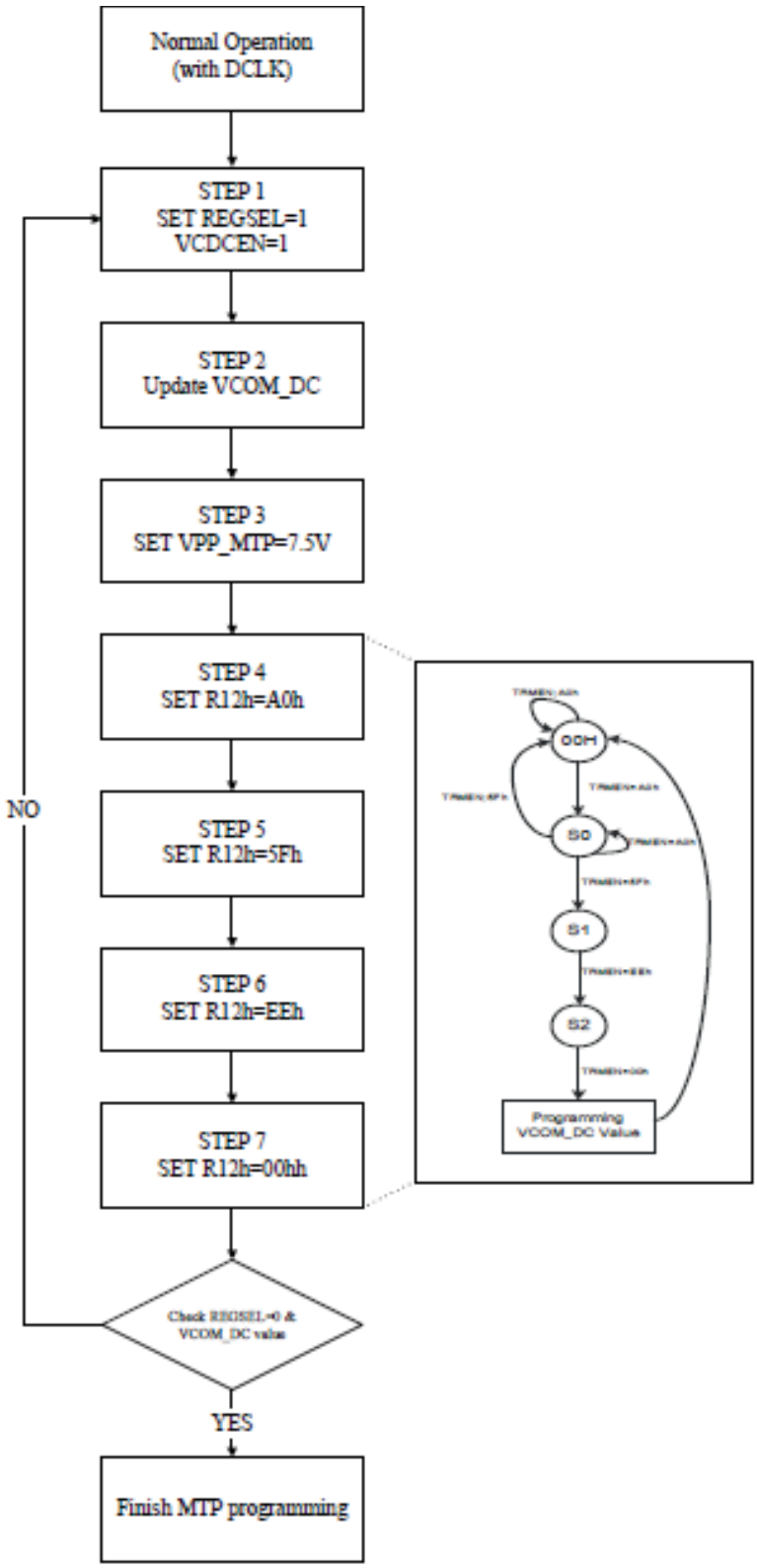

Figure 6.3: MTP programming flow chart

Note:(1) The Trim Block can be writing only for "3" times.
(2) After finishing TRMEN command do not power off within 1 second.
(3) Trim command exceed the limit may cause the VCOMDC output unknown value.

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R13h：Entry function control

Address								Data setting							
A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	0	1	1	-	-	-	-	-	-	-	ENTRY_EN
Initial setting value (Default)								-	-	-	-	-	-	-	0

ENTRY_EN：Entry function control

D0	Entry function
0	Through mode: Input data must be aligned with the color filter arrangement (Default).
1	Alignment mode: Input data must always be the R1, G1, B1,R2, G2, B2, …sequence, and the R/G/B data will be swapped automatically based on the selected color filter arrangement.

R16h：Gamma 2.2

Address								Data setting							
A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	1	1	0	-	-	-	-	-	GAMMA2.2	-	-
Initial setting value (Default)								-	-	-	-	-	1	-	-

GAMMA2.2 : Select auto or manual gamma setting

D2	GAMMA2.2 function
0	Manual set gamma by R30h~R3Bh and R6Ch~R77h.
1	Auto set to gamma2.2. (Default)

R2Bh：Standby mode

Address								Data setting							
A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	0	1	1	-	-	-	-	-	-	-	STB
Initial setting value (Default)								-	-	-	-	-	-	-	0

R2Fh：

Address								Data setting							
A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	1	1	1	VGH_SEL			CF_SEL	LC_TYPE		SOPC	
Initial setting value (Default)								0	1	1	0	0	0	0	1

SOPC：Source output driving capability selection

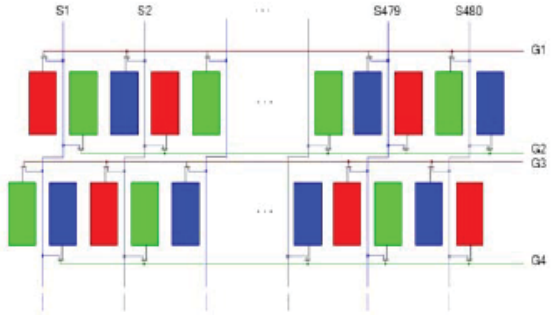
D1	D0	Source driver capability
0	0	-25%.
0	1	Normal. (Default)
1	0	+25%.
1	1	+50%.

LC_TYPE : LC type selection

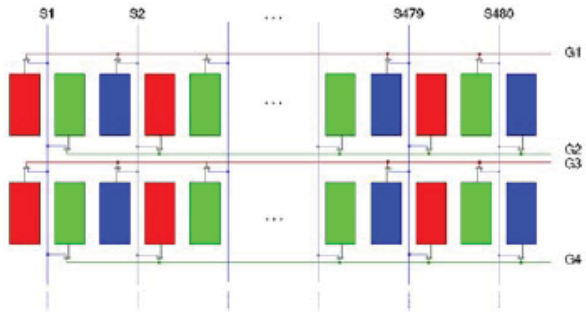
D5	D4	LC_TYPE function
0	0	Low voltage LC (Default)
0	1	Reserved
1	0	Normal LC2
1	1	Normal LC1

CF_SEL : Color filter selection

CF_SEL	CF_SEL function
0	Delta color filter. (Default)
1	Stripe color filter.



Delta color filter@960x240



Stripe color filter@960x240

VGH_SEL : VGH voltage level selection

VGH_SEL			
D7	D6	D5	VGH voltage
0	0	0	13V
0	0	1	14V
0	1	0	15V
0	1	1	16V (Default)
1	0	0	17V
1	0	1	18V
1	1	0	18V
1	1	1	18V

Register	Parameter Data							
	D7	D6	D5	D4	D3	D2	D1	D0
R2Bh	x	x	x	x	x	x	x	STB (0)

STB(R2Bh[0]): Standby (Power saving) mode control

D0	STB Function
0	Standby Mode. (**default**)
1	Normal operation.

Register	Parameter Data							
	D7	D6	D5	D4	D3	D2	D1	D0
R2Fh	x	VGH_SEL (11)		CF_SEL (0)	LC_SEL (00)		SPOC (01)	

SOPC (R2Fh[1:0]): Source output driving capability selection

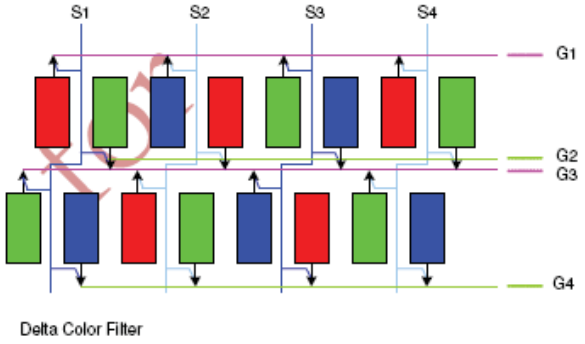
D1	D0	Source Driver Capability
0	0	-25%.
0	1	Normal. (**default**)
1	0	+25%
1	1	+50%

LC_SEL (R2Fh[3:2]): Source output driving capability selection

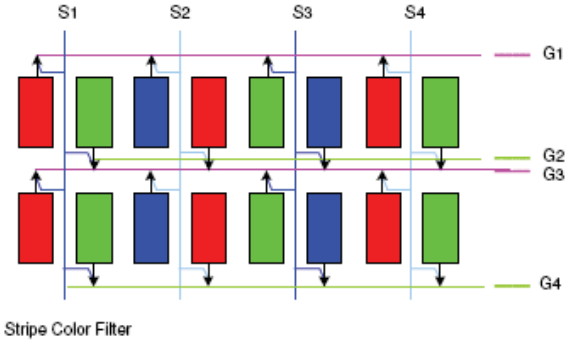
D3	D2	LC type selection
0	0	Low Voltage LC (**default**)
0	1	-
1	0	Normal Voltage LC 2
1	1	Normal Voltage LC 1

CF_SEL(R2Fh[4]): Color filter selection

D4	Function
0	Delta color filter. (**default**)
1	Stripe color filter.



Delta Color Filter



Stripe Color Filter

VGH_SEL : VGH voltage level selection

VGH_SEL			
D7	D6	D5	VGH voltage
0	0	0	13V
0	0	1	14V
0	1	0	15V
0	1	1	16V (Default)
1	0	0	17V
1	0	1	18V
1	1	0	18V
1	1	1	18V

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R30h~3Bh R6Ch~R77h：Gamma point setting

Register	Register Address								Register Data (default)							
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R30h	0	0	1	1	0	0	0	0	5GammaNP_sel	x		L00P_SEL				
									1			1	1	0	0	1
R31h	0	0	1	1	0	0	0	1	x			L02P_SEL				
												1	0	1	0	0
R32h	0	0	1	1	0	0	1	0	x			L08P_SEL				
												0	1	0	0	0
R33h	0	0	1	1	0	0	1	1	x			L16P_SEL				
												0	1	0	0	0
R34h	0	0	1	1	0	1	0	0	x			L32P_SEL				
												0	1	0	0	0
R35h	0	0	1	1	0	1	0	1	x			L50P_SEL				
												0	1	0	0	0
R36h	0	0	1	1	0	1	1	0	x			L72P_SEL				
												0	1	0	0	0
R37h	0	0	1	1	0	1	1	1	x			L96P_SEL				
												0	1	0	0	0
R38h	0	0	1	1	1	0	0	0	x			L110P_SEL				
												0	1	0	0	0
R39h	0	0	1	1	1	0	0	1	x			L120P_SEL				
												0	0	1	0	0
R3Ah	0	0	1	1	1	0	1	0	x			L125P_SEL				
												0	0	0	1	1
R3Bh	0	0	1	1	1	0	1	1	x			L127P_SEL				
												0	1	1	0	1
R6Ch	1	0	1	0	1	1	0	0	x			L00N_SEL				
												1	1	1	0	0
R6Dh	1	0	1	0	1	1	0	1	x			L02N_SEL				
												1	0	1	1	1
R6Dh	1	0	1	0	1	1	0	1	x			L02N_SEL				
												1	0	1	1	1
R6Eh	1	0	1	0	1	1	1	0	x			L08N_SEL				
												0	1	0	0	0
R6Fh	1	0	1	0	0	1	1	1	x			L16N_SEL				
												0	1	0	0	0
R70h	1	0	1	1	0	0	0	0	x			L32N_SEL				
												0	1	0	0	0
R71h	1	0	1	1	0	0	0	1	x			L50N_SEL				
												0	1	0	0	0
R72h	1	0	1	1	0	0	1	0	x			L72N_SEL				
												0	1	0	0	0
R73h	1	0	1	1	0	0	1	1	x			L96N_SEL				
												0	1	0	0	0
R74h	1	0	1	1	0	1	0	0	x			L110N_SEL				
												0	1	0	0	0
R75h	1	0	1	1	0	1	0	1	x			L120N_SEL				
												0	0	1	0	1
R76h	1	0	1	1	0	1	1	0	x			L125N_SEL				
												0	0	1	0	0
R77h	1	0	1	1	0	1	1	1	x			L127N_SEL				
												0	0	0	0	0

Note: (1)For low voltage LC △V=25mV ,For Normal voltage LC △V=40mV

R30h:

5GammaNP_sel: Gamma reference point control selection

D7	5GammaNP_sel function
0	LxN reference point control setting follow LxP
1	LxP / LxN Reference point control independently

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R55h : Inversion selection

Address								Data setting							
A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	0	1	0	1	-	INV_SEL	NBW	-	-	-	-	-
Initial setting value (Default)								-	0	0	-	-	-	-	-

NBW : Normal white/Normally black panel selection

D5	NBW function
0	Normally white panel
1	Normally black panel

INV_SEL: Inversion mode selection

D6	INV_SEL function
0	One line inversion. (Default)
1	Column inversion.

R57h : VGH/L_ENB

Address								Data setting							
A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	0	1	1	1	VGH/L_ENB	-	-	-	-	-	-	-
Initial setting value (Default)								0	-	-	-	-	-	-	-

D7	VGH/L_ENB function
0	VGH/VGL charge pump enable (Default)
1	For external VGH/VGL application

R5Ah : VGL_SEL

Address								Data setting							
A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
1	-	0	1	1	0	1	0	-	-	-	-	-	VGL_SEL		
Initial setting value (Default)								-	-	-	-	-	010		

VGL_SEL			
D2	D1	D0	VGL voltage
0	0	0	-8V
0	0	1	-9V
0	1	0	-10V(Default)
0	1	1	-11V
1	0	0	-7V
1	0	1	-7V
1	1	0	-12V
1	1	1	-12V

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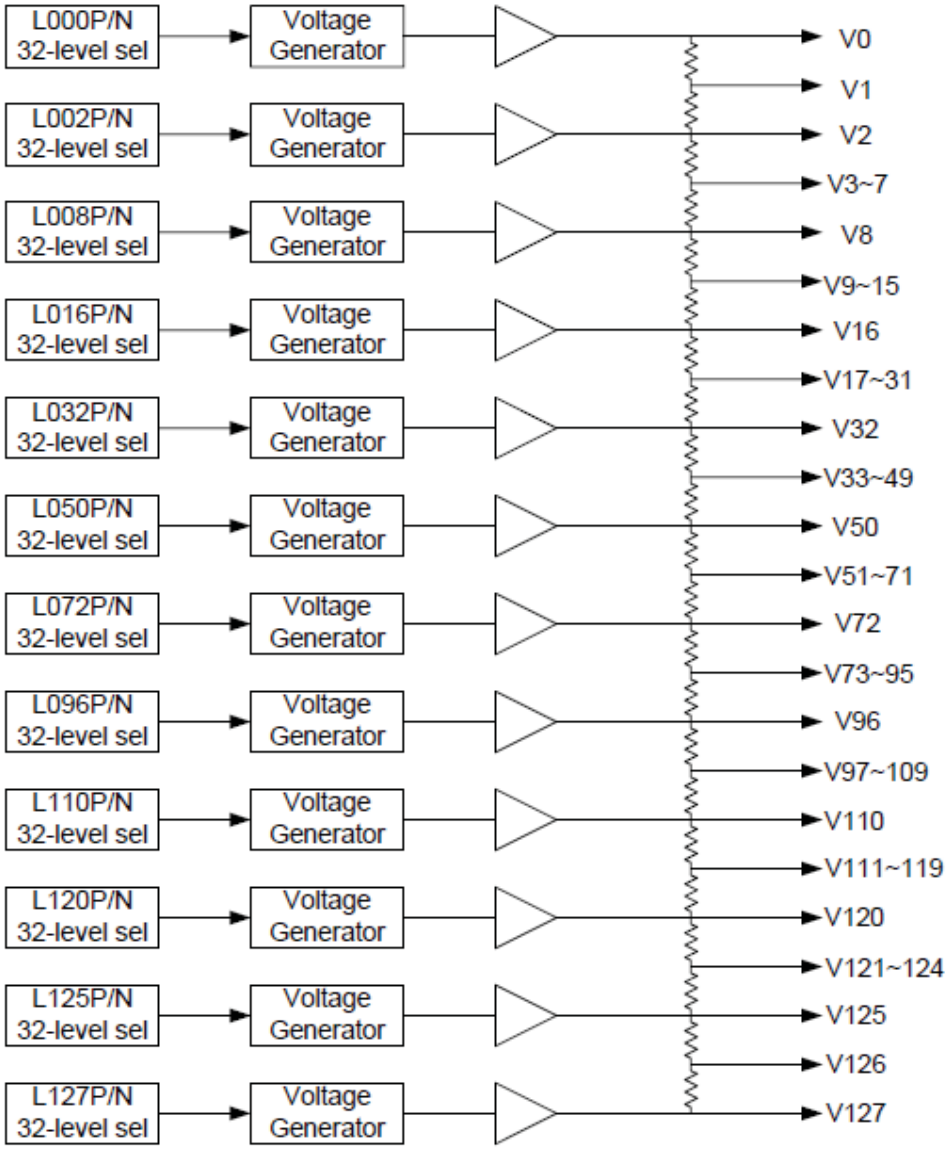
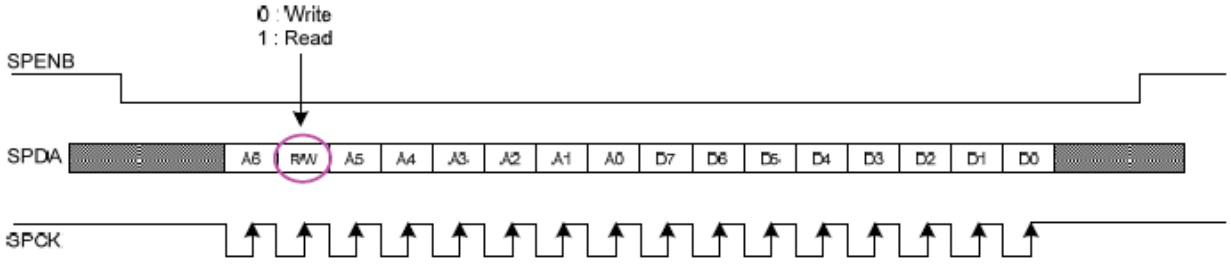
Internal gamma reference voltage generator

12 gamma correction reference point;
V0/V2/V8/V16/V32/V50/V72/V96/V110/V120/V125/127 are generated within driver IC and adjustable through serial register setting.



8.4 DATA INPUT FORMAT

SPI timing



- Each serial command consists of 16 bits of data that is loaded one bit a time at the rising edge of serial clock SPCK. Command loading operation starts from the falling edge of SPENB and is completed at the next rising edge of SPENB.
- The serial control block is operational after power on reset. If command is transferred multiple times for the same register, the last command before the VSD signal is valid.
- If less than 16 bits of SPCK are input while SPENB is low, the transferred data is ignored.
- If 16 bits or more of SPCK are input while SPENB is low, the last 16 bits of transferred data before the rising edge of SPENB pulse are valid data.
- Serial block operates with the SPCK clock
- Serial data can be accepted in the power save mode.

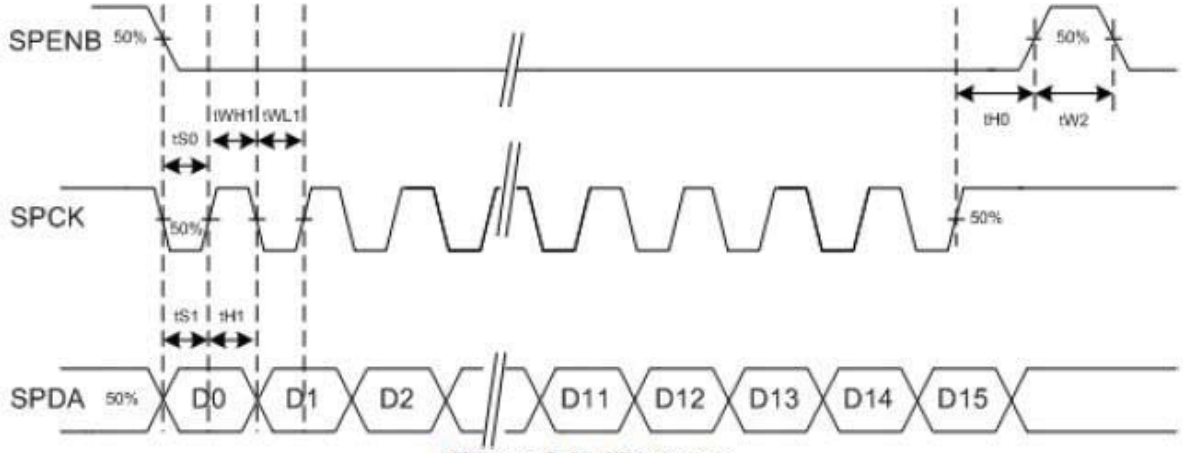


Figure 8.2: SPI timing

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
SPENB input setup time	tS0	50	-	-	ns
SPDA input setup time	tS1	50	-	-	ns
SPENB input hold time	tH0	50	-	-	ns
SPDA input hold time	tH1	50	-	-	ns
SPCK pulse high width	tWH1	50	-	-	ns
SPCK pulse low width	tWL1	50	-	-	ns
SPENB pulse high width	tW2	400	-	-	ns

Serial 8-bit RGB / 8-bit dummy RGB / YUV mode data format

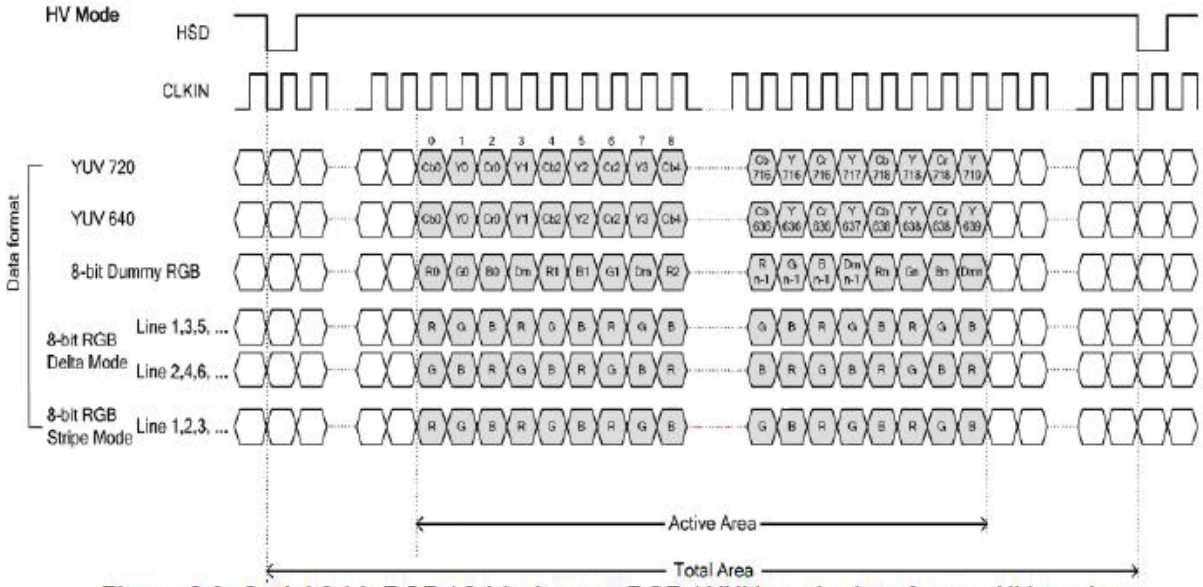
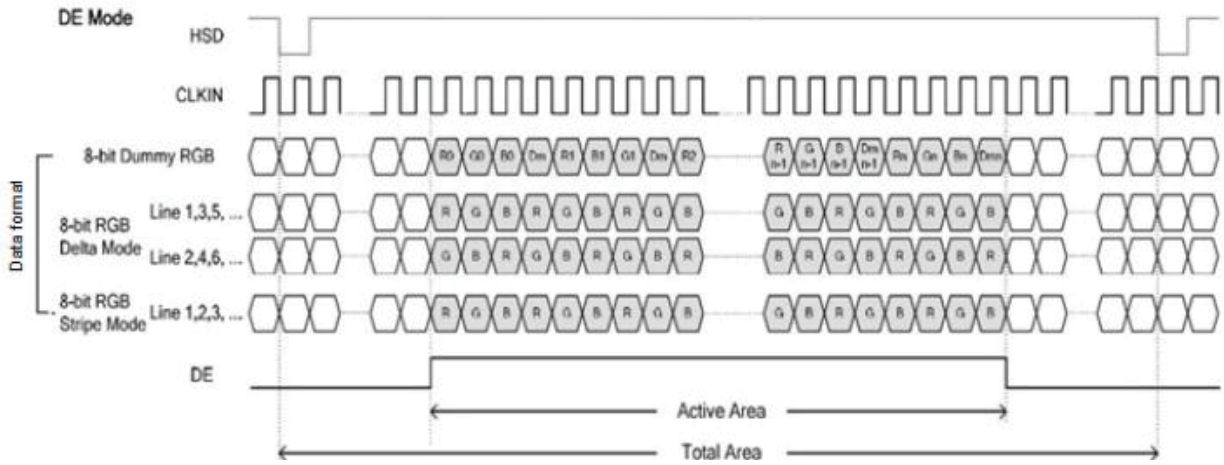
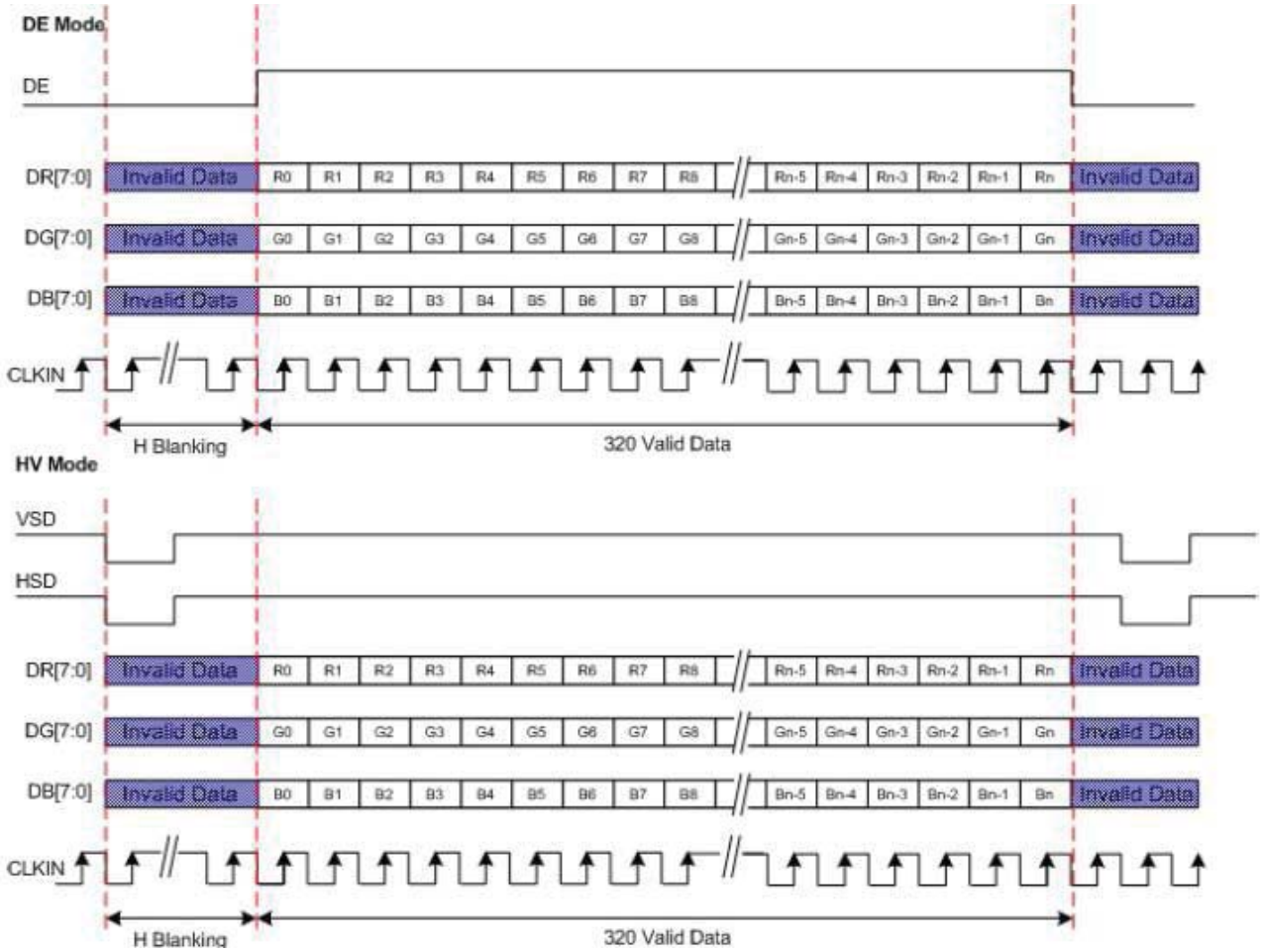


Figure 8.3: Serial 8-bit RGB / 8-bit dummy RGB / YUV mode data format HV mode



Parallel RGB mode data format



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CCIR_656 mode data format

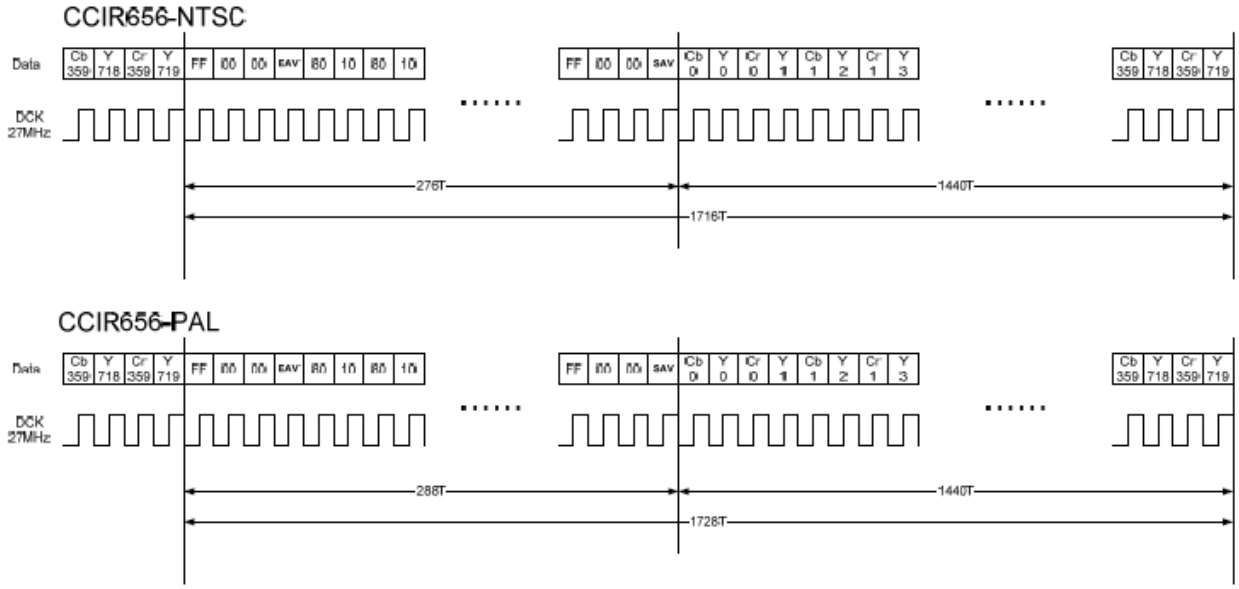

Figure 8.6: CCIR_656 mode data format

- FF 00 00 XY signals are involved with HSD , VSD and Field
- XY encode following bits : F=field select
  V=indicate vertical blanking , H=1 @ EAV , H = 0 @ SAV
  P3 ~ P0=protection bits :
  P3=V⊕H P2=F⊕H P1=F⊕V P0=F⊕V⊕H ⊕: Represents the exclusive-OR function
- Horizontal blanking section consists of repeating pattern 80 10 80 10

XY							
D7	D6	D5	D4	D3	D2	D1	D0
1	F	V	H	P3	P2	P1	P0

CCIR656/YUV640/YUV720 to RGB conversion formula

$Rn=1.164 \times [(Y_{2n-1} + Y_{2n}) / 2 - 16] + 1.596 \times (Cr_n-128)$
$Gn=1.164 \times [(Y_{2n-1} + Y_{2n}) / 2 - 16] - 0.813 \times (Cr_n-128) – 0.392 \times (Cb_n-128)$
$Bn=1.164 \times [(Y_{2n-1} + Y_{2n}) / 2 - 16] + 2.017 \times (Cb_n-128)$

Where Y: 16~235 Cr: 16~240 Cb: 16~240

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INPUT TIMING FORMAT

8-bit RGB input timing

Parameter		Symbol	Interlace			Unit
			Min.	Typ.	Max.	
CLKIN frequency		fCLKIN	13.5	27	27.19	MHz
HSD period		tH		1716	1728	CLKIN
HSD display period		tHD		960		CLKIN
HSD back porch		tHBP		70	255	CLKIN
HSD front porch		tHFP		686	718	CLKIN
HSD pulse width		tHPW	1	1	tHBP-1	CLKIN
VSD period time		tV	242.5	262.5	450.5	H
Vertical display area		tVD		240		H
VSD back porch	Odd field	tVBP	3	21	31	H
	Even field		3.5	21.5	31.5	
VSD front porch	Odd field	tVFP	1.5	1.5	179.5	H
	Even field		1	1	179	
VSD pulse width		tVSW	1 CLKIN	1CLKIN	6H	-
1 Frame		-	485	525	901	H

8-bit dummy RGB (320 mode/NTSC/24.535MHz) input timing

Parameter		Symbol	Interlace			Unit
			Min.	Typ.	Max.	
CLKIN frequency		fCLKIN	20.45	24.535	30	MHz
HSD period		tH		1560	1907	CLKIN
HSD display period		tHD		1280		CLKIN
HSD back porch		tHBP		241	255	CLKIN
HSD front porch		tHFP		39	372	CLKIN
HSD pulse width		tHPW	1	1	200	CLKIN
VSD period time		tV	242.5	262.5	450.5	H
Vertical display area		tVD		240		H
VSD back porch	Odd field	tVBP	3	21	31	H
	Even field		3.5	21.5	31.5	
VSD front porch	Odd field	tVFP	1.5	1.5	179.5	H
	Even field		1	1	179	
VSD pulse width		tVSW	1	1	200	CLKIN
1 Frame		-	485	525	901	H

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8-bit dummy RGB (320 mode/PAL/24.375MHz) input timing

Parameter		Symbol	Interlace			Unit
			Min.	Typ.	Max.	
CLKIN frequency		fCLKIN	20.45	24.375	30	MHz
HSD period		tH		1560	1920	CLKIN
HSD display period		tHD		1280		CLKIN
HSD back porch		tHBP		241	255	CLKIN
HSD front porch		tHFP		39	385	CLKIN
HSD pulse width		tHPW	1	1	200	CLKIN
VSD period time		tV	292.5	312.5	450.5	H
Vertical display area		tVD		288		H
VSD back porch	Odd field	tVBP	3	23	34	H
	Even field		3.5	23.5	34.5	
VSD front porch	Odd field	tVFP	1.5	1.5	128.5	H
	Even field		1	1	128	
VSD pulse width		tVSW	1	1	200	CLKIN
1 Frame		-	585	625	901	H

8-bit dummy RGB (360 mode/NTSC/27MHz) input timing

Parameter		Symbol	Interlace			Unit
			Min.	Typ.	Max.	
CLKIN frequency		fCLKIN	23	27	30	MHz
HSD period		tH		1716	1907	CLKIN
HSD display period		tHD		1440		CLKIN
HSD back porch		tHBP		241	255	CLKIN
HSD front porch		tHFP		35	212	CLKIN
HSD pulse width		tHPW	1	1	200	CLKIN
VSD period time		tV	242.5	262.5	450.5	H
Vertical display area		tVD		240		H
VSD back porch	Odd field	tVBP	3	21	31	H
	Even field		3.5	21.5	31.5	
VSD front porch	Odd field	tVFP	1.5	1.5	179.5	H
	Even field		1	1	179	
VSD pulse width		tVSW	1	1	200	CLKIN
1 Frame		-	485	525	901	H

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8-bit dummy RGB (360 mode/PAL/27MHz) input timing

Parameter		Symbol	Interlace			Unit
			Min.	Typ.	Max.	
CLKIN frequency		fCLKIN	23	27	30	MHz
HSD period		tH		1728	1920	CLKIN
HSD display period		tHD		1440		CLKIN
HSD back porch		tHBP		241	255	CLKIN
HSD front porch		tHFP		47	225	CLKIN
HSD pulse width		tHPW	1	1	200	CLKIN
VSD period time		tV	292.5	312.5	450.5	H
Vertical display area		tVD		288		H
VSD back porch	Odd field	tVBP	3	23	34	H
	Even field		3.5	23.5	34.5	
VSD front porch	Odd field	tVFP	1.5	1.5	128.5	H
	Even field		1	1	128	
VSD pulse width		tVSW	1	1	200	CLKIN
1 Frame		-	585	625	901	H

YUV720 mode/NTSC input timing

Parameter		Symbol	Interlace			Unit
			Min.	Typ.	Max.	
CLKIN frequency		fCLKIN	-	27	-	MHz
HSD period		tH	-	1716	-	CLKIN
HSD display period		tHD		1440		CLKIN
HSD back porch		tHBP	-	240	-	CLKIN
HSD front porch		tHFP	-	36	-	CLKIN
HSD pulse width		tHPW	-	1	-	CLKIN
VSD period time		tV	-	262.5	-	H
Vertical display area		tVD		240		H
VSD back porch	Odd field	tVBP	-	21	-	H
	Even field		-	21.5	-	
VSD front porch	Odd field	tVFP	-	1.5	-	H
	Even field		-	1	-	
VSD pulse width		tVSW	-	1	1	CLKIN
1 Frame		-	-	525	-	H

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YUV720 mode/PAL input timing

Parameter		Symbol	Interlace			Unit
			Min.	Typ.	Max.	
CLKIN frequency		fCLKIN	-	27	-	MHz
HSD period		tH	-	1728	-	CLKIN
HSD display period		tHD		1440		CLKIN
HSD back porch		tHBP	-	240	-	CLKIN
HSD front porch		tHFP	-	48	-	CLKIN
HSD pulse width		tHPW	-	1	-	CLKIN
VSD period time		tV	-	312.5	-	H
Vertical display area		tVD		288		H
VSD back porch	Odd field	tVBP	-	24	-	H
	Even field		-	24.5	-	
VSD front porch	Odd field	tVFP	-	0.5	-	H
	Even field		-	0	-	
VSD pulse width		tVSW	-	1	-	CLKIN
1 Frame		-	-	625	-	H

YUV640 mode/NTSC input timing

Parameter		Symbol	Interlace			Unit
			Min.	Typ.	Max.	
CLKIN frequency		fCLKIN	-	24.535	-	MHz
HSD period		tH	-	1560	-	CLKIN
HSD display period		tHD		1280		CLKIN
HSD back porch		tHBP	-	240	-	CLKIN
HSD front porch		tHFP	-	40	-	CLKIN
HSD pulse width		tHPW	-	1	-	CLKIN
VSD period time		tV	-	262.5	-	H
Vertical display area		tVD		240		H
VSD back porch	Odd field	tVBP	-	21	-	H
	Even field		-	21.5	-	
VSD front porch	Odd field	tVFP	-	1.5	-	H
	Even field		-	1	-	
VSD pulse width		tVSW	-	1	-	CLKIN
1 Frame		-	-	525	-	H

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YUV640 mode/PAL input timing

Parameter		Symbol	Interlace			Unit
			Min.	Typ.	Max.	
CLKIN frequency		fCLKIN	-	24.375	-	MHz
HSD period		tH	-	1560	-	CLKIN
HSD display period		tHD		1280		CLKIN
HSD back porch		tHBP	-	240	-	CLKIN
HSD front porch		tHFP	-	40	-	CLKIN
HSD pulse width		tHPW	-	1	-	CLKIN
VSD period time		tV	-	312.5	-	H
Vertical display area		tVD		288		H
VSD back porch	Odd field	tVBP	-	24	-	H
	Even field		-	24.5	-	
VSD front porch	Odd field	tVFP	-	0.5	-	H
	Even field		-	0	-	
VSD pulse width		tVSW	-	1	-	CLKIN
1 Frame		-	-	625	-	H

Parallel RGB input timing

Parameter		Symbol	Interlace			Unit
			Min.	Typ.	Max.	
CLKIN frequency		fCLKIN	-	6.14	-	MHz
HSD period		tH	-	390	-	CLKIN
HSD display period		tHD		320		CLKIN
HSD back porch		tHBP	40	61	-	CLKIN
HSD front porch		tHFP	-	9	-	CLKIN
HSD pulse width		tHPW	-	1	-	CLKIN
VSD period time		tV	-	262.5	-	H
Vertical display area		tVD		240		H
VSD back porch	Odd field	tVBP	-	21	-	H
	Even field		-	21.5	-	
VSD front porch	Odd field	tVFP	-	1.5	-	H
	Even field		-	1	-	
VSD pulse width		tVSW	-	1	-	CLKIN
1 Frame		-	-	525	-	H

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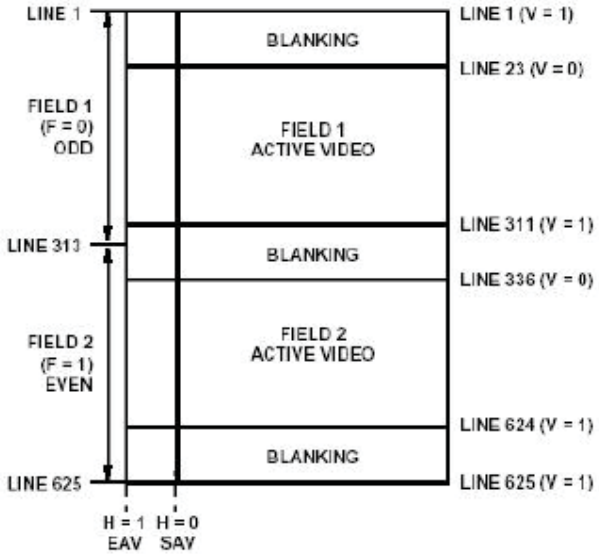
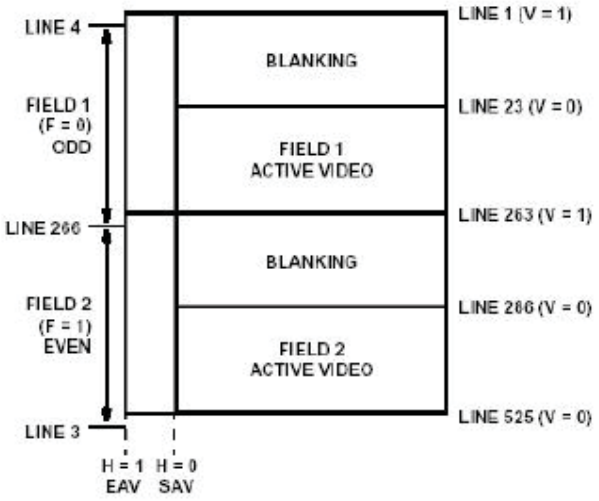
CCIR656 vertical input timing

PAL mode



LINE NUMBER	F	V	H (EAV)	H (SAV)
1-22	0	1	1	0
23-310	0	0	1	0
311-312	0	1	1	0
313-335	1	1	1	0
336-623	1	0	1	0
624-625	1	1	1	0

NTSC mode



LINE NUMBER	F	V	H (EAV)	H (SAV)
1-3	1	1	1	0
4-22	0	1	1	0
23-262	0	0	1	0
263-265	0	1	1	0
266-285	1	1	1	0
286-525	1	0	1	0

	F	H	V
1	EVEN Field	EAV	BLANKING
0	Odd Field	SAV	ACTIVE VIDEO

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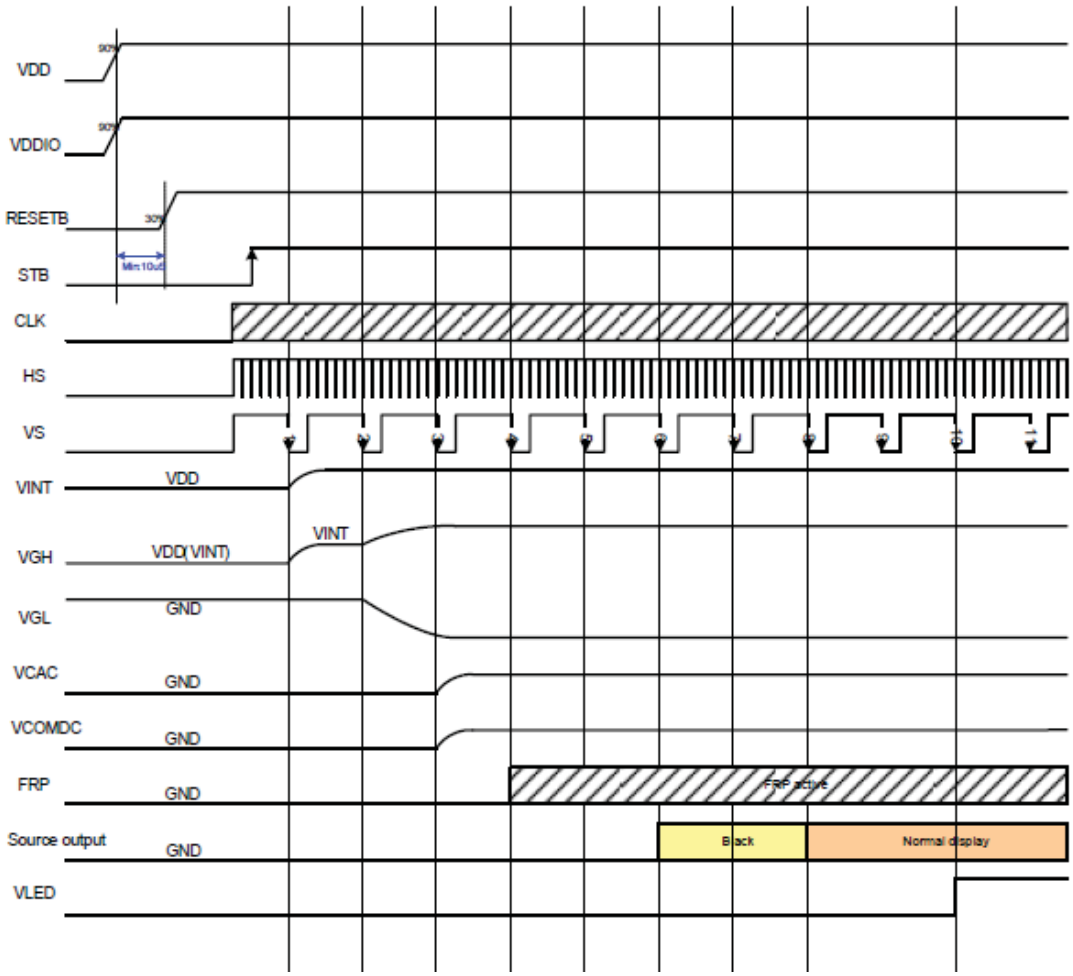
8.5 AC ELECTRICAL CHARACTERISTICS

(VDD=3.0~3.6V,VDDIO=AVDD=VDD,BGND=AGND=0V, TA=25℃)

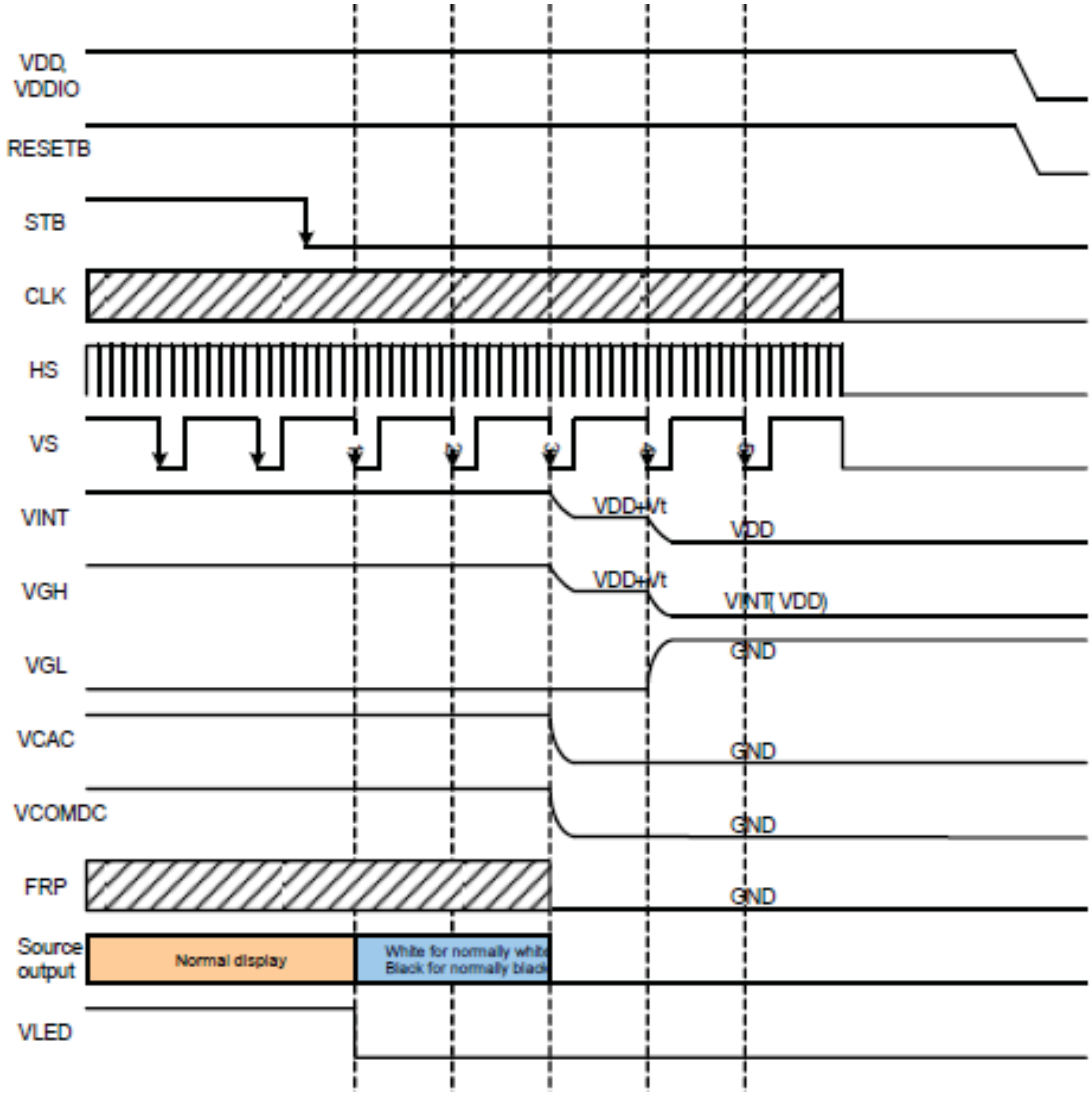
Parameter	Symbol	Spec.			Unit	Condition
		Min.	Typ.	Max.		
HSD period time	Th	60			us	-
HSD setup time	Thst	9	-	-	ns	-
HSD hold time	Thhd	9	-	-	ns	-
VSD setup time	Tvst	9	-	-	ns	-
VSD hold time	Tvhd	9	-	-	ns	-
DEN setup time	Tdest	9	-	-	ns	-
DEN hold time	Tdehd	9	-	-	ns	-
Data setup time	Tdsu	9	-	-	ns	-
Data hold time	Tdhd	9	-	-	ns	-
Source output settling time	TST	-	-	8	us	R=5Kohm , C=30pF
Gate output settling time	Tgst	-	0.5	1	us	R=3Kohm , C=25pF
VCOM setting time	TST,vcom	-	-	9	us	R=200ohm , C=5nF

8.6 Power ON/OFF Sequence

8.6.1 POWER ON SEQUENCE



8.6.2 POWER OFF SEQUENCE



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9. Optical Specification

Ta=25℃

Item		Symbol	Condition	Min	Typ.	Max.	Unit	Remark
Contrast Ratio		CR	θ=0°	200	300	-		Note1 Note2
Response Time		Ton/ Toff	25℃	-	25	45	ms	Note1 Note3
View Angles		ΘT	CR≧10	-	50	-	Degree	Note 4
		ΘB		-	60	-		
		ΘL		-	60	-		
		θR		-	60	-		
Chromaticity	White	x	Brightness is on	(0.256)	(0.306)	(0.356)		Note5, Note1
		y		(0.276)	(0.326)	(0.376)		
	Red	x		(0.520)	(0.570)	(0.620)		
		y		(0.290)	(0.340)	(0.390)		
	Green	x		(0.297)	(0.347)	(0.397)		
		y		(0.479)	(0.529)	(0.579)		
	Blue	x		(0.101)	(0.151)	(0.201)		
		y		(0.057)	(0.107)	(0.157)		
NTSC		S			45		%	Note5
Luminance		L		320	370	-	cd/m^2	Note1 Note6
Uniformity		U		75	80	-	%	Note1 Note7

Test condition: V_F=3.2V ,I_F=20mA(LED current), the ambient temperature is 25℃.

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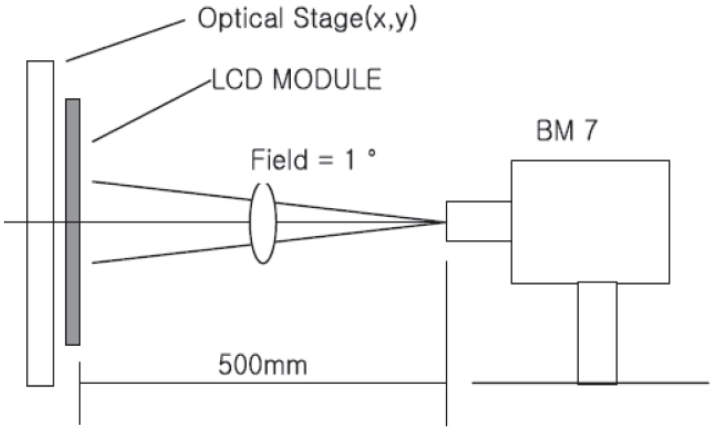
Note 1: Definition of optical measurement system.

Temperature = 25℃(±3℃)

LED back-light: ON, Environment brightness < 150 lx

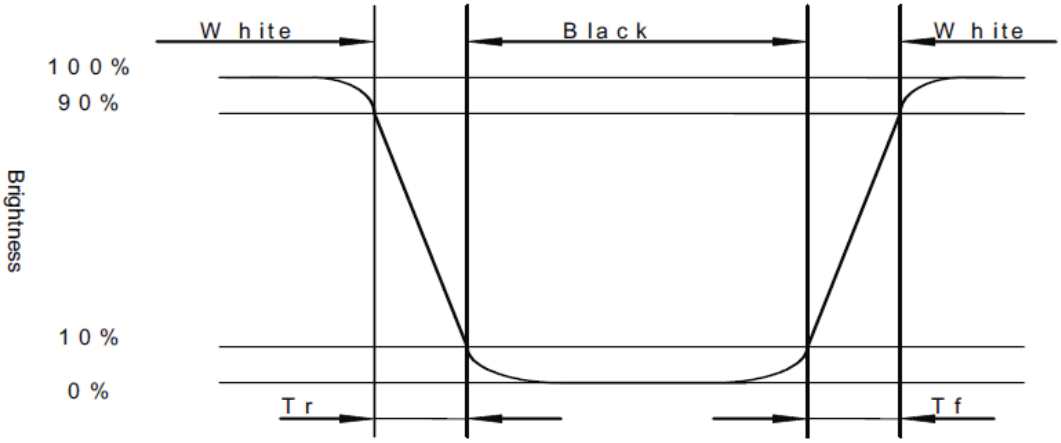


Note 2: Contrast ratio is defined as follow:

$$\text{Contrast Ratio} = \frac{\text{Surface Luminance with all white pixels}}{\text{Surface Luminance with all black pixels}}$$

Note 3: Response time is defined as follow:

Response time is the time required for the display to transition from black to white (Rise Time, Tr) and from white to black(Decay Time, Tf).



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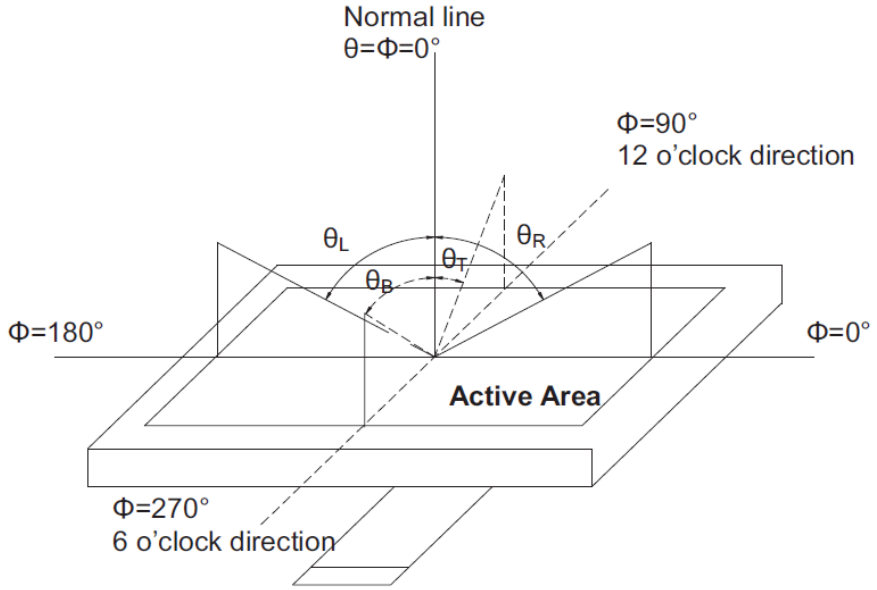
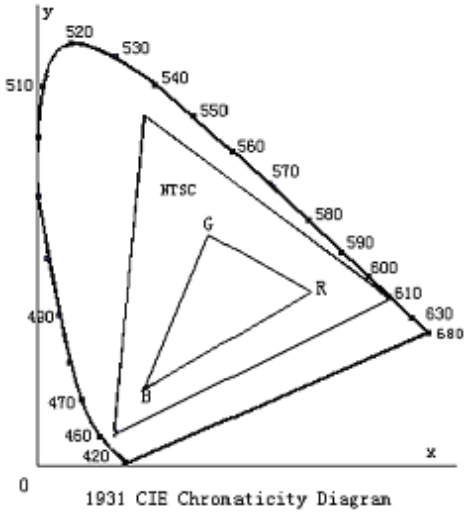
Note 4: Viewing angle range is defined as follow:

Viewing angle is measured at the center point of the LCD.



Note 5: Color chromaticity is defined as follow: (CIE1931)

Color coordinates measured at center point of LCD.



$$S = \frac{\text{area of RGB triangle}}{\text{area of NTSC triangle}} \times 100\%$$

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Note 6: Luminance is defined as follow:

Luminance is defined as the brightness of all pixels “White” at the center of display area on optimum contrast.

Note 7: Luminance Uniformity is defined as follow:

Active area is divided into 9 measuring areas (Refer Fig. 2). Every measuring point is placed at the center of each measuring area.

$$\text{Uniformity(U)} = \frac{\text{Minimum Luminance(brightness) in 9 points}}{\text{Maximum Luminance(brightness) in 9 points}}$$

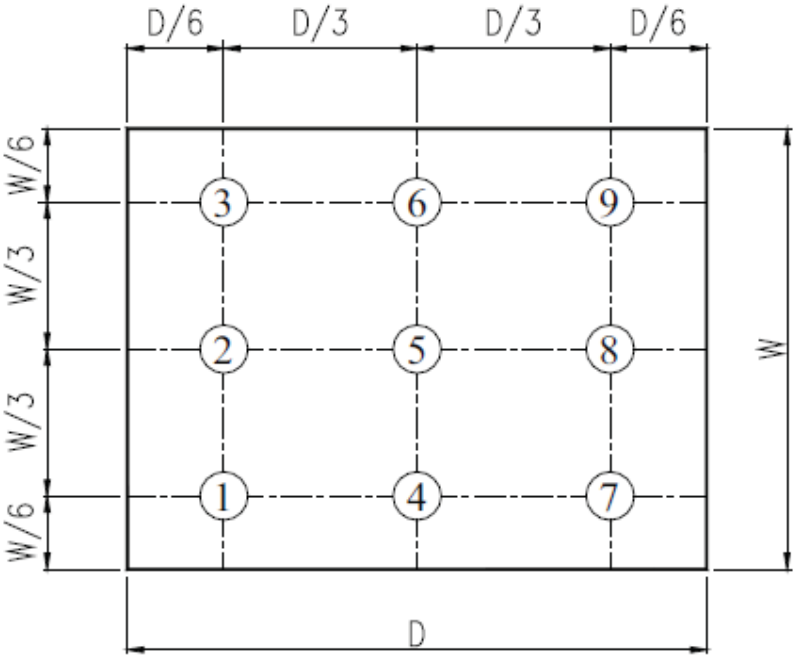

Fig. 2 Definition of uniformity

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10. Environmental / Reliability Tests

No	Test Item	Condition	Judgment criteria
1	High Temp Operation	Ts=+60℃, 120hrs	Per table in below
2	Low Temp Operation	Ta=0℃, 120hrs	Per table in below
3	High Temp Storage	Ta=+70℃, 120hrs	Per table in below
4	Low Temp Storage	Ta=-30℃, 120hrs	Per table in below
5	High Temp & High Humidity Storage	Ta=+60℃, 90% RH 120 hours	Per table in below (polarizer discoloration is excluded)
6	Thermal Shock (Non-operation)	-30℃ 30 min~+70℃ 30 min, Change time:5min, 10 Cycles	Per table in below
7	ESD (Operation)	C=150pF, R=330Ω，5points/panel Air:±8KV, 5times; Contact:±4KV, 5 times;	Per table in below
8	Vibration (Non-operation)	Frequency range:10~55Hz, Stroke:1.5mm Sweep:10Hz~55Hz~10Hz 2 hours for each direction of X.Y.Z.	Per table in below
9	Shock (Non-operation)	60G 6ms, ±X,±Y,±Z 3times, for each direction	Per table in below
10	Package Drop Test	Height:80 cm, 1 corner, 3 edges, 6 surfaces	Per table in below

INSPECTION	CRITERION(after test)
Appearance	No Crack on the FPC, on the LCD Panel
Alignment of LCD Panel	No Bubbles in the LCD Panel No other Defects of Alignment in Active area
Electrical current	Within device specifications
Function / Display	No Broken Circuit, No Short Circuit or No Black line No Other Defects of Display

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11. Precautions for Use of LCD Modules

11.1 Safety

The liquid crystal in the LCD is poisonous. Do not put it in your mouth. If the liquid crystal touches your skin or clothes, wash it off immediately using soap and water.

11.2 Handling

A. The LCD and touch panel is made of plate glass. Do not subject the panel to mechanical shock or to excessive force on its surface.
B. Do not handle the product by holding the flexible pattern portion in order to assure the reliability
C. Transparency is an important factor for the touch panel. Please wear clear finger sacks, gloves and mask to protect the touch panel from finger print or stain and also hold the portion outside the view area when handling the touch panel.
D. Provide a space so that the panel does not come into contact with other components.
E. To protect the product from external force, put a covering lens (acrylic board or similar board) and keep an appropriate gap between them.
F. Transparent electrodes may be disconnected if the panel is used under environmental conditions where dew condensation occurs.
G. Property of semiconductor devices may be affected when they are exposed to light, possibly resulting in IC malfunctions.
H. To prevent such IC malfunctions, your design and mounting layout shall be done in the way that the IC is not exposed to light in actual use.

11.3 Static Electricity

A. Ground soldering iron tips, tools and testers when they are in operation.
B. Ground your body when handling the products.
C. Power on the LCD module before applying the voltage to the input terminals.
D. Do not apply voltage which exceeds the absolute maximum rating.
E. Store the products in an anti-electrostatic bag or container.

11.4Storage

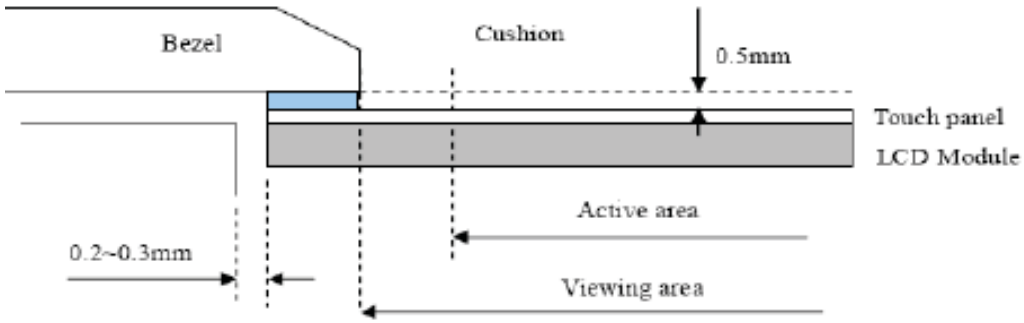
A. Store the products in a dark place at +25℃±10℃ with low humidity (40% RH to 60% RH). Don't expose to sunlight or fluorescent light.
B. Storage in a clean environment, free from dust, active gas, and solvent.

11.5 Cleaning

A. Do not wipe the touch panel with dry cloth, as it may cause scratch.
B. Wipe off the stain on the product by using soft cloth moistened with ethanol. Do not allow ethanol to get in between the upper film and the bottom glass. It may cause peeling issue or defective operation. Do not use any organic solvent or detergent other than ethanol.

11.6 Cautions for installing and assembling

Bezel edge must be positioned in the area between the Active area and View area. The bezel may press the touch screen and cause activation if the edge touches the active area. A gap of approximately 0.5mm is needed between the bezel and the top electrode. It may cause unexpected activation if the gap is too narrow. There is a tolerance of 0.2 to 0.3mm for the outside dimensions of the touch panel and tail. A gap must be made to absorb the tolerance in the case and connector.



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