OPENCALC PA1

Title	OPENCALC OC1 TITLE		
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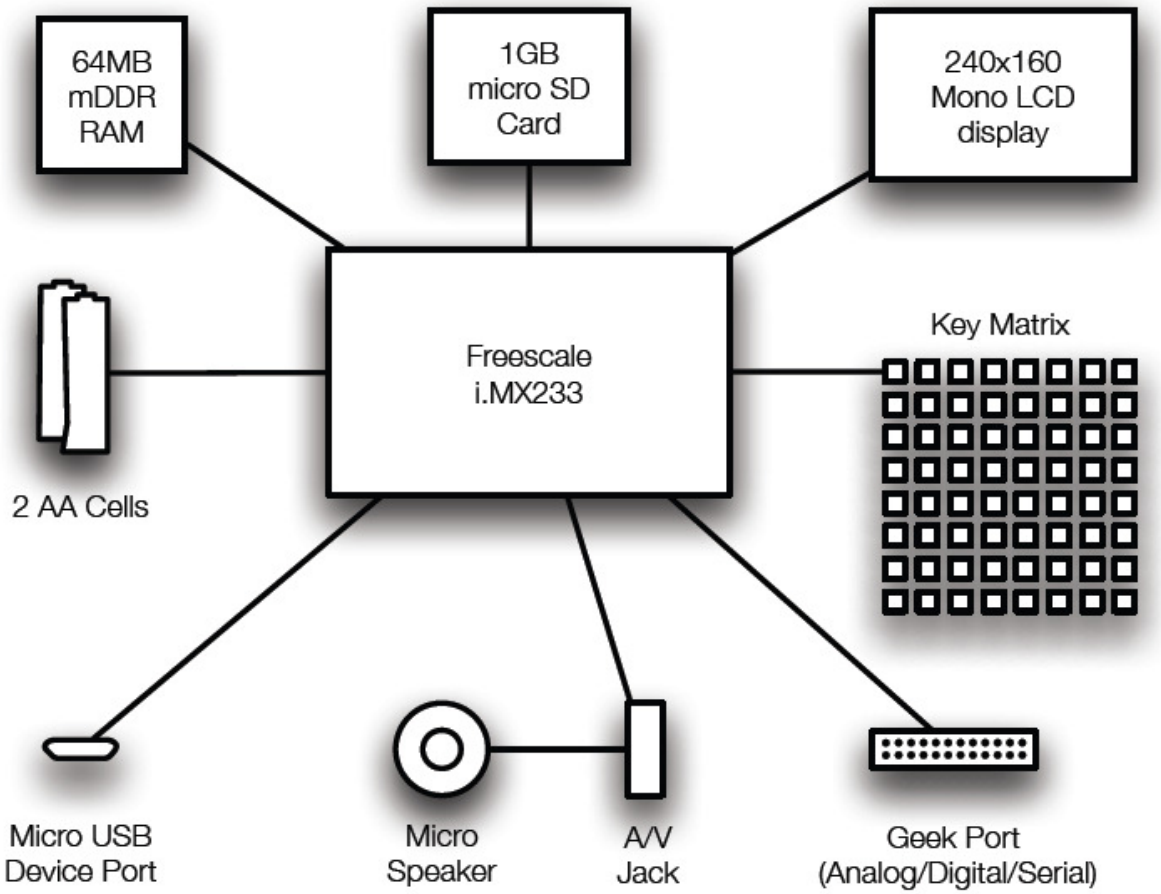

OPENCALC BLOCK DIAGRAM

Title: OPENCALC OC1 BLOCK DIAGRAM		
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Questions

Should DQS have pulldowns on board?

Q. In USB-only power mode is it possible to enumerate at 100mA VBUS current consumption?
A. Our team believes this is possible, but is not supported by default in the BSP today. Using mobile DDR would be recommended to achieve this reliably.

Q. PSWITCH recovery vs. regular USB mode: Is there any difference between the USB boot mode (selected by the boot mode pins) and the recovery mode (selected by the PSWITCH) mode? Is this simply 2 ways of entering the same USB mode?
A. Yes, these are equivalent. PSWITCH is is just the manual entry into USB recovery mode. You can also enter USB recovery mode if there is a non-recoverable boot time error. Of course the bootmode switches can land you here as well.

Q. What's the fundamental difference between the application UART and the debug UART? Does the debug UART have any special function in the various boot modes? Or is it simply a difference in speed it's capable of?
A. The debug UART is limited to 115.2Kbps with no flow control pins available in either package. The application UART's are capable of 3.25Mbps with one UART having flow control pins available in the 169 pin BGA, though not in the QFP.

Q. Does the DC-DC only run off of 4.2V? that is: can we connect 5V to the 4.2V supply directly and avoid loosing the 0.8V drop in efficiency? ABS MAX ratings show VDD4P2V maximum at 4.242. Is that a hard requirement?
A. When using a 5V supply the 4P2 regulator is a hard requirement. Again AN3989 can shed a little light on the situation.

Q. Have customers successfully implemented the MX233 in QFP on 4 layer boards and met EMI? Seems like it may be a bit of a challenge.
A. Per AN3883 it can be done but ESD performance will be comprimised. See the attached copy. I will also ask the factory to see if they can provide any more information.

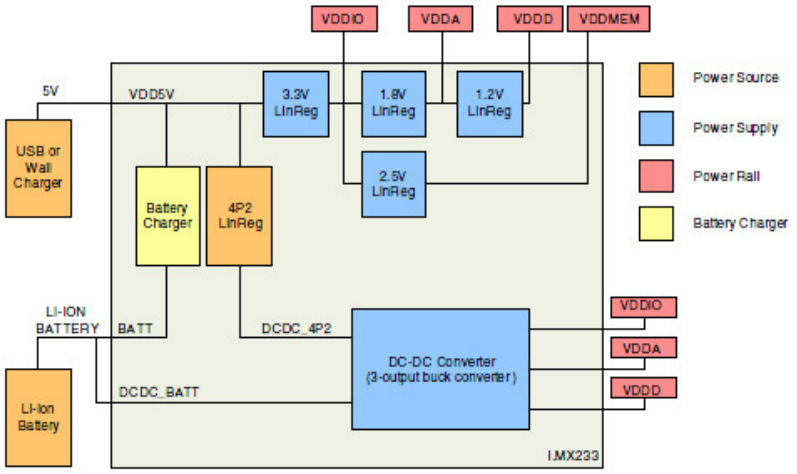

Figure 1. Logical Diagram of i.MX233 PMU

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Changelist

6/25/2011: Initial Revision

TODO

put protection on the SD port

put detection on the headset port.

MX233 Port Usage

* I2C/AUART1 -> GEEK PORT
* AUART2 (ALL 4 PINS) -> RESERVED FOR BLUETOOTH
* EMI -> mDDR
* SSP1 -> uSD card
* LCD -> LCD
* SAIF -> GEEK PORT gpio pins

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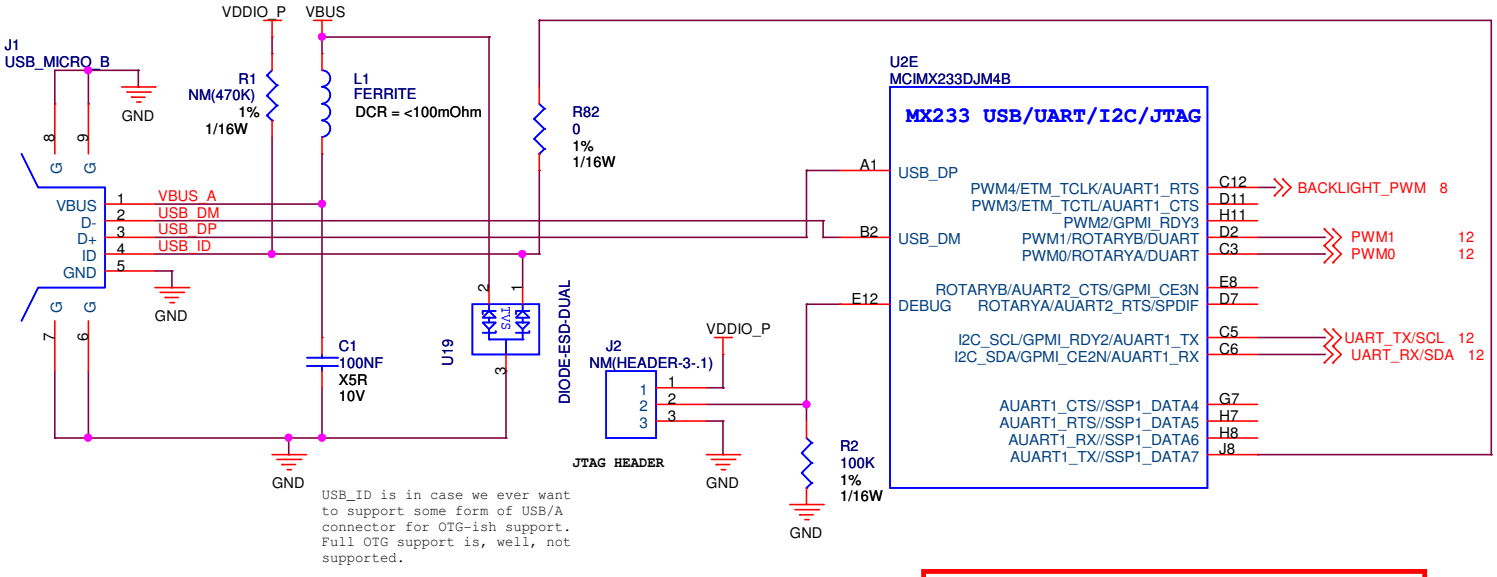
USB/CRYSTAL/JTAG

Layout Note: Low impedance Vias to GND! for ESD

Ferrites, CMC and ESD diode examples from murata applications guide, and intel guide in 'docs' directory.



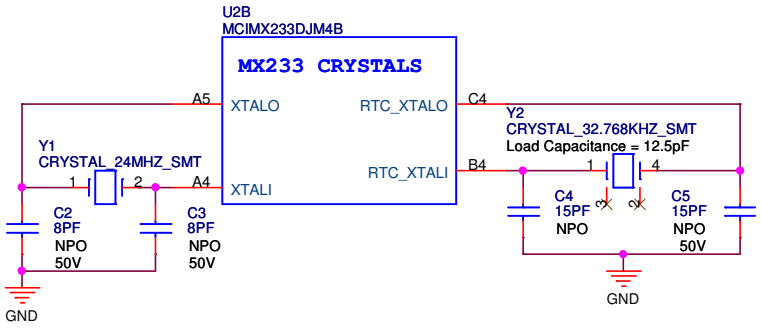
USB_ID is in case we ever want to support some form of USB/A connector for OTG-ish support. Full OTG support is, well, not supported.

Crystal Design Notes:
The 24 MHz crystal should be located close to the mx25.

Cload = [(C1*C2)/(C1+C2)]+Cstray

Cstray =~ 4-6pF

Set C1 == C2:
Cload = (C1^2/2C1)+CStray
Cload = C1/2 + CStray
C1 = 2 * (Cload - CStray)
C1 = C2 = 2 * (8pF - 4pF) = 8pF



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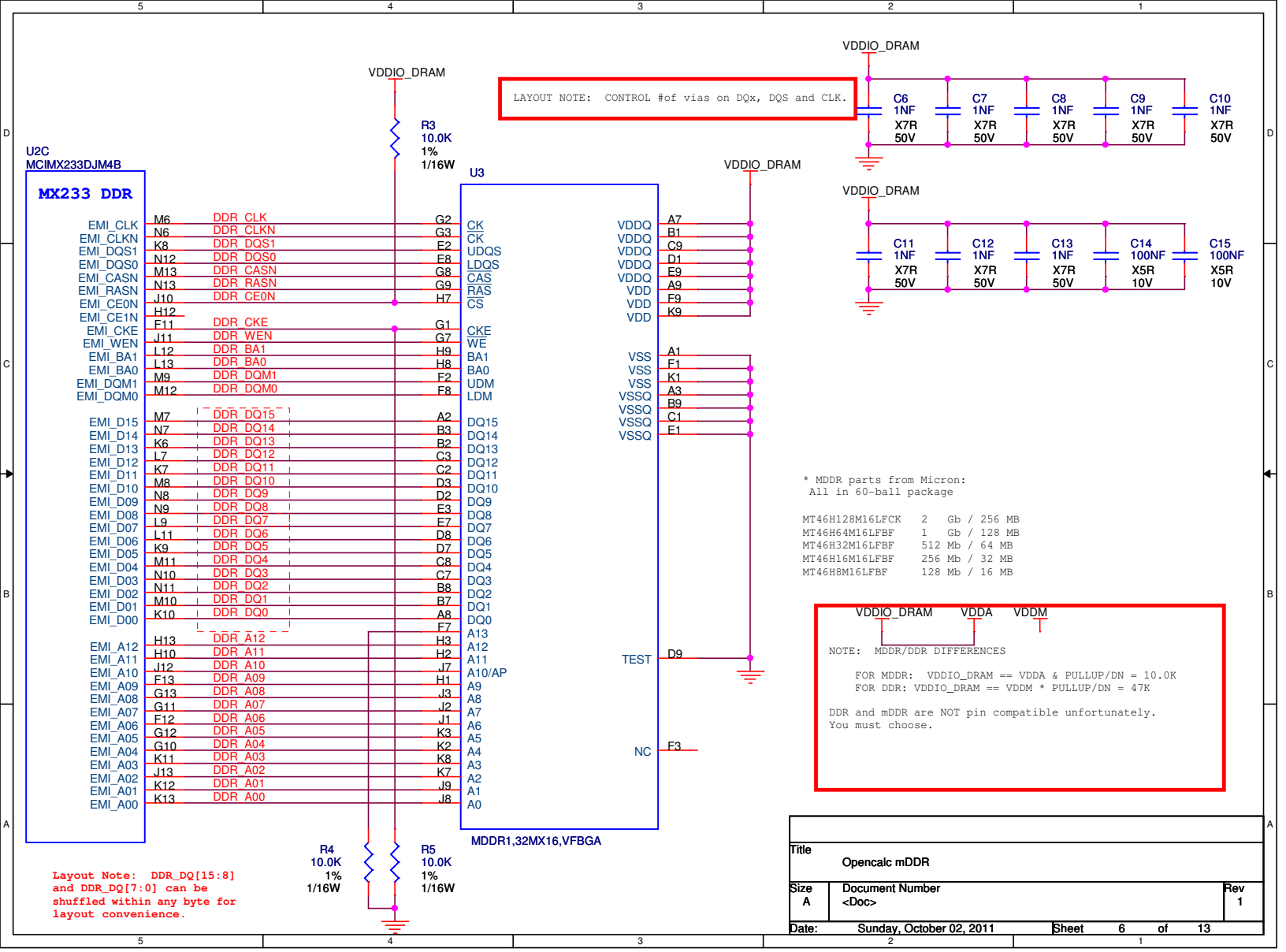
VDDIO_DRAM
R3
10.0K
1%
1/16W
LAYOUT NOTE: CONTROL #of vias on DQx, DQS and CLK.
C6 1NF X7R 50V
C7 1NF X7R 50V
C8 1NF X7R 50V
C9 1NF X7R 50V
C10 1NF X7R 50V
C11 1NF X7R 50V
C12 1NF X7R 50V
C13 1NF X7R 50V
C14 100NF X5R 10V
C15 100NF X5R 10V
U2C
MCIMX233DJM4B
MX233 DDR
U3
MDDR1,32MX16,VFBGA
R4 10.0K 1% 1/16W
R5 10.0K 1% 1/16W
* MDDR parts from Micron:
All in 60-ball package
MT46H128M16LFCK 2 Gb / 256 MB
MT46H64M16LFBF 1 Gb / 128 MB
MT46H32M16LFBF 512 Mb / 64 MB
MT46H16M16LFBF 256 Mb / 32 MB
MT46H8M16LFBF 128 Mb / 16 MB
VDDIO_DRAM VDDA VDDM
NOTE: MDDR/DDR DIFFERENCES
FOR MDDR: VDDIO_DRAM == VDDA & PULLUP/DN = 10.0K
FOR DDR: VDDIO_DRAM == VDDM * PULLUP/DN = 47K
DDR and mDDR are NOT pin compatible unfortunately.
You must choose.
Layout Note: DDR_DQ[15:8] and DDR_DQ[7:0] can be shuffled within any byte for layout convenience.
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Opencalc mDDR
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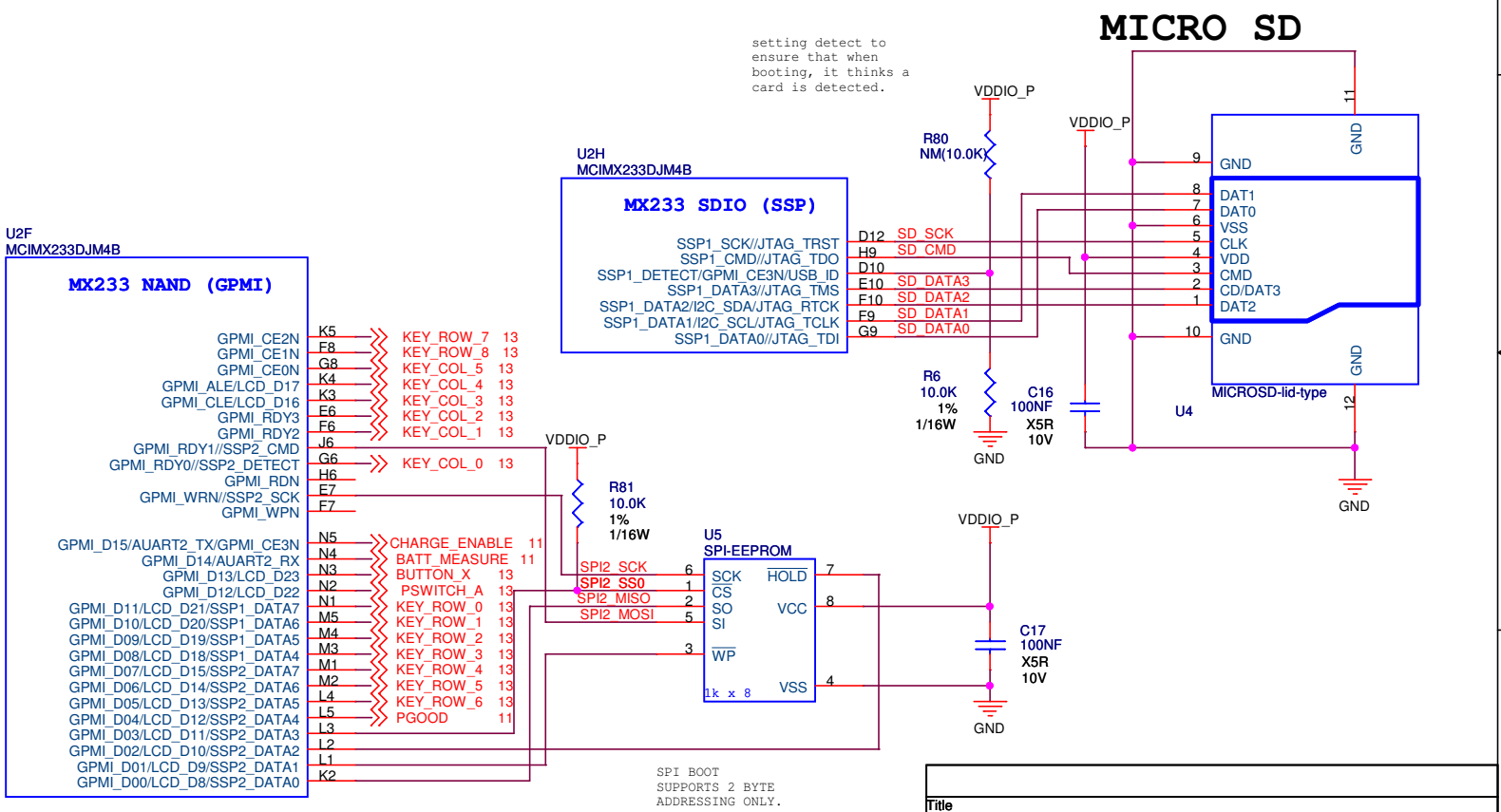
FLASH



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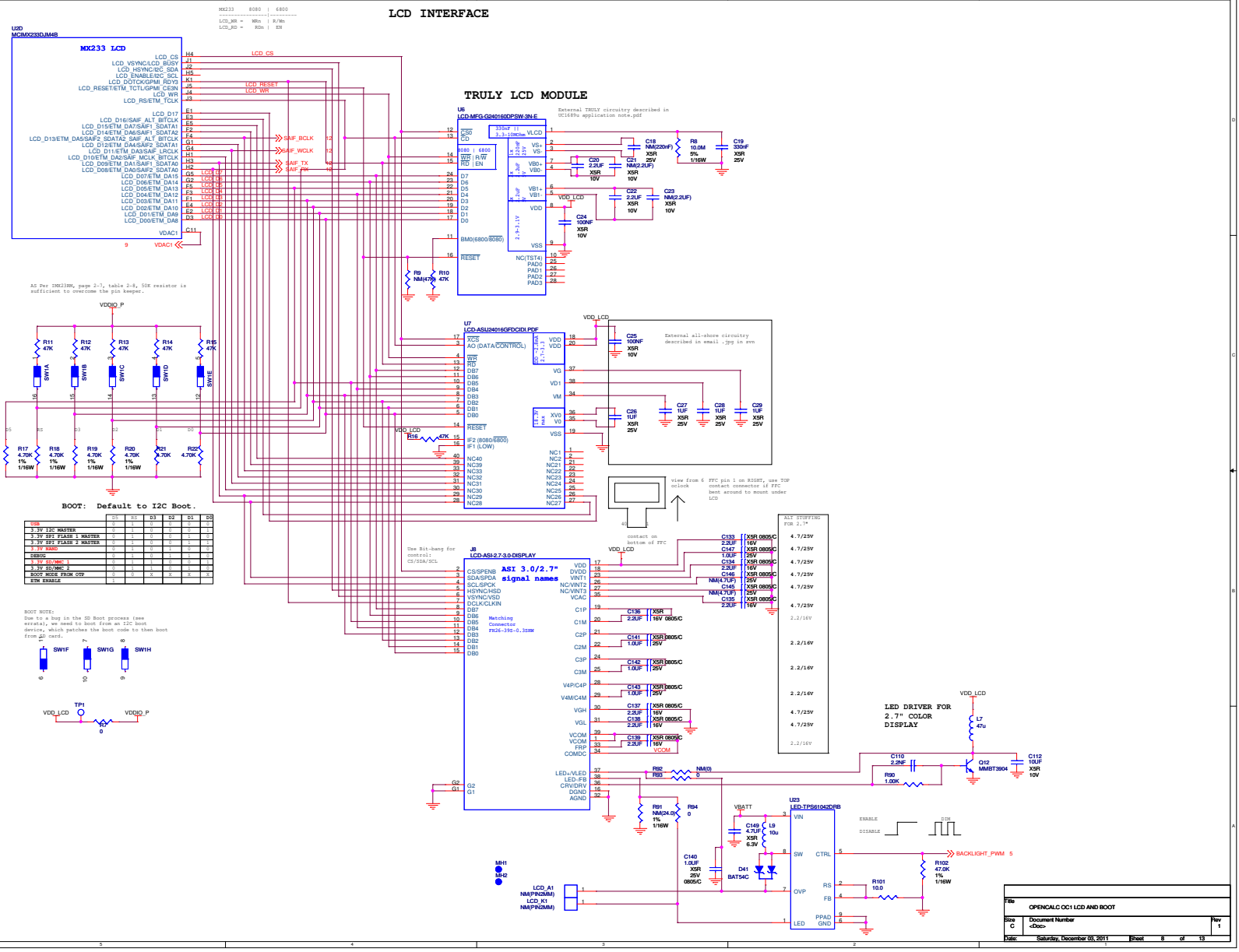
LCD INTERFACE



Title			
	OPENCALC OC1 LCD AND BOOT		
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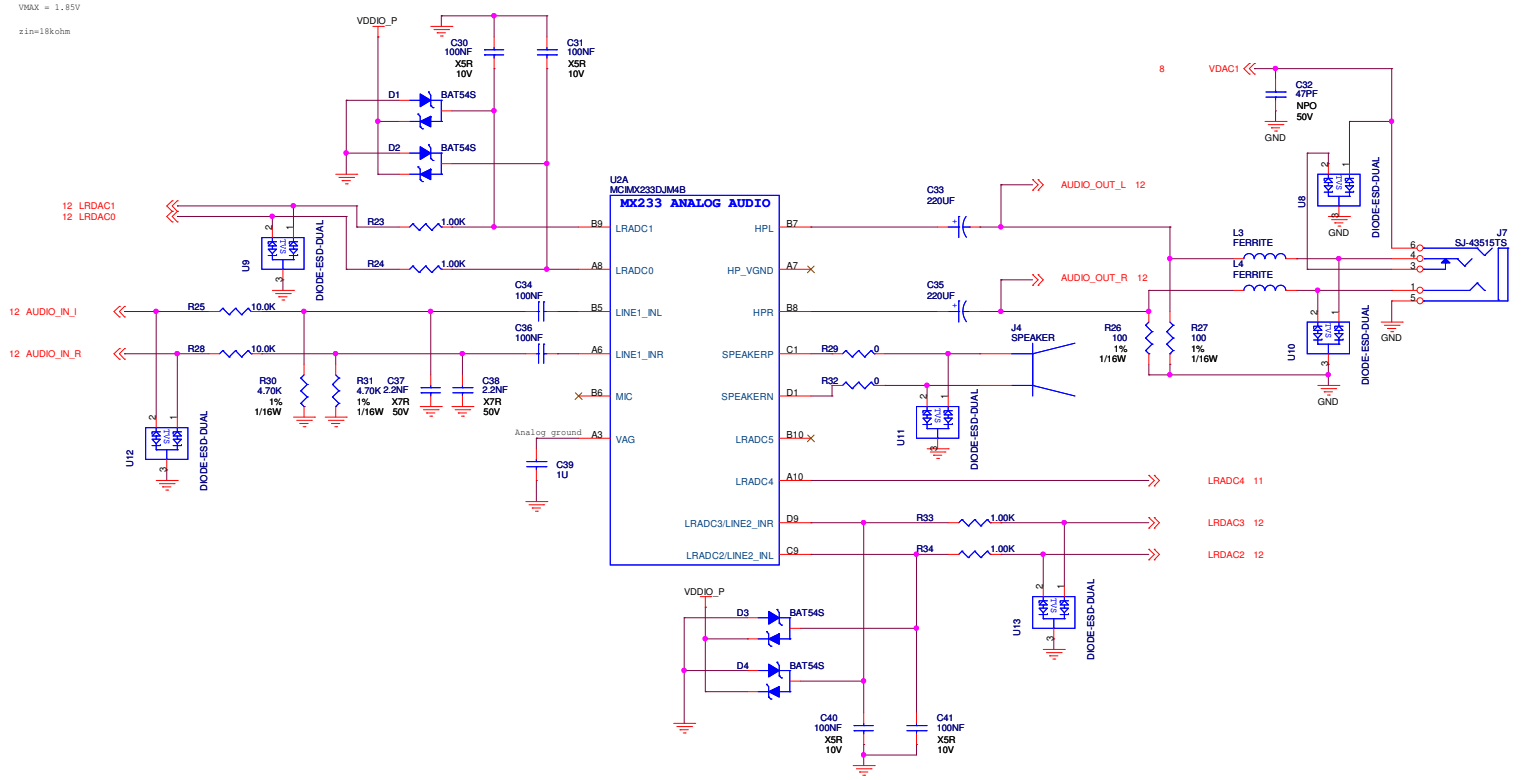

Title	OPENCALC OC1 AUDIO	
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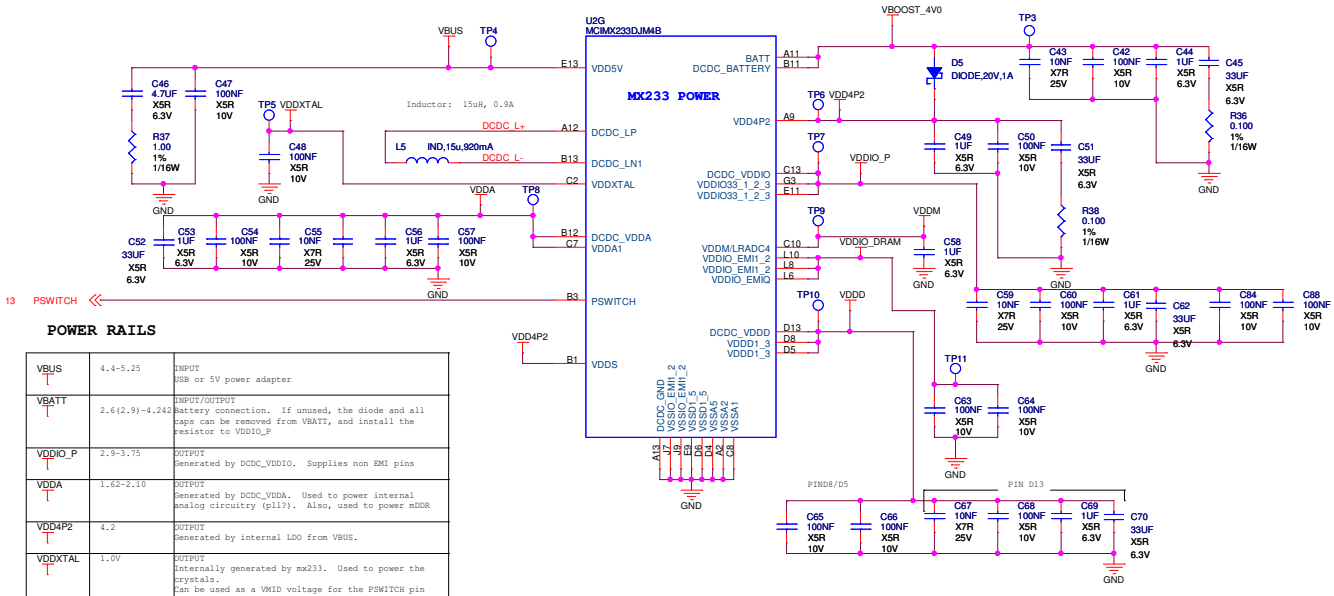
POWER



POWER RAILS

VBUS	4.4-5.25	INPUT USB or 5V power adapter
VBATT	2.6(2.9)-4.242	INPUT/OUTPUT Battery connection. If unused, the diode and all caps can be removed from VBATT, and install the resistor to VDDIO_P
VDDIO_P	2.9-3.75	OUTPUT Generated by DCDC_VDDIO. Supplies non EMI pins
VDDA	1.62-2.10	OUTPUT Generated by DCDC_VDDA. Used to power internal analog circuitry (pll?). Also, used to power mDDR
VDD4P2	4.2	OUTPUT Generated by internal LDO from VBUS.
VDDXTAL	1.0V	OUTPUT Internally generated by mx233. Used to power the crystals. Can be used as a VMID voltage for the PSWITCH pin
VDDM	2.5V	OUTPUT 2.5v supply for DDR (not for MDDR).
VDDIO_DRAM	1.8-3.25V	OUTPUT Must be shorted either to VDDM (DDR) or VDDA (mDDR). This is done on the memory page. Leave unconnected on this page.
VDDD	1.0-1.55V	OUTPUT Core voltage. Generated by LDO or DC-DC on chip.

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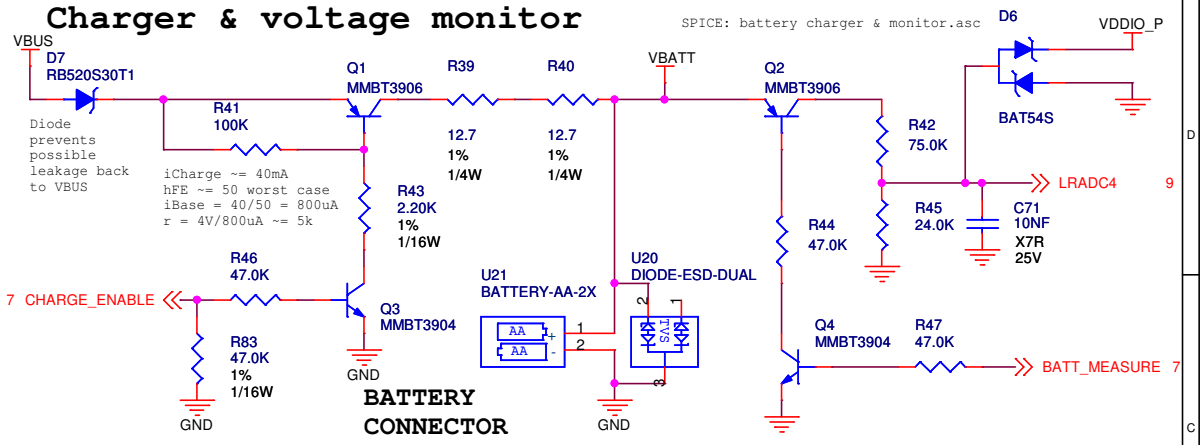
Charger & voltage monitor

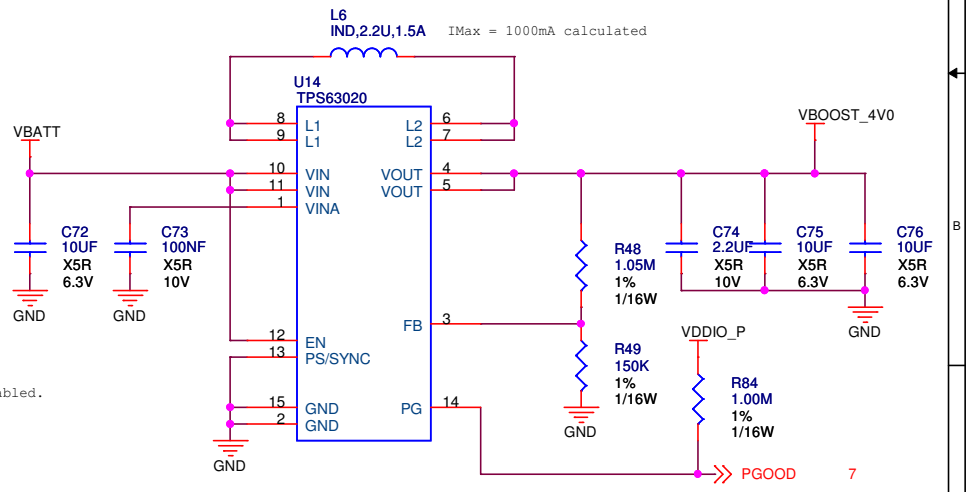
SPICE: battery charger & monitor.asc

```
VBATT = 2.0 - 3.2
C = 2200 mAh
C/30 = 73mA
VBUS = 5.0 nom
Ifinal = 73mA
R = V/I = (5-3.2)/73mA = 25 Ohms
Pmax = (5.25 - 2.0)^2/25 = 0.42 Watts
Pfinal = (5.25 - 3.2)^2/25 = 0.17 Watts
Iinitial = (5.25 - 2.0)/25 = 130mA
Ifinal = (5.25 - 23.2)/25 = 82mA
```



Battery (1.8 to 5.25 possbile) to VBOOST_4V0

```
Vin1: 5.25;
Vin2: 1.8;
Iout: 600e-3;
fr: 2.4;
Vout: 1.2;
L1: (Vin1 - Vout)*.5;
L2: Vout * .5;
L: max(L1, L2);
L: 2.2;
I1: Iout/.8 + Vout * (Vin1 - Vout)/(2 * Vin2 * fr * L);
I2: Vout * Iout/(.8*Vin2) + Vin2 * (Vout - Vin2)/(2*Vout*fr*L);
Imax = max(I1, I2);
Cout = 10 * L;
```




```
Battery only:
   All system power is provided through the boost regulator.
USB plugged in:
   All system power comes through VBUS.
USB+BATT:
   All system power comes through VBUS.  Battery charging enabled.
```

```
TPS63020 LEAKAGE = 25 uA typ
MX233 LEAKAGE = 11 uA typ when shut down

So, that looks like 40 uA to be safe for boost +
mx233.
1200e3 uA-h / 40 uA = 3.4 years on a full charge
before depletion.  This should be less than the
internal leakage for all except the best NiMH
batteries.  Not as good as Alkaline.
```

```
R1 = R2 * (Vout/Vfb -1 );
R2 = 150k;
Iout = Vfb/R2 = 0.5/150k = 3.33333uA
Vout = 4.0V
R1 = (4.0-0.5)/3.33333uA = 1.05mOhm
```

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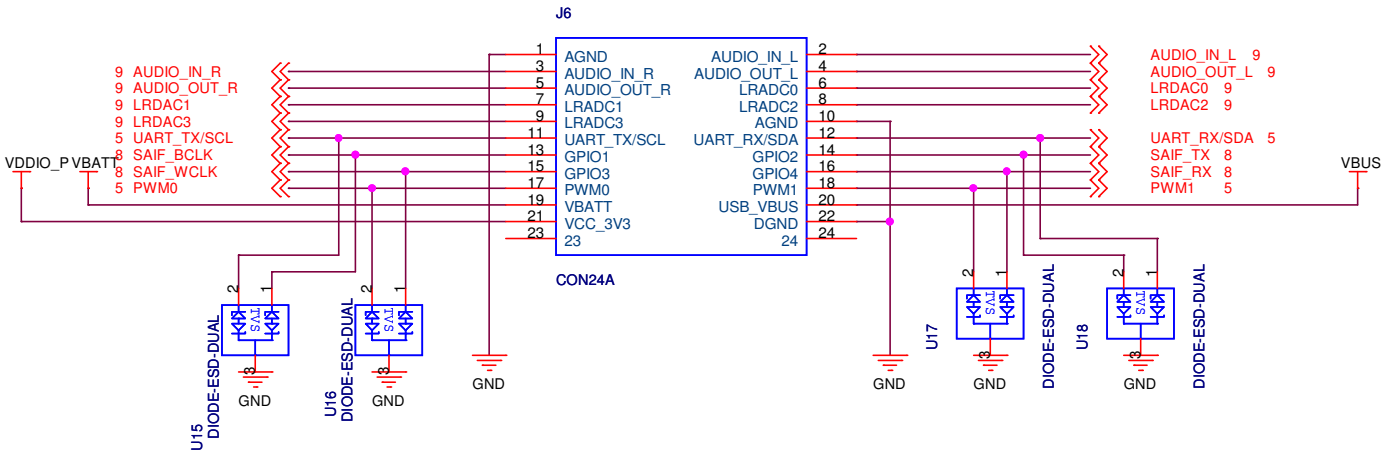
GEEK PORT

* TODO: IO protection on geek port pins

* All pins must be protected during system power off. This means that even when VDDIO_P is 0 V, no pin (at the CPU) is allowed to exceed VDDIO_P + 0.3 V, and GND - 0.3V. This will require something like a resistor + schottkey at each pin.

This can get tricky for analog pins.



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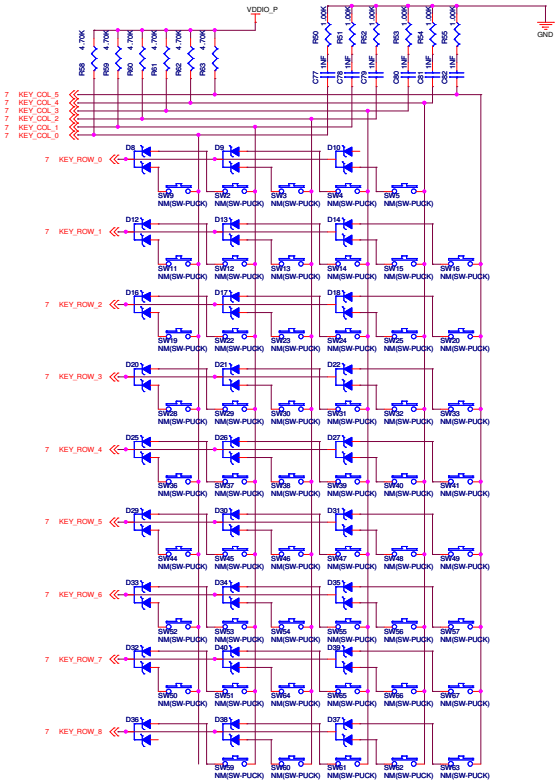
KEYPAD MATRIX



Keyscan Technique:

Software must drive rows low, and set col lines to input, interrupt whenever a colum line goes low. (or poll, that's fine too)

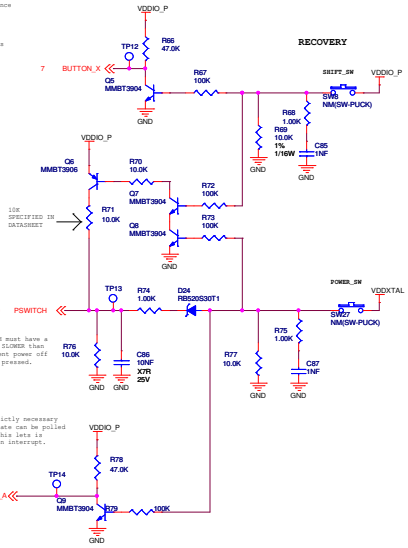
Then, when a column line goes low, to determine which key has been pressed, in the ISR sequence through each row with one-row-high and see which col line topples.

Any col lines that go high is pressed. The diodes prevent shorting 2 row and 2 col lines directly.

No ESD protection required if keymat can be made without locating holes. Is it possible to make the keymat holes just indentations?

NOTE; These caps are to keep the contacts clean, not to do any debouncing.

PRESS BOTH SW67 AND SW68 TO ENTER RECOVERY MODE.



PSWITCH_A is not strictly necessary -- the PSWITCH pin state can be polled from software. But this lets is operate simply from an interrupt.

PSWITCH STATES:
* If PSWITCH > min (MID) for > 100mS, then power on
* If PSWITCH has a falling edge faster than 15nS, power OFF
* If PSWITCH > min(MID), lower bit of HW_POWER_STS_PSWITCH is set.
* if PSWITCH is pulled to VDDIO via a resistor, upper bit of HW_POWER_STS_PSWITCH is set.
* If PSWITCH is pulled to VDDIO during initial boot sequence for more than 5 seconds, FW recovery mode is entered.

LOW: 0 < PSWITCH < 0.30
MID: 0.65 < PSWITCH < 1.5
HIGH: 2.1 < PSWITCH < VDDXTAL+1.575 = 2.575

VDDXTAL: ~ 1V
VDDIO: ~3.3

Title	OPENCALC OC1 KEYPAD MATRIX	
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