NOVATEK
聯 詠 科 技

Data Sheet

NT53002

Single Chip 480x480 Driver with Timing Controller

For 960x240 TFT LCD

V0.0
Preliminary

Revise History

Version	Content	Page	Date
0.0	Original.	All	7/30'08

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Features

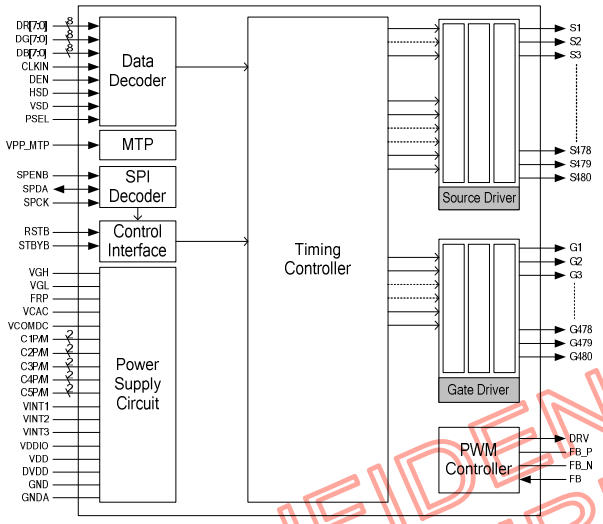
- Generate 480x480 TFT control signals with timing controller
- Panel resolution(H×V): 960×240
- Support low voltage / Normal LC α-TFT panel
- Support parallel RGB, series interface
- Support 8-bit RGB, 8-bit Dummy RGB, CCIR601 and CCIR656 input
- 8-bit resolution 256-gray scale with dithering.
- Build-in DC-DC control circuit, charge pump, VCOM with programmable DC/AC adjustment.
- Support Delta and Stripe color filter arrangement.
- Display control and function select by 3-wire serial communication control.
- Built-in R-DAC gamma correction.
- Ability to operate in single power supply(VDD):3.0V ~ 3.6V
- Power for digital interface(VDDIO): 1.8V~VDD
- Maximum operating frequency : 30MHz
- Output deviation: +/- 20mV.
- COG package.

General Description

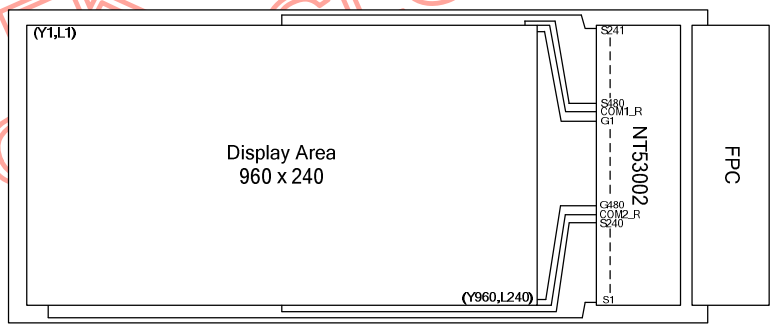
NT53002 is the one-chip solution for TFT-LCD small panel application. This chip is integrated source driver, gate driver, power generator and timing controller for the small panel application focused on the resolution of 960X240. The serial communication interface is also embedded for function setting.

This chip can be operated under a wide range of supply voltage. By applying “Double Gate Driver” panel architecture, the number of source output channel is reduced to 480 and the number of gate output channel is increased to 480. For the concern of lower power dissipation, line inversion driving technique is adopted. With dithering technique was applied, source output support 8-bit resolution 256-gray scale for small output deviation are designed to support higher color resolution

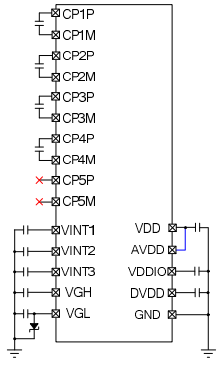
System Block Diagram



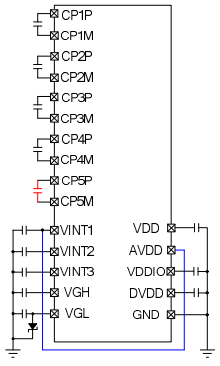
Application Block Diagram



Charge Pump Circuit



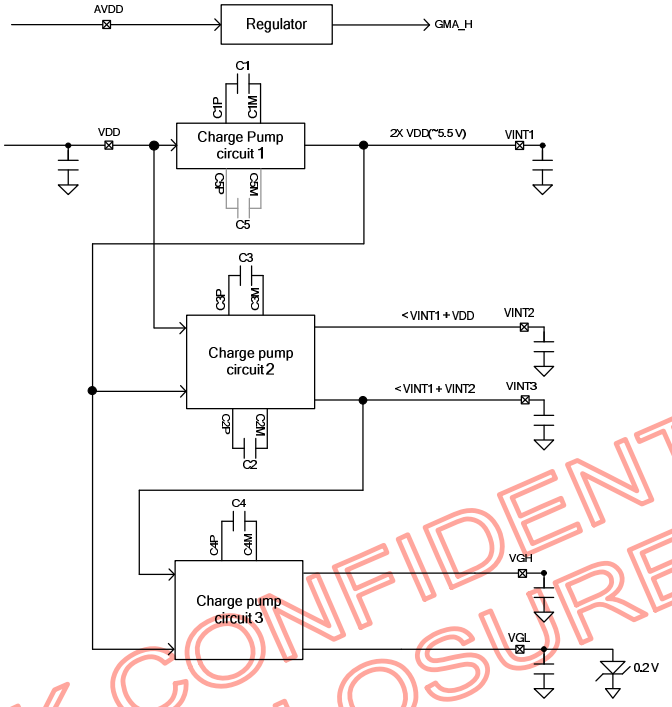
for Low Voltage LC



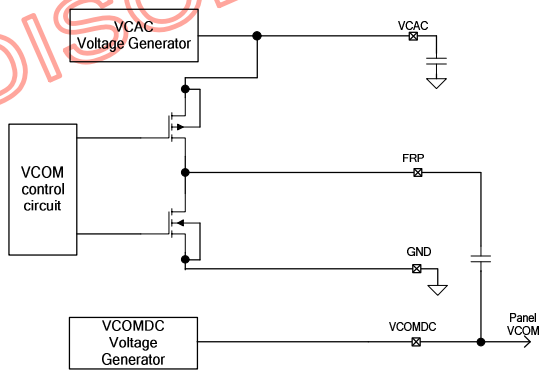
for Normal LC

Note: Schottky diode turn-on voltage<0.2V

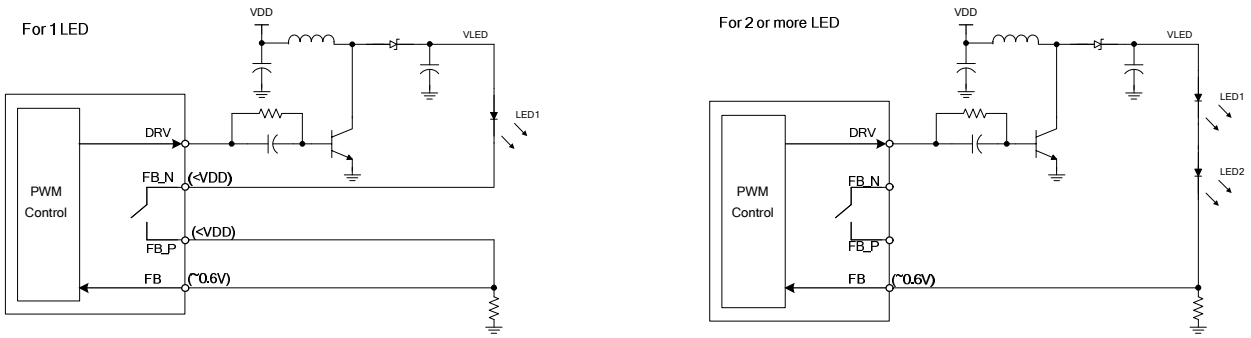
Charge Pump Block Diagram



VCOM Circuit



DC-DC Control Circuit



* Build-in switch was control by PWM_EN (R05H[1])

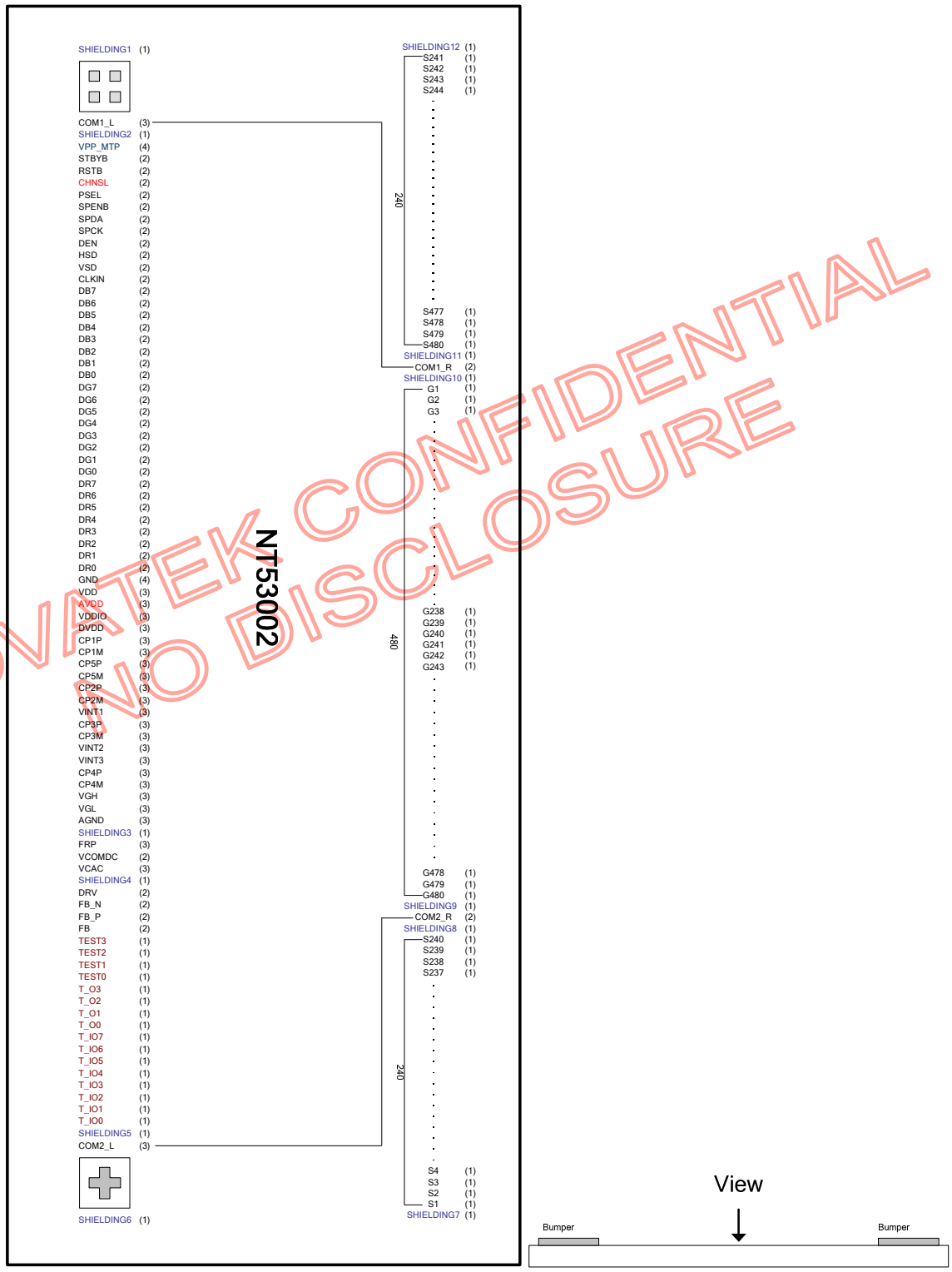
Recommend value of wiring resistance and capacitor.

Pad Name	Resistance (Ohm)	Pad Name	Resistance (Ohm)	Pad Name	Resistance (Ohm)
COM1_L	<=5	DG6	<=100	CP5P	<=5
VPP_MTP	<=5	DG5	<=100	CP5M	<=5
STBYB	<=100	DG4	<=100	CP2P	<=5
RSTB	<=100	DG3	<=100	CP2M	<=5
CHNSL	<=100	DG2	<=100	VINT1	<=5
PSEL	<=100	DG1	<=100	CP3P	<=5
SPENB	<=100	DG0	<=100	CP3M	<=5
SPDA	<=100	DR7	<=100	VINT2	<=5
SPCK	<=100	DR6	<=100	VINT3	<=5
DEN	<=100	DR5	<=100	CP4P	<=5
HSD	<=100	DR4	<=100	CP4M	<=5
VSD	<=100	DR3	<=100	VGH	<=5
CLKIN	<=100	DR2	<=100	VGL	<=5
DB7	<=100	DR1	<=100	AGND	<=5
DB6	<=100	DR0	<=100	FRP	<=5
DB5	<=100	GND	<=5	VCOMDC	<=5
DB4	<=100	VDD	<=5	VCAC	<=5
DB3	<=100	AVDD	<=5	DRV	<=5
DB2	<=100	VDDIO	<=5	FB_N	<=5
DB1	<=100	DVDD	<=5	FB_P	<=5
DB0	<=100	CP1P	<=5	FB	<=100
DG7	<=100	CP1M	<=5	COM2_L	<=5

Pin name	Capacitor no.	Withstanding voltage (V)	CAP (uF)
C1P	C1	10	≥2.2
C1M			
C2P	C2	10	≥2.2
C2M			
C3P	C3	16	≥2.2
C3M			
C4P	C4	16	≥2.2
C4M			
C5P	C5 (*)	10	≥2.2
C5M			
VDD/AVDD		6.3	≥4.7
DVDD		6.3	≥4.7
VINT1		10	≥4.7
VINT2		16	≥4.7
VINT3		25	≥4.7
VGH		25	≥4.7
VGL		16	≥4.7
VCAC		10	≥4.7
FRP-VCOMDC		10	≥2.2

Note: (*) C5 can be removing in Low Voltage LC application.

Pad Sequence (Bumper Side)



Pad Description

Designation	Type	Description
VDDIO	P	Power supply for digital interface.
VDD	P	Power supply for charge pump circuit.
AVDD	P	Power supply for analog circuit
GND	P	Ground for digital circuit.
AGND	P	Ground for analog circuit.
VGH	C	Power setting capacitor connecting pins.
VGL	C	Power setting capacitor connecting pins.
DVDD	C	Power setting capacitor connecting pins. (internal core use, typical 1.8V)
C1P/M	C	Capacitor for Charge Pump.
C2P/M	C	Capacitor for Charge Pump.
C3P/M	C	Capacitor for Charge Pump.
C4P/M	C	Capacitor for Charge Pump.
C5P/M	C	Capacitor for Charge Pump. (***)
VINT1	C	Power setting capacitor connecting pins.
VINT2	C	Power setting capacitor connecting pins.
VINT3	C	Power setting capacitor connecting pins.
STBYB	I	Standby setting pin, It should be connected to VDD or left floating in normal operation. If connected to GND, the IC is in standby mode. (Internal pulled high)
RSTB	I	Global reset pin, it should be connected to VDD or left floating in normal operation. If connected to GND, the controller is in reset state. (Internal pulled high)
COM1_L COM1_R	S	The internal link together between input side and output side.
COM2_L COM2_R	S	The internal link together between input side and output side.
CHNSL	I	Output channel selection pin. (Internal pulled high) CHNEL = "High": 480 channel source output. CHNEL = "Low": 320 channel source output. Output channel S1~S80 and S401~S480 will be disabled and output was random value.
PSEL	I	Parallel 24-bit and Serial 8-bit data input selection. (internal pulled high) PSEL =“High”: Serial 8-bit data input through DG0~DG7. PSEL =“Low”: Parallel 24-bit RGB input through DR0~DR7, DB0~DB7, DG0~DG7. (**)
SPENB	I	Serial communication chip select. (internal pulled High)
SPDA	I/O	Serial communication data input.
SPCK	I	Serial communication clock input.
VPP_MTP	P	MTP power input pin
DEN	I	Data Input Enable. Active High to enable the data input under “DE Mode”. (Internal pulled low)
HSD	I	Horizontal sync input. Negative polarity. (Internal pulled high)
VSD	I	Vertical sync input. Negative polarity. (Internal pulled high)
CLKIN	I	Clock signal. Latching data at the rising edge.
DB0~DB7	I	8-bit digital Blue data input, only valid when PSEL =“Low” (Parallel mode). (Internal pulled low)
DG0~DG7	I	When PSEL =“High”, these will be treated as serial 8-bit digital data input. (Including RGB or YUV). When PSEL =“Low”, these will be treated as 8-bit digital Green data input. (Internal pulled low)
DR0~DR7	I	8-bit digital Red data input, only valid when PSEL =“Low” (Parallel mode). (Internal pulled low)
FRP	O	Frame polarity output for panel VCOM.
VCOMDC	O	VCOM DC output.
VCAC	C	Power setting capacitor for VCOM AC.
DRV	O	Power transistor signal for back light power boost converter.
FB_P	I	ILED input and pass to one switch. Note: Voltage apply to this pad should < VDD.
FB_N	I	ILED output from one switch output. Note: Voltage apply to this pad should < VDD.
FB	I	Back light power boost converter feedback input.
S1~S480	O	Analog data output.

Designation	Type	Description
G1~G480	O	Gate control signal output.
TEST0~3	I	Test pin, reserved floating for normal operation.
T_O0~T_O3	O	Test pin, reserved floating for normal operation.
T_IO0~T_IO7	I/O	Test pin, reserved floating for normal operation.
SHIELDINGx	P	These pins were connecting to VGL internally. Reserved floating for normal operation.

Legend: I: Input, O: Output, P: power, D: Dummy, C: Capacitor, S: Pass line, T: Testing.

Note: (*) The voltage level of these signals is the same as VDDIO.
(**) It depends on the register setting. Please see three-wire for detailed description.
(***) Apply this capacitor or not base on application.

Align Mark:

Description	Type	Description
ALIGN_R	M	For assembly alignment.
ALIGN_L	M	For assembly alignment.

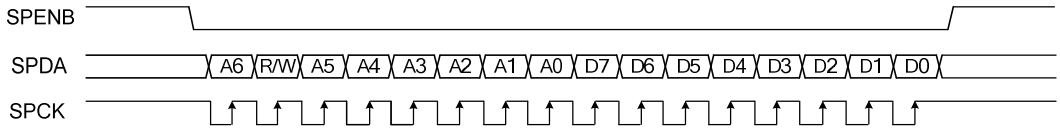
Legend: M: Marker

Pass Line Description:

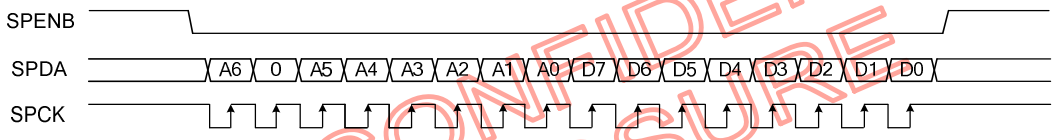
Pass Line No:	**Pad Name**	
1	COM1_L	COM1_R
2	COM2_L	COM2_R

3-Wire Serial control interface

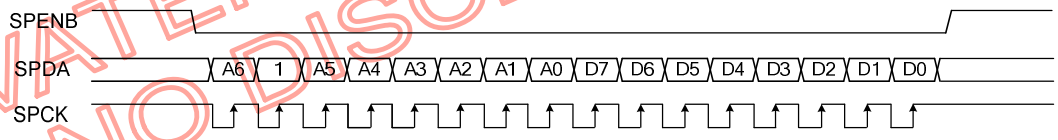
3-Wire Serial command format



- Each serial command consists of 16 bits of data that is loaded one bit a time at the rising edge of serial clock SPCK. Command loading operation starts from the falling edge of SPENB and is completed at the next rising edge of SPENB.
- The serial control block is operational after power on reset, but commands are established by the VSD signal. If command is transferred multiple times for the same register, the last command before the VSD signal is valid.
- If less than 16 bits of SPCK are input while SPENB is low, the transferred data is ignored.
- Serial block operates with the SPCK clock
- Serial data can be accepted in the stand-by mode.



Serial Interface Write Sequence



Serial Interface Read Sequence

3-Wire Register table

Register	Register Address								Default Value	Register Data (default)							
	A6	R/W	A5	A4	A3	A2	A1	A0		D7	D6	D5	D4	D3	D2	D1	D0
R00H	0	**1/0**	0	0	0	0	0	0	06h	Y_CbCr (0)	C601_EN (0)	x	x	VCAC (0110)			
R01H	0	**1/0**	0	0	0	0	0	1	51h	VCDCEN (1)	x	VCDC (21h)					
R03H	0	**1/0**	0	0	0	0	1	1	40h	BRIGHTNESS (40h)							
R04H	0	**1/0**	0	0	0	1	0	0	0Bh	NARROW (0)	C656_EN (0)	IF_SEL (00)		NP_SEL (10)		LDIR (1)	YDIR (1)
R05H	0	**1/0**	0	0	0	1	0	1	5Eh	DRV_SET (0)	GRB (1)	PWM_SEL (011)			VGHL_EN (1)	PWM_EN (1)	x
R06H	0	**1/0**	0	0	0	1	1	0	15h	HBLK_EN (0)	FB_SEL (00)	VBLK (15h)					
R07H	0	**1/0**	0	0	0	1	1	1	46h	HBLK (46h)							
R08H	0	**1/0**	0	0	1	0	0	0	00h	DRV_SEL (00)		x	x	x	x	x	x
R0BH	0	**1/0**	0	0	1	0	1	1	00h	REGSEL (0)	x	x	X	x	x	x	x
R0CH	0	**1/0**	0	0	1	1	0	0	06h	VST (00)		DE_EN (0)	CbCr (0)	DENP (0)	VSDP (1)	HSDP (1)	CLKINP (0)
R0DH	0	**1/0**	0	0	1	1	0	1	40h	CONTRAST (40h)							
R0EH	0	**1/0**	0	0	1	1	1	0	40h	x	R_CONT (40h)						
R0FH	0	**1/0**	0	0	1	1	1	1	40h	x	R_BRIGHT (40h)						
R10H	0	**1/0**	0	1	0	0	0	0	40h	x	B_CONT (40h)						
R11H	0	**1/0**	0	1	0	0	0	1	40h	x	B_BRIGHT (40h)						
R12H	0	**1/0**	0	1	0	0	1	0	00h	TRMEN (00)							
R16H	0	**1/0**	0	1	0	1	1	0	04h	x	x	x	x	x	GOP_EN (1)	x	x
R17H	0	**1/0**	0	1	0	1	1	1	54h	x	L016_SEL (101)			x	L008_SEL (100)		
R18H	0	**1/0**	0	1	1	0	0	0	54h	x	L050_SEL (101)			x	L032_SEL (100)		
R19H	0	**1/0**	0	1	1	0	0	1	43h	x	L096_SEL (100)			x	L072_SEL (011)		
R1AH	0	**1/0**	0	1	1	0	1	0	54h	x	L120_SEL (101)			x	L110_SEL (100)		
R2BH	0	**1/0**	1	0	1	0	1	1	00h	x	x	x	x	x	x	x	STB (0)
R2FH	0	**1/0**	1	0	1	1	1	1	61h	0	VGH_SEL (11)		CF_SET (0)	LC_SEL (00)		SOPC (01)	
R55H	1	**1/0**	0	1	0	1	0	1	00h	x	INV_SET (0)	x	x	x	x	x	x
R5Ah	1	**1/0**	0	1	1	0	1	0	02h	x	x	x	x	x	x	VGL_SEL (10)	

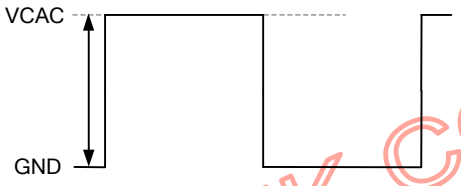
Notes:
1. When RSTB is low, all registers reset to default values.
2. Serial commands are executed at next VSD signal.
3. The register except upper list was for testing use, to read/write test register are not allow.

3-Wire Register Description

R00H – VCAC(R00H[3:0]): Common voltage AC level selection

D3	D2	D1	D0	VCAC voltage (V)
0	0	0	0	3.6
0	0	0	1	3.7
0	0	1	0	3.8
0	0	1	1	3.9
0	1	0	0	4.0
0	1	0	1	4.1
0	1	1	0	4.2 (default)
0	1	1	1	4.3
1	0	0	0	4.4
1	0	0	1	4.5
1	0	1	0	4.6
1	0	1	1	4.7
1	1	X	X	4.8

FRP Output



R00H – C601_EN (R00H[6]): CCIR601 input timing selection

CCIR601	Function
0	Disable CCIR601. (Default)
1	Enable CCIR601. (please refer to the table of R04H(IF_SEL) for detail description)

R00H - Y_CbCr (R00H[7]): Y & CbCr exchange position (only valid for 8-bit input YUV640 / YUV720)

	R0C[4] = '0'								R0C[4] = '1'							
Y_CbCr = '0' (Default)	Cb0	Y0	Cr0	Y1	Cb2	Y2	Cr2	Y3	Cr0	Y0	Cb0	Y1	Cr2	Y2	Cb2	Y3
Y_CbCr = '1'	Y0	Cb0	Y1	Cr0	Y2	Cb2	Y3	Cr2	Y0	Cr0	Y1	Cb0	Y2	Cr2	Y3	Cb2

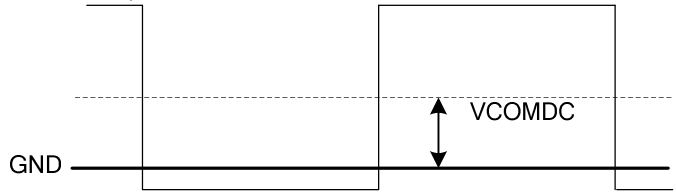
R01H – VCDC(R01H[5:0]): Common voltage DC level selection

Setting accuracy 20mV/step

D5~D0	VCOMDC Level selection
00h	0.24
:	:
21h	0.90 . (Default)
:	:
3Fh	1.5

Note: The MTP memory and 3-wire register was link to the same address in 3-wrie interface.
It will switch to MTP memory in default setting. To set REGSEL = 1 to switch to 3-wire register.

VCOMDC couple by FRP



R01H – VCDCEN(R01H[7]): VCOMDC output control

D7	VCDCE Function
0	The VCOMDC pin is disabled.
1	The VCOMDC output voltage follows VCOM_DC setting. (default)

R03H - BRIGHTNESS (R03H[7:0]): RGB brightness level

Setting accuracy 1bit/step

D7~D0	Brightness gain
00h	Dark. (-64)
40h	Center (0). (default)
FFh	Bright. (+191)

R04H – YDIR (R04H[0]): Shift registers of source driver direction selection

D0	HDIR Function
0	Shift from right to left. Y1←Y2←…←Y959←Y960
1	Shift from left to right. Y1→Y2→…→Y959→Y960 (Default)

R04H - LDIR (R04H [1]): Gate driver output direction selection

D1	VDIR Function
0	Shift from down to up. L1←L2←…←L239←L240
1	Shift from up to down. L1→L2→…→L239→L240 (Default)

R04H– NP_SEL (R04H [3:2]): NTSC or PAL input mode selection

D3	D2	NTSC/PAL Mode
0	0	PAL.
0	1	NTSC.
1	x	Auto detection. (Default)

R04H– IF_SEL (R04H [5:4]): Input format selection register

C601_EN	C656_EN	IF_SEL		Input format selection
		D5	D4	
0	0	0	0	8-bit RGB. (Default)
0	0	0	1	8-bit Dummy RGB 320 x 240.
0	0	1	x	8-bit Dummy RGB 360 x 240.
0	1	x	x	CCIR656.
1	1	0	x	YUV 640.
1	1	1	0	YUV 720.

R04H– C656_EN (R04H [6]): CCIR656/CCIR601 or RGB/RGB-Dummy input selection

D6	Data format
0	RGB input. (Default)
1	CCIR656/YUV640/YUV720 input.

YUV mode is executed immediately after program.

R04H– NARROW (R04H [7]): Normal display and Narrow display selection.

D7	Function
0	Normal display. (Default)
1	Narrow display.

R04H[7] = 0

R04H[7] = 1

R05H– PWM_EN (R05H [1]): Back light power converter enable control

D1	PWM enable control
0	The DRV output is off.
1	The DRV output is controlled by STB's power on/off sequence. (Default)

R05H– VGHL_EN (R05H [2]): VGH/VGL charge pump enable control

D2	VGHL enable control
0	VGH/VGL charge pump is off, VGL will set to GND level.
1	VGH/VGL charge pump is controlled by STB's power on/off sequence. (Default)

R05H– PWM_SEL (R05H [4:3]) : PWM duty cycle selection for back light power convert

PWM_SEL			function
D5	D4	D3	PWM duty cycle
0	0	0	**55%**
0	0	1	**60%**
0	1	0	**65%**
0	1	1	**70% (Default)**
1	0	0	**75%**
1	0	1	**80%**
1	1	0	**85%**
1	1	1	**90%**

R05H– GRB (R05H [6]): Global reset control register

D6	GRB Function
0	Reset all registers to default value.
1	Normal operation. (Default)

R05H– DRV_SET (R05H [7]): DRV signal frequency setting register

D7	DRV operation frequency
0	CLKIN/64. (Default)
1	CLKIN/128.

R06H - VBLK (R06H[4:0]): Vertical blanking setting register

For 8-bit RGB, 8-bit Dummy RGB, CCIR656, YUV640 and YUV720 NTSC mode,
Parallel RGB input mode (PSEL="Low"),

D4~D0	VBLK selection	Unit
00h~03h	3.	H
04h~14h	4~20	
15h	21. (Default)	
16h~1Fh	22~31	

For 8-bit Dummy RGB, CCIR656, YUV640 and YUV720 PAL mode. (Vertical blanking+3)

D4~D0	VBLK selection	Unit
00h~14h	3~23.	H
15h	24. (Default)	
16h~1Fh	25~34.	

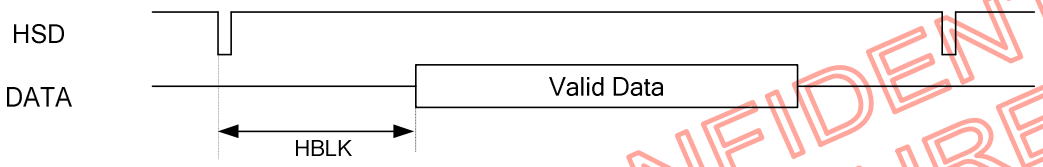
R06H - FB_SEL (R06H[6:5]): FB pin feedback voltage selector

D6~D5	FB threshold voltage
00	0.6 V. (default)
01	0.75V.
10	0.45V.
11	0.3V.

R06H/R07H – HBLK_EN(R6H[7]): HBLK function enable
HBLK (R07H[7:0]): Horizontal blanking setting

HBLK_EN	D7~D0	HBLK	Unit	NTSC/PAL Mode
X	32h~45h	50~69	CLKIN(*)	8-bit RGB.
X	46h	70		
X	47~FFh	71~255		
0	XXh	241	CLKIN(*)	8-bit Dummy RGB.
1	00h~03h	3		
	04h~FFh	4~255		
0	XXh	240	CLKIN(*)	YUV840, YUV720.
1	00h~03h	3		
	04h~FFh	4~255		
0	XXh	61	CLKIN(*)	Parallel RGB
1	04h~3Fh	4~63		

* The frequency of CLKIN is different under different input timing.



R08H –DRV_SEL(R08H[7:6]) : Backlight driving capability setting

D7	D6	DRV driving capability
0	0	Normal capability. (Default)
0	1	2 times the Normal capability.
1	0	4 times the Normal capability.
1	1	8 times the Normal capability.

R0BH – REGSEL(R0BH[7]): VCOMDC output select register

D7	REGSEL function
0	VCOMDC output voltage level was control by MTP memory. (Default)
1	VCOMDC output voltage level was control by 3-wire register memory (VCDC(R01H[5:0])). When user want to adjust the VCOMDC voltage level by R01H[5:0], user have to change the register to '1'. Refer to the "TRMEN" control register for the proper MPT write operation.

R0CH – CLKINP(R0CH[0]):CLKIN polarity selection

D0	CLKINP Function
0	Positive polarity. (Default)
1	Negative polarity

R0CH - HSDP((R0CH[1]):HSD polarity selection

D1	HSDP Function
0	Positive polarity.
1	Negative polarity. (Default)

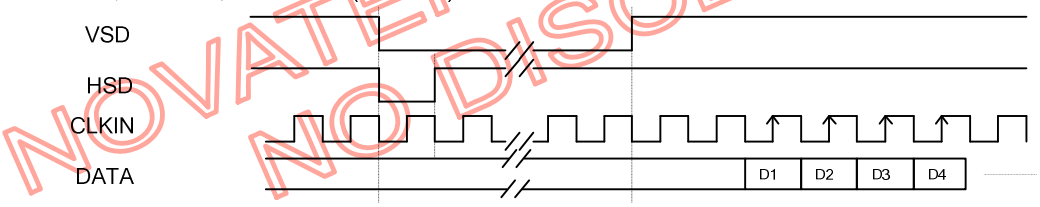
R0CH– VSDP(R0CH[2]):VSD polarity selection

D2	VSDP Function
0	Positive polarity.
1	Negative polarity. (Default)

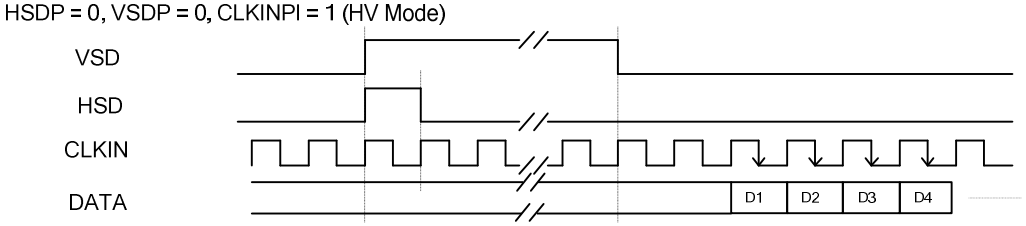
R0CH– DENP(R0CH [3]):DEN polarity selection

D3	DENP Function
0	Positive polarity (Default)
1	Negative polarity

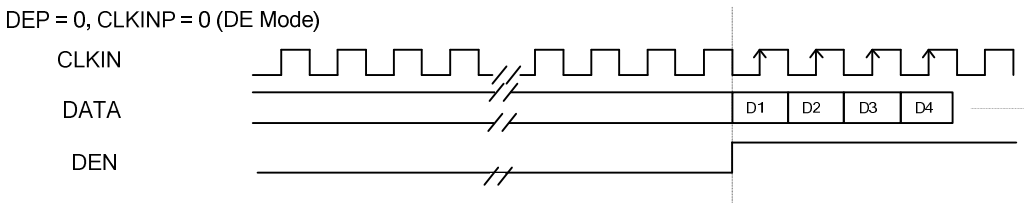
HSDP = 1, VSDP = 1, CLKINP = 0 (HV Mode)



HSDP = 0, VSDP = 0, CLKINPI = 1 (HV Mode)



DEP = 0, CLKINP = 0 (DE Mode)



R0CH– CbCr(R0CH [4]): Cb & Cr exchange position (for CCIR656 and YUV640/YUV720)

D4	CbCr Function
0	Cb→Y→Cr. (Default)
1	Cr→Y→Cb.

R0C– DE_EN (R0C [5]):DE Mode enable control

D5	DESEL Function
0	HV mode selected. (Default)
1	DE mode selected.

* DE_EN only controls the HV and DE mode at 8-bit RGB, 8-bit Dummy RGB and Parallel Mode.

R0CH - VST(R0CH [7:6]):Vertical start time of Odd/Even Frame

8-bit RGB / 8-bit Dummy RGB NTSC / 8-bit Dummy RGB PAL(*)
Parallel RGB input mode (PSEL= “Low”)

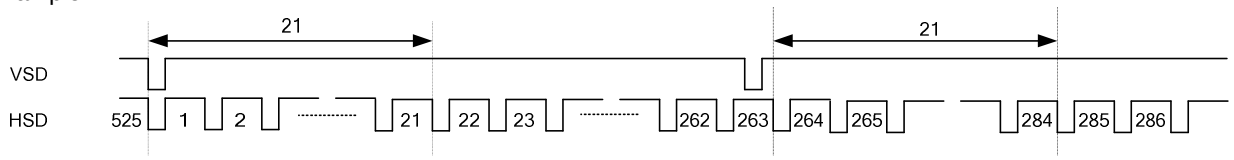
VST		VBLK	Unit
D7	D6	ODD/EVEN	
X	0	N / N. (Default)	H (Line)
X	1	N / N-1.	

CCIR656/YUV640/YUV720 NTSC/PAL(**)

VST		VBLK	Unit
D7	D6	ODD/EVEN	
0	0	N / N. (Default)	H (Line)
0	1	N / N+1.	
1	0	N+1 / N.	
1	1	N+1 / N+1.	

(*)The typical value of VBLK of 8-bit Dummy RGB PAL(24 H) is different than 8-bit RGB/8-bit Dummy RGB NTSC(21H).
(**) The typical value of VBLK of CCIR656 PAL(24 H) is different than CCIR656 NTSC(21H).
Note: VBLK must be adjusted base on the input data.

For example:



R0DH – CONTRAST(R0DH [7:0]) : RGB contrast level setting, the gain changes (1/64) / bit

D7~D0	Contrast gain
00h	0
40h	1(Default)
FFh	3.984

R0EH – R_CONT(R0EH [6:0]):Red sub-pixel contrast level setting, the gain changes (1/256)/bit

D6~D0	R Contrast gain
00h	0.75
40h	1(Default)
7Fh	1.246

R0FH – R_BRIGHT(R0FH [6:0]):Red sub-pixel brightness level setting, setting accuracy:1 step/bit

D6~D0	R Brightness gain
00h	DARK (-64)
40h	Center (0) (Default)
7Fh	Bright (+63)

R10H – B_CONT(R10 [6:0]):Blue sub-pixel contrast level setting, the gain changes (1/256)/bit

D6~D0	B Contrast gain
00h	0.75
40h	1 (Default)
7Fh	1.246

R11H – B_BRIGHT(R11H[6:0]):Blue sub-pixel brightness level setting, setting accuracy:1 step/bit

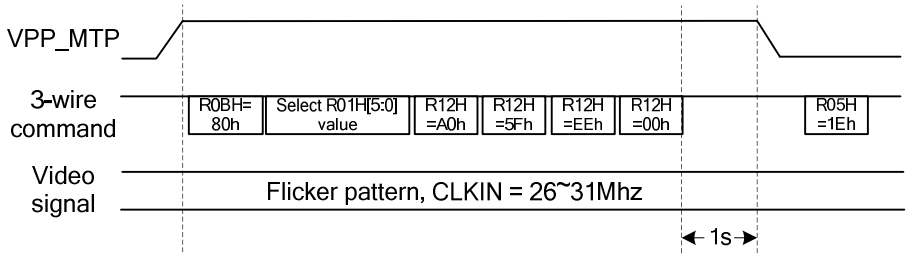
D6~D0	B Brightness gain
00h	DARK (-64)
40h	Center(0) (Default)
7Fh	Bright (+63)

R12H –TRMEN(R12H[7:0]): VCOM DC Trim Function Control Register

VCOMDC Trim function control register, this IC have build-in MTP memory, at Power-on, IC will auto load the MTP memory to set the VCOMDC level to prevent flick issue.

Operation condition:
1. CLKIN frequency range 26Mhz ~ 31Mhz
2. Apply 6VDC to VPPMTP pin.

Programming procedure:
1. Set REGSEL = 1 (R0BH = 80h)
2. Adjustment VCDC(R01H[5:0]) value, select proper VCOM_DC value
3. Set TRMEN[7:0] (R12H) as following sequence : A0h → 5Fh → EEh →00h.
4. Hold 1s for MTP control block operation.
5. Set global reset (set R05H = 1Eh) and restart the display operation.
6. Check the voltage level of VCOMDC pin.



Note:
1. The Trim Block can be writing only for "**2**" times.
2. After finishing TRMEN command do not power off within 1 second.
3. Trim command exceed the limit may cause the VCOMDC output unknown value.

R16H – GOP_EN(R16H[2]): Internal gamma op enable control

D2	Gamma op enable control
0	Output characteristic curve control by R17H~R1AH.
1	Output characteristic curve define by gamma correction resistor.(default)

R17H ~ R1AH

L008_SEL (R17H [2:0]): Gamma op output selection to level 8;
L016_SEL (R17H [6:4]): Gamma op output selection to level 16;
L032_SEL (R18H [2:0]): Gamma op output selection to level 32;
L050_SEL (R18H [6:4]): Gamma op output selection to level 50;
L072_SEL (R19H [2:0]): Gamma op output selection to level 72;
L096_SEL (R19H [6:4]): Gamma op output selection to level 96;
L110_SEL (R1AH [2:0]): Gamma op output selection to level 110;
L120_SEL (R1AH [6:4]): Gamma op output selection to level 120;

Reference point	000	001	010	011	100	101	110	111
L008 (100)	-100mV	-75mV	-50mV	-25mV	Default	+25mV	+50mV	+75mV
L016 (101)	-125mV	-100mV	-75mV	-50mV	-25mV	Default	+25mV	+50mV
L032 (100)	-100mV	-75mV	-50mV	-25mV	Default	+25mV	+50mV	+75mV
L050 (101)	-125mV	-100mV	-75mV	-50mV	-25mV	Default	+25mV	+50mV
L072 (011)	-75mV	-50mV	-25mV	Default	+25mV	+50mV	+75mV	+100mV
L096 (100)	-100mV	-75mV	-50mV	-25mV	Default	+25mV	+50mV	+75mV
L110 (100)	-100mV	-75mV	-50mV	-25mV	Default	+25mV	+50mV	+75mV
L120 (101)	-125mV	-100mV	-75mV	-50mV	-25mV	Default	+25mV	+50mV

R2BH – STB (R2BH [0]) : Normal / Standby mode control register

D0	STB Function
0	Standby Mode. (Default)
1	Normal operation.

R2FH – SOPC(R2FH[1:0]): Source output driving capability selection

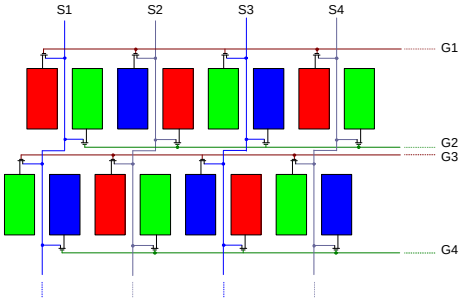
D1	D0	Source driver capability
0	0	-25%.
0	1	Normal. (default)
1	0	+25%.
1	1	+50%.

R2FH – LC_SEL(R55H[3:2]): LC type selection register

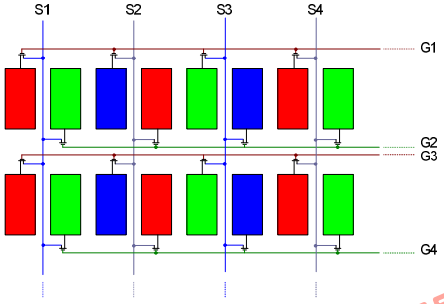
D5	D4	LC type selection
0	0	Low Voltage LC. (Default)
0	1	Reserved
1	0	Reserved
1	1	Normal LC

R2FH – CF_SET(R2FH[4]): Color filter selection register

CF_SET	Function
0	Delta color filter. (Default)
1	Stripe color filter.



Delta Color Filter



Stripe Color Filter

R2FH– VGH_SEL (R2FH[6:5]): VGH voltage level selection

D1	D0	VGH_SEL Function
0	0	|VGL| + 2V.
0	1	|VGL| + 3V.
1	0	|VGL| + 4V.
1	1	|VGL| + 5V. (Default)

R55H – INV_SET (R55H[6]): Inversion type selection

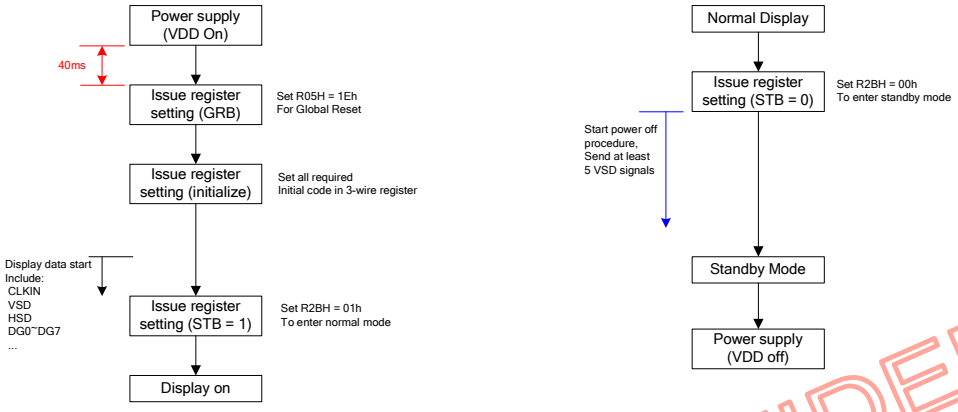
D6	INV_SEL Function
0	One line inversion. (Default)
1	Column inversion.

R5FH – VGL_SEL (R5FH[0:1]): VGL voltage level selection

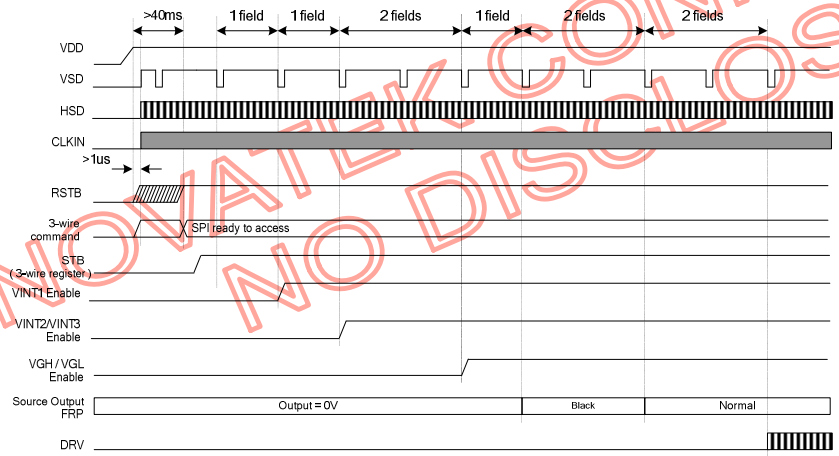
D1	D0	VGL_SEL Function
0	0	-8V.
0	1	-9V
1	0	-10V. (Default)
1	1	-11V

Function Description

Initialize flow chart

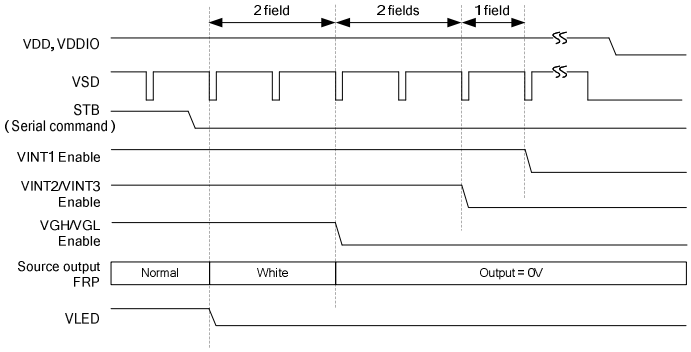


Power on sequence



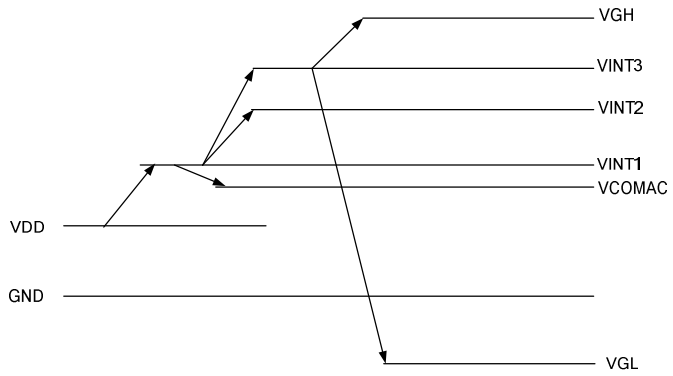
Note: 1. The RSTB should keep low state till VDD was stable, and set to high state before SPI command start.
2. After STB set to 1, it takes 9 VSD pulse for power on operation.

Power off sequence

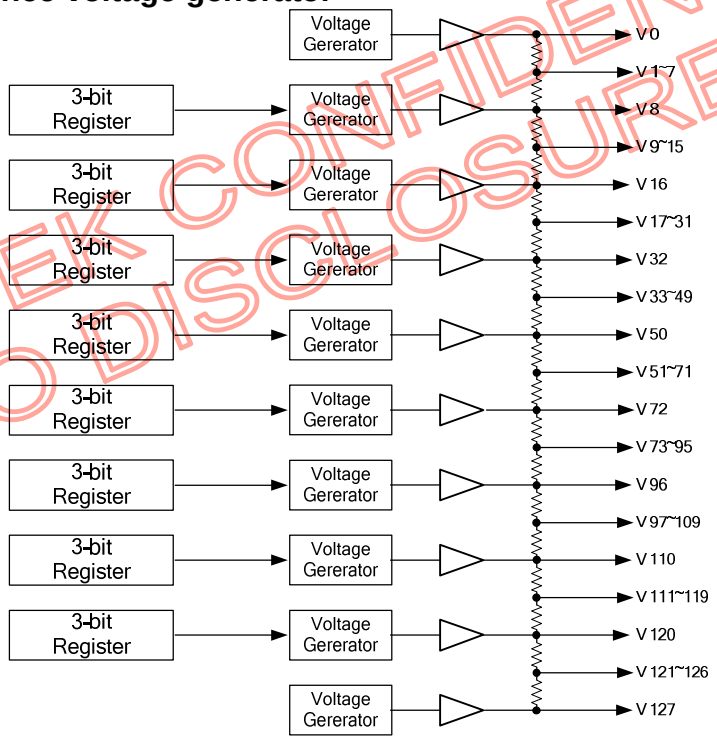


Note: For properly power off operation, the extra 5 VSD pulses (or more) after STB set to low were required.

Pattern diagram for voltage setting



Internal Gamma reference voltage generator



- 8 gamma correction reference point; V8/V16/V32/V50/V72/V96/V110/V120 are generated within driver IC and adjustable through serial register setting.
- Gamma correct reference point voltage step : 25mV

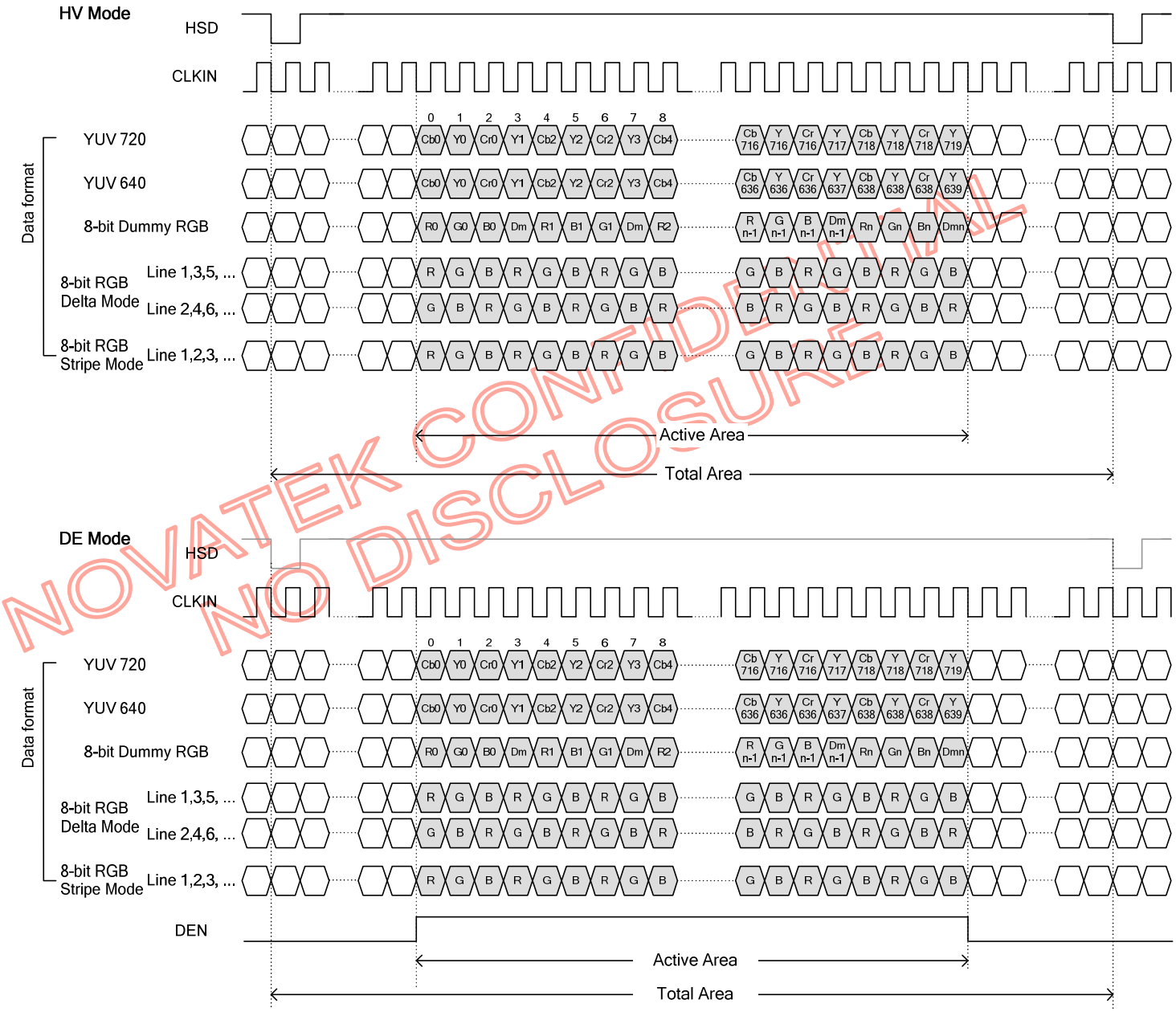
Output Voltage V.S. Input Data

Data	Voltage (FRP = Low)		Data	Voltage (FRP = High)
00	GAM_H x	1.000	00	GAM_H x 0.036
01	GAM_H x	0.989	01	GAM_H x 0.047
02	GAM_H x	0.949	02	GAM_H x 0.087
03	GAM_H x	0.914	03	GAM_H x 0.122
04	GAM_H x	0.882	04	GAM_H x 0.154
05	GAM_H x	0.855	05	GAM_H x 0.180
06	GAM_H x	0.832	06	GAM_H x 0.203
07	GAM_H x	0.812	07	GAM_H x 0.224
08	GAM_H x	0.795	08	GAM_H x 0.241
09	GAM_H x	0.779	09	GAM_H x 0.257
0A	GAM_H x	0.764	0A	GAM_H x 0.272
0B	GAM_H x	0.751	0B	GAM_H x 0.285
0C	GAM_H x	0.738	0C	GAM_H x 0.298
0D	GAM_H x	0.726	0D	GAM_H x 0.309
0E	GAM_H x	0.716	0E	GAM_H x 0.320
0F	GAM_H x	0.706	0F	GAM_H x 0.330
10	GAM_H x	0.696	10	GAM_H x 0.339
11	GAM_H x	0.686	11	GAM_H x 0.349
12	GAM_H x	0.676	12	GAM_H x 0.359
13	GAM_H x	0.667	13	GAM_H x 0.368
14	GAM_H x	0.659	14	GAM_H x 0.376
15	GAM_H x	0.651	15	GAM_H x 0.385
16	GAM_H x	0.643	16	GAM_H x 0.393
17	GAM_H x	0.636	17	GAM_H x 0.400
18	GAM_H x	0.628	18	GAM_H x 0.407
19	GAM_H x	0.621	19	GAM_H x 0.415
1A	GAM_H x	0.615	1A	GAM_H x 0.421
1B	GAM_H x	0.608	1B	GAM_H x 0.427
1C	GAM_H x	0.602	1C	GAM_H x 0.434
1D	GAM_H x	0.597	1D	GAM_H x 0.439
1E	GAM_H x	0.591	1E	GAM_H x 0.444
1F	GAM_H x	0.586	1F	GAM_H x 0.450
20	GAM_H x	0.580	20	GAM_H x 0.455
21	GAM_H x	0.575	21	GAM_H x 0.461
22	GAM_H x	0.570	22	GAM_H x 0.466
23	GAM_H x	0.564	23	GAM_H x 0.472
24	GAM_H x	0.559	24	GAM_H x 0.477
25	GAM_H x	0.554	25	GAM_H x 0.482
26	GAM_H x	0.550	26	GAM_H x 0.486
27	GAM_H x	0.545	27	GAM_H x 0.491
28	GAM_H x	0.541	28	GAM_H x 0.495
29	GAM_H x	0.536	29	GAM_H x 0.500
2A	GAM_H x	0.532	2A	GAM_H x 0.504
2B	GAM_H x	0.527	2B	GAM_H x 0.509
2C	GAM_H x	0.523	2C	GAM_H x 0.513
2D	GAM_H x	0.518	2D	GAM_H x 0.518
2E	GAM_H x	0.514	2E	GAM_H x 0.521
2F	GAM_H x	0.511	2F	GAM_H x 0.525
30	GAM_H x	0.507	30	GAM_H x 0.528
31	GAM_H x	0.504	31	GAM_H x 0.532
32	GAM_H x	0.500	32	GAM_H x 0.536
33	GAM_H x	0.497	33	GAM_H x 0.539
34	GAM_H x	0.494	34	GAM_H x 0.542
35	GAM_H x	0.490	35	GAM_H x 0.545
36	GAM_H x	0.487	36	GAM_H x 0.549
37	GAM_H x	0.484	37	GAM_H x 0.552
38	GAM_H x	0.481	38	GAM_H x 0.555
39	GAM_H x	0.477	39	GAM_H x 0.558
3A	GAM_H x	0.474	3A	GAM_H x 0.562
3B	GAM_H x	0.471	3B	GAM_H x 0.565
3C	GAM_H x	0.468	3C	GAM_H x 0.568
3D	GAM_H x	0.464	3D	GAM_H x 0.571
3E	GAM_H x	0.461	3E	GAM_H x 0.575
3F	GAM_H x	0.458	3F	GAM_H x 0.578
40	GAM_H x	0.455	40	GAM_H x 0.581
41	GAM_H x	0.451	41	GAM_H x 0.584
42	GAM_H x	0.448	42	GAM_H x 0.588
43	GAM_H x	0.445	43	GAM_H x 0.591
44	GAM_H x	0.442	44	GAM_H x 0.594
45	GAM_H x	0.438	45	GAM_H x 0.597

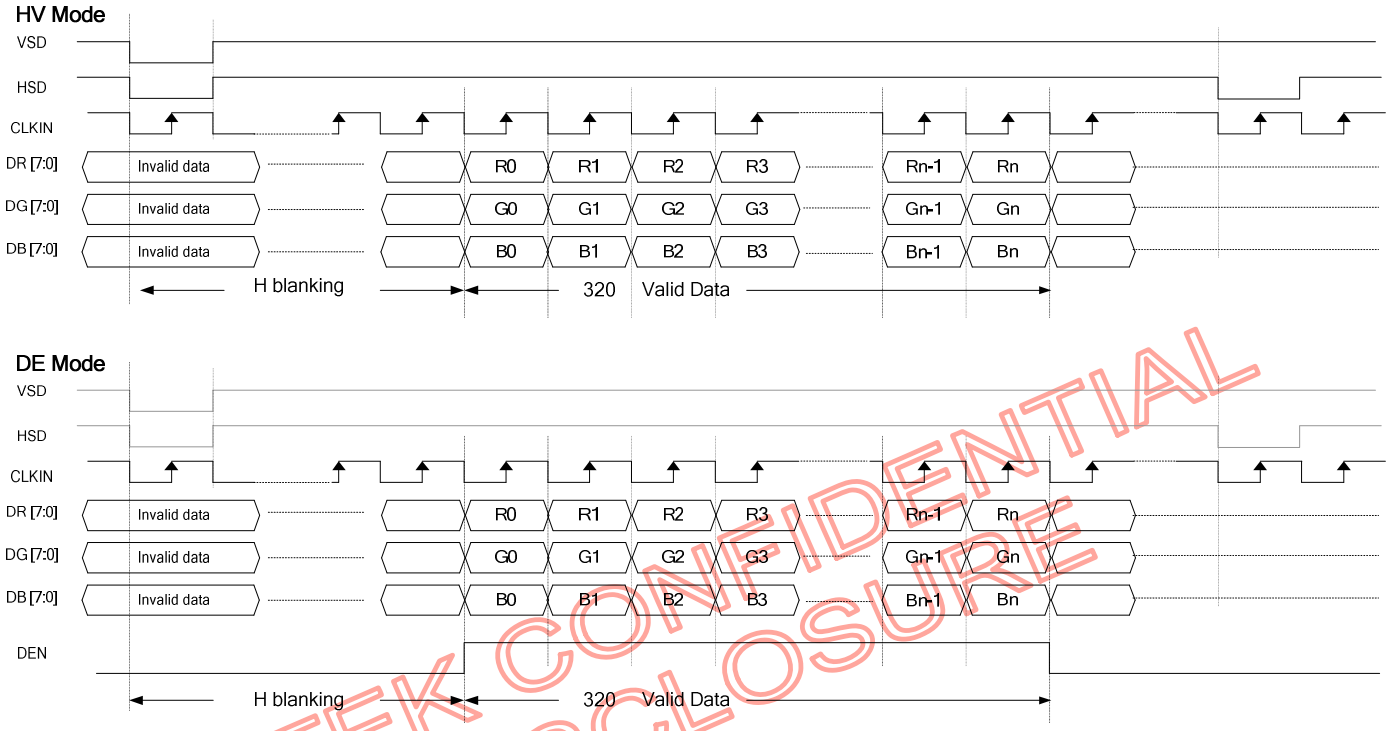
Data	Voltage (FRP = Low)		Data	Voltage (FRP = High)	
46	GAM_H x	0.435	46	GAM_H x	0.601
47	GAM_H x	0.432	47	GAM_H x	0.604
48	GAM_H x	0.429	48	GAM_H x	0.607
49	GAM_H x	0.425	49	GAM_H x	0.610
4A	GAM_H x	0.422	4A	GAM_H x	0.614
4B	GAM_H x	0.419	4B	GAM_H x	0.617
4C	GAM_H x	0.415	4C	GAM_H x	0.621
4D	GAM_H x	0.412	4D	GAM_H x	0.624
4E	GAM_H x	0.408	4E	GAM_H x	0.627
4F	GAM_H x	0.405	4F	GAM_H x	0.631
50	GAM_H x	0.402	50	GAM_H x	0.634
51	GAM_H x	0.398	51	GAM_H x	0.637
52	GAM_H x	0.395	52	GAM_H x	0.641
53	GAM_H x	0.392	53	GAM_H x	0.644
54	GAM_H x	0.388	54	GAM_H x	0.647
55	GAM_H x	0.385	55	GAM_H x	0.651
56	GAM_H x	0.382	56	GAM_H x	0.654
57	GAM_H x	0.378	57	GAM_H x	0.657
58	GAM_H x	0.375	58	GAM_H x	0.661
59	GAM_H x	0.372	59	GAM_H x	0.664
5A	GAM_H x	0.368	5A	GAM_H x	0.667
5B	GAM_H x	0.365	5B	GAM_H x	0.671
5C	GAM_H x	0.362	5C	GAM_H x	0.674
5D	GAM_H x	0.358	5D	GAM_H x	0.677
5E	GAM_H x	0.355	5E	GAM_H x	0.681
5F	GAM_H x	0.352	5F	GAM_H x	0.684
60	GAM_H x	0.348	60	GAM_H x	0.688
61	GAM_H x	0.345	61	GAM_H x	0.691
62	GAM_H x	0.341	62	GAM_H x	0.694
63	GAM_H x	0.338	63	GAM_H x	0.698
64	GAM_H x	0.335	64	GAM_H x	0.701
65	GAM_H x	0.331	65	GAM_H x	0.705
66	GAM_H x	0.328	66	GAM_H x	0.708
67	GAM_H x	0.324	67	GAM_H x	0.711
68	GAM_H x	0.320	68	GAM_H x	0.716
69	GAM_H x	0.316	69	GAM_H x	0.720
6A	GAM_H x	0.312	6A	GAM_H x	0.724
6B	GAM_H x	0.307	6B	GAM_H x	0.728
6C	GAM_H x	0.303	6C	GAM_H x	0.733
6D	GAM_H x	0.299	6D	GAM_H x	0.737
6E	GAM_H x	0.295	6E	GAM_H x	0.741
6F	GAM_H x	0.289	6F	GAM_H x	0.746
70	GAM_H x	0.284	70	GAM_H x	0.751
71	GAM_H x	0.279	71	GAM_H x	0.757
72	GAM_H x	0.274	72	GAM_H x	0.762
73	GAM_H x	0.268	73	GAM_H x	0.768
74	GAM_H x	0.262	74	GAM_H x	0.774
75	GAM_H x	0.256	75	GAM_H x	0.780
76	GAM_H x	0.249	76	GAM_H x	0.787
77	GAM_H x	0.241	77	GAM_H x	0.795
78	GAM_H x	0.232	78	GAM_H x	0.804
79	GAM_H x	0.223	79	GAM_H x	0.813
7A	GAM_H x	0.212	7A	GAM_H x	0.823
7B	GAM_H x	0.200	7B	GAM_H x	0.836
7C	GAM_H x	0.186	7C	GAM_H x	0.850
7D	GAM_H x	0.160	7D	GAM_H x	0.876
7E	GAM_H x	0.133	7E	GAM_H x	0.902
7F	GAM_H x	0.036	7F	GAM_H x	1.000

Data Input Format

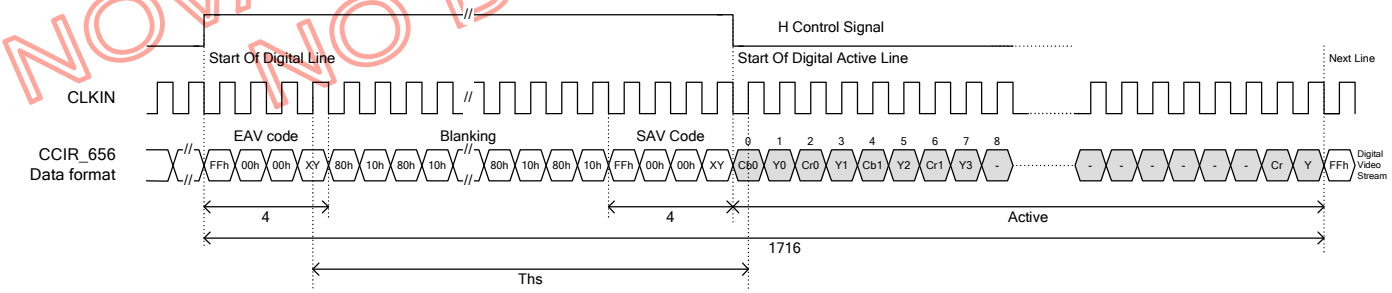
Serial 8-bit RGB / 8-bit Dummy RGB / YUV Mode Data format



Parallel RGB Mode Data format



CCIR_656 Mode Data format



- FF 00 00 XY signals are involved with HSD,VSD and Field
- XY encode following bits:
  F=field select
  V=indicate vertical blanking
  H=1 if EAV else 0 for SAV
  P3-P0=protection bits :
  P3=V⊕H P2=F⊕H P1=F⊕V P0=F⊕V⊕H ⊕: Represents the exclusive-OR function

XY							
D7 (MSB)	D6	D5	D4	D3	D2	D1	D0
1	F	V	H	P3	P2	P1	P0

- Control is provided through “End of Video” (EAV) and “Start of Video” (SAV) timing references.
- Horizontal blanking section consists of repeating pattern "80 10 80 10".

Data Active Area

Input Format	Format Standard	CLKIN(MHz)	H	Total AREA	Active AREA
YUV	CCIR_601	fCLKIN = 27	1	1716	1440
	CCIR_656			1728	
	CCIR_601	fCLKIN = 24.54	1	1560	1280
8-bit Dummy RGB	NTSC/PAL	fCLKIN = 27	1	1560	1440
		fCLKIN = 24.54			1280
8-bit RGB	NTSC/PAL	fCLKIN = 27	1	1716	960
24bit RGB	320RGB x 240	fCLKIN =6.4	1	408	320 (RGB)

(Unit:CLKIN)

CCIR656/YUV640/YUV720 to RGB Conversion Formula

Rn = 1.164*[(Y2n-1+Y2n)/2-16] + 1.596*(Crn-128)
Gn = 1.164*[(Y2n-1+Y2n)/2-16] - 0.813*(Crn-128) – 0.392*(Cbn-128)
Bn = 1.164*[(Y2n-1+Y2n)/2-16] + 2.017*(Cbn-128)
Where Y: 16~235 Cr: 16~240 Cb: 16~240

Absolute Maximum Ratings*

Supply voltage, VDD	**-0.3V to 5V**
Interface supply voltage, VDDIO	**-0.3V to VDD+0.3V**
Logic supply voltage, DVDD	**-0.3V to 3V**
Input signal voltage	**-0.3V to VDDIO+0.3V**
Storage temperature	**-55°C to 125°C**
Operating temperature	**-20°C to 85°C**

*Comments

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or under any other conditions above those indicated in the operational sections of this specification are not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended operation range

(GND=AGND=PGND= 0V, TA = -20 to 85°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Digital Supply Voltage	VDD	3.0	3.3	3.6	V	

DC Electrical Characteristics

(VDD=3.0~3.6V, VDDIO=AVDD=VDD, AGND=GND=0V, TA=25°C)
• (For the digital circuit :)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
I/O Supply Voltage	VDDIO	1.8	-	VDD	V	
High Level Input Voltage	Vih	0.7xVDDIO	-	VDDIO	V	VDDIO = 2.7V~3.6V
		0.8xVDDIO	-	VDDIO	V	VDDIO = 1.8V~2.7V
Low Level Input Voltage	Vil	GND	-	0.3xVDDIO	V	VDDIO = 2.7V~3.6V
		GND	-	0.2xVDDIO	V	VDDIO = 1.8V~2.7V
High Level Output Voltage	Voh	VDDIO-0.4V	-	VDDIO	V	VDDIO = 3.3V @ Ioh = -400uA
Low Level Output Voltage	Vol	GND	-	0.4V	V	VDDIO = 3.3V @ Iol = 400uA
Input Leakage Current	Ii	-	-	±1	uA	Digital input pins.
Pull-high/low Impedance	Rin	125k	200k	350k	ohm	VDDIO = 3.3V

•(For the analog circuit)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Analog supply voltage	AVDD	VDD	-	VINT1	V	
Gamma supply voltage	GMA_H	-	2.8 (5)	-	V	For Low Voltage LC
		-	4.6 (5)	-	V	For Normal Voltage LC
Voltage Deviation of Outputs	Vvd	-	±20	±35	mV	Vo=0.1V ~ 0.5V & GMA_H-0.5 ~ GMA_H- 0.1V
			±15	±20	mV	Vo=0.5V ~ GMA_H-0.5V
Dynamic Range of Output	Vdr	0.1	-	GMA_H-0.1	V	S1 ~ S480
Driving current of Source outputs	IOHS	-	-25	-	uA	Vos = GMA_H-0.2V, Vys = GMA_H-1.1V (1)
Sinking current of Source outputs	IOLS	-	25	-	uA	Vos = 0.2V, Vys = 1.1V (1)
Driving current of Gate outputs	IOHG	-	-200	-	uA	VGH = 15V, VGL = -10V, Vog = 15V, Vyg = 14.5V (2)
Sinking current of Gate outputs	IOLG	-	200	-	uA	VGH = 15V, VGL = -10V, Vog = -10V, Vyg = -9.5V (2)
Base drive current for PWM	IDRV	-	0.25	-	mA	VDD=3.3V, DRV=0.7 V
DRV output voltage for PWM	VDRV	0	-	VDD	V	
Feed back voltage for PWM	VFB	0.25	0.6	0.8	V	DC/DC operating
VCAC DC Tolerance	VCAC	-100	-	+100	mV	VCAC value by VCOM_AC setting
FRP Low level output current	IOLF	-	5	-	mA	For VCAC = 4.2V, Vofrp = 0V (4) Vyfrp = 0.9V (3)
FRP High level output current	IOHF	-	-5	-	mA	For VCAC = 4.2V, Vofrp = 4.2V (4) Vyfrp = 3.3V (3)
GMA_H voltage tolerance	VGMAHT	-70	-	+70	mV	VDD = AVDD = 3.0V~3.6V, Low Voltage LC
		-140	-	+140	mV	AVDD = VINT1, Normal LC
VGH output tolerance	VGHT1	-0.6	-	+1.0	V	CLKIN=27MHz, VSD = 60hz, HSD = 15.75Khz VGH_SEL = 01b, 10b, and 11b.
	VGHT2	-0.7	-	+1.1	V	CLKIN=27MHz, VSD = 60hz, HSD = 15.75Khz VGH_SEL = 00b.
VGL output tolerance	VGLT1	-0.6	-	+0.6	V	CLKIN=27MHz, VSD = 60hz, HSD = 15.75Khz VGL_SEL = 01b, 10b, and 11b.
	VGLT2	-0.6	-	+1.1	V	CLKIN=27MHz, VSD = 60hz, HSD = 15.75Khz VGL_SEL = 00b.
Driving current of VCOMDC	ICDCH	-10	-	-	uA	Vycdc = VCOMDC - 1V
Sinking current of VCOMDC	ICDCL	-	-	10	uA	Vycdc = VCOMDC + 1V
VCOMDC output tolerance	VDCT	-35	-	+35	mV	No Loads.
Ripple of VGL	Vglrp	-150	-	50	mV	No loads, Power setting capacitors are default setting.
Stand-by Current	Ist	-	80	100	uA	STB="0",all function are shutdown
Operating Current	Iop	-	6.5	8	mA	No load, line inversion, @Frame rate = 60Hz Low voltage LC
		-	13	(TBD)		No load, line inversion, @Frame rate = 60Hz Normal LC

Notes:
1. Vys, Vyg is the voltage applies to source and gate output pins.
2. Vos, Vog is the output voltage of source and gate output pins.
3. Vyfrp is the voltage applies to FRP pin.
4. Vofrp is the output voltage of FRP pin.
5. Vycdc is the voltage applies to VCOMDC pin

AC Electrical Characteristics

(VDD=3.0~3.6V, VDDIO=AVDD=VDD, AGND=GND=0V, TA=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
CLKIN clock pulse width	Tcpw	33			ns	
CLKIN pulse duty cycle	Tcw	40	50	60	%	
VSD setup time	Tvst	12	-	-	ns	
VSD hold time	Tvhd	12	-	-	ns	
HSD setup time	Thst	12	-	-	ns	
HSD hold time	Thhd	12	-	-	ns	
HSD period time	Th	37	-	68	us	
DEN setup time	Tdest	12	-	-	ns	
DEN hold time	Tdehd	12	-	-	ns	
Data setup time	Tdsu	12	-	-	ns	DR0~DR7, DG0~DG7, DB0~DB7 to CLKIN
Data hold time	Tdhd	12	-	-	ns	DR0~DR7, DG0~DG7, DB0~DB7 to CLKIN
Time that VSD to 1st Gate output	Tstv	1	21	31	H	@ 8-bit RGB, 8-bit Dummy RGB NTSC, and Parallel RGB, Delay by VBLK setting.
Time that CCIR_V to 1st Gate output	Tstv	1	22	31	H	@ CCIR656 NTSC, Delay by VBLK setting.
Time that CCIR_V to 1st Gate output	Tstv	3	24	34	H	@ 8-bit Dummy RGB & CCIR656 PAL, Delay by VBLK setting.
Source output setting time	Tst	-	-	8	us	R= 25K ohm , C= 30 pF, 10% → 90% final.
Gate output setting time	Tstg	-	0.5	1	us	R= 3K ohm , C= 25 pF, 10% → 90% final.
VCOM setting time	Tst,vcom	-	-	9	us	R= 200 ohm , C= 5 nF, 10% → 90% final.
Time that HSD pulse width	Twh	1	-	-	CLKIN	

Serial Control Timing

(VDD=3.0~3.6V, VDDIO=AVDD=VDD, AGND=GND=0V, TA=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
SPENB input setup time	Tsens	50			ns	
Serial data input setup time	Tsdas	50			ns	
SPENB input hold time	Tsenh	50			ns	
Serial data input hold time	Tsdah	50			ns	
SPCK pulse high width	Tsckh	50			ns	
SPCK pulse low width	Tsckl	50			ns	
SPENB pulse high width	Tsenp	400			ns	

Output Timing Table

8-bit RGB / 8-bit Dummy RGB / YUV640 / YUV720 / CCIR_656

AC Electrical Characteristics (VDD =3.0~3.6V, VDDIO=AVDD=VDD, AGND=GND=0V, TA=25°C)

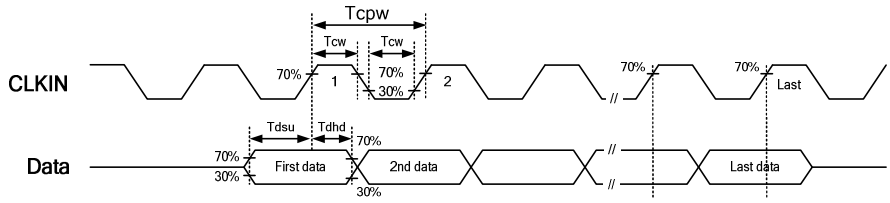
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Time that the HSD to Source output	Thso	-	3.5	-	CLKIN	
Time that the HSD to Gate output	Thgo	-	64.5	-	CLKIN	
Time that the HSD to Gate output off	Thgz	-	22.5	-	CLKIN	

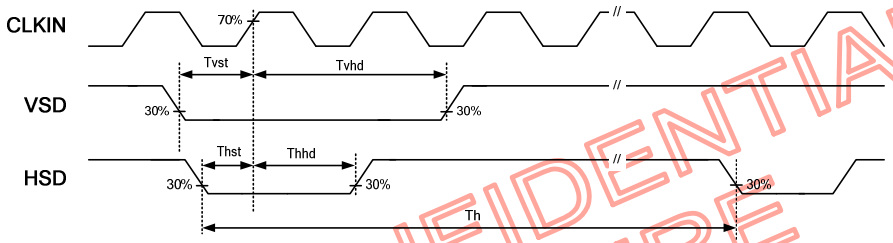
Parallel RGB

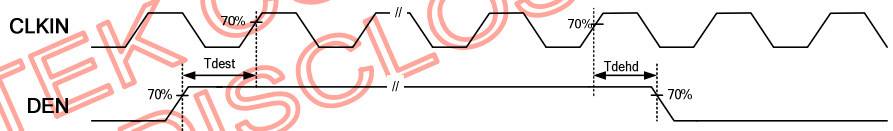
AC Electrical Characteristics (VDD =3.0~3.6V, VDDIO=AVDD=VDD, AGND=GND=0V, TA=25°C)

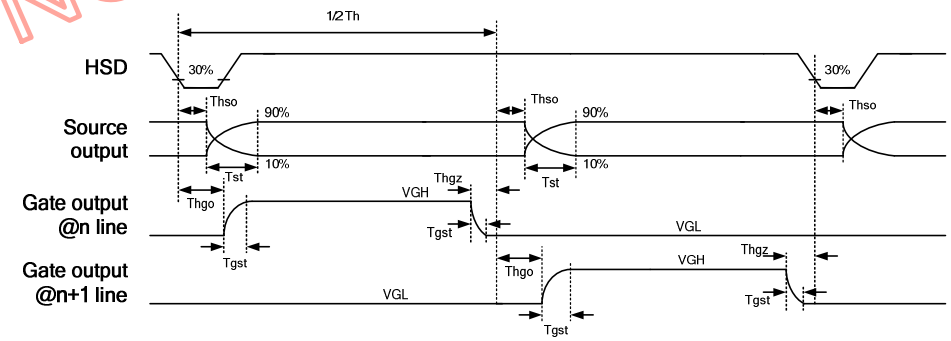
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Time that the HSD to Source output	Thso	-	3.5	-	CLKIN	
Time that the HSD to Gate output	Thgo	-	16.5	-	CLKIN	
Time that the HSD to Gate output off	Thgz	-	4.5	-	CLKIN	

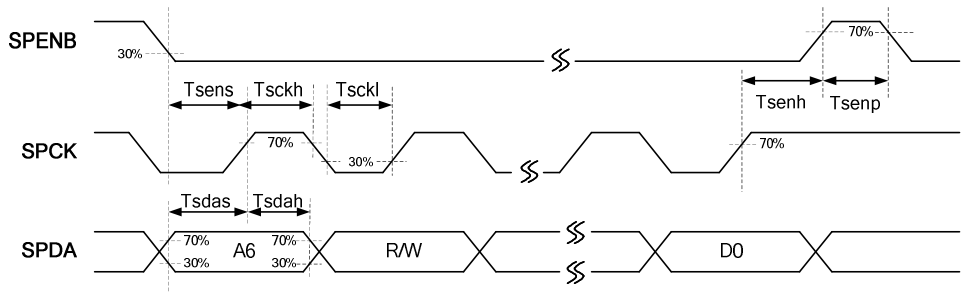
Timing Diagram





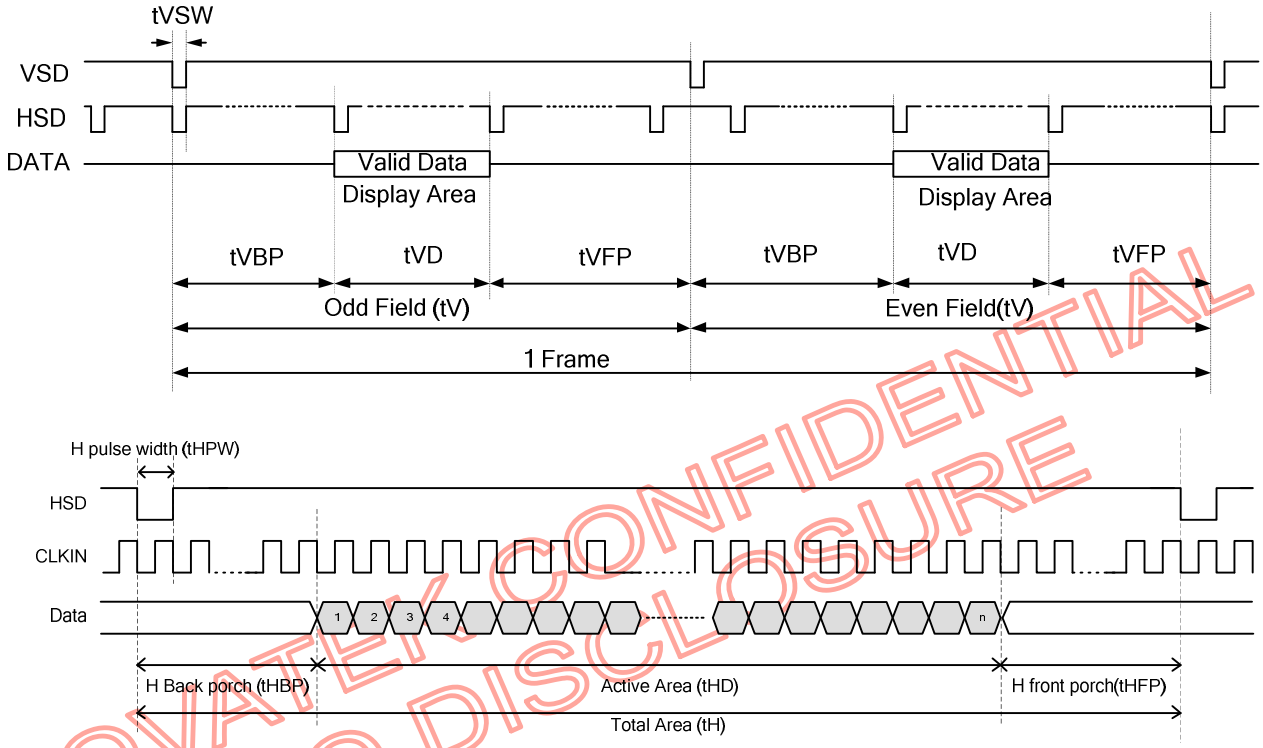






Input timing format

8-bit RGB/8-bit Dummy RGB/YUV /Parallel RGB Input timing chart



8-bit RGB input timing

Parameter		Symbol	Interlace			Unit
			Min.	Typ.	Max.	
CLKIN frequency		fCLKIN	13.5	27	27.19	MHz
HSD period		tH	1024	1716	1728	CLKIN
HSD display period		tHD		960		CLKIN
HSD back porch		tHBP	50	70	255	CLKIN
HSD front porch		tHFP	14	686	718	CLKIN
HSD pulse width		tHSW	1	1	tHBP-1	CLKIN
VSD period time		tV	242.5	262.5	450.5	H
Vertical display area		tVD		240		H
VSD back porch	Odd field	tVBP	1	21	31	H
	Even field		1.5	21.5	31.5	
VSD front porch	Odd field	tVFP	1.5	1.5	179.5	H
	Even field		1	1	179	
VSD pulse width		tVSW	1	1	6H	H
1 Frame			485	525	901	H

8-bit Dummy RGB input timing

8-bit Dummy RGB (320 mode/NTSC/24.535Mhz) input timing

Parameter		Symbol	Interlace			Unit
			Min.	Typ.	Max.	
CLKIN frequency		fCLKIN	20.45	24.535	30	MHz
HSD period		tH	1306	1560	1907	CLKIN
HSD display period		tHD		1280		CLKIN
HSD back porch		tHBP	3	241	255	CLKIN
HSD front porch		tHFP	25	39	372	CLKIN
HSD pulse width		tHSW	1	1	200	CLKIN
VSD period time		tV	242.5	262.5	450.5	H
Vertical display area		tVD		240		H
VSD back porch	Odd field	tVBP	1	21	31	H
	Even field		1.5	21.5	31.5	
VSD front porch	Odd field	tVFP	1.5	1.5	179.5	H
	Even field		1	1	179	
VSD pulse width		tVSW	1	1	6	H
1 Frame			485	525	901	H

8-bit Dummy RGB (320 mode/PAL/24.375Mhz) input timing

Parameter		Symbol	Interlace			Unit
			Min.	Typ.	Max.	
CLKIN frequency		fCLKIN	20.45	24.375	30	MHz
HSD period		tH	1306	1560	1920	CLKIN
HSD display period		tHD		1280		CLKIN
HSD back porch		tHBP	3	241	255	CLKIN
HSD front porch		tHFP	25	39	385	CLKIN
HSD pulse width		tHSW	1	1	200	CLKIN
VSD period time		tV	292.5	312.5	450.5	H
Vertical display area		tVD		288		H
VSD back porch	Odd field	tVBP	3	23	34	H
	Even field		3.5	23.5	34.5	
VSD front porch	Odd field	tVFP	1.5	1.5	128.5	H
	Even field		1	1	128	
VSD pulse width		tVSW	1	1	6	H
1 Frame			585	625	901	H

8-bit Dummy RGB (360 mode/NTSC/27Mhz) input timing

Parameter		Symbol	Interlace			Unit
			Min.	Typ.	Max.	
CLKIN frequency		fCLKIN	23	27	30	MHz
HSD period		tH	1466	1716	1907	CLKIN
HSD display period		tHD		1440		CLKIN
HSD back porch		tHBP	3	241	255	CLKIN
HSD front porch		tHFP	25	35	212	CLKIN
HSD pulse width		tHSW	1	1	200	CLKIN
VSD period time		tV	242.5	262.5	450.5	H
Vertical display area		tVD		240		H
VSD back porch	Odd field	tVBP	1	21	31	H
	Even field		1.5	21.5	31.5	
VSD front porch	Odd field	tVFP	1.5	1.5	179.5	H
	Even field		1	1	179	
VSD pulse width		tVSW	1	1	6	H
1 Frame			485	525	901	H

8-bit Dummy RGB (360 mode/PAL/27Mhz) input timing

Parameter		Symbol	Interlace			Unit
			Min.	Typ.	Max.	
CLKIN frequency		fCLKIN	23	27	30	MHz
HSD period		tH	1466	1728	1920	CLKIN
HSD display period		tHD		1440		CLKIN
HSD back porch		tHBP	3	241	255	CLKIN
HSD front porch		tHFP	25	47	225	CLKIN
HSD pulse width		tHSW	1	1	200	CLKIN
VSD period time		tV	292.5	312.5	450.5	H
Vertical display area		tVD		288		H
VSD back porch	Odd field	tVBP	3	23	34	H
	Even field		3.5	23.5	34.5	
VSD Front porch	Odd field	tVFP	1.5	1.5	128.5	H
	Even field		1	1	128	
VSD pulse width		tVSW	1	1	6	H
1 Frame			585	625	901	H

YUV720 and YUV640 input timing

YUV 720 mode/NTSC input timing

Parameter		Symbol	Interlace			Unit
			Min.	Typ.	Max.	
CLKIN frequency		fCLKIN	-	27	-	MHz
HSD period		tH	-	1716	-	CLKIN
HSD display period		tHD		1440		CLKIN
HSD back porch		tHBP	-	240	-	CLKIN
HSD front porch		tHFP	-	36	-	CLKIN
HSD pulse width		tHSW	-	1	-	CLKIN
VSD period time		tV	-	262.5	-	H
Vertical display area		tVD		240		H
VSD back porch	Odd field	tVBP	-	21	-	H
	Even field		-	21.5	-	
VSD front porch	Odd field	tVFP	-	1.5	-	H
	Even field		-	1	-	
VSD pulse width		tVSW	-	1	6	H
1 Frame			-	525	-	H

YUV 720 mode/PAL input timing

Parameter		Symbol	Interlace			Unit
			Min.	Typ.	Max.	
CLKIN frequency		fCLKIN	-	27	-	MHz
HSD period		tH	-	1728	-	CLKIN
HSD display period		tHD		1440		CLKIN
HSD back porch		tHBP	-	240	-	CLKIN
HSD front porch		tHFP	-	48	-	CLKIN
HSD pulse width		tHSW	-	1	-	CLKIN
VSD period time		tV	-	312.5	-	H
Vertical display area		tVD		288		H
VSD back porch	Odd field	tVBP	-	24	-	H
	Even field		-	24.5	-	
VSD front porch	Odd field	tVFP	-	0.5	-	H
	Even field		-	0	-	
VSD pulse width		tVSW	-	1	6	H
1 Frame			-	625	-	H

YUV 640 mode/NTSC input timing

Parameter		Symbol	Interlace			Unit
			Min.	Typ.	Max.	
CLKIN frequency		fCLKIN	-	24.535	-	MHz
HSD period		tH	-	1560	-	CLKIN
HSD display period		tHD		1280		CLKIN
HSD back porch		tHBP	-	240	-	CLKIN
HSD front porch		tHFP	-	40	-	CLKIN
HSD pulse width		tHSW	-	1	-	CLKIN
VSD period time		tV	-	262.5	-	H
Vertical display area		tVD		240		H
VSD back porch	Odd field	tVBP	-	21	-	H
	Even field		-	21.5	-	
VSD front porch	Odd field	tVFP	-	1.5	-	H
	Even field		-	1	-	
VSD pulse width		tVSW	-	1	6	H
1 Frame			-	525	-	H

YUV 640 mode/PAL input timing

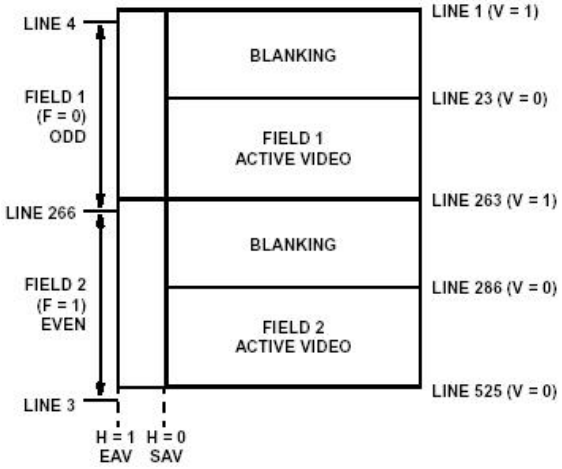
Parameter		Symbol	Interlace			Unit
			Min.	Typ.	Max.	
CLKIN frequency		fCLKIN	-	24.375	-	MHz
HSD period		tH	-	1560	-	CLKIN
HSD display period		tHD		1280		CLKIN
HSD back porch		tHBP	-	240	-	CLKIN
HSD front porch		tHFP	-	40	-	CLKIN
HSD pulse width		tHSW	-	1	-	CLKIN
VSD period time		tV	-	312.5	-	H
Vertical display area		tVD		288		H
VSD back porch	Odd field	tVBP	-	24	-	H
	Even field		-	24.5	-	
VSD front porch	Odd field	tVFP	-	0.5	-	H
	Even field		-	0	-	
VSD pulse width		tVSW	-	1	6	H
1 Frame			-	625	-	H

Parallel RGB Input Timing

Parameter		Symbol	Interlace			Unit
			Min.	Typ.	Max.	
CLKIN frequency		fCLKIN	-	6.2	7.5	MHz
HSD period		tH	-	390	-	CLKIN
HSD display period		tHD		320		CLKIN
HSD back porch		tHBP	40	61	-	CLKIN
HSD front porch		tHFP	-	9	-	CLKIN
HSD pulse width		tHSW	-	1	-	CLKIN
VSD period time		tV	-	262.5	-	H
Vertical display area		tVD		240		H
VSD back porch	Odd field	tVBP	-	21	-	H
	Even field		-	21.5	-	
VSD front porch	Odd field	tVFP	-	1.5	-	H
	Even field		-	1	-	
VSD pulse width		tVSW	-	1	6	H
1 Frame			-	525	-	H

CCIR656 vertical input timing

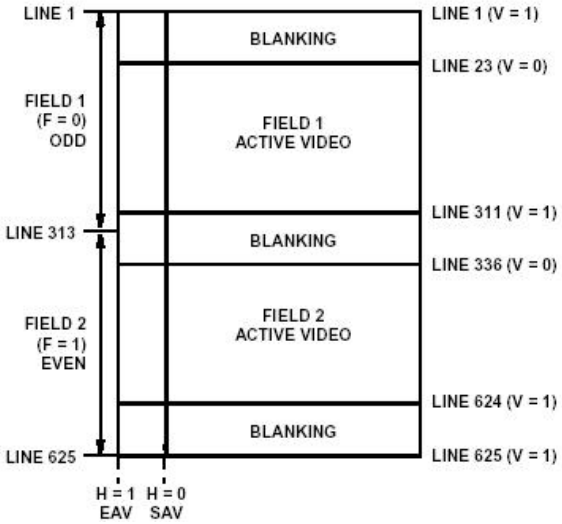
NTSC mode



LINE NUMBER	F	V	H (EAV)	H (SAV)
1-3	1	1	1	0
4-22	0	1	1	0
23-262	0	0	1	0
263-265	0	1	1	0
266-285	1	1	1	0
286-525	1	0	1	0

	F	H	V
1	EVEN Field	EAV	BLANKING
0	ODD Field	SAV	ACTIVE VIDEO

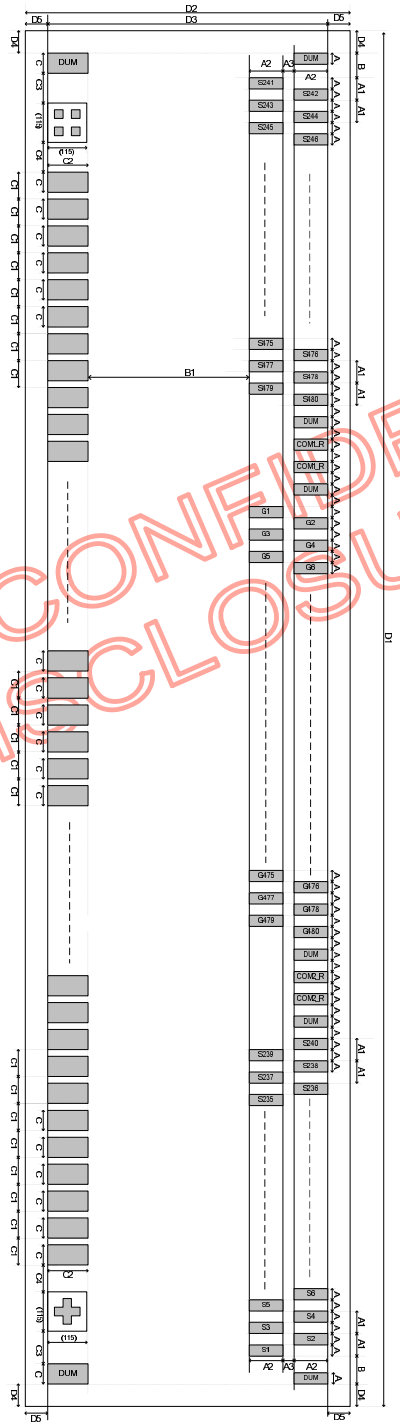
PAL mode



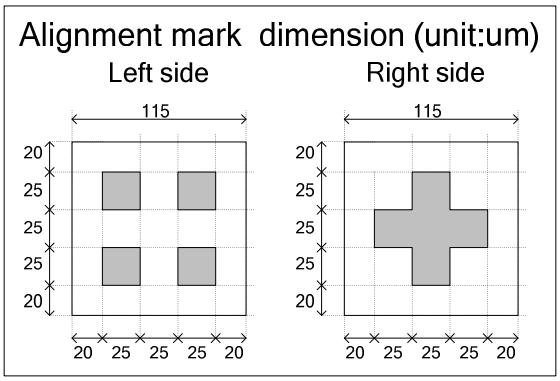
LINE NUMBER	F	V	H (EAV)	H (SAV)
1-22	0	1	1	0
23-310	0	0	1	0
311-312	0	1	1	0
313-335	1	1	1	0
336-623	1	0	1	0
624-625	1	1	1	0

	F	H	V
1	EVEN Field	EAV	BLANKING
0	ODD Field	SAV	ACTIVE VIDEO

Pad Outline Dimension (Bumper Side)



Alignment Mark Dimension



Pad outline dimension table

Symbol	Dimension (um)	Symbol	Dimension (um)
A	17	C	70
A1	34	C1	90
A2	115	C2	120
A3	30	C3	33
		C4	33
B	28		
B1	252	D1	16800 (MAX)
		D2	750 (MAX)
		D3	632
		D4	59
		D5	59

Appendix A: Pad Coordinate

Num	Pad Name	CX	CY
1	SHIELDING1	-8306	-256
2	COM1_L	-8055	-256
3	COM1_L	-7965	-256
4	COM1_L	-7875	-256
5	SHIELDING2	-7785	-256
6	VPP_MTP	-7695	-256
7	VPP_MTP	-7605	-256
8	VPP_MTP	-7515	-256
9	VPP_MTP	-7425	-256
10	STBYB	-7335	-256
11	STBYB	-7245	-256
12	RSTB	-7155	-256
13	RSTB	-7065	-256
14	CHNSL	-6975	-256
15	CHNSL	-6885	-256
16	PSEL	-6795	-256
17	PSEL	-6705	-256
18	SPENB	-6615	-256
19	SPENB	-6525	-256
20	SPDA	-6435	-256
21	SPDA	-6345	-256
22	SPCK	-6255	-256
23	SPCK	-6165	-256
24	DEN	-6075	-256
25	DEN	-5985	-256
26	HSD	-5895	-256
27	HSD	-5805	-256
28	VSD	-5715	-256
29	VSD	-5625	-256
30	CLKIN	-5535	-256
31	CLKIN	-5445	-256
32	DB7	-5355	-256
33	DB7	-5265	-256
34	DB6	-5175	-256
35	DB6	-5085	-256
36	DB5	-4995	-256
37	DB5	-4905	-256
38	DB4	-4815	-256
39	DB4	-4725	-256
40	DB3	-4635	-256
41	DB3	-4545	-256
42	DB2	-4455	-256
43	DB2	-4365	-256
44	DB1	-4275	-256
45	DB1	-4185	-256
46	DB0	-4095	-256
47	DB0	-4005	-256
48	DG7	-3915	-256
49	DG7	-3825	-256
50	DG6	-3735	-256
51	DG6	-3645	-256
52	DG5	-3555	-256
53	DG5	-3465	-256
54	DG4	-3375	-256
55	DG4	-3285	-256
56	DG3	-3195	-256
57	DG3	-3105	-256
58	DG2	-3015	-256
59	DG2	-2925	-256
60	DG1	-2835	-256
61	DG1	-2745	-256
62	DG0	-2655	-256
63	DG0	-2565	-256
64	DR7	-2475	-256
65	DR7	-2385	-256
66	DR6	-2295	-256
67	DR6	-2205	-256
68	DR5	-2115	-256
69	DR5	-2025	-256
70	DR4	-1935	-256
71	DR4	-1845	-256
72	DR3	-1755	-256
73	DR3	-1665	-256
74	DR2	-1575	-256
75	DR2	-1485	-256
76	DR1	-1395	-256
77	DR1	-1305	-256
78	DR0	-1215	-256
79	DR0	-1125	-256
80	GND	-1035	-256
81	GND	-945	-256
82	GND	-855	-256
83	GND	-765	-256
84	VDD	-675	-256
85	VDD	-585	-256
86	VDD	-495	-256
87	AVDD	-405	-256
88	AVDD	-315	-256
89	AVDD	-225	-256
90	VDDIO	-135	-256
91	VDDIO	-45	-256
92	VDDIO	45	-256
93	DVDD	135	-256
94	DVDD	225	-256
95	DVDD	315	-256
96	CP1P	405	-256
97	CP1P	495	-256
98	CP1P	585	-256
99	CP1M	675	-256
100	CP1M	765	-256
101	CP1M	855	-256
102	CP5P	945	-256
103	CP5P	1035	-256
104	CP5P	1125	-256
105	CP5M	1215	-256
106	CP5M	1305	-256
107	CP5M	1395	-256
108	CP2P	1485	-256
109	CP2P	1575	-256
110	CP2P	1665	-256
111	CP2M	1755	-256
112	CP2M	1845	-256
113	CP2M	1935	-256
114	VINT1	2025	-256
115	VINT1	2115	-256
116	VINT1	2205	-256
117	CP3P	2295	-256
118	CP3P	2385	-256
119	CP3P	2475	-256
120	CP3M	2565	-256
121	CP3M	2655	-256
122	CP3M	2745	-256
123	VINT2	2835	-256
124	VINT2	2925	-256
125	VINT2	3015	-256
126	VINT3	3105	-256
127	VINT3	3195	-256
128	VINT3	3285	-256
129	CP4P	3375	-256
130	CP4P	3465	-256
131	CP4P	3555	-256
132	CP4M	3645	-256
133	CP4M	3735	-256
134	CP4M	3825	-256
135	VGH	3915	-256
136	VGH	4005	-256
137	VGH	4095	-256
138	VGL	4185	-256
139	VGL	4275	-256
140	VGL	4365	-256
141	AGND	4455	-256
142	AGND	4545	-256
143	AGND	4635	-256
144	SHIELDING3	4725	-256
145	FRP	4815	-256
146	FRP	4905	-256
147	FRP	4995	-256
148	VCOMDC	5085	-256
149	VCOMDC	5175	-256
150	VCAC	5265	-256
151	VCAC	5355	-256
152	VCAC	5445	-256
153	SHIELDING4	5535	-256
154	DRV	5625	-256
155	DRV	5715	-256
156	FB_N	5805	-256
157	FB_N	5895	-256
158	FB_P	5985	-256
159	FB_P	6075	-256
160	FB	6165	-256
161	FB	6255	-256
162	TEST3	6345	-256
163	TEST2	6435	-256
164	TEST1	6525	-256
165	TEST0	6615	-256
166	T_O3	6705	-256
167	T_O2	6795	-256
168	T_O1	6885	-256
169	T_O0	6975	-256
170	T_IO7	7065	-256
171	T_IO6	7155	-256
172	T_IO5	7245	-256
173	T_IO4	7335	-256
174	T_IO3	7425	-256
175	T_IO2	7515	-256
176	T_IO1	7605	-256
177	T_IO0	7695	-256
178	SHIELDING5	7785	-256
179	COM2_L	7875	-256
180	COM2_L	7965	-256

Num	Pad Name	CX	CY
181	COM2_L	8055	-256
182	SHIELDING6	8306	-256
183	SHIELDING7	8332.5	258.5
184	S_1	8304.5	113.5
185	S_2	8287.5	258.5
186	S_3	8270.5	113.5
187	S_4	8253.5	258.5
188	S_5	8236.5	113.5
189	S_6	8219.5	258.5
190	S_7	8202.5	113.5
191	S_8	8185.5	258.5
192	S_9	8168.5	113.5
193	S_10	8151.5	258.5
194	S_11	8134.5	113.5
195	S_12	8117.5	258.5
196	S_13	8100.5	113.5
197	S_14	8083.5	258.5
198	S_15	8066.5	113.5
199	S_16	8049.5	258.5
200	S_17	8032.5	113.5
201	S_18	8015.5	258.5
202	S_19	7998.5	113.5
203	S_20	7981.5	258.5
204	S_21	7964.5	113.5
205	S_22	7947.5	258.5
206	S_23	7930.5	113.5
207	S_24	7913.5	258.5
208	S_25	7896.5	113.5
209	S_26	7879.5	258.5
210	S_27	7862.5	113.5
211	S_28	7845.5	258.5
212	S_29	7828.5	113.5
213	S_30	7811.5	258.5
214	S_31	7794.5	113.5
215	S_32	7777.5	258.5
216	S_33	7760.5	113.5
217	S_34	7743.5	258.5
218	S_35	7726.5	113.5
219	S_36	7709.5	258.5
220	S_37	7692.5	113.5
221	S_38	7675.5	258.5
222	S_39	7658.5	113.5
223	S_40	7641.5	258.5
224	S_41	7624.5	113.5
225	S_42	7607.5	258.5
226	S_43	7590.5	113.5
227	S_44	7573.5	258.5
228	S_45	7556.5	113.5
229	S_46	7539.5	258.5
230	S_47	7522.5	113.5
231	S_48	7505.5	258.5
232	S_49	7488.5	113.5
233	S_50	7471.5	258.5
234	S_51	7454.5	113.5
235	S_52	7437.5	258.5
236	S_53	7420.5	113.5
237	S_54	7403.5	258.5
238	S_55	7386.5	113.5
239	S_56	7369.5	258.5
240	S_57	7352.5	113.5
241	S_58	7335.5	258.5
242	S_59	7318.5	113.5
243	S_60	7301.5	258.5
244	S_61	7284.5	113.5
245	S_62	7267.5	258.5
246	S_63	7250.5	113.5
247	S_64	7233.5	258.5
248	S_65	7216.5	113.5
249	S_66	7199.5	258.5
250	S_67	7182.5	113.5
251	S_68	7165.5	258.5
252	S_69	7148.5	113.5
253	S_70	7131.5	258.5
254	S_71	7114.5	113.5
255	S_72	7097.5	258.5
256	S_73	7080.5	113.5
257	S_74	7063.5	258.5
258	S_75	7046.5	113.5
259	S_76	7029.5	258.5
260	S_77	7012.5	113.5
261	S_78	6995.5	258.5
262	S_79	6978.5	113.5
263	S_80	6961.5	258.5
264	S_81	6944.5	113.5
265	S_82	6927.5	258.5
266	S_83	6910.5	113.5
267	S_84	6893.5	258.5
268	S_85	6876.5	113.5
269	S_86	6859.5	258.5
270	S_87	6842.5	113.5
271	S_88	6825.5	258.5
272	S_89	6808.5	113.5
273	S_90	6791.5	258.5
274	S_91	6774.5	113.5
275	S_92	6757.5	258.5
276	S_93	6740.5	113.5
277	S_94	6723.5	258.5
278	S_95	6706.5	113.5
279	S_96	6689.5	258.5
280	S_97	6672.5	113.5
281	S_98	6655.5	258.5
282	S_99	6638.5	113.5
283	S_100	6621.5	258.5
284	S_101	6604.5	113.5
285	S_102	6587.5	258.5
286	S_103	6570.5	113.5
287	S_104	6553.5	258.5
288	S_105	6536.5	113.5
289	S_106	6519.5	258.5
290	S_107	6502.5	113.5
291	S_108	6485.5	258.5
292	S_109	6468.5	113.5
293	S_110	6451.5	258.5
294	S_111	6434.5	113.5
295	S_112	6417.5	258.5
296	S_113	6400.5	113.5
297	S_114	6383.5	258.5
298	S_115	6366.5	113.5
299	S_116	6349.5	258.5
300	S_117	6332.5	113.5
301	S_118	6315.5	258.5
302	S_119	6298.5	113.5
303	S_120	6281.5	258.5
304	S_121	6264.5	113.5
305	S_122	6247.5	258.5
306	S_123	6230.5	113.5
307	S_124	6213.5	258.5
308	S_125	6196.5	113.5
309	S_126	6179.5	258.5
310	S_127	6162.5	113.5
311	S_128	6145.5	258.5
312	S_129	6128.5	113.5
313	S_130	6111.5	258.5
314	S_131	6094.5	113.5
315	S_132	6077.5	258.5
316	S_133	6060.5	113.5
317	S_134	6043.5	258.5
318	S_135	6026.5	113.5
319	S_136	6009.5	258.5
320	S_137	5992.5	113.5
321	S_138	5975.5	258.5
322	S_139	5958.5	113.5
323	S_140	5941.5	258.5
324	S_141	5924.5	113.5
325	S_142	5907.5	258.5
326	S_143	5890.5	113.5
327	S_144	5873.5	258.5
328	S_145	5856.5	113.5
329	S_146	5839.5	258.5
330	S_147	5822.5	113.5
331	S_148	5805.5	258.5
332	S_149	5788.5	113.5
333	S_150	5771.5	258.5
334	S_151	5754.5	113.5
335	S_152	5737.5	258.5
336	S_153	5720.5	113.5
337	S_154	5703.5	258.5
338	S_155	5686.5	113.5
339	S_156	5669.5	258.5
340	S_157	5652.5	113.5
341	S_158	5635.5	258.5
342	S_159	5618.5	113.5
343	S_160	5601.5	258.5
344	S_161	5584.5	113.5
345	S_162	5567.5	258.5
346	S_163	5550.5	113.5
347	S_164	5533.5	258.5
348	S_165	5516.5	113.5
349	S_166	5499.5	258.5
350	S_167	5482.5	113.5
351	S_168	5465.5	258.5
352	S_169	5448.5	113.5
353	S_170	5431.5	258.5
354	S_171	5414.5	113.5
355	S_172	5397.5	258.5
356	S_173	5380.5	113.5
357	S_174	5363.5	258.5
358	S_175	5346.5	113.5
359	S_176	5329.5	258.5
360	S_177	5312.5	113.5
361	S_178	5295.5	258.5
362	S_179	5278.5	113.5
363	S_180	5261.5	258.5
364	S_181	5244.5	113.5
365	S_182	5227.5	258.5
366	S_183	5210.5	113.5
367	S_184	5193.5	258.5
368	S_185	5176.5	113.5
369	S_186	5159.5	258.5
370	S_187	5142.5	113.5
371	S_188	5125.5	258.5
372	S_189	5108.5	113.5

Num	Pad Name	CX	CY
373	S_190	5091.5	258.5
374	S_191	5074.5	113.5
375	S_192	5057.5	258.5
376	S_193	5040.5	113.5
377	S_194	5023.5	258.5
378	S_195	5006.5	113.5
379	S_196	4989.5	258.5
380	S_197	4972.5	113.5
381	S_198	4955.5	258.5
382	S_199	4938.5	113.5
383	S_200	4921.5	258.5
384	S_201	4904.5	113.5
385	S_202	4887.5	258.5
386	S_203	4870.5	113.5
387	S_204	4853.5	258.5
388	S_205	4836.5	113.5
389	S_206	4819.5	258.5
390	S_207	4802.5	113.5
391	S_208	4785.5	258.5
392	S_209	4768.5	113.5
393	S_210	4751.5	258.5
394	S_211	4734.5	113.5
395	S_212	4717.5	258.5
396	S_213	4700.5	113.5
397	S_214	4683.5	258.5
398	S_215	4666.5	113.5
399	S_216	4649.5	258.5
400	S_217	4632.5	113.5
401	S_218	4615.5	258.5
402	S_219	4598.5	113.5
403	S_220	4581.5	258.5
404	S_221	4564.5	113.5
405	S_222	4547.5	258.5
406	S_223	4530.5	113.5
407	S_224	4513.5	258.5
408	S_225	4496.5	113.5
409	S_226	4479.5	258.5
410	S_227	4462.5	113.5
411	S_228	4445.5	258.5
412	S_229	4428.5	113.5
413	S_230	4411.5	258.5
414	S_231	4394.5	113.5
415	S_232	4377.5	258.5
416	S_233	4360.5	113.5
417	S_234	4343.5	258.5
418	S_235	4326.5	113.5
419	S_236	4309.5	258.5
420	S_237	4292.5	113.5
421	S_238	4275.5	258.5
422	S_239	4258.5	113.5
423	S_240	4241.5	258.5
424	SHIELDING8	4207.5	258.5
425	COM2_R	4173.5	258.5
426	COM2_R	4139.5	258.5
427	SHIELDING9	4105.5	258.5
428	G_480	4071.5	258.5
429	G_479	4054.5	113.5
430	G_478	4037.5	258.5
431	G_477	4020.5	113.5
432	G_476	4003.5	258.5
433	G_475	3986.5	113.5
434	G_474	3969.5	258.5
435	G_473	3952.5	113.5
436	G_472	3935.5	258.5
437	G_471	3918.5	113.5
438	G_470	3901.5	258.5
439	G_469	3884.5	113.5
440	G_468	3867.5	258.5
441	G_467	3850.5	113.5
442	G_466	3833.5	258.5
443	G_465	3816.5	113.5
444	G_464	3799.5	258.5
445	G_463	3782.5	113.5
446	G_462	3765.5	258.5
447	G_461	3748.5	113.5
448	G_460	3731.5	258.5
449	G_459	3714.5	113.5
450	G_458	3697.5	258.5
451	G_457	3680.5	113.5
452	G_456	3663.5	258.5
453	G_455	3646.5	113.5
454	G_454	3629.5	258.5
455	G_453	3612.5	113.5
456	G_452	3595.5	258.5
457	G_451	3578.5	113.5
458	G_450	3561.5	258.5
459	G_449	3544.5	113.5
460	G_448	3527.5	258.5
461	G_447	3510.5	113.5
462	G_446	3493.5	258.5
463	G_445	3476.5	113.5
464	G_444	3459.5	258.5
465	G_443	3442.5	113.5
466	G_442	3425.5	258.5
467	G_441	3408.5	113.5
468	G_440	3391.5	258.5
469	G_439	3374.5	113.5
470	G_438	3357.5	258.5
471	G_437	3340.5	113.5
472	G_436	3323.5	258.5
473	G_435	3306.5	113.5
474	G_434	3289.5	258.5
475	G_433	3272.5	113.5
476	G_432	3255.5	258.5
477	G_431	3238.5	113.5
478	G_430	3221.5	258.5
479	G_429	3204.5	113.5
480	G_428	3187.5	258.5
481	G_427	3170.5	113.5
482	G_426	3153.5	258.5
483	G_425	3136.5	113.5
484	G_424	3119.5	258.5
485	G_423	3102.5	113.5
486	G_422	3085.5	258.5
487	G_421	3068.5	113.5
488	G_420	3051.5	258.5
489	G_419	3034.5	113.5
490	G_418	3017.5	258.5
491	G_417	3000.5	113.5
492	G_416	2983.5	258.5
493	G_415	2966.5	113.5
494	G_414	2949.5	258.5
495	G_413	2932.5	113.5
496	G_412	2915.5	258.5
497	G_411	2898.5	113.5
498	G_410	2881.5	258.5
499	G_409	2864.5	113.5
500	G_408	2847.5	258.5
501	G_407	2830.5	113.5
502	G_406	2813.5	258.5
503	G_405	2796.5	113.5
504	G_404	2779.5	258.5
505	G_403	2762.5	113.5
506	G_402	2745.5	258.5
507	G_401	2728.5	113.5
508	G_400	2711.5	258.5
509	G_399	2694.5	113.5
510	G_398	2677.5	258.5
511	G_397	2660.5	113.5
512	G_396	2643.5	258.5
513	G_395	2626.5	113.5
514	G_394	2609.5	258.5
515	G_393	2592.5	113.5
516	G_392	2575.5	258.5
517	G_391	2558.5	113.5
518	G_390	2541.5	258.5
519	G_389	2524.5	113.5
520	G_388	2507.5	258.5
521	G_387	2490.5	113.5
522	G_386	2473.5	258.5
523	G_385	2456.5	113.5
524	G_384	2439.5	258.5
525	G_383	2422.5	113.5
526	G_382	2405.5	258.5
527	G_381	2388.5	113.5
528	G_380	2371.5	258.5
529	G_379	2354.5	113.5
530	G_378	2337.5	258.5
531	G_377	2320.5	113.5
532	G_376	2303.5	258.5
533	G_375	2286.5	113.5
534	G_374	2269.5	258.5
535	G_373	2252.5	113.5
536	G_372	2235.5	258.5
537	G_371	2218.5	113.5
538	G_370	2201.5	258.5
539	G_369	2184.5	113.5
540	G_368	2167.5	258.5
541	G_367	2150.5	113.5
542	G_366	2133.5	258.5
543	G_365	2116.5	113.5
544	G_364	2099.5	258.5
545	G_363	2082.5	113.5
546	G_362	2065.5	258.5
547	G_361	2048.5	113.5
548	G_360	2031.5	258.5
549	G_359	2014.5	113.5
550	G_358	1997.5	258.5
551	G_357	1980.5	113.5
552	G_356	1963.5	258.5
553	G_355	1946.5	113.5
554	G_354	1929.5	258.5
555	G_353	1912.5	113.5
556	G_352	1895.5	258.5
557	G_351	1878.5	113.5
558	G_350	1861.5	258.5
559	G_349	1844.5	113.5
560	G_348	1827.5	258.5
561	G_347	1810.5	113.5
562	G_346	1793.5	258.5
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564	G_344	1759.5	258.5

Num	Pad Name	CX	CY
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568	G_340	1691.5	258.5
569	G_339	1674.5	113.5
570	G_338	1657.5	258.5
571	G_337	1640.5	113.5
572	G_336	1623.5	258.5
573	G_335	1606.5	113.5
574	G_334	1589.5	258.5
575	G_333	1572.5	113.5
576	G_332	1555.5	258.5
577	G_331	1538.5	113.5
578	G_330	1521.5	258.5
579	G_329	1504.5	113.5
580	G_328	1487.5	258.5
581	G_327	1470.5	113.5
582	G_326	1453.5	258.5
583	G_325	1436.5	113.5
584	G_324	1419.5	258.5
585	G_323	1402.5	113.5
586	G_322	1385.5	258.5
587	G_321	1368.5	113.5
588	G_320	1351.5	258.5
589	G_319	1334.5	113.5
590	G_318	1317.5	258.5
591	G_317	1300.5	113.5
592	G_316	1283.5	258.5
593	G_315	1266.5	113.5
594	G_314	1249.5	258.5
595	G_313	1232.5	113.5
596	G_312	1215.5	258.5
597	G_311	1198.5	113.5
598	G_310	1181.5	258.5
599	G_309	1164.5	113.5
600	G_308	1147.5	258.5
601	G_307	1130.5	113.5
602	G_306	1113.5	258.5
603	G_305	1096.5	113.5
604	G_304	1079.5	258.5
605	G_303	1062.5	113.5
606	G_302	1045.5	258.5
607	G_301	1028.5	113.5
608	G_300	1011.5	258.5
609	G_299	994.5	113.5
610	G_298	977.5	258.5
611	G_297	960.5	113.5
612	G_296	943.5	258.5
613	G_295	926.5	113.5
614	G_294	909.5	258.5
615	G_293	892.5	113.5
616	G_292	875.5	258.5
617	G_291	858.5	113.5
618	G_290	841.5	258.5
619	G_289	824.5	113.5
620	G_288	807.5	258.5
621	G_287	790.5	113.5
622	G_286	773.5	258.5
623	G_285	756.5	113.5
624	G_284	739.5	258.5
625	G_283	722.5	113.5
626	G_282	705.5	258.5
627	G_281	688.5	113.5
628	G_280	671.5	258.5
629	G_279	654.5	113.5
630	G_278	637.5	258.5
631	G_277	620.5	113.5
632	G_276	603.5	258.5
633	G_275	586.5	113.5
634	G_274	569.5	258.5
635	G_273	552.5	113.5
636	G_272	535.5	258.5
637	G_271	518.5	113.5
638	G_270	501.5	258.5
639	G_269	484.5	113.5
640	G_268	467.5	258.5
641	G_267	450.5	113.5
642	G_266	433.5	258.5
643	G_265	416.5	113.5
644	G_264	399.5	258.5
645	G_263	382.5	113.5
646	G_262	365.5	258.5
647	G_261	348.5	113.5
648	G_260	331.5	258.5
649	G_259	314.5	113.5
650	G_258	297.5	258.5
651	G_257	280.5	113.5
652	G_256	263.5	258.5
653	G_255	246.5	113.5
654	G_254	229.5	258.5
655	G_253	212.5	113.5
656	G_252	195.5	258.5
657	G_251	178.5	113.5
658	G_250	161.5	258.5
659	G_249	144.5	113.5
660	G_248	127.5	258.5
661	G_247	110.5	113.5
662	G_246	93.5	258.5
663	G_245	76.5	113.5
664	G_244	59.5	258.5
665	G_243	42.5	113.5
666	G_242	25.5	258.5
667	G_241	8.5	113.5
668	G_240	-8.5	258.5
669	G_239	-25.5	113.5
670	G_238	-42.5	258.5
671	G_237	-59.5	113.5
672	G_236	-76.5	258.5
673	G_235	-93.5	113.5
674	G_234	-110.5	258.5
675	G_233	-127.5	113.5
676	G_232	-144.5	258.5
677	G_231	-161.5	113.5
678	G_230	-178.5	258.5
679	G_229	-195.5	113.5
680	G_228	-212.5	258.5
681	G_227	-229.5	113.5
682	G_226	-246.5	258.5
683	G_225	-263.5	113.5
684	G_224	-280.5	258.5
685	G_223	-297.5	113.5
686	G_222	-314.5	258.5
687	G_221	-331.5	113.5
688	G_220	-348.5	258.5
689	G_219	-365.5	113.5
690	G_218	-382.5	258.5
691	G_217	-399.5	113.5
692	G_216	-416.5	258.5
693	G_215	-433.5	113.5
694	G_214	-450.5	258.5
695	G_213	-467.5	113.5
696	G_212	-484.5	258.5
697	G_211	-501.5	113.5
698	G_210	-518.5	258.5
699	G_209	-535.5	113.5
700	G_208	-552.5	258.5
701	G_207	-569.5	113.5
702	G_206	-586.5	258.5
703	G_205	-603.5	113.5
704	G_204	-620.5	258.5
705	G_203	-637.5	113.5
706	G_202	-654.5	258.5
707	G_201	-671.5	113.5
708	G_200	-688.5	258.5
709	G_199	-705.5	113.5
710	G_198	-722.5	258.5
711	G_197	-739.5	113.5
712	G_196	-756.5	258.5
713	G_195	-773.5	113.5
714	G_194	-790.5	258.5
715	G_193	-807.5	113.5
716	G_192	-824.5	258.5
717	G_191	-841.5	113.5
718	G_190	-858.5	258.5
719	G_189	-875.5	113.5
720	G_188	-892.5	258.5
721	G_187	-909.5	113.5
722	G_186	-926.5	258.5
723	G_185	-943.5	113.5
724	G_184	-960.5	258.5
725	G_183	-977.5	113.5
726	G_182	-994.5	258.5
727	G_181	-1011.5	113.5
728	G_180	-1028.5	258.5
729	G_179	-1045.5	113.5
730	G_178	-1062.5	258.5
731	G_177	-1079.5	113.5
732	G_176	-1096.5	258.5
733	G_175	-1113.5	113.5
734	G_174	-1130.5	258.5
735	G_173	-1147.5	113.5
736	G_172	-1164.5	258.5
737	G_171	-1181.5	113.5
738	G_170	-1198.5	258.5
739	G_169	-1215.5	113.5
740	G_168	-1232.5	258.5
741	G_167	-1249.5	113.5
742	G_166	-1266.5	258.5
743	G_165	-1283.5	113.5
744	G_164	-1300.5	258.5
745	G_163	-1317.5	113.5
746	G_162	-1334.5	258.5
747	G_161	-1351.5	113.5
748	G_160	-1368.5	258.5
749	G_159	-1385.5	113.5
750	G_158	-1402.5	258.5
751	G_157	-1419.5	113.5
752	G_156	-1436.5	258.5
753	G_155	-1453.5	113.5
754	G_154	-1470.5	258.5
755	G_153	-1487.5	113.5
756	G_152	-1504.5	258.5

Num	Pad Name	CX	CY
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758	G_150	-1538.5	258.5
759	G_149	-1555.5	113.5
760	G_148	-1572.5	258.5
761	G_147	-1589.5	113.5
762	G_146	-1606.5	258.5
763	G_145	-1623.5	113.5
764	G_144	-1640.5	258.5
765	G_143	-1657.5	113.5
766	G_142	-1674.5	258.5
767	G_141	-1691.5	113.5
768	G_140	-1708.5	258.5
769	G_139	-1725.5	113.5
770	G_138	-1742.5	258.5
771	G_137	-1759.5	113.5
772	G_136	-1776.5	258.5
773	G_135	-1793.5	113.5
774	G_134	-1810.5	258.5
775	G_133	-1827.5	113.5
776	G_132	-1844.5	258.5
777	G_131	-1861.5	113.5
778	G_130	-1878.5	258.5
779	G_129	-1895.5	113.5
780	G_128	-1912.5	258.5
781	G_127	-1929.5	113.5
782	G_126	-1946.5	258.5
783	G_125	-1963.5	113.5
784	G_124	-1980.5	258.5
785	G_123	-1997.5	113.5
786	G_122	-2014.5	258.5
787	G_121	-2031.5	113.5
788	G_120	-2048.5	258.5
789	G_119	-2065.5	113.5
790	G_118	-2082.5	258.5
791	G_117	-2099.5	113.5
792	G_116	-2116.5	258.5
793	G_115	-2133.5	113.5
794	G_114	-2150.5	258.5
795	G_113	-2167.5	113.5
796	G_112	-2184.5	258.5
797	G_111	-2201.5	113.5
798	G_110	-2218.5	258.5
799	G_109	-2235.5	113.5
800	G_108	-2252.5	258.5
801	G_107	-2269.5	113.5
802	G_106	-2286.5	258.5
803	G_105	-2303.5	113.5
804	G_104	-2320.5	258.5
805	G_103	-2337.5	113.5
806	G_102	-2354.5	258.5
807	G_101	-2371.5	113.5
808	G_100	-2388.5	258.5
809	G_99	-2405.5	113.5
810	G_98	-2422.5	258.5
811	G_97	-2439.5	113.5
812	G_96	-2456.5	258.5
813	G_95	-2473.5	113.5
814	G_94	-2490.5	258.5
815	G_93	-2507.5	113.5
816	G_92	-2524.5	258.5
817	G_91	-2541.5	113.5
818	G_90	-2558.5	258.5
819	G_89	-2575.5	113.5
820	G_88	-2592.5	258.5
821	G_87	-2609.5	113.5
822	G_86	-2626.5	258.5
823	G_85	-2643.5	113.5
824	G_84	-2660.5	258.5
825	G_83	-2677.5	113.5
826	G_82	-2694.5	258.5
827	G_81	-2711.5	113.5
828	G_80	-2728.5	258.5
829	G_79	-2745.5	113.5
830	G_78	-2762.5	258.5
831	G_77	-2779.5	113.5
832	G_76	-2796.5	258.5
833	G_75	-2813.5	113.5
834	G_74	-2830.5	258.5
835	G_73	-2847.5	113.5
836	G_72	-2864.5	258.5
837	G_71	-2881.5	113.5
838	G_70	-2898.5	258.5
839	G_69	-2915.5	113.5
840	G_68	-2932.5	258.5
841	G_67	-2949.5	113.5
842	G_66	-2966.5	258.5
843	G_65	-2983.5	113.5
844	G_64	-3000.5	258.5
845	G_63	-3017.5	113.5
846	G_62	-3034.5	258.5
847	G_61	-3051.5	113.5
848	G_60	-3068.5	258.5
849	G_59	-3085.5	113.5
850	G_58	-3102.5	258.5
851	G_57	-3119.5	113.5
852	G_56	-3136.5	258.5
853	G_55	-3153.5	113.5
854	G_54	-3170.5	258.5
855	G_53	-3187.5	113.5
856	G_52	-3204.5	258.5
857	G_51	-3221.5	113.5
858	G_50	-3238.5	258.5
859	G_49	-3255.5	113.5
860	G_48	-3272.5	258.5
861	G_47	-3289.5	113.5
862	G_46	-3306.5	258.5
863	G_45	-3323.5	113.5
864	G_44	-3340.5	258.5
865	G_43	-3357.5	113.5
866	G_42	-3374.5	258.5
867	G_41	-3391.5	113.5
868	G_40	-3408.5	258.5
869	G_39	-3425.5	113.5
870	G_38	-3442.5	258.5
871	G_37	-3459.5	113.5
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873	G_35	-3493.5	113.5
874	G_34	-3510.5	258.5
875	G_33	-3527.5	113.5
876	G_32	-3544.5	258.5
877	G_31	-3561.5	113.5
878	G_30	-3578.5	258.5
879	G_29	-3595.5	113.5
880	G_28	-3612.5	258.5
881	G_27	-3629.5	113.5
882	G_26	-3646.5	258.5
883	G_25	-3663.5	113.5
884	G_24	-3680.5	258.5
885	G_23	-3697.5	113.5
886	G_22	-3714.5	258.5
887	G_21	-3731.5	113.5
888	G_20	-3748.5	258.5
889	G_19	-3765.5	113.5
890	G_18	-3782.5	258.5
891	G_17	-3799.5	113.5
892	G_16	-3816.5	258.5
893	G_15	-3833.5	113.5
894	G_14	-3850.5	258.5
895	G_13	-3867.5	113.5
896	G_12	-3884.5	258.5
897	G_11	-3901.5	113.5
898	G_10	-3918.5	258.5
899	G_9	-3935.5	113.5
900	G_8	-3952.5	258.5
901	G_7	-3969.5	113.5
902	G_6	-3986.5	258.5
903	G_5	-4003.5	113.5
904	G_4	-4020.5	258.5
905	G_3	-4037.5	113.5
906	G_2	-4054.5	258.5
907	G_1	-4071.5	113.5
908	SHIELDING10	-4105.5	258.5
909	COM1_R	-4139.5	258.5
910	COM1_R	-4173.5	258.5
911	SHIELDING11	-4207.5	258.5
912	S_480	-4241.5	258.5
913	S_479	-4258.5	113.5
914	S_478	-4275.5	258.5
915	S_477	-4292.5	113.5
916	S_476	-4309.5	258.5
917	S_475	-4326.5	113.5
918	S_474	-4343.5	258.5
919	S_473	-4360.5	113.5
920	S_472	-4377.5	258.5
921	S_471	-4394.5	113.5
922	S_470	-4411.5	258.5
923	S_469	-4428.5	113.5
924	S_468	-4445.5	258.5
925	S_467	-4462.5	113.5
926	S_466	-4479.5	258.5
927	S_465	-4496.5	113.5
928	S_464	-4513.5	258.5
929	S_463	-4530.5	113.5
930	S_462	-4547.5	258.5
931	S_461	-4564.5	113.5
932	S_460	-4581.5	258.5
933	S_459	-4598.5	113.5
934	S_458	-4615.5	258.5
935	S_457	-4632.5	113.5
936	S_456	-4649.5	258.5
937	S_455	-4666.5	113.5
938	S_454	-4683.5	258.5
939	S_453	-4700.5	113.5
940	S_452	-4717.5	258.5
941	S_451	-4734.5	113.5
942	S_450	-4751.5	258.5
943	S_449	-4768.5	113.5
944	S_448	-4785.5	258.5
945	S_447	-4802.5	113.5
946	S_446	-4819.5	258.5
947	S_445	-4836.5	113.5
948	S_444	-4853.5	258.5

Num	Pad Name	CX	CY
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951	S_441	-4904.5	113.5
952	S_440	-4921.5	258.5
953	S_439	-4938.5	113.5
954	S_438	-4955.5	258.5
955	S_437	-4972.5	113.5
956	S_436	-4989.5	258.5
957	S_435	-5006.5	113.5
958	S_434	-5023.5	258.5
959	S_433	-5040.5	113.5
960	S_432	-5057.5	258.5
961	S_431	-5074.5	113.5
962	S_430	-5091.5	258.5
963	S_429	-5108.5	113.5
964	S_428	-5125.5	258.5
965	S_427	-5142.5	113.5
966	S_426	-5159.5	258.5
967	S_425	-5176.5	113.5
968	S_424	-5193.5	258.5
969	S_423	-5210.5	113.5
970	S_422	-5227.5	258.5
971	S_421	-5244.5	113.5
972	S_420	-5261.5	258.5
973	S_419	-5278.5	113.5
974	S_418	-5295.5	258.5
975	S_417	-5312.5	113.5
976	S_416	-5329.5	258.5
977	S_415	-5346.5	113.5
978	S_414	-5363.5	258.5
979	S_413	-5380.5	113.5
980	S_412	-5397.5	258.5
981	S_411	-5414.5	113.5
982	S_410	-5431.5	258.5
983	S_409	-5448.5	113.5
984	S_408	-5465.5	258.5
985	S_407	-5482.5	113.5
986	S_406	-5499.5	258.5
987	S_405	-5516.5	113.5
988	S_404	-5533.5	258.5
989	S_403	-5550.5	113.5
990	S_402	-5567.5	258.5
991	S_401	-5584.5	113.5
992	S_400	-5601.5	258.5
993	S_399	-5618.5	113.5
994	S_398	-5635.5	258.5
995	S_397	-5652.5	113.5
996	S_396	-5669.5	258.5
997	S_395	-5686.5	113.5
998	S_394	-5703.5	258.5
999	S_393	-5720.5	113.5
1000	S_392	-5737.5	258.5
1001	S_391	-5754.5	113.5
1002	S_390	-5771.5	258.5
1003	S_389	-5788.5	113.5
1004	S_388	-5805.5	258.5
1005	S_387	-5822.5	113.5
1006	S_386	-5839.5	258.5
1007	S_385	-5856.5	113.5
1008	S_384	-5873.5	258.5
1009	S_383	-5890.5	113.5
1010	S_382	-5907.5	258.5
1011	S_381	-5924.5	113.5
1012	S_380	-5941.5	258.5
1013	S_379	-5958.5	113.5
1014	S_378	-5975.5	258.5
1015	S_377	-5992.5	113.5
1016	S_376	-6009.5	258.5
1017	S_375	-6026.5	113.5
1018	S_374	-6043.5	258.5
1019	S_373	-6060.5	113.5
1020	S_372	-6077.5	258.5
1021	S_371	-6094.5	113.5
1022	S_370	-6111.5	258.5
1023	S_369	-6128.5	113.5
1024	S_368	-6145.5	258.5
1025	S_367	-6162.5	113.5
1026	S_366	-6179.5	258.5
1027	S_365	-6196.5	113.5
1028	S_364	-6213.5	258.5
1029	S_363	-6230.5	113.5
1030	S_362	-6247.5	258.5
1031	S_361	-6264.5	113.5
1032	S_360	-6281.5	258.5
1033	S_359	-6298.5	113.5
1034	S_358	-6315.5	258.5
1035	S_357	-6332.5	113.5
1036	S_356	-6349.5	258.5
1037	S_355	-6366.5	113.5
1038	S_354	-6383.5	258.5
1039	S_353	-6400.5	113.5
1040	S_352	-6417.5	258.5
1041	S_351	-6434.5	113.5
1042	S_350	-6451.5	258.5
1043	S_349	-6468.5	113.5
1044	S_348	-6485.5	258.5
1045	S_347	-6502.5	113.5
1046	S_346	-6519.5	258.5
1047	S_345	-6536.5	113.5
1048	S_344	-6553.5	258.5
1049	S_343	-6570.5	113.5
1050	S_342	-6587.5	258.5
1051	S_341	-6604.5	113.5
1052	S_340	-6621.5	258.5
1053	S_339	-6638.5	113.5
1054	S_338	-6655.5	258.5
1055	S_337	-6672.5	113.5
1056	S_336	-6689.5	258.5
1057	S_335	-6706.5	113.5
1058	S_334	-6723.5	258.5
1059	S_333	-6740.5	113.5
1060	S_332	-6757.5	258.5
1061	S_331	-6774.5	113.5
1062	S_330	-6791.5	258.5
1063	S_329	-6808.5	113.5
1064	S_328	-6825.5	258.5
1065	S_327	-6842.5	113.5
1066	S_326	-6859.5	258.5
1067	S_325	-6876.5	113.5
1068	S_324	-6893.5	258.5
1069	S_323	-6910.5	113.5
1070	S_322	-6927.5	258.5
1071	S_321	-6944.5	113.5
1072	S_320	-6961.5	258.5
1073	S_319	-6978.5	113.5
1074	S_318	-6995.5	258.5
1075	S_317	-7012.5	113.5
1076	S_316	-7029.5	258.5
1077	S_315	-7046.5	113.5
1078	S_314	-7063.5	258.5
1079	S_313	-7080.5	113.5
1080	S_312	-7097.5	258.5
1081	S_311	-7114.5	113.5
1082	S_310	-7131.5	258.5
1083	S_309	-7148.5	113.5
1084	S_308	-7165.5	258.5
1085	S_307	-7182.5	113.5
1086	S_306	-7199.5	258.5
1087	S_305	-7216.5	113.5
1088	S_304	-7233.5	258.5
1089	S_303	-7250.5	113.5
1090	S_302	-7267.5	258.5
1091	S_301	-7284.5	113.5
1092	S_300	-7301.5	258.5
1093	S_299	-7318.5	113.5
1094	S_298	-7335.5	258.5
1095	S_297	-7352.5	113.5
1096	S_296	-7369.5	258.5
1097	S_295	-7386.5	113.5
1098	S_294	-7403.5	258.5
1099	S_293	-7420.5	113.5
1100	S_292	-7437.5	258.5
1101	S_291	-7454.5	113.5
1102	S_290	-7471.5	258.5
1103	S_289	-7488.5	113.5
1104	S_288	-7505.5	258.5
1105	S_287	-7522.5	113.5
1106	S_286	-7539.5	258.5
1107	S_285	-7556.5	113.5
1108	S_284	-7573.5	258.5
1109	S_283	-7590.5	113.5
1110	S_282	-7607.5	258.5
1111	S_281	-7624.5	113.5
1112	S_280	-7641.5	258.5
1113	S_279	-7658.5	113.5
1114	S_278	-7675.5	258.5
1115	S_277	-7692.5	113.5
1116	S_276	-7709.5	258.5
1117	S_275	-7726.5	113.5
1118	S_274	-7743.5	258.5
1119	S_273	-7760.5	113.5
1120	S_272	-7777.5	258.5
1121	S_271	-7794.5	113.5
1122	S_270	-7811.5	258.5
1123	S_269	-7828.5	113.5
1124	S_268	-7845.5	258.5
1125	S_267	-7862.5	113.5
1126	S_266	-7879.5	258.5
1127	S_265	-7896.5	113.5
1128	S_264	-7913.5	258.5
1129	S_263	-7930.5	113.5
1130	S_262	-7947.5	258.5
1131	S_261	-7964.5	113.5
1132	S_260	-7981.5	258.5
1133	S_259	-7998.5	113.5
1134	S_258	-8015.5	258.5
1135	S_257	-8032.5	113.5
1136	S_256	-8049.5	258.5
1137	S_255	-8066.5	113.5
1138	S_254	-8083.5	258.5
1139	S_253	-8100.5	113.5
1140	S_252	-8117.5	258.5

Num	Pad Name	CX	CY
1141	S_251	-8134.5	113.5
1142	S_250	-8151.5	258.5
1143	S_249	-8168.5	113.5
1144	S_248	-8185.5	258.5
1145	S_247	-8202.5	113.5
1146	S_246	-8219.5	258.5
1147	S_245	-8236.5	113.5
1148	S_244	-8253.5	258.5
1149	S_243	-8270.5	113.5
1150	S_242	-8287.5	258.5
1151	S_241	-8304.5	113.5
1152	SHIELDING12	-8332.5	258.5