OPENCALC PA1

Title	OPENCALC OC1 TITLE	
Size A	Document Number <Doc>	Rev 1
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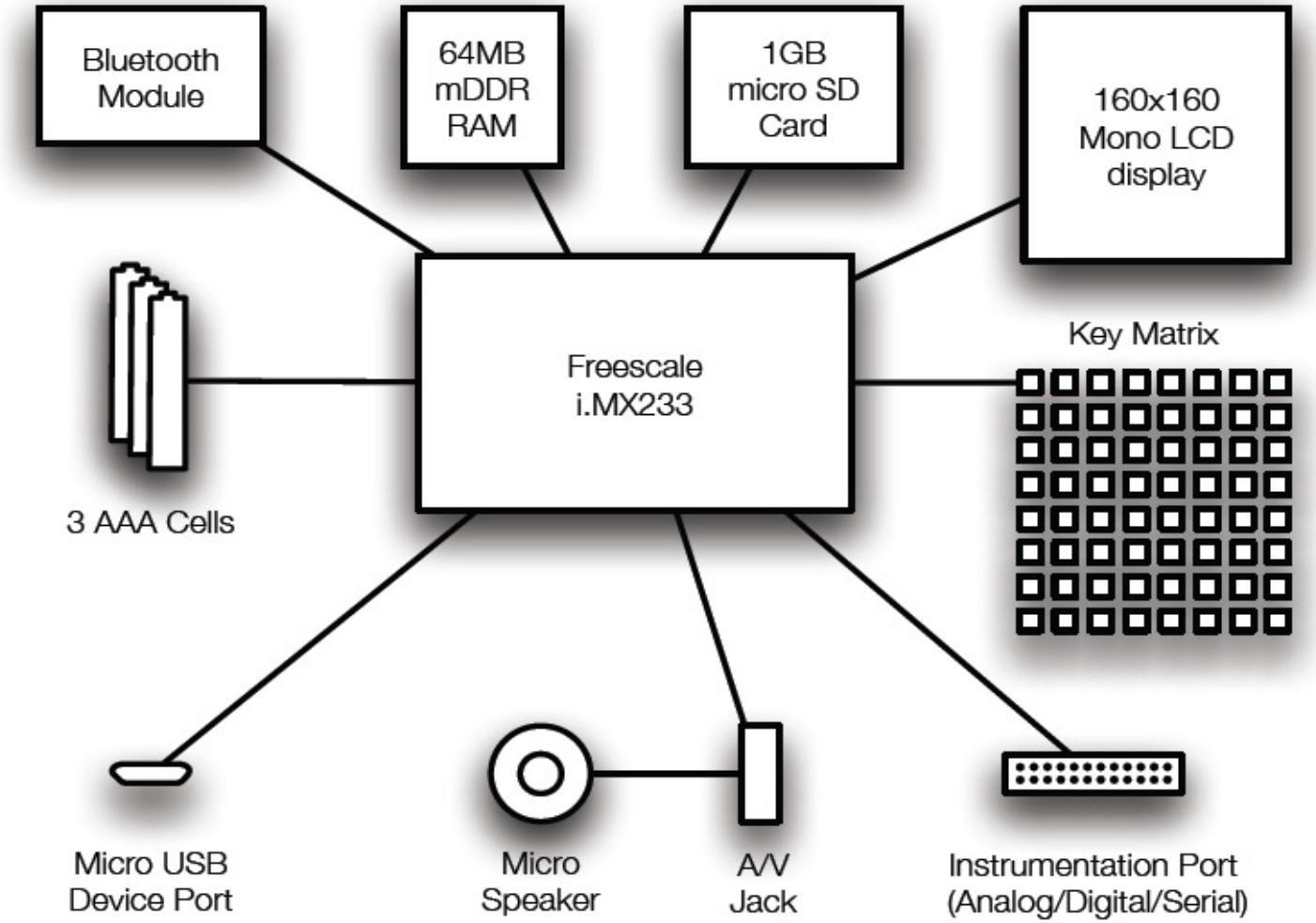
OPENCALC BLOCK DIAGRAM



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TODO

* Everything
* Use LRDAC 7 to monitor battery (RM 32.5), use FIQ for quick shutdown

Questions

Should DQS have pulldowns on board?

Q. I removed all battery related capacitors on BATT and DCDC_BATTTERY, and the schottkey between BATT and V4P2. Is that acceptable, assuming we never plan to use a battery? Seems like it should be okay, right?
A. [from Jim Kenney] I've discussed with the analog designers. They'd prefer to keep BATT and DCDC_BATT at some known voltage so they aren't floating, even if they aren't being used. So they recommended adding a 1K resistor from those pins to VDDIO.
There shouldn't be any bulk capacitor required though.
++++++++++++++++++++
From a software standpoint, it should be ok as far as I know. I've tested booting and running without a battery although not extensively.
You'll want to disable the battery charger as in its present state it could cause problems if left active with no battery actually attached.
Unfortunately, the battery charger driver is also part of the power source driver so the driver module itself can't be omitted. I'd suggest apps look at this driver and recommend the best way to keep the Battery Charger disabled for devices with no battery attached.

Q. How much power does the MX233 Take:
A. MX233 Power Consumption Spreadsheet
http://sites.google.com/a/britepad.com/project/documents/IMX23_Power_Consumption_Calculator_REVA_10-06-2009.xls

Q. In USB-only power mode is it possible to enumerate at 100mA VBUS current consumption?
A. Our team believes this is possible, but is not supported by default in the BSP today.
Using mobile DDR would be recommended to achieve this reliably.

Q. Is it possible to get down to 2.5mA VBUS, yet still monitor the USB lines and resume when the USB bus resumes? I'm assuming that we power-gate the DDR to off, and only use on-chip RAM.
A. Our team believes this is possible, but is not supported by default in the BSP today. 2. Using mDDR and it is only put in self refresh, not gated off. It is not possible using DDR1 and leaving it in self refresh.

Q. If #2 is possible, is it possible to power-gate the DDR and ensure no voltage is sent to the DDR pins during the DDR-gated-off mode? i.e. is it possible to guarantee that all pins connected to the DDR are driven LOW, or at least floating?
A. For mDDR, we don't have the ability gate it's power off internally. We can configure the chip in it's lowest power mode which cuases it to lose the contents of memory (consult mddr datasheet for more info).
But this is uneccessary.

Q. OTP: I can't tell if the OTP block is really one-time-programmable. Is this really a one-time programmable block, or is it reprogrammable?
A. These are truly one-time programmable bits. They are implemented using an eFuse technology.
You only get one shot at greatness here. ;-)

Q. PSWITCH recovery vs. regular USB mode: Is there any difference between the USB boot mode (selected by the boot mode pins) and the recovery mode (selected by the PSWITCH) mode? Is this simply 2 ways of entering the same USB mode?
A. Yes, these are equivalent. PSWITCH is is just the manual entry into USB recovery mode. You can also enter USB recovery mode if there is a non-recoverable boot time error. Of course the bootmode switches can land you here as well.

Q. Have customers successfully implemented the MX233 in QFP on 4 layer boards and met EMI? Seems like it may be a bit of a challenge.
A. Per AN3883 it can be done but ESD performance will be comprimised. See the attached copy. I will also ask the factory to see if they can provide any more information.

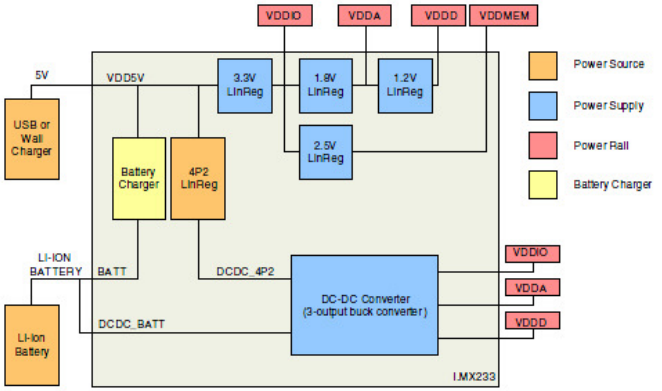

Figure 1. Logical Diagram of i.MX233 PMU

Q. We plan on making this product run as a device on USB only with no battery:Is there a problem running on 500mA USB only? What issues do you foresee? DDR1, Full speed core, display backlight?
A. The MX233 can operate "permanently attached" to a USB power supply. See AN3989 (attached) for a bit of information. There is another issue you need to work through. The on board supplies can support around 1.5W to at the very most, 2W of system power. Anything beyond this will require off chip supplies to cover. The hard limit, of course, is the USB 2.5W supply maxiumum as spec'd by USB 2.0. If you work off the charger spec you can see a lot more current but you end up not being able to use a PC port, although I have been told many PC's will supply current in excess fo the 500mA spec.

Q. Does the DC-DC only run off of 4.2V? that is: can we connect 5V to the 4.2V supply directly and avoid loosing the 0.8V drop in efficiency? ABS MAX ratings show VDD4P2V maximum at 4.242. Is that a hard requirement?
A. When using a 5V supply the 4P2 regulator is a hard requirement. Again AN3989 can shed a little light on the situation.

Q. What's the fundamental difference between the application UART and the debug UART? Does the debug UART have any special function in the various boot modes? Or is it simply a difference in speed it's capable of?
A. The debug UART is limited to 115.2Kbps with no flow control pins available in either package. The application UART's are capable of 3.25Mbps with one UART having flow control pins available in the 169 pin BGA, though not in the QFP.

Q. 1-Wire vs parallel JTAG info.
A. Check

Power Consumption Spreadsheet can be found here
http://spreadsheets.google.com/a/britepad.com/ccc?key=0AkaMDBXLVs6ydExkMU82Wnc0UTQ5NU5ZdWhWZlZzN3c&hl=en

Title: OPENCALC OC1 DESIGN NOTES		
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6/25/2011: Initial Revision

TODO:

* Can we boot without programming any OTP bits?

PORT USAGE:

* I2C/AUART1 -> GEEK PORT
* AUART2 (ALL 4 PINS) -> RESERVED FOR BLUETOOTH
* EMI -> mDDR
* SSP1 -> uSD card
* LCD -> LCD
* SAIF -> GEEK PORT gpio pins

Title: OPENCALC OC1 CHANGELIST		
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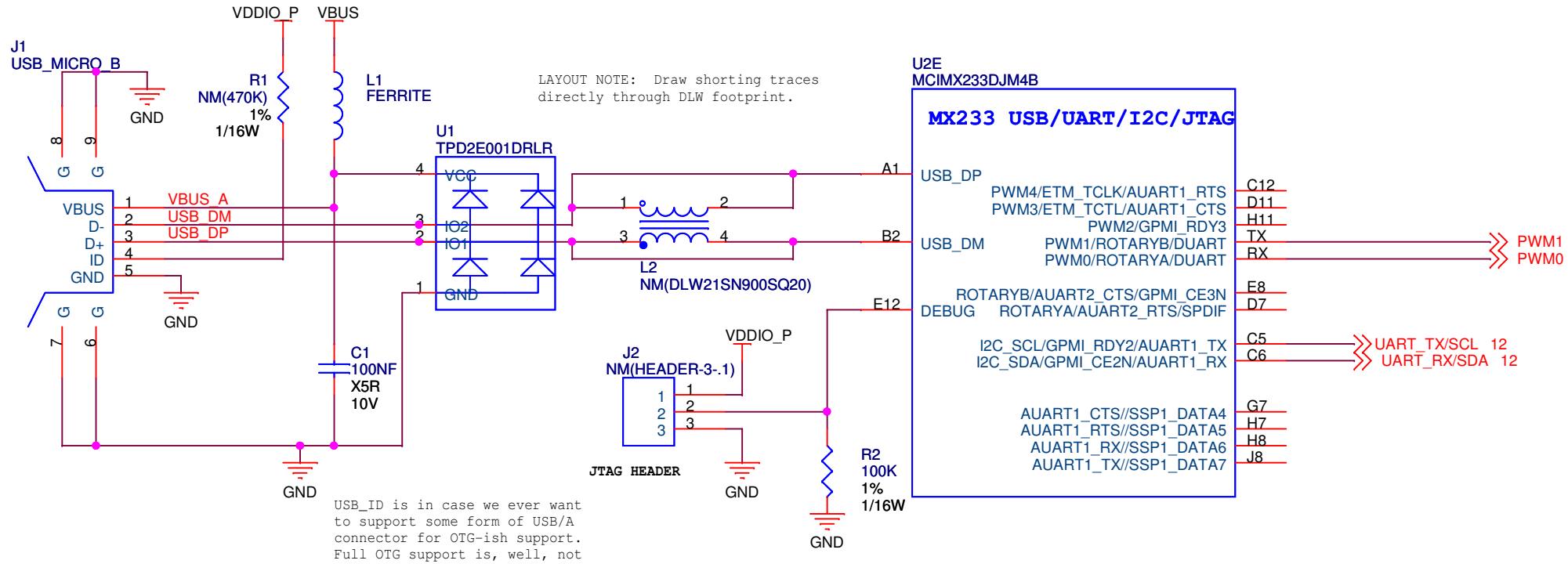
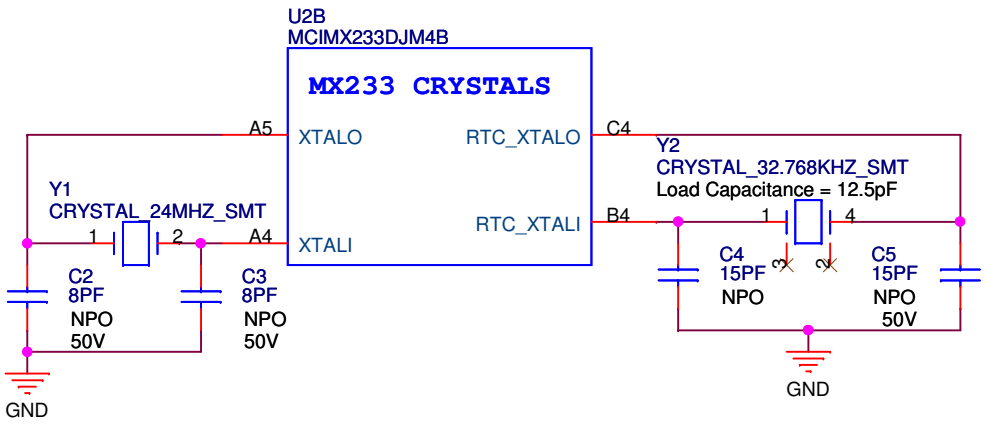
USB/CRYSTAL/JTAG

Layout Note: Low impedance Vias to GND! for ESD

Ferrites, CMC and ESD diode examples from murata applications guide, and intel guide in 'docs' directory.





Crystal Design Notes:
The 24 MHz crystal should be located close to the mx25.

Cload = [(C1*C2)/(C1+C2)]+Cstray

Cstray =~ 4-6pF

Set C1 == C2:
Cload = (C1^2/2C1)+CStray
Cload = C1/2 + CStray
C1 = 2 * (Cload - CStray)
C1 = C2 = 2 * (8pF - 4pF) = 8pF

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CHUMBYONE uses a 110 ohm resistor between EMI_CLK and EMI_CLKN. But MX233 SPF77066_B1.PDF does not. Is it necessary/recommended?

LAYOUT NOTE: CONTROL #of vias on DQx, DQS and CLK.

U2C
MCIMX233DJM4B

MX233 DDR

EMI_CLK	M6	DDR_CLK
EMI_CLKN	N6	DDR_CLKN
EMI_DQS1	K8	DDR_DQS1
EMI_DQS0	N12	DDR_DQS0
EMI_CASN	M13	DDR_CASN
EMI_RASN	N13	DDR_RASN
EMI_CE0N	J10	DDR_CE0N
EMI_CE1N	H12	
EMI_CKE	F11	DDR_CKE
EMI_WEN	J11	DDR_WEN
EMI_BA1	L12	DDR_BA1
EMI_BA0	L13	DDR_BA0
EMI_DQM1	M9	DDR_DQM1
EMI_DQM0	M12	DDR_DQM0
EMI_D15	M7	DDR_DQ15
EMI_D14	N7	DDR_DQ14
EMI_D13	K6	DDR_DQ13
EMI_D12	L7	DDR_DQ12
EMI_D11	K7	DDR_DQ11
EMI_D10	M8	DDR_DQ10
EMI_D09	N8	DDR_DQ9
EMI_D08	N9	DDR_DQ8
EMI_D07	L9	DDR_DQ7
EMI_D06	L11	DDR_DQ6
EMI_D05	K9	DDR_DQ5
EMI_D04	M11	DDR_DQ4
EMI_D03	N10	DDR_DQ3
EMI_D02	N11	DDR_DQ2
EMI_D01	M10	DDR_DQ1
EMI_D00	K10	DDR_DQ0
EMI_A12	H13	DDR_A12
EMI_A11	H10	DDR_A11
EMI_A10	J12	DDR_A10
EMI_A09	F13	DDR_A09
EMI_A08	G13	DDR_A08
EMI_A07	G11	DDR_A07
EMI_A06	F12	DDR_A06
EMI_A05	G12	DDR_A05
EMI_A04	G10	DDR_A04
EMI_A03	K11	DDR_A03
EMI_A02	J13	DDR_A02
EMI_A01	K12	DDR_A01
EMI_A00	K13	DDR_A00

VDDIO_DRAM

R26 10.0K 1% 1/16W

U3

	G2	CK
	G3	$\overline{CK}$
	E2	UDQS
	E8	LDQS
	G8	$\overline{CAS}$
	G9	$\overline{RAS}$
	H7	$\overline{CS}$
	G1	CKE
	G7	$\overline{WE}$
	H9	BA1
	H8	BA0
	F2	UDM
	F8	LDM
	A2	DQ15
	B3	DQ14
	B2	DQ13
	C3	DQ12
	C2	DQ11
	D3	DQ10
	D2	DQ9
	E3	DQ8
	E7	DQ7
	D8	DQ6
	D7	DQ5
	C8	DQ4
	C7	DQ3
	B8	DQ2
	B7	DQ1
	A8	DQ0
	F7	A13
	H3	A12
	H2	A11
	J7	A10/AP
	H1	A9
	J3	A8
	J2	A7
	J1	A6
	K3	A5
	K2	A4
	K8	A3
	K7	A2
	J9	A1
	J8	A0

MDDR1,32MX16,VFBGA

VDDIO_DRAM

VDDQ	A7	
VDDQ	B1	
VDDQ	C9	
VDDQ	D1	
VDDQ	E9	
VDDQ	A9	
VDD	F9	
VDD	K9	
VSS	A1	
VSS	F1	
VSS	K1	
VSSQ	A3	
VSSQ	B9	
VSSQ	C1	
VSSQ	E1	
TEST	D9	
NC	F3	

VDDIO_DRAM

C8 1NF X7R 50V
C9 1NF X7R 50V
C10 1NF X7R 50V
C11 1NF X7R 50V
C12 1NF X7R 50V

VDDIO_DRAM

C13 1NF X7R 50V
C14 1NF X7R 50V
C15 1NF X7R 50V
C16 100NF X5R 10V
C17 100NF X5R 10V

* MDDR parts from Micron:
All in 60-ball package

MT46H128M16LFCK	2	Gb / 256 MB
MT46H64M16LFBF	1	Gb / 128 MB
MT46H32M16LFBF	512	Mb / 64 MB
MT46H16M16LFBF	256	Mb / 32 MB
MT46H8M16LFBF	128	Mb / 16 MB

VDDIO_DRAM VDDA VDDM

NOTE: MDDR/DDR DIFFERENCES

FOR MDDR: VDDIO_DRAM == VDDA & PULLUP/DN = 10.0K
FOR DDR: VDDIO_DRAM == VDDM * PULLUP/DN = 47K

DDR and mDDR are NOT pin compatible unfortunately.
You must choose.

R28 10.0K 1% 1/16W
R27 10.0K 1% 1/16W

Layout Note: DDR_DQ[15:8] and DDR_DQ[7:0] can be shuffled within any byte for layout convenience.

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FLASH

setting detect to
ensure that when
booting, it thinks a
card is detected.

MICRO SD

U2F
MCIMX233DJM4B

MX233 NAND (GPMI)

GPMI_CE2N	K5	KEY_COL_7	13
GPMI_CE1N	F8	KEY_COL_6	13
GPMI_CE0N	G8	KEY_COL_5	13
GPMI_ALE/LCD_D17	K4	KEY_COL_4	13
GPMI_CLE/LCD_D16	K3	KEY_COL_3	13
GPMI_RDY3	E6	KEY_COL_2	13
GPMI_RDY2	F6	KEY_COL_1	13
GPMI_RDY1//SSP2_CMD	J6		
GPMI_RDY0//SSP2_DETECT	G6	KEY_COL_0	13
GPMI_RDN	H6		
GPMI_WRN//SSP2_SCK	E7		
GPMI_WPN	F7		
GPMI_D15/AUART2_TX/GPMI_CE3N	N5		
GPMI_D14/AUART2_RX	N4		
GPMI_D13/LCD_D23	N3		
GPMI_D12/LCD_D22	N2	PSWITCH_A	13
GPMI_D11/LCD_D21/SSP1_DATA7	N1	KEY_ROW_0	13
GPMI_D10/LCD_D20/SSP1_DATA6	M5	KEY_ROW_1	13
GPMI_D09/LCD_D19/SSP1_DATA5	M4	KEY_ROW_2	13
GPMI_D08/LCD_D18/SSP1_DATA4	M3	KEY_ROW_3	13
GPMI_D07/LCD_D15/SSP2_DATA7	M1	KEY_ROW_4	13
GPMI_D06/LCD_D14/SSP2_DATA6	M2	KEY_ROW_5	13
GPMI_D05/LCD_D13/SSP2_DATA5	L4	KEY_ROW_6	13
GPMI_D04/LCD_D12/SSP2_DATA4	L5	KEY_ROW_7	13
GPMI_D03/LCD_D11/SSP2_DATA3	L3		
GPMI_D02/LCD_D10/SSP2_DATA2	L2		
GPMI_D01/LCD_D9/SSP2_DATA1	L1		
GPMI_D00/LCD_D8/SSP2_DATA0	K2		

U2H
MCIMX233DJM4B

MX233 SDIO (SSP)

SSP1_SCK//JTAG_TRST	D12	SD_SCK
SSP1_CMD//JTAG_TDO	H9	SD_CMD
SSP1_DETECT/GPMI_CE3N/USB_ID	D10	
SSP1_DATA3//JTAG_TMS	E10	SD_DATA3
SSP1_DATA2/I2C_SDA/JTAG_RTCK	F10	SD_DATA2
SSP1_DATA1/I2C_SCL/JTAG_TCLK	F9	SD_DATA1
SSP1_DATA0//JTAG_TDI	G9	SD_DATA0

U28
SPI-EEPROM

SPI2_SCK	6	SCK	HOLD 7
SPI2_SS0	1	CS	
SPI2_MISO	2	SO	VCC 8
SPI2_MOSI	5	SI	
VDDIO_P	3	WP	
		1k x 8	VSS 4

SPI BOOT SUPPORTS 2 BYTE ADDRESSING ONLY.

VDDIO_P

R117
10.0K
1%
1/16W

C18
100NF
X5R
10V

C20
100NF
X5R
10V

GND

U4
MICROSD-lid-type

9	GND
8	DAT1
7	DAT0
6	VSS
5	CLK
4	VDD
3	CMD
2	CD/DAT3
1	DAT2
10	GND
11	GND
12	GND

BOOT FROM I2C:
I2C MUST BE ADDRESS 1010000 (0x50)
and must have a 2-byte 'sub' address
must be 400kHz

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LCD INTERFACE

NOTE: I'm not 100% sure on the connection of the RD pin. I believe that this LCD interface CAN NOT READ from the LCD, so simply set the mode to 8080, set RD high.

```
MX233     8080  |  6800
----------------|---------
LCD_WR =   WRn  | R/Wn
LCD_RD =   RDn  |  EN
```

U2D
MCIMX233DJM4B

MX233 LCD

LCD_CS	H4	LCD_CS
LCD_VSYNC/LCD_BUSY	J1	
LCD_HSYNC/I2C_SDA	J2	
LCD_ENABLE/I2C_SCL	H5	
LCD_DOTCK/GPMI_RDY3	K1	
LCD_RESET/ETM_TCTL/GPMI_CE3N	J5	LCD_RESET
LCD_WR	J4	LCD_WR
LCD_RS/ETM_TCLK	J3	
LCD_D17	E1	
LCD_D16//SAIF_ALT_BITCLK	E3	
LCD_D15/ETM_DA7/SAIF1_SDATA1	E5	CHARGE_ENABLE 11
LCD_D14/ETM_DA6/SAIF1_SDATA2	F2	BATT_MEASURE 11
LCD_D13/ETM_DA5/SAIF2_SDATA2_SAIF_ALT_BITCLK	F4	SAIF_BCLK 12
LCD_D12/ETM_DA4/SAIF2_SDATA1	G1	
LCD_D11/ETM_DA3/SAIF_LRCLK	G4	SAIF_WCLK 12
LCD_D10/ETM_DA2/SAIF_MCLK_BITCLK	H1	
LCD_D09/ETM_DA1/SAIF1_SDATA0	H3	SAIF_TX 12
LCD_D08/ETM_DA0/SAIF2_SDATA0	H2	SAIF_RX 12
LCD_D07/ETM_DA15	G5	LCD_D7
LCD_D06/ETM_DA14	G2	LCD_D6
LCD_D05/ETM_DA13	F5	LCD_D5
LCD_D04/ETM_DA12	F3	LCD_D4
LCD_D03/ETM_DA11	F1	LCD_D3
LCD_D02/ETM_DA10	E4	LCD_D2
LCD_D01/ETM_DA9	E2	LCD_D1
LCD_D00/ETM_DA8	D3	LCD_D0
VDAC1	C11	VDAC1 9

TRULY LCD MODULE

U27
LCD-MFG-G240160DPSW-3N-E

12	CS0	330nF || 3.3-10MOhm	1 VLCD
13	CD		2 VS+
	8080 | 6800	1x 220nF 25V	3 VS-
14	WR | R/W		7 VB0+
15	RD | EN	2x 2.2uF 5V	4 VB0-
24	D7		6 VB1+
23	D6	2x 2.2uF 5V	5 VB1-
22	D5		8 VDD
21	D4	2.9-3.1V	
20	D3		9 VSS
19	D2		10 NC(TST4)
18	D1		25 PAD0
17	D0		26 PAD1
11	BM0(6800/8080)		27 PAD2
16	RESET		28 PAD3

C118 NM(220nF) X5R 25V
R115 10.0M 5% 1/16W
C117 330nF X5R 25V
C120 2.2UF X5R 10V
C119 2.2UF X5R 10V
C121 2.2UF X5R 10V
C122 2.2UF X5R 10V
C123 100NF X5R 10V
VDDIO_P
R19 47K

AS Per IMX23RM, page 2-7, table 2-8, 50K resistor is sufficient to overcome the pin keeper.

VDDIO_P

R7 47K — SW66E (5/12)
R8 47K — SW66D (4/13)
R9 47K — SW66C (3/14)
R10 47K — SW66B (2/15)
R11 47K — SW66A (1/16)

SW66F (6/11)
SW66H (8/9)
SW66G (7/10)

D5	R123 4.70K 1% 1/16W	
RS	R122 4.70K 1% 1/16W	
D3	R121 4.70K 1% 1/16W	
D2	R120 4.70K 1% 1/16W	
D1	R119 4.70K 1% 1/16W	
D0	R118 4.70K 1% 1/16W	

BOOT: Default to I2C Boot.

	D5	RS	D3	D2	D1	D0
USB	0	1	0	0	0	0
3.3V I2C MASTER	0	1	0	0	0	1
3.3V SPI FLASH 1 MASTER	0	1	0	0	1	0
3.3V SPI FLASH 2 MASTER	0	1	0	0	1	1
3.3V NAND	0	1	0	1	0	0
DEBUG	0	1	0	1	1	0
3.3V SD/MMC 1	0	1	1	0	0	1
3.3V SD/MMC 2	0	1	1	0	1	0
BOOT MODE FROM OTP	0	0	X	X	X	X
ETM ENABLE	1					

BOOT NOTE:
Due to a bug in the SD Boot process (see errata), we need to boot from an I2C boot device, which patches the boot code to then boot from SD card.

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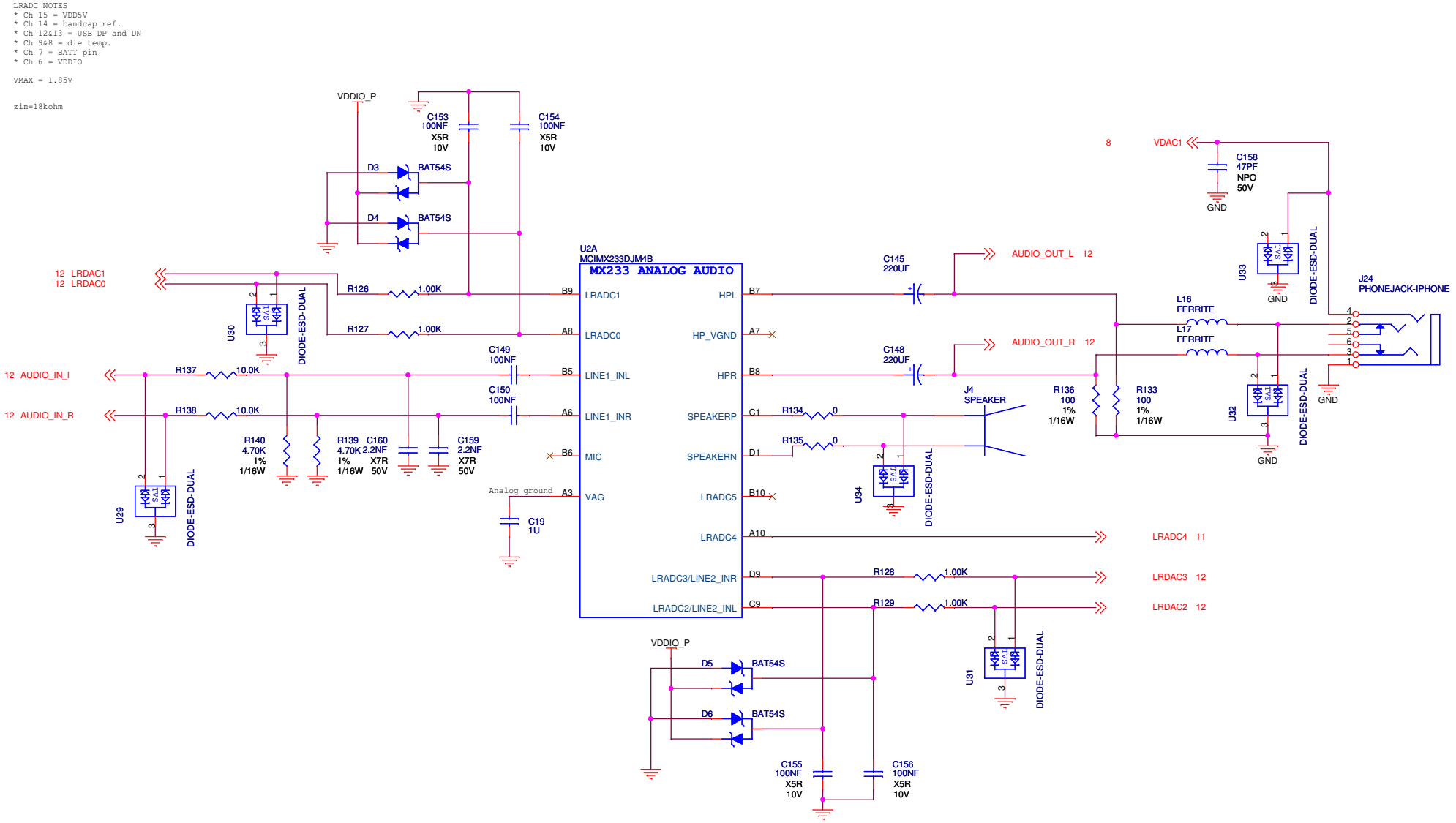
LRADC NOTES
* Ch 15 = VDD5V
* Ch 14 = bandcap ref.
* Ch 12&13 = USB DP and DN
* Ch 9&8 = die temp.
* Ch 7 = BATT pin
* Ch 6 = VDDIO
VMAX = 1.85V
zin=18kohm
VDDIO_P
C153 100NF X5R 10V
C154 100NF X5R 10V
D3 BAT54S
D4 BAT54S
U2A
MCIMX233DJM4B
MX233 ANALOG AUDIO
LRADC1
LRADC0
LINE1_INL
LINE1_INR
MIC
VAG
HPL
HP_VGND
HPR
SPEAKERP
SPEAKERN
LRADC5
LRADC4
LRADC3/LINE2_INR
LRADC2/LINE2_INL
12 LRDAC1
12 LRDAC0
R126 1.00K
R127 1.00K
U30 DIODE-ESD-DUAL
12 AUDIO_IN_I
12 AUDIO_IN_R
R137 10.0K
R138 10.0K
C149 100NF
C150 100NF
R140 4.70K 1% 1/16W
R139 4.70K 1% 1/16W
C160 2.2NF X7R 50V
C159 2.2NF X7R 50V
U29 DIODE-ESD-DUAL
Analog ground
C19 1U
C145 220UF
C148 220UF
AUDIO_OUT_L 12
AUDIO_OUT_R 12
R134 0
R135 0
J4 SPEAKER
U34 DIODE-ESD-DUAL
R136 100 1% 1/16W
R133 100 1% 1/16W
L16 FERRITE
L17 FERRITE
U32 DIODE-ESD-DUAL
U33 DIODE-ESD-DUAL
J24 PHONEJACK-IPHONE
8 VDAC1
C158 47PF NPO 50V
GND
LRADC4 11
LRDAC3 12
LRDAC2 12
R128 1.00K
R129 1.00K
VDDIO_P
D5 BAT54S
D6 BAT54S
U31 DIODE-ESD-DUAL
C155 100NF X5R 10V
C156 100NF X5R 10V
Title
OPENCALC OC1 AUDIO
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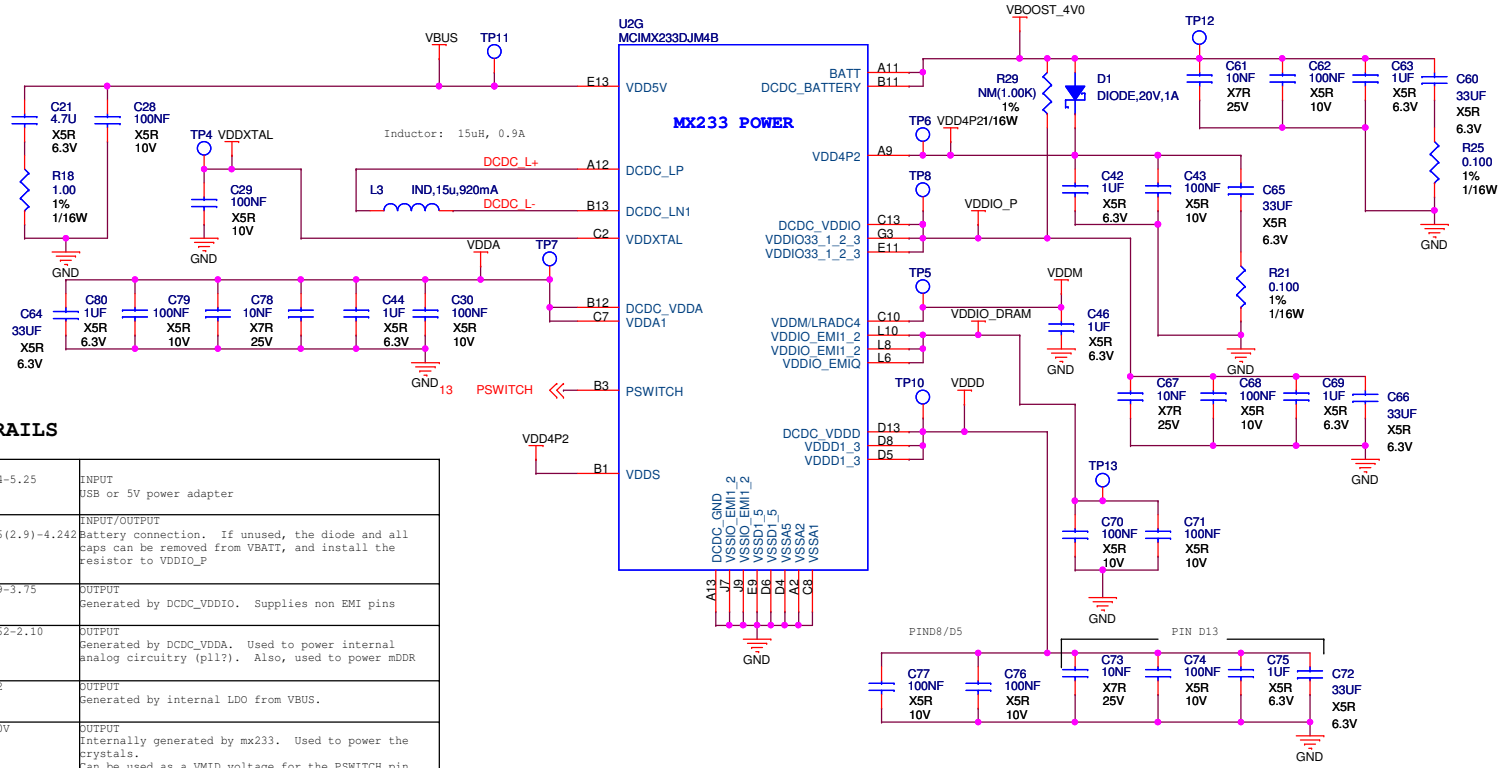
POWER



POWER RAILS

VBUS	4.4-5.25	INPUT USB or 5V power adapter
VBATT	2.6(2.9)-4.242	INPUT/OUTPUT Battery connection. If unused, the diode and all caps can be removed from VBATT, and install the resistor to VDDIO_P
VDDIO_P	2.9-3.75	OUTPUT Generated by DCDC_VDDIO. Supplies non EMI pins
VDDA	1.62-2.10	OUTPUT Generated by DCDC_VDDA. Used to power internal analog circuitry (pll?). Also, used to power mDDR
VDD4P2	4.2	OUTPUT Generated by internal LDO from VBUS.
VDDXTAL	1.0V	OUTPUT Internally generated by mx233. Used to power the crystals. Can be used as a VMID voltage for the PSWITCH pin
VDDM	2.5V	OUTPUT 2.5v supply for DDR (not for MDDR).
VDDIO_DRAM	1.8-3.25V	OUTPUT Must be shorted either to VDDM (DDR) or VDDA (mDDR). This is done on the memory page. Leave unconnected on this page.
VDDD	1.0-1.55V	OUTPUT Core voltage. Generated by LDO or DC-DC on chip.

PSWITCH STATES:
* If PSWITCH > min (MID) for > 100mS, then power on
* If PSWITCH has a falling edge faster than 15nS, power OFF
* If PSWITCH > min(MID), lower bit of HW_POWER_STS_PSWITCH is set.
* if PSWITCH is pulled to VDDIO via a resistor, upper bit of HW_POWER_STS_PSWITCH is set.
* if PSWITCH is pulled to VDDIO during initial boot sequence for more than 5 seconds, FW recovery mode is entered.

Desired functionality:
Turn on immediately upon VBUS
Force off if button held > 5 s
Soft-off capability

LOW: 0 < PSWITCH < 0.30
MID: 0.65 < PSWITCH < 1.5
HIGH: 2.1 < PSWITCH < VDDXTAL+1.575 = 2.575

VDDXTAL: ~ 1V
VDDIO: ~3.3

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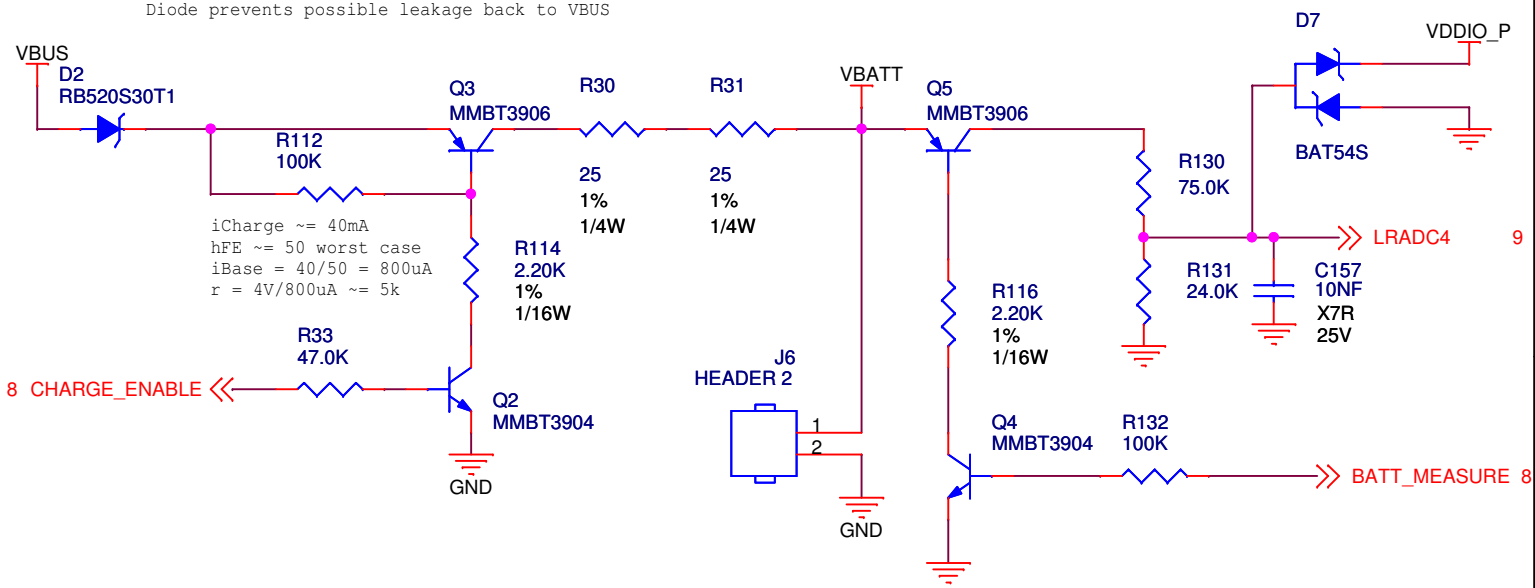
```
VBATT = 2.0 - 3.2
C = 2200 mAh
C/30 = 73mA
VBUS = 5.0 nom
Ifinal = 73mA
R = V/I = (5-3.2)/73mA = 25 Ohms
Pmax = (5.25 - 2.0)^2/25 = 0.42 Watts
Pfinal = (5.25 - 3.2)^2/25 = 0.17 Watts
Iinitial = (5.25 - 2.0)/25 = 130mA
Ifinal = (5.25 - 23.2)/25 = 82mA
```

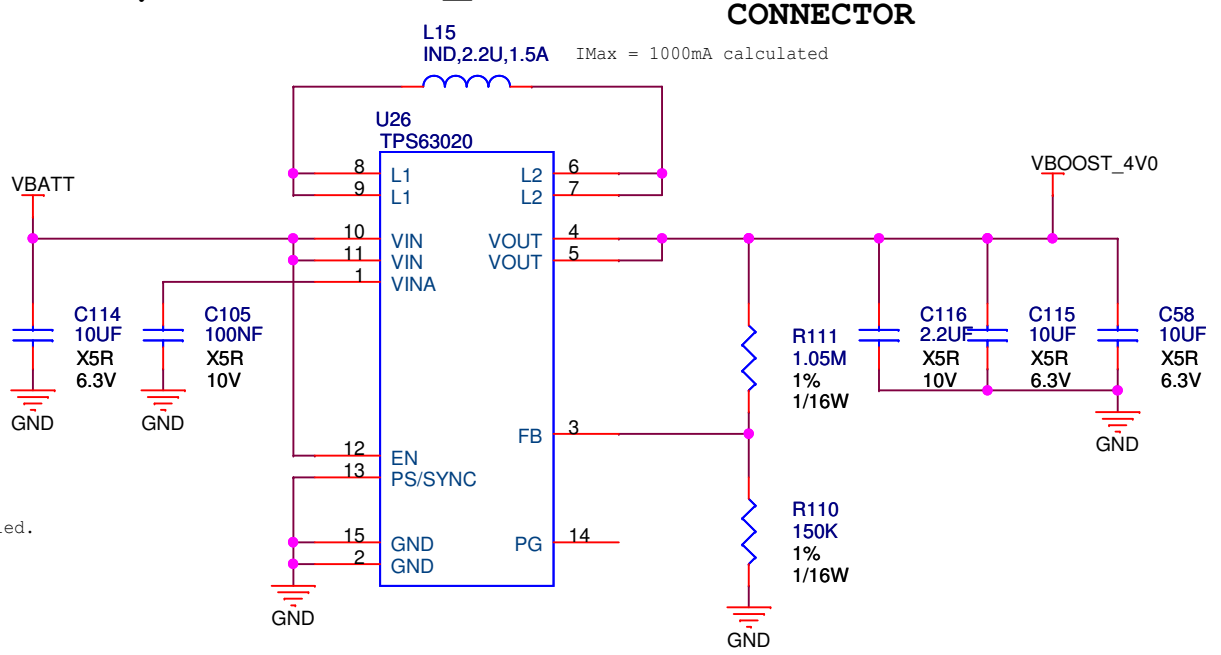
Diode prevents possible leakage back to VBUS



Battery (1.8 to 5.25 possbile) to VBOOST_4V0

BATTERY CONNECTOR

```
Vin1: 5.25;
Vin2: 1.8;
Iout: 600e-3;
fr: 2.4;
Vout: 1.2;
L1: (Vin1 - Vout)*.5;
L2: Vout * .5;
L: max(L1, L2);
L: 2.2;
I1: Iout/.8 + Vout * (Vin1 - Vout)/(2 * Vin2 * fr * L);
I2: Vout * Iout/(.8*Vin2) + Vin2 * (Vout - Vin2)/(2*Vout*fr*L);
Imax = max(I1, I2);
Cout = 10 * L;
```




```
Battery only:
   All system power is provided through the boost regulator.
USB plugged in:
   All system power comes through VBUS.
USB+BATT:
   All system power comes through VBUS.  Battery charging enabled.
```

```
TPS63020 LEAKAGE = 25 uA typ
MX233 LEAKAGE = 11 uA typ when shut down

So, that looks like 40 uA to be safe for boost +
mx233.
1200e3 uA-h / 40 uA = 3.4 years on a full charge
before depletion.  This should be less than the
internal leakage for all except the best NiMH
batteries.  Not as good as Alkaline.
```

```
R1 = R2 * (Vout/Vfb -1 );
R2 = 150k;
Iout = Vfb/R2 = 0.5/150k = 3.33333uA
Vout = 4.0V
R1 = (4.0-0.5)/3.33333uA = 1.05mOhm
```

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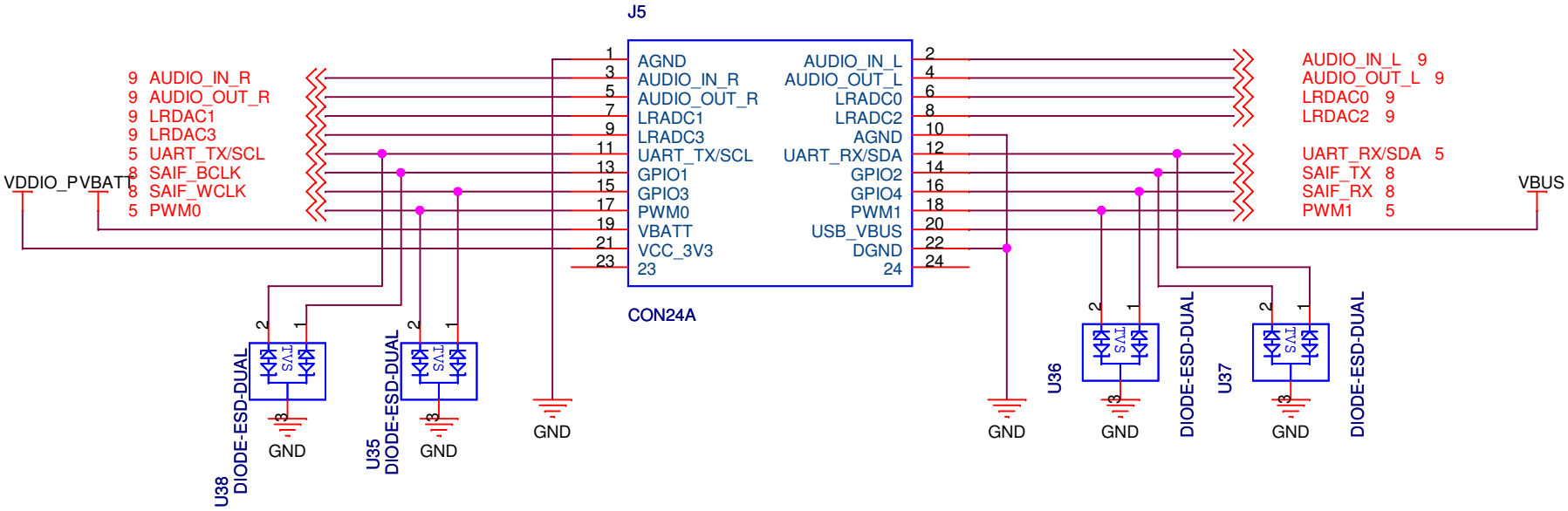
GEEK PORT

* TODO: IO protection on geek port pins

* All pins must be protected during system power off. This means that even when VDDIO_P is 0 V, no pin (at the CPU) is allowed to exceed VDDIO_P + 0.3 V, and GND - 0.3V. This will require something like a resistor + schottkey at each pin.

This can get tricky for analog pins.



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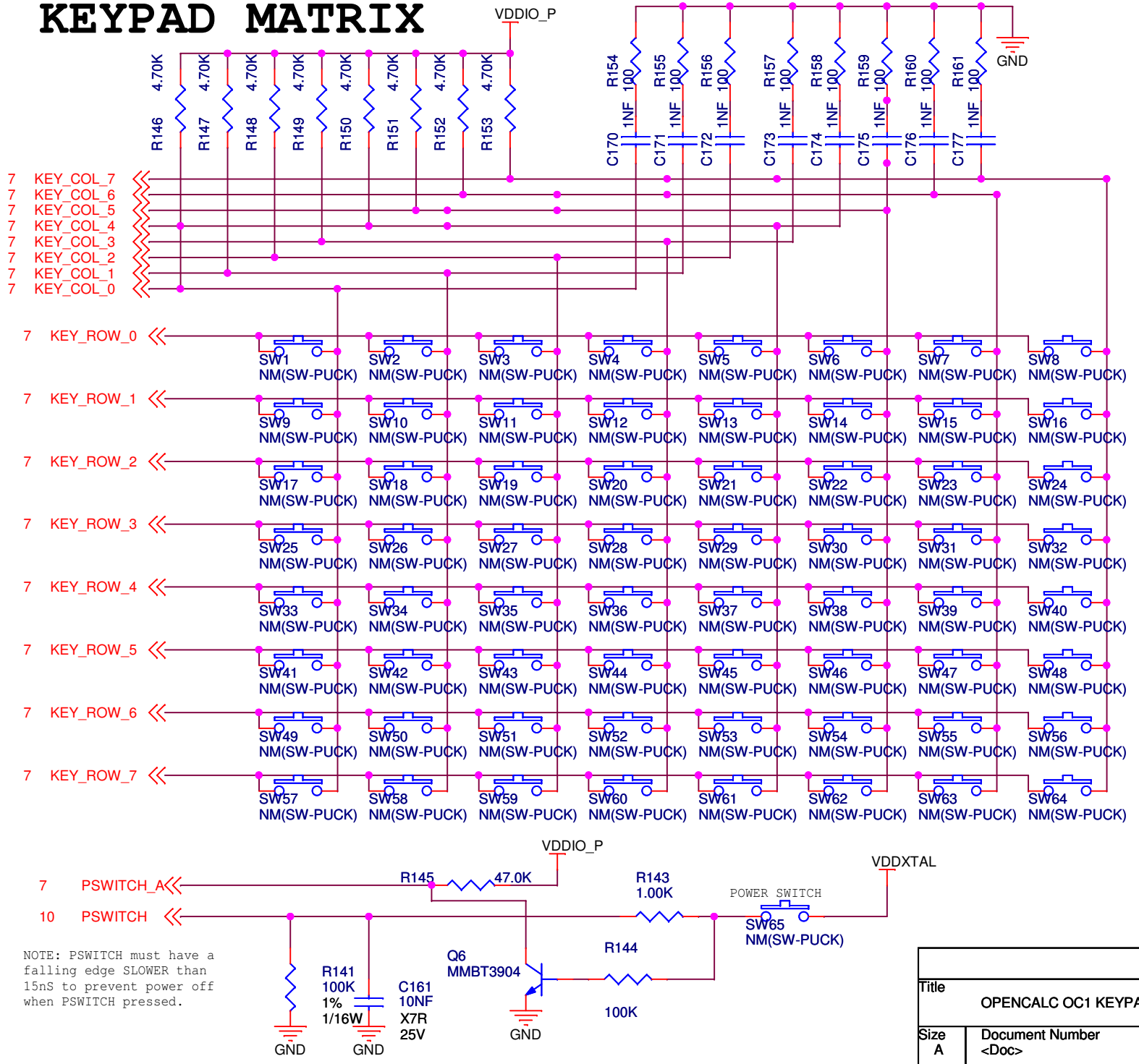
KEYPAD MATRIX



Software must configure pullups on column lines, and drive rows low, and interrupt whenever a colum line goes low.

Then, to determine which key has been pressed, in the ISR sequence through each row with one-row-high and see which col line toggles.

No ESD protection required if keymat can be made without locating holes. Is it possible to make the keymat holes just indentations?

NOTE; These caps are to keep the contacts clean, not to do any debouncing.

NOTE: PSWITCH must have a falling edge SLOWER than 15nS to prevent power off when PSWITCH pressed.

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