ALL SHORE INDUSTRIES

ASI-T-270EA2AN/D

Item	Contents	Unit
Size	2.7	inch
Resolution	320(RGB)x240	/
Interface	8-bit RGB /8-bit Dummy RGB/CCIR656/601	/
Technology type	a-Si TFT	/
Pixel pitch	0.056x0.168	mm
Pixel Configuration	R.G.B. Delta	
Outline Dimension (W x H x D)	63.50x46.60x2.60	mm
Active Area	54.00 x 40.50	mm
Display Mode	Transmissive, Normally white	/
Viewing Direction	12 O'clock	/
Backlight Type	LED	/
Driver IC	NT53002	/

Record of Revision

Date	Revision No.	Summary

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1. Scope

This data sheet introduceS the specification of ASI-T-270EA2AN/D active matrix TFT module. It is composed of a color TFT-LCD panel, driver ICs, FPC and a backlight unit. The 2.7″ display area contains 320(RGB)x 240

2. Application

Digital equipments which need color display, Digital Camera, mobile phone, mobile navigator/video systems.

3. General Information

Item	Contents	Unit
Size	2.7	inch
Resolution	□20□□□□□2□0	/
Interface	8-bit RGB /8-bit Dummy RGB/CCIR656/601	/
Technology type	a-Si TFT	/
Pixel pitch	0.056x0.168	mm
Pixel Configuration	R.G.B. Delta	
Outline Dimension (W x H x D)	63.50x46.60x2.60	mm
Active Area	54.00 x 40.50	mm
Display Mode	Transmissive, Normally white	/
Viewing Direction	12 O'clock	/
Backlight Type	LED	/
Driver IC	NT53002	/

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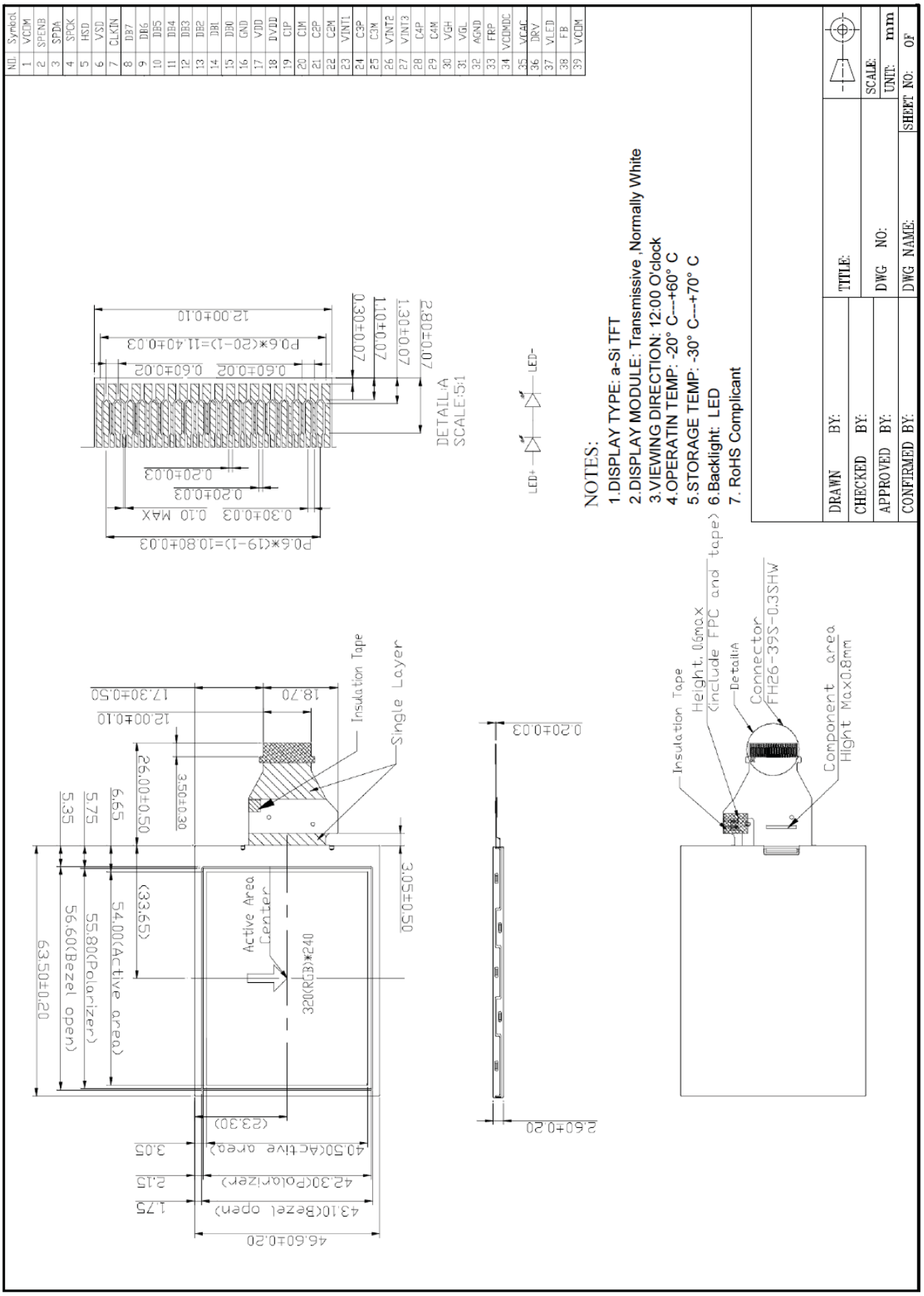
4. Outline Drawing



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5. Interface signals

No	Symbol	I/O	Description	Remark
1	VCOM	I	Panel common voltage	
2	SPENB	I	SPI enable	
3	SPDA	I/O	SPI data input/output	
4	SPCK	I	SPI clock input	
5	HSD	I	Horizontal sync input	
6	VSD	I	Vertical sync input	
7	CLKIN	I	Data clock input	
8	DB7	I	Data input; MSB	
9	DB6	I	Data input	
10	DB5	I	Data input	
11	DB4	I	Data input	
12	DB3	I	Data input	
13	DB2	I	Data input	
14	DB1	I	Data input	
15	DB0	I	Data input; LSB	
16	GND	P	Power ground	
17	VDD	P	Supple power	
18	DVDD	C	Power setting capacitor connect pin	
19	C1P	C	Capacitor for charge pump	
20	C1M	C	Capacitor for charge pump	
21	C2P	C	Capacitor for charge pump	
22	C2M	C	Capacitor for charge pump	
23	VINT1	C	Power setting capacitor connect pin	
24	C3P	C	Capacitor for charge pump	
25	C3M	C	Capacitor for charge pump	
26	VINT2	C	Power setting capacitor connect pin	
27	VINT3	C	Power setting capacitor connect pin	
28	C4P	C	Capacitor for charge pump	
29	C4M	C	Capacitor for charge pump	
30	VGH	C	Power setting capacitor connect pin	
31	VGL	C	Power setting capacitor connect pin	
32	AGND	P	Power ground	
33	FRP	O	Frame Polarity output for VCOM	
34	VCOMDC	O	VCOM DC output in	
35	VCAC	C	Power setting capacitor connect pin	
36	DRV	O	VLED boost driving signal	
37	VLED	P	LED power anode	
38	FB	P	LED power cathode	
39	VCOM	I	Panel common voltage	

Note: Matching Connector: FH26-39S-0.3SHW

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6. Absolute maximum Ratings

6.1. Electrical Absolute max. ratings

Parameter	Symbol	MIN	MAX	Unit	Remark
Supply Voltage	VDD	-0.3	5.0	V	
Input signal voltage	DB0~DB7,VCOM,SPENB,SPDA,SPCK,HSD,VSD,CLKIN	-0.3	VDD +0.3	V	

6.2. Environment Conditions

Item	Symbol	MIN	MAX	Unit	Remark
Operating Temperature	TOPR	-20	60	℃	
Storage Temperature	TSTG	-30	70	℃	

6.3. LED Backlight Absolute max. ratings

Item	Symbol	MIN	MAX	Unit	Remark
LED Forward Current	ILED	--	28	mA	One LED

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7. Electrical Specifications

7.1 Electrical characteristics

GND=0V, Ta=25℃

Item	Symbol	MIN	TYP	MAX	Unit	Remark
Supply Voltage	VDD	3.0	3.3	3.6	V	
Input Signal Voltage	VIL	0	--	0.2xVDD	V	Note
	VIH	0.8xVDD	--	VDD	V	
Output Signal Voltage	VOL	0	--	0.2xVDD	V	SPDA,FRP,VCOMDC
	VOH	0.8xVDD	--	VDD	V	

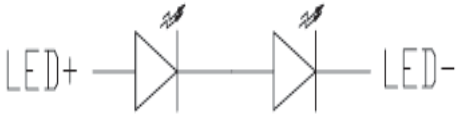
Note: DB0~DB7,VCOM,SPENB,SPDA,SPCK,HSD,VSD,CLKIN

7.2 LED Backlight

Ta=25℃

Item	Symbol	MIN	TYP	MAX	Unit	Remark
Forward Current	IF		20		mA	For one LED Note 1,2,3
Forward Voltage	VF		3.2		V	
Power Consumption	--		128		mW	

Note 1: Backlight LED Circuit:



Note 2: One LED : IF =20mA, VF=3.2V

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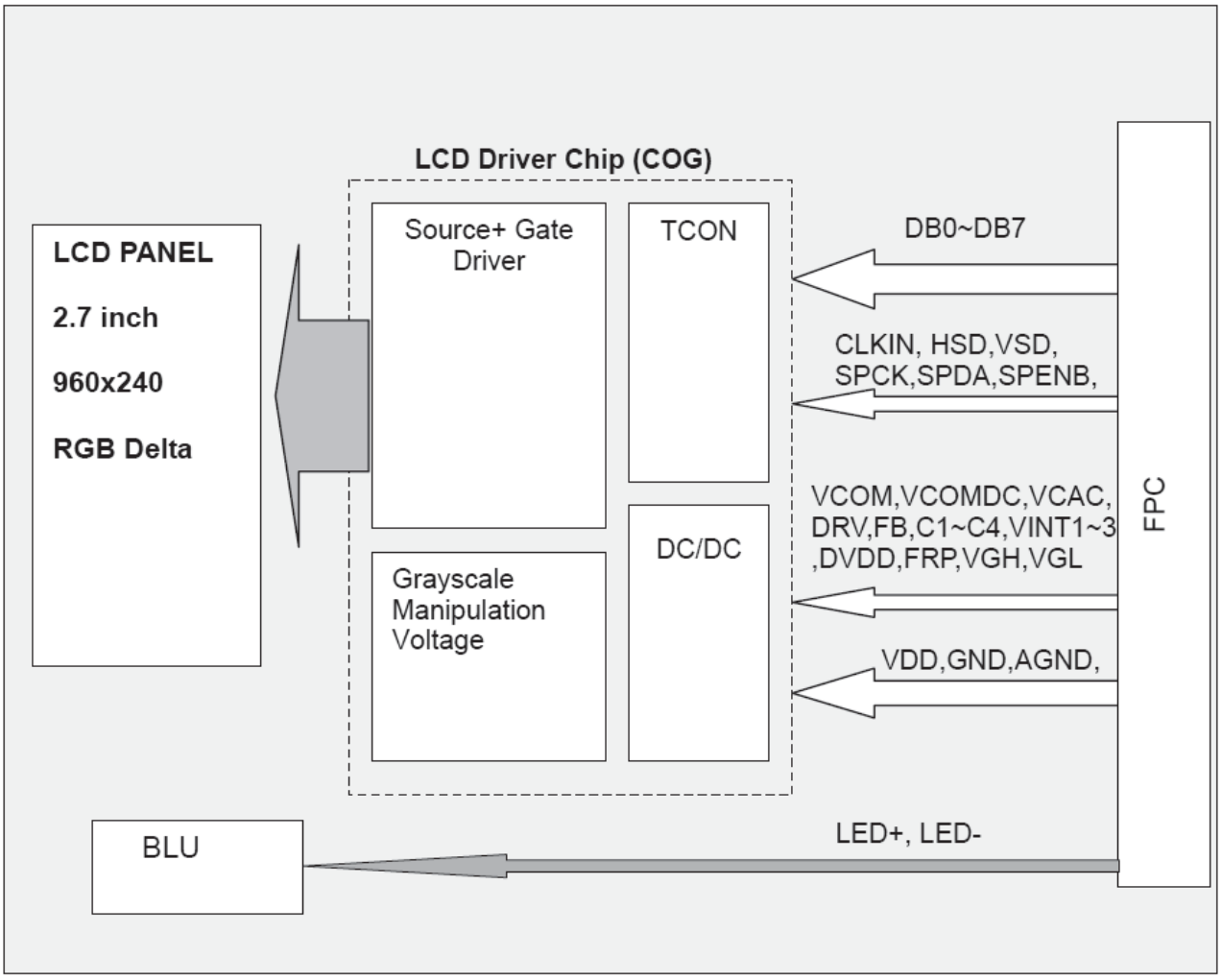
7.3 Block Diagram



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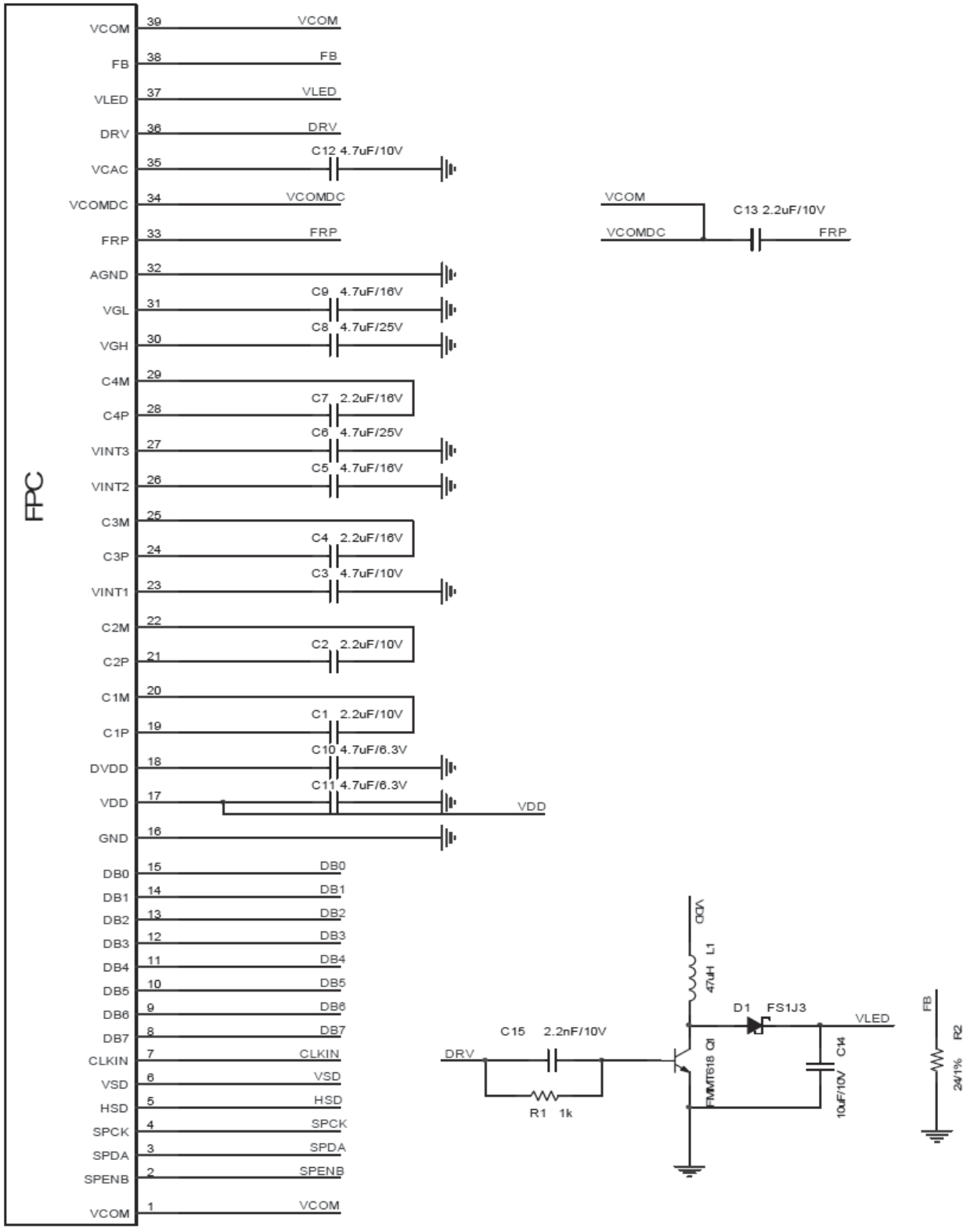
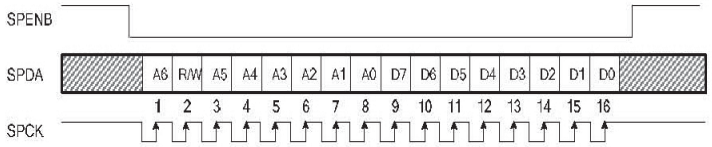
7.4 Application Circuit

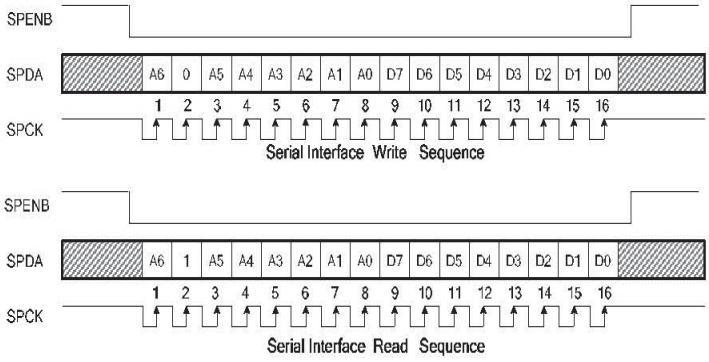


8. Command/AC Timing

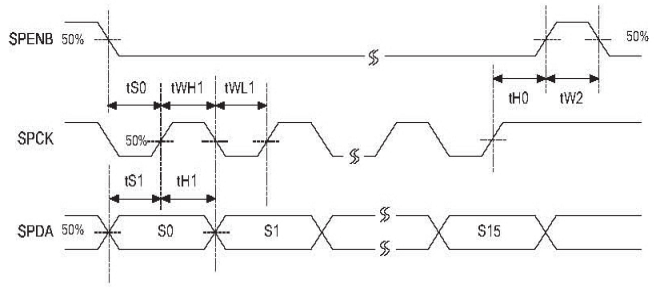
8.1 3-Wire Serial Control Interface



- Each serial command consists of 16 bits of data that is loaded one bit a time at the rising edge of serial clock SPCK. Command loading operation starts from the falling edge of SPENB and is completed at the next rising edge of SPENB.
- The serial control block is operational after power on reset, but commands are established by the VSD signal. If command is transferred multiple times for the same register, the last command before the VSD signal is valid.
- If less than 16 bits of SPCK are input while SPENB is low, the transferred data is ignored.
- If 16 bits or more of SPCK are input while SPENB is low, the last 16 bits of transferred data before the rising edge of SPENB pulse are valid data.
- Serial block operates with the SPCK clock
- Serial data can be accepted in the power save mode.



Serial Control Timing



Item	symbol	Min.	Typ.	Max.	Unit
SPENB input setup time	tS0	50			ns
SPDA input setup time	tS1	50			ns
SPENB input hold time	tH0	50			ns
SPDA input hold time	tH1	50			ns
SPCK pulse high width	tWH1	50			ns
SPCK pulse low width	tWL1	50			ns
SPENB pulse high width	tW2	400			ns

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8.2 Register Table

Register	Register Address								Default Value	Register Data (default)							
	A6	R/W	A5	A4	A3	A2	A1	A0		D7	D6	D5	D4	D3	D2	D1	D0
R00H	0	1/0	0	0	0	0	0	0	06h	Y_CbCr (0)	C601_EN (0)	x	x	VCAC (0110)			
R01H	0	1/0	0	0	0	0	0	1	51h	VCDCEN (1)	x	VCDC (21h)					
R03H	0	1/0	0	0	0	0	1	1	40h	BRIGHTNESS (40h)							
R04H	0	1/0	0	0	0	1	0	0	0Bh	NARROW (0)	C656_EN (0)	IF_SEL (00)		NP_SEL (10)		LDIR (1)	YDIR (1)
R05H	0	1/0	0	0	0	1	0	1	5Eh	DRV_SET (0)	GRB (1)	PWM_SEL (011)			VGHL_EN (1)	PWM_EN (1)	x
R06H	0	1/0	0	0	0	1	1	0	15h	HBLK_EN (0)	FB_SEL (00)		VBLK (15h)				
R07H	0	1/0	0	0	0	1	1	1	46h	HBLK (46h)							
R08H	0	1/0	0	0	1	0	0	0	00h	DRV_SEL (00)		x	x	x	x	x	x
R0BH	0	1/0	0	0	1	0	1	1	00h	REGSEL (0)	x	x	X	x	x	x	x
R0CH	0	1/0	0	0	1	1	0	0	06h	VST (00)		DE_EN (0)	CbCr (0)	DENP (0)	VSDP (1)	HSDP (1)	CLKINP (0)
R0DH	0	1/0	0	0	1	1	0	1	40h	CONTRAST (40h)							
R0EH	0	1/0	0	0	1	1	1	0	40h	x	R_CONT (40h)						
R0FH	0	1/0	0	0	1	1	1	1	40h	x	R_BRIGHT (40h)						
R10H	0	1/0	0	1	0	0	0	0	40h	x	B_CONT (40h)						
R11H	0	1/0	0	1	0	0	0	1	40h	x	B_BRIGHT (40h)						
R12H	0	1/0	0	1	0	0	1	0	00h	TRMEN (00)							
R16H	0	1/0	0	1	0	1	1	0	04h	x	x	x	x	x	GOP_EN (1)	x	x
R17H	0	1/0	0	1	0	1	1	1	54h	x	L016_SEL (101)			x	L008_SEL (100)		
R18H	0	1/0	0	1	1	0	0	0	54h	x	L050_SEL (101)			x	L032_SEL (100)		
R19H	0	1/0	0	1	1	0	0	1	43h	x	L096_SEL (100)			x	L072_SEL (011)		
R1AH	0	1/0	0	1	1	0	1	0	54h	x	L120_SEL (101)			x	L110_SEL (100)		
R2BH	0	1/0	1	0	1	0	1	1	00h	x	x	x	x	x	x	x	STB (0)
R2FH	0	1/0	1	0	1	1	1	1	61h	0	VGH_SEL (11)		CF_SET (0)	LC_SEL (00)		SOPC (01)	
R55H	1	1/0	0	1	0	1	0	1	00h	x	INV_SET (0)	x	x	x	x	x	x
R5Ah	1	1/0	0	1	1	0	1	0	02h	x	x	x	x	x	x	VGL_SEL (10)	

Notes:

1. When RSTB is low, all registers reset to default values.
2. Serial commands are executed at next VSD signal.
3. The register except upper list was for testing use, to read/write test register are not allow.

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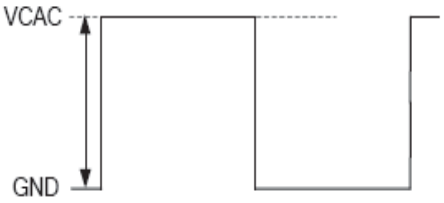
8.3 3-Wire Register Description

R00H – VCAC(R00H[3:0]): Common voltage AC level selection

D3	D2	D1	D0	VCAC voltage (V)
0	0	0	0	3.6
0	0	0	1	3.7
0	0	1	0	3.8
0	0	1	1	3.9
0	1	0	0	4.0
0	1	0	1	4.1
0	1	1	0	4.2 (default)
0	1	1	1	4.3
1	0	0	0	4.4
1	0	0	1	4.5
1	0	1	0	4.6
1	0	1	1	4.7
1	1	X	X	4.8

FRP Output



R00H – C601_EN (R00H[6]): CCIR601 input timing selection

CCIR601	Function
0	Disable CCIR601. (Default)
1	Enable CCIR601. (please refer to the table of R04H(IF_SEL) for detail description)

R00H - Y_CbCr (R00H[7]): Y & CbCr exchange position (only valid for 8-bit input YUV640 / YUV720)

	R0C[4] = '0'								R0C[4] = '1'							
Y_CbCr = '0' (Default)	Cb0	Y0	Cr0	Y1	Cb2	Y2	Cr2	Y3	Cr0	Y0	Cb0	Y1	Cr2	Y2	Cb2	Y3
Y_CbCr = '1'	Y0	Cb0	Y1	Cr0	Y2	Cb2	Y3	Cr2	Y0	Cr0	Y1	Cb0	Y2	Cr2	Y3	Cb2

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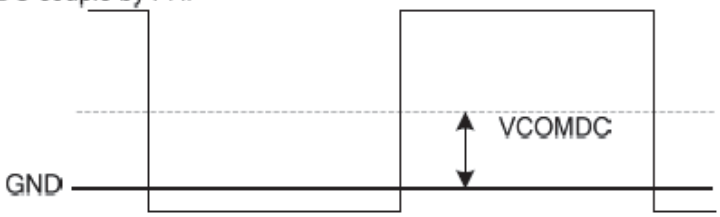
R01H – VCDC(R01H[5:0]): Common voltage DC level selection

Setting accuracy 20mV/step

D5~D0	VCOMDC Level selection
00h	0.24
:	:
21h	0.90 . (Default)
:	:
3Fh	1.5

Note: The MTP memory and 3-wire register was link to the same address in 3-wrie interface.
It will switch to MTP memory in default setting. To set REGSEL = 1 to switch to 3-wire register.

VCOMDC couple by FRP



R01H – VCDCEN(R01H[7]): VCOMDC output control

D7	VCDCE Function
0	The VCOMDC pin is disabled.
1	The VCOMDC output voltage follows VCOM DC setting. (default)

R03H - BRIGHTNESS (R03H[7:0]): RGB brightness level

Setting accuracy 1bit/step

D7~D0	Brightness gain
00h	Dark. (-64)
40h	Center (0). (default)
FFh	Bright. (+191)

R04H – YDIR (R04H[0]): Shift registers of source driver direction selection

D0	HDIR Function
0	Shift from right to left. Y1←Y2←…←Y959←Y960
1	Shift from left to right. Y1→Y2→…→Y959→Y960 (Default)

R04H - LDIR (R04H [1]): Gate driver output direction selection

D1	VDIR Function
0	Shift from down to up. L1←L2←…←L239←L240
1	Shift from up to down. L1→L2→…→L239→L240 (Default)

R04H– NP_SEL (R04H [3:2]): NTSC or PAL input mode selection

D3	D2	NTSC/PAL Mode
0	0	PAL.
0	1	NTSC.
1	x	Auto detection. (Default)

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R04H– IF_SEL (R04H [5:4]): Input format selection register

C601_EN	C656_EN	IF SEL		Input format selection
		D5	D4	
0	0	0	0	8-bit RGB. (Default)
0	0	0	1	8-bit Dummy RGB 320 x 240.
0	0	1	x	8-bit Dummy RGB 360 x 240.
0	1	x	x	CCIR656.
1	1	0	x	YUV 640.
1	1	1	0	YUV 720.

R04H– C656_EN (R04H [6]): CCIR656/CCIR601 or RGB/RGB-Dummy input selection

D6	Data format
0	RGB input. (Default)
1	CCIR656/YUV640/YUV720 input.

YUV mode is executed immediately after program.

R04H– NARROW (R04H [7]): Normal display and Narrow display selection.

D7	Function
0	Normal display. (Default)
1	Narrow display.

R04H[7] = 0

R04H[7] = 1

R05H– PWM_EN (R05H [1]): Back light power converter enable control

D1	PWM enable control
0	The DRV output is off.
1	The DRV output is controlled by STB's power on/off sequence. (Default)

R05H– VGHL_EN (R05H [2]): VGH/VGL charge pump enable control

D2	VGHL enable control
0	VGH/VGL charge pump is off, VGL will set to GND level.
1	VGH/VGL charge pump is controlled by STB's power on/off sequence. (Default)

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R05H– PWM_SEL (R05H [4:3]) : PWM duty cycle selection for back light power convert

PWM SEL			function
D5	D4	D3	PWM duty cycle
0	0	0	**55%**
0	0	1	**60%**
0	1	0	**65%**
0	1	1	**70% (Default)**
1	0	0	**75%**
1	0	1	**80%**
1	1	0	**85%**
1	1	1	**90%**

R05H– GRB (R05H [6]): Global reset control register

D6	GRB Function
0	Reset all registers to default value.
1	Normal operation. (Default)

R05H– DRV_SET (R05H [7]): DRV signal frequency setting register

D7	DRV operation frequency
0	CLKIN/64. (Default)
1	CLKIN/128.

R06H - VBLK (R06H[4:0]): Vertical blanking setting register

For 8-bit RGB, 8-bit Dummy RGB, CCIR656, YUV640 and YUV720 NTSC mode, Parallel RGB input mode (PSEL="Low"),

D4~D0	VBLK selection	Unit
00h~03h	3.	H
04h~14h	4~20	
15h	21. (Default)	
16h~1Fh	22~31	

For 8-bit Dummy RGB, CCIR656, YUV640 and YUV720 PAL mode. (Vertical blanking+3)

D4~D0	VBLK selection	Unit
00h~14h	3~23.	H
15h	24. (Default)	
16h~1Fh	25~34.	

R06H - FB_SEL (R06H[6:5]): FB pin feedback voltage selector

D6~D5	FB threshold voltage
00	0.6 V. (default)
01	0.75V.
10	0.45V.
11	0.3V.

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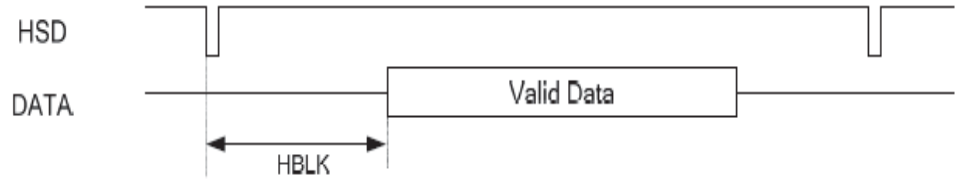
R06H/R07H – HBLK_EN(R6H[7]): HBLK function enable
HBLK (R07H[7:0]): Horizontal blanking setting

HBLK_EN	D7~D0	HBLK	Unit	NTSC/PAL Mode
X	32h~45h	50~69	CLKIN(*)	8-bit RGB.
X	46h	70		
X	47~FFh	71~255		
0	XXh	241	CLKIN(*)	8-bit Dummy RGB.
1	00h~03h	3		
	04h~FFh	4~255		
0	XXh	240	CLKIN(*)	YUV840, YUV720.
1	00h~03h	3		
	04h~FFh	4~255		
0	XXh	61	CLKIN(*)	Parallel RGB
1	04h~3Fh	4~63		

* The frequency of CLKIN is different under different input timing.



R08H –DRV_SEL(R08H[7:6]) : Backlight driving capability setting

D7	D6	DRV driving capability
0	0	Normal capability. (Default)
0	1	2 times the Normal capability.
1	0	4 times the Normal capability.
1	1	8 times the Normal capability.

R0BH – REGSEL(R0BH[7]): VCOMDC output select register

D7	REGSEL function
0	VCOMDC output voltage level was control by MTP memory. (Default)
1	VCOMDC output voltage level was control by 3-wire register memory (VCDC(R01H[5:0])). When user want to adjust the VCOMDC voltage level by R01H[5:0], user have to change the register to '1'. Refer to the "TRMEN" control register for the proper MPT write operation.

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R0CH – CLKINP(R0CH[0]):CLKIN polarity selection

D0	CLKINP Function
0	Positive polarity. (Default)
1	Negative polarity

R0CH - HSDP((R0CH[1]):HSD polarity selection

D1	HSDP Function
0	Positive polarity.
1	Negative polarity. (Default)

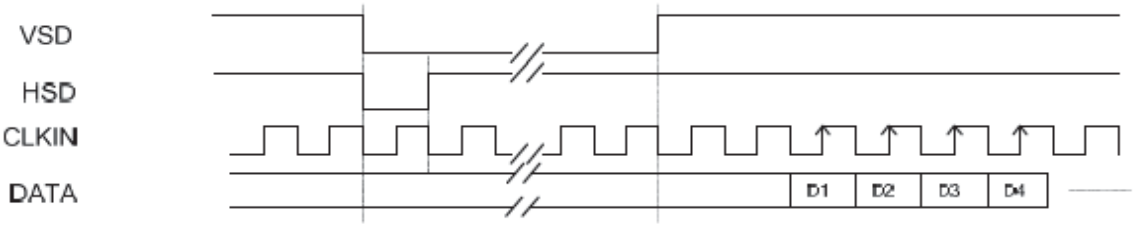
R0CH– VSDP(R0CH[2]):VSD polarity selection

D2	VSDP Function
0	Positive polarity.
1	Negative polarity. (Default)

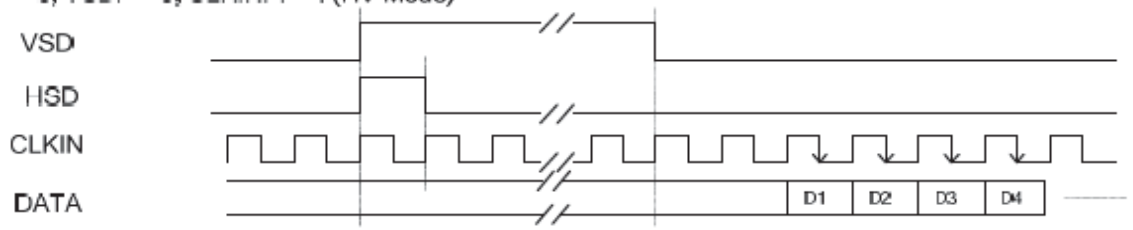
R0CH– DENP(R0CH [3]):DEN polarity selection

D3	DENP Function
0	Positive polarity (Default)
1	Negative polarity

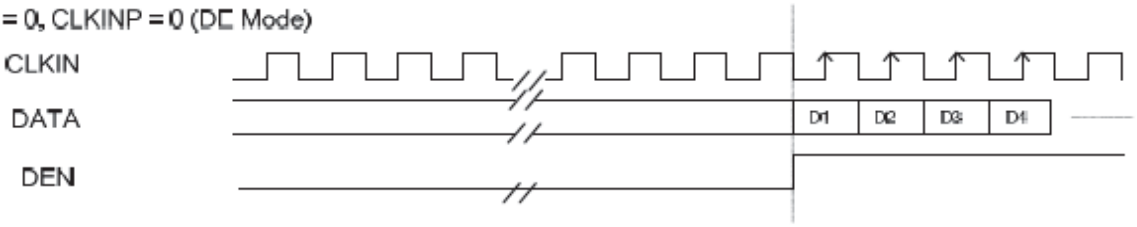
HSDP = 1, VSDP = 1, CLKINP = 0 (HV Mode)



HSDP = 0, VSDP = 0, CLKINPI = 1 (HV Mode)



DEP = 0, CLKINP = 0 (DE Mode)



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R0CH– CbCr(R0CH [4]): Cb & Cr exchange position (for CCIR656 and YUV640/YUV720)

D4	CbCr Function
0	Cb→Y→Cr. (Default)
1	Cr→Y→Cb.

R0C– DE_EN (R0C [5]):DE Mode enable control

D5	DESEL Function
0	HV mode selected. (Default)
1	DE mode selected.

* DE_EN only controls the HV and DE mode at 8-bit RGB, 8-bit Dummy RGB and Parallel Mode.

R0CH - VST(R0CH [7:6]):Vertical start time of Odd/Even Frame

8-bit RGB / 8-bit Dummy RGB NTSC / 8-bit Dummy RGB PAL(*)
Parallel RGB input mode (PSEL= "Low")

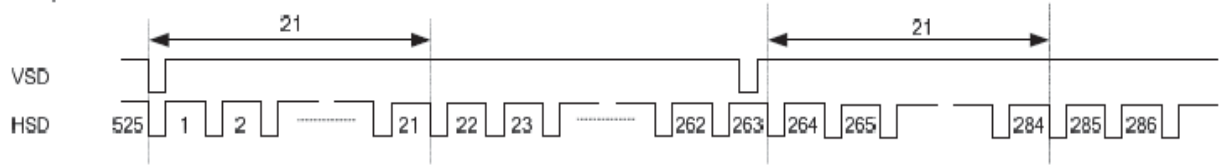
VST		VBLK	Unit
D7	D6	ODD/EVEN	
X	0	N / N. (Default)	H (Line)
X	1	N / N-1.	

CCIR656/YUV640/YUV720 NTSC/PAL(**)

VST		VBLK	Unit
D7	D6	ODD/EVEN	
0	0	N / N. (Default)	H (Line)
0	1	N / N+1.	
1	0	N+1 / N.	
1	1	N+1 / N+1.	

(*)The typical value of VBLK of 8-bit Dummy RGB PAL(24 H) is different than 8-bit RGB/8-bit Dummy RGB NTSC(21H).
(**) The typical value of VBLK of CCIR656 PAL(24 H) is different than CCIR656 NTSC(21H).
Note: VBLK must be adjusted base on the input data.

For example:



R0DH – CONTRAST(R0DH [7:0]) : RGB contrast level setting, the gain changes (1/64) / bit

D7~D0	Contrast gain
00h	0
40h	1(Default)
FFh	3.984

R0EH – R_CONT(R0EH [6:0]):Red sub-pixel contrast level setting, the gain changes (1/256)/bit

D6~D0	R Contrast gain
00h	0.75
40h	1(Default)
7Fh	1.246

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R0FH – R_BRIGHT(R0FH [6:0]):Red sub-pixel brightness level setting, setting accuracy:1 step/bit

D6~D0	R Brightness gain
00h	DARK (-64)
40h	Center (0) (Default)
7Fh	Bright (+63)

R10H – B_CONT(R10 [6:0]):Blue sub-pixel contrast level setting, the gain changes (1/256)/bit

D6~D0	B Contrast gain
00h	0.75
40h	1 (Default)
7Fh	1.246

R11H – B_BRIGHT(R11H[6:0]):Blue sub-pixel brightness level setting, setting accuracy:1 step/bit

D6~D0	B Brightness gain
00h	DARK (-64)
40h	Center(0) (Default)
7Fh	Bright (+63)

R12H –TRMEN(R12H[7:0]): VCOM DC Trim Function Control Register

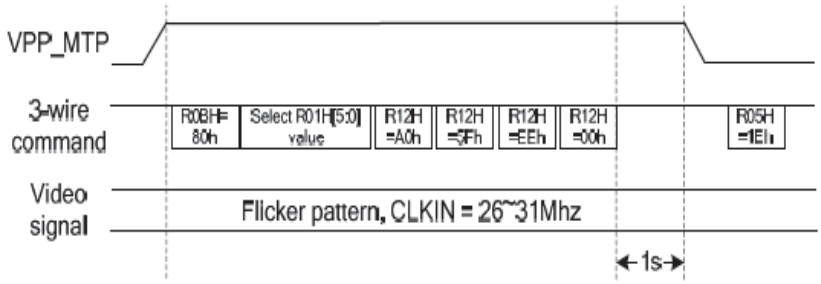
VCOMDC Trim function control register, this IC have build-in MTP memory, at Power-on, IC will auto load the MTP memory to set the VCOMDC level to prevent flick issue.

Operation condition:

1. CLKIN frequency range 26Mhz ~ 31Mhz
2. Apply 6VDC to VPPMTP pin.

Programming procedure:

1. Set REGSEL = 1 (R0BH = 80h)
2. Adjustment VCDC(R01H[5:0]) value, select proper VCOM_DC value
3. Set TRMEN[7:0] (R12H) as following sequence : A0h → 5Fh → EEh →00h.
4. Hold 1s for MTP control block operation.
5. Set global reset (set R05H = 1Eh) and restart the display operation.
6. Check the voltage level of VCOMDC pin.



Note:

1. The Trim Block can be writing only for "**2**" times.
2. After finishing TRMEN command do not power off within 1 second.
3. Trim command exceed the limit may cause the VCOMDC output unknown value.

R16H – GOP_EN(R16H[2]): Internal gamma op enable control

D2	Gamma op enable control
0	Output characteristic curve control by R17H~R1AH.
1	Output characteristic curve define by gamma correction resistor.(default)

R17H ~ R1AH

L008_SEL (R17H [2:0]): Gamma op output selection to level 8;
L016_SEL (R17H [6:4]): Gamma op output selection to level 16;
L032_SEL (R18H [2:0]): Gamma op output selection to level 32;
L050_SEL (R18H [6:4]): Gamma op output selection to level 50;
L072_SEL (R19H [2:0]): Gamma op output selection to level 72;
L096_SEL (R19H [6:4]): Gamma op output selection to level 96;
L110_SEL (R1AH [2:0]): Gamma op output selection to level 110;
L120_SEL (R1AH [6:4]): Gamma op output selection to level 120;

Reference point	000	001	010	011	100	101	110	111
L008 (100)	-100mV	-75mV	-50mV	-25mV	Default	+25mV	+50mV	+75mV
L016 (101)	-125mV	-100mV	-75mV	-50mV	-25mV	Default	+25mV	+50mV
L032 (100)	-100mV	-75mV	-50mV	-25mV	Default	+25mV	+50mV	+75mV
L050 (101)	-125mV	-100mV	-75mV	-50mV	-25mV	Default	+25mV	+50mV
L072 (011)	-75mV	-50mV	-25mV	Default	+25mV	+50mV	+75mV	+100mV
L096 (100)	-100mV	-75mV	-50mV	-25mV	Default	+25mV	+50mV	+75mV
L110 (100)	-100mV	-75mV	-50mV	-25mV	Default	+25mV	+50mV	+75mV
L120 (101)	-125mV	-100mV	-75mV	-50mV	-25mV	Default	+25mV	+50mV

R2BH – STB (R2BH [0]) : Normal / Standby mode control register

D0	STB Function
0	Standby Mode. (Default)
1	Normal operation.

R2FH – SOPC(R2FH[1:0]): Source output driving capability selection

D1	D0	Source driver capability
0	0	-25%.
0	1	Normal. (default)
1	0	+25%.
1	1	+50%.

R2FH – LC_SEL(R55H[3:2]): LC type selection register

D5	D4	LC type selection
0	0	Low Voltage LC. (Default)
0	1	Reserved
1	0	Reserved
1	1	Normal LC

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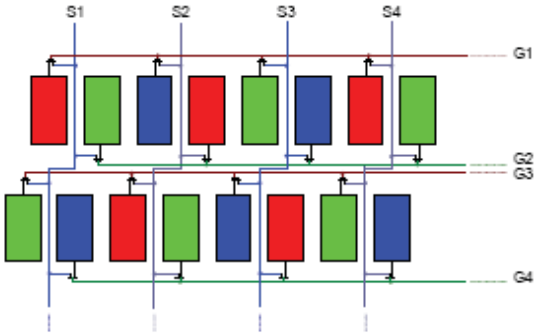
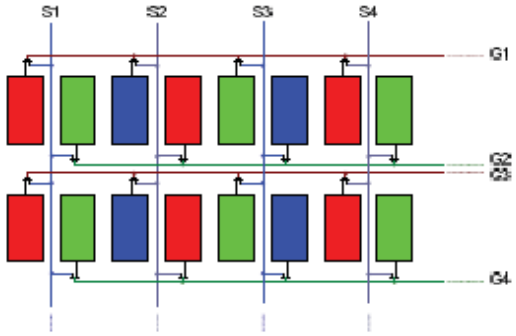
R2FH – CF_SET(R2FH[4]): Color filter selection register

CF_SET	Function
0	Delta color filter. (Default)
1	Stripe color filter.



Delta Color Filter



Stripe Color Filter

R2FH– VGH_SEL (R2FH[6:5]): VGH voltage level selection

D1	D0	VGH_SEL Function
0	0	|VGL| + 2V.
0	1	|VGL| + 3V.
1	0	|VGL| + 4V.
1	1	|VGL| + 5V. (Default)

R55H – INV_SET (R55H[6]): Inversion type selection

D6	INV_SEL Function
0	One line inversion. (Default)
1	Column inversion.

R5FH – VGL_SEL (R5FH[0:1]): VGL voltage level selection

D1	D0	VGL_SEL Function
0	0	-8V.
0	1	-9V
1	0	-10V. (Default)
1	1	-11V

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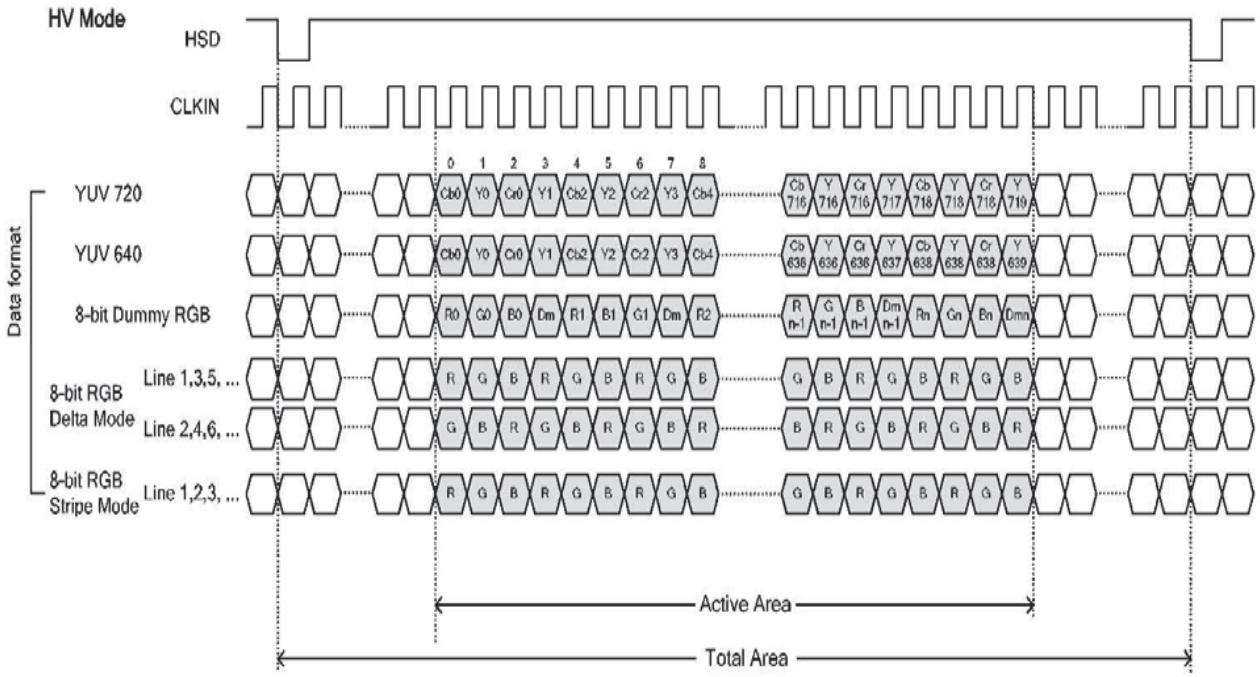
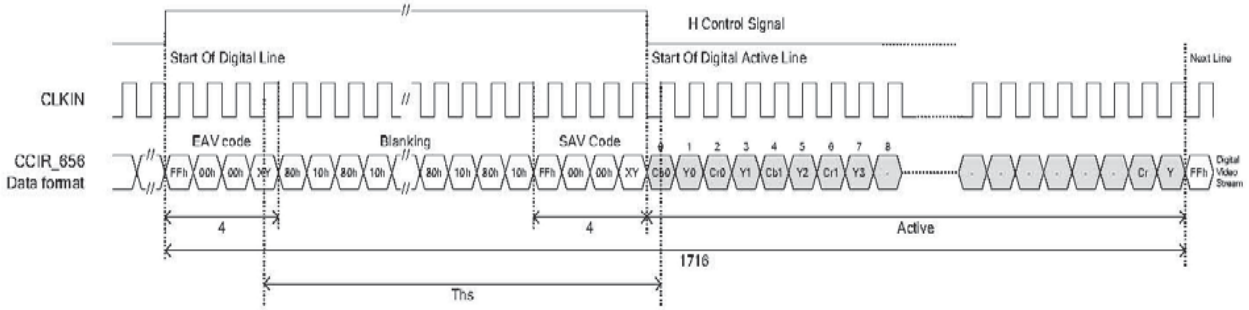
8.4 Data Input Format

Serial 8-bit RGB / 8-bit Dummy RGB / YUV Mode Data format



CCIR_656 Mode Data format



- FF 00 00 XY signals are involved with HSD,VSD and Field
- XY encode following bits:
  F=field select
  V=indicate vertical blanking
  H=1 if EAV else 0 for SAV
  P3-P0=protection bits :
  P3=V⊕H P2=F⊕H P1=F⊕V P0=F⊕V⊕H ⊕: Represents the exclusive-OR function

XY							
D7 (MSB)	D6	D5	D4	D3	D2	D1	D0
1	F	V	H	P3	P2	P1	P0

- Control is provided through "End of Video" (EAV) and "Start of Video" (SAV) timing references.
- Horizontal blanking section consists of repeating pattern 80 10 80 10

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Data Active Area

Input Format	Format Standard	CLKIN(MHz)	H	Total AREA	Active AREA
YUV	CCIR_601	fCLKIN = 27	1	1716	1440
	CCIR_656			1728	
	CCIR_601	fCLKIN = 24.54	1	1560	1280
8-bit Dummy RGB	NTSC/PAL	fCLKIN = 27	1	1560	1440
		fCLKIN = 24.54			1280
8-bit RGB	NTSC/PAL	fCLKIN = 27	1	1716	960

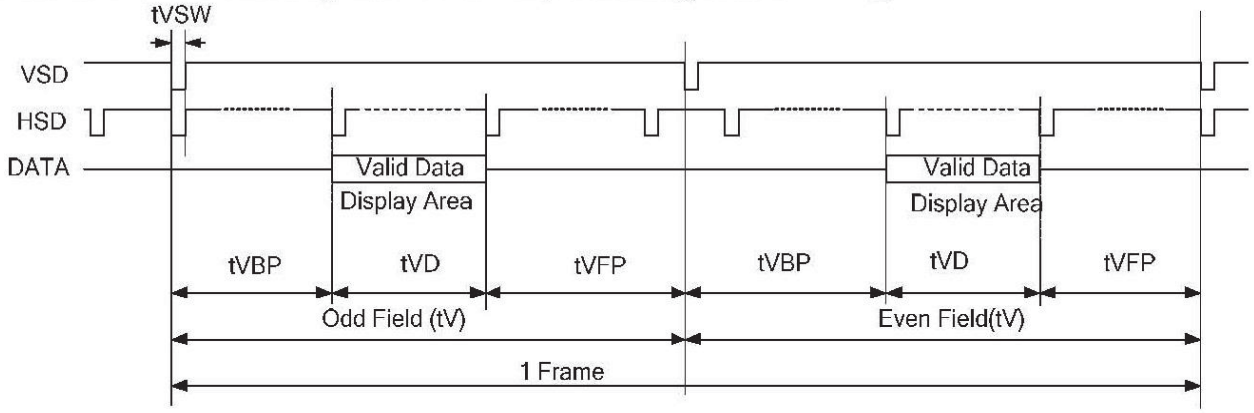
(Unit:CLKIN)

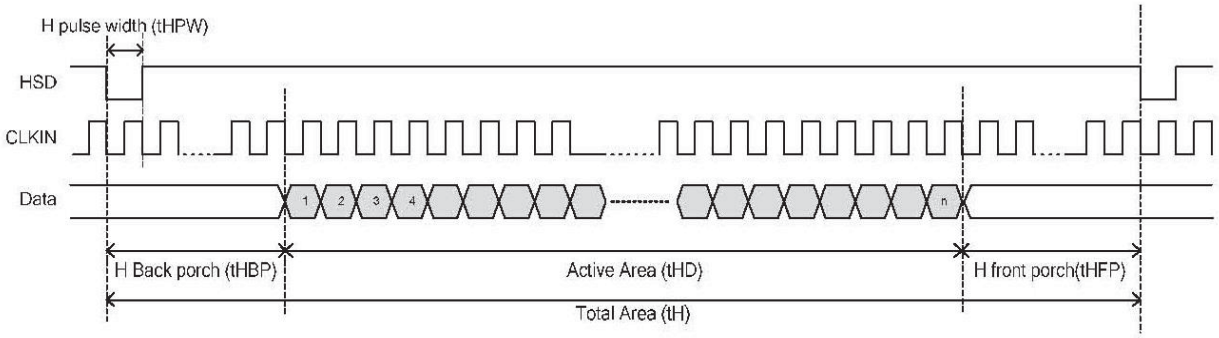
CCIR656/YUV640/YUV720 to RGB Conversion Formula

Rn = 1.164*[(Y2n-1+Y2n)/2-16] + 1.596*(Crn-128)
Gn = 1.164*[(Y2n-1+Y2n)/2-16] - 0.813*(Crn-128) – 0.392*(Cbn-128)
Bn = 1.164*[(Y2n-1+Y2n)/2-16] + 2.017*(Cbn-128)
Where Y: 16~235 Cr: 16~240 Cb: 16~240

8.5 Input Timing Format

8-bit RGB/8-bit Dummy RGB/YUV Input timing chart





8-bit RGB input timing

Parameter		Symbol	Interlace			Unit
			Min.	Typ.	Max.	
CLKIN frequency		fCLKIN	13.5	27	27.19	MHz
HSD period		tH	1024	1716	1728	CLKIN
HSD display period		tHD		960		CLKIN
HSD back porch		tHBP	50	70	255	CLKIN
HSD front porch		tHFP	14	686	718	CLKIN
HSD pulse width		tHSW	1	1	tHBP-1	CLKIN
VSD period time		tV	242.5	262.5	450.5	H
Vertical display area		tVD		240		H
VSD back porch	Odd field	tVBP	3	21	31	H
	Even field		3.5	21.5	31.5	
VSD front porch	Odd field	tVFP	1.5	1.5	179.5	H
	Even field		1	1	179	
VSD pulse width		tVSW	1 CLKIN	1CLKIN	6H	
1 Frame			485	525	901	H

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8-bit Dummy RGB input timing

8-bit Dummy RGB (320 mode/NTSC/24.535Mhz) input timing

Parameter		Symbol	Interlace			Unit
			Min.	Typ.	Max.	
CLKIN frequency		fCLKIN	20.45	24.535	30	MHz
HSD period		tH	1306	1560	1907	CLKIN
HSD display period		tHD		1280		CLKIN
HSD back porch		tHBP	3	241	255	CLKIN
HSD front porch		tHFP	25	39	372	CLKIN
HSD pulse width		tHSW	1	1	200	CLKIN
VSD period time		tV	242.5	262.5	450.5	H
Vertical display area		tVD		240		H
VSD back porch	Odd field	tVBP	3	21	31	H
	Even field		3.5	21.5	31.5	
VSD front porch	Odd field	tVFP	1.5	1.5	179.5	H
	Even field		1	1	179	
VSD pulse width		tVSW	1	1	200	CLKIN
1 Frame			485	525	901	H

8-bit Dummy RGB (320 mode/PAL/24.375Mhz) input timing

Parameter		Symbol	Interlace			Unit
			Min.	Typ.	Max.	
CLKIN frequency		fCLKIN	20.45	24.375	30	MHz
HSD period		tH	1306	1560	1920	CLKIN
HSD display period		tHD		1280		CLKIN
HSD back porch		tHBP	3	241	255	CLKIN
HSD front porch		tHFP	25	39	385	CLKIN
HSD pulse width		tHSW	1	1	200	CLKIN
VSD period time		tV	292.5	312.5	450.5	H
Vertical display area		tVD		288		H
VSD back porch	Odd field	tVBP	3	23	34	H
	Even field		3.5	23.5	34.5	
VSD front porch	Odd field	tVFP	1.5	1.5	128.5	H
	Even field		1	1	128	
VSD pulse width		tVSW	1	1	200	CLKIN
1 Frame			585	625	901	H

8-bit Dummy RGB (360 mode/NTSC/27Mhz) input timing

Parameter		Symbol	Interlace			Unit
			Min.	Typ.	Max.	
CLKIN frequency		fCLKIN	23	27	30	MHz
HSD period		tH	1466	1716	1907	CLKIN
HSD display period		tHD		1440		CLKIN
HSD back porch		tHBP	3	241	255	CLKIN
HSD front porch		tHFP	25	35	212	CLKIN
HSD pulse width		tHSW	1	1	200	CLKIN
VSD period time		tV	242.5	262.5	450.5	H
Vertical display area		tVD		240		H
VSD back porch	Odd field	tVBP	3	21	31	H
	Even field		3.5	21.5	31.5	
VSD front porch	Odd field	tVFP	1.5	1.5	179.5	H
	Even field		1	1	179	
VSD pulse width		tVSW	1	1	200	CLKIN
1 Frame			485	525	901	H

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8-bit Dummy RGB (360 mode/PAL/27Mhz) input timing

Parameter		Symbol	Interlace			Unit
			Min.	Typ.	Max.	
CLKIN frequency		fCLKIN	23	27	30	MHz
HSD period		tH	1466	1728	1920	CLKIN
HSD display period		tHD		1440		CLKIN
HSD back porch		tHBP	3	241	255	CLKIN
HSD front porch		tHFP	25	47	225	CLKIN
HSD pulse width		tHSW	1	1	200	CLKIN
VSD period time		tV	292.5	312.5	450.5	H
Vertical display area		tVD		288		H
VSD back porch	Odd field	tVBP	3	23	34	H
	Even field		3.5	23.5	34.5	
VSD Front porch	Odd field	tVFP	1.5	1.5	128.5	H
	Even field		1	1	128	
VSD pulse width		tVSW	1	1	200	CLKIN
1 Frame			585	625	901	H

YUV720 and YUV640 input timing

YUV 720 mode/NTSC input timing

Parameter		Symbol	Interlace			Unit
			Min.	Typ.	Max.	
CLKIN frequency		fCLKIN	-	27	-	MHz
HSD period		tH	-	1716	-	CLKIN
HSD display period		tHD		1440		CLKIN
HSD back porch		tHBP	-	240	-	CLKIN
HSD front porch		tHFP	-	36	-	CLKIN
HSD pulse width		tHSW	-	1	-	CLKIN
VSD period time		tV	-	262.5	-	H
Vertical display area		tVD		240		H
VSD back porch	Odd field	tVBP	-	21	-	H
	Even field		-	21.5	-	
VSD front porch	Odd field	tVFP	-	1.5	-	H
	Even field		-	1	-	
VSD pulse width		tVSW	-	1	-	CLKIN
1 Frame			-	525	-	H

YUV 720 mode/PAL input timing

Parameter		Symbol	Interlace			Unit
			Min.	Typ.	Max.	
CLKIN frequency		fCLKIN	-	27	-	MHz
HSD period		tH	-	1728	-	CLKIN
HSD display period		tHD		1440		CLKIN
HSD back porch		tHBP	-	240	-	CLKIN
HSD front porch		tHFP	-	48	-	CLKIN
HSD pulse width		tHSW	-	1	-	CLKIN
VSD period time		tV	-	312.5	-	H
Vertical display area		tVD		288		H
VSD back porch	Odd field	tVBP	-	24	-	H
	Even field		-	24.5	-	
VSD front porch	Odd field	tVFP	-	0.5	-	H
	Even field		-	0	-	
VSD pulse width		tVSW	-	1	-	CLKIN
1 Frame			-	625	-	H

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YUV 640 mode/NTSC input timing

Parameter		Symbol	Interlace			Unit
			Min.	Typ.	Max.	
CLKIN frequency		fCLKIN	-	24.535	-	MHz
HSD period		tH	-	1560	-	CLKIN
HSD display period		tHD		1280		CLKIN
HSD back porch		tHBP	-	240	-	CLKIN
HSD front porch		tHFP	-	40	-	CLKIN
HSD pulse width		tHSW	-	1	-	CLKIN
VSD period time		tV	-	262.5	-	H
Vertical display area		tVD		240		H
VSD back porch	Odd field	tVBP	-	21	-	H
	Even field		-	21.5	-	
VSD front porch	Odd field	tVFP	-	1.5	-	H
	Even field		-	1	-	
VSD pulse width		tVSW	-	1	-	CLKIN
1 Frame			-	525	-	H

YUV 640 mode/PAL input timing

Parameter		Symbol	Interlace			Unit
			Min.	Typ.	Max.	
CLKIN frequency		fCLKIN	-	24.375	-	MHz
HSD period		tH	-	1560	-	CLKIN
HSD display period		tHD		1280		CLKIN
HSD back porch		tHBP	-	240	-	CLKIN
HSD front porch		tHFP	-	40	-	CLKIN
HSD pulse width		tHSW	-	1	-	CLKIN
VSD period time		tV	-	312.5	-	H
Vertical display area		tVD		288		H
VSD back porch	Odd field	tVBP	-	24	-	H
	Even field		-	24.5	-	
VSD front porch	Odd field	tVFP	-	0.5	-	H
	Even field		-	0	-	
VSD pulse width		tVSW	-	1	-	CLKIN
1 Frame			-	625	-	H

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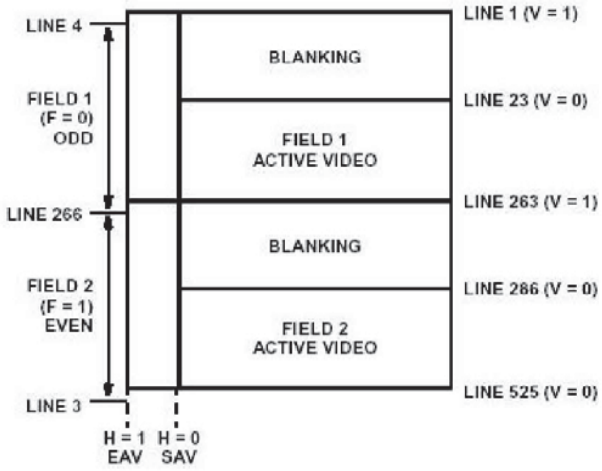
CCIR656 input timing

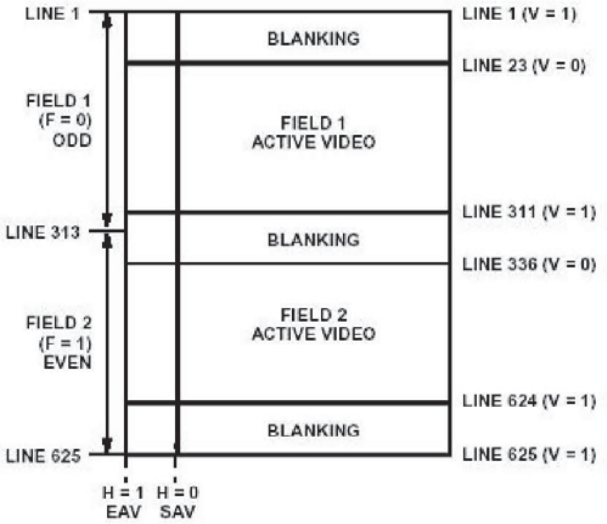
NTSC mode



LINE NUMBER	F	V	H (EAV)	H (SAV)
1-3	1	1	1	0
4-22	0	1	1	0
23-262	0	0	1	0
263-265	0	1	1	0
266-285	1	1	1	0
286-525	1	0	1	0

	F	H	V
1	EVEN Field	EAV	BLANKING
0	ODD Field	SAV	ACTIVE VIDEO

PAL mode



LINE NUMBER	F	V	H (EAV)	H (SAV)
1-22	0	1	1	0
23-310	0	0	1	0
311-312	0	1	1	0
313-335	1	1	1	0
336-623	1	0	1	0
624-625	1	1	1	0

	F	H	V
1	EVEN Field	EAV	BLANKING
0	ODD Field	SAV	ACTIVE VIDEO

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8.6 AC Electrical Characteristics

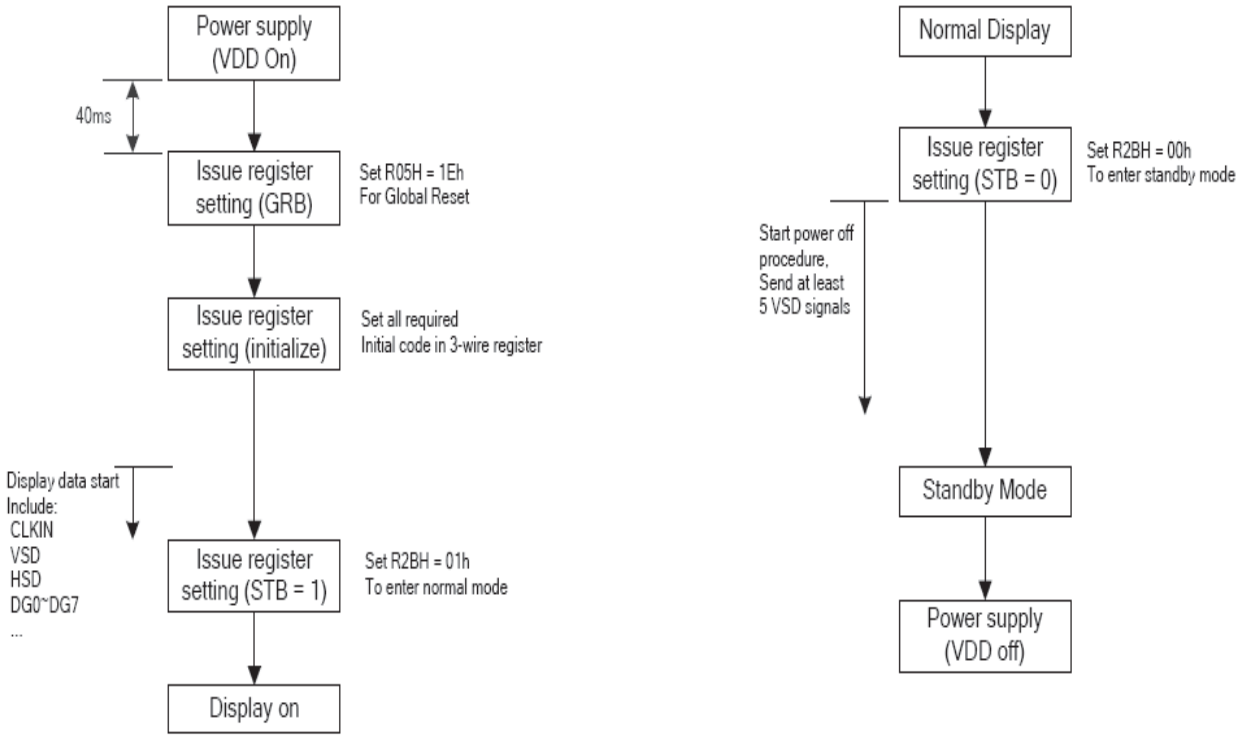
(VDD=3.0~3.6V, VDDIO=AVDD=VDD, AGND=GND=0V, TA=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
HSD period time	Th	60	63.56	67	us	
VSD setup time	Tvst	12	-	-	ns	
VSD hold time	Tvhd	12	-	-	ns	
HSD setup time	Thst	12	-	-	ns	
HSD hold time	Thhd	12	-	-	ns	
Data setup time	Tdsu	12	-	-	ns	DB0~DB7 to CLKIN
Data hold time	Tdhd	12	-	-	ns	DB0~DB7 to CLKIN
Time that VSD to 1st Gate output	Tstv	0	21	31	H	@ 8-bit RGB, 8-bit Dummy RGB NTSC, Delay by VBLK setting.
Time that CCIR_V to 1st Gate output	Tstv	0	22	31	H	@ CCIR656 NTSC, Delay by VBLK setting.
Time that CCIR_V to 1st Gate output	Tstv	3	24	34	H	@ 8-bit Dummy RGB & CCIR656 PAL, Delay by VBLK setting.
Source output setting time (*1)	Tst	-	-	8	us	R= 25K ohm , C= 30 pF 10% → 90% final.
Gate output setting time (*1)	Tstg	-	0.5	1	us	R= 3K ohm , C= 25 pF 10% → 90% final.
VCOM setting time (*1)	Tst,vcom	-	-	9	us	R= 200 ohm , C= 5 nF 10% → 90% final.
Time that HSD width	Twh	1	-	-	CLKIN	

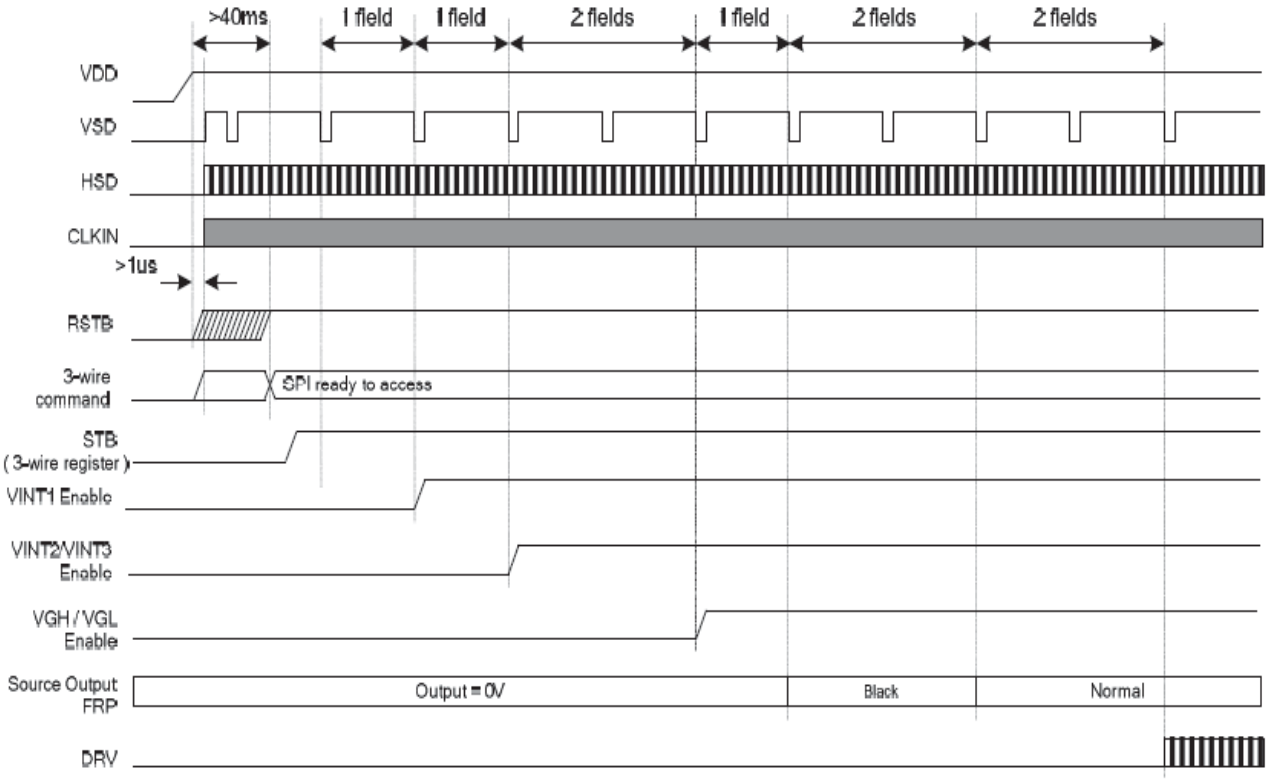
Ps. (*1) Test Condition:
When the tested signal is changed from Vo, min to Vo,max, the time that is from the start of change to the time that the swing voltage at point B is less than +/- 20 mV is called the setting time of the tested signal.

8.7 Power On/Off Sequence

8.7.1 Initialize Flow Chart



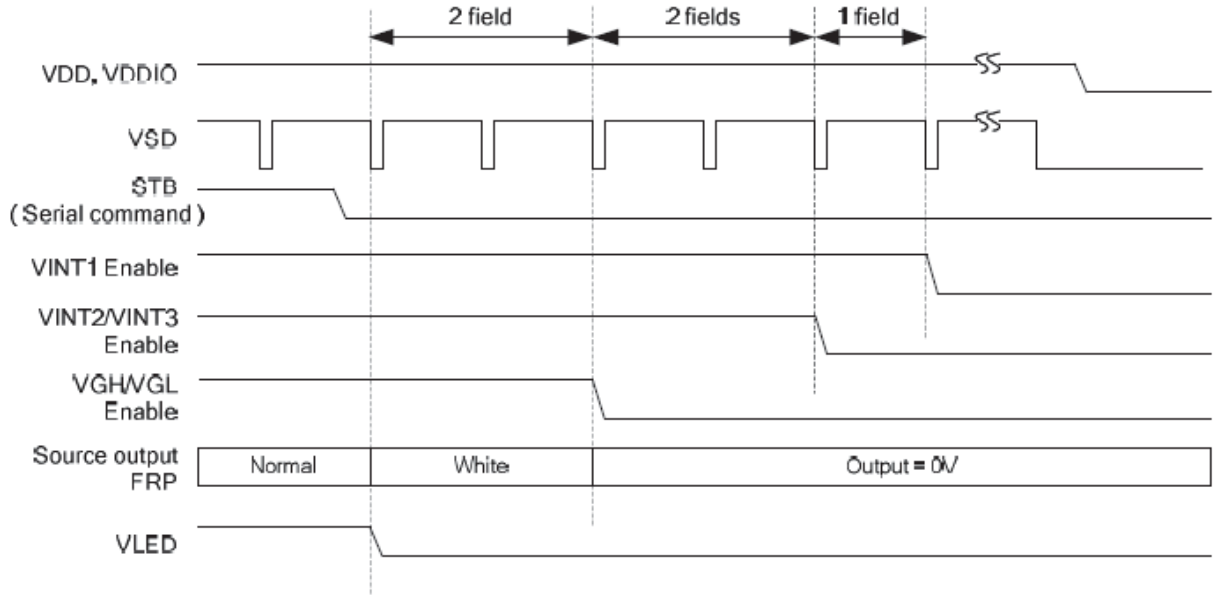
8.7.2 Power On Sequence



Note:

1. The RSTB should keep low state till VDD was stable, and set to high state before SPI command start.
2. After STB set to 1, it takes 9 VSD pulse for power on operation.

8.7.3 Power Off Sequence



Note: For properly power off operation, the extra 5 VSD pulses (or more) after STB set to low were required.

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9. Optical Specification

Ta=25℃

Item		Symbol	Condition	Min	Typ.	Max.	Unit	Remark
Contrast Ratio		CR	θ=0°	200	350	-		Note1 Note2
Response Time		Ton/ Toff	25℃	-	25	40	ms	Note1 Note3
View Angles		ΘT	CR≧10		25	-	Degree	Note 4
		ΘB			55	-		
		ΘL			50	-		
		θR			50	-		
Chromaticity	White	x	Brightness is on	0.257	0.307	0.357		Note5, Note1
		y		0.290	0.340	0.390		
	Red	x		0.540	0.590	0.640		
		y		0.300	0.350	0.400		
	Green	x		0.291	0.341	0.391		
		y		0.481	0.531	0.581		
	Blue	x		0.095	0.145	0.195		
		y		0.073	0.123	0.173		
NTSC		S			40		%	Note5
Luminance		L		230	250	-	cd/m^2	Note1 Note6
Uniformity		U		75	80	-	%	Note1 Note7

Test condition: VF=3.2V, IL=20mA(Backlight current), the ambient temperature is 25℃.

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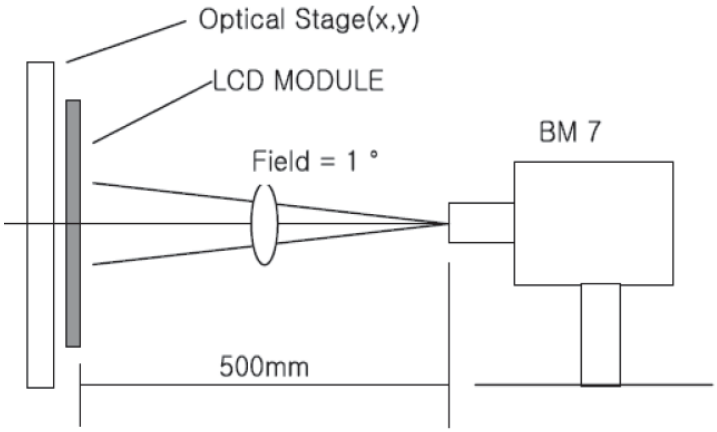
Note 1: Definition of optical measurement system.

Temperature = 25℃(±3℃)

LED back-light: ON, Environment brightness < 150 lx

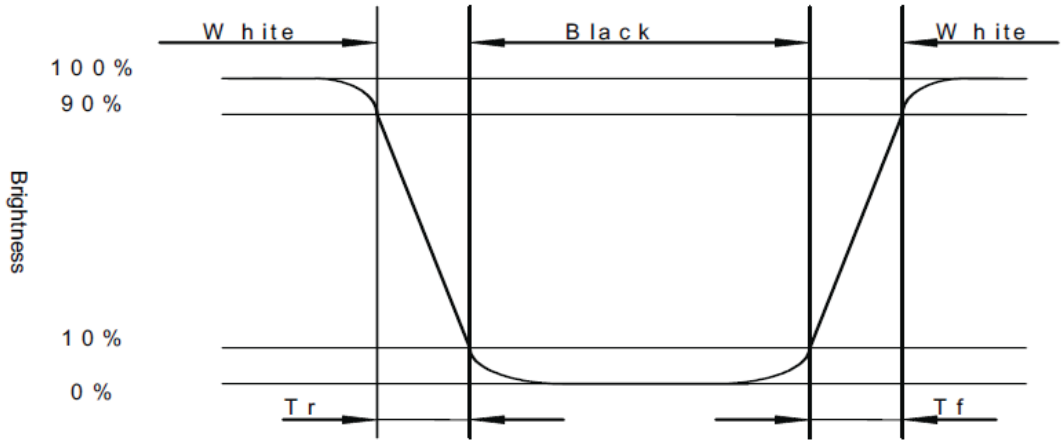


Note 2: Contrast ratio is defined as follow:

$$\text{Contrast Ratio} = \frac{\text{Surface Luminance with all white pixels}}{\text{Surface Luminance with all black pixels}}$$

Note 3: Response time is defined as follow:

Response time is the time required for the display to transition from black to white (Rise Time, Tr) and from white to black(Decay Time, Tf).



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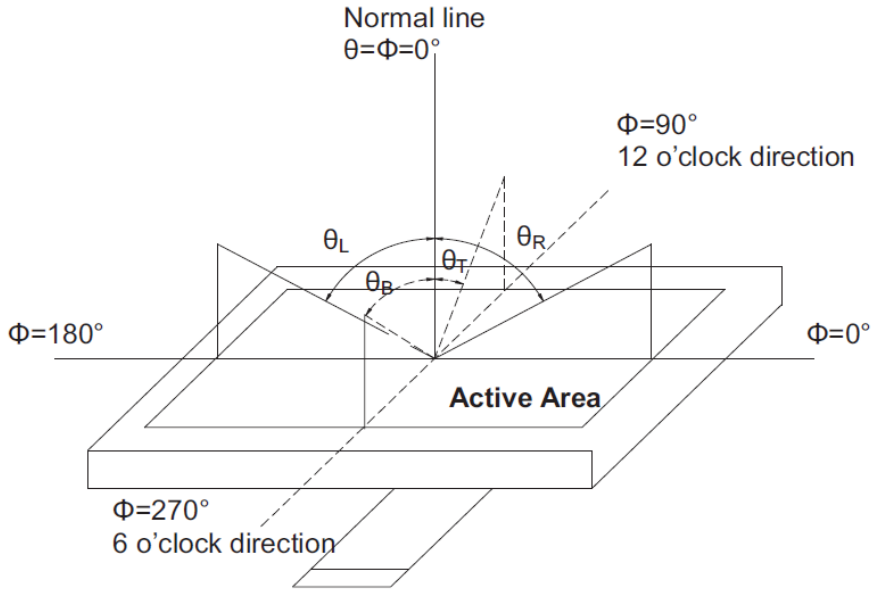
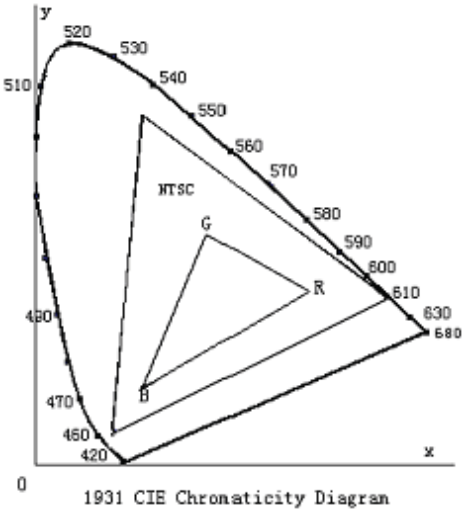
Note 4: Viewing angle range is defined as follow:

Viewing angle is measured at the center point of the LCD.



Note 5: Color chromaticity is defined as follow: (CIE1931)

Color coordinates measured at center point of LCD.



1931 CIE Chromaticity Diagram

$$S = \frac{\text{area of RGB triangle}}{\text{area of NTSC triangle}} \times 100\%$$

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Note 6: Luminance is defined as follow:

Luminance is defined as the brightness of all pixels “White” at the center of display area on optimum contrast.

Note 7: Luminance Uniformity is defined as follow:

Active area is divided into 9 measuring areas (Refer Fig. 2). Every measuring point is placed at the center of each measuring area.

$$\text{Uniformity (U)} = \frac{\text{Minimum Luminance(brightness) in 9 points}}{\text{Maximum Luminance(brightness) in 9 points}}$$

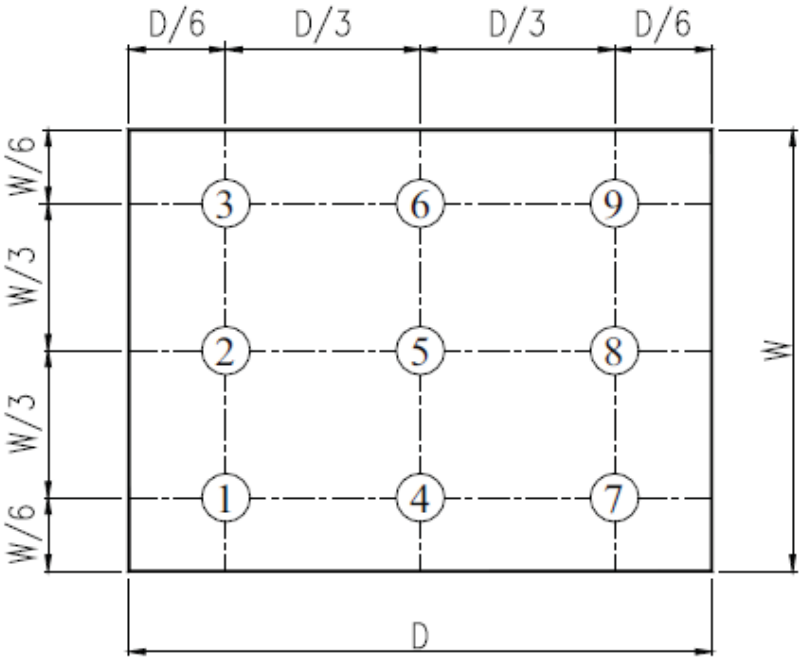

Fig. 2 Definition of uniformity

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10. Environmental / Reliability Tests

No	Test Item	Condition	Judgment criteria
1	High Temp Operation	Ts=+60℃, 120hrs	Per table in below
2	Low Temp Operation	Ta=-20℃, 120hrs	Per table in below
3	High Temp Storage	Ta=+70℃, 120hrs	Per table in below
4	Low Temp Storage	Ta=-30℃, 120hrs	Per table in below
5	High Temp & High Humidity Storage	Ta=+40℃, 90% RH 120 hours	Per table in below (polarizer discoloration is excluded)
6	Thermal Shock (Non-operation)	-30℃ 30 min~+70℃ 30 min, Change time:5min, 10 Cycles	Per table in below
7	ESD (Operation)	C=150pF, R=330Ω，5points/panel Air:±8KV, 5times; Contact:±4KV, 5 times;	Per table in below
8	Vibration (Non-operation)	Frequency range:10~55Hz, Stroke:1.5mm Sweep:10Hz~55Hz~10Hz 2 hours for each direction of X.Y.Z.	Per table in below
9	Shock (Non-operation)	60G 6ms, ±X,±Y,±Z 3times, for each direction	Per table in below
10	Package Drop Test	Height:80 cm, 1 corner, 3 edges, 6 surfaces	Per table in below

INSPECTION	CRITERION(after test)
Appearance	No Crack on the FPC, on the LCD Panel
Alignment of LCD Panel	No Bubbles in the LCD Panel No other Defects of Alignment in Active area
Electrical current	Within device specifications
Function / Display	No Broken Circuit, No Short Circuit or No Black line No Other Defects of Display

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11. Precautions for Use of LCD Modules

11.1 Safety

The liquid crystal in the LCD is poisonous. Do not put it in your mouth. If the liquid crystal touches your skin or clothes, wash it off immediately using soap and water.

11.2 Handling

A. The LCD and touch panel is made of plate glass. Do not subject the panel to mechanical shock or to excessive force on its surface.
B. Do not handle the product by holding the flexible pattern portion in order to assure the reliability
C. Transparency is an important factor for the touch panel. Please wear clear finger sacks, gloves and mask to protect the touch panel from finger print or stain and also hold the portion outside the view area when handling the touch panel.
D. Provide a space so that the panel does not come into contact with other components.
E. To protect the product from external force, put a covering lens (acrylic board or similar board) and keep an appropriate gap between them.
F. Transparent electrodes may be disconnected if the panel is used under environmental conditions where dew condensation occurs.
G. Property of semiconductor devices may be affected when they are exposed to light, possibly resulting in IC malfunctions.
H. To prevent such IC malfunctions, your design and mounting layout shall be done in the way that the IC is not exposed to light in actual use.

11.3 Static Electricity

A. Ground soldering iron tips, tools and testers when they are in operation.
B. Ground your body when handling the products.
C. Power on the LCD module before applying the voltage to the input terminals.
D. Do not apply voltage which exceeds the absolute maximum rating.
E. Store the products in an anti-electrostatic bag or container.

11.4Storage

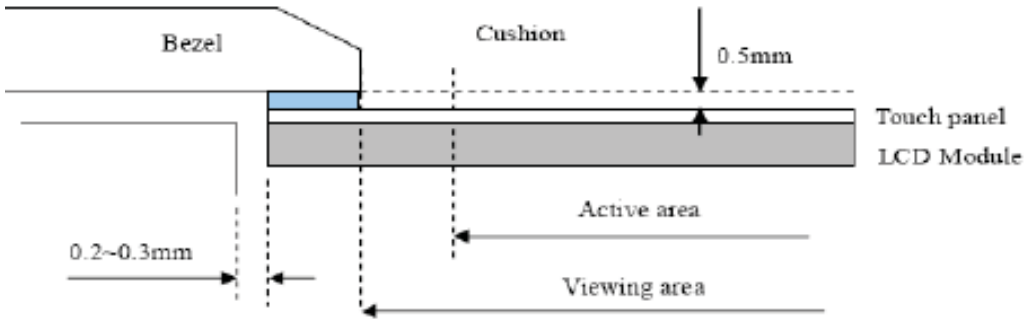
A. Store the products in a dark place at +25℃±10℃ with low humidity (40% RH to 60% RH). Don't expose to sunlight or fluorescent light.
B. Storage in a clean environment, free from dust, active gas, and solvent.

11.5 Cleaning

A. Do not wipe the touch panel with dry cloth, as it may cause scratch.
B. Wipe off the stain on the product by using soft cloth moistened with ethanol. Do not allow ethanol to get in between the upper film and the bottom glass. It may cause peeling issue or defective operation. Do not use any organic solvent or detergent other than ethanol.

11.6 Cautions for installing and assembling

Bezel edge must be positioned in the area between the Active area and View area. The bezel may press the touch screen and cause activation if the edge touches the active area. A gap of approximately 0.5mm is needed between the bezel and the top electrode. It may cause unexpected activation if the gap is too narrow. There is a tolerance of 0.2 to 0.3mm for the outside dimensions of the touch panel and tail. A gap must be made to absorb the tolerance in the case and connector.



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