DATA SHEET

(DOC No. HX8268-C-DS)

HX8268-C

480x480 TFT LCD Single Chip Digital Driver

Preliminary version 01 June, 2010

Himax Technologies, Inc.
http://www.himax.com.tw

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June, 2010

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1. General Description

HX8268-C is a 480x480 single chip digital driver with functions of 480-channels source driver (S/D), 480 channels gate driver (G/D), timing controller (TCON) with serial peripheral interface (SPI), and power supply circuits. HX8268-C is special designed for dual-gate architecture TFT panel. This chip is dedicated for the display resolution of 960*240.

HX8268-C supports 8-bit serial RGB , 24-bit parallel RGB and 8-bit Dummy RGB or BT. 601/656 interface with 8 bit data input for NTSC and PAL TV systems. It generates corresponding 256-level gray scale voltage output by source driver, which can realize 16M colors with dithering feature enabled.

The operation parameters can be set by serial peripheral interface commands from microcontroller to fine tune the functions such as display start position, improving display quality by gamma setting, and power control.

2. Features

- Generate 480x480 TFT control signals with timing controller
- Support panel resolution $960_{(Dot)}$x240
- Support 24-bit parallel RGB,8-bit RGB, 8-bit Dummy RGB, CCIR601 and CCIR656 input
- Support 3-wire serial communication control
- Internal dithering 8-bit data to 7-bit data for Source Driver Circuit
- Support stripe and delta types of panel group
- Support Interlace panel type
- Support line inversion/Column inversion.
- Build-in DC-DC control circuit, charge pump, VCOM with programmable DC/AC adjustment.
- Built-in R-DAC gamma correction.
- Operation frequency: 30 MHz max
- Power for charge pump(VDD):2.7V ~ 3.6V
- Power for digital circuits(VDD): 2.7V ~3.6V (Built-in Regulator for internal circuit)
- Power for source driver (AVDD): VDD/VINT
- Power for digital interface(VDDIO): 1.65V~VDD
- Output deviation: +/- 20mV.
- COG package.

3. Block Diagram

3.1 Block diagram

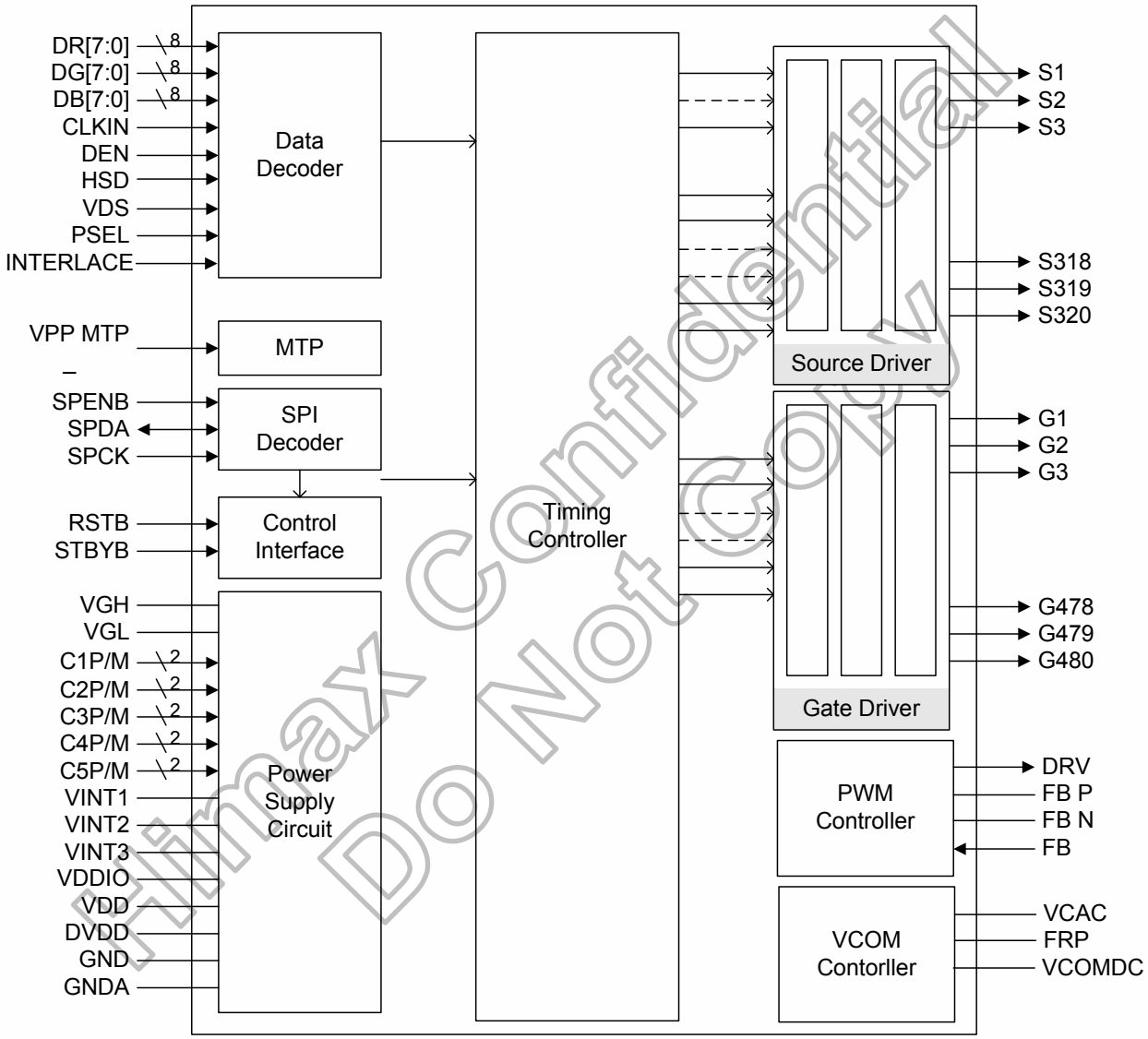


Figure 3.1: Block Diagram

4. Application Block Diagram

4.1 Charge Pump Circuit reference design

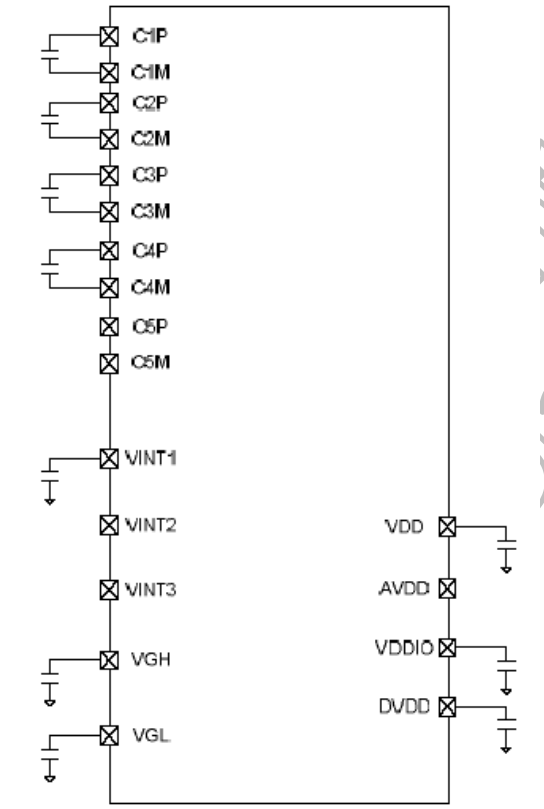


Figure 4.1: Charge pump circuit reference design

4.2 Backlight Circuit

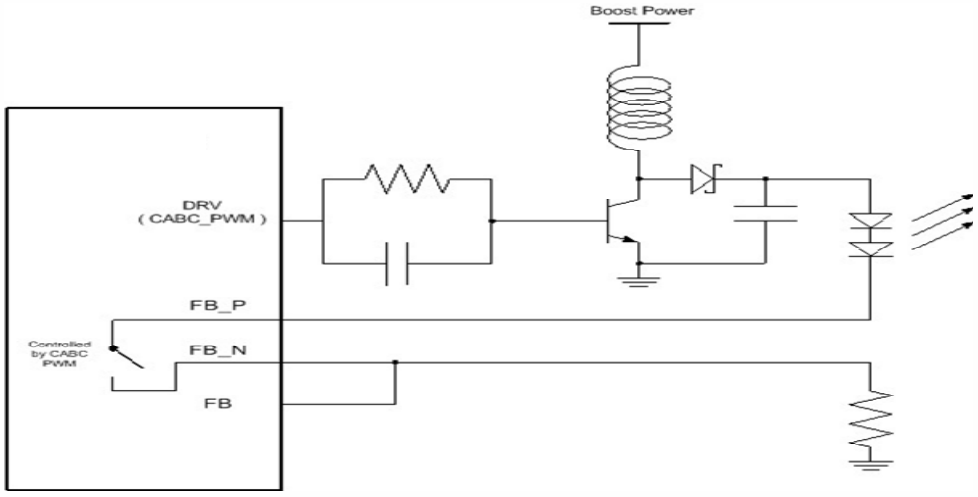


Figure 4.2: Backlight Circuit

4.3 Recommend wiring resistance values

Pad Name	Resistance (Ohm)	Pad Name	Resistance (Ohm)	Pad Name	Resistance (Ohm)
COM1_L	<=5	DG6	<=100	C1N	<=5
VPP_MTP	<=5	DG5	<=100	C2P	<=5
STBYB	<=100	DG4	<=100	C2N	<=5
RSTB	<=100	DG3	<=100	VINT	<=5
PSEL	<=100	DG2	<=100	C3P	<=5
SPENB	<=100	DG1	<=100	C3N	<=5
SPDA	<=100	DG0	<=100	C4P	<=5
SPCK	<=100	DR7	<=100	C4N	<=5
DEN	<=100	DR6	<=100	VGH	<=5
HSD	<=100	DR5	<=100	VGL	<=5
VSD	<=100	DR4	<=100	AGND	<=5
CLKIN	<=100	DR3	<=100	FRP	<=5
DB7	<=100	DR2	<=100	VCOMDC	<=5
DB6	<=100	DR1	<=100	VCAC	<=5
DB5	<=100	DR0	<=100	DRV	<=5
DB4	<=100	BGND	<=5	FB_N	<=5
DB3	<=100	VDD	<=5	FB_P	<=5
DB2	<=100	AVDD	<=5	FB	<=100
DB1	<=100	VDDIO	<=5	COM2_L	<=5
DB0	<=100	DVDD	<=5	INTLACE	<=100
DG7	<=100	C1P	<=5		

Table 4.1 Recommend wiring resistance values

4.4 Recommend value of capacitor

Pad Name	Standing voltage (V)	CAP (μF)	Pad Name	Standing voltage (V)	CAP (μF)
C1P	6.3	Cp1=1	VDD/AVDD	6.3	2.2 ~ 4.7
C1N			DVDD	6.3	2.2 ~ 4.7
C2P	6.3	Cp2=1	VINT	10	2.2 ~ 4.7
C2N			VGH	25	1 ~ 2.2
C3P	16	Cp3=1	VGL	16	1 ~ 2.2
C3N			VCAC	10	2.2 ~ 4.7
C4P	16	Cp4=1	FRP-VCOMDC	10	2.2 ~ 4.7
C4N					

Table 4.2 Recommend value of capacitor

4.5 Panel Type Selection(P_TYPE)

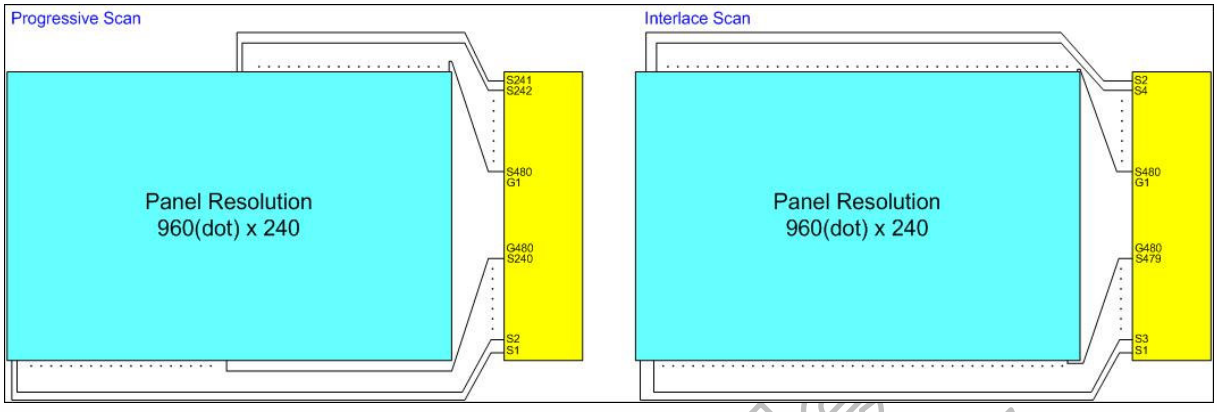


Figure 4.3 Panel Type selection(P_TYPE)

Progressive scan and Interlace scan source pad mapping table

Pad name	progressive	interlace	Pad name	progressive	interlace
S_1	S_1	S_1	S_241	S_241	S_2
S_2	S_2	S_3	S_242	S_242	S_4
S_3	S_3	S_5	S_243	S_243	S_6
S_4	S_4	S_7	S_244	S_244	S_8
S_5	S_5	S_9	S_245	S_245	S_10
S_6	S_6	S_11	S_246	S_246	S_12
S_7	S_7	S_13	S_247	S_247	S_14
S_8	S_8	S_15	S_248	S_248	S_16
S_9	S_9	S_17	S_249	S_249	S_18
S_10	S_10	S_19	S_250	S_250	S_20
:	:	:	:	:	:
:	:	:	:	:	:
S_230	S_230	S_459	S_470	S_470	S_460
S_231	S_231	S_461	S_471	S_471	S_462
S_232	S_232	S_463	S_472	S_472	S_464
S_233	S_233	S_465	S_473	S_473	S_466
S_234	S_234	S_467	S_474	S_474	S_468
S_235	S_235	S_469	S_475	S_475	S_470
S_236	S_236	S_471	S_476	S_476	S_472
S_237	S_237	S_473	S_477	S_477	S_474
S_238	S_238	S_475	S_478	S_478	S_476
S_239	S_239	S_477	S_479	S_479	S_478
S_240	S_240	S_479	S_480	S_480	S_480

Table 4.3 Progressive scan and Interlace scan source pad mapping table

5. Pin Description

Pin name	I/O	Description
VDDIO	P	Power supply for digital interface.
VDD	P	Power supply for charge pump circuit.
AVDD	P	Power supply for analog circuit. Connect to VDD for low voltage LC application and to VINT for normal voltage LC application inside IC.
DGND	P	Ground for digital circuit & charge pump .
AGND	P	Ground for analog circuit.
VGH	C	Power setting capacitor connecting pins.
VGL	C	Power setting capacitor connecting pins.
DVDD	C	Power setting capacitor connecting pins. (internal core use, typical 1.8V)
C1P/N	C	Capacitor for charge pump.
C2P/N	C	Capacitor for charge pump.
C3P/N	C	Capacitor for charge pump.
C4P/N	C	Capacitor for charge pump.
C5/P/N	C	floating
VINT1	C	Power setting capacitor connecting pins.
VINT2	C	Floating this pin
VINT3	C	Floating this pin
STBYB	I	Standby setting for testing, It should be connected to VDDIO in normal operation. If connected to ground, the IC is in standby mode. (Internal pulled high)
RSTB	I	Global reset pin, it should be connected to VDDIO in normal operation. If connected to ground, the controller is in reset state. (Internal pulled high)
COM1_L COM1_R COM2_L COM2_R	S	The internal link together between input side and output side.
PSEL	I	Parallel 24-bit and Serial 8-bit data input selection. (internal pulled high) PSEL ="High": Serial 8-bit data input through DG0~DG7. PSEL ="Low": Parallel 24-bit RGB input through DR0~DR7, DB0~DB7, DG0~DG7.
P_TYPE	I	Panel Type selection (internal pulled high) P_TYPE="High" Progressive panel type P_TYPE="Low" Interlace panel type
SPENB	I	Serial communication chip select. (internal pulled High)
SPDA	I/O	Serial communication data input.
SPCK	I	Serial communication clock input.
VPP_MTP	P	MTP power input pin (please reference to TRMEN(R18))
DEN	I	Data Input Enable. Active High to enable the data input Bus under "DE Mode". (Internal pulled low)
HSD	I	Horizontal sync input. Negative polarity. (Internal pulled high)
VSD	I	Vertical sync input. Negative polarity. (Internal pulled high)
CLKIN	I	Clock signal. Latching data at the rising edge.
DB0~DB7	I	8-bit digital Blue data input, only valid when PSEL ="Low" (Parallel mode). (Internal pulled low)
DG0~DG7	I	When PSEL ="High" These will be treated as serial 8-bit digital data input. (Including serial RGB or YUV). When PSEL ="Low" These will be treated as 8-bit digital Green data input(Parallel mode).(Internal floating)
DR0~DR7	I	8-bit digital Red data input, only valid when PSEL ="Low" (Parallel mode). (Internal pulled low)
FRP	O	Frame polarity output for panel VCOM.
VCOMDC	O	VCOM DC output.

VCAC	C	Power setting capacitor for VCOM AC.
Pin name	I/O	Description
DRV	O	Power transistor signal for back light power boost converter.
FB_P	I	ILED input and pass to one switch.(controlled by R5[1]) Note: Voltage apply to this pad should <VDD
FB_N	O	ILED output from one switch output. (controlled by R5[1]) Note: Voltage apply to this pad should < VDD
FB	I	Back light power boost converter feedback input.
S1~S480	O	Source Driver Output Signals.
G1~G480	O	Gate Driver Output Signals.
VD1	O	Light sensor output signals
VD2	O	Light sensor output signals
VD3	O	Light sensor output signals
VG1	O	Light sensor output signals
VG1	O	Light sensor output signals
VG1	O	Light sensor output signals
VS1	I	Light sensor input signals
VS2	I	Light sensor input signals
VS3	I	Light sensor input signals
TEST0~TEST3	T	Test pin for Himax only. Float these pins for normal operation.
TO0~TO7	T	Test pin for Himax only. Float these pins for normal operation.
GMAH_PAD	T	Test pin for Himax only. Float these pins for normal operation.
VERF_PAD	T	Test pin for Himax only. Float these pins for normal operation.
SHIELDINGx	SH	All SHIELDINGs are connected to GND internally, Reserved floating for normal operation.
ALIGN_T	M	For assembly alignment.
ALIGN_B	M	For assembly alignment.

6. SPI Register

6.1 Register Table

Register	Register Address								Register Data (default)							
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R00h	0	0	0	0	0	0	0	0	Y_CbCr	CCIR601			VCOM_AC			
									0	0	x		1	0	1	1
R01h	0	0	0	0	0	0	0	1	VCDCEN		VCOM_DC					
									1	x	0	1	1	1	0	0
R03h	0	0	0	0	0	0	1	1	Brightness							
									0	1	0	0	0	0	0	0
R04h	0	0	0	0	0	1	0	0	Narrow	YUV	SEL		NTSC/PAL		VDIR	HDIR
									0	0	0	0	1	0	1	1
R05h	0	0	0	0	0	1	0	1	DRV_FREQ	GRB	PWM_DUTY			VGH/L_EN	LED_EN	
									0	1	0	1	1	1	1	x
R06h	0	0	0	0	0	1	1	0	HBLK_EN	LED_Current			VBLK			
									0	0	0	1	0	1	0	1
R07h	0	0	0	0	0	1	1	1	HBLK							
									0	1	0	0	0	1	1	0
R08h	0	0	0	0	1	0	0	0	BL_DRV							
									0	0	x					
R0Bh	0	0	0	0	1	0	1	1	REGSEL							
									0	x						
R0Ch	0	0	0	0	1	1	0	0	PAIR		DESEL	CbCr	DEpol	VDpol	HDpol	CLKINpol
									0	0	0	0	0	1	1	0
R0Dh	0	0	0	0	1	1	0	1	CONTRAST							
									0	1	0	0	0	0	0	0
R0Eh	0	0	0	0	1	1	1	0	SUB-CONTRAST_R							
									×	1	0	0	0	0	0	0
R0Fh	0	0	0	0	1	1	1	1	SUB-BRIGHTNESS_R							
									×	1	0	0	0	0	0	0
R10h	0	0	0	1	0	0	0	0	SUB-CONTRAST_B							
									×	1	0	0	0	0	0	0
R11h	0	0	0	1	0	0	0	1	SUB-BRIGHTNESS_B							
									×	1	0	0	0	0	0	0
R12h	0	0	0	1	0	0	1	0	TRMEN							
									0	0	0	0	0	0	0	0
R13h	0	0	0	1	0	0	1	1	x							ENTRY_EN
																0
R16h	0	0	0	1	0	1	1	0	×					GAMMA2.2		
														1	×	
R17h	0	0	0	1	0	1	1	1	×	GMA_VP16			×	GMA_VP8		
										1	0	0		1	0	0
R18h	0	0	0	1	1	0	0	0	×	GMA_VP50			×	GMA_VP32		
										1	0	1		1	0	0
R19h	0	0	0	1	1	0	0	1	×	GMA_VP96			×	GMA_VP72		
										1	0	0		0	1	1
R1Ah	0	0	0	1	1	0	1	0	×	GMA_VP120			×	GMA_VP110		
										1	0	1		1	0	0
R2Bh	0	0	1	0	1	0	1	1	×							STB
																0
R2Fh	0	0	1	0	1	1	1	1	VGH_SEL			CF_SEL	LC_TYPE		SOPC	
									0	1	1	0	1	1	0	1
R3Ch	0	0	0	1	0	1	1	1	×	GMA_VP127			×	GMA_VP0		
										0	1	1		1	0	0
R3Dh	0	0	0	1	1	0	0	0	×	GMA_VPN127			×	GMA_VN0		
										0	1	0		1	0	1
R3Eh	0	0	0	1	1	0	0	1	×	GMA_VN16			×	GMA_VN8		
										1	0	0		1	0	0
R3Fh	0	0	0	1	1	0	1	0	×	GMA_VN50			×	GMA_VN32		
										1	0	1		1	0	0
R40h	0	0	0	1	1	0	0	0	×	GMA_VN96			×	GMA_VN72		
										1	0	0		0	1	1
R41h	0	0	0	1	1	0	0	1	×	GMA_VN120			×	GMA_VN110		
										1	0	1		1	0	0
R4Fh	0	0	0	1	1	1	1	1	×	ID						
										0	0	0	1	0	0	1
R55h	1	0	0	1	0	1	0	1	×	INV_SEL	DAT_INV					
										0	0			x		
R57h	1	0	0	1	0	1	1	1	×	VGHL_ENB						
										0	x					
R5Ah	1	0	0	1	1	0	1	0	x					VGL_SEL		
														0	1	0

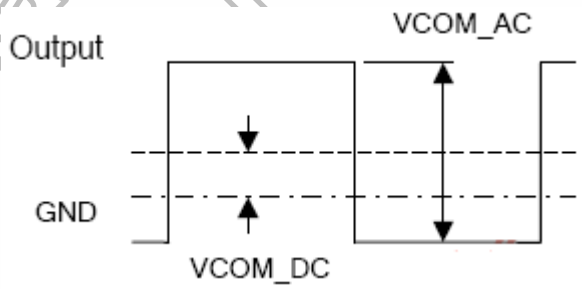
6.2 Register Description

R00h：Data Format & VCOM AC Setting

Address								Data setting							
A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	Y_Cb Cr	CCIR601	-	-	VCOM_AC			
Initial setting value (default)								0	0	-	-	1	0	1	1

VCOM_AC : Common voltage AC level selection

D3	D2	D1	D0	LV LC (V)	NV LC-1 (V)	NV LC-2 (V)
0	0	0	0	3.7	4.0	5.0
0	0	0	1	3.8	4.1	5.1
0	0	1	0	3.9	4.2	5.2
0	0	1	1	4.0	4.3	5.3
0	1	0	0	4.1	4.4	5.4
0	1	0	1	4.2	4.5	5.5
0	1	1	0	4.3	4.6	5.6
0	1	1	1	4.4	4.7	5.7
1	0	0	0	4.5	4.8	5.8
1	0	0	1	4.6	4.9	5.9
1	0	1	0	4.7	5.0	6.0
1	0	1	1	4.8 (**default**)	5.1 (**default**)	6.1 (**default**)
1	1	0	0	4.9	5.2	6.2
1	1	0	1	5.0	5.2	6.2
1	1	1	0	5.1	5.2	6.2
1	1	1	1	5.2	5.2	6.2



CCIR601 : CCIR601 input timing selection

CCIR601	Function
0	Disable CCIR601. (Default)
1	Enable CCIR601. (please refer to the table of R4(SEL) for detail description)

Y_CbCr : Y & CbCr exchange position (only valid for 8-bit input YUV640 / YUV720)

Y_CbCr	CbCr (R12[4])															
	0								1							
0	Cb0	Y0	Cr0	Y1	Cb2	Y2	Cr2	Y3	Cr0	Y0	Cb0	Y1	Cr2	Y2	Cb2	Y3
1	Y0	Cb0	Y1	Cr0	Y2	Cb2	Y3	Cr2	Y0	Cr0	Y1	Cb0	Y2	Cr2	Y3	Cb2

R01h：VCOM DC Setting

Address								Data setting							
A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	1	VCDCE	-	VCOM_DC					
Initial setting value (default)								1	-	1	0	1	1	0	0

VCOM_DC: Common voltage DC level selection (20mV/step)

D[5:0]	VCOM DC offset
00h	0.24
:	:
1Ch	**0.8** (**default**)
3Fh	1.5

VCDCE : VCOM DC enable control

VCDCE	Function
0	VCOM_DC function disabled. The VCOMDC pin is disabled
1	VCOM_DC function enabled. The VCOMDC voltage follows VCOM_DC setting. (default)

R03h：Whole Brightness Adjustment

Address								Data setting							
A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	1	1	Brightness							
Initial setting value (default)								0	1	0	0	0	0	0	0

Brightness : Adjust RGB Brightness

D7~D0	Brightness gain
00h	Dark(-64)
40h	Center(0)(default)
FFh	Bright(+191)

Setting accuracy 1bit/step

R04h：

Address								Data setting							
A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	1	0	0	Narrow	YUV	SEL		NTSC/PAL		VDIR	HDIR
Initial setting value (default)								0	0	0	0	1	0	1	1

HDIR : Shift registers of source driver direction selection

D0	HDIR Function
0	Shift from right to left. Y0 Y1 … Yn-1 Yn
1	Shift from left to right. Y0 Y1 … Yn-1 Yn (Default)

VDIR : Gate driver output direction selection

D1	VDIR Function
0	Shift from down to up. L0 L1 … L239 L240
1	Shift from up to down. L0 L1 … L239 L240 (Default)

NTSC/ PAL : NTSC or PAL input mode selection

D3	D2	NTSC/PAL Mode
0	0	PAL.
0	1	NTSC.
1	x	Auto detection. (Default)

SEL : Input data timing format selection

CCIR601	YUV	SEL		Input Timing format
		D5	D4	
0	0	0	0	8-bit RGB. (Default)
0	0	0	1	8-bit Dummy RGB 320 x 240.
0	0	1	x	8-bit Dummy RGB 360 x 240.
0	1	x	x	CCIR656.
1	1	0	x	YUV 640.
1	1	1	0	YUV 720.

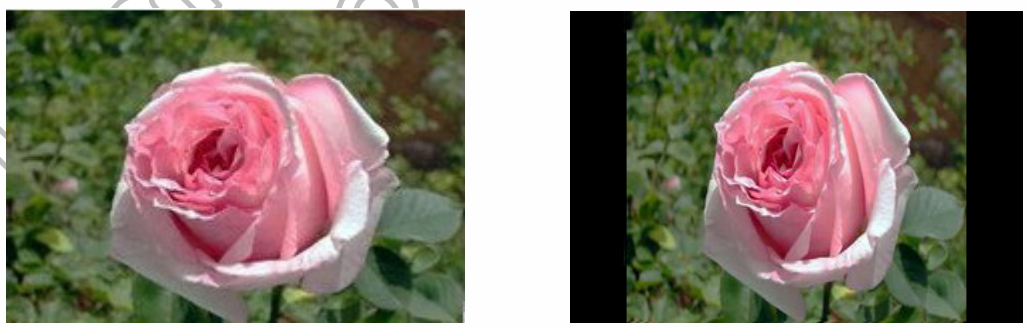
YUV : YUV(CCIR656) or RGB input selection

D6	Data format
0	RGB input. (Default)
1	CCIR656/YUV640/YUV720 input.

Narrow : Normal display and Narrow display selection

D7	Function
0	Normal display. (Default)
1	Narrow display

Note: Narrow function was not supporting 8-bit RGB and 24-bit RGB input mode.



Narrow = 0 Narrow = 1

Figure 6.1 The Narrow function

R05h :

Address								Data setting							
A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	1	0	1	DRV_ RREQ	GRB	PWM_DUTY			VGH/L_ EN	LED_ EN	-
Initial setting value (default)								0	1	0	1	1	1	1	-

LED_EN : Shut down for back light power converter

D1	LED_EN Function
0	The back light power converter is off.
1	The back light power converter is controlled by STB's power on/off sequence. (Default)

VGH/L_EN : Shut down for VGH/VGL charge pump

D1	VGH/L_EN Function
0	VGH/VGL charge pump is off.
1	VGH/VGL charge pump is controlled by STB's power on/off sequence. (Default)

PWM_DUTY : PWM duty cycle selection for back light power convert

PWM_DUTY			Function
D5	D4	D3	PWM duty cycle
0	0	0	20%
0	0	1	26%
0	1	0	32%
0	1	1	38% (Default)
1	0	0	44%
1	0	1	50%
1	1	0	56%
1	1	1	62%

GRB : Global reset

D6	GRB Function
0	Reset all registers to default value.
1	Normal operation. (Default)

DRV_FREQ : DRV signal frequency setting

D7	GRB Function
0	High frequency (Default)
1	Low frequency

R06h :

Address								Data setting							
A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	1	1	0	HBLK_EN	LED_Current		VBLK				
Initial setting value (default)								0	0	0	1	0	1	0	1

VBLK : Vertical blanking setting for 8-bit RGB , 8-bit Dummy RGB & CCIR656

For 8-bit RGB, 8-bit Dummy RGB, CCIR656, YUV640 and YUV720 NTSC mode, parallel RGB mode(PSEL=0)

D[4:0]	Function	Unit
00h~03h	3	H(Line)
04h	4	
15h	21(Default)	
1Fh	31	

For 8-bit Dummy RGB, CCIR656, YUV640 and YUV720 PAL mode. (Vertical blanking+3)

D[4:0]	Function	Unit
00h	3	H(Line)
04h	7	
15h	24(Default)	
1Fh	34	

LED_CURRENT : LED current adjustable for DC-DC feedback threshold voltage

D[6:5]	Feedback Threshold Voltage
00	0.6 V. (default)
01	0.75V.
10	0.45V.
11	0.3V.

HBLK_EN : HBLK function enable

D[7]	HBLK EN Function
0	Disable(**default**)
1	Enable

R07h：Horizontal Blanking Setting

Address								Data setting							
A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	1	1	1	HBLK							
Initial setting value (default)								0	1	0	0	0	1	1	0

HBLK : Horizontal blanking setting

HBLK_EN	D7~D0	HBLK	Unit	NTSC/PAL Mode
X	32h~45h	50~69	CLKIN	8-bit RGB.
X	46h	70		
X	47h~FFh	71~255		
0	X	241		8-bit Dummy RGB.
1	00h~03h	3		
	04h~FFh	4~255		
0	XXh	240		YUV640, YUV720.
1	00h~03h	3		
	04h~FFh	4~255		
0	X	61		Parallel RGB
1	04h~3Fh~	4~63		

R08h：Backlight Driving Capacity Setting

Address								Data setting							
A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	0	0	0	BL_DRV		-	-	-	-	-	-
Initial setting value (default)								0	0	-	-	-	-	-	-

BL_DRV : Backlight driving capability setting

D7	D6	BL_DRV capability
0	0	Normal capability. (Default)
0	1	2 times the Normal capability.
1	0	4 times the Normal capability.
1	1	8 times the Normal capability.

R0Bh：MTP

Address								Data setting							
A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	0	1	1	REGSEL	-	-	-	-	-	-	-
Initial setting value (default)								0	-	-	-	-	-	-	-

REGSEL：MTP function control register

D7	REGSEL Function
0	VCOM_DC[5:0] is read from MTP memory. (Default)
1	VCOM_DC[5:0] is switch to the 3-wire register memory when user want to adjust the VCOMDC level for test

R0Ch：

Address								Data setting							
A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	1	0	0	PAIR		SESEL	CbCr	DEpol	VDpol	HDpol	CLKINpol
Initial setting value (default)								0	0	0	0	0	1	1	0

CLKINpol：CLKIN polarity selection

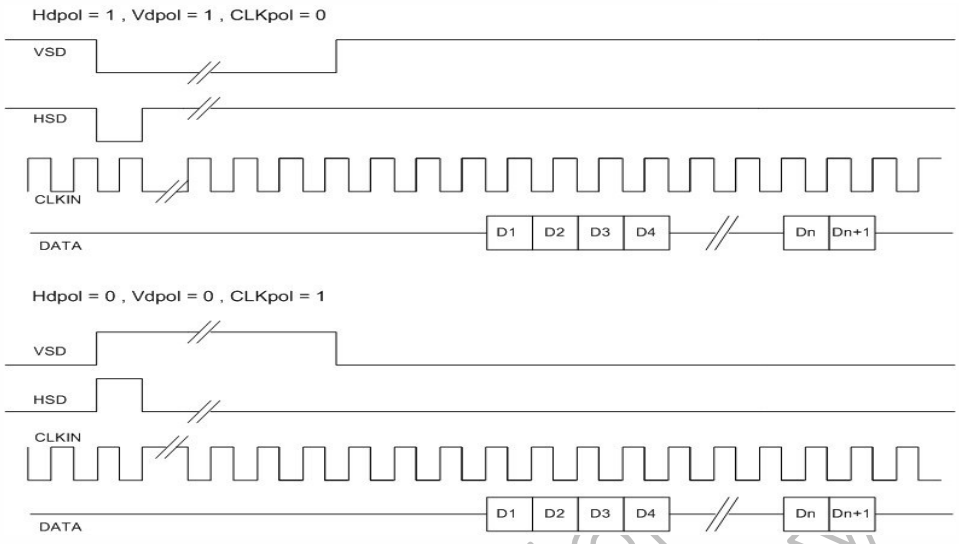
D0	CLKINpol Function
0	Positive polarity. (Default)
1	Negative polarity

HDpol：HSD polarity selection

D1	HDpol Function
0	Positive polarity.
1	Negative polarity. (Default)

VDpol：VSD polarity selection

D2	VDpol Function
0	Positive polarity.
1	Negative polarity. (Default)



DEpol：DEN polarity selection

D3	DEpol Function
0	Positive polarity (Default)
1	Negative polarity

CbCr：Cb & Cr exchange position (valid for CCIR656 and YUV640/YUV720)

D4	CbCr Function
0	Cb Y Cr. (Default)
1	Cr Y Cb

DESEL：DE Mode selection

D5	DESEL Function
0	HV mode selected. (Default)
1	DE mode selected.

DESEL only controls the HV and DE mode at 8-bit RGB, 8-bit Dummy RGB and Parallel Mode.

PAIR：Vertical start time of Odd/Even Frame

PAIR		VBLK	Unit
D7	D6	ODD/EVEN	
-	0	21/21. (Default)	H (Line)
-	1	21/20.	

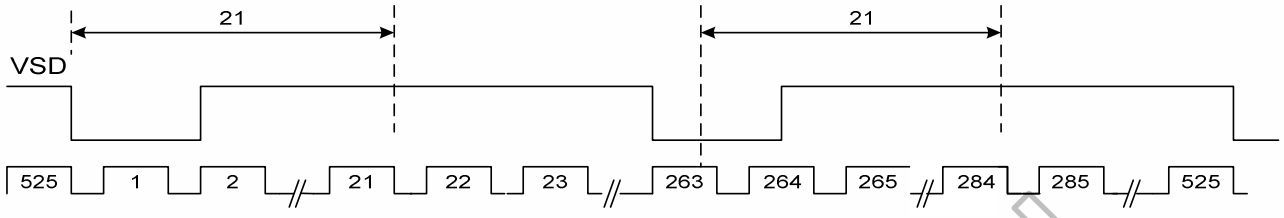
For 8-bit RGB / 8-bit Dummy RGB NTSC / 8-bit Dummy RGB PAL, parallel RGB mode(PSEL=0)
The typical value of VBLK of 8-bit Dummy RGB PAL(24 H) is different than 8-bit RGB/8-bit Dummy RGB NTSC(21H)

PAIR		VBLK	Unit
D7	D6	ODD/EVEN	
0	0	21/21. (Default)	H (Line)
0	1	21/22.	
1	0	22/21.	
1	1	22/22.	

For CCIR656/YUV640/YUV720 NTSC/PAL
The typical value of VBLK of CCIR656 PAL(24 H) is different than CCIR656 NTSC(21H).

Note: Vertical blanking must be adjusted base on the input data.

For example:



R0Dh：Whole Contrast Adjustment

Address								Data setting							
A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	1	0	1	CONTRAST							
Initial setting value (default)								0	1	0	0	0	0	0	0

CONTRAST : RGB contrast level setting , the gain changes (1/64) / bit

D[7:0]	Contrast gain
00h	0
40h	1 (Default)
FFh	3.984

R0Eh：R Contrast Adjustment

Address								Data setting							
A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	1	1	0	-	SUB-CONTRAST_R						
Initial setting value (default)								-	1	0	0	0	0	0	0

SUB-CONTRAST_R : Red sub-pixel contrast level setting, the gain changes (1/256)/bit

D[6:0]	R Contrast gain
00h	0.75
40h	1 (Default)
7Fh	1.246

R0Fh：R Brightness Adjustment

Address								Data setting							
A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	1	1	1	-	SUB-BRIGHTNESS_R						
Initial setting value (default)								-	1	0	0	0	0	0	0

SUB-BRIGHTNESS_R：Red sub-pixel brightness level setting, setting accuracy:1 step/bit

D[6:0]	R Brightness gain
00h	DARK (-64)
40h	Center (0) (Default)
7Fh	Bright (+63)

R10h：B Contrast Adjustment

Address								Data setting							
A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	0	0	0	-	SUB-CONTRAST_B						
Initial setting value (default)								-	1	0	0	0	0	0	0

SUB-CONTRAST_B：Blue sub-pixel contrast level setting, the gain changes (1/256)/bit

D[6:0]	B Contrast gain
00h	0.75
40h	1 (Default)
7Fh	1.246

R11h：B Brightness Adjustment

Address								Data setting							
A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	0	0	1	-	SUB-BRIGHTNESS_B						
Initial setting value (default)								-	1	0	0	0	0	0	0

SUB-BRIGHTNESS_B：Blue sub-pixel brightness level setting, setting accuracy:1 step/bit

D6~D0	B Brightness gain
00h	DARK (-64)
40h	Center(0) (Default)
7Fh	Bright (+63)

R12h：Instruction for OTP

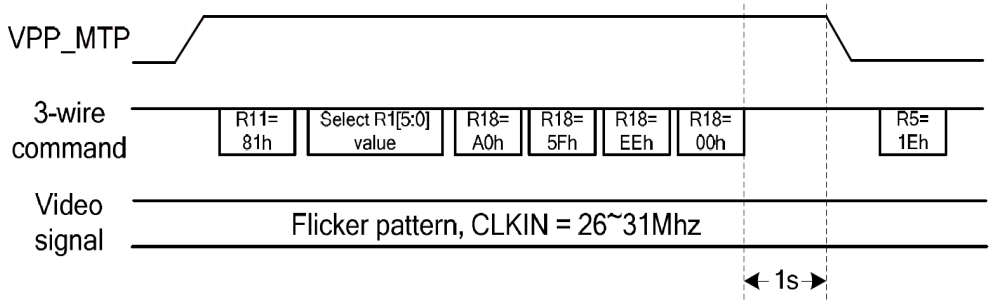
Address								Data setting							
A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	0	1	0	TRMEN							
Initial setting value (default)								0	0	0	0	0	0	0	0

TRMEN：VCOM DC Trim Function Control Register

VCOMDC Trim function control register, this IC have build-in MTP memory, at Power-on, IC will auto load the MTP memory to set the VCOMDC level to prevent flick issue.

Operation condition:
1. CLKIN frequency range 26Mhz ~ 31Mhz
2. Apply 7.5V to VPPMTP pin.

Programming procedure:
1. Set REGSEL = 1
2. Adjustment VCOM_DC(R1[5:0]) value, select proper VCOM_DC value
3. Set TRMEN[7:0] as following sequence : **A0h 5Fh EEh 00h**.
4. Hold 1s for MTP control block operation.
5. Set global reset (set R5[6] = 1) and restart the display operation.
6. Check the VCOMDC value.



Note:(1) The Trim Block can be writing only for "3" times.
(2) After finishing TRMEN command do not power off within 1 second.
(3) Trim command exceed the limit may cause the VCOMDC output unknown value.

R13h：Entry Function Control

Address								Data setting							
A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	0	1	1	-	-	-	-	-	-	-	ENTRY_EN
Initial setting value (default)								-	-	-	-	-	-	-	0

ENTRY_EN：Entry function control

ENTRY_EN	Function
0	Through mode: Input data must be aligned with the color filter arrangement (default).
1	Alignment mode: Input data must always be the R1, G1, B1,R2, G2,

R16h：Gamma 2.2

Address								Data setting							
A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	1	1	0	-	-	-	-	-	GAMMA2.2	-	-
Initial setting value (default)								-	-	-	-	-	1	-	-

GAMMA2.2 : Select auto or manual gamma setting

D2	Function
0	Manual set gamma by R17h~R1Ah and R3Ch~R41h.
1	Auto set to gamma2.2. (default)

R17h、R18h、R19h、R1Ah：Gamma Point Setting

Address								Data setting							
A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	1	1	1	-	GMA_VP16			-	GMA_VP8		
Initial setting value (default)								-	1	0	0	-	1	0	0
0	0	0	1	1	0	0	0	-	GMA_VP50			-	GMA_VP32		
Initial setting value (default)								-	1	0	1	-	1	0	0
0	0	0	1	1	0	0	1	-	GMA_VP96			-	GMA_VP72		

Initial setting value (default)								-	1	0	0	-	0	1	1
0	0	0	1	1	0	1	0	-	GMA_VP120			-	GMA_VP110		
Initial setting value (default)								-	1	0	1	-	1	0	0

GMA_VP8：Gamma reference voltage VP8;
GMA_VP16：Gamma reference voltage VP16;
GMA_VP32：Gamma reference voltage VP32;
GMA_VP50：Gamma reference voltage VP50;
GMA_VP72：Gamma reference voltage VP72;
GMA_VP96：Gamma reference voltage VP96;
GMA_VP110：Gamma reference voltage VP110;
GMA_VP120：Gamma reference voltage VP120;

Reference point	000	001	010	011	8	101	110	111
VP0	-8△V	-6△V	-4△V	-2△V	Default	+2△V	+4△V	+6△V
VP8	-8△V	-6△V	-4△V	-2△V	Default	+2△V	+4△V	+6△V
VP16	-4△V	-3△V	-2△V	-△V	Default	+△V	+2△V	+3△V
VP32	-4△V	-3△V	-2△V	-△V	Default	+△V	+2△V	+3△V
VP50	-5△V	-4△V	-3△V	-2△V	-△V	Default	+△V	+2△V
VP72	-3△V	-2△V	-△V	Default	+△V	+2△V	+3△V	+4△V
VP96	-4△V	-3△V	-2△V	-△V	Default	+△V	+2△V	+3△V
VP110	-4△V	-3△V	-2△V	-△V	Default	+△V	+2△V	+3△V
VP120	-10△V	-8△V	-6△V	-4△V	-2△V	Default	+2△V	+4△V
VP127	-6△V	-4△V	-2△V	Default	+2△V	+4△V	+6△V	+8△V
VN0	-10△V	-8△V	-6△V	-4△V	-2△V	Default	+2△V	+4△V
VN8	-8△V	-6△V	-4△V	-2△V	Default	+2△V	+4△V	+6△V
VN16	-4△V	-3△V	-2△V	-△V	Default	+△V	+2△V	+3△V
VN32	-4△V	-3△V	-2△V	-△V	Default	+△V	+2△V	+3△V
VN50	-5△V	-4△V	-3△V	-2△V	-△V	Default	+△V	+2△V
VN72	-3△V	-2△V	-△V	Default	+△V	+2△V	+3△V	+4△V
VN96	-4△V	-3△V	-2△V	-△V	Default	+△V	+2△V	+3△V
VN110	-4△V	-3△V	-2△V	-△V	Default	+△V	+2△V	+3△V
VN120	-10△V	-8△V	-6△V	-4△V	-2△V	Default	+2△V	+4△V
VN127	-4△V	-3△V	-2△V	-△V	Default	+△V	+2△V	+3△V

Note: (1)For low voltage LC △V=25mV ,For Normal voltage LC △V=40mV

R2Bh：Standby Mode

Address								Data setting							
A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	0	1	1	-	-	-	-	-	-	-	STB
Initial setting value (default)								-	-	-	-	-	-	-	0

STB：Standby (Power saving) mode

STB	Function
0	Standby Mode. (Default)
1	Normal operation.

R2Fh：

Address								Data setting							
A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	1	1	1	VGH_SEL			CF_SEL	LC_TYPE		SOPC	
Initial setting value (default)								0	1	1	0	0	0	0	1

VGH_SEL			VGH Voltage
D7	D6	D5	
0	0	0	13V
0	0	1	14V
0	1	0	15V
0	1	1	16V
1	0	0	17V
1	0	1	18V
1	1	0	18V
1	1	1	18V

SOPC：Source output driving capability selection

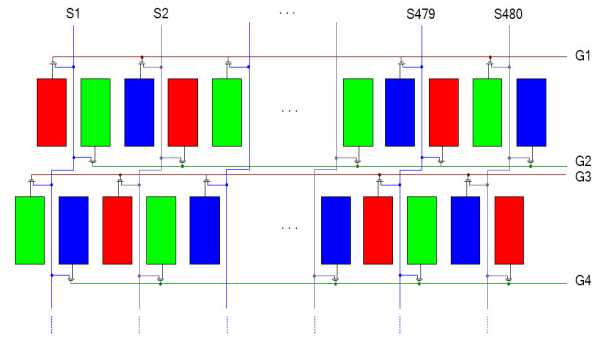
SOPC	Source driver capability
0	-25%.
1	Normal. (default)
2	+25%.
3	+50%.

LC_TYPE : LC type select

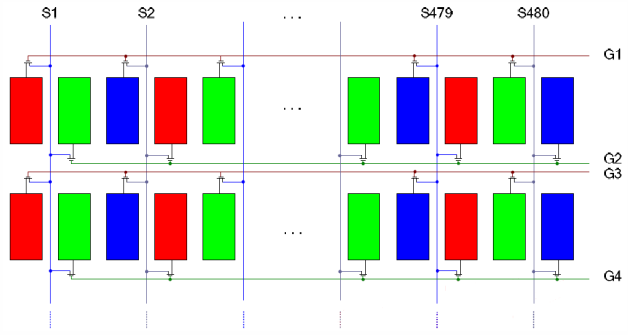
D5	D4	LC_TYPE Function
0	0	Low voltage LC(Default)
0	1	Reserved
1	0	Reserved
1	1	Normal LC

CF_SEL : Color filter selection register

CF_SEL	Function
0	Delta color filter. (Default)
1	Stripe color filter.



Delta color filter@960x240



Stripe color filter@960x240

R55h：Inversion selection

Address								Data setting							
A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	0	1	0	1	-	INV_SEL	DAT_INV	-	-	-	-	-
Initial setting value (default)								-	0	0	-	-	-	-	-

DAT_INV	Inversion
0	Normal data output. (Default)
1	Inversion data output

INV_SEL	Inversion
0	One line inversion. (Default)
1	Column inversion.

R57h：VGHL_ENB

Address								Data setting							
A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	0	1	1	1	VGHL_ENB	-	-	-	-	-	-	-
Initial setting value (default)								0	-	-	-	-	-	-	-

VGHL_ENB	Inversion
0	VGH/VGL charge pump enable (Default)
1	For external VGH/VGL application

R5Ah：VGL_SEL

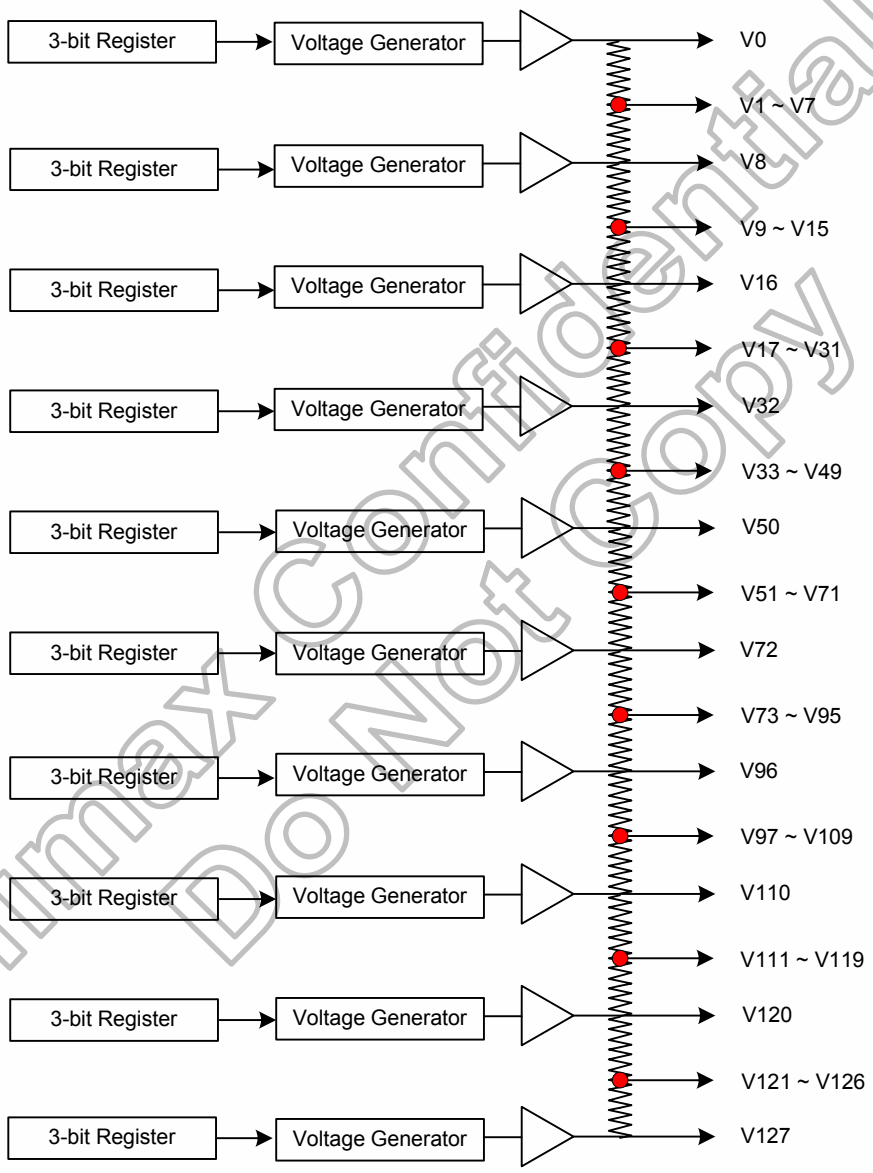
Address								Data setting							
A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
1	-	0	1	1	0	1	0	-	-	-	-	-	VGL_SEL		
Initial setting value (default)								-	-	-	-	-	0		

VGL_SEL			VGL Voltage
D2	D1	D0	
0	0	0	-8V
0	0	1	-9V
0	1	0	-10V(default)
0	1	1	-11V
1	0	0	-7V
1	0	1	-7V
1	1	0	-11V
1	1	1	-11V

7. Gamma adjustment

7.1 Internal Gamma reference voltage generator

10 gamma correction reference point; V0/V8/V16/V32/V50/V72/V96/V110/V120/V127 are generated within driver IC and adjustable through serial register setting.



7.2 Output Voltages vs. Source Input Data

TBD.

8. Timing characteristics

8.1 SPI timing

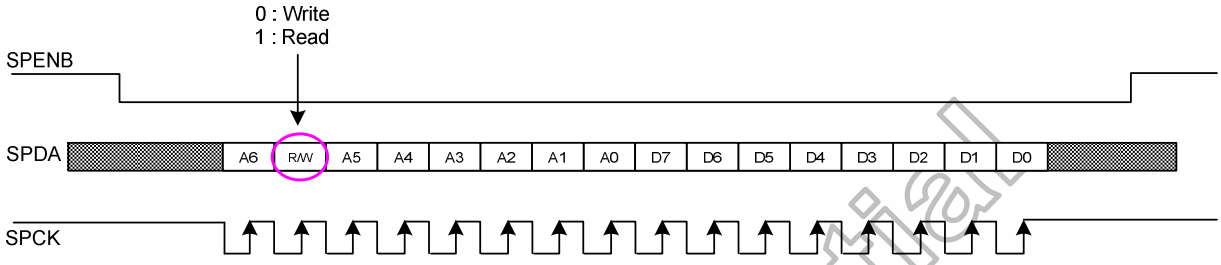


Figure 8.1 : SPI command format

- Each serial command consists of 16 bits of data that is loaded one bit a time at the rising edge of serial clock SPCK. Command loading operation starts from the falling edge of SPENB and is completed at the next rising edge of SPENB.
- The serial control block is operational after power on reset, but commands are established by the VSD signal. If command is transferred multiple times for the same register, the last command before the VSD signal is valid.
- If less than 16 bits of SPCK are input while SPENB is low, the transferred data is ignored.
- If 16 bits or more of SPCK are input while SPENB is low, the last 16 bits of transferred data before the rising edge of SPENB pulse are valid data.
- Serial block operates with the SPCK clock
- Serial data can be accepted in the power save mode.

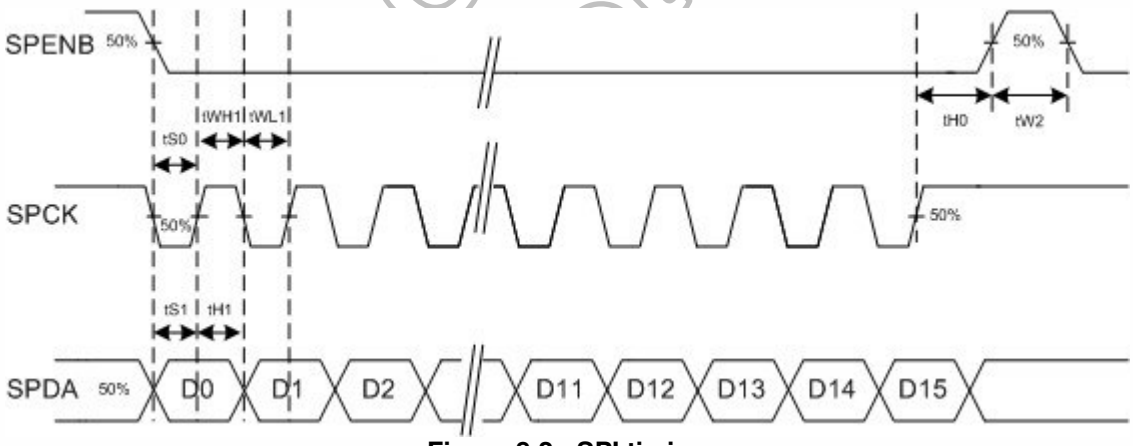


Figure 8.2 : SPI timing

PARAMETER	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
SPENB input setup time	tS0	50			ns
SPDA input setup time	tS1	50			ns
SPENB input hold time	tH0	50			ns
SPDA input hold time	tH1	50			ns
SPCK pulse high width	tWH1	50			ns
SPCK pulse low width	tWL1	50			ns
SPENB pulse high width	tW2	400			ns

8.2 Data Input format and timing

8.2.1 Serial 8-bit RGB / 8-bit Dummy RGB / YUV Mode Data format

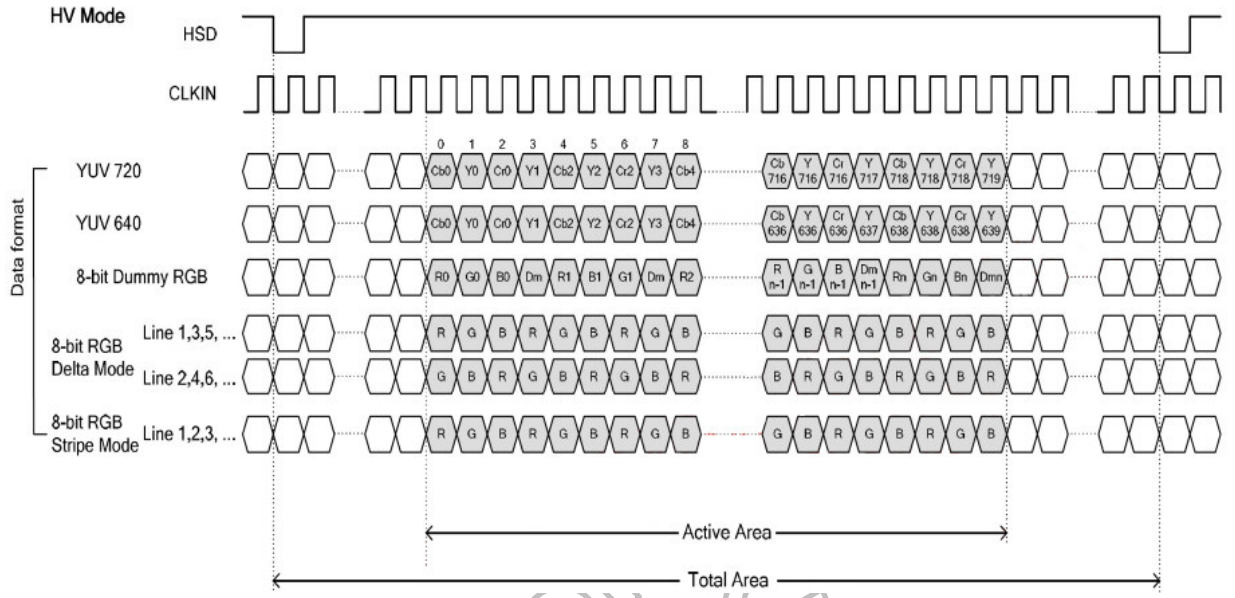


Figure 8.3 : Serial 8-bit RGB / 8-bit Dummy RGB / YUV Mode Data format HV mode

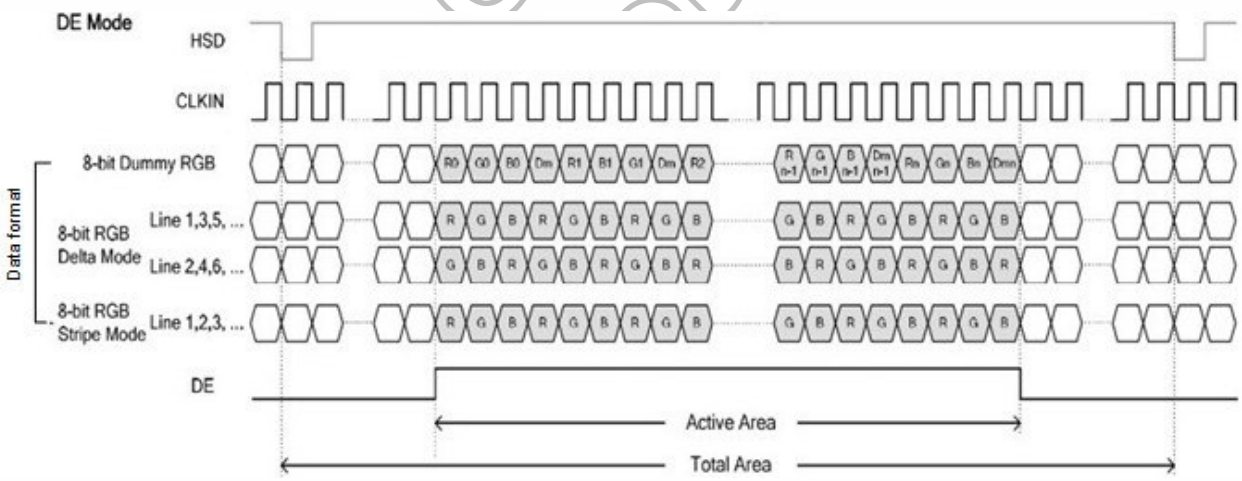


Figure 8.4 : Serial 8-bit RGB / 8-bit Dummy RGB / YUV Mode Data format DE mode

8.2.2 Parallel RGB Mode Data format

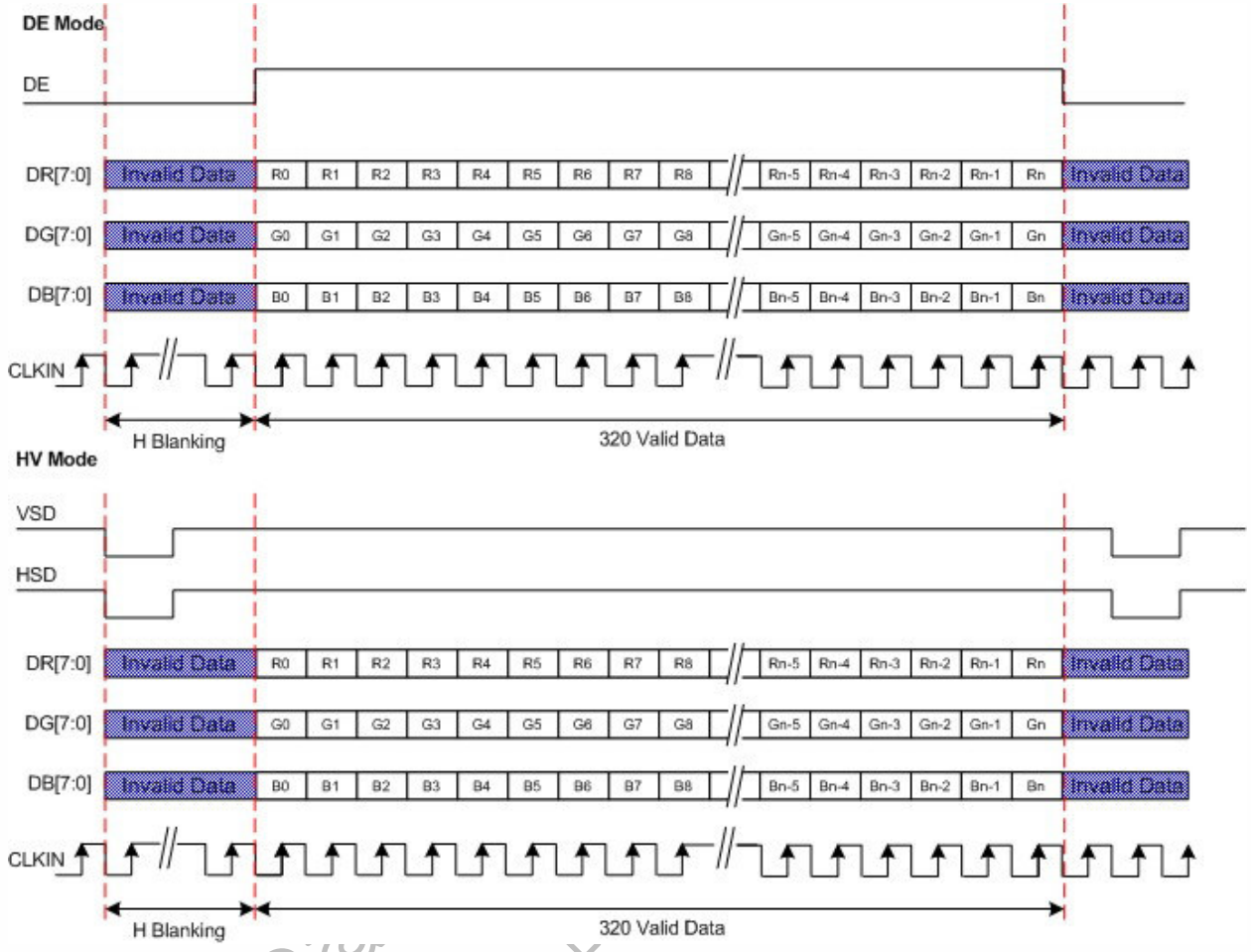


Figure 8.5 : Parallel RGB Mode Data format

8.2.3 CCIR_656 Mode Data format

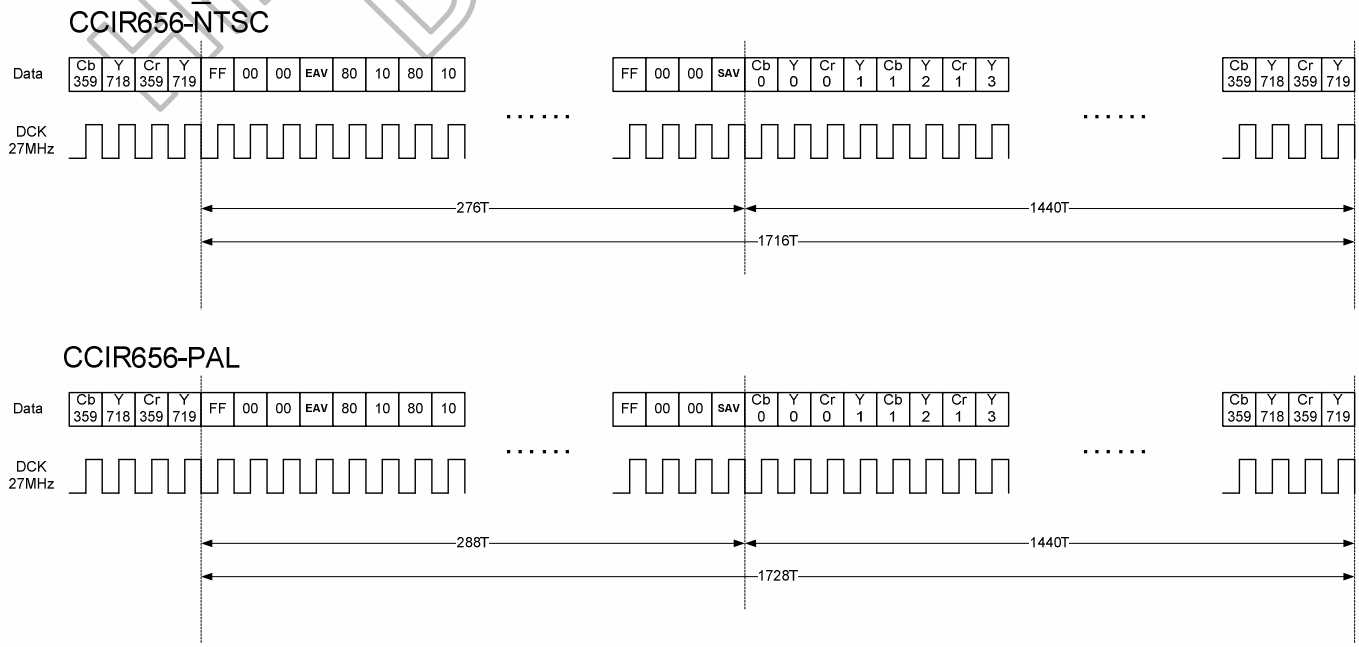


Figure 8.6 : CCIR_656 Mode Data format

XY							
D7	D6	D5	D4	D3	D2	D1	D0
1	F	V	H	P3	P2	P1	P0

8.2.4 CCIR656/YUV640/YUV720 to RGB Conversion Formula

$Rn = 1.164 \times [(Y_{2n-1} + Y_{2n}) / 2 - 16] + 1.596 \times (Cr_n-128)$
$Gn = 1.164 \times [(Y_{2n-1} + Y_{2n}) / 2 - 16] - 0.813 \times (Cr_n-128) – 0.392 \times (Cb_n-128)$
$Bn = 1.164 \times [(Y_{2n-1} + Y_{2n}) / 2 - 16] + 2.017 \times (Cb_n-128)$

Where Y : 16~235 Cr : 16~240 Cb : 16~240

9. Data Input Timing

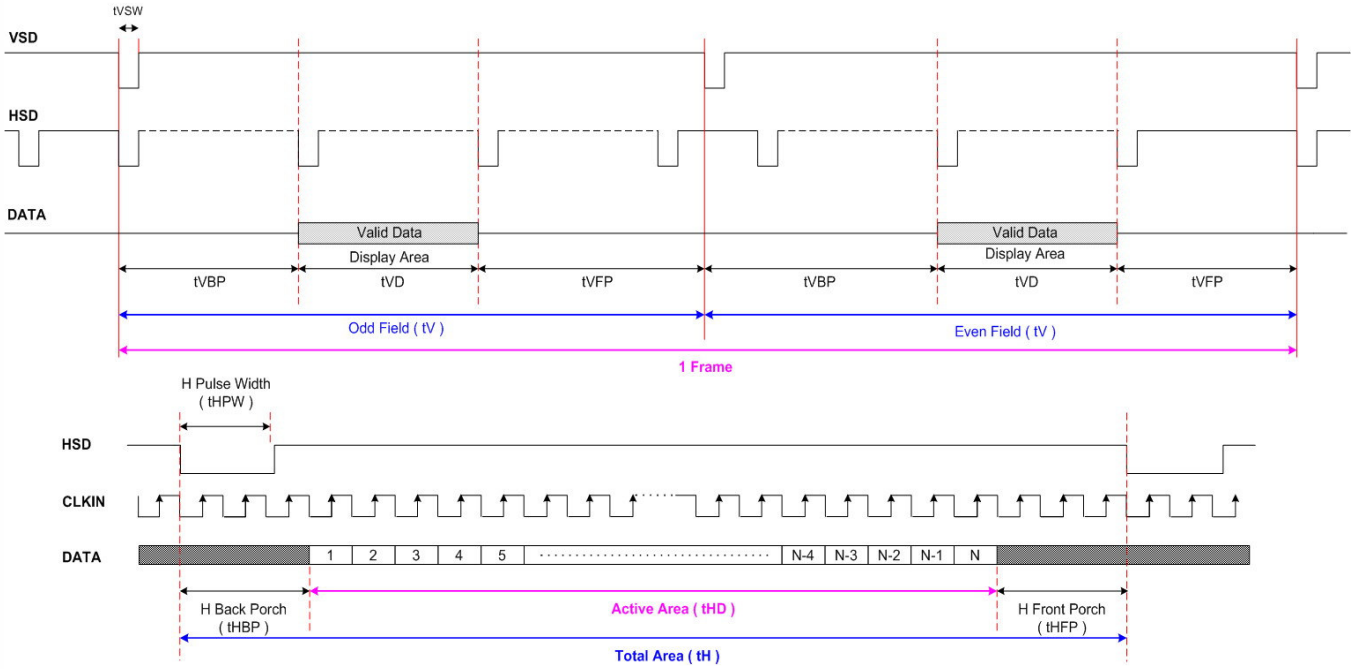


Figure 9.1 8-bit RGB/8-bit Dummy RGB/YUV /Parallel RGB Input timing chart

9.1 8-bit RGB input timing

Parameter		Symbol	Interlace			Unit
			Min.	Typ.	Max.	
CLKIN frequency		fCLKIN	13.5	27	27.19	MHz
HSD period		tH	1024	1716	1728	CLKIN
HSD display period		tHD	960			CLKIN
HSD back porch		tHBP	50	70	255	CLKIN
HSD front porch		tHFP	14	686	718	CLKIN
HSD pulse width		tHPW	1	1	tHBP-1	CLKIN
VSD period time		tV	242.5	262.5	450.5	H
Vertical display area		tVD	240			H
VSD back porch	Odd field	tVBP	3	21	31	H
	Even field		3.5	21.5	31.5	
VSD front porch	Odd field	tVFP	1.5	1.5	179.5	H
	Even field		1	1	179	
VSD pulse width		tVSW	1 CLKIN	1CLKIN	6H	
1 Frame			485	525	901	H

Table 9.1 8-bit RGB input timing

9.2 8-bit Dummy RGB input timing

9.2.1 8-bit Dummy RGB (320 mode/NTSC/24.535Mhz) input timing

Parameter		Symbol	Interlace			Unit
			Min.	Typ.	Max.	
CLKIN frequency		fCLKIN	20.45	24.535	30	MHz
HSD period		tH	1306	1560	1907	CLKIN
HSD display period		tHD		1280		CLKIN
HSD back porch		tHBP	3	241	255	CLKIN
HSD front porch		tHFP	25	39	372	CLKIN
HSD pulse width		tHPW	1	1	200	CLKIN
VSD period time		tV	242.5	262.5	450.5	H
Vertical display area		tVD		240		H
VSD back porch	Odd field	tVBP	3	21	31	H
	Even field		3.5	21.5	31.5	
VSD front porch	Odd field	tVFP	1.5	1.5	179.5	H
	Even field		1	1	179	
VSD pulse width		tVSW	1	1	200	CLKIN
1 Frame			485	525	901	H

Table 9.2 8-bit Dummy RGB (320 mode/NTSC/24.535Mhz) input timing

9.2.2 8-bit Dummy RGB (320 mode/PAL/24.375Mhz) input timing

Parameter		Symbol	Interlace			Unit
			Min.	Typ.	Max.	
CLKIN frequency		fCLKIN	20.45	24.375	30	MHz
HSD period		tH	1306	1560	1920	CLKIN
HSD display period		tHD		1280		CLKIN
HSD back porch		tHBP	3	241	255	CLKIN
HSD front porch		tHFP	25	39	385	CLKIN
HSD pulse width		tHPW	1	1	200	CLKIN
VSD period time		tV	292.5	312.5	450.5	H
Vertical display area		tVD		288		H
VSD back porch	Odd field	tVBP	3	23	34	H
	Even field		3.5	23.5	34.5	
VSD front porch	Odd field	tVFP	1.5	1.5	128.5	H
	Even field		1	1	128	
VSD pulse width		tVSW	1	1	200	CLKIN
1 Frame			585	625	901	H

Table 9.3 8-bit Dummy RGB (320 mode/PAL/24.375Mhz) input timing

9.2.3 8-bit Dummy RGB (360 mode/NTSC/27Mhz) input timing

Parameter		Symbol	Interlace			Unit
			Min.	Typ.	Max.	
CLKIN frequency		fCLKIN	23	27	30	MHz
HSD period		tH	1466	1716	1907	CLKIN
HSD display period		tHD		1440		CLKIN
HSD back porch		tHBP	3	241	255	CLKIN
HSD front porch		tHFP	25	35	212	CLKIN
HSD pulse width		tHPW	1	1	200	CLKIN
VSD period time		tV	242.5	262.5	450.5	H
Vertical display area		tVD		240		H
VSD back porch	Odd field	tVBP	3	21	31	H
	Even field		3.5	21.5	31.5	
VSD front porch	Odd field	tVFP	1.5	1.5	179.5	H
	Even field		1	1	179	
VSD pulse width		tVSW	1	1	200	CLKIN
1 Frame			485	525	901	H

Table 9.4 8-bit Dummy RGB (360 mode/NTSC/27Mhz) input timing

9.2.4 8-bit Dummy RGB (360 mode/PAL/27Mhz) input timing

Parameter		Symbol	Interlace			Unit
			Min.	Typ.	Max.	
CLKIN frequency		fCLKIN	23	27	30	MHz
HSD period		tH	1466	1728	1920	CLKIN
HSD display period		tHD		1440		CLKIN
HSD back porch		tHBP	3	241	255	CLKIN
HSD front porch		tHFP	25	47	225	CLKIN
HSD pulse width		tHPW	1	1	200	CLKIN
VSD period time		tV	292.5	312.5	450.5	H
Vertical display area		tVD		288		H
VSD back porch	Odd field	tVBP	3	23	34	H
	Even field		3.5	23.5	34.5	
VSD front porch	Odd field	tVFP	1.5	1.5	128.5	H
	Even field		1	1	128	
VSD pulse width		tVSW	1	1	200	CLKIN
1 Frame			585	625	901	H

Table 9.5 8-bit Dummy RGB (360 mode/PAL/27Mhz) input timing

9.3 YUV720 and YUV640 input timing

9.3.1 YUV720 mode/NTSC input timing

Parameter		Symbol	Interlace			Unit
			Min.	Typ.	Max.	
CLKIN frequency		fCLKIN	-	27	-	MHz
HSD period		tH	-	1716	-	CLKIN
HSD display period		tHD		1440		CLKIN
HSD back porch		tHBP	-	240	-	CLKIN
HSD front porch		tHFP	-	36	-	CLKIN
HSD pulse width		tHPW	-	1	-	CLKIN
VSD period time		tV	-	262.5	-	H
Vertical display area		tVD		240		H
VSD back porch	Odd field	tVBP	-	21	-	H
	Even field		-	21.5	-	
VSD front porch	Odd field	tVFP	-	1.5	-	
	Even field		-	1	-	
VSD pulse width		tVSW	-	1	1	
1 Frame			-	525	-	

Table 9.6 YUV720 mode/NTSC input timing

9.3.2 YUV720 mode/PAL input timing

Parameter		Symbol	Interlace			Unit
			Min.	Typ.	Max.	
CLKIN frequency		fCLKIN	-	27	-	MHz
HSD period		tH	-	1728	-	CLKIN
HSD display period		tHD		1440		CLKIN
HSD back porch		tHBP	-	240	-	CLKIN
HSD front porch		tHFP	-	48	-	CLKIN
HSD pulse width		tHPW	-	1	-	CLKIN
VSD period time		tV	-	312.5	-	H
Vertical display area		tVD		288		H
VSD back porch	Odd field	tVBP	-	24	-	H
	Even field		-	24.5	-	
VSD front porch	Odd field	tVFP	-	0.5	-	H
	Even field		-	0	-	
VSD pulse width		tVSW	-	1	-	CLKIN
1 Frame			-	625	-	H

Table 9.7 YUV720 mode/PAL input timing

9.3.3 YUV640 mode/NTSC input timing

Parameter		Symbol	Interlace			Unit
			Min.	Typ.	Max.	
CLKIN frequency		fCLKIN	-	24.535	-	MHz
HSD period		tH	-	1560	-	CLKIN
HSD display period		tHD		1280		CLKIN
HSD back porch		tHBP	-	240	-	CLKIN
HSD front porch		tHFP	-	40	-	CLKIN
HSD pulse width		tHPW	-	1	-	CLKIN
VSD period time		tV	-	262.5	-	H
Vertical display area		tVD		240		H
VSD back porch	Odd field	tVBP	-	21	-	H
	Even field		-	21.5	-	
VSD front porch	Odd field	tVFP	-	1.5	-	H
	Even field		-	1	-	
VSD pulse width		tVSW	-	1	-	CLKIN
1 Frame			-	525	-	H

Table 9.8 YUV640 mode/NTSC input timing

9.3.4 YUV640 mode/PAL input timing

Parameter		Symbol	Interlace			Unit
			Min.	Typ.	Max.	
CLKIN frequency		fCLKIN	-	24.375	-	MHz
HSD period		tH	-	1560	-	CLKIN
HSD display period		tHD		1280		CLKIN
HSD back porch		tHBP	-	240	-	CLKIN
HSD front porch		tHFP	-	40	-	CLKIN
HSD pulse width		tHPW	-	1	-	CLKIN
VSD period time		tV	-	312.5	-	H
Vertical display area		tVD		288		H
VSD back porch	Odd field	tVBP	-	24	-	H
	Even field		-	24.5	-	
VSD front porch	Odd field	tVFP	-	0.5	-	H
	Even field		-	0	-	
VSD pulse width		tVSW	-	1	-	CLKIN
1 Frame			-	625	-	H

Table 9.9 YUV640 mode/PAL input timing

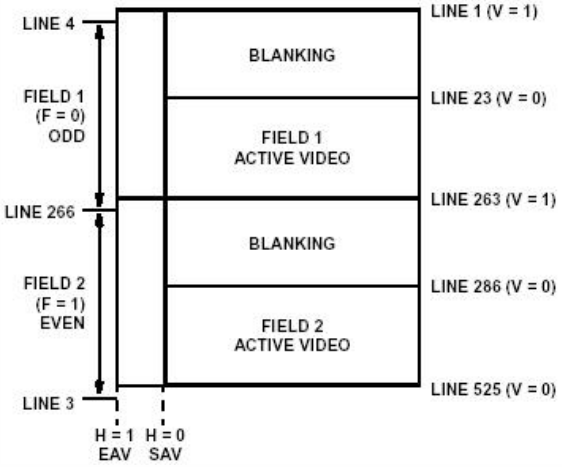
9.4 Parallel RGB input timing

Parameter		Symbol	Interlace			Unit
			Min.	Typ.	Max.	
CLKIN frequency		fCLKIN	-	6.14	-	MHz
HSD period		tH	-	390	-	CLKIN
HSD display period		tHD		320		CLKIN
HSD back porch		tHBP	40	61	-	CLKIN
HSD front porch		tHFP	-	9	-	CLKIN
HSD pulse width		tHPW	-	1	-	CLKIN
VSD period time		tV	-	262.5	-	H
Vertical display area		tVD		240		H
VSD back porch	Odd field	tVBP	-	21	-	H
	Even field		-	21.5	-	
VSD front porch	Odd field	tVFP	-	1.5	-	H
	Even field		-	1	-	
VSD pulse width		tVSW	-	1	-	CLKIN
1 Frame			-	525	-	H

Table 9.10 Parallel RGB input timing input timing

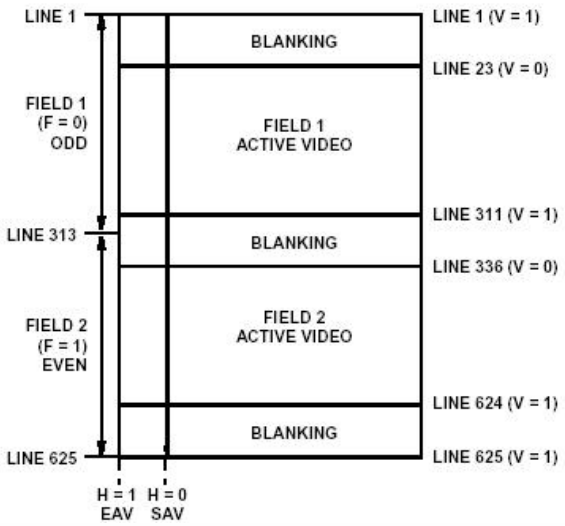
9.5 CCIR656 vertical input timing

9.5.1 NTSC mode



LINE NUMBER	F	V	H (EAV)	H (SAV)
1-3	1	1	1	0
4-22	0	1	1	0
23-262	0	0	1	0
263-265	0	1	1	0
266-285	1	1	1	0
286-525	1	0	1	0

9.5.2 PAL mode



LINE NUMBER	F	V	H (EAV)	H (SAV)
1-22	0	1	1	0
23-310	0	0	1	0
311-312	0	1	1	0
313-335	1	1	1	0
336-623	1	0	1	0
624-625	1	1	1	0

	F	H	V
1	EVEN Field	EAV	BLANKING
0	Odd Field	SAV	ACTIVE VIDEO

10. Power Sequence

10.1 Power On Sequence

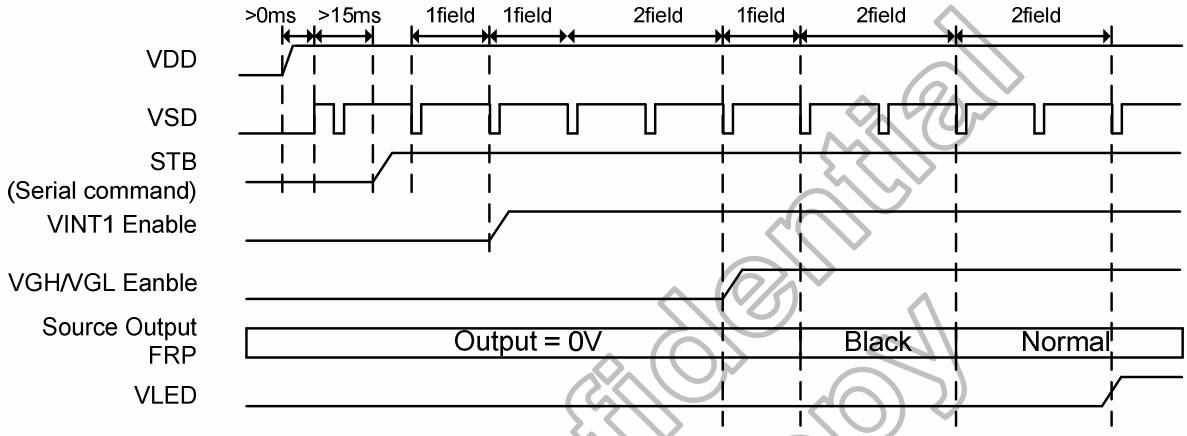


Figure 10.1 Power On Sequence

10.2 Power off Sequence

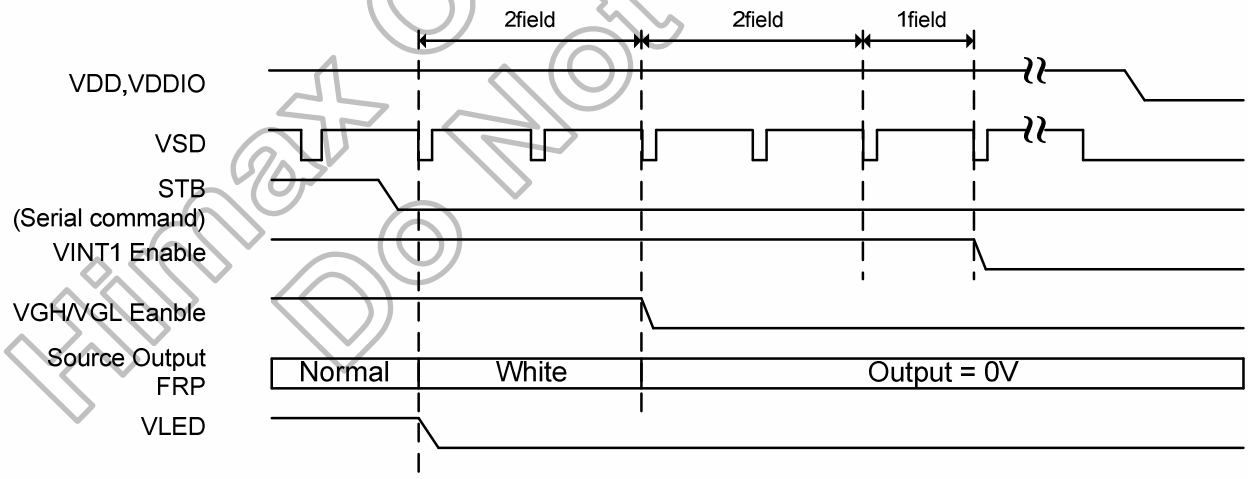


Figure 10.2 Power On Sequence

11. DC Electrical Characteristics

11.1 Absolute Maximum Rating

(BGND=AGND=0V)

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Power supply voltage 1	VDD	-0.3	-	+5.0	V
Power supply voltage 2	VDDIO	-0.3	-	+5.0	V
Logic supply Voltage	DVDD	-0.3	-	+3.0	V
Input voltage	Vin	-0.3	-	VDDIO+0.3	V
Operation temperature	T_{OPR}	-20	-	+85	℃
Storage temperature	T_{STG}	-55	-	+125	℃

Note: (1)All of the voltages listed above are with respective to BGND=AGND=0V.
(2)Device is subject to be damaged permanently if stresses beyond those absolute maximum ratings listed above.

11.2 Operation Rating

(VDD=3.0~3.6V,VDDIO=AVDD=VDD,BGND=AGND=0V, TA=25℃)

Parameter	Symbol	Spec.			Unit	Condition
		Min.	Typ.	Max.		
Power supply voltage1	VDD	2.7	3.3	3.6	V	-20℃~85℃
Power supply voltage2	VDDIO	1.65	-	VDD	V	-
Low level input voltage	V_{IL}	0	-	0.3VDDIO	V	Digital input pins,VDDIO=2.7V~3.6V
		0	-	0.2VDDIO	V	Digital input pins,VDDIO=1.8~2.7V
High level input voltage	V_{IH}	0.7VDDIO	-	VDDIO	V	Digital input pins,VDDIO=2.7V~3.6V
		0.8VDDIO	-	VDDIO	V	Digital input pins,VDDIO=1.8~2.7V
Output low voltage	V_{OL}	0	-	0.4	V	VDDIO=3.3V,@I_{OL}=400μA
Output high voltage	V_{OH}	VDDIO-0.4	-	VDDIO	V	VDDIO=3.3V,@I_{OH}=-400μA
Input leakage current	I_{IN}	-	-	±1	μA	Digital input pins.
Pull-high/low Impedance	R_{IN}	150k	200k	250k	ohm	VDDIO=3.3V
Gamma supply voltage	GMA_H	-	2.8	-	V	For low voltage LC
		-	4.7	-	V	For normal voltage LC
GMA_H voltage tolerance	GMA_HT	-70	-	+70	mV	Low voltage LC
		-140	-	+140	mV	Normal voltage LC
Voltage deviation of outputs	V_{VD}	-	±20	±35	mV	Vo=0.1V~0.5V GMA_H-0.5V~GMA_H-0.1V
			±15	±20	mV	Vo=0.5V~GAM_H-0.5V
Dynamic Range of Output	V_{DR}	0.1	-	GMA_H-0.1	V	S1~S480
Driving current of Source outputs	IOHS	-	-25	-	uA	Vos=GMA_H-0.2V,Vys=GMA_H-1.1V
Sinking current of Source output	IOLS	-	25	-	uA	Vos=0.2V, Vys=1.1V
Driving current of Gate outputs	IOHG	-	-200	-	uA	VGH=15V ,VGL=-10V Vog=15V, Vyg=14.5V
Sinking current of Gate outputs	IOLG	-	200	-	uA	VGH=15V ,VGL=-10V Vog=-10V, Vyg=-9.5V
Base drive current for PWM	IDRV	-	0.25	-	mA	VDD=3.3V, DRV=0.7V
DRV output voltage for PWM	VDRV	0	-	VDD	V	
Feed back voltage for PWM	VFB	0.25	0.6	0.8	V	DC/DC operating
VCAC DC Tolerance	VCAC	-100	-	+100	mV	VCAC value by VCOM DC setting
FRP Low level output current	IOLF	-	5	-	mA	For VCAC=5V, Vofrp=0V,Vyfrp=0.9V
FRP High level output current	IOHF	-	-5	-	mA	For VCAC=5V, Vofrp=5V,Vyfrp=4.1V
VCOMDC output tolerance	VDCT	-35	-	+35	mV	No loads
VGH output tolerance	VGHT	-0.6	-	+1	V	CLKIN=27MHZMVSD=60HZ, HSD=15.75KHZ VGH_SEL=01B,10B and 11B
		-0.7	-	+1.1	V	CLKIN=27MHZMVSD=60HZ, HSD=15.75KHZ VGH_SEL=00B
VGL output tolerance	VGLT	-0.6	-	+0.6	V	CLKIN=27MHZMVSD=60HZ, HSD=15.75KHZ VGL_SEL=01B,10B and 11B
		-0.6	-	+1.1	V	CLKIN=27MHZMVSD=60HZ, HSD=15.75KHZ VGL_SEL=00B

(VDD=3.0~3.6V,VDDIO=AVDD=VDD,BGND=AGND=0V, TA=25℃)

Parameter	Symbol	Spec.			Unit	Condition
		Min.	Typ.	Max.		
Ripple of VGL	Vglrp	-150	-	50	mV	No loads,Power setting capacitors are default setting
Stand-by Current	Ist	-	80	100	uA	STBYB=0, all functions are stopped, and no CLK input
Operating Current	Iop	-	6.5	8	mA	No loads, line inversion ,CLKIN=27MHZ Low voltage LC
		-	13	-		No loads, line inversion ,CLKIN=27MHZ Normal voltage LC

Note : (1) Vys,Vyg is the voltage applies to source and gate output pins.
(2) Vos,Vog is the output voltage of source and gate output pins.
(3) Vyfrp is the voltage applies to FRP pin.
(4) Vofrp is the output voltage of FRP pin.
(5) Vycdc is the voltage applies to VCOMDC pin.
(6) When VDDIO is used on 1.65V (over SPEC. use)，for operation stability，please confirm the followings：
SPI： VIH = 0.9 x VDDIO、SPI VIL = 0.1x VDDIO
others： VIH = 0.9 x VDDIO、VIL=0.1 x VDDIO

12. AC Electrical Characteristics

12.1 Timing Characteristics

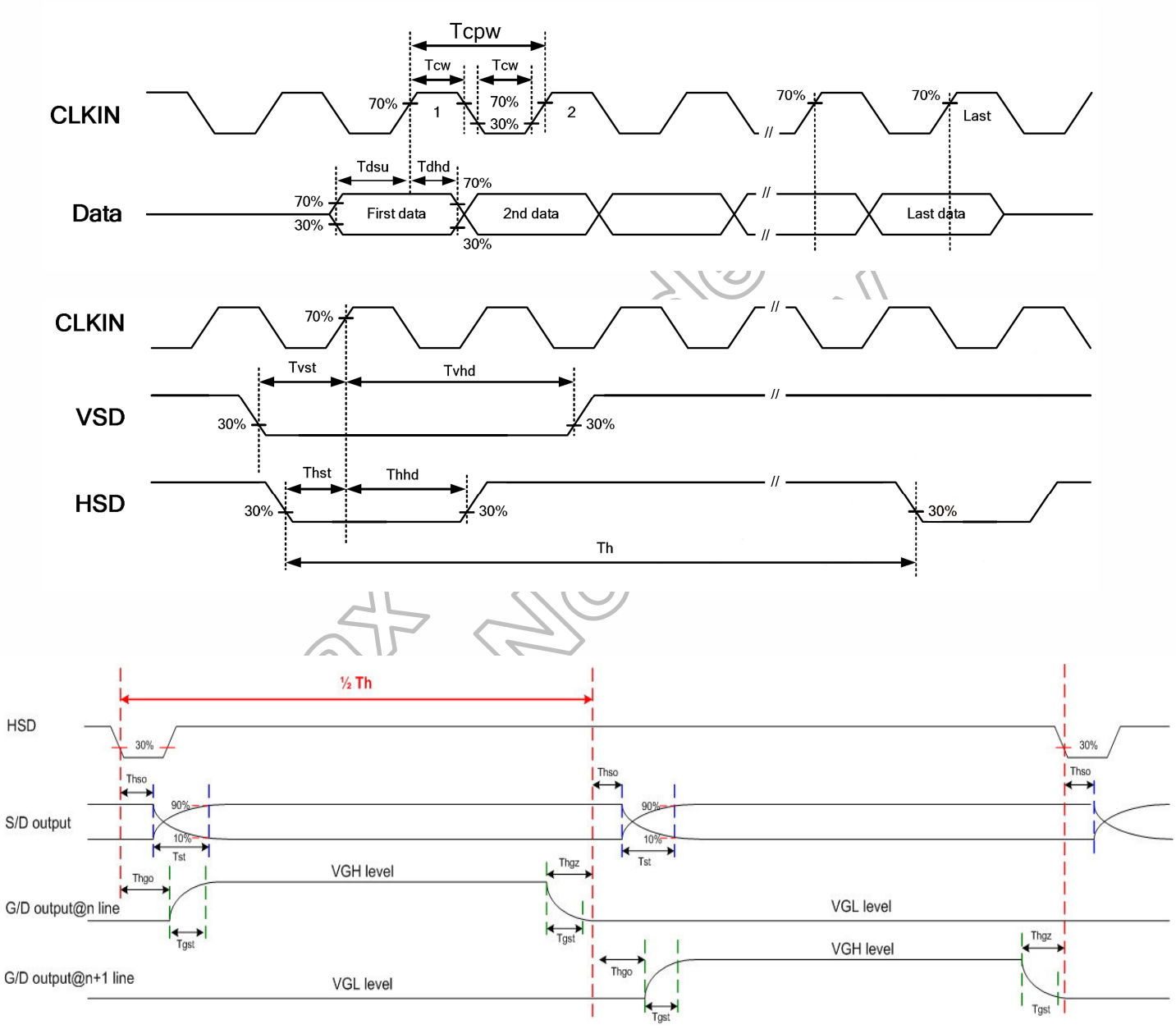


Figure 12.1 Timing Characteristics

(VDD=3.0~3.6V,VDDIO=AVDD=VDD,BGND=AGND=0V, TA=25℃)

PARAMETER	Symbol	Spec.			Unit	Conditions
		Min.	Typ.	Max.		
HSD period time	Th	60	63.56	67	us	
HSD setup time	Thst	12	-	-	ns	
HSD hold time	Thhd	12	-	-	ns	
VSD setup time	Tvst	12	-	-	ns	
VSD hold time	Tvhd	12	-	-	ns	
Data setup time	Tdsu	12	-	-	ns	
Data hold time	Tdhd	12	-	-	ns	
Source output settling time	TST	-	-	8	us	R=5Kohm , C=30pF
Gate output settling time	Tgst	-	0.5	1	us	R=3Kohm , C=25pF
VCOM setting time	TST,vcom	-	-	9	us	R=200ohm , C=5nF

12.2 Output Timing Table

12.2.1 8-bit RGB

AC Electrical Characteristics (VDD =3.0~3.6V, VDDIO=AVDD=VDD, AGND=BGND=0V, TA=25℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
CLKIN frequency	Fclk	-	19	30	MHz	
CLKIN cycle time	Tcph	-	52	-	ns	
CLK pulse duty	Tcw	40	50	60	%	Tcph
Time that the HSD to Source output	Thso	-	3.5	-	CLKIN	
Time that the HSD to Gate output	Thgo	-	64.5	-	CLKIN	
Time that the HSD to Gate output off	Thgz	-	22.5	-	CLKIN	

12.2.2 8-bit Dummy RGB

AC Electrical Characteristics (VDD =3.0~3.6V, VDDIO=AVDD=VDD, AGND=BGND=0V, TA=25℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
CLKIN frequency	Fclk	-	24.5/27	30	MHz	
CLKIN cycle time	Tcph	-	40/37	-	ns	
CLK pulse duty	Tcw	40	50	60	%	Tcph
Time that the HSD to Source output	Thso	-	3.5	-	CLKIN	
Time that the HSD to Gate output	Thgo	-	64.5	-	CLKIN	
Time that the HSD to Gate output off	Thgz	-	22.5	-	CLKIN	

12.2.3 YUV640/YUV720

AC Electrical Characteristics (VDD =3.0~3.6V, VDDIO=AVDD=VDD, AGND=BGND=0V, TA=25℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
CLKIN frequency	Fclk	-	24.5/27	30	MHz	
CLKIN cycle time	Tcph	-	40/37	-	ns	
CLK pulse duty	Tcw	40	50	60	%	Tcph
Time that the HSD to Source output	Thso	-	3.5	-	CLKIN	
Time that the HSD to Gate output	Thgo	-	64.5	-	CLKIN	
Time that the HSD to Gate output off	Thgz	-	22.5	-	CLKIN	

12.2.4 CCIR_656

AC Electrical Characteristics (VDD =2.7~3.6V, VDDIO=AVDD=VDD, AGND=BGND=0V, TA=25℃)

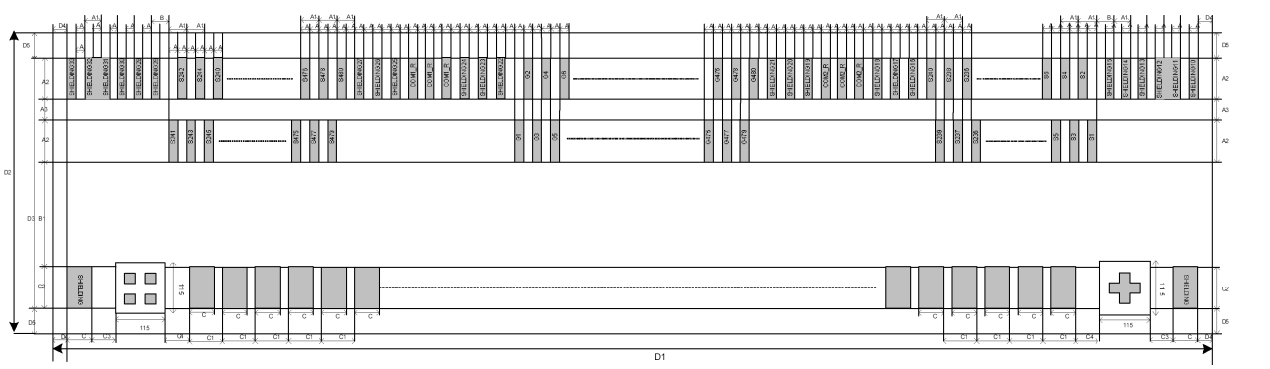
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
CLKIN frequency	Fclk	-	27	30	MHz	
CLKIN cycle time	Tcph	33	37	-	ns	
CLK pulse duty	Tcw	40	50	60	%	Tcph
Time that the HSD to Source output	Thso	-	3.5	-	CLKIN	
Time that the HSD to Gate output	Thgo	-	64.5	-	CLKIN	
Time that the HSD to Gate output off	Thgz	-	22.5	-	CLKIN	

12.2.5 Parallel RGB

AC Electrical Characteristics (VDD =2.7~3.6V, VDDIO=AVDD=VDD, AGND=BGND=0V, TA=25℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
CLKIN frequency	Fclk	-	6.2	7.5	MHz	
CLKIN cycle time	Tcph	-	161	-	ns	
CLK pulse duty	Tcw	40	50	60	%	Tcph
Time that the HSD to Source output	Thso	-	3.5	-	CLKIN	
Time that the HSD to Gate output	Thgo	-	16.5	-	CLKIN	
Time that the HSD to Gate output off	Thgz	-	4.5	-	CLKIN	

13. PAD Information

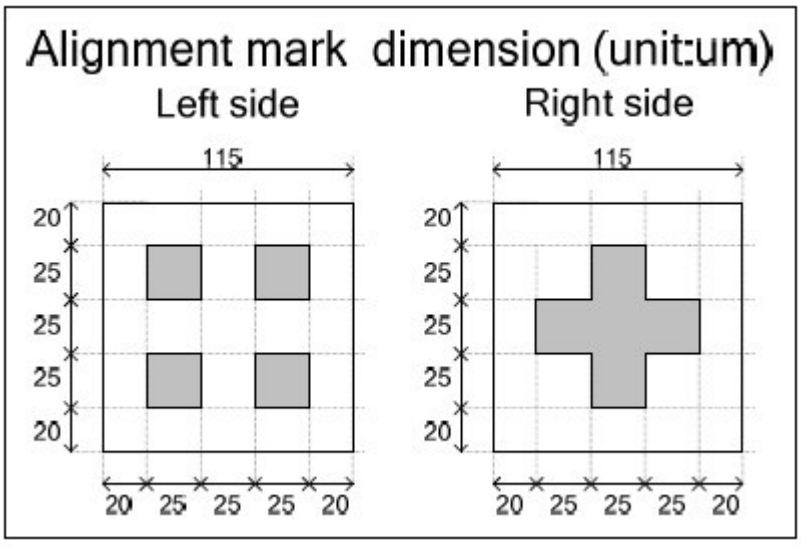


Symbol	Dimension(um)
A	14
A1	28
A2	100
A3	20
B	50
B1	250

Symbol	Dimension(um)
C	55
C1	75
C2	100
C3	39.25
C4	39.25
D1	14470
D2	670
D3	570
D4	59
D5	50

Symbol	Dimension(um)	Symbol	Dimension(um)
A	14	C	55
A1	28	C1	75
A2	115	C2	80
A3	30		

Pad outline dimension table



14. Pad Coordinate

NUM	NAME	X	Y	NUM	NAME	X	Y	NUM	NAME	X	Y
1	SHIELDING1	-7148.5	-235	61	VDDIO	-2475	-235	121	CP4P	2025	-235
2	COM1_L	-6900	-235	62	DVDD	-2400	-235	122	CP4M	2100	-235
3	COM1_L	-6825	-235	63	DVDD	-2325	-235	123	CP4M	2175	-235
4	COM1_L	-6750	-235	64	DVDD	-2250	-235	124	CP4M	2250	-235
5	SHIELDING2	-6675	-235	65	CP1P	-2175	-235	125	CP4M	2325	-235
6	VPP_MTP	-6600	-235	66	CP1P	-2100	-235	126	CP4M	2400	-235
7	VPP_MTP	-6525	-235	67	CP1P	-2025	-235	127	VGH	2475	-235
8	VPP_MTP	-6450	-235	68	CP1P	-1950	-235	128	VGH	2550	-235
9	VPP_MTP	-6375	-235	69	CP1M	-1875	-235	129	VGH	2625	-235
10	VPP_MTP	-6300	-235	70	CP1M	-1800	-235	130	VGH	2700	-235
11	STBYB	-6225	-235	71	CP1M	-1725	-235	131	VGL	2775	-235
12	RSTB	-6150	-235	72	CP1M	-1650	-235	132	VGL	2850	-235
13	P_TYPE	-6075	-235	73	CP1M	-1575	-235	133	VGL	2925	-235
14	PSEL	-6000	-235	74	CP5P	-1500	-235	134	VGL	3000	-235
15	SPENB	-5925	-235	75	CP5P	-1425	-235	135	AGND	3075	-235
16	SPDA	-5850	-235	76	CP5P	-1350	-235	136	AGND	3150	-235
17	SPCK	-5775	-235	77	CP5P	-1275	-235	137	AGND	3225	-235
18	DEN	-5700	-235	78	CP5M	-1200	-235	138	AGND	3300	-235
19	HSD	-5625	-235	79	CP5M	-1125	-235	139	SHIELDING6	3375	-235
20	VSD	-5550	-235	80	CP5M	-1050	-235	140	FRP	3450	-235
21	CLKIN	-5475	-235	81	CP5M	-975	-235	141	FRP	3525	-235
22	DB7	-5400	-235	82	CP5M	-900	-235	142	FRP	3600	-235
23	DB6	-5325	-235	83	CP2P	-825	-235	143	VCOMDC	3675	-235
24	DB5	-5250	-235	84	CP2P	-750	-235	144	VCOMDC	3750	-235
25	DB4	-5175	-235	85	CP2P	-675	-235	145	VCOMDC	3825	-235
26	DB3	-5100	-235	86	CP2P	-600	-235	146	VCOMDC	3900	-235
27	DB2	-5025	-235	87	CP2M	-525	-235	147	VCOMDC	3975	-235
28	DB1	-4950	-235	88	CP2M	-450	-235	148	VCAC	4050	-235
29	DB0	-4875	-235	89	CP2M	-375	-235	149	VCAC	4125	-235
30	DG7	-4800	-235	90	CP2M	-300	-235	150	VCAC	4200	-235
31	DG6	-4725	-235	91	CP2M	-225	-235	151	VCAC	4275	-235
32	DG5	-4650	-235	92	VINT1	-150	-235	152	VCAC	4350	-235
33	DG4	-4575	-235	93	VINT1	-75	-235	153	SHIELDING7	4425	-235
34	DG3	-4500	-235	94	VINT1	0	-235	154	DRV	4500	-235
35	DG2	-4425	-235	95	VINT1	75	-235	155	DRV	4575	-235
36	DG1	-4350	-235	96	VINT1	150	-235	156	DRV	4650	-235
37	DG0	-4275	-235	97	CP3P	225	-235	157	FB_N	4725	-235
38	DR7	-4200	-235	98	CP3P	300	-235	158	FB_N	4800	-235
39	DR6	-4125	-235	99	CP3P	375	-235	159	FB_N	4875	-235
40	DR5	-4050	-235	100	CP3P	450	-235	160	FB_N	4950	-235
41	DR4	-3975	-235	101	CP3P	525	-235	161	FB_P	5025	-235
42	DR3	-3900	-235	102	CP3M	600	-235	162	FB_P	5100	-235
43	DR2	-3825	-235	103	CP3M	675	-235	163	FB_P	5175	-235
44	DR1	-3750	-235	104	CP3M	750	-235	164	FB_P	5250	-235
45	DR0	-3675	-235	105	CP3M	825	-235	165	FB	5325	-235
46	SHIELDING3	-3600	-235	106	CP3M	900	-235	166	FB	5400	-235
47	SHIELDING4	-3525	-235	107	VINT2	975	-235	167	TEST3	5475	-235
48	SHIELDING5	-3450	-235	108	VINT2	1050	-235	168	TEST2	5550	-235
49	GND	-3375	-235	109	VINT2	1125	-235	169	TEST1	5625	-235
50	GND	-3300	-235	110	VINT2	1200	-235	170	TEST0	5700	-235
51	GND	-3225	-235	111	VINT2	1275	-235	171	T_O3	5775	-235
52	GND	-3150	-235	112	VINT3	1350	-235	172	T_O2	5850	-235
53	VDD	-3075	-235	113	VINT3	1425	-235	173	T_O1	5925	-235
54	VDD	-3000	-235	114	VINT3	1500	-235	174	T_O0	6000	-235
55	VDD	-2925	-235	115	VINT3	1575	-235	175	T_IO7	6075	-235
56	AVDD	-2850	-235	116	VINT3	1650	-235	176	T_IO6	6150	-235
57	AVDD	-2775	-235	117	CP4P	1725	-235	177	T_IO5	6225	-235
58	AVDD	-2700	-235	118	CP4P	1800	-235	178	T_IO4	6300	-235
59	VDDIO	-2625	-235	119	CP4P	1875	-235	179	T_IO3	6375	-235
60	VDDIO	-2550	-235	120	CP4P	1950	-235	180	T_IO2	6450	-235

NUM	NAME	X	Y	NUM	NAME	X	Y	NUM	NAME	X	Y
181	T_IO1	6525	-235	241	S_48	6321	235	301	S_108	5481	235
182	T_IO0	6600	-235	242	S_49	6307	115	302	S_109	5467	115
183	SHIELDING8	6675	-235	243	S_50	6293	235	303	S_110	5453	235
184	COM2_L	6750	-235	244	S_51	6279	115	304	S_111	5439	115
185	COM2_L	6825	-235	245	S_52	6265	235	305	S_112	5425	235
186	COM2_L	6900	-235	246	S_53	6251	115	306	S_113	5411	115
187	SHIELDING9	7148.5	-235	247	S_54	6237	235	307	S_114	5397	235
188	SHIELDING10	7169	235	248	S_55	6223	115	308	S_115	5383	115
189	SHIELDING11	7141	235	249	S_56	6209	235	309	S_116	5369	235
190	SHIELDING12	7113	235	250	S_57	6195	115	310	S_117	5355	115
191	SHIELDING13	7085	235	251	S_58	6181	235	311	S_118	5341	235
192	SHIELDING14	7057	235	252	S_59	6167	115	312	S_119	5327	115
193	SHIELDING15	7029	235	253	S_60	6153	235	313	S_120	5313	235
194	S_1	6979	115	254	S_61	6139	115	314	S_121	5299	115
195	S_2	6965	235	255	S_62	6125	235	315	S_122	5285	235
196	S_3	6951	115	256	S_63	6111	115	316	S_123	5271	115
197	S_4	6937	235	257	S_64	6097	235	317	S_124	5257	235
198	S_5	6923	115	258	S_65	6083	115	318	S_125	5243	115
199	S_6	6909	235	259	S_66	6069	235	319	S_126	5229	235
200	S_7	6895	115	260	S_67	6055	115	320	S_127	5215	115
201	S_8	6881	235	261	S_68	6041	235	321	S_128	5201	235
202	S_9	6867	115	262	S_69	6027	115	322	S_129	5187	115
203	S_10	6853	235	263	S_70	6013	235	323	S_130	5173	235
204	S_11	6839	115	264	S_71	5999	115	324	S_131	5159	115
205	S_12	6825	235	265	S_72	5985	235	325	S_132	5145	235
206	S_13	6811	115	266	S_73	5971	115	326	S_133	5131	115
207	S_14	6797	235	267	S_74	5957	235	327	S_134	5117	235
208	S_15	6783	115	268	S_75	5943	115	328	S_135	5103	115
209	S_16	6769	235	269	S_76	5929	235	329	S_136	5089	235
210	S_17	6755	115	270	S_77	5915	115	330	S_137	5075	115
211	S_18	6741	235	271	S_78	5901	235	331	S_138	5061	235
212	S_19	6727	115	272	S_79	5887	115	332	S_139	5047	115
213	S_20	6713	235	273	S_80	5873	235	333	S_140	5033	235
214	S_21	6699	115	274	S_81	5859	115	334	S_141	5019	115
215	S_22	6685	235	275	S_82	5845	235	335	S_142	5005	235
216	S_23	6671	115	276	S_83	5831	115	336	S_143	4991	115
217	S_24	6657	235	277	S_84	5817	235	337	S_144	4977	235
218	S_25	6643	115	278	S_85	5803	115	338	S_145	4963	115
219	S_26	6629	235	279	S_86	5789	235	339	S_146	4949	235
220	S_27	6615	115	280	S_87	5775	115	340	S_147	4935	115
221	S_28	6601	235	281	S_88	5761	235	341	S_148	4921	235
222	S_29	6587	115	282	S_89	5747	115	342	S_149	4907	115
223	S_30	6573	235	283	S_90	5733	235	343	S_150	4893	235
224	S_31	6559	115	284	S_91	5719	115	344	S_151	4879	115
225	S_32	6545	235	285	S_92	5705	235	345	S_152	4865	235
226	S_33	6531	115	286	S_93	5691	115	346	S_153	4851	115
227	S_34	6517	235	287	S_94	5677	235	347	S_154	4837	235
228	S_35	6503	115	288	S_95	5663	115	348	S_155	4823	115
229	S_36	6489	235	289	S_96	5649	235	349	S_156	4809	235
230	S_37	6475	115	290	S_97	5635	115	350	S_157	4795	115
231	S_38	6461	235	291	S_98	5621	235	351	S_158	4781	235
232	S_39	6447	115	292	S_99	5607	115	352	S_159	4767	115
233	S_40	6433	235	293	S_100	5593	235	353	S_160	4753	235
234	S_41	6419	115	294	S_101	5579	115	354	S_161	4739	115
235	S_42	6405	235	295	S_102	5565	235	355	S_162	4725	235
236	S_43	6391	115	296	S_103	5551	115	356	S_163	4711	115
237	S_44	6377	235	297	S_104	5537	235	357	S_164	4697	235
238	S_45	6363	115	298	S_105	5523	115	358	S_165	4683	115
239	S_46	6349	235	299	S_106	5509	235	359	S_166	4669	235
240	S_47	6335	115	300	S_107	5495	115	360	S_167	4655	115

NUM	NAME	X	Y	NUM	NAME	X	Y	NUM	NAME	X	Y
361	S_168	4641	235	421	S_228	3801	235	481	G_442	2821	235
362	S_169	4627	115	422	S_229	3787	115	482	G_441	2807	115
363	S_170	4613	235	423	S_230	3773	235	483	G_440	2793	235
364	S_171	4599	115	424	S_231	3759	115	484	G_439	2779	115
365	S_172	4585	235	425	S_232	3745	235	485	G_438	2765	235
366	S_173	4571	115	426	S_233	3731	115	486	G_437	2751	115
367	S_174	4557	235	427	S_234	3717	235	487	G_436	2737	235
368	S_175	4543	115	428	S_235	3703	115	488	G_435	2723	115
369	S_176	4529	235	429	S_236	3689	235	489	G_434	2709	235
370	S_177	4515	115	430	S_237	3675	115	490	G_433	2695	115
371	S_178	4501	235	431	S_238	3661	235	491	G_432	2681	235
372	S_179	4487	115	432	S_239	3647	115	492	G_431	2667	115
373	S_180	4473	235	433	S_240	3633	235	493	G_430	2653	235
374	S_181	4459	115	434	SHIELDING16	3605	235	494	G_429	2639	115
375	S_182	4445	235	435	SHIELDING17	3577	235	495	G_428	2625	235
376	S_183	4431	115	436	SHIELDING18	3549	235	496	G_427	2611	115
377	S_184	4417	235	437	COM2_R	3521	235	497	G_426	2597	235
378	S_185	4403	115	438	COM2_R	3493	235	498	G_425	2583	115
379	S_186	4389	235	439	COM2_R	3465	235	499	G_424	2569	235
380	S_187	4375	115	440	SHIELDING19	3437	235	500	G_423	2555	115
381	S_188	4361	235	441	SHIELDING20	3409	235	501	G_422	2541	235
382	S_189	4347	115	442	SHIELDING21	3381	235	502	G_421	2527	115
383	S_190	4333	235	443	G_480	3353	235	503	G_420	2513	235
384	S_191	4319	115	444	G_479	3339	115	504	G_419	2499	115
385	S_192	4305	235	445	G_478	3325	235	505	G_418	2485	235
386	S_193	4291	115	446	G_477	3311	115	506	G_417	2471	115
387	S_194	4277	235	447	G_476	3297	235	507	G_416	2457	235
388	S_195	4263	115	448	G_475	3283	115	508	G_415	2443	115
389	S_196	4249	235	449	G_474	3269	235	509	G_414	2429	235
390	S_197	4235	115	450	G_473	3255	115	510	G_413	2415	115
391	S_198	4221	235	451	G_472	3241	235	511	G_412	2401	235
392	S_199	4207	115	452	G_471	3227	115	512	G_411	2387	115
393	S_200	4193	235	453	G_470	3213	235	513	G_410	2373	235
394	S_201	4179	115	454	G_469	3199	115	514	G_409	2359	115
395	S_202	4165	235	455	G_468	3185	235	515	G_408	2345	235
396	S_203	4151	115	456	G_467	3171	115	516	G_407	2331	115
397	S_204	4137	235	457	G_466	3157	235	517	G_406	2317	235
398	S_205	4123	115	458	G_465	3143	115	518	G_405	2303	115
399	S_206	4109	235	459	G_464	3129	235	519	G_404	2289	235
400	S_207	4095	115	460	G_463	3115	115	520	G_403	2275	115
401	S_208	4081	235	461	G_462	3101	235	521	G_402	2261	235
402	S_209	4067	115	462	G_461	3087	115	522	G_401	2247	115
403	S_210	4053	235	463	G_460	3073	235	523	G_400	2233	235
404	S_211	4039	115	464	G_459	3059	115	524	G_399	2219	115
405	S_212	4025	235	465	G_458	3045	235	525	G_398	2205	235
406	S_213	4011	115	466	G_457	3031	115	526	G_397	2191	115
407	S_214	3997	235	467	G_456	3017	235	527	G_396	2177	235
408	S_215	3983	115	468	G_455	3003	115	528	G_395	2163	115
409	S_216	3969	235	469	G_454	2989	235	529	G_394	2149	235
410	S_217	3955	115	470	G_453	2975	115	530	G_393	2135	115
411	S_218	3941	235	471	G_452	2961	235	531	G_392	2121	235
412	S_219	3927	115	472	G_451	2947	115	532	G_391	2107	115
413	S_220	3913	235	473	G_450	2933	235	533	G_390	2093	235
414	S_221	3899	115	474	G_449	2919	115	534	G_389	2079	115
415	S_222	3885	235	475	G_448	2905	235	535	G_388	2065	235
416	S_223	3871	115	476	G_447	2891	115	536	G_387	2051	115
417	S_224	3857	235	477	G_446	2877	235	537	G_386	2037	235
418	S_225	3843	115	478	G_445	2863	115	538	G_385	2023	115
419	S_226	3829	235	479	G_444	2849	235	539	G_384	2009	235
420	S_227	3815	115	480	G_443	2835	115	540	G_383	1995	115

NUM	NAME	X	Y	NUM	NAME	X	Y	NUM	NAME	X	Y
541	G_382	1981	235	601	G_322	1141	235	661	G_262	301	235
542	G_381	1967	115	602	G_321	1127	115	662	G_261	287	115
543	G_380	1953	235	603	G_320	1113	235	663	G_260	273	235
544	G_379	1939	115	604	G_319	1099	115	664	G_259	259	115
545	G_378	1925	235	605	G_318	1085	235	665	G_258	245	235
546	G_377	1911	115	606	G_317	1071	115	666	G_257	231	115
547	G_376	1897	235	607	G_316	1057	235	667	G_256	217	235
548	G_375	1883	115	608	G_315	1043	115	668	G_255	203	115
549	G_374	1869	235	609	G_314	1029	235	669	G_254	189	235
550	G_373	1855	115	610	G_313	1015	115	670	G_253	175	115
551	G_372	1841	235	611	G_312	1001	235	671	G_252	161	235
552	G_371	1827	115	612	G_311	987	115	672	G_251	147	115
553	G_370	1813	235	613	G_310	973	235	673	G_250	133	235
554	G_369	1799	115	614	G_309	959	115	674	G_249	119	115
555	G_368	1785	235	615	G_308	945	235	675	G_248	105	235
556	G_367	1771	115	616	G_307	931	115	676	G_247	91	115
557	G_366	1757	235	617	G_306	917	235	677	G_246	77	235
558	G_365	1743	115	618	G_305	903	115	678	G_245	63	115
559	G_364	1729	235	619	G_304	889	235	679	G_244	49	235
560	G_363	1715	115	620	G_303	875	115	680	G_243	35	115
561	G_362	1701	235	621	G_302	861	235	681	G_242	21	235
562	G_361	1687	115	622	G_301	847	115	682	G_241	7	115
563	G_360	1673	235	623	G_300	833	235	683	G_240	-7	235
564	G_359	1659	115	624	G_299	819	115	684	G_239	-21	115
565	G_358	1645	235	625	G_298	805	235	685	G_238	-35	235
566	G_357	1631	115	626	G_297	791	115	686	G_237	-49	115
567	G_356	1617	235	627	G_296	777	235	687	G_236	-63	235
568	G_355	1603	115	628	G_295	763	115	688	G_235	-77	115
569	G_354	1589	235	629	G_294	749	235	689	G_234	-91	235
570	G_353	1575	115	630	G_293	735	115	690	G_233	-105	115
571	G_352	1561	235	631	G_292	721	235	691	G_232	-119	235
572	G_351	1547	115	632	G_291	707	115	692	G_231	-133	115
573	G_350	1533	235	633	G_290	693	235	693	G_230	-147	235
574	G_349	1519	115	634	G_289	679	115	694	G_229	-161	115
575	G_348	1505	235	635	G_288	665	235	695	G_228	-175	235
576	G_347	1491	115	636	G_287	651	115	696	G_227	-189	115
577	G_346	1477	235	637	G_286	637	235	697	G_226	-203	235
578	G_345	1463	115	638	G_285	623	115	698	G_225	-217	115
579	G_344	1449	235	639	G_284	609	235	699	G_224	-231	235
580	G_343	1435	115	640	G_283	595	115	700	G_223	-245	115
581	G_342	1421	235	641	G_282	581	235	701	G_222	-259	235
582	G_341	1407	115	642	G_281	567	115	702	G_221	-273	115
583	G_340	1393	235	643	G_280	553	235	703	G_220	-287	235
584	G_339	1379	115	644	G_279	539	115	704	G_219	-301	115
585	G_338	1365	235	645	G_278	525	235	705	G_218	-315	235
586	G_337	1351	115	646	G_277	511	115	706	G_217	-329	115
587	G_336	1337	235	647	G_276	497	235	707	G_216	-343	235
588	G_335	1323	115	648	G_275	483	115	708	G_215	-357	115
589	G_334	1309	235	649	G_274	469	235	709	G_214	-371	235
590	G_333	1295	115	650	G_273	455	115	710	G_213	-385	115
591	G_332	1281	235	651	G_272	441	235	711	G_212	-399	235
592	G_331	1267	115	652	G_271	427	115	712	G_211	-413	115
593	G_330	1253	235	653	G_270	413	235	713	G_210	-427	235
594	G_329	1239	115	654	G_269	399	115	714	G_209	-441	115
595	G_328	1225	235	655	G_268	385	235	715	G_208	-455	235
596	G_327	1211	115	656	G_267	371	115	716	G_207	-469	115
597	G_326	1197	235	657	G_266	357	235	717	G_206	-483	235
598	G_325	1183	115	658	G_265	343	115	718	G_205	-497	115
599	G_324	1169	235	659	G_264	329	235	719	G_204	-511	235
600	G_323	1155	115	660	G_263	315	115	720	G_203	-525	115

NUM	NAME	X	Y	NUM	NAME	X	Y	NUM	NAME	X	Y
721	G_202	-539	235	781	G_142	-1379	235	841	G_82	-2219	235
722	G_201	-553	115	782	G_141	-1393	115	842	G_81	-2233	115
723	G_200	-567	235	783	G_140	-1407	235	843	G_80	-2247	235
724	G_199	-581	115	784	G_139	-1421	115	844	G_79	-2261	115
725	G_198	-595	235	785	G_138	-1435	235	845	G_78	-2275	235
726	G_197	-609	115	786	G_137	-1449	115	846	G_77	-2289	115
727	G_196	-623	235	787	G_136	-1463	235	847	G_76	-2303	235
728	G_195	-637	115	788	G_135	-1477	115	848	G_75	-2317	115
729	G_194	-651	235	789	G_134	-1491	235	849	G_74	-2331	235
730	G_193	-665	115	790	G_133	-1505	115	850	G_73	-2345	115
731	G_192	-679	235	791	G_132	-1519	235	851	G_72	-2359	235
732	G_191	-693	115	792	G_131	-1533	115	852	G_71	-2373	115
733	G_190	-707	235	793	G_130	-1547	235	853	G_70	-2387	235
734	G_189	-721	115	794	G_129	-1561	115	854	G_69	-2401	115
735	G_188	-735	235	795	G_128	-1575	235	855	G_68	-2415	235
736	G_187	-749	115	796	G_127	-1589	115	856	G_67	-2429	115
737	G_186	-763	235	797	G_126	-1603	235	857	G_66	-2443	235
738	G_185	-777	115	798	G_125	-1617	115	858	G_65	-2457	115
739	G_184	-791	235	799	G_124	-1631	235	859	G_64	-2471	235
740	G_183	-805	115	800	G_123	-1645	115	860	G_63	-2485	115
741	G_182	-819	235	801	G_122	-1659	235	861	G_62	-2499	235
742	G_181	-833	115	802	G_121	-1673	115	862	G_61	-2513	115
743	G_180	-847	235	803	G_120	-1687	235	863	G_60	-2527	235
744	G_179	-861	115	804	G_119	-1701	115	864	G_59	-2541	115
745	G_178	-875	235	805	G_118	-1715	235	865	G_58	-2555	235
746	G_177	-889	115	806	G_117	-1729	115	866	G_57	-2569	115
747	G_176	-903	235	807	G_116	-1743	235	867	G_56	-2583	235
748	G_175	-917	115	808	G_115	-1757	115	868	G_55	-2597	115
749	G_174	-931	235	809	G_114	-1771	235	869	G_54	-2611	235
750	G_173	-945	115	810	G_113	-1785	115	870	G_53	-2625	115
751	G_172	-959	235	811	G_112	-1799	235	871	G_52	-2639	235
752	G_171	-973	115	812	G_111	-1813	115	872	G_51	-2653	115
753	G_170	-987	235	813	G_110	-1827	235	873	G_50	-2667	235
754	G_169	-1001	115	814	G_109	-1841	115	874	G_49	-2681	115
755	G_168	-1015	235	815	G_108	-1855	235	875	G_48	-2695	235
756	G_167	-1029	115	816	G_107	-1869	115	876	G_47	-2709	115
757	G_166	-1043	235	817	G_106	-1883	235	877	G_46	-2723	235
758	G_165	-1057	115	818	G_105	-1897	115	878	G_45	-2737	115
759	G_164	-1071	235	819	G_104	-1911	235	879	G_44	-2751	235
760	G_163	-1085	115	820	G_103	-1925	115	880	G_43	-2765	115
761	G_162	-1099	235	821	G_102	-1939	235	881	G_42	-2779	235
762	G_161	-1113	115	822	G_101	-1953	115	882	G_41	-2793	115
763	G_160	-1127	235	823	G_100	-1967	235	883	G_40	-2807	235
764	G_159	-1141	115	824	G_99	-1981	115	884	G_39	-2821	115
765	G_158	-1155	235	825	G_98	-1995	235	885	G_38	-2835	235
766	G_157	-1169	115	826	G_97	-2009	115	886	G_37	-2849	115
767	G_156	-1183	235	827	G_96	-2023	235	887	G_36	-2863	235
768	G_155	-1197	115	828	G_95	-2037	115	888	G_35	-2877	115
769	G_154	-1211	235	829	G_94	-2051	235	889	G_34	-2891	235
770	G_153	-1225	115	830	G_93	-2065	115	890	G_33	-2905	115
771	G_152	-1239	235	831	G_92	-2079	235	891	G_32	-2919	235
772	G_151	-1253	115	832	G_91	-2093	115	892	G_31	-2933	115
773	G_150	-1267	235	833	G_90	-2107	235	893	G_30	-2947	235
774	G_149	-1281	115	834	G_89	-2121	115	894	G_29	-2961	115
775	G_148	-1295	235	835	G_88	-2135	235	895	G_28	-2975	235
776	G_147	-1309	115	836	G_87	-2149	115	896	G_27	-2989	115
777	G_146	-1323	235	837	G_86	-2163	235	897	G_26	-3003	235
778	G_145	-1337	115	838	G_85	-2177	115	898	G_25	-3017	115
779	G_144	-1351	235	839	G_84	-2191	235	899	G_24	-3031	235
780	G_143	-1365	115	840	G_83	-2205	115	900	G_23	-3045	115

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901	G_22	-3059	235	961	S_451	-4039	115	1021	S_391	-4879	115
902	G_21	-3073	115	962	S_450	-4053	235	1022	S_390	-4893	235
903	G_20	-3087	235	963	S_449	-4067	115	1023	S_389	-4907	115
904	G_19	-3101	115	964	S_448	-4081	235	1024	S_388	-4921	235
905	G_18	-3115	235	965	S_447	-4095	115	1025	S_387	-4935	115
906	G_17	-3129	115	966	S_446	-4109	235	1026	S_386	-4949	235
907	G_16	-3143	235	967	S_445	-4123	115	1027	S_385	-4963	115
908	G_15	-3157	115	968	S_444	-4137	235	1028	S_384	-4977	235
909	G_14	-3171	235	969	S_443	-4151	115	1029	S_383	-4991	115
910	G_13	-3185	115	970	S_442	-4165	235	1030	S_382	-5005	235
911	G_12	-3199	235	971	S_441	-4179	115	1031	S_381	-5019	115
912	G_11	-3213	115	972	S_440	-4193	235	1032	S_380	-5033	235
913	G_10	-3227	235	973	S_439	-4207	115	1033	S_379	-5047	115
914	G_9	-3241	115	974	S_438	-4221	235	1034	S_378	-5061	235
915	G_8	-3255	235	975	S_437	-4235	115	1035	S_377	-5075	115
916	G_7	-3269	115	976	S_436	-4249	235	1036	S_376	-5089	235
917	G_6	-3283	235	977	S_435	-4263	115	1037	S_375	-5103	115
918	G_5	-3297	115	978	S_434	-4277	235	1038	S_374	-5117	235
919	G_4	-3311	235	979	S_433	-4291	115	1039	S_373	-5131	115
920	G_3	-3325	115	980	S_432	-4305	235	1040	S_372	-5145	235
921	G_2	-3339	235	981	S_431	-4319	115	1041	S_371	-5159	115
922	G_1	-3353	115	982	S_430	-4333	235	1042	S_370	-5173	235
923	SHIELDING22	-3381	235	983	S_429	-4347	115	1043	S_369	-5187	115
924	SHIELDING23	-3409	235	984	S_428	-4361	235	1044	S_368	-5201	235
925	SHIELDING24	-3437	235	985	S_427	-4375	115	1045	S_367	-5215	115
926	COM1_R	-3465	235	986	S_426	-4389	235	1046	S_366	-5229	235
927	COM1_R	-3493	235	987	S_425	-4403	115	1047	S_365	-5243	115
928	COM1_R	-3521	235	988	S_424	-4417	235	1048	S_364	-5257	235
929	SHIELDING25	-3549	235	989	S_423	-4431	115	1049	S_363	-5271	115
930	SHIELDING26	-3577	235	990	S_422	-4445	235	1050	S_362	-5285	235
931	SHIELDING27	-3605	235	991	S_421	-4459	115	1051	S_361	-5299	115
932	S_480	-3633	235	992	S_420	-4473	235	1052	S_360	-5313	235
933	S_479	-3647	115	993	S_419	-4487	115	1053	S_359	-5327	115
934	S_478	-3661	235	994	S_418	-4501	235	1054	S_358	-5341	235
935	S_477	-3675	115	995	S_417	-4515	115	1055	S_357	-5355	115
936	S_476	-3689	235	996	S_416	-4529	235	1056	S_356	-5369	235
937	S_475	-3703	115	997	S_415	-4543	115	1057	S_355	-5383	115
938	S_474	-3717	235	998	S_414	-4557	235	1058	S_354	-5397	235
939	S_473	-3731	115	999	S_413	-4571	115	1059	S_353	-5411	115
940	S_472	-3745	235	1000	S_412	-4585	235	1060	S_352	-5425	235
941	S_471	-3759	115	1001	S_411	-4599	115	1061	S_351	-5439	115
942	S_470	-3773	235	1002	S_410	-4613	235	1062	S_350	-5453	235
943	S_469	-3787	115	1003	S_409	-4627	115	1063	S_349	-5467	115
944	S_468	-3801	235	1004	S_408	-4641	235	1064	S_348	-5481	235
945	S_467	-3815	115	1005	S_407	-4655	115	1065	S_347	-5495	115
946	S_466	-3829	235	1006	S_406	-4669	235	1066	S_346	-5509	235
947	S_465	-3843	115	1007	S_405	-4683	115	1067	S_345	-5523	115
948	S_464	-3857	235	1008	S_404	-4697	235	1068	S_344	-5537	235
949	S_463	-3871	115	1009	S_403	-4711	115	1069	S_343	-5551	115
950	S_462	-3885	235	1010	S_402	-4725	235	1070	S_342	-5565	235
951	S_461	-3899	115	1011	S_401	-4739	115	1071	S_341	-5579	115
952	S_460	-3913	235	1012	S_400	-4753	235	1072	S_340	-5593	235
953	S_459	-3927	115	1013	S_399	-4767	115	1073	S_339	-5607	115
954	S_458	-3941	235	1014	S_398	-4781	235	1074	S_338	-5621	235
955	S_457	-3955	115	1015	S_397	-4795	115	1075	S_337	-5635	115
956	S_456	-3969	235	1016	S_396	-4809	235	1076	S_336	-5649	235
957	S_455	-3983	115	1017	S_395	-4823	115	1077	S_335	-5663	115
958	S_454	-3997	235	1018	S_394	-4837	235	1078	S_334	-5677	235
959	S_453	-4011	115	1019	S_393	-4851	115	1079	S_333	-5691	115
960	S_452	-4025	235	1020	S_392	-4865	235	1080	S_332	-5705	235

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1081	S_331	-5719	115	1114	S_298	-6181	235	1147	S_265	-6643	115
1082	S_330	-5733	235	1115	S_297	-6195	115	1148	S_264	-6657	235
1083	S_329	-5747	115	1116	S_296	-6209	235	1149	S_263	-6671	115
1084	S_328	-5761	235	1117	S_295	-6223	115	1150	S_262	-6685	235
1085	S_327	-5775	115	1118	S_294	-6237	235	1151	S_261	-6699	115
1086	S_326	-5789	235	1119	S_293	-6251	115	1152	S_260	-6713	235
1087	S_325	-5803	115	1120	S_292	-6265	235	1153	S_259	-6727	115
1088	S_324	-5817	235	1121	S_291	-6279	115	1154	S_258	-6741	235
1089	S_323	-5831	115	1122	S_290	-6293	235	1155	S_257	-6755	115
1090	S_322	-5845	235	1123	S_289	-6307	115	1156	S_256	-6769	235
1091	S_321	-5859	115	1124	S_288	-6321	235	1157	S_255	-6783	115
1092	S_320	-5873	235	1125	S_287	-6335	115	1158	S_254	-6797	235
1093	S_319	-5887	115	1126	S_286	-6349	235	1159	S_253	-6811	115
1094	S_318	-5901	235	1127	S_285	-6363	115	1160	S_252	-6825	235
1095	S_317	-5915	115	1128	S_284	-6377	235	1161	S_251	-6839	115
1096	S_316	-5929	235	1129	S_283	-6391	115	1162	S_250	-6853	235
1097	S_315	-5943	115	1130	S_282	-6405	235	1163	S_249	-6867	115
1098	S_314	-5957	235	1131	S_281	-6419	115	1164	S_248	-6881	235
1099	S_313	-5971	115	1132	S_280	-6433	235	1165	S_247	-6895	115
1100	S_312	-5985	235	1133	S_279	-6447	115	1166	S_246	-6909	235
1101	S_311	-5999	115	1134	S_278	-6461	235	1167	S_245	-6923	115
1102	S_310	-6013	235	1135	S_277	-6475	115	1168	S_244	-6937	235
1103	S_309	-6027	115	1136	S_276	-6489	235	1169	S_243	-6951	115
1104	S_308	-6041	235	1137	S_275	-6503	115	1170	S_242	-6965	235
1105	S_307	-6055	115	1138	S_274	-6517	235	1171	S_241	-6979	115
1106	S_306	-6069	235	1139	S_273	-6531	115	1172	SHIELDING28	-7029	235
1107	S_305	-6083	115	1140	S_272	-6545	235	1173	SHIELDING29	-7057	235
1108	S_304	-6097	235	1141	S_271	-6559	115	1174	SHIELDING30	-7085	235
1109	S_303	-6111	115	1142	S_270	-6573	235	1175	SHIELDING31	-7113	235
1110	S_302	-6125	235	1143	S_269	-6587	115	1176	SHIELDING32	-7141	235
1111	S_301	-6139	115	1144	S_268	-6601	235	1177	SHIELDING33	-7169	235
1112	S_300	-6153	235	1145	S_267	-6615	115				
1113	S_299	-6167	115	1146	S_266	-6629	235				

15. Ordering Information

Part NO.	Package
HX8268-C00xPDxxx	PD : mean COG xxx : mean chip thickness (μm)

16. Revision History

Version	Date	Description of Changes
01	2010/06/23	Setup