# Features

- Fully qualified Bluetooth® v2.1 + EDR Specification
- Piconet and scatternet support
- Minimum external components
- Low-power 1.5V operation, 1.8V to 3.6V I/O
- Integrated 1.8V and 1.5V regulators
- UART to 4Mbaud
- SDIO (Bluetooth Type A)/CSPI interface
- Integrated CSR AuriStream® low-power codec for wide-band voice quality
- Deep sleep SDIO operation
- 40-lead 6 x 6 x 0.9mm 0.5mm pitch QFN
- Support for IEEE 802.11 coexistence
- Green ( RoHS and no antimony or halogenated flame retardants)

# BlueCore®6-ROM QFN

## Single-chip Bluetooth v2.1 + EDR System

**Production Information**

**BC63B239A**

**Issue 9**

# General Description

**BlueCore®6-ROM QFN** is a single-chip radio and baseband IC for Bluetooth 2.4GHz systems including EDR to 3Mbps.

With the on-chip CSR Bluetooth software stack, it provides a fully compliant Bluetooth v2.1 + EDR specification system for data and voice communications.

BlueCore6-ROM QFN has been designed to reduce the number of external components required which ensures production costs are minimised.

BlueCore6-ROM QFN includes AuriStream, which offers significant power reduction over the CVSD-based system when used at both ends of the link.

# Applications

- Cellular handsets
- PDAs
- Automotive

The device incorporates auto-calibration and BIST routines to simplify development, type approval and production test. All hardware and device firmware is fully compliant with the Bluetooth v2.1 + EDR specification.

To improve the performance of both Bluetooth and 802.11b/g co-located systems a wide range of coexistence features are available including a variety of hardware signalling: basic activity signalling and Intel WCS activity and channel signalling.



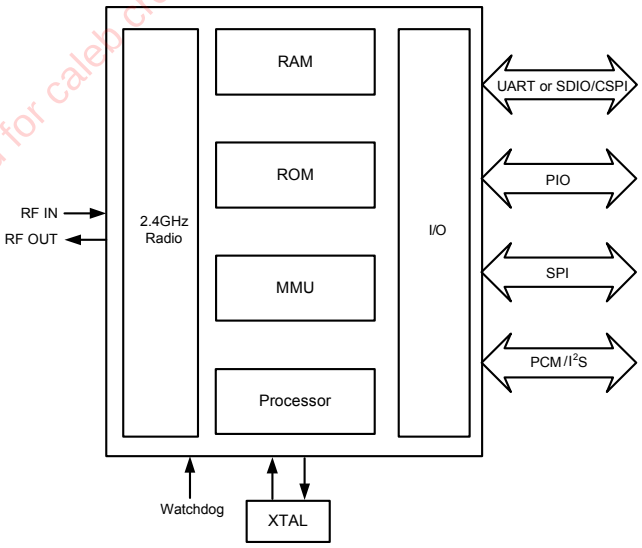


**Figure: System Architecture**

# Document History

| Revision | Date | Change Reason |
|---|---|---|
| 1 | 15 MAR 07 | Original publication of this document. |
| 2 | 14 MAY 07 | Application Schematic added. Digital Audio Interface ($I^2S$) to Audio Interfaces section added. Device Diagram updated. Package Information, Bluetooth RF Interface Description, Power Control and Regulation, Electrical Characteristics, and Terms and Definitions sections updated. Editorial changes throughout. |
| 3 | 16 APR 08 | Minimum temperatures changed. Device diagram and application schematic updated. |
| 4 | 15 AUG 08 | Device Terminal Functions, Electrical Characteristics and Ordering Information sections updated. Editorial changes throughout. |
| 5 | 12 SEP 08 | Recommended Operating Conditions table footnote updated. |
| 6 | 18 JUN 09 | Updates to Applications, Device Details, Ordering Information and 32kHz clock domain information. ROM size corrected. |
| 7 | 22 JUL 09 | Section 11.4 updated. |
| 8 | 21 AUG 09 | Removed Additional Software for Other Embedded Applications section. Updated High-Voltage Linear Regulator and Device Terminal Functions sections. |
| 9 | 27 OCT 09 | Package Dimensions figure corrected.<br>If you have any comments about this document, email comments@csr.com giving the number, title and section with your feedback. |

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The status of this Product Data Sheet is **Production Information**.

CSR Product Data Sheets progress according to the following format:

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Information for designers concerning CSR product in development. All values specified are the target values of the design. Minimum and maximum values specified are only given as guidance to the final specification limits and must not be considered as the final values.

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Final Data Sheet including the guaranteed minimum and maximum limits for the electrical specifications.

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# List of Equations

# 1 Device Details

### Bluetooth Radio

- Common TX/RX terminal simplifies external matching; eliminates external antenna switch
- No external trimming is required in production
- Bluetooth v2.1 + EDR Specification compliant

### Bluetooth Transmitter

- 8dBm RF transmit power with level control from on-chip 6-bit DAC over a dynamic range >30dB

### Bluetooth Receiver

- Receiver sensitivity of -90dBm
- Integrated channel filters
- Digital demodulator for improved sensitivity and co-channel rejection
- Real-time digitised RSSI available on HCI interface
- Fast AGC for enhanced dynamic range
- Channel classification for AFH

### Synthesiser

- Fully integrated synthesiser requires no external VCO varactor diode, resonator or loop filter
- Compatible with crystals 16-26MHz or an external clock between 12-52MHz

### Baseband and Software

- AuriStream (16, 24, 32, 40Kbps) codec
- Internal 48KB RAM, allows full-speed data transfer, mixed voice and data, and full piconet operation, including all EDR packet types
- Logic for forward error correction, header error control, access code correlation, CRC, demodulation, encryption bit stream generation, whitening and transmit pulse shaping. Supports all Bluetooth v2.1 + EDR features including eSCO and AFH
- Transcoders for A-law, μ-law and linear voice from host and A-law, μ-law and CVSD voice over air

### Physical Interfaces

- SDIO and CSPI
- SPI interface up to 4Mbps for system debugging
- UART interface with programmable data rate up to 4Mbaud
- Bi-directional serial programmable audio interface supporting PCM and $I^2S$ formats

### Auxiliary Features

- Crystal oscillator with built-in digital trimming
- Clock request output to control an external clock
- Device can run in low power modes from an external 32768Hz clock signal
- Power management includes digital shutdown, and wake up commands with an integrated low power oscillator for ultra low power Park/Sniff/Hold mode
- Auto Baud Rate setting, subject to host interface in use
- On-chip linear regulators:
  - 1.8V output from typical 2.7-5.5V input to power I/O ring (load current 70mA)

    second low dropout linear regulator producing 1.5V core voltage from 1.8V
- Power-on-reset cell detects low supply voltage
- Arbitrary sequencing of power supplies is permitted

### Bluetooth Stack

CSR's Bluetooth Protocol Stack runs on the on-chip MCU in the configuration:

- Standard HCI over UART

### Package Options

- 40-lead 6 x 6 x 0.9mm, 0.5mm pitch QFN.

# 2 Device Diagram

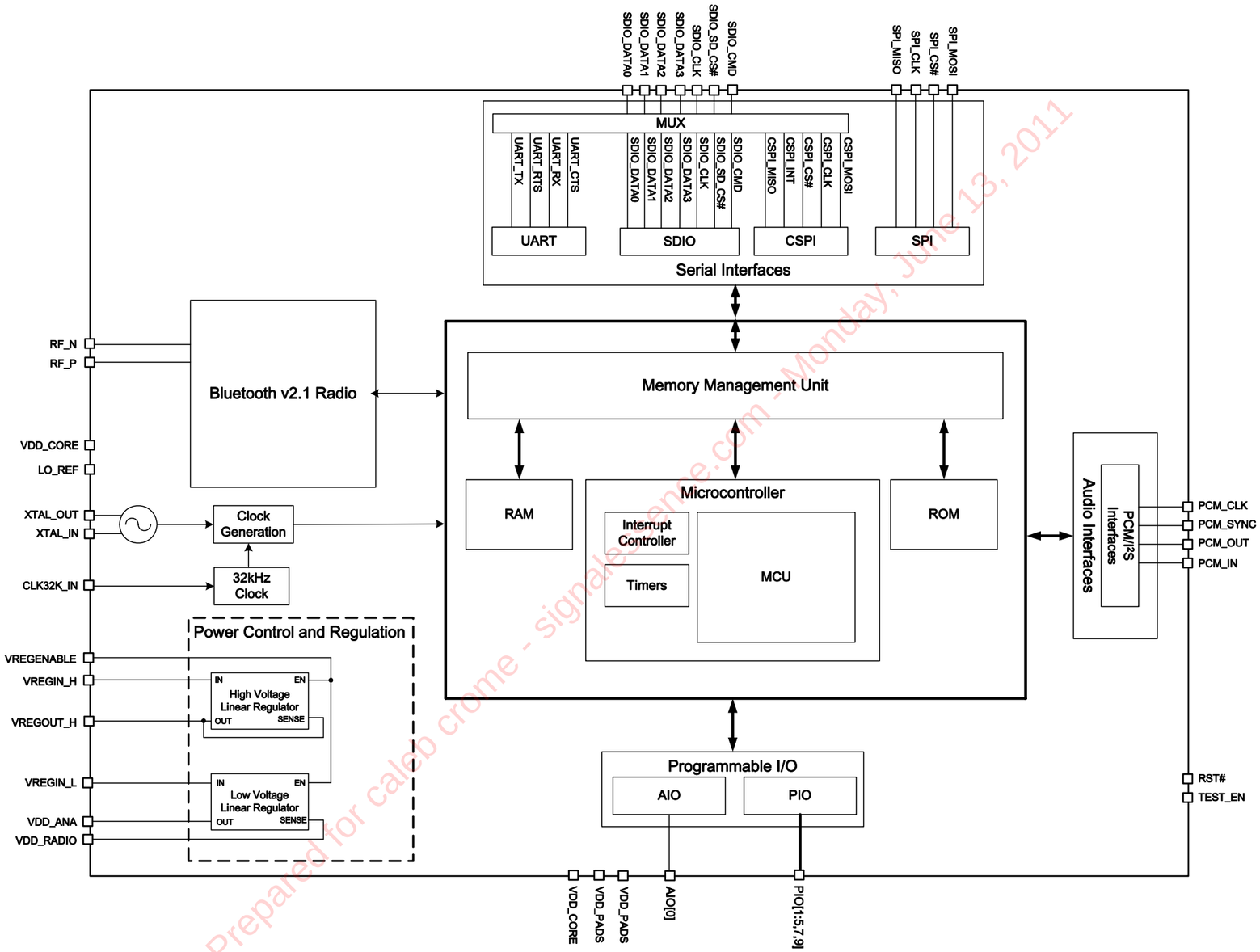



Figure 2.1: Device Diagram

# 3 Package Information

## 3.1 Device Pinout

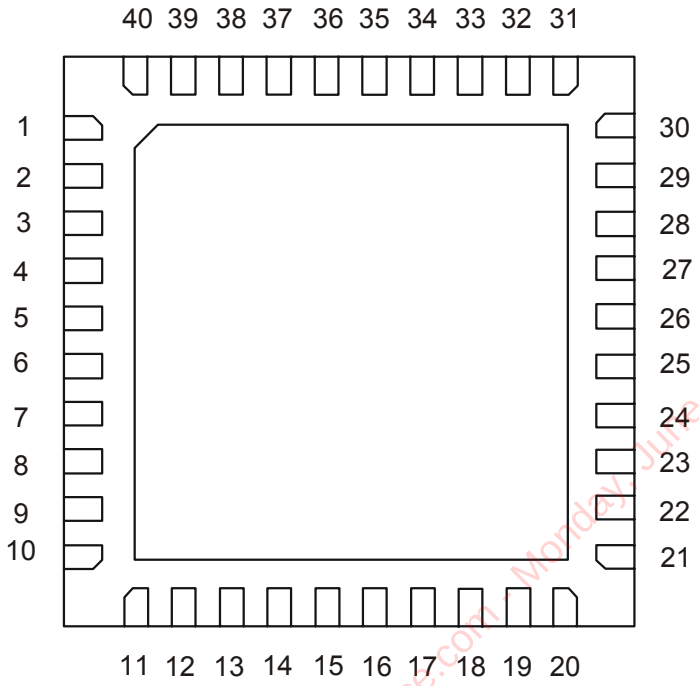



**Figure 3.1: BlueCore6-ROM QFN Device Pinout**

## 3.2 Device Terminal Functions

| Bluetooth Radio | Lead | Pad Type | Supply Domain | Description |
|---|---|---|---|---|
| RF_N | 7 | RF | VDD_RADIO | Transmitter output/switched receiver input |
| RF_P | 6 | RF | VDD_RADIO | Complement of RF_N |

| Synthesiser and Oscillator | Lead | Pad Type | Supply Domain | Description |
|---|---|---|---|---|
| XTAL_IN | 11 | Analogue | VDD_ANA | For crystal or external clock input |
| XTAL_OUT | 12 | Analogue | VDD_ANA | Drive for crystal |
| LO_REF | 13 | Analogue | VDD_ANA | Reference voltage decoupling |
| CLK_32K | 27 | Input with weak internal pull-down | VDD_PADS | Dedicated 32kHz external reference clock input |

| SPI Interface | Lead | Pad Type | Supply Domain | Description |
|---|---|---|---|---|
| SPI_MOSI | 3 | Input, with weak internal pull-down | VDD_PADS | SPI data input |
| SPI_CS# | 2 | Bi-directional with weak internal pull-down | VDD_PADS | Chip select for SPI, active low |
| SPI_CLK | 1 | Bi-directional with weak internal pull-down | VDD_PADS | SPI clock |
| SPI_MISO | 40 | Output, tri-state, with weak internal pull-down | VDD_PADS | SPI data output |

| SDIO/CSPI/UART Interfaces | Lead | Pad Type | Supply Domain | Description |
|---|---|---|---|---|
| SDIO_DATA[0] | 28 | Bi-directional with weak internal pull-up | VDD_PADS | Synchronous data input/output |
| CSPI_MISO | | | | CSPI data output |
| UART_TX | | | | UART data output, active high |
| SDIO_DATA[1] | 29 | Bi-directional with weak internal pull-up | VDD_PADS | Synchronous data input/output |
| CSPI_INT | | | | CSPI data input |
| UART_RTS | | | | UART request to send, active low |
| SDIO_DATA[2] | 30 | Bi-directional with weak internal pull-up | VDD_PADS | Synchronous data input/output |
| UART_RX | | | | UART data input, active high |

| SDIO/CSPI/UART Interfaces | Lead | Pad Type | Supply Domain | Description |
|---|---|---|---|---|
| SDIO_DATA[3] | 31 | Bi-directional with weak internal pull-up | VDD_PADS | Synchronous data input/output |
| CSPI_CS# | | | | Chip select for CSPI, active low |
| UART_CTS | | | | UART clear to send, active low |
| SDIO_CLK | 32 | Bi-directional with weak internal pull-up | VDD_PADS | SDIO Clock |
| CSPI_CLK | | | | CSPI Clock |
| SDIO_CMD | 34 | Bi-directional with weak internal pull-up | VDD_PADS | SDIO data input |
| CSPI_MOSI | | | | CSPI data input |
| SDIO_SD_CS# | 33 | Bi-directional with weak internal pull-up | VDD_PADS | SDIO chip select to allow SDIO Accesses |

| PCM Interface | Lead | Pad Type | Supply Domain | Description |
|---|---|---|---|---|
| PCM_OUT | 38 | Output, tri-state, with weak internal pull-down | VDD_PADS | Synchronous data output |
| PCM_IN | 39 | Input, with weak internal pull-down | VDD_PADS | Synchronous data input |
| PCM_SYNC | 36 | Bi-directional with weak internal pull-down | VDD_PADS | Synchronous data sync |
| PCM_CLK | 37 | Bi-directional with weak internal pull-down | VDD_PADS | Synchronous data clock |

| PIO Port | Lead | Pad Type | Supply Domain | Description |
|---|---|---|---|---|
| PIO[9] | 25 | Bi-directional with programmable strength internal pull-up/down | VDD_PADS | Programmable input/output line |
| PIO[7] | 24 | Bi-directional with programmable strength internal pull-up/down | VDD_PADS | Programmable input/output line |
| PIO[5] | 23 | Bi-directional with programmable strength internal pull-up/down | VDD_PADS | Programmable input/output line |
| PIO[4] | 22 | Bi-directional with programmable strength internal pull-up/down | VDD_PADS | Programmable input/output line |
| PIO[3] | 21 | Bi-directional with programmable strength internal pull-up/down | VDD_PADS | Programmable input/output line |
| PIO[2] | 20 | Bi-directional with programmable strength internal pull-up/down | VDD_PADS | Programmable input/output line |
| PIO[1] | 19 | Bi-directional with programmable strength internal pull-up/down | VDD_PADS | Programmable input/output line |
| AIO[0] | 14 | Bi-directional | VDD_ANA | Programmable input/output line |

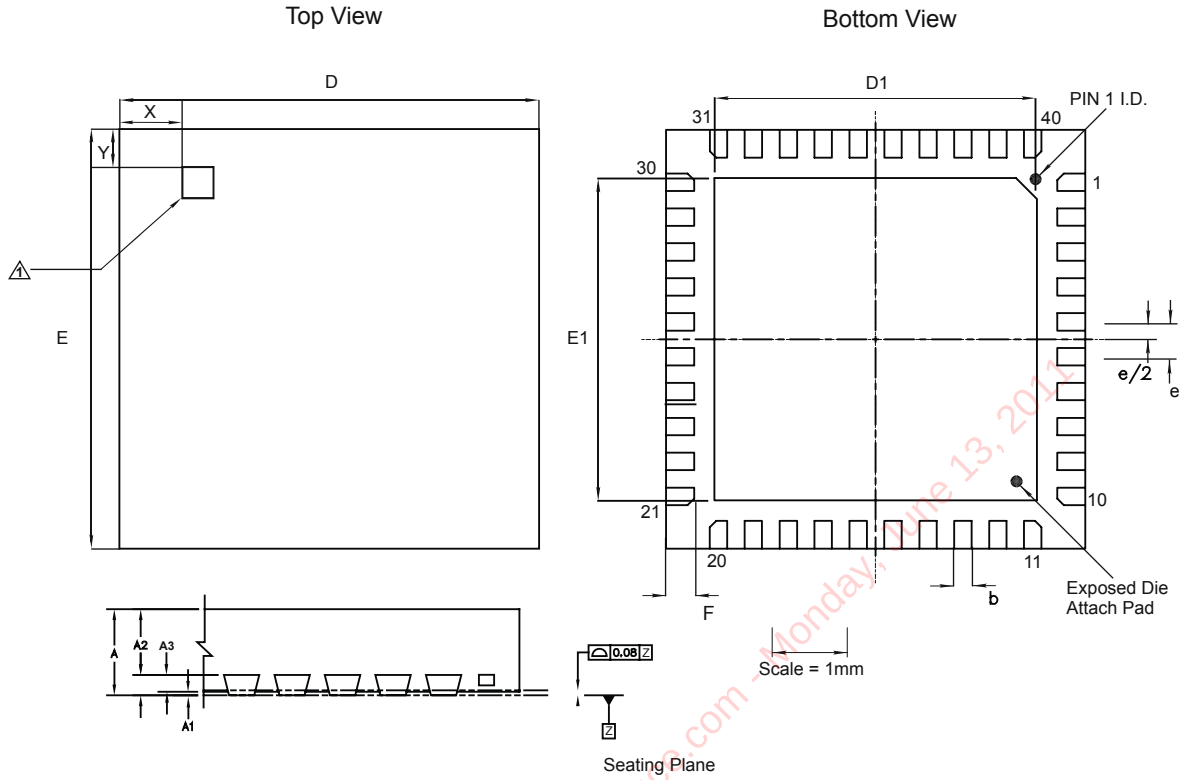
| Test and Debug | Lead | Pad Type | Supply Domain | Description |
|---|---|---|---|---|
| RST# | 4 | Input with weak internal pull-up | VDD_PADS | Reset if low. Input debounced so must be low for >5ms to cause a reset |
| TEST_EN | 5 | Input with strong internal pull-down | VDD_PADS | For test purposes only (leave unconnected) |

| Power Supplies Control | Lead | Description |
|---|---|---|
| VREGENABLE | 17 | Take high to enable low and high voltage regulators |

| Power Supplies | Lead | Description |
|---|---|---|
| VREGIN_L | 9 | Input to internal low-voltage regulator |
| VREGIN_H | 16 | Input to internal high-voltage regulator |
| VREGOUT_H | 15 | High-voltage regulator output |

| Power Supplies | Lead | Description |
|---|---|---|
| VDD_PADS | 18, 35 | Positive supply for digital input/output ports<br><br>including PIO[1:5, 7, 9] |
| VDD_CORE | 26 | Positive supply for internal digital circuitry |
| VDD_RADIO | 8 | Positive supply for RF circuitry |
| VDD_ANA | 10 | Positive supply for analogue circuitry, AIO[0]. Output from internal 1.5V regulator. |
| VSS | Exposed pad | Ground connections |

## 3.3 Package Dimensions




| Description | 40-Lead Quad Flat No-lead (QFN) Package | | | |
|---|---|---|---|---|
| **Size** | 6 x 6 x 0.9mm | | | |
| **Pitch** | 0.5mm | | | |
| **Dimension** | **Minimum** | **Typical** | **Maximum** | **Notes** |
| A | 0.80 | 0.85 | 0.90 | 1 Top-side polarity mark. The dimensions of the square polarity mark are TBD x TBDmm. |
| A1 | 0.00 | 0.035 | 0.05 | |
| A2 | - | 0.65 | 0.67 | |
| A3 | - | 0.203 | - | |
| b | 0.20 | 0.25 | 0.30 | |
| D | | 6.00 | | |
| E | | 6.00 | | |
| e | | 0.5 | | |
| D1 | 4.52 | 4.62 | 4.72 | |
| E1 | 4.52 | 4.62 | 4.72 | |
| F | 0.35 | 0.40 | 0.45 | |
| X | | TBD | | |
| Y | | TBD | | |
| **JEDEC** | MO-220 | | | |
| **Unit** | mm | | | |



**Figure 3.2: Package Dimensions**

## 3.4 PCB Design and Assembly Considerations

This section lists recommendations to achieve maximum board-level reliability of the 6 x 6 x 0.9mm 40-lead QFN package:

- NSMD lands (lands smaller than the solder mask aperture) are preferred because of the greater accuracy of the metal definition process compared to the solder mask process. With solder mask defined pads, the overlap of the solder mask on the land creates a step in the solder at the land interface, which can cause stress concentration and act as a point for crack initiation.
- PCB land width should be 0.3mm and PCB land length should be 0.8mm to achieve maximum reliability.
- Solder paste must be used during the assembly process.

# 4 Bluetooth Modem

## 4.1 RF Ports

### 4.1.1 RF_N and RF_P

RF_N and RF_P form a complementary balanced pair and are available for both transmit and receive. On transmit their outputs are combined using an external balun into the single-ended output required for the antenna. Similarly, on receive their input signals are combined internally.

Both terminals present similar complex impedances that may require matching networks between them and the balun. Viewed from the chip, the outputs can each be modelled as an ideal current source in parallel with a lossy capacitor. An equivalent series inductance can represent the package parasitics.

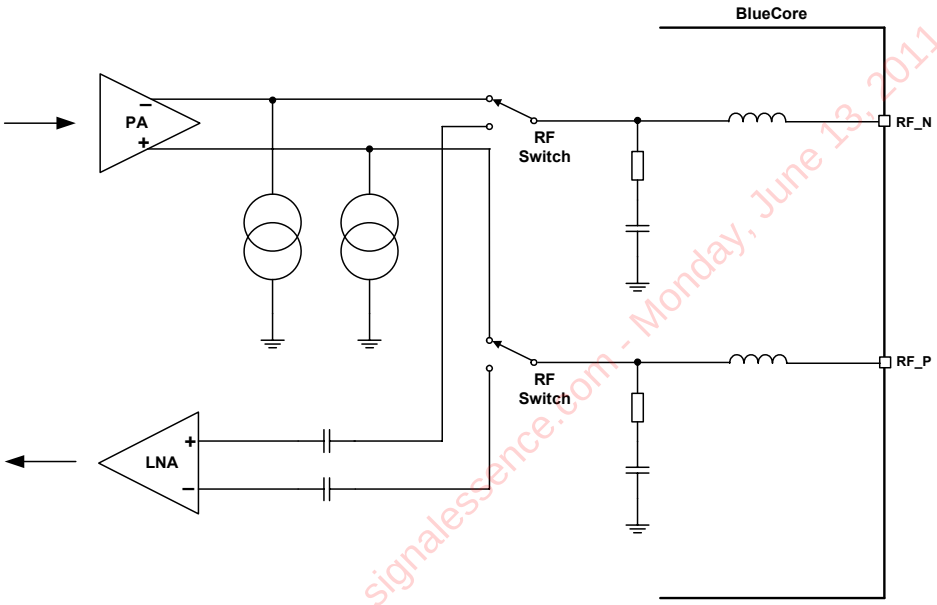



**Figure 4.1: Simplified Circuit RF_N and RF_P**

The DC level must be set at VDD_RADIO.

## 4.2 RF Receiver

The receiver features a near-zero IF architecture that allows the channel filters to be integrated onto the die. Sufficient out-of-band blocking specification at the LNA input allows the receiver to be used in close proximity to GSM and W-CDMA cellular phone transmitters without being desensitised. The use of a digital FSK discriminator means that no discriminator tank is needed and its excellent performance in the presence of noise allows BlueCore6-ROM QFN to exceed the Bluetooth requirements for co-channel and adjacent channel rejection.

For EDR, the demodulator contains an ADC which digitises the IF received signal. This information is then passed to the EDR modem.

### 4.2.1 Low Noise Amplifier

The LNA operates in differential mode and takes its input from the shared RF port.

### 4.2.2 RSSI Analogue to Digital Converter

The ADC implements fast AGC. The ADC samples the RSSI voltage on a slot-by-slot basis. The front-end LNA gain is changed according to the measured RSSI value, keeping the first mixer input signal within a limited range. This improves the dynamic range of the receiver, improving performance in interference limited environments.

## 4.3 RF Transmitter

### 4.3.1 IQ Modulator

The transmitter features a direct IQ modulator to minimise the frequency drift during a transmit timeslot, which results in a controlled modulation index. Digital baseband transmit circuitry provides the required spectral shaping.

### 4.3.2 Power Amplifier

The internal PA has a maximum output power of 9dBm. This allows BlueCore6-ROM QFN to be used in Class 2 and Class 3 Bluetooth radios without an external RF PA. Support for transmit power control allows a simple implementation for Class 1 with an external RF PA.

## 4.4 Bluetooth Radio Synthesiser

The Bluetooth radio synthesiser is fully integrated onto the die with no requirement for an external VCO screening can, varactor tuning diodes, LC resonators or loop filter. The synthesiser is guaranteed to lock in sufficient time across the guaranteed temperature range to meet the Bluetooth v2.1 + EDR specification.

## 4.5 Baseband

### 4.5.1 Burst Mode Controller

During transmission the BMC constructs a packet from header information previously loaded into memory-mapped registers by the software and payload data/voice taken from the appropriate ring buffer in the RAM. During reception, the BMC stores the packet header in memory-mapped registers and the payload data in the appropriate ring buffer in RAM. This architecture minimises the intervention required by the processor during transmission and reception.

### 4.5.2 Physical Layer Hardware Engine

Dedicated logic performs the following:

- Forward error correction
- Header error control
- Cyclic redundancy check
- Encryption
- Data whitening
- Access code correlation
- Audio transcoding

Firmware performs the following voice data translations and operations:

- A-law/μ-law/linear voice data (from host)
- A-law/μ-law/CVSD (over the air)
- Voice interpolation for lost packets
- Rate mismatches

The hardware supports all optional and mandatory features of Bluetooth v2.1 + EDR specification including AFH and eSCO.

## 4.6 AuriStream Codec

The AuriStream codec is an ADPCM codec and works on the principle of transmitting the difference between the actual value of the signal and a prediction rather than the signal itself. Therefore, the information transmitted is reduced along with the power requirement. The quality of the output depends on the number of bits used to represent the sample.

**Note:**

The use of the AuriStream codec is as follows:

- The AuriStream codec is an alternative to standard CVSD
- It requires CSR devices supporting AuriStream at both ends of the link
- AuriStream is negotiated when the link is brought up. If AuriStream is not supported on either end, the system will switch to standard CVSD ensuring full interoperability with any non-AuriStream Bluetooth devices

The inclusion of the AuriStream codec can greatly enhance audio quality in the wideband mode and results in reduced power consumption compared to a CVSD implementation when used at both ends of the system.

AuriStream supports the G726 mode of operation shown in Table 4.1.

| fs | Bit-rate (kbps) | | | | | | |
|---|---|---|---|---|---|---|---|
| | 16 | 20 | 24 | 32 | 48 | 64 | 80 |
| 8kHz | ✓ | | ✓ | ✓ | | | |
| 16kHz | | | | ✓ | ✓ | ✓ | ✓ |

**Table 4.1: AuriStream Supported Bit-rates for G726**

## 4.7 Basic Rate Modem

The basic rate modem satisfies the basic data rate requirements of the Bluetooth v2.1 + EDR specification. The basic rate was the standard data rate available on the Bluetooth v1.2 specification and below, it is based on GFSK modulation scheme.

The inclusion of the basic rate modem allows BlueCore6-ROM QFN compatibility with earlier Bluetooth products.

The basic rate modem uses the RF ports, receiver, transmitter and synthesiser, alongside the baseband components described in Section 4.5.

## 4.8 Enhanced Data Rate Modem

The EDR modem satisfies the requirements of the Bluetooth v2.1 + EDR specification. EDR has been introduced to provide 2x and 3x data rates with minimal disruption to higher layers of the Bluetooth stack. BlueCore6-ROM QFN supports both the basic and enhanced data rates and is compliant with the Bluetooth v2.1 + EDR specification.

At the baseband level, EDR utilises both the same 1.6kHz slot rate and the 1MHz symbol rate as defined for the basic data rate. EDR differs in that each symbol in the payload portion of a packet represents 2 or 3-bits. This is achieved using two new distinct modulation schemes. Table 4.2 and Figure 4.2 summarise these. Link Establishment and management are unchanged and still use GFSK for both the header and payload portions of these packets.

The enhanced data rate modems uses the RF Ports, Receiver, Transmitter and Synthesiser, with the baseband components described in Section 4.5.

| Data Rate Scheme | Bits Per Symbol | Modulation |
|---|---|---|
| Basic Data Rate | 1 | GFSK |
| EDR | 2 | π/4 DQPSK |
| EDR | 3 | 8DPSK (optional) |

**Table 4.2: Data Rate Schemes**

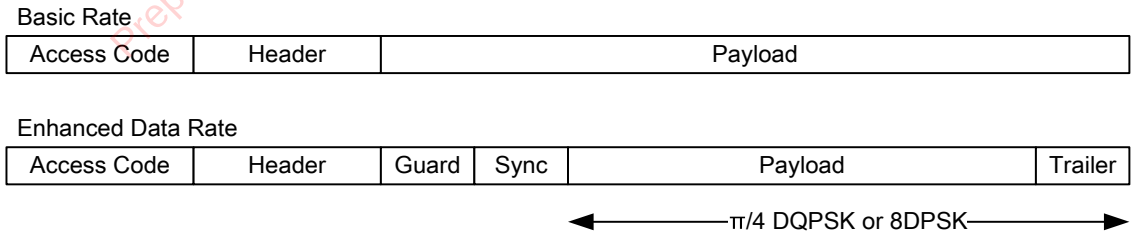



**Figure 4.2: Basic Rate and Enhanced Data Rate Packet Structure**

### 4.8.1 Enhanced Data Rate π/4 DQPSK

The 2x data rate for EDR uses a π/4-DQPSK. Each symbol represents 2-bits of information. Figure 4.3 shows the constellation. It has two planes, each having four points. Although it seems there are eight possible phase states, the encoding ensures that the trajectory of the modulation between symbols is restricted to the four states in the other plane.

For a given starting point, each phase change between symbols is restricted to +3π/4, +π/4, -π/4 or -3π/4 radians (+135°, +45°, -45° or -135°). For example, the arrows shown in Figure 4.3 represent trajectory to the four possible states in the other plane. Table 4.3 shows the phase shift encoding of symbols.

There are two main advantages in using π/4 DQPSK modulation:

- The scheme avoids the crossing of the origin (a +π or -π phase shift) and therefore minimises amplitude variations in the envelope of the transmitted signal. This in turn allows the RF power amplifiers of the transmitter to be operated closer to their compression point without introducing spectral distortions. Consequently, the DC to RF efficiency is maximised.
- The differential encoding also allows for the demodulation without the knowledge of an absolute value for the phase of the RF carrier.

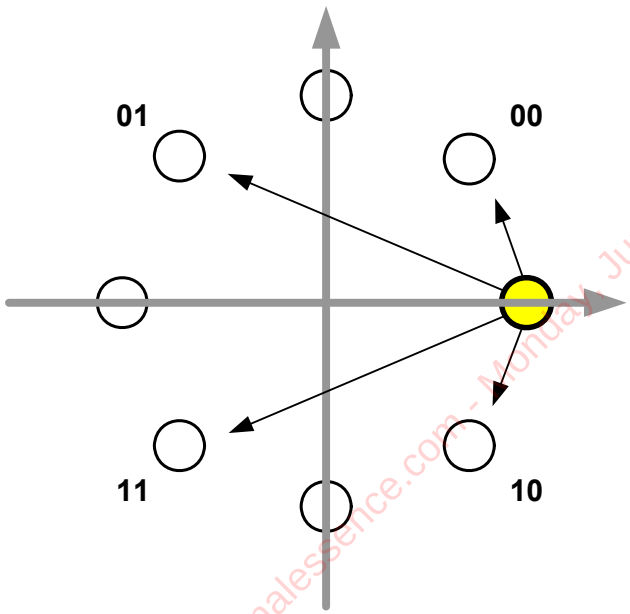



**Figure 4.3: π/4 DQPSK Constellation Pattern**

| Bit Pattern | Phase Shift |
|---|---|
| 00 | π/4 |
| 01 | 3π/4 |
| 11 | -3π/4 |
| 10 | -π/4 |

**Table 4.3: 2-Bits Determine Phase Shift Between Consecutive Symbols**

### 4.8.2 Enhanced Data Rate 8DPSK

The 3x data rate modulation uses 8DPSK. Each symbol in the payload portion of the packet represents 3 baseband bits. Although it seems the 8DPSK is similar to π/4 DQPSK, the differential phase shifts between symbols are now permissible between any of the eight possible phase states. This reduces the separation between adjacent symbols on the constellation to π/4 (45°) and thereby reduces the noise and interference immunity of the modulation scheme. Nevertheless, because each symbol now represents 3 baseband bits, the actual throughput of the data is 3x when compared with the basic rate packet.

Figure 4.4 shows the 8DPSK constellation and Table 4.4 shows the phase encoding.

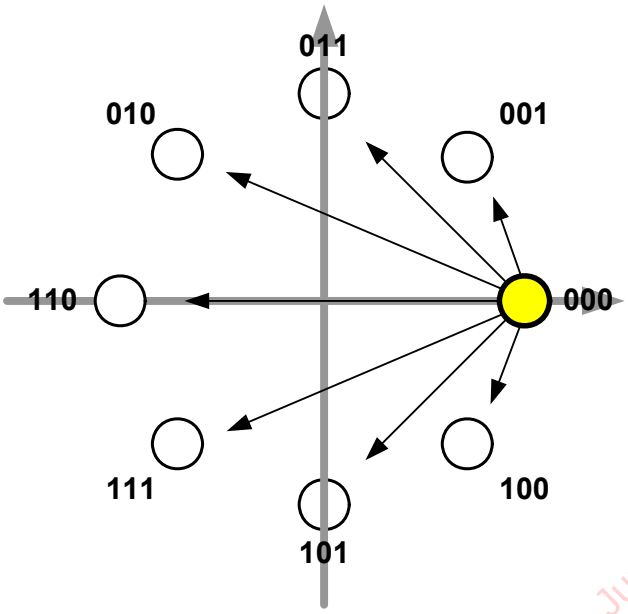



Figure 4.4: 8DPSK Constellation Pattern

| Bit Pattern | Phase Shift |
|---|---|
| 000 | 0 |
| 001 | π/4 |
| 011 | π/2 |
| 010 | 3π/4 |
| 110 | π |
| 111 | -3π/4 |
| 101 | -π/2 |
| 100 | -π/4 |

Table 4.4: 3-Bits Determine Phase Shift Between Consecutive Symbols

# 5 Clock Generation

BlueCore6-ROM QFN requires a Bluetooth reference clock. This can be an externally connected crystal, or an external TCXO source.

All BlueCore6-ROM QFN internal digital clocks are generated using a phase locked loop, which is locked to the frequency of the external reference clock source.

Also supplied to the digits is a watchdog clock, for use in low power modes. This uses a frequency of 32.768kHz from CLK_32K, or an internally generated reference clock frequency of 1kHz, determined by PSKEY_DEEP_SLEEP_EXTERNAL_CLOCK_SOURCE.

The use of the watchdog clock is determined with respect to Bluetooth operation in low power modes.

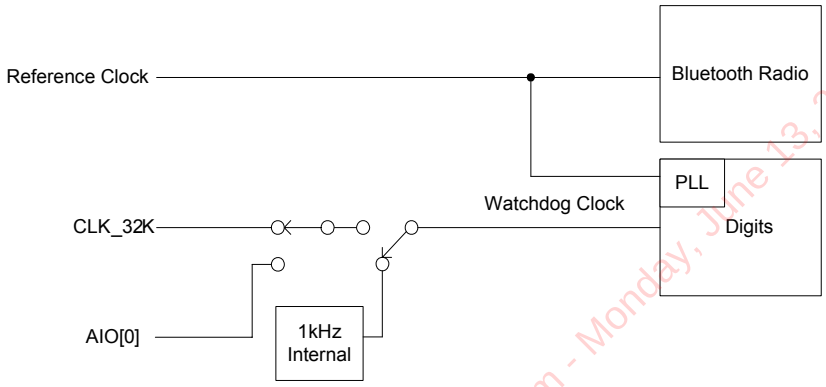



**Figure 5.1: Clock Architecture**

## 5.1 Input Frequencies and PS Key Settings

BlueCore6-ROM QFN should be configured to operate with the chosen reference frequency. Do this by setting the PS Key ANA_FREQ (0x01FE) for all frequencies with an integer multiple of 250kHz. The input frequency default setting in BlueCore6-ROM QFN is 26MHz depending on the software build. Full details are in the software release note for the specific build from www.csrsupport.com.

The following CDMA/3G phone TCXO frequencies are also catered for: 14.40, 15.36, 16.2, 16.8, 19.2, 19.44, 19.68, 19.8 and 38.4MHz. The value of the PS Key is a multiple of 1kHz, so 38.4MHz is selected by using a PS Key value of 38400.

| Reference Crystal Frequency (MHz) | ANA_FREQ (0x1fe) (kHz) |
|---|---|
| 14.40 | 14400 |
| 15.36 | 15360 |
| 16.20 | 16200 |
| 16.80 | 16800 |
| 19.20 | 19200 |

| Reference Crystal Frequency (MHz) | ANA_FREQ (0x1fe) (kHz) |
|---|---|
| 19.44 | 19440 |
| 19.68 | 19680 |
| 19.80 | 19800 |
| 38.40 | 38400 |
| n x 0.25 | n x 250 |
| 26.00 (default) | 26000 |

Table 5.1: PS Key Values for CDMA/3G Phone TCXO

## 5.2 Crystal Oscillator (XTAL_IN, XTAL_OUT)

BlueCore6-ROM QFN contains a crystal driver circuit. This operates with an external crystal and capacitors to form a Pierce oscillator. The external crystal is connected to pins XTAL_IN, XTAL_OUT.

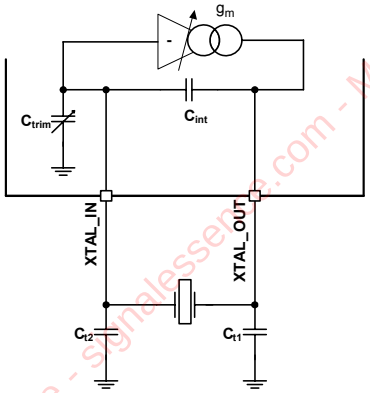



Figure 5.2: Crystal Driver Circuit

Figure 5.3 shows an electrical equivalent circuit for a crystal. The crystal appears inductive near its resonant frequency. It forms a resonant circuit with its load capacitors.

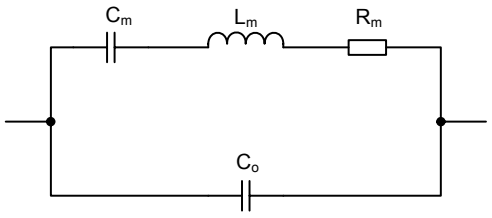



Figure 5.3: Crystal Equivalent Circuit

The resonant frequency may be trimmed with the crystal load capacitance. BlueCore6-ROM QFN contains variable internal capacitors to provide a fine trim.

| Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|
| Frequency | 16 | 26 | 26 | MHz |
| Initial Tolerance | - | ±25 | - | ppm |
| Pullability | - | ±20 | - | ppm/pF |
| Transconductance | 2.0 | - | - | mS |

**Table 5.2: Crystal Specification**

The BlueCore6-ROM QFN driver circuit is a transconductance amplifier. A voltage at XTAL_IN generates a current at XTAL_OUT. The value of transconductance is variable and may be set for optimum performance.

### 5.2.1 Load Capacitance

For resonance at the correct frequency the crystal should be loaded with its specified load capacitance, which is defined for the crystal. This is the total capacitance across the crystal viewed from its terminals. BlueCore6-ROM QFN provides some of this load with the capacitors $C_{trim}$ and $C_{int}$. The remainder should be from the external capacitors labelled $C_{t1}$ and $C_{t2}$. $C_{t1}$ should be three times the value of $C_{t2}$ for best noise performance. This maximises the signal swing, hence slew rate at XTAL_IN (to which all on-chip clocks are referred).

Crystal load capacitance, $C_l$ is calculated with Equation 5.1:

$$C_l = C_{int} + \frac{(C_{t2} + C_{trim})C_{t1}}{C_{t2} + C_{trim} + C_{t1}}$$

**Equation 5.1: Load Capacitance**

**Note:**

$C_{trim}$ = 3.4pF nominal (mid-range setting)

$C_{int}$ = 1.5pF

$C_{int}$ does not include the crystal internal self capacitance; it is the driver self capacitance.

### 5.2.2 Frequency Trim

BlueCore6-ROM QFN enables frequency adjustments to be made. This feature is typically used to remove initial tolerance frequency errors associated with the crystal. Frequency trim is achieved by adjusting the crystal load capacitance with an on-chip trim capacitor, $C_{trim}$. The value of $C_{trim}$ is set by a 6-bit word in the PS Key ANA_FTRIM (`0x1f6`). Its value is calculated as follows:

$$C_{trim} = 125fF \times PSKEY\_ANA\_FTRIM$$

**Equation 5.2: Trim Capacitance**

The $C_{trim}$ capacitor is connected between XTAL_IN and ground. When viewed from the crystal terminals, the combination of the tank capacitors and the trim capacitor presents a load across the terminals of the crystal which varies in steps of typically 125fF for each least significant bit increment of ANA_FTRIM.

Equation 5.3 describes the frequency trim.

$$\frac{\Delta(F_x)}{F_x} = pullability \times 0.110 \times \left(\frac{C_{t1}}{C_{t1} + C_{t2} + C_{trim}}\right) (ppm / LSB)$$

**Equation 5.3: Frequency Trim**

**Note:**

$F_x$ = crystal frequency

Pullability is a crystal parameter with units of ppm/pF.

Total trim range is 0 to 63.

If not specified, the pullability of a crystal may be calculated from its motional capacitance with Equation 5.4.

$$\frac{\partial(F_X)}{\partial(C_l)} = F_X \cdot \frac{C_m}{2(C_l + C_0)^2}$$

**Equation 5.4: Pullability**

**Note:**

$C_0$ = Crystal self capacitance (shunt capacitance)

$C_m$ = Crystal motional capacitance (series branch capacitance in crystal model). See Figure 5.3.

It is a Bluetooth requirement that the frequency is always within ±20ppm. The trim range should be sufficient to pull the crystal within ±5ppm of the exact frequency. This leaves a margin of ±15ppm for frequency drift with ageing and temperature. A crystal with an ageing and temperature drift specification of better than ±15ppm is required.

### 5.2.3 Transconductance Driver Model

The crystal and its load capacitors should be viewed as a transimpedance element, whereby a current applied to one terminal generates a voltage at the other. The transconductance amplifier in BlueCore6-ROM QFN uses the voltage at its input, XTAL_IN, to generate a current at its output, XTAL_OUT. Therefore, the circuit will oscillate if the transconductance, transimpedance product is greater than unity. For sufficient oscillation amplitude, the product should be greater than three. The transconductance required for oscillation is defined by the relationship shown in Equation 5.5.

$$g_m > 3\,\frac{(2\pi F_x)^2 R_m \left((C_0 + C_{int})(C_{t1} + C_{t2} + C_{trim}) + C_{t1}(C_{t2} + C_{trim})\right)}{C_{t1}(C_{t2} + C_{trim})}$$

**Equation 5.5: Transconductance Required for Oscillation**

BlueCore6-ROM QFN guarantees a transconductance value of at least 2mA/V at maximum drive level.

**Note:**

More drive strength is required for higher frequency crystals, higher loss crystals (larger $R_m$) or higher capacitance loading.

Optimum drive level is attained when the level at XTAL_IN is approximately 1V pk-pk. The drive level is determined by the crystal driver transconductance.

### 5.2.4 Negative Resistance Model

An alternative representation of the crystal and its load capacitors is a frequency dependent resistive element. The driver amplifier may be considered as a circuit that provides negative resistance. For oscillation, the value of the negative resistance must be greater than that of the crystal circuit equivalent resistance. Although the BlueCore6-ROM QFN crystal driver circuit is based on a transimpedance amplifier, an equivalent negative resistance can be calculated for it using Equation 5.6.

$$R_{neg} > \frac{C_{t1}(C_{t2} + C_{trim})}{g_m (2\pi F_x)^2 (C_0 + C_{int})\left((C_{t1} + C_{t2} + C_{trim}) + C_{t1}(C_{t2} + C_{trim})\right)^2}$$

**Equation 5.6: Equivalent Negative Resistance**

This formula shows the negative resistance of the BlueCore6-ROM QFN driver as a function of its drive strength.

The value of the driver negative resistance may be easily measured by placing an additional resistance in series with the crystal. The maximum value of this resistor (oscillation occurs) is the equivalent negative resistance of the oscillator.

### 5.2.5 Crystal PS Key Settings

The BlueCore6-ROM QFN firmware automatically controls the drive level on the crystal circuit to achieve optimum input swing. The PS Key PSKEY_XTAL_TARGET_AMPLITUDE (`0x24b`) is used by the firmware to servo the required amplitude of crystal oscillation. Refer to the software build release note for a detailed description.

BlueCore6-ROM QFN should be configured to operate with the chosen reference frequency.

## 5.3 32kHz External Reference Clock

A 32kHz clock can be applied to either AIO[0] or CLK_32K, using PSKEY_DEEP_SLEEP_EXTERNAL_CLOCK_SOURCE.

If the external clock is applied to the analogue pad AIO[0] in the VDD_ANA domain, the digital signal should be driven with a maximum 1.5V. The CLK_32K pad is in the VDD_PADS domain with all the other digital I/O pads and is driven between levels specified in Section 13.4.7.

**Note:**

If the 32kHz clock is accurate and stable to within 200ppm, then further power saving features can be enabled. See the relevant software release note for more information.

## 5.4 Clock Start-up Delay

BlueCore6-ROM QFN hardware incorporates an automatic 5ms delay after the assertion of the system clock request signal before running firmware. This is suitable for most applications using an external clock source. However, there may be scenarios where the clock cannot be guaranteed to either exist or be stable after this period. Under these conditions, BlueCore6-ROM QFN firmware provides a software function that extends the system clock request signal by a period stored in PSKEY_CLOCK_STARTUP_DELAY. This value is set in milliseconds from 1-31ms. Zero is the default entry for 5ms delay.

This PS Key allows the designer to optimise a system where clock latencies may be longer than 5ms while still keeping the current consumption of BlueCore6-ROM QFN as low as possible. BlueCore6-ROM QFN consumes about 2mA of current for the duration of PSKEY_CLOCK_STARTUP_DELAY before activating the firmware.

# 6 Bluetooth Stack Microcontroller

The MCU, interrupt controller and event timer run the Bluetooth software stack and control the Bluetooth radio and host interfaces. A 16-bit RISC microcontroller is used for low power consumption and efficient use of memory.

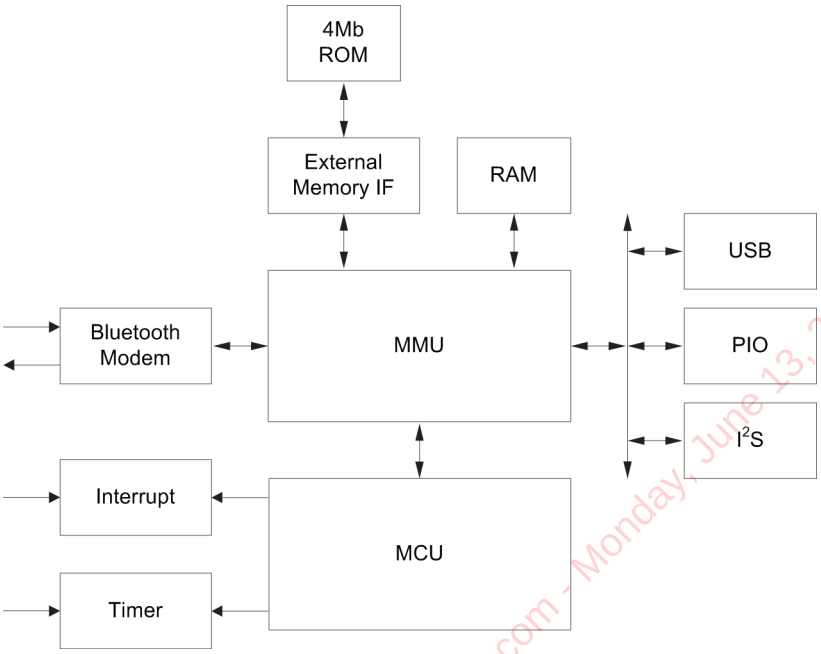



**Figure 6.1: Baseband Digits Block Diagram**

## 6.1 Configurable I/O Parallel Ports

7 lines of programmable bi-directional *input/outputs* (I/O) are provided. PIO[1:5, 7, 9] are powered from VDD_PADS. AIO[0] is powered from VDD_ANA.

PIO lines can be configured through software to have either weak or strong pull-ups or pull-downs. All PIO lines are conFigured as inputs with weak pull-downs at reset.

Any of the PIO lines can be configured as interrupt request lines or as wake-up lines from sleep modes. PIO[2] can be configured as a request line for an external clock source. Using `PSKEY_CLOCK_REQUEST_ENABLE` (`0x246`), this terminal can be configured to be low when BlueCore6-ROM QFN is in Deep Sleep and high when a clock is required. See also Section 6.2.

**Note:**

CSR cannot guarantee that the PIO assignments remain as described. Refer to the relevant software release note for the implementation of these PIO lines, as they are firmware build-specific.

## 6.2 TCXO Enable OR Function

An OR function exists for clock enable signals from a host controller and BlueCore6-ROM QFN where either device can turn on the clock without having to wake up the other device, see Figure 6.2. PIO[3] can be used as the host clock enable input and PIO[2] can be used as the OR output with the TCXO enable signal from BlueCore6-ROM QFN.

**Note:**

To turn on the clock, the clock enable signal on PIO[3] must be high.

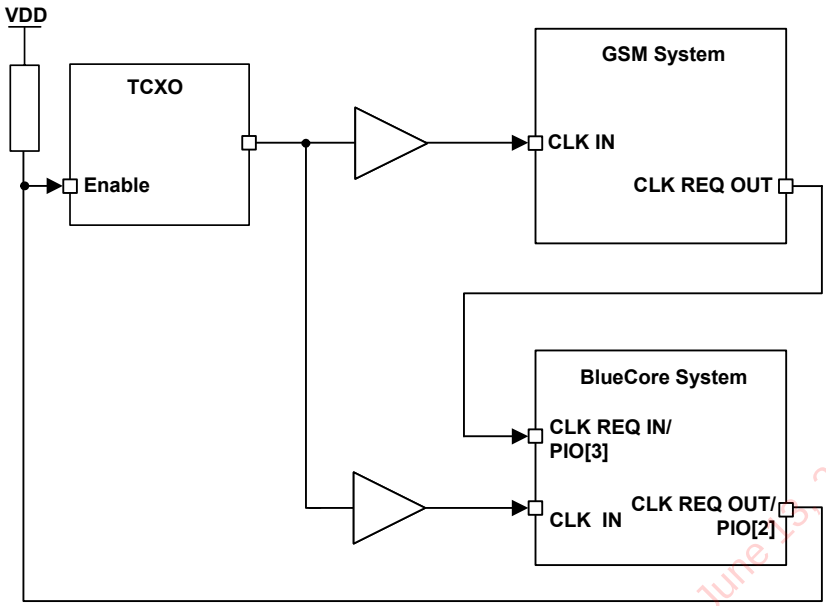



Figure 6.2: Example TCXO Enable OR Function

On reset and up to the time the PIO has been configured, PIO[2] is tri-state. Therefore, the developer must ensure that the circuitry connected to this pin is pulled via a 470kΩ resistor to the appropriate power rail. This ensures that the TCXO is oscillating at start up.

## 6.3 WLAN Coexistence Interface

Dedicated hardware is provided to implement a variety of coexistence schemes. Channel skipping AFH, priority signalling, channel signalling and host passing of channel instructions are all supported. The features are configured in firmware using PS Keys or via the host.

For more information see *CSR Bluetooth Coexistence Implementations*.

# 7 Memory Interface and Management

## 7.1 Memory Management Unit

The MMU provides a number of dynamically allocated ring buffers that hold the data that is in transit between the host, the air or the Kalimba DSP. The dynamic allocation of memory ensures efficient use of the available RAM and is performed by a hardware MMU to minimise the overheads on the processor during data/voice transfers.

## 7.2 System RAM

48KB of on-chip RAM supports the RISC MCU and is shared between the ring buffers used to hold voice/data for each active connection and the general-purpose memory required by the Bluetooth stack.

## 7.3 Internal ROM

4Mb of internal ROMis provided on the BlueCore6-ROM QFN. This memory is provided for system firmware and the Kalimba DSP co-processor code implementation.

# 8 Serial Interfaces

## 8.1 Serial Peripheral Interface

The primary function of the SPI is for debug. BlueCore6-ROM QFN uses a 16-bit data and 16-bit address SPI, where transactions may occur when the internal processor is running or is stopped. This section details the interface considerations for connection to BlueCore6-ROM QFN .

Data may be written or read one word at a time, or the auto-increment feature is available for block access.

### 8.1.1 Instruction Cycle

The BlueCore6-ROM QFN is the slave and receives commands on SPI_MOSI and outputs data on SPI_MISO. Table 8.1 shows the instruction cycle for an SPI transaction.

| | | |
|---|---|---|
| 1 | Reset the SPI interface | Hold SPI_CS# high for two SPI_CLK cycles |
| 2 | Write the command word | Take SPI_CS# low and clock in the 8-bit command |
| 3 | Write the address | Clock in the 16-bit address word |
| 4 | Write or read data words | Clock in or out 16-bit data word(s) |
| 5 | Termination | Take SPI_CS# high |

**Table 8.1: Instruction Cycle for an SPI Transaction**

With the exception of reset, SPI_CS# must be held low during the transaction. Data on SPI_MOSI is clocked into the BlueCore6-ROM QFN on the rising edge of the clock line SPI_CLK. When reading, BlueCore6-ROM QFN replies to the master on SPI_MISO with the data changing on the falling edge of the SPI_CLK. The master provides the clock on SPI_CLK. The transaction is terminated by taking SPI_CS# high.

Sending a command word and the address of a register for every time it is to be read or written is a significant overhead, especially when large amounts of data are to be transferred. To overcome this BlueCore6-ROM QFN offers increased data transfer efficiency via an auto increment operation. To invoke auto increment, SPI_CS# is kept low, which auto increments the address, while providing an extra 16 clock cycles for each extra word to be written or read.

### 8.1.2 Writing to the Device

To write to BlueCore6-ROM QFN, the 8-bit write command (00000010) is sent first (C[7:0]) followed by a 16-bit address (A[15:0]). The next 16-bits (D[15:0]) clocked in on SPI_MOSI are written to the location set by the address (A). Thereafter for each subsequent 16-bits clocked in, the address (A) is incremented and the data written to consecutive locations until the transaction terminates when SPI_CS# is taken high.

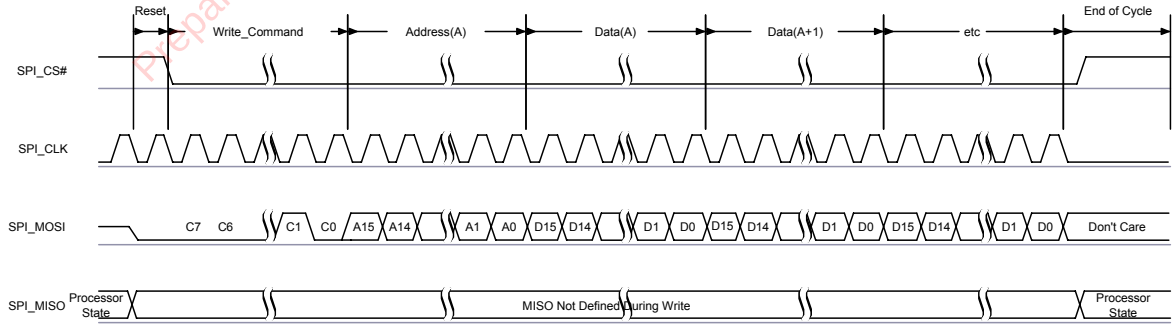



**Figure 8.1: SPI Write Operation**

### 8.1.3 Reading from the Device

Reading from BlueCore6-ROM QFN is similar to writing to it. An 8-bit read command (00000011) is sent first (C[7:0]), followed by the address of the location to be read (A[15:0]). BlueCore6-ROM QFN then outputs on SPI_MISO a check word during T[15:0] followed by the 16-bit contents of the addressed location during bits D[15:0].

The check word is composed of {command, address [15:8]}. The check word may be used to confirm a read operation to a memory location. This overcomes the problems encountered with typical serial peripheral interface slaves, whereby it is impossible to determine whether the data returned by a read operation is valid data or the result of the slave device not responding.

If SPI_CS# is kept low, data from consecutive locations is read out on SPI_MISO for each subsequent 16 clocks, until the transaction terminates when SPI_CS# is taken high.

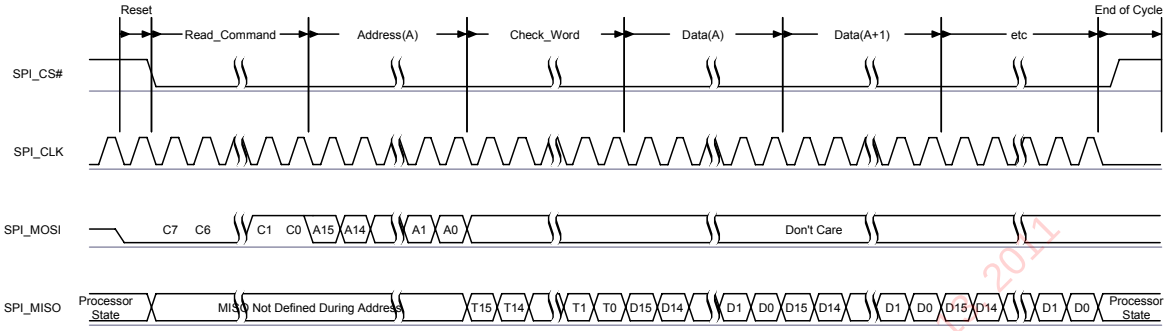



**Figure 8.2: SPI Read Operation**

### 8.1.4 Multi-slave Operation

BlueCore6-ROM QFN should not be connected in a multi-slave arrangement by simple parallel connection of slave MISO lines. When BlueCore6-ROM QFN is deselected (SPI_CS# = 1), the SPI_MISO line does not float. Instead, BlueCore6-ROM QFN outputs 0 if the processor is running or 1 if it is stopped.

# 9 Host Interfaces

## 9.1 Host Selection

BlueCore6-ROM QFN switches between UART and SDIO transport at boot-up by reading the status of PIO[4]:

- PIO[4] = pulled low: UART mode is selected (Casira default setting).
- PIO[4] = driven high: SDIO or CSPI host interface is selected.

The protocol used by the UART host interface is determined by the status of the SDIO_CLK and SDIO_CMD lines at the time PIO[4] is sampled. Table 9.1 lists the different protocols available along with the required configuration of CLK and CMD for each one.

To select a different UART Protocol, connect external 100kΩ pull-up and/or pull-down resistors as appropriate.

For example:

- To select BCSP, connect 100kΩ pull-downs to both SDIO_CLK and SDIO_CMD.
- To select H4DS, connect a 100kΩ pull-up to SDIO_CLK and a 100kΩ pull-down to SDIO_CMD.

| CLK | CMD | UART Protocol |
|---|---|---|
| 0 | 0 | BCSP |
| 0 | 1 | H4 |
| 1 | 0 | H4DS |
| 1 | 1 | H5 |

**Table 9.1: UART Protocol Selection**

## 9.2 UART Interface

BlueCore6-ROM QFN has a standard UART serial interface that provides a simple mechanism for communicating using RS232 protocol.

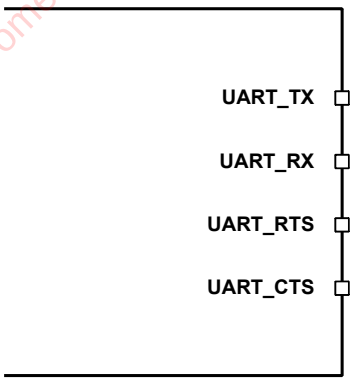



**Figure 9.1: Universal Asynchronous Receiver**

Figure 9.1 shwos the 4 signals that implement the UART function. When BlueCore6-ROM QFN is connected to another digital device, UART_RX and UART_TX transfer data between the 2 devices. The remaining 2 signals, UART_CTS and UART_RTS, can implement RS232 hardware flow control where both are active low indicators.

UART configuration parameters, such as baud rate and packet format, are set using BlueCore6-ROM QFN firmware.

**Note:**

To communicate with the UART at its maximum data rate using a standard PC, an accelerated serial port adapter card is required for the PC.

| Parameter | | Possible Values |
|---|---|---|
| Baud rate | Minimum | 1200 baud (≤2%Error) |
| | | 9600 baud (≤1%Error) |
| | Maximum | 4Mbaud (≤1%Error) |
| Flow control | | RTS/CTS or None |
| Parity | | None, Odd or Even |
| Number of stop bits | | 1 or 2 |
| Bits per byte | | 8 |

**Table 9.2: Possible UART Settings**

The UART interface can reset BlueCore6-ROM QFN on reception of a break signal. A break is identified by a continuous logic low (0V) on the UART_RX terminal, as shown in Figure 9.2. If $t_{BRK}$ is longer than the value, defined by the PS Key PSKEY_HOSTIO_UART_RESET_TIMEOUT, (0x1a4), a reset occurs. This feature allows a host to initialise the system to a known state. Also, BlueCore6-ROM QFN can emit a break character that may be used to wake the host.

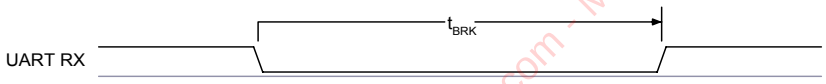



**Figure 9.2: Break Signal**

Table 9.3 shows a list of commonly used baud rates and their associated values for the PS Key PSKEY_UART_BAUDRATE (0x1be). There is no requirement to use these standard values. Any baud rate within the supported range can be set in the PS Key according to the formula in Equation 9.1.

$$\text{Baud Rate} = \frac{\text{PSKEY\_UART\_BAUDRATE}}{0.004096}$$

**Equation 9.1: Baud Rate**

| Baud Rate | Persistent Store Value | | Error |
|---|---|---|---|
| | Hex | Dec | |
| 1200 | 0x0005 | 5 | 1.73% |
| 2400 | 0x000a | 10 | 1.73% |
| 4800 | 0x0014 | 20 | 1.73% |
| 9600 | 0x0027 | 39 | -0.82% |
| 19200 | 0x004f | 79 | 0.45% |
| 38400 | 0x009d | 157 | -0.18% |
| 57600 | 0x00ec | 236 | 0.03% |
| 76800 | 0x013b | 315 | 0.14% |
| 115200 | 0x01d8 | 472 | 0.03% |

| Baud Rate | Persistent Store Value | | Error |
|---|---|---|---|
| | Hex | Dec | |
| 230400 | 0x03b0 | 944 | 0.03% |
| 460800 | 0x075f | 1887 | -0.02% |
| 921600 | 0x0ebf | 3775 | 0.00% |
| 1382400 | 0x161e | 5662 | -0.01% |
| 1843200 | 0x1d7e | 7550 | 0.00% |
| 2764800 | 0x2c3d | 11325 | 0.00% |
| 3686400 | 0x3afb | 15099 | 0.00% |

**Table 9.3: Standard Baud Rates**

### 9.2.1 UART Configuration While Reset is Active

The UART interface for BlueCore6-ROM QFN is tri-state while the chip is being held in reset. This allows the user to daisy chain devices onto the physical UART bus. The constraint on this method is that any devices connected to this bus must tri-state when BlueCore6-ROM QFN reset is de-asserted and the firmware begins to run.

## 9.3 CSR Serial Peripheral Interface

The CSPI is a host interface which shares pins with the SDIO. It has been defined by CSR with the intention of producing a very simple interface. This has two advantages:

- It allows maximum compatibility with the possible host drivers
- It minimises the host software effort needed to form the data to be sent by, for example, removing the need to calculate CRCs

This host interface allows an external host to control the , using a proprietary defined protocol built upon a 4-wire SPI bus.

CSPI allows access to the following:

- Function 0 registers
- Bluetooth Acceleration Registers
- MCU I/O Registers
- Bluetooth MMU port

The CSPI is a third protocol available for the host to transfer data into the and shares pins with the other SDIO protocols.

MMU buffers are accessed using burst read/writes. The command and address fields are used to select the correct buffer. The CSPI is able to generate an interrupt to the host when a memory access fails. This interrupt line is shared with the SDIO functions.

Table 9.4 shows the mapping of SDIO pins onto the CSPI functions when CSPI is enabled.

| CSPI Function | Pin | Direction | Description |
|---|---|---|---|
| MISO | SDIO_DATA[0] | Output | Master In Slave Out |
| INT | SDIO_DATA[1] | Output | Interrupt |
| CSB | SDIO_DATA[3] | Input | Chip Select |
| MOSI | SDIO_CMD | Input | Master Out Slave In |
| CLK | SDIO_CLK | Input | Clock |

**Table 9.4: SDIO Mapping to CSPI Functions**

The CSPI Interface is an extension of the basic SPI Interface, with the access type determined by the following fields:

- 8-bit command (to initiate CSPI read/write access)
- 24-bit address
- 16-bit burst length (optional). Only applicable for burst transfers into or out of the MMU

### 9.3.1 CSPI Read/Write Cycles

Register read/write cycles are used to access Function 0, Bluetooth acceleration and MCU registers.

Burst read/write cycles are used to access the MMU.

### 9.3.2 CSPI Register Write Cycle

The command and address are locked into the slave, followed by 16bits of write data. An Error Byte is returned on the MISO signal indicating whether or not the transfer has been successful.

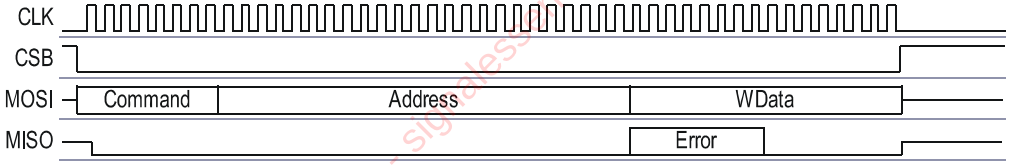



**Figure 9.3: CSPI Register Write Cycle**

### 9.3.3 CSPI Register Read Cycle

The command and address field are clocked into the slave, the slave then returns the following:

- Bytes of Padding data (MISO held low)
- Error Byte
- 16-bits of read data

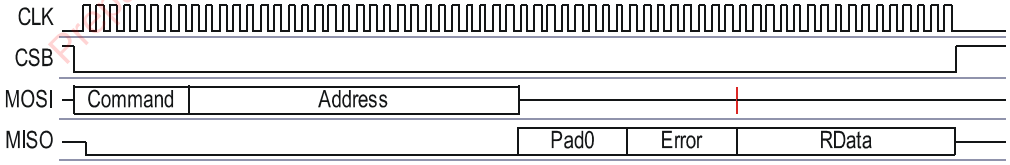



**Figure 9.4: CSPI Register Read Cycle**

### 9.3.4 CSPI Burst Write Cycle

Burst transfers are used to access the MMU buffers. They cannot be used to access registers. Burst read/write cycles are selected by setting the `nRegister/Burst` bit in the command field to `1`.

Burst transfers are byte orientated, have a minimum length of 0 bytes and a maximum length of 64Kbytes. Setting the length field to `0` results in no data being transferred to or from the MMU.

As with a register access, the command and address fields are transferred first. There is an optional length field transferred after the address. The use of the length field is controlled by the LengthFieldPresent bit in the Function 0 registers, which is cleared on reset.

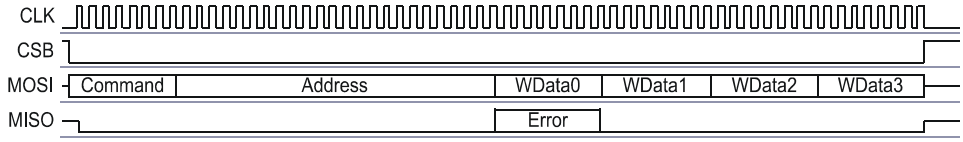



**Figure 9.5: CSPI Burst Write Cycle**

### 9.3.5 CSPI Burst Read Cycle

Burst reads have a programmable amount of padding data that is returned by the slave. 0-15 bytes are returned as defined in the BurstPadding register. Following this the Error byte is returned followed by the data. Once the transfer has started, no further padding is needed.

A FIFO within SDIO_TOP will pre-fetch the data. The address is not retransmitted, and is auto-updated within the slave.

The length field is transmitted if LengthFieldPresent in the Function 0 registers is set. In the absence of a length field the CSB signal is used to indicate the end of the burst.

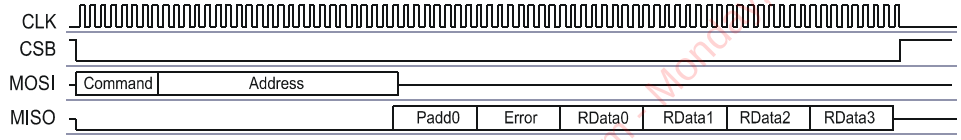



**Figure 9.6: CSPI Burst Read Cycle**

## 9.4 SDIO Interface

This is a host interface which allows a SDIO host to gain access to the internals of the chip. It provides all defined slave modes (SPI, SD 1bit, SD 4bit), but not SD host function.

The function provided includes generating responses to each command in hardware and implementing the state machines defined in the SDIO specification. Within the various modes of operation, it provides initialisation functions (cmds 0,3,5,7,15,59) and two other functions:

- Function 1 provides Bluetooth type A support, and follows that specification
- Function 2 provides generic register access (cmd52 (byte read/write))

For more information, see the following specifications:

- *SD Specifications Part 1 Physical layer specification v1.10*
- *SD Specifications Part E1 SDIO specification v1.10*
- *SDIO Card Part E2 Type-A Specification for Bluetooth v1.00*

### 9.4.1 SDIO/CSPI Deep Sleep Control Schemes

This is the lowest power mode, where the processor, the internal reference (fast) clock, and much of the digital and analogue hardware are shut down. To support this power consumption reduction solution and to prevent any errors arising on the SDIO host interface there are two deep sleep control schemes.

1. The host retransmits any packets that was unable to receive as a result of being in deep sleep.
2. Introduces additional signaling to prevent the need for retransmissions

During deep sleep the internal reference clock is turned off. However, the host transport protocols (SDIO/UART/ CSPI) are driven from the SDIO clock and so continue to function during deep sleep, enabling access to the function 0 interface, but not the function 1 interface.

### 9.4.2 Retransmission

Bluecore enters Deep-Sleep whenever it becomes idle after which time, when the host transmits a message on function 1 an illegal command error will be signaled. The activity that this initiates on the SDIO Interface provokes Bluecore into wakeup after which the host re-transmits the original message.

Bluecore will wait for a configurable period of time before re-entering Deep-Sleep, thus ensuring that the original packet is sent/received on retransmission. This control scheme is the default mode of operation.

### 9.4.3 Signalling

Signalling between the host and enables host control over deep sleep mode. Consequently the host is aware of when it is appropriate to send HCI traffic over function 1.

The signals used by this scheme are `HOST WAKEUP` and `READY STATUS INTERRUPT SELECT`, implemented as register bits in the vendor-unique area of function 0.

# 10 Audio Interfaces

## 10.1 PCM Interface

The audio PCM interface supports continuous transmission and reception of PCM encoded audio data over Bluetooth.

PCM is a standard method used to digitise audio (particularly voice) for transmission over digital communication channels. Through its PCM interface, BlueCore6-ROM QFN has hardware support for continual transmission and reception of PCM data, thus reducing processor overhead for wireless headset applications. BlueCore6-ROM QFN offers a bi-directional digital audio interface that routes directly into the baseband layer of the on-chip firmware. It does not pass through the HCI protocol layer.

Hardware on BlueCore6-ROM QFN allows the data to be sent to and received from a SCO connection.

Up to three SCO connections can be supported by the PCM interface at any one time.

BlueCore6-ROM QFN can operate as the PCM interface master generating an output clock of 128, 256, 512, 1536 or 2400kHz. When configured as a PCM interface slave, it can operate with an input clock up to 2400kHz. BlueCore6-ROM QFN is compatible with a variety of clock formats, including Long Frame Sync, Short Frame Sync and GCI timing environments.

It supports 13-bit or 16-bit linear, 8-bit µ-law or A-law companded sample formats at 8ksamples/s and can receive and transmit on any selection of three of the first four slots following PCM_SYNC. The PCM configuration options are enabled by setting `PSKEY_PCM_CONFIG32` (`0x1b3`).

BlueCore6-ROM QFN interfaces directly to PCM audio devices including the following:

- Qualcomm MSM 3000 series and MSM 5000 series CDMA baseband devices
- OKI MSM7705 four channel A-law and µ-law codec
- Motorola MC145481 8-bit A-law and µ-law codec
- Motorola MC145483 13-bit linear codec
- STW 5093 and 5094 14-bit linear codecs
- BlueCore6-ROM QFN is also compatible with the Motorola SSI interface

### 10.1.1 PCM Interface Master/Slave

When configured as the master of the PCM interface, BlueCore6-ROM QFN generates PCM_CLK and PCM_SYNC.

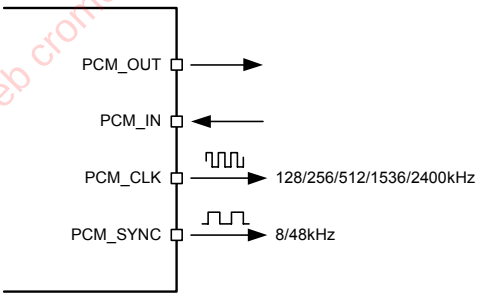



**Figure 10.1: PCM Interface Master**

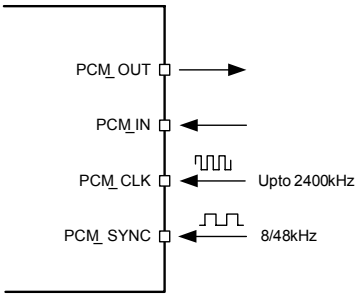



**Figure 10.2: PCM Interface Slave**

### 10.1.2 Long Frame Sync

Long Frame Sync is the name given to a clocking format that controls the transfer of PCM data words or samples. In Long Frame Sync, the rising edge of PCM_SYNC indicates the start of the PCM word. When BlueCore6-ROM QFN is configured as PCM master, generating PCM_SYNC and PCM_CLK, then PCM_SYNC is 8-bits long. When BlueCore6-ROM QFN is configured as PCM Slave, PCM_SYNC may be from two consecutive falling edges of PCM_CLK to half the PCM_SYNC rate, i.e. 62.5µs long.

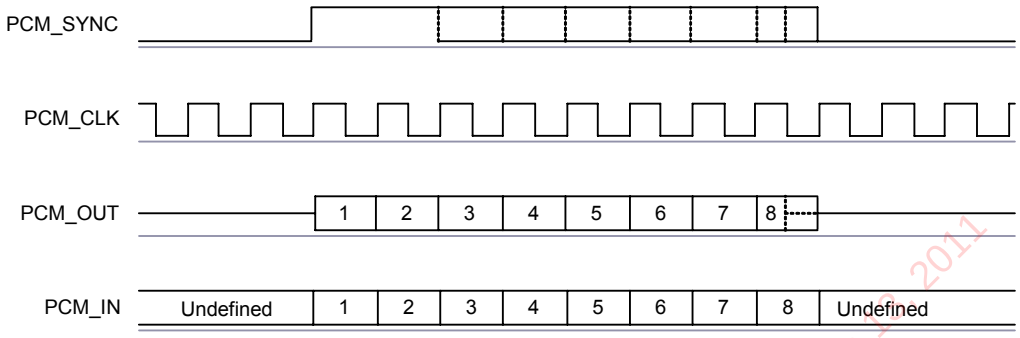



**Figure 10.3: Long Frame Sync (Shown with 8-bit Companded Sample)**

BlueCore6-ROM QFN samples PCM_IN on the falling edge of PCM_CLK and transmits PCM_OUT on the rising edge. PCM_OUT may be configured to be high impedance on the falling edge of PCM_CLK in the LSB position or on the rising edge.

### 10.1.3 Short Frame Sync

In Short Frame Sync, the falling edge of PCM_SYNC indicates the start of the PCM word. PCM_SYNC is always one clock cycle long.

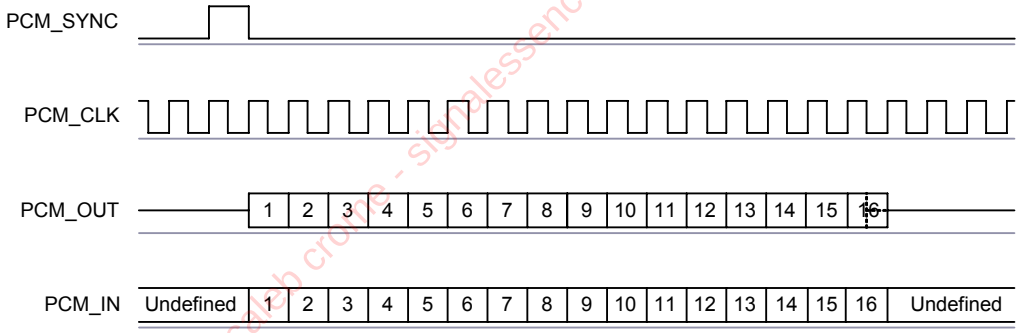



**Figure 10.4: Short Frame Sync (Shown with 16-bit Sample)**

As with Long Frame Sync, BlueCore6-ROM QFN samples PCM_IN on the falling edge of PCM_CLK and transmits PCM_OUT on the rising edge. PCM_OUT may be configured to be high impedance on the falling edge of PCM_CLK in the LSB position or on the rising edge.

### 10.1.4 Multi-slot Operation

More than one SCO connection over the PCM interface is supported using multiple slots. Up to three SCO connections can be carried over any of the first four slots.

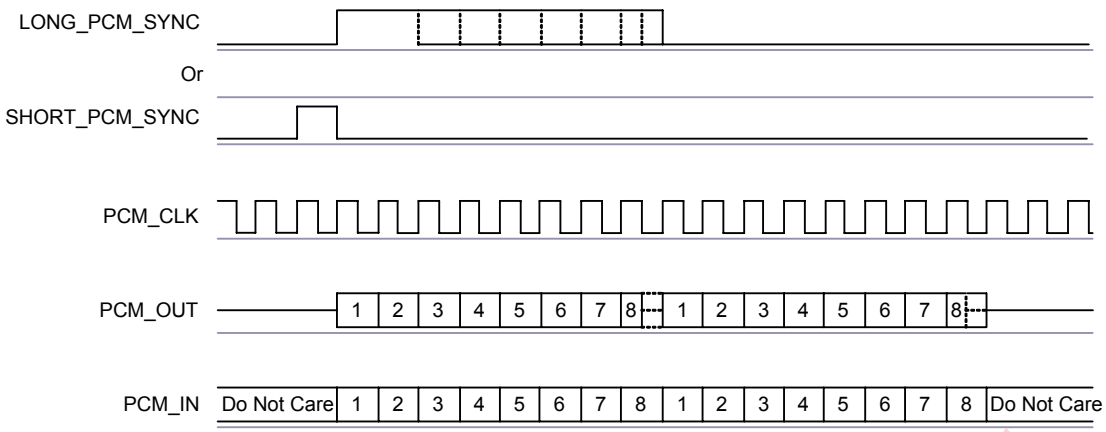



**Figure 10.5: Multi-slot Operation with Two Slots and 8-bit Companded Samples**

### 10.1.5 GCI Interface

BlueCore6-ROM QFN is compatible with the GCI, a standard synchronous 2B+D ISDN timing interface. The two 64kbps B channels can be accessed when this mode is configured.

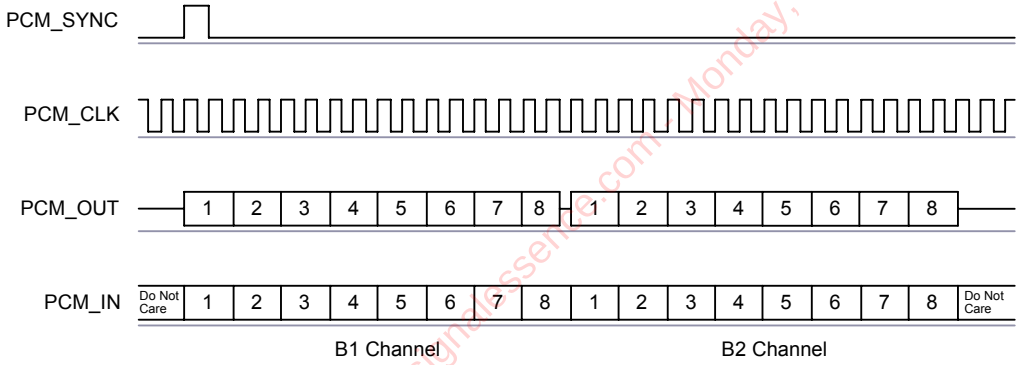



**Figure 10.6: GCI Interface**

The start of frame is indicated by the rising edge of PCM_SYNC and runs at 8kHz. With BlueCore6-ROM QFN in Slave mode, the frequency of PCM_CLK can be up to 4.096MHz

### 10.1.6 Slots and Sample Formats

BlueCore6-ROM QFN can receive and transmit on any selection of the first four slots following each sync pulse. Slot durations can be either 8 or 16 clock cycles. Durations of 8 clock cycles may only be used with 8-bit sample formats. Durations of 16 clocks may be used with 8-bit, 13-bit or 16-bit sample formats.

BlueCore6-ROM QFN supports 13-bit linear, 16-bit linear and 8-bit μ-law or A-law sample formats. The sample rate is 8ksamples/s. The bit order may be little or big endian. When 16-bit slots are used, the 3 or 8 unused bits in each slot may be filled with sign extension, padded with zeros or a programmable 3-bit audio attenuation compatible with some Motorola CODECs.

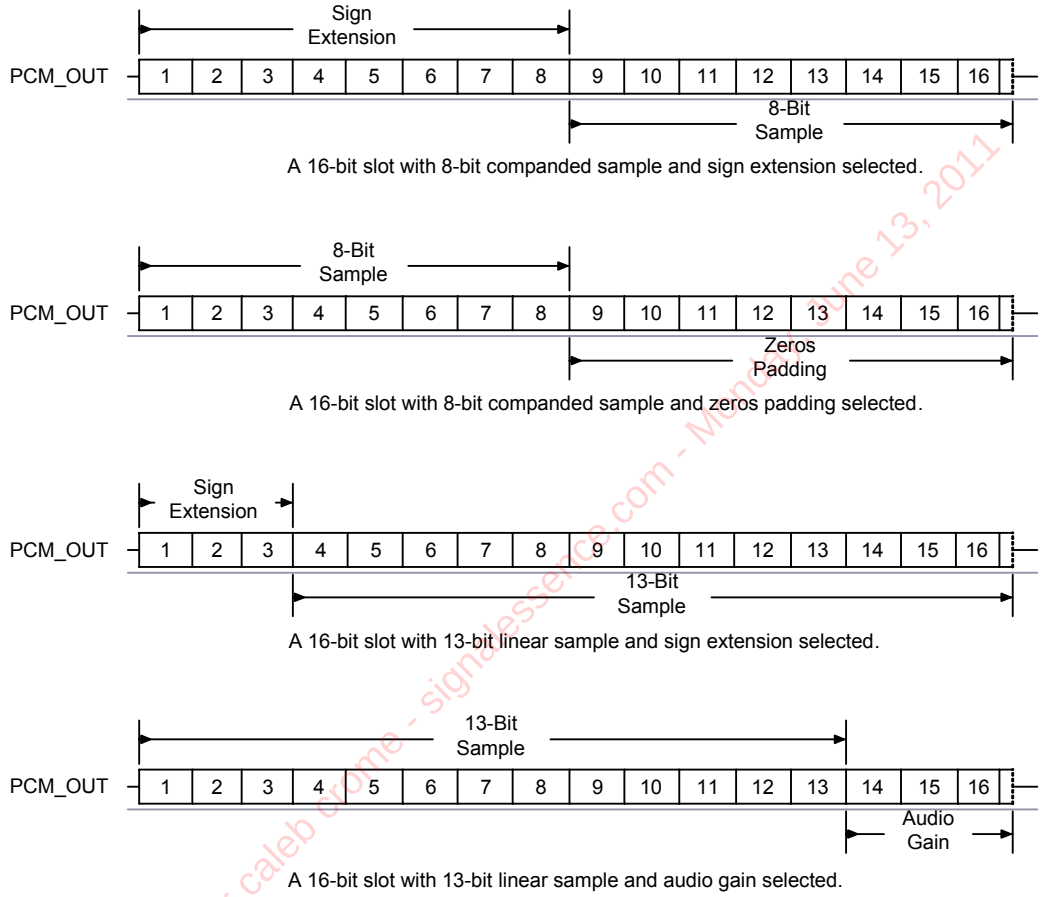



**Figure 10.7: 16-Bit Slot Length and Sample Formats**

### 10.1.7 Additional Features

BlueCore6-ROM QFN has a mute facility that forces PCM_OUT to be 0. In master mode, PCM_SYNC may also be forced to 0 while keeping PCM_CLK running which some CODECs use to control power down.

### 10.1.8 PCM Timing Information

| Symbol | Parameter | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{mclk}$ | PCM_CLK frequency | 4MHz DDS generation. Selection of frequency is programmable. See Table 10.4. | - | 128 | - | kHz |
| | | | | 256 | | |
| | | | | 512 | | |
| | | 48MHz DDS generation. Selection of frequency is programmable. See Table 10.3 and Section 10.1.9. | 2.9 | - | - | kHz |
| - | PCM_SYNC frequency for SCO connection | | - | 8 | - | kHz |
| $t_{mclkh}$ [(a)] | PCM_CLK high | 4MHz DDS generation | 980 | - | - | ns |
| $t_{mclkl}$ [(a)] | PCM_CLK low | 4MHz DDS generation | 730 | - | - | ns |
| - | PCM_CLK jitter | 48MHz DDS generation | - | - | 21 | ns pk-pk |
| $t_{dmclksynch}$ | Delay time from PCM_CLK high to PCM_SYNC high | | - | - | 20 | ns |
| $t_{dmclkpout}$ | Delay time from PCM_CLK high to valid PCM_OUT | | - | - | 20 | ns |
| $t_{dmclklsyncl}$ | Delay time from PCM_CLK low to PCM_SYNC low (Long Frame Sync only) | | - | - | 20 | ns |
| $t_{dmclkhsyncl}$ | Delay time from PCM_CLK high to PCM_SYNC low | | - | - | 20 | ns |
| $t_{dmclklpoutz}$ | Delay time from PCM_CLK low to PCM_OUT high impedance | | - | - | 20 | ns |
| $t_{dmclkhpoutz}$ | Delay time from PCM_CLK high to PCM_OUT high impedance | | - | - | 20 | ns |
| $t_{supinclkl}$ | Set-up time for PCM_IN valid to PCM_CLK low | | 30 | - | - | ns |
| $t_{hpinclkl}$ | Hold time for PCM_CLK low to PCM_IN invalid | | 10 | - | - | ns |

**Table 10.1: PCM Master Timing**

[(a)] Assumes normal system clock operation. Figures will vary during low power modes, when system clock speeds are reduced.

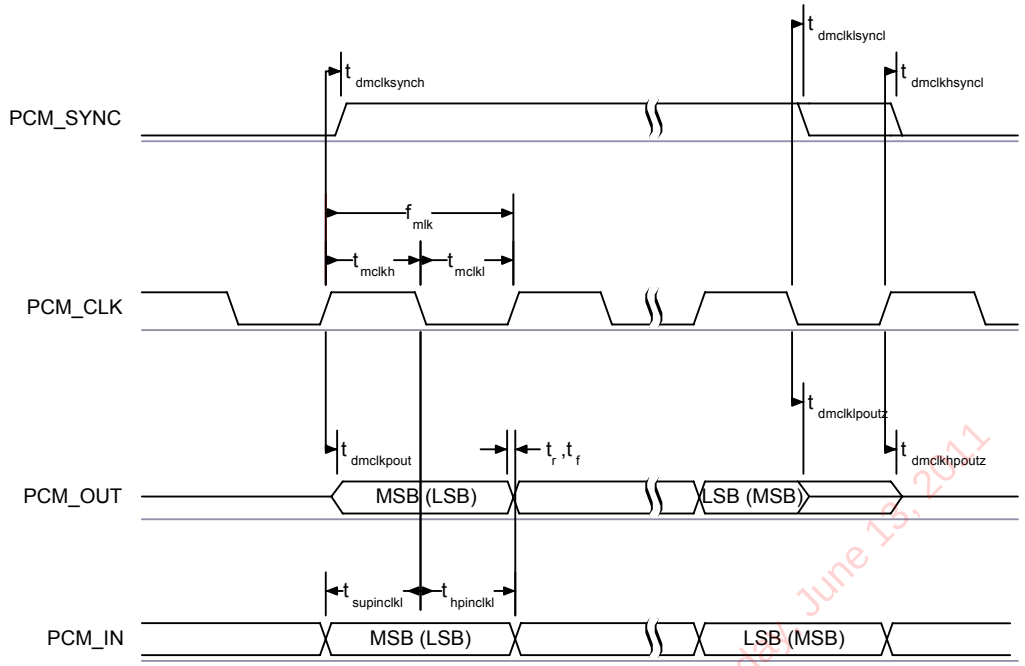



**Figure 10.8: PCM Master Timing Long Frame Sync**

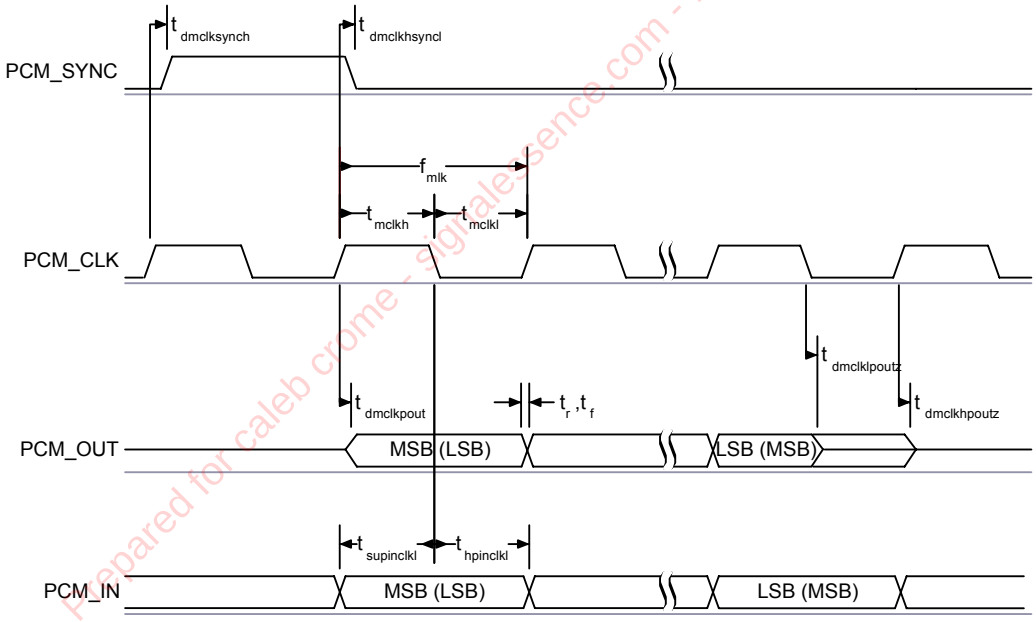



**Figure 10.9: PCM Master Timing Short Frame Sync**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $f_{sclk}$ | PCM clock frequency (Slave mode: input) | 64 | - | 2048 | kHz |
| $f_{sclk}$ | PCM clock frequency (GCI mode) | 128 | - | 4096 | kHz |
| $t_{sclkl}$ | PCM_CLK low time | 200 | - | - | ns |
| $t_{sclkh}$ | PCM_CLK high time | 200 | - | - | ns |
| $t_{hsclksynch}$ | Hold time from PCM_CLK low to PCM_SYNC high | 30 | - | - | ns |
| $t_{susclksynch}$ | Set-up time for PCM_SYNC high to PCM_CLK low | 30 | - | - | ns |
| $t_{dpout}$ | Delay time from PCM_SYNC or PCM_CLK whichever is later, to valid PCM_OUT data (Long Frame Sync only) | - | - | 20 | ns |
| $t_{dsclkhpout}$ | Delay time from CLK high to PCM_OUT valid data | - | - | 20 | ns |
| $t_{dpoutz}$ | Delay time from PCM_SYNC or PCM_CLK low, whichever is later, to PCM_OUT data line high impedance | - | - | 20 | ns |
| $t_{supinsclkl}$ | Set-up time for PCM_IN valid to CLK low | 30 | - | - | ns |
| $t_{hpinsclkl}$ | Hold time for PCM_CLK low to PCM_IN invalid | 30 | - | - | ns |

**Table 10.2: PCM Slave Timing**

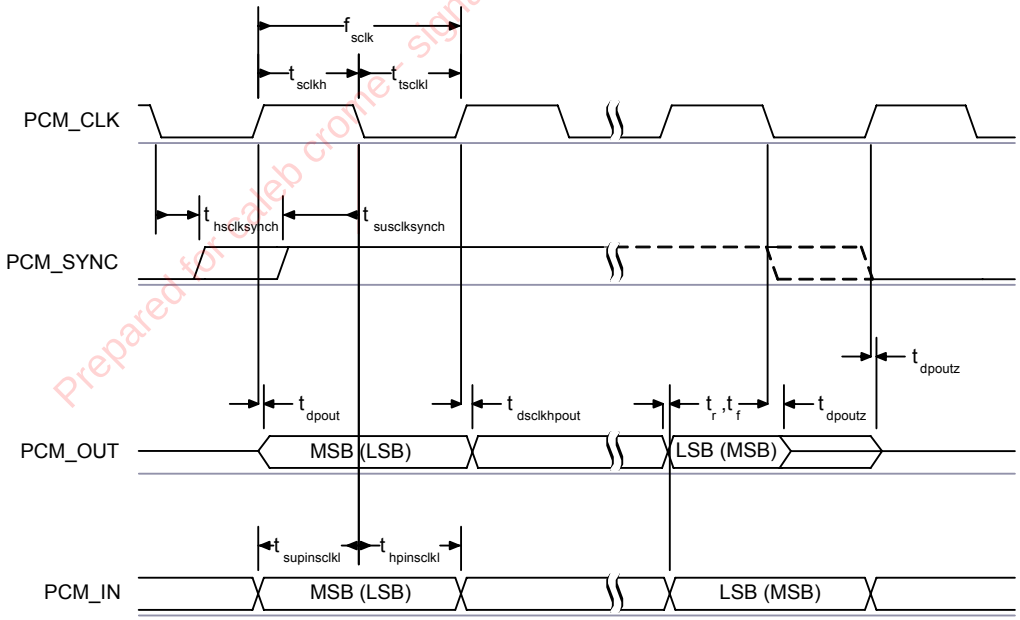



**Figure 10.10: PCM Slave Timing Long Frame Sync**

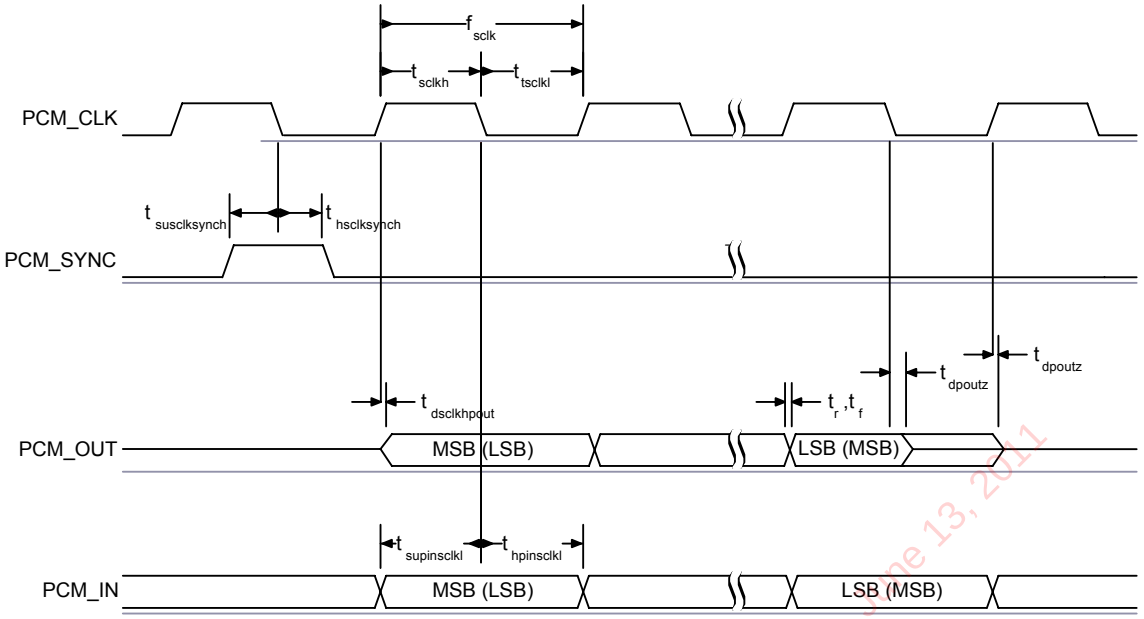



**Figure 10.11: PCM Slave Timing Short Frame Sync**

### 10.1.9 PCM_CLK and PCM_SYNC Generation

BlueCore6-ROM QFN has two methods of generating PCM_CLK and PCM_SYNC in master mode:

- Generating these signals by DDS from BlueCore6-ROM QFN internal 4MHz clock. Using this mode limits PCM_CLK to 128, 256 or 512kHz and PCM_SYNC to 8kHz.
- Generating these signals by DDS from an internal 48MHz clock (which allows a greater range of frequencies to be generated with low jitter but consumes more power). This method is selected by setting bit 48M_PCM_CLK_GEN_EN in PSKEY_PCM_CONFIG32. When in this mode and with long frame sync, the length of PCM_SYNC can be either 8 or 16 cycles of PCM_CLK, determined by LONG_LENGTH_SYNC_EN in PSKEY_PCM_CONFIG32.

Equation 10.1 describes PCM_CLK frequency when being generated using the internal 48MHz clock:

$$f = \frac{CNT\_RATE}{CNT\_LIMIT} \times 24MHz$$

**Equation 10.1: PCM_CLK Frequency When Being Generated Using the Internal 48MHz Clock**

The frequency of PCM_SYNC relative to PCM_CLK is set using Equation 10.2 or Equation 10.3 by setting the value of PCM_SYNC_MULT (see Table 10.4) :

$$f = \frac{PCM\_CLK}{SYNC\_LIMIT \times 8}$$

**Equation 10.2: PCM_SYNC Frequency Relative to PCM_CLK (PCM_SYNC_MULT = 0)**

$$f = \frac{PCM\_CLK}{SYNC\_LIMIT}$$

**Equation 10.3: PCM_SYNC Frequency Relative to PCM_CLK (PCM_SYNC_MULT = 1)**

CNT_RATE, CNT_LIMIT and SYNC_LIMIT are set using PSKEY_PCM_LOW_JITTER_CONFIG. As an example, to generate PCM_CLK at 512kHz with PCM_SYNC at 8kHz, set PSKEY_PCM_LOW_JITTER_CONFIG to 0x08080177.

### 10.1.10 PCM Configuration

The PCM configuration is set using the PS Keys, PSKEY_PCM_CONFIG32 described in Table 10.4 and PSKEY_PCM_LOW_JITTER_CONFIG in Table 10.3. The default for PSKEY_PCM_CONFIG32 is 0x00800000, i.e., first slot following sync is active, 13-bit linear voice format, long frame sync and interface master generating 256kHz PCM_CLK from 4MHz internal clock with no tri-state of PCM_OUT.

| Name | Bit Position | Description |
|---|---|---|
| CNT_LIMIT | [12:0] | Sets PCM_CLK counter limit |
| CNT_RATE | [23:16] | Sets PCM_CLK count rate |
| SYNC_LIMIT | [31:24] | Sets PCM_SYNC division relative to PCM_CLK |

**Table 10.3: PSKEY_PCM_LOW_JITTER_CONFIG Description**

| Name | Bit Position | Description |
|---|---|---|
| - | 0 | Set to 0. |
| SLAVE_MODE_EN | 1 | 0 = master mode with internal generation of PCM_CLK and PCM_SYNC.<br>1 = slave mode requiring externally generated PCM_CLK and PCM_SYNC. |
| SHORT_SYNC_EN | 2 | 0 = long frame sync (rising edge indicates start of frame).<br>1 = short frame sync (falling edge indicates start of frame). |

| Name | Bit Position | Description |
|---|---|---|
| - | 3 | Set to 0. |
| SIGN_EXTEND_EN | 4 | 0 = padding of 8 or 13-bit voice sample into a 16-bit slot by inserting extra LSBs. When padding is selected with 13-bit voice sample, the 3 padding bits are the audio gain setting; with 8-bit sample the 8 padding bits are zeroes.<br>1 = sign-extension. |
| LSB_FIRST_EN | 5 | 0 = MSB first of transmit and receive voice samples.<br>1 = LSB first of transmit and receive voice samples. |
| TX_TRISTATE_EN | 6 | 0 = drive PCM_OUT continuously.<br>1 = tri-state PCM_OUT immediately after falling edge of PCM_CLK in the last bit of an active slot, assuming the next slot is not active. |
| TX_TRISTATE_RISING_EDGE_EN | 7 | 0 = tri-state PCM_OUT immediately after falling edge of PCM_CLK in last bit of an active slot, assuming the next slot is also not active.<br>1 = tri-state PCM_OUT after rising edge of PCM_CLK. |
| SYNC_SUPPRESS_EN | 8 | 0 = enable PCM_SYNC output when master.<br>1 = suppress PCM_SYNC while keeping PCM_CLK running. Some CODECS use this to enter a low power state. |
| GCI_MODE_EN | 9 | 1 = enable GCI mode. |
| MUTE_EN | 10 | 1 = force PCM_OUT to 0. |
| 48M_PCM_CLK_GEN_EN | 11 | 0 = set PCM_CLK and PCM_SYNC generation via DDS from internal 4MHz clock.<br>1 = set PCM_CLK and PCM_SYNC generation via DDS from internal 48MHz clock. |
| LONG_LENGTH_SYNC_EN | 12 | 0 = set PCM_SYNC length to 8 PCM_CLK cycles.<br>1 = set length to 16 PCM_CLK cycles.<br>Only applies for long frame sync and with 48M_PCM_CLK_GEN_EN set to 1. |
| PCM_SYNC_MULT | 12 | 0 = Sync limit = SYNC_LIMIT x 8.<br>1 = SYNC_LIMIT. |
| - | [20:16] | Set to 0b00000. |
| MASTER_CLK_RATE | [22:21] | Selects 128 (0b01), 256 (0b00), 512 (0b10) kHz PCM_CLK frequency when master and 48M_PCM_CLK_GEN_EN (bit 11) is low. |
| ACTIVE_SLOT | [26:23] | Default is 0001. Ignored by firmware. |
| SAMPLE_FORMAT | [28:27] | Selects between 13 (0b00), 16 (0b01), 8 (0b10) bit sample with 16-cycle slot duration or 8 (0b11) bit sample with 8-cycle slot duration. |

**Table 10.4: PSKEY_PCM_CONFIG32 Description**

## 10.2 Digital Audio Interface (I²S)

The digital audio interface supports the industry standard formats for I²S, left-justified or right-justified. The interface shares the same pins as the PCM interface, which means each audio bus is mutually exclusive in its usage. Table 10.5 lists these alternative functions. Figure 10.12 shows the timing diagram.

| PCM Interface | I²S Interface |
|---|---|
| PCM_OUT | SD_OUT |
| PCM_IN | SD_IN |
| PCM_SYNC | WS |
| PCM_CLK | SCK |

**Table 10.5: Alternative Functions of the Digital Audio Bus Interface on the PCM Interface**

Table 10.6 describes the values for the PS Key (PSKEY_DIGITAL_AUDIO_CONFIG) that is used to set-up the digital audio interface. For example, to configure an I²S interface with 16-bit SD data set PSKEY_DIGITAL_CONFIG to 0x0406.

| Bit | Mask | Name | Description |
|---|---|---|---|
| D[0] | 0x0001 | CONFIG_JUSTIFY_FORMAT | 0 for left justified, 1 for right justified. |
| D[1] | 0x0002 | CONFIG_LEFT_JUSTIFY_DELAY | For left justified formats: 0 is MSB of SD data occurs in the first SCLK period following WS transition. 1 is MSB of SD data occurs in the second SCLK period. |
| D[2] | 0x0004 | CONFIG_CHANNEL_POLARITY | For 0, SD data is left channel when WS is high. For 1 SD data is right channel. |
| D[3] | 0x0008 | CONFIG_AUDIO_ATTEN_EN | For 0, 17 bit SD data is rounded down to 16 bits. For 1, the audio attenuation defined in CONFIG_AUDIO_ATTEN is applied over 24 bits with saturated rounding. Requires CONFIG_16_BIT_CROP_EN to be 0. |
| D[7:4] | 0x00F0 | CONFIG_AUDIO_ATTEN | Attenuation in 6 dB steps. |
| D[9:8] | 0x0300 | CONFIG_JUSTIFY_RESOLUTION | Resolution of data on SD_IN, 00=16 bit, 01=20 bit, 10=24 bit, 11=Reserved. This is required for right justified format and with left justified LSB first. |
| D[10] | 0x0400 | CONFIG_16_BIT_CROP_EN | For 0, 17 bit SD_IN data is rounded down to 16 bits. For 1 only the most significant 16 bits of data are received. |

**Table 10.6: PSKEY_DIGITAL_AUDIO_CONFIG**

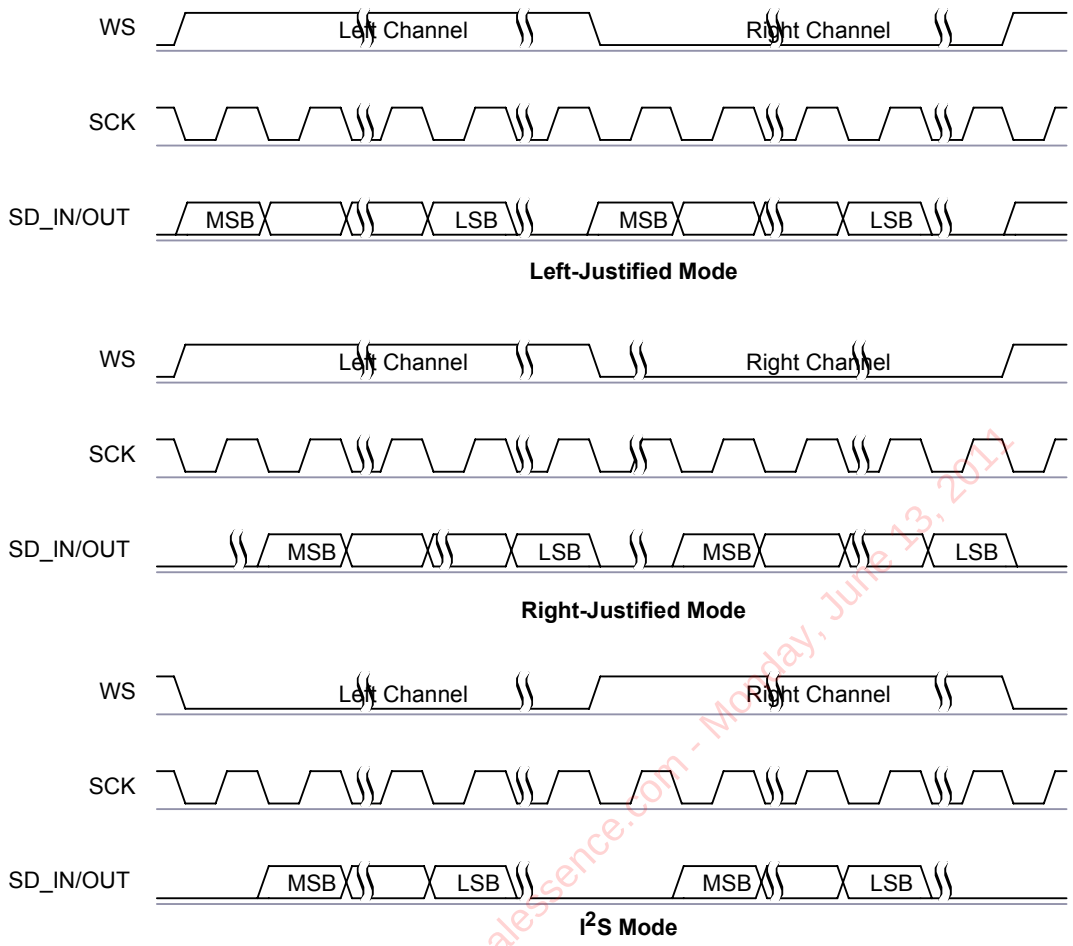



**Figure 10.12: Digital Audio Interface Modes**

The internal representation of audio samples within BlueCore6-ROM QFN is 16-bit and data on SD_OUT is limited to 16-bit per channel.

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| - | SCK Frequency | - | - | 6.2 | MHz |
| - | WS Frequency | - | - | 96 | kHz |
| $t_{ch}$ | SCK high time | 80 | - | - | ns |
| $t_{cl}$ | SCK low time | 80 | - | - | ns |
| $t_{opd}$ | SCK to SD_OUT delay | - | - | 20 | ns |
| $t_{ssu}$ | WS to SCK set-up time | 20 | - | - | ns |
| $t_{sh}$ | WS to SCK hold time | 20 | - | - | ns |
| $t_{isu}$ | SD_IN to SCK set-up time | 20 | - | - | ns |
| $t_{ih}$ | SD_IN to SCK hold time | 20 | - | - | ns |

**Table 10.7: Digital Audio Interface Slave Timing**

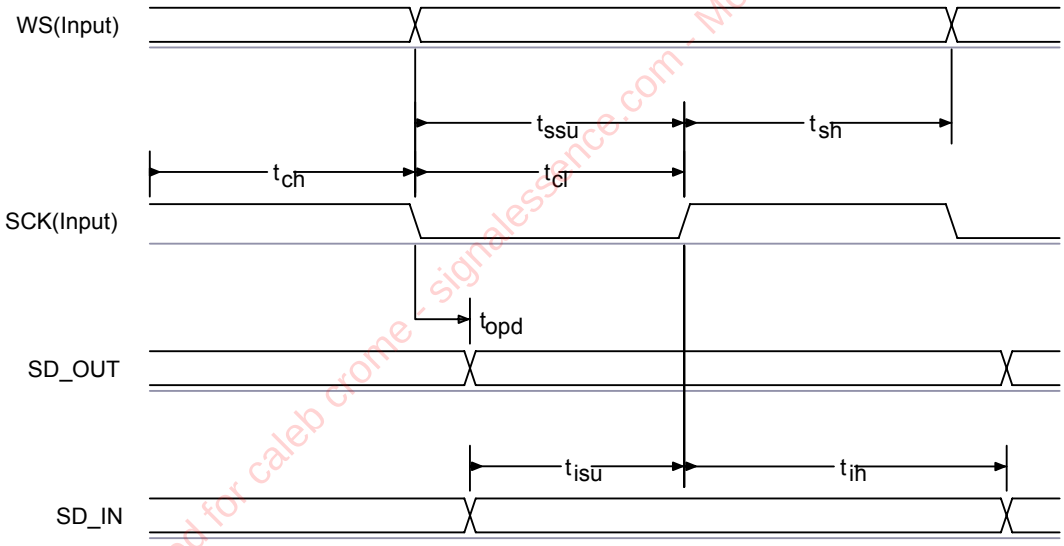



**Figure 10.13: Digital Audio Interface Slave Timing**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| - | SCK Frequency | - | - | 6.2 | MHz |
| - | WS Frequency | - | - | 96 | kHz |
| $t_{opd}$ | SCK to SD_OUT delay | - | - | 20 | ns |
| $t_{spd}$ | SCK to WS delay | - | - | 20 | ns |
| $t_{isu}$ | SD_IN to SCK set-up time | 20 | - | - | ns |
| $t_{ih}$ | SD_IN to SCK hold time | 10 | - | - | ns |

**Table 10.8: Digital Audio Interface Master Timing**

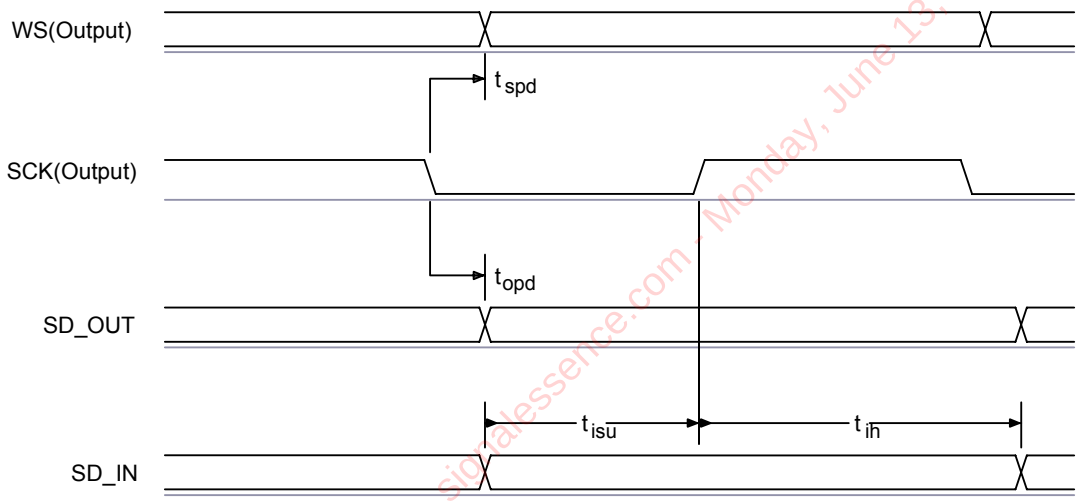



**Figure 10.14: Digital Audio Interface Master Timing**

# 11 Power Control and Regulation

BlueCore6-ROM QFN contains two linear regulators:

- A high-voltage regulator to generate a 1.8V rail for the chip I/Os
- A low-voltage regulator to supply the 1.5V core supplies from the 1.8V rail.

The chip can be powered from a high-voltage rail through both regulators. Alternatively the chip can be powered directly from an external 1.8V rail, bypassing the high-voltage regulator, or from an external 1.5V rail omitting both regulators.

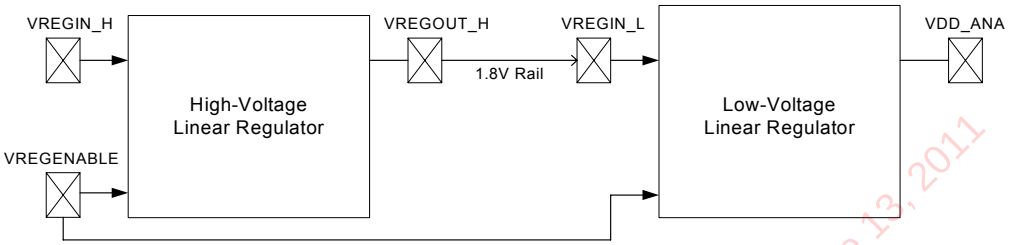



**Figure 11.1: Voltage Regulator Configuration**

## 11.1 Sequencing

The 1.5V supplies are VDD_ANA, VDD_RADIO and VDD_CORE. It is recommended that the 1.5V supplies are all powered at the same time.

The order of powering the 1.5V supplies relative to the other I/O supply (VDD_PADS) is not important. However, if the I/O supply is powered before the 1.5V supplies the digital pads default to their No Core Voltage Reset state. VDD_ANA and VDD_RADIO should be connected directly to the 1.5V supply; a simple RC filter is recommended for VDD_CORE to reduce transients fed back onto the power supply rails.

The I/O supplies may be connected together or independently to supplies at an appropriate voltage. They should be simply decoupled.

## 11.2 External Voltage Source

If the 1.5V rails of BlueCore6-ROM QFN are supplied from an external voltage source, it is recommended that VDD_RADIO and VDD_ANA should have less than 10mV rms noise levels between 0 to 10MHz. Single tone frequencies are also to be avoided.

The transient response of any regulator used should be 20µs or less. It is essential that the power rail recovers quickly at the start of a packet, where the power consumption jumps to high levels (refer to the average current consumption specification of the regulator).

## 11.3 High-Voltage Linear Regulator

CSR does not recommend using the high-voltage linear regulator to power any additional circuitry.

A smoothing circuit, using a low ESR 2.2µF capacitor and a 2.2Ω resistor to ground, should be connected to the output of the high-voltage linear regulator, VREGOUT_H.

Alternatively use a 2.2µF capacitor with an ESR of at least 2Ω.

The high-voltage linear regulator is enabled by the VREGENABLE_H pin.

The regulator is switched into a low-power mode when the device is in deep-sleep mode, or in reset.

When this regulator is not required, the VREGIN_H and VREGOUT_H terminals should be tied together or left unconnected.

## 11.4 Low-Voltage Linear Regulator

The on-chip low-voltage regulator may be used to power all the chip 1.5V supplies. The output of this regulator is connected internally to VDD_ANA, and must be connected externally to the other 1.5V supply pads. A smoothing circuit using a low ESR capacitor (2.2µF) and a resistor (2.2Ω) to ground should be connected to the output of the regulator. Alternatively use a 2.2µF capacitor with an ESR of at least 2Ω. See the Example Application Schematic.

The low-voltage linear regulator is enabled by the VREGENABLE pin.

The regulator is switched into a low power mode when the device is in Deep-Sleep mode, or in reset.

When this regulator is not used the terminal VREGIN_L must be left unconnected, or tied to VDD_ANA.

## 11.5 VREGENABLE

The regulator enable pin VREGENABLE is used to enable and disable the BlueCore6-ROM QFN device if the on-chip regulators are being used. VREGENABLE enables both the high voltage regulator and the low voltage regulator.

The pin is active high, with a logic threshold of around 1V, and has a weak pull-down to ground.

## 11.6 Reset (RST#)

BlueCore6-ROM QFN may be reset from several sources:

- RST# pin
- Power on reset
- A UART break character
- Via a software configured watchdog timer

The RST# pin is an active low reset and is internally filtered using the internal low frequency clock oscillator. A reset is performed between 1.5 and 4.0ms following RST# being active. It is recommended that RST# be applied for a period greater than 5ms.

The power on reset occurs when the VDD_CORE supply falls below typically 1.24V and is released when VDD_CORE rises above typically 1.31V. At reset the digital I/O pins are set to inputs for bi-directional pins and outputs are tri-state. The pull-down state is shown in . Following a reset, BlueCore6-ROM QFN assumes the maximum XTAL_IN frequency, which ensures that the internal clocks run at a safe (low) frequency until BlueCore6-ROM QFN is configured for the actual XTAL_IN frequency. If no clock is present at XTAL_IN, the oscillator in BlueCore6-ROM QFN free runs, again at a safe frequency.

### 11.6.1 Digital Pin States on Reset

The digital I/O interfaces on the BlueCore6-ROM QFN device are optimised for minimum power consumption after initialisation of digital interfaces.

Table 11.1 shows the pin states of BlueCore6-ROM QFN on reset. Pull-up (PU) and pull-down (PD) default to weak values unless specified otherwise.

| Pin Name/Group | I/O Type | No Core Voltage Reset | | Full Chip Reset | |
|---|---|---|---|---|---|
| | | Pull R | I/O | Pull R | I/O |
| Reset/Control | | | | | |
| RST# | Digital input | PU | Input | PU | Input |
| **Pin Name/Group** | **I/O Type** | **No Core Voltage Reset** | | **Full Chip Reset** | |
| | | **Pull R** | **I/O** | **Pull R** | **I/O** |
| Digital Interfaces - SDIO | | | | | |
| SDIO_DATA[3] | Digital bi-directional | PD | Input | PU | Input |
| SDIO_DATA[2] | Digital bi-directional | PD | Input | PU | Input |

| Pin Name/Group | I/O Type | No Core Voltage Reset | | Full Chip Reset | |
|---|---|---|---|---|---|
| | | Pull R | I/O | Pull R | I/O |
| SDIO_DATA[1] | Digital bi-directional | PD | Input | PU | Input |
| SDIO_DATA[0] | Digital bi-directional | PD | Input | PU | Input |
| SDIO_SD_CS# | Digital bi-directional | PD | Input | PU | Input |
| SDIO_CMD | Digital bi-directional | PD | Input | PU | Input |
| SDIO_CLK | Digital bi-directional | PD | Input | PU | Input |
| **Pin Name/Group** | **I/O Type** | **No Core Voltage Reset** | | **Full Chip Reset** | |
| | | **Pull R** | **I/O** | **Pull R** | **I/O** |
| PCM Interface | | | | | |
| PCM_IN | Digital input | PD | Input | PD | Input |
| PCM_OUT | Digital tri-state output | PD | High impedance | PD | High impedance |
| PCM_CLK | Digital bi-directional | PD | Input | PD | Input |
| PCM_SYNC | Digital bi-directional | PD | Input | PD | Input |
| **Pin Name/Group** | **I/O Type** | **No Core Voltage Reset** | | **Full Chip Reset** | |
| | | **Pull R** | **I/O** | **Pull R** | **I/O** |
| SPI Interface | | | | | |
| SPI_MOSI | Digital input | PD | Input | PD | Input |
| SPI_CLK | Digital input | PD | Input | PD | Input |
| SPI_CS# | Digital input | PU | Input | PU | Input |
| SPI_MISO | Digital tri-state output | PD | High impedance | PD | High impedance |
| **Pin Name/Group** | **I/O Type** | **No Core Voltage Reset** | | **Full Chip Reset** | |
| | | **Pull R** | **I/O** | **Pull R** | **I/O** |
| PIOs | | | | | |
| PIO[1] | Digital bi-directional | PD | Input | PD | Input |
| PIO[2] | Digital bi-directional | PD | Input | PD | Input |
| PIO[3] | Digital bi-directional | PD | Input | PD | Input |
| PIO[4] | Digital bi-directional | PD | Input | PD | Input |
| PIO[5] | Digital bi-directional | PD | Input | PD | Input |

| Pin Name/Group | I/O Type | No Core Voltage Reset | | Full Chip Reset | |
|---|---|---|---|---|---|
| | | Pull R | I/O | Pull R | I/O |
| PIO[7] | Digital bi-directional | PD | Input | PD | Input |
| PIO[9] | Digital bi-directional | PD | Input | PD | Input |
| **Pin Name/Group** | **I/O Type** | **No Core Voltage Reset** | | **Full Chip Reset** | |
| | | **Pull R** | **I/O** | **Pull R** | **I/O** |
| Clocks | | | | | |
| XTAL_IN | Ref clock | None | Input | None | Input |
| CLK_32K | Digital input | PD | Input | PD | Input |
| **Pin Name/Group** | **I/O Type** | **No Core Voltage Reset** | | **Full Chip Reset** | |
| | | **Pull R** | **I/O** | **Pull R** | **I/O** |
| Test | | | | | |
| TEST_EN | Digital input | Strong PD | Input | Strong PD | Input |

**Table 11.1: Pin States of BlueCore6-ROM QFN on Reset**

# 12 Example Application Schematic

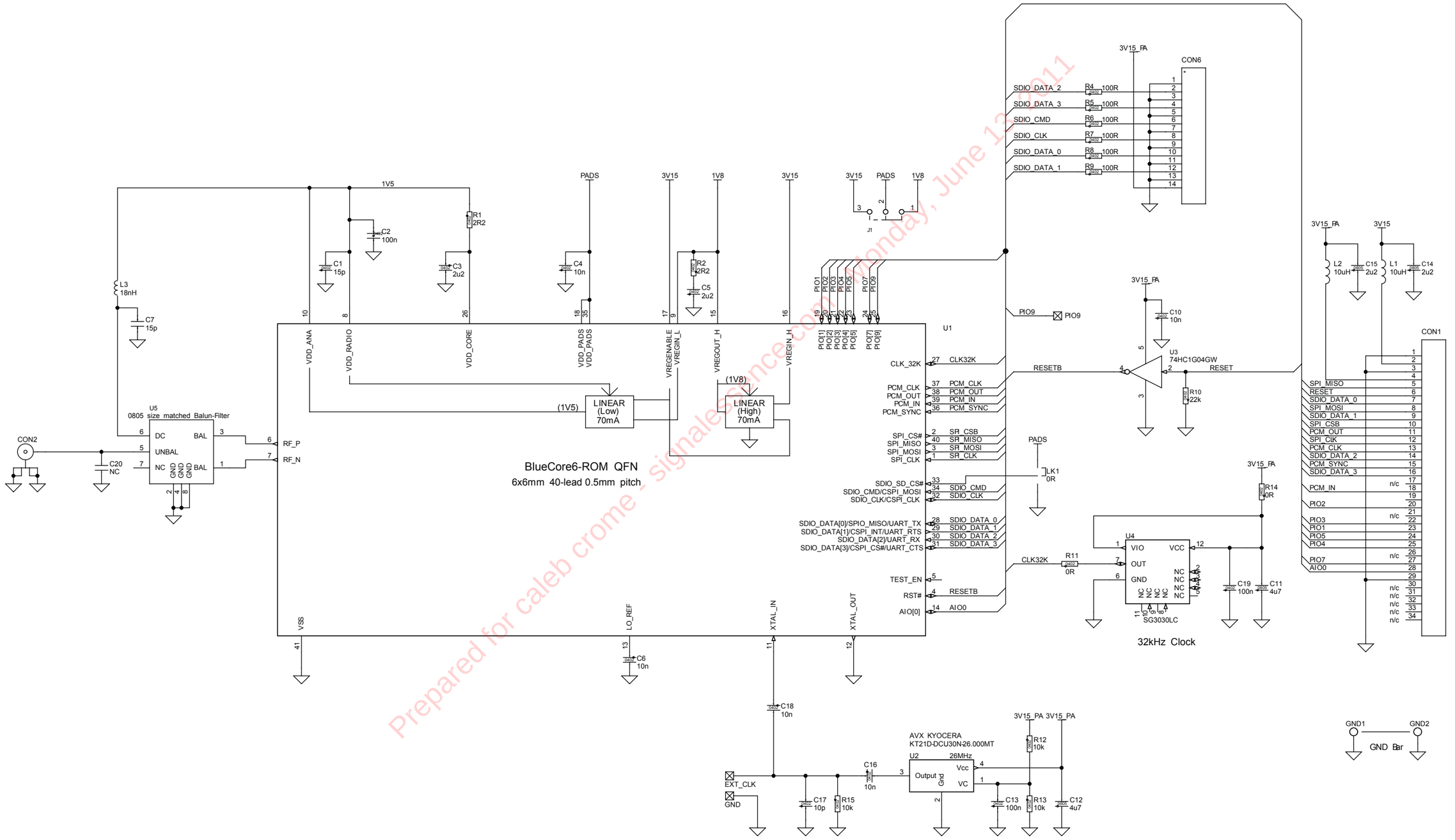



**Figure 12.1: Example Application Schematic**

# 13 Electrical Characteristics

## 13.1 ESD Precautions

BlueCore6-ROM QFN is classified as a JESD22-A114 Class 2 product. Apply ESD static handling precautions during manufacturing.

## 13.2 Absolute Maximum Ratings

| Rating | | Min | Max | Unit |
|---|---|---|---|---|
| Storage Temperature | | -40 | 85 | °C |
| Core Supply Voltage | VDD_RADIO, VDD_ANA and VDD_CORE | -0.4 | 1.65 | V |
| IO Voltage | VDD_PADS | -0.4 | 3.7 | V |
| Supply Voltage | VREGIN_L | -0.4 | 2.7 | V |
| | VREGIN_H, VREGENABLE | -0.4 | 4.9[a] | V |
| Other Terminal Voltages | | VSS-0.4 | VDD+0.4 | V |

[a] Operation up to 5.5V is permissible without damage and without the output voltage rising sufficiently to damage the rest of BlueCore6-ROM QFN, but output regulation and other specifications are no longer guaranteed at input voltages in excess of 4.9V. 5.5V can only be tolerated for short periods.

## 13.3 Recommended Operating Conditions

| Operating Condition | | Min | Max | Unit |
|---|---|---|---|---|
| Operating Temperature Range | | -40[a] | 85 | °C |
| Core Supply Voltage | VDD_RADIO, VDD_ANA and VDD_CORE | 1.4 | 1.6 | V |
| IO Voltage | VDD_PADS | 1.7 | 3.7 | V |

[a] CSR does not guarantee EDR receive sensitivity 8DPSK performance below 0°C.

## 13.4 Input/Output Terminal Characteristics

**Note:**

VDD_CORE, VDD_RADIO and VDD_ANA are at 1.5V unless shown otherwise.

VDD_PADS is at 1.8V unless shown otherwise.

Current drawn into a pin is defined as positive; current supplied out of a pin is defined as negative.

### 13.4.1 High-voltage Linear Regulator

| Normal Operation | Min | Typ | Max | Unit |
|---|---|---|---|---|
| Input voltage | 2.7 | - | 4.9[a] | V |
| Output voltage ($I_{load}$ = 70mA / VREGIN_H = 3.0V) | 1.70 | 1.80 | 1.90 | V |
| Temperature coefficient | -250 | 0 | 250 | ppm/°C |
| Output Noise[b] [c] | - | - | 1 | mV rms |
| Load regulation ($I_{load}$ < 70mA ) | - | - | 50 | mV/A |
| Settling time[b] [d] | - | - | 50 | µs |
| Maximum output current | 70 | - | - | mA |
| Minimum load current | 5 | - | - | µA |
| Quiescent current (excluding load, $I_{load}$ < 1mA) | 30 | 40 | 60 | µA |
| **Low Power Mode** [e] | | | | |
| Quiescent current (excluding load, $I_{load}$ < 100µA) | 10 | 13 | 21 | µA |
| **Standby Mode** | | | | |
| Quiescent current | 1.5 | 2.5 | 3.3 | µA |

[a] Short-term operation up to 5.5V is permissible without damage and without the output voltage rising sufficiently to damage the rest of BlueCore6-ROM QFN, but output regulation and other specifications are no longer guaranteed at input voltages in excess of 4.9V. 5.5V can only be tolerated for short periods.

[b] Regulator output connected to 47nF pure and 4.7µF 2.2Ω ESR capacitors.

[c] Frequency range 100Hz - 100kHz.

[d] 1mA - 70mA pulsed load.

[e] The regulator is in low power mode when the chip is in deep sleep mode.

### 13.4.2 Low-voltage Linear Regulator

| Normal Operation | Min | Typ | Max | Unit |
|---|---|---|---|---|
| Input voltage | 1.7 | - | 2.7 | V |
| Output voltage ($I_{load}$ = 70mA / VREGIN_L = 1.7V) | 1.4 | 1.5 | 1.6 | V |
| Temperature coefficient | -250 | 0 | 250 | ppm/°C |
| Output noise[a] [b] | - | - | 1 | mV rms |
| Load regulation ( $I_{load}$ < 70mA ) | - | - | 50 | mV/A |
| Settling time[a] [c] | - | - | 50 | µs |
| Maximum output current | 70 | - | - | mA |
| Minimum load current | 5 | - | - | µA |
| Quiescent current (excluding load, $I_{load}$ < 1mA) | 50 | 90 | 150 | µA |
| **Low Power Mode** [d] | | | | |
| Quiescent current (excluding load, $I_{load}$ < 100µA) | 6 | 10 | 17 | µA |
| **Standby Mode** | | | | |
| Quiescent current | 1.5 | 2.5 | 3.5 | µA |

[a] Regulator output connected to 47nF pure and 4.7µF 2.2Ω ESR capacitors

[b] Frequency range 100Hz to 100kHz

[c] 1mA to 70mA pulsed load

[d] The regulator is in low power mode when the chip is in deep sleep mode

### 13.4.3 Digital

| Digital Terminals | Min | Typ | Max | Unit |
|---|---|---|---|---|
| **Input Voltage Levels** | | | | |
| $V_{IL}$ input logic level low 1.7V ≤ VDD ≤ 3.6V | -0.4 | - | +0.25xVDD | V |
| $V_{IH}$ input logic level high | 0.7VDD | - | VDD+0.3 | V |
| **Output Voltage Levels** | | | | |
| $V_{OL}$ output logic level low, ($I_o$ = 4.0mA), 1.7V ≤ VDD ≤ 3.6V | - | - | 0.125 | V |
| $V_{OH}$ output logic level high, ($I_o$ = -4.0mA), 1.7V ≤ VDD ≤ 3.6V | VDD-0.4 | - | VDD | V |
| **Input and Tri-state Current with:** | | | | |
| Strong pull-up | -100 | -40 | -10 | µA |
| Strong pull-down | +10 | +40 | +100 | µA |
| Weak pull-up | -5.0 | -1.0 | -0.2 | µA |
| Weak pull-down | +0.2 | +1.0 | +5.0 | µA |
| I/O pad leakage current | -1 | 0 | +1 | µA |
| $C_I$ Input capacitance | 1.0 | - | 5.0 | pF |

### 13.4.4 Clocks

| Clock Source | Min | Typ | Max | Unit |
|---|---|---|---|---|
| **Crystal Oscillator** | | | | |
| Crystal frequency[a] | 16 | 26 | 26 | MHz |
| Digital trim range[b] | 5.0 | 6.2 | 8.0 | pF |
| Trim step size[b] | - | 0.1 | - | pF |
| Transconductance | 2.0 | - | - | mS |
| Negative resistance[c] | 870 | 1500 | 2400 | Ω |

| Clock Source | Min | Typ | Max | Unit |
|---|---|---|---|---|
| **External Clock** | | | | |
| Input frequency[d] | 12 | 26 | 52 | MHz |
| Clock input level[e] | 0.4 | - | VDD_ANA | V pk-pk |
| Edge jitter (allowable jitter), at zero crossing | - | - | 15 | ps rms |
| XTAL_IN input impedance | - | ≥10 | - | kΩ |
| XTAL_IN input capacitance | - | ≤4 | - | pF |

[a] Integer multiple of 250kHz

[b] The difference between the internal capacitance at minimum and maximum settings of the internal digital trim.

[c] XTAL frequency = 16MHz; XTAL $C_0$ = 0.75pF; XTAL load capacitance = 8.5pF.

[d] Clock input can be any frequency between 12MHz to 52MHz in steps of 250kHz plus CDMA/3G TCXO frequencies of 14.40, 15.36, 16.2, 16.8, 19.2, 19.44, 19.68, 19.8 and 38.4MHz.

[e] Clock input can be either sinusoidal or square wave. If the peaks of the signal are below VSS_ANA or above VDD_ANA. A DC blocking capacitor is required between the signal and XTAL_IN.

### 13.4.5 Reset

| Power-on Reset | Min | Typ | Max | Unit |
|---|---|---|---|---|
| VDD_CORE falling threshold | 1.13 | 1.25 | 1.30 | V |
| VDD_CORE rising threshold | 1.20 | 1.30 | 1.35 | V |
| Hysteresis | 0.05 | 0.10 | 0.15 | V |

### 13.4.6 RSSI ADC

| RSSI ADC[a] | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Resolution | | - | - | 10 | Bits |
| Input voltage range (LSB size = VDD_ANA/1024) | | 0 | - | VDD_ANA | V |
| Accuracy (Guaranteed monotonic) | INL | -1 | - | 1 | LSB |
| | DNL | 0 | - | 1 | LSB |
| Offset | | -4 | - | 4 | LSB |
| Gain Error | | -0.2 | - | 0.2 | % |
| Input Bandwidth | | - | 100 | - | kHz |
| Conversion time | | - | 2.75 | - | µs |
| Sample rate | | - | - | 700 | Samples/s |

[a] For more information about this ADC, see Section 4.2.2

### 13.4.7 32kHz External Reference Clock

| 32kHz External Reference Clock | Min | Typ | Max | Units |
|---|---|---|---|---|
| Frequency | 32748 | 32768 | 32788 | Hz |
| Frequency deviation at @25°C | - | - | ±20 | ppm |
| Frequency deviation at -30°C to 85°C | - | - | ±150 | ppm |
| Input high level, square wave | 0.625 x V1[(a)] | - | - | V |
| Input low level, square wave | - | - | 0.425 x V1[(a)] | V |
| Duty cycle square wave | 30 | - | 70 | % |
| Rise and fall time | - | - | 50 | ns |
| Integrated frequency jitter<br>Integrated over the band 200Hz to 15kHz | - | - | - | Hz (rms) |

[(a)] V1 = VDD_ANA for AIO[0] pad and VDD_PADS for CLK_32K pad.

# 14 HCI Power Consumption

| Operation Mode | Connection Type | Average | Unit |
|---|---|---|---|
| Page scan, time interval 1.28s | - | 0.4 | mA |
| Inquiry and page scan, time interval 1.28s | - | 0.8 | mA |
| ACL no traffic | Master | 4 | mA |
| ACL with file transfer | Master | 9 | mA |
| ACL 40ms sniff | Master | 2 | mA |
| ACL 1.28s sniff | Master | 0.2 | mA |
| eSCO EV5 | Master | 12 | mA |
| eSCO EV3 | Master | 18 | mA |
| eSCO EV3 - hands-free - setting S1 | Master | 18.5 | mA |
| SCO HV1 | Master | 37 | mA |
| SCO HV3 | Master | 17 | mA |
| SCO HV3 30ms sniff | Master | 17 | mA |
| ACL no traffic | Slave | 14 | mA |
| ACL with file transfer | Slave | 17 | mA |
| ACL 40ms sniff | Slave | 1.6 | mA |
| ACL 1.28s sniff | Slave | 0.2 | mA |
| eSCO EV5 | Slave | 19 | mA |
| eSCO EV3 | Slave | 23 | mA |
| eSCO EV3 - hands-free - setting S1 | Slave | 23 | mA |
| SCO HV1 | Slave | 37 | mA |
| SCO HV3 | Slave | 23 | mA |
| SCO HV3 30ms sniff | Slave | 16 | mA |
| Standby host connection (Deep-Sleep) | - | 40 | µA |
| Reset (active low) | - | 39 | µA |

**Note:**

Conditions: 20°C, VREGIN_H 3.15V

VDD_PADS: 3.15V

UART BAUD rate: 115.2kbps

| Typical Peak Current @ +20°C | |
|---|---|
| **Device Activity/State** | **Current (mA)** |
| Peak current during cold boot | 45 |
| Peak TX current Master | 45 |
| Peak RX current Master | 40 |
| Peak TX current Slave | 45 |
| Peak RX current Slave | 45 |
| **Conditions** | |
| Firmware | HCI 23c |
| VREGIN_H, VDD_PADS | 3.15 |
| Host Interfaces | UART |
| UART Baud rate | 115200 |
| Clock source | 26MHz crystal |
| RF output power | 0dBm |

# 15 CSR Software Stacks

BlueCore6-ROM QFN is supplied with Bluetooth v2.1 + EDR compliant stack firmware, which runs on the internal RISC MCU.

## 15.1 BlueCore HCI Stack

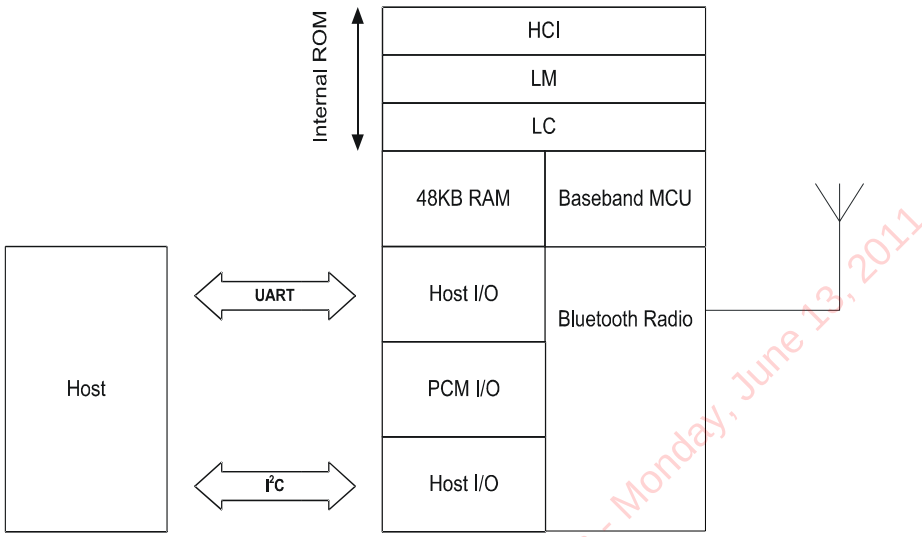



**Figure 15.1: BlueCore HCI Stack**

In the implementation shown in Section 15.1 the internal processor runs the Bluetooth stack up to the HCI. The Host processor must provide all upper layers including the application.

### 15.1.1 Key Features of the HCI Stack: Standard Bluetooth Functionality

CSR supports the following Bluetooth v2.1 + EDR functionality:

- Secure simple pairing
- Sniff subrating
- Encryption pause resume
- Packet boundary flags
- Encryption
- Extended inquiry response

CSR supports the following Bluetooth v2.0 + EDR mandatory functionality:

- AFH, including classifier
- Faster connection: enhanced Inquiry Scan (immediate FHS response)
- LMP improvements
- Parameter ranges

Optional Bluetooth v2.0 + EDR functionality supported:

- AFH as Master and Automatic Channel Classification
- Fast Connect: Interlaced Inquiry and Page Scan plus RSSI during Inquiry
- eSCO, eV3 +CRC, eV4, eV5
- SCO handle
- Synchronisation

The firmware was written against the Bluetooth v2.0 + EDR specification.

- Bluetooth components:

    - Baseband, including LC
    - LM
    - HCI
- Standard UART HCI Transport Layers
- All standard Bluetooth radio packet types
- Full Bluetooth data rate, enhanced data rates of 2 and 3Mbps . This is the maximum allowed by Bluetooth v2.0 + EDR specification
- Operation with up to 7 active slaves
- Scatternet v2.5 operation
- Maximum number of simultaneous active ACL connections: 7. BlueCore6-ROM QFN Supports all combinations of active ACL and SCO channels for both master and slave operation, as specified by the Bluetooth v2.0 + EDR specification
- Maximum number of simultaneous active SCO connections: 3
- Operation with up to 3 SCO links, routed to one or more slaves
- All standard SCO voice coding, plus transparent SCO
- Standard operating modes: Page, Inquiry, Page Scan and Inquiry Scan
- All standard pairing, authentication, link key and encryption operations
- Standard Bluetooth power saving mechanisms
- Dynamic control of peers' transmit power via LMP
- Master/Slave switch
- Broadcast
- Channel quality driven data rate
- All standard Bluetooth test modes

### 15.1.2 Key Features of the HCI Stack: Extra Functionality

The firmware extends the standard Bluetooth functionality with the following features:

- Supports BCSP, a proprietary, reliable alternative to the standard Bluetooth UART Host Transport
- Supports H4DS, a proprietary alternative to the standard Bluetooth UART Host Transport, supporting deep sleep for low-power applications
- Provides a set of approximately 50 manufacturer-specific HCI extension commands. This command set, called BCCMD, provides:
    - Access to the IC's general-purpose PIO port
    - The negotiated effective encryption key length on established Bluetooth links
    - Access to the firmware's random number generator
    - Controls to set the default and maximum transmit powers; these can help minimise interference between overlapping, fixed-location piconets
    - Dynamic UART configuration
    - Bluetooth radio transmitter enable/disable. A simple command connects to a dedicated hardware switch that determines whether the radio can transmit.
- The firmware can read the voltage on a pair of the IC's external pins. This is normally used to build a battery monitor
- A block of BCCMD commands provides access to the IC's PS configuration database. The database sets the device's Bluetooth address, Class of Device, Bluetooth radio (transmit class) configuration, SCO routing, LM, constants, etc.
- A UART break condition can be used in three ways:
    6.1 Presenting a UART break condition to the IC can force the IC to perform a hardware reboot
    6.2 Presenting a break condition at boot time can hold the IC in a low power state, preventing normal initialisation while the condition exists
    6.3 With BCSP, the firmware can be configured to send a break to the host before sending data. (This is normally used to wake the host from a deep sleep state.)
- A block of Bluetooth radio test or BIST commands allows direct control of the IC's radio. This aids the development of modules' radio designs, and can be used to support Bluetooth qualification.
- Hardware low power modes: shallow sleep and deep sleep. The IC drops into modes that significantly reduce power consumption when the software goes idle.
- SCO channels are normally routed via HCI (over BCSP). However, up to three SCO channels can be routed over the IC's PCM ports (at the same time as routing any remaining SCO channels over HCI).

**Note:**

Always refer to the firmware release note for the specific functionality of a particular build.

## 15.2 BCHS Software

BCHS is enables CSR customers to implement Bluetooth functionality into embedded products quickly, cheaply and with low risk.

BCHS works withCSR's family of BlueCore ICs. BCHS is intended for embedded products that have a host processor for running BCHS and the Bluetooth application, such as a mobile phone or a PDA. BCHS together with the BlueCore IC with embedded Bluetooth core stack (L2CAP, RFCOMM and SDP) is a complete Bluetooth system solution from RF to profiles.

BCHS includes most of the Bluetooth intelligence and gives the user a simple API. This makes it possible to develop a Bluetooth product without in-depth Bluetooth knowledge.

BCHS contains three elements:

- Example Drivers
- Bluetooth Profile Managers
- Example Applications

The profiles are qualified which makes the qualification of the final product very easy. BCHS is delivered with source code (ANSI C). It also comes with example applications in ANSI C, which makes the process of writing the application easier.

## 15.3 CSR Development Systems

CSR's BlueLab and Casira development kits are available to allow the evaluation of the BlueCore6-ROM QFN hardware and software, and as toolkits for developing on-chip and host software.

# 16 Ordering Information

| Interface Version | Package | | | Order Number |
|---|---|---|---|---|
| | Type | Size | Shipment Method | |
| UART | 40-lead QFN<br>(Pb free) | 6 x 6 x 0.9mm (max.), 0.5mm pitch | Tape and reel | BC63B239A04-ICXL-R |

**Note:**

**Minimum Order Quantity**

2kpcs taped and reeled

**Supply chain**: CSR's manufacturing policy is to multisource volume products. For further details, contact your local sales account manager or representative.

To contact a CSR representative, send e-mail to sales@csr.com or go to www.csr.com/contacts.htm.

## 16.1 Ordering Information

| Interface Version | Package | | | Order Number |
|---|---|---|---|---|
| | Type | Size | Shipment Method | |
| UART, SDIO, CSPI | 40-lead QFN<br>(Pb free) | 6 x 6 x 0.9mm, 0.5mm pitch | Tape and reel | BC63B239A04-IQD-E4 |

**Note:**

**Minimum Order Quantity**

2kpcs taped and reeled

To contact a CSR representative, send e-mail to sales@csr.com or go to www.csr.com/contacts.htm.

## 16.2 Tape and Reel Information

For tape and reel packing and labeling see *IC Packing and Labelling Specification*.

### 16.2.1 Tape Orientation

The general orientation of the QFN in the tape is as shown in Figure 16.1.

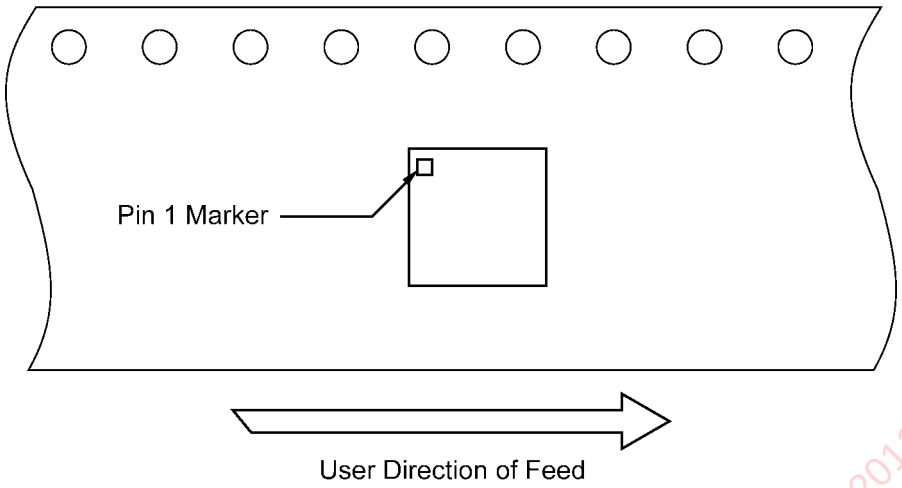
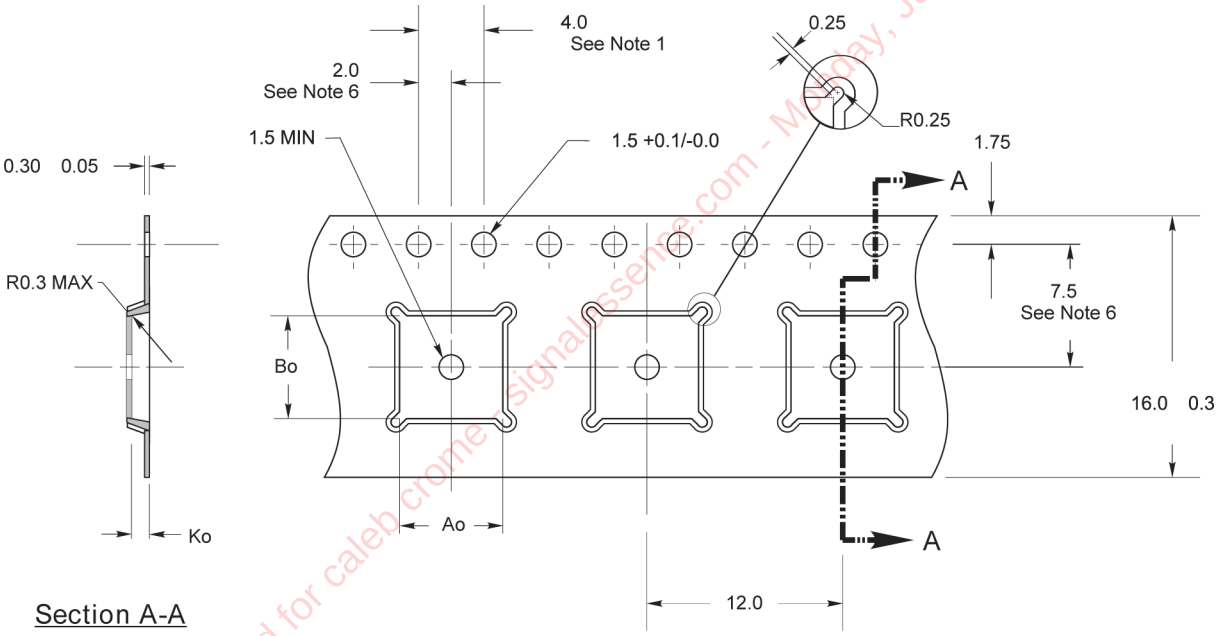



**Figure 16.1: Tape and Reel Orientation**

### 16.2.2 Tape Dimensions




| $A_0$ | $B_0$ | $K_0$ | Unit | Notes |
|---|---|---|---|---|
| 6.3 | 6.3 | 1.1 | mm | 1. 10 sprocket hole pitch cumulative tolerance ±0.02<br>2. Camber not to exceed 1mm in 100mm<br>3. Material: PS + C<br>4. $A_0$ and $B_0$ measured as indicated<br>5. $K_0$ measured from a plane on the inside bottom of the pocket to the top surface of the carrier<br>6. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole |

### 16.2.3 Reel Information

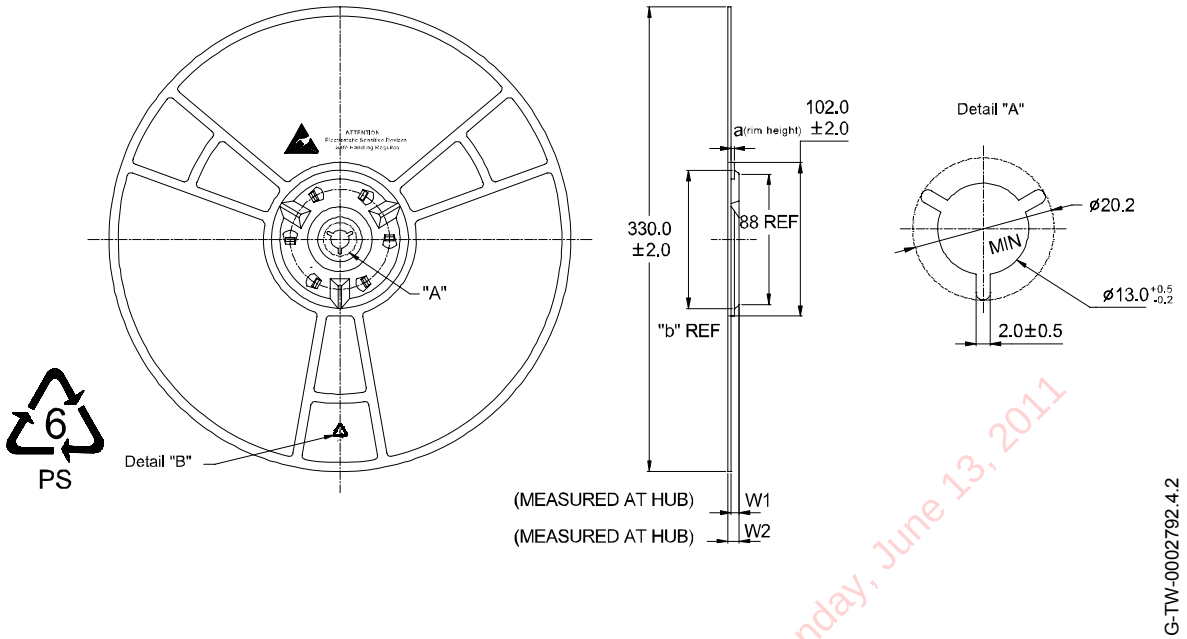



**Figure 16.2: Reel Dimensions**

| Package Type | Nominal Hub Width (Tape Width) | a | b | W1 | W2 Max | Units |
|---|---|---|---|---|---|---|
| 6 x 6 x 0.9mm QFN | 16mm | 4.5 | 98.0 | 16.4 (3.0/-0.2) | 19.1 | mm |

# 17 Document References

| Document: | Reference, Date: |
|---|---|
| *Core Specification of the Bluetooth System* | v2.1 + EDR, 31 July 2007 |
| *Core Specification of the Bluetooth System* | v2.0 + EDR, 10 November 2004 |
| *CSR Bluetooth Coexistence Implementations* | CS-110632-AN |
| *BCCMD Commands* | CS-101482-SPP (bcore-sp-005P) |
| *HQ Commands* | CS-101677-SPP (bcore-sp-003P) |
| *IC Packing and Labelling Specification* | CS-112584-SPP |
| *SD Specifications Part 1 Physical layer specification v1.10* | For more information, see http://www.sdcard.org/sdio/index.html |
| *SD Specifications Part E1 SDIO specification v1.10* | |
| *SDIO Card Part E2 Type-A Specification for Bluetooth v1.00* | |
| *Typical Solder Reflow Profile for Lead-free Devices* | CS-116434-ANP |

# Terms and Definitions

| Term | Definition |
|---|---|
| 802.11™ | WLAN specification defined by a working group within the IEEE |
| 8DPSK | 8-phase Differential Phase Shift Keying |
| π/4 DQPSK | π/4 rotated Differential Quaternary Phase Shift Keying |
| ADC | Analogue to Digital Converter |
| ADPCM | Adaptive Differential Pulse Code Modulation (e.g G.726) |
| AFH | Adaptive Frequency Hopping |
| AGC | Automatic Gain Control |
| AuriStream | CSR proprietary ADPCM codec |
| BCCMD | BlueCore Command |
| BCHS | BlueCore Host Software |
| BCSP | BlueCore Serial Protocol |
| BIST | Built-In Self-Test |
| Bluetooth® | Set of technologies providing audio and data transfer over short-range radio connections |
| BMC | Burst Mode Controller |
| codec | Coder decoder |
| CRC | Cyclic Redundancy Check |
| CSB | Chip Select |
| CSPI | CSR Serial Peripheral Interface |
| CSR | Cambridge Silicon Radio |
| CVSD | Continuous Variable Slope Delta Modulation |
| DC | Direct Current |
| DDS | Direct Digital Synthesis |
| EDR | Enhanced Data Rate |
| eSCO | Extended SCO |
| ESD | Electrostatic Discharge |
| FIFO | First-In First-Out (queue) |
| FSK | Frequency Shift Keying |
| GCI | General Circuit Interface |
| GFSK | Gaussian Frequency Shift Keying |
| GSM | Global System for Mobile communications |
| H4DS | H4 Deep Sleep |
| HCI | Host Controller Interface |
| I/O | Input/Output |
| IC | Integrated Circuit |
| IEEE | Institute of Electronic and Electrical Engineers |
| IF | Intermediate Frequency |
| L2CAP | Logical Link Control and Adaptation Protocol |
| LC | An inductor (L) and capacitor (C) network |
| LM | Link Manager |
| LNA | Low Noise Amplifier |
| LSB | Least-Significant Bit (or Byte) |

| Term | Definition |
|---|---|
| Mbps | Megabits per second |
| MCU | MicroController Unit |
| MMU | Memory Management Unit |
| PA | Power Amplifier |
| PDA | Personal Digital Assistant |
| PIO | Programmable Input/Output |
| plc | Public Limited Company |
| PS | Persistent Store |
| QFN | Quad-Flat No-lead |
| RAM | Random Access Memory |
| RFCOMM | Radio Frequency COMMunication. Protocol layer providing serial port emulation over L2CAP |
| RISC | Reduced Instruction Set Computer |
| RoHS | Restriction of Hazardous Substances in Electrical and Electronic Equipment Directive (2002/95/EC) |
| RSSI | Received Signal Strength Indication |
| SCO | Synchronous Connection-Oriented |
| SDIO | Secure Digital Input/Output |
| SDP | Service Discovery Protocol; element of Bluetooth |
| SIG | (Bluetooth) Special Interest Group |
| UART | Universal Asynchronous Receiver Transmitter |
| VCO | Voltage Controlled Oscillator |
| W-CDMA | Wideband Code Division Multiple Access |
| WCS | Wireless Coexistence System |