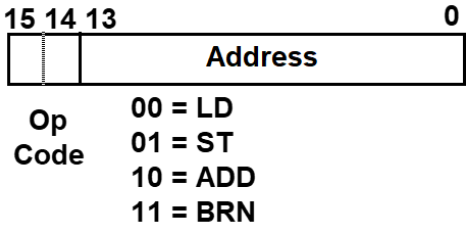
SAM CPU Implementation

1. Project Summary

   - Implement SAM CPU using Verilog language.
   - Number of team members : 1-3
   - Due date: Dec 16, 23:59

2. Implementation Specification

   - An incomplete Verilog code of SAM CPU will be given on YSCEC. Download the code and complete it. You can complete the code by filling missing parts which is indicated as comments "To-do:". A sample testbench will be given to test your codes.
   - CPU instructions are Identical to the instructions in the lecture note.
     - The leftmost two bits of the instructions are op codes (see the figure below). A list of instructions and actions are given in the table below.



OP-code	Instruction	Action
00	Load from memory	Mem[Address] → AC
01	Store to memory	AC → Mem[Address]
10	Add from memory	AC+Mem[Address] → AC
11	Branch if accumulator is negative	IF AC<0, Address → PC

3. Submit Form

   - Submit all modified Verilog files from the sample code.
     - Verilog files uploaded on YSCEC will be enough to implement SAM CPU, but if you want to add new modules, you are free to implement/use and upload ones.
   - On Dec 17, 15:00, you'll have time to demonstrate your codes. The place will be noticed on YSCEC later. Testbench for demonstration will be released right after submission. You can use the output formats described in your testbench.