Project-1 :
Design and Comparison of Adders

Project 1

Due Date

- Nov. 4, 19:00 pm

Summary

- Design ripple carry adder (RCA) and carry look-ahead adder (CLA) using Verilog language.
- Compare delay and price of the modules using given gate delays and prices.

Submit Form

- Submit all Verilog files (files with .v extension) and a report file.

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Implementation Specifics

- Implement RCA and CLA modules with Verilog language. Modules should be named as ‘rca’ and ‘cla’.
- The adders should perform 4-bit + 4-bit operation. The module should have two 4-bit inputs, one 4-bit result output, and 1-bit overflow flag output. Subtraction is not required for this project.
- A sample testbench will be given as ‘testbench.v’ file and your modules should be compatible with the given testbench.
- Use only the gates in the following table. You can’t use other gates or expressions (4-bit and gate, if-else clause, etc.)

Module	Delay	Price	Module	Delay	Price
Inverter	5ps	2			
2 input AND	20ps	5	3 input AND	30ps	8
2 input OR	20ps	5	3 input OR	30ps	8
2 input NAND	15ps	4	3 input NAND	25ps	7
2 input NOR	15ps	4	3 input NOR	25ps	7
2 input XOR	30ps	7	3 input XOR	45ps	10

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❖ The sample testbench

```
`timescale 1ns/1ns

module testbench_prj1();
        reg [3:0] a,b;           // 4-bit inputs
        wire [3:0] s_rca,s_cla; // 4-bit sum outpus
        wire o_rca, o_cla;       // 1-bit overflow flags

        rca my_rca(a,b,s_rca,c_rca);
        cla my_cla(a,b,s_cla,c_cla);

        initial begin
                a=5;b=3; #1;     // s=8(-8), o=1
                a=4;b=-2; #1;    // s=2, o=0
                a=7;b=6; #1;     // s=13(-3), o=1
                a=8;b=9; #1;     // s=1, o=1
        end

endmodule
```

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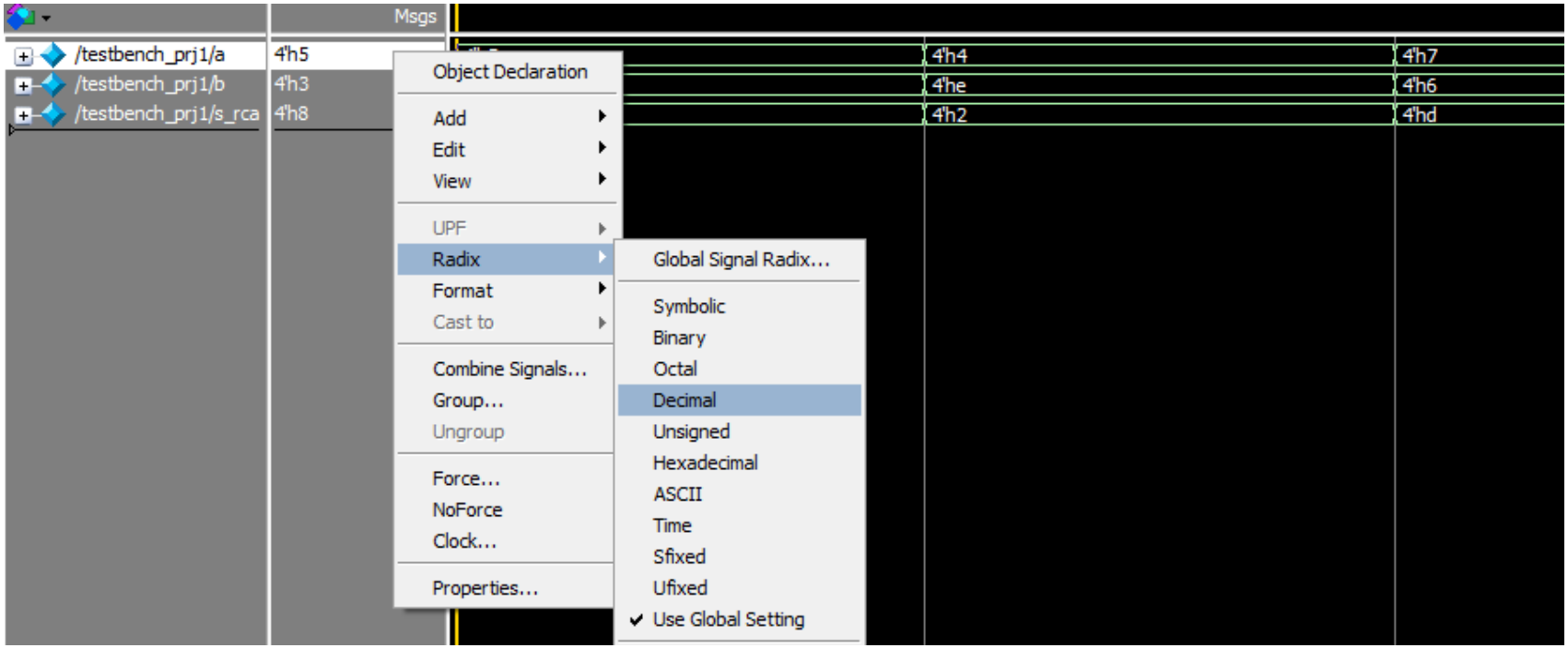
❖ Setting Radix



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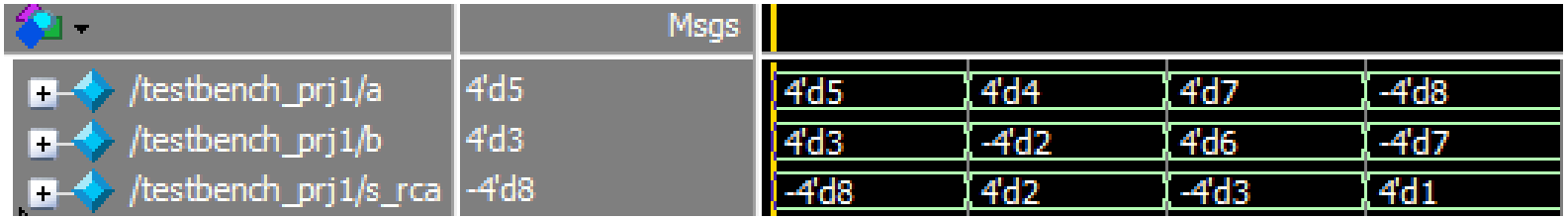
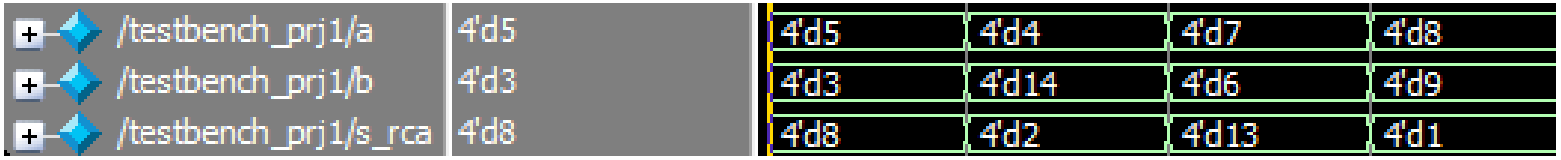
❖ Decimal



❖ Unsigned



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- **Analysis Report**
  - Calculate and compare the delay and price of the RCA and CLA modules with gate delays and prices in the table above.
  - Take a screenshot of the waveform which expresses the calculated delay.

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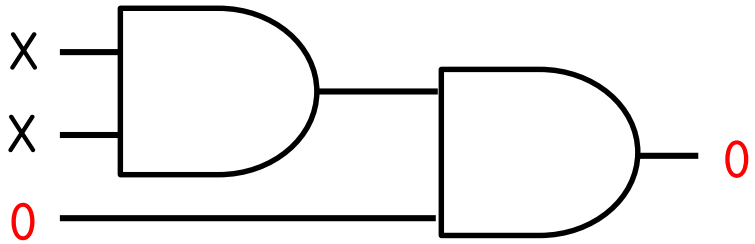
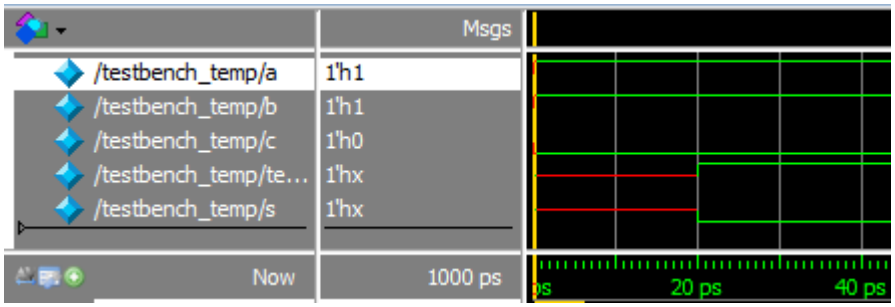
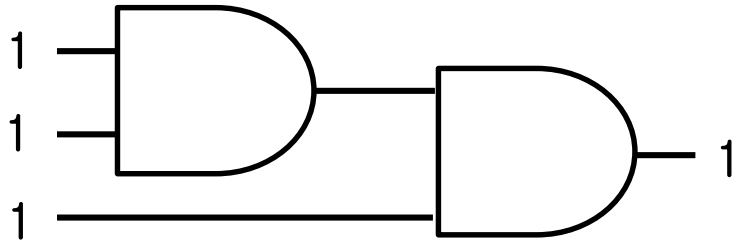
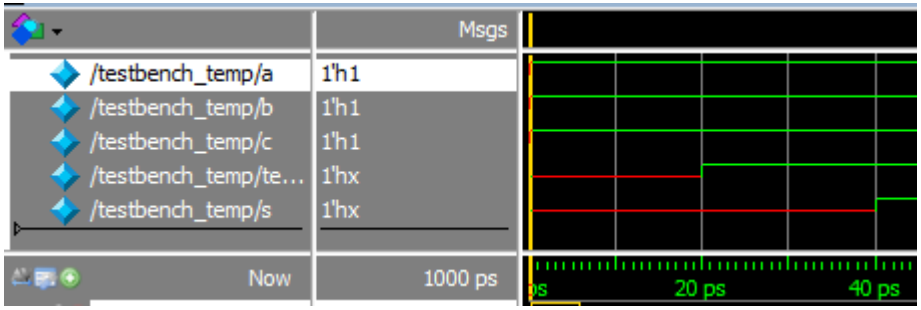
- **Maximum delay matters**
  - but not all inputs give maximum delays









Q & A

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