

COMP4300 Fall 2022  
Homework 2

1. Suppose you are designing a cache for a machine with 28-bit addresses. The cache is 8MB in size. Cache blocks are 8192 bytes.

a. How many blocks can be held in the cache

$$1 \text{ MB} = 2^{20} \text{ bytes}$$

$$8 \text{ MB} = 2^{23} \text{ bytes}$$

$$8192 \text{ bytes} = 2^{13} \text{ bytes}$$

$$2^{23} / 2^{13} = 2^{10} = 1024 \text{ blocks}$$

b. How many bits of the address are devoted to the offset?

$$8192 = 2^{13}$$

**So 13 bits of the address are devoted to the offset**

c. If the cache is direct-mapped, how many bits are devoted to the tag and index?

$$\text{Index} = \text{cache size} / \text{block size}$$

$$\text{Index} = 2^{23} / 2^{13} = 2^{10} = 10 \text{ bits to the index}$$

$$\text{Tag} = \text{machine address} - \text{offset} - \text{index}$$

$$\text{Tag} = 28 - 13 - 10 = 5 \text{ bit to the tag}$$

d. If the cache is 8-way set associative, how many bits are devoted to the tag and index? How many sets are there?

$$\text{Sets} = \text{blocks} / 8 = 1024 / 8 = 128 = 2^7 \text{ sets}$$

$$7 \text{ bits for the index}$$

$$\text{Tag} = 28 - 13 - 7 = 8 \text{ bits for the tag}$$

e. If the cache is fully associative, how many bits are devoted to the tag and index?

**Index is 0 in fully associative mapping**

**Tag = machine address – offset = 28 – 13 = 15 bits for the tag**

**So 15 bits for the tag**

**0 bits for the index**

**13 bits for the offset**

2. Suppose you have a machine with separate I- and D- caches. The miss rate on the I-cache is 1.2%, and on the D-cache 3.4%. On an I-cache hit, the value can be read in the same cycle the data is requested. On a D-cache hit, one additional cycle is required to read the value. The miss penalty is 90 cycles for data cache, 100 for I-cache. 22% of the instructions on this RISC machine are LW or SW instructions, the only instructions that access data memory. A cycle is 0.5ns. What is the average memory access time?

**miss rate of I-cache = 1.2% = 0.012**

**miss rate of D-cache = 3.4% = 0.034**

**Access time for I-cache = 1 cycle = 0.5ns**

**Access time for D-cache = 2 cycles = 1ns**

**Miss penalty for D-cache = 90 cycles**

**Miss penalty for I-cache = 100 cycles**

**Branch instructions = 22%**

**Non-branch instruction = 78%**

**Average access time = access time + miss rate \* miss penalty**

**Average access time for I-cache = 0.5 + 0.012 \* 100 = 1.7 ns**

**Average access time for D-cache = 1 + 0.034 \* 90 = 4.06 ns**

**Average memory access time = 0.22 \* 4.06 + 0.78 \* 1.7 = 2.2192 ns**