

MCAL Configuration Verification Manual for Pwm_17_GtmCcu6

32-bit TriCore™ AURIX™ TC3xx microcontroller family

About this document

Scope and purpose

This Configuration Data Reference document is applicable to all TC3xx devices in the TriCore™ AURIX™ family of 32-bit microcontrollers.

The purpose of this document is to facilitate the integrator to verify the generated code based on the input configuration parameters. This document describes details of structures, defines, macros and variables generated from the configuration parameters.

Intended audience

This document is intended for integrators who need to understand the logic of the generated configuration code of AURIX™ AUTOSAR MCAL.

Reference documents

This document should be read in conjunction with the following documents:

AURIX™ TC3xx MCAL User Manual Pwm_17_GtmCcu6

RESTRICTED

AURIX 2G Family

MCAL Configuration Verification Manual for Pwm_17_GtmCcu6



Table of contents

Table of contents

About	t this documentt	. 1
Table	of contents	. 2
1	Pwm_17_GtmCcu6 driver	. 4
1.1	File: Pwm_17_GtmCcu6_Cfg.h	4
1.1.1	Macro: PWM_17_GTMCCU6_AR_RELEASE_MAJOR_VERSION	4
1.1.2	Macro: PWM_17_GTMCCU6_AR_RELEASE_MINOR_VERSION	4
1.1.3	Macro: PWM_17_GTMCCU6_AR_RELEASE_REVISION_VERSION	
1.1.4	Macro: PWM_17_GTMCCU6_SW_MAJOR_VERSION	
1.1.5	Macro: PWM_17_GTMCCU6_SW_MINOR_VERSION	
1.1.6	Macro: PWM_17_GTMCCU6_SW_PATCH_VERSION	
1.1.7	Macro: PWM_17_GTMCCU6_SAFETY_ENABLE	
1.1.8	Macro: PWM_17_GTMCCU6_INITCHECK_API	
1.1.9	Macro: PWM_17_GTMCCU6_DE_INIT_API	
1.1.10		
1.1.11		
1.1.12		
1.1.13		
1.1.14		
1.1.15		
1.1.16		
1.1.17 1.1.18		
1.1.19		
1.1.20		
1.1.21		
1.1.22		
1.1.23		
1.1.24		
1.1.25		
1.1.26	Macro: PWM_17_GTMCCU6_MAX_CORES	.14
1.1.27	Macro: PWM_17_GTMCCU6_GTM_TIMER_USED	.14
1.1.28	Macro: PWM_17_GTMCCU6_CCU6_TIMER_USED	.15
1.1.29	Macro: Pwm_17_GtmCcu6Conf_PwmChannel_ <channel name=""></channel>	16
1.2	File: Pwm_17_GtmCcu6[_ <variant>]_PBcfg.c</variant>	.16
1.2.1	Structure: Pwm_17_GtmCcu6_Config[_ <variant>]</variant>	
1.2.1.	• = = = :	
1.2.1.2		
1.2.1.3		
1.2.2	Structure: Pwm_CoreConfigCore_ <x>[_<variant>]</variant></x>	
1.2.2.	_ 0	
1.2.2.2		
1.2.3	Structure: Pwm_kChannelConfigurationCore <x>[_<variant>]</variant></x>	
1.2.3.		
1.2.3.2		
1.2.3.3 1.2.3.4		
1.2.3.		
1.2.3.	MICHIDEL FWITHFEHOUDEIAUR	ZÕ

RESTRICTED

AURIX 2G Family



MCAL Configuration Verification Manual for Pwm_17_GtmCcu6

Table of contents

1.2.3.6	Member: PwmDutycycleDefault	28
1.2.3.7	Member: PwmShiftValue	29
1.2.3.8	Member: PwmTimerPtr	30
1.2.4	Array: Pwm_ChannelIndexMap[_ <variant>][PWM_17_GTMCCU6_MAX_CHANNELS]</variant>	30
1.2.5	Structure: Pwm_kChannelConfigGtm_Core <x> [_<variant>][<y>]</y></variant></x>	32
1.2.5.1	Member: TimerType	33
1.2.5.2	Member: TimerId	34
1.2.5.3	Member: TimerChCtrlReg	35
1.2.5.4	Member: TimerChCN0Reg	38
1.2.5.5	Member: TimerChCM0Reg	40
1.2.5.6	Member: TimerChCM1Reg	42
1.2.5.7	Member: TimerChSR0Reg	44
1.2.5.8	Member: TimerChSR1Reg	45
1.2.5.9	Member: TimerChIntEnMode	45
1.2.6	Structure: Pwm_kChannelConfigCcu6_Core <x> [_<variant>][<y>]</y></variant></x>	46
1.2.6.1	Member: TimerId	47
1.2.6.2	Member: TimerCtrlReg0	48
1.2.6.3	Member: ModCtrlReg	49
1.2.6.4	Member: PasStateLvlReg	50
1.2.6.5	Member: TimerCntReg	53
1.2.6.6	Member: TimerPeriodReg	55
1.2.6.7	Member: Ccu6ShadowReg	55
1.2.6.8	Member: TimerModeSelectReg	57
1.2.6.9	Member: PortInSelReg0	58
1.2.6.10	Member: IntEnReg	58
1.2.6.11	Member: IntNodePointerReg	59
1.3	File: Pwm_17_GtmCcu6[_ <variant>]_PBcfg.h</variant>	
1.3.1	Extern: Pwm_17_GtmCcu6_Config[_ <variant>]</variant>	61
Revision I	nistory	62

MCAL Configuration Verification Manual for Pwm_17_GtmCcu6



Pwm_17_GtmCcu6 driver

1 Pwm 17 GtmCcu6 driver

This chapter describes the details of the configuration data generated from the PWM driver.

1.1 File: Pwm_17_GtmCcu6_Cfg.h

The generated header file contains all pre-compile configuration parameters. Pre-compile time configuration allows decoupling of the static configuration from implementation. The file is generated in 'inc' folder.

1.1.1 Macro: PWM_17_GTMCCU6_AR_RELEASE_MAJOR_VERSION

Table 1 PWM_17_GTMCCU6_AR_RELEASE_MAJOR_VERSION

Name	PWM_17_GTMCCU6_AR_RELEASE_MAJOR_VERSION	
Description	Major version number of AUTOSAR release on which the Pwm_17_GtmCcu6 implementation is based on.	
Verification method	The macro is generated with the 'CommonPublishedInformation' Note: The macro is not	·
Example(s)	Action	Generated output
	Generate Pwm_17_GtmCcu6_Cfg.h file with ArMajorVersion 4	#define PWM_17_GTMCCU6_AR_RELEASE_MAJOR_VERSION (4U)

1.1.2 Macro: PWM_17_GTMCCU6_AR_RELEASE_MINOR_VERSION

Table 2 PWM_17_GTMCCU6_AR_RELEASE_MINOR_VERSION

_		
Name	PWM_17_GTMCCU6_AR_RELEASE_MINOR_VERSION	
Description	Minor version number of AUTOSAR release on which the Pwm_17_GtmCcu6 implementation is based on.	
Verification method	The macro is generated with th 'CommonPublishedInformation Note: The macro is no	•
Example(s)	Action	Generated output
	Generate Pwm_17_GtmCcu6_Cfg.h file with ArMinorVersion 2	#define PWM_17_GTMCCU6_AR_RELEASE_MINOR_VERSION (2U)

1.1.3 Macro: PWM_17_GTMCCU6_AR_RELEASE_REVISION_VERSION

Table 3 PWM_17_GTMCCU6_AR_RELEASE_REVISION_VERSION

1 4210 5	
Name	PWM_17_GTMCCU6_AR_RELEASE_REVISION_VERSION
	·

MCAL Configuration Verification Manual for Pwm_17_GtmCcu6



Pwm_17_GtmCcu6 driver

Description	Revision version number of AUTOSAR release on which the Pwm_17_GtmCcu6 implementation is based on.	
Verification method	The macro is generated with the value present in 'CommonPublishedInformation/ArPatchVersion'. Note: The macro is not user configurable.	
Example(s)	Action Generated output	
	Generate Pwm_17_GtmCcu6_Cfg.h file with ArPatchVersion 2	<pre>#define PWM_17_GTMCCU6_AR_RELEASE_REVISION_VERSION (2U)</pre>

1.1.4 Macro: PWM_17_GTMCCU6_SW_MAJOR_VERSION

Table 4 PWM_17_GTMCCU6_SW_MAJOR_VERSION

Name	PWM_17_GTMCCU6_SW_MAJOR_VERSION	
Description	Major version number of the Pwm_17_GtmCcu6 module.	
Verification method	The macro is generated with the value present in 'CommonPublishedInformation/SwMajorVersion'. Note: The macro is not user configurable.	
Example(s)	Action	Generated output
	Generate Pwm_17_GtmCcu6_Cfg.h file with SwMajorVersion 20	#define PWM_17_GTMCCU6_SW_MAJOR_VERSION (20U)

1.1.5 Macro: PWM_17_GTMCCU6_SW_MINOR_VERSION

Table 5 PWM_17_GTMCCU6_SW_MINOR_VERSION

Name	PWM_17_GTMCCU6_SW_MINOR_VERSION	
Description	Minor version number of the Pwm_17_GtmCcu6 module.	
Verification method	The macro is generated with the value present in 'CommonPublishedInformation/SwMinorVersion'. Note: The macro is not user configurable.	
Example(s)	Action Generated output	
	Generate Pwm_17_GtmCcu6_Cfg.h file with SwMinorVersion 0	#define PWM_17_GTMCCU6_SW_MINOR_VERSION (0U)

1.1.6 Macro: PWM_17_GTMCCU6_SW_PATCH_VERSION

Table 6 PWM_17_GTMCCU6_SW_PATCH_VERSION

MCAL Configuration Verification Manual for Pwm_17_GtmCcu6



Pwm_17_GtmCcu6 driver

Name	PWM_17_GTMCCU6_SW_PATCH_VERSION	
Description	Patch level version number of the Pwm_17_GtmCcu6 module.	
Verification method	The macro is generated with the value present in 'CommonPublishedInformation/SwPatchVersion'. Note: The macro is not user configurable.	
Example(s)	Action	Generated output
	Generate Pwm_17_GtmCcu6_Cfg.h file with SwPatchVersion 0	#define PWM_17_GTMCCU6_SW_PATCH_VERSION (0U)

1.1.7 Macro: PWM_17_GTMCCU6_SAFETY_ENABLE

Table 7 PWM_17_GTMCCU6_SAFETY_ENABLE

Name	PWM_17_GTMCCU6_SAFETY_ENABLE	
Description	Enables/disables safety features	
Verification method	The macro is generated as STD_ON if PwmSafetyEnable configuration parameter is set to 'True' else the macro is generated as STD_OFF.	
Example(s)	Action	Generated output
	PwmSafetyEnable = True	#define PWM_17_GTMCCU6_SAFETY_ENABLE (STD_ON)
	PwmSafetyEnable = False	<pre>#define PWM_17_GTMCCU6_SAFETY_ENABLE (STD_OFF)</pre>

1.1.8 Macro: PWM_17_GTMCCU6_INITCHECK_API

Table 8 PWM_17_GTMCCU6_INITCHECK_API

Name	PWM_17_GTMCCU6_INITCHECK_API	
Description	Enables/disables Pwm_17_GtmCcu6_InitCheck API	
Verification method	The macro is generated as STD_ON if PwmInitCheckApi configuration parameter is set to 'True' else the macro is generated as STD_OFF.	
Example(s)	Action	Generated output
	PwmInitCheckApi = True	<pre>#define PWM_17_GTMCCU6_INITCHECK_API (STD_ON)</pre>
	PwmInitCheckApi = False	<pre>#define PWM_17_GTMCCU6_INITCHECK_API (STD_OFF)</pre>

1.1.9 Macro: PWM_17_GTMCCU6_DE_INIT_API

Table 9 PWM_17_GTMCCU6_DE_INIT_API

Name	PWM_17_GTMCCU6_DE_INIT_API
Description	Decides the mode of execution of Init and DeInit API's.

MCAL Configuration Verification Manual for Pwm_17_GtmCcu6



Pwm_17_GtmCcu6 driver

Verification method	The macro is generated as STD_ON if PwmDeInitApi configuration parameter is set to 'True' else the macro is generated as STD_OFF.	
Example(s)	Action	Generated output
	PwmDeInitApi = True	<pre>#define PWM_17_GTMCCU6_DE_INIT_API (STD_ON)</pre>
	PwmDeInitApi = False	<pre>#define PWM_17_GTMCCU6_DE_INIT_API (STD_OFF)</pre>

1.1.10 Macro: PWM_17_GTMCCU6_DEV_ERROR_DETECT

Table 10 PWM_17_GTMCCU6_DEV_ERROR_DETECT

Name	PWM_17_GTMCCU6_DEV_ERROR_DETECT	
Description	Enables/disables the Development Error Detection.	
Verification method	The macro is generated as STD_ON if PwmDevErrorDetect configuration parameter is set to 'True' else the macro is generated as STD_OFF.	
Example(s)	Action	Generated output
	PwmDevErrorDetect = True	<pre>#define PWM_17_GTMCCU6_DEV_ERROR_DETECT (STD_ON)</pre>
	PwmDevErrorDetect = False	<pre>#define PWM_17_GTMCCU6_DEV_ERROR_DETECT (STD_OFF)</pre>

1.1.11 Macro: PWM_17_GTMCCU6_MULTICORE_ERROR_DETECT

Table 11 PWM_17_GTMCCU6_MULTICORE_ERROR_DETECT

Name	PWM_17_GTMCCU6_MULTICORE_ERROR_DETECT	
Description	Enables/disables MultiCore DET Check	
Verification method	The macro is generated as STD_ON if PwmMultiCoreErrorDetect configuration parameter is set to 'True' else the macro is generated as STD_OFF.	
Example(s)	Action	Generated output
	PwmMultiCoreErrorDetect = True	<pre>#define PWM_17_GTMCCU6_MULTICORE_ERROR_DETECT (STD_ON)</pre>
	PwmMultiCoreErrorDetect = False	<pre>#define PWM_17_GTMCCU6_MULTICORE_ERROR_DETECT (STD_OFF)</pre>

1.1.12 Macro: PWM_17_GTMCCU6_SET_DUTY_CYCLE_API

Table 12 PWM_17_GTMCCU6_SET_DUTY_CYCLE_API

Name	PWM_17_GTMCCU6_SET_DUTY_CYCLE_API
Description	Enables/disables Pwm_17_GtmCcu6_SetDutyCycle API
	· · · · · · · · · · · · · · · · · · ·

MCAL Configuration Verification Manual for Pwm_17_GtmCcu6



Pwm_17_GtmCcu6 driver

Verification method	•	The macro is generated as STD_ON if PwmSetDutyCycle configuration parameter is set to 'True' else the macro is generated as STD_OFF.	
Example(s) Action Generated output		Generated output	
	PwmSetDutyCycle = True	#define PWM_17_GTMCCU6_SET_DUTY_CYCLE_API (STD_ON)	
	PwmSetDutyCycle = False	<pre>#define PWM_17_GTMCCU6_SET_DUTY_CYCLE_API (STD_OFF)</pre>	

1.1.13 Macro: PWM_17_GTMCCU6_GET_OUTPUT_STATE_API

Table 13 PWM 17 GTMCCU6 GET OUTPUT STATE API

Name	PWM_17_GTMCCU6_GET_OUTPUT_STATE_API	
Description	Enables/disables Pwm_17_GtmCcu6_GetOutputState API	
Verification method	The macro is generated as STD_ON if PwmGetOutputState configuration parameter is set to 'True' else the macro is generated as STD_OFF.	
Example(s)	Action	Generated output
	PwmGetOutputState = True	#define PWM_17_GTMCCU6_GET_OUTPUT_STATE_API (STD_ON)
	PwmGetOutputState = False	#define PWM_17_GTMCCU6_GET_OUTPUT_STATE_API (STD_OFF)

1.1.14 Macro: PWM_17_GTMCCU6_SET_OUTPUT_TO_IDLE_API

Table 14 PWM_17_GTMCCU6_SET_OUTPUT_TO_IDLE_API

Name	PWM_17_GTMCCU6_SET_OUTPUT_TO_IDLE_API	
Description	Enables/disables Pwm_17_GtmCcu6_SetOutputToIdle API	
Verification method	The macro is generated as STD_ON if PwmSetOutputToIdle configuration parameter is set to 'True' else the macro is generated as STD_OFF.	
Example(s)	Action	Generated output
	PwmSetOutputToIdle = True	#define PWM_17_GTMCCU6_SET_OUTPUT_TO_IDLE_API (STD_ON)
	PwmSetOutputToIdle = False	<pre>#define PWM_17_GTMCCU6_SET_OUTPUT_TO_IDLE_API (STD_OFF)</pre>

MCAL Configuration Verification Manual for Pwm_17_GtmCcu6



Pwm_17_GtmCcu6 driver

1.1.15 Macro: PWM_17_GTMCCU6_VERSION_INFO_API

Table 15 PWM_17_GTMCCU6_VERSION_INFO_API

Name	PWM_17_GTMCCU6_VERSION_INFO_API	
Description	Enables/disables Pwm_17_GtmCcu6_GetVersionInfo API	
Verification method	The macro is generated as STD_ON if PwmVersionInfoApi configuration parameter is set to 'True' else the macro is generated as STD_OFF.	
Example(s) Action Generated output		Generated output
	PwmVersionInfoApi = True	<pre>#define PWM_17_GTMCCU6_VERSION_INFO_API (STD_ON)</pre>
	PwmVersionInfoApi = False	<pre>#define PWM_17_GTMCCU6_VERSION_INFO_API (STD_OFF)</pre>

1.1.16 Macro: PWM_17_GTMCCU6_SET_PERIOD_AND_DUTY_API

Table 16 PWM_17_GTMCCU6_SET_PERIOD_AND_DUTY_API

· · · · · · · · · · · · · · · · · · ·		
Name	PWM_17_GTMCCU6_SET_PERIOD_AND_DUTY_API	
Description	Enables/disables Pwm_17_GtmCcu6_SetPeriodAndDuty API	
Verification method	The macro is generated as STD_ON if PwmSetPeriodAndDuty configuration parameter is set to 'True' else the macro is generated as STD_OFF.	
Example(s) Action Generated output		Generated output
	PwmSetPeriodAndDuty = True	#define PWM_17_GTMCCU6_SET_PERIOD_AND_DUTY_API (STD_ON)
	PwmSetPeriodAndDuty = False	<pre>#define PWM_17_GTMCCU6_SET_PERIOD_AND_DUTY_API (STD_OFF)</pre>

1.1.17 Macro: PWM_17_GTMCCU6_HANDLE_SHIFT_BY_OFFSET

Table 17 PWM_17_GTMCCU6_HANDLE_SHIFT_BY_OFFSET

Name	PWM_17_GTMCCU6_HANDLE_SHIFT_BY_OFFSET	
Description	Enable/disable the handling of Shifted channel by offset	
Verification method	The macro is generated as STD_ON if PwmHandleShiftByOffset configuration parameter is set to 'True' else the macro is generated as STD_OFF.	
Example(s) Action Generated output		Generated output
	PwmHandleShiftByOffset = True	#define PWM_17_GTMCCU6_HANDLE_SHIFT_BY_OFFSET (STD_ON)
	PwmHandleShiftByOffset = False	#define PWM_17_GTMCCU6_HANDLE_SHIFT_BY_OFFSET (STD_OFF)

MCAL Configuration Verification Manual for Pwm_17_GtmCcu6



Pwm_17_GtmCcu6 driver

1.1.18 Macro: PWM_17_GTMCCU6_NOTIFICATION_SUPPORTED

Table 18 PWM_17_GTMCCU6_NOTIFICATION_SUPPORTED

Name	PWM_17_GTMCCU6_NOTIFICATION_SUPPORTED	
Description	Enable/disable following APIs:	
	Pwm_17_GtmCcu6_EnableNot	ification
	Pwm_17_GtmCcu6_DisableNotification	
Verification method	The macro is generated as STD_ON if PwmNotificationSupported configuration parameter is set to 'True' else the macro is generated as STD_OFF.	
Example(s)	Action	Generated output
	PwmNotificationSupported = True	#define PWM_17_GTMCCU6_NOTIFICATION_SUPPORTED (STD_ON)
	PwmNotificationSupported = False	<pre>#define PWM_17_GTMCCU6_NOTIFICATION_SUPPORTED (STD_OFF)</pre>

1.1.19 Macro: PWM_17_GTMCCU6_NOTIF_FOR_100_0_ENABLE

Table 19 PWM_17_GTMCCU6_NOTIF_FOR_100_0_ENABLE

Table 13 PWN	1_11_01MCC00_NOTIF_FOK_100_0	_ LIANDEE
Name	PWM_17_GTMCCU6_NOTIF_FOR_100_0_ENABLE	
Description	Enable/disable notification for 0% and 100% duty for variable and fixed period channels	
Verification method	 The macro is generated As STD_ON, if PwmNotificationSupported configuration parameter is set to 'True' at PwmEnable0Or100DutyNotification configuration parameter is set to 'True'. As STD_OFF, if PwmNotificationSupported configuration parameter is set to 'True' and PwmEnable0Or100DutyNotification configuration parameter is set to 'False'. As STD_OFF, if PwmNotificationSupported configuration parameter is set to 'False'. 	
Example(s)	 Action PwmNotificationSupported = True PwmEnable0Or100DutyNot ification = True 	#define PWM_17_GTMCCU6_NOTIF_FOR_100_0_ENABLE (STD_ON)
	 PwmNotificationSupported = True PwmEnable0Or100DutyNot ification = False 	<pre>#define PWM_17_GTMCCU6_NOTIF_FOR_100_0_ENABLE (STD_OFF)</pre>

1.1.20 Macro: PWM_17_GTMCCU6_DUTYCYCLE_UPDATED_ENDPERIOD

MCAL Configuration Verification Manual for Pwm_17_GtmCcu6



Pwm_17_GtmCcu6 driver

Name	PWM_17_GTMCCU6_DUTYCYCLE_UPDATED_ENDPERIOD		
Description	Enables/disables the update of	Enables/disables the update of duty at the end period	
Verification method	 The macro is generated As STD_ON, if PwmChannelCoherentSelection configuration parameter is set to 'False' and PwmDutycycleUpdatedEndperiod configuration parameter is set to 'False' and PwmChannelCoherentSelection configuration parameter is set to 'False' and PwmDutycycleUpdatedEndperiod configuration parameter is set to 'False'. As STD_OFF, if PwmChannelCoherentSelection configuration parameter is set to 'True' 		
Example(s)	Action	Generated output	
	 PwmChannelCoherentSele ction = False PwmDutycycleUpdatedEnd period = True 	#define PWM_17_GTMCCU6_DUTYCYCLE_UPDATED_ENDPER IOD (STD_ON)	
	 PwmChannelCoherentSele ction = False PwmDutycycleUpdatedEnd period = False 	#define PWM_17_GTMCCU6_DUTYCYCLE_UPDATED_ENDPER IOD (STD_OFF)	

1.1.21 Macro: PWM_17_GTMCCU6_DUTY_PERIOD_UPDATED_ENDPERIOD

Table 21 PWM_17_GTMCCU6_DUTY_PERIOD_UPDATED_ENDPERIOD

Name	PWM_17_GTMCCU6_DUTY_PER	PWM_17_GTMCCU6_DUTY_PERIOD_UPDATED_ENDPERIOD	
Description	Enables the update of period a	Enables the update of period and duty at the end period for variable period channel	
Verification method	 The macro is generated As STD_ON, if PwmChannelCoherentSelection configuration parameter is set to 'False' and PwmPeriodUpdatedEndperiod configuration parameter is set to 'True'. As STD_OFF, if PwmChannelCoherentSelection configuration parameter is set to 'False' and PwmPeriodUpdatedEndperiod configuration parameter is set to 'False'. As STD_OFF, if PwmChannelCoherentSelection configuration parameter is set to 'True' 		
Example(s)	Action	Generated output	
,		dellerated output	
	 PwmChannelCoherentSele ction = False PwmPeriodUpdatedEndper iod = True 	#define PWM_17_GTMCCU6_DUTY_PERIOD_UPDATED_ENDP ERIOD (STD_ON)	

MCAL Configuration Verification Manual for Pwm_17_GtmCcu6



Pwm_17_GtmCcu6 driver

1.1.22 Macro: PWM_17_GTMCCU6_DUTY_SHIFT_IN_TICKS

Table 22 PWM_17_GTMCCU6_DUTY_SHIFT_IN_TICKS

Name	PWM_17_GTMCCU6_DUTY_SHIFT_IN_TICKS	
Description	Enables the user to enter the duty cycle and shift value in absolute ticks, instead of percentage	
Verification method	The macro is generated as STD_ON if PwmDutyShiftInTicks configuration parameter is set to 'True' else the macro is generated as STD_OFF.	
Example(s)	Action	Generated output
	PwmDutyShiftInTicks = True	<pre>#define PWM_17_GTMCCU6_DUTY_SHIFT_IN_TICKS (STD_ON)</pre>
	PwmDutyShiftInTicks = False	<pre>#define PWM_17_GTMCCU6_DUTY_SHIFT_IN_TICKS (STD_OFF)</pre>

1.1.23 Macro: PWM_17_GTMCCU6_INSTANCE_ID

Table 23 PWM_17_GTMCCU6_INSTANCE_ID

Name	PWM_17_GTMCCU6_INSTANC	PWM_17_GTMCCU6_INSTANCE_ID	
Description	Instance ID of PWM module	Instance ID of PWM module	
Verification method	The macro is generated as a numeric value set in the configuration parameter 'PwmIndex'		
Example(s)	Action	Generated output	
	Set PwmIndex as 0	<pre>#define PWM_17_GTMCCU6_INSTANCE_ID (0U)</pre>	
	Set PwmIndex as 170	<pre>#define PWM_17_GTMCCU6_INSTANCE_ID (170U)</pre>	

1.1.24 Macro: PWM_17_GTMCCU6_MAX_CHANNELS_CORE<x>

Table 24 PWM_17_GTMCCU6_MAX_CHANNELS_CORE<x>

Name	PWM_17_GTMCCU6_MAX_CHAI	PWM_17_GTMCCU6_MAX_CHANNELS_CORE <x></x>	
Description	PWM_17_GTMCCU6_MAX_CHAI	PWM_17_GTMCCU6_MAX_CHANNELS_CORE <x> (x ranges from 0 to 5)</x>	
Verification method	Indicates the total number of channels configured for CORE <x>. Note: Channels not assigned to any core are assigned to master core</x>		
		Note: Channels not assigned to any core are assigned to master core (ResourceMMasterCore).	
Example(s)	Action	Generated output	
	• Configure 9 PWM channels	#define	

Example(s)	Action	Generated output
	• Configure 9 PWM channels	#define
	in	PWM_17_GTMCCU6_MAX_CHANNELS_CORE0 (0U)
	Pwm/PwmChannelConfigS	 #define
	et/PwmChannel	PWM 17 GTMCCU6 MAX CHANNELS CORE1 (0U)
	(PwmChannel_0 to	#define

MCAL Configuration Verification Manual for Pwm_17_GtmCcu6



Pwm_17_GtmCcu6 driver

PwmChannel_8).	PWM_17_GTMCCU6_MAX_CHANNELS_CORE2	(OU)
ResourceMMasterCore is CORE3 in	#define PWM_17_GTMCCU6_MAX_CHANNELS_CORE3	(5U)
ResourceM/ResourceMMcal Config/ResourceMMcalConf ig_0	<pre>#define PWM_17_GTMCCU6_MAX_CHANNELS_CORE4 #define</pre>	(4U)
 Assign PwmChannel_0, PwmChannel_3, PwmChannel_6 and PwmChannel_7 with ResourceMCoreID as CORE4 in ResourceM/ResourceMMcal Config/ResourceMMcalConfig_0/ResourceMMcalCore/ ResourceMAllocation 	PWM_17_GTMCCU6_MAX_CHANNELS_CORE5	(0U)
 Do not assign rest of the PWM channels to any core. 		
Configure 4 PWM channels in Pwm/Pwm/ChannelConfigS	#define PWM_17_GTMCCU6_MAX_CHANNELS_CORE0	(OU)
Pwm/PwmChannelConfigS et/PwmChannel (PwmChannel_0 to PwmChannel_3).	<pre>#define PWM_17_GTMCCU6_MAX_CHANNELS_CORE1 #define</pre>	
Set ResourceMMasterCore as CORE1 in	PWM_17_GTMCCU6_MAX_CHANNELS_CORE2 #define	
ResourceM/ResourceMMcal Config/ResourceMMcalConf ig_0	PWM_17_GTMCCU6_MAX_CHANNELS_CORE3 #define PWM_17_GTMCCU6_MAX_CHANNELS_CORE4	
Do not assign PWM channels in any ResourceMAllocation	#define PWM_17_GTMCCU6_MAX_CHANNELS_CORE5	(OU)
• Configure 4 PWM channels in	#define PWM_17_GTMCCU6_MAX_CHANNELS_CORE0	(4U)
Pwm/PwmChannelConfigS et/PwmChannel (PwmChannel_0 to	<pre>#define PWM_17_GTMCCU6_MAX_CHANNELS_CORE1</pre>	(OU)
PwmChannel_3).	<pre>#define PWM_17_GTMCCU6_MAX_CHANNELS_CORE2</pre>	(OU)
 Assign all the channels with ResourceMCoreID as COREO in 	<pre>#define PWM_17_GTMCCU6_MAX_CHANNELS_CORE3 #define</pre>	(OU)
ResourceM/ResourceMMcal Config/ResourceMMcalConf	PWM_17_GTMCCU6_MAX_CHANNELS_CORE4 #define	(OU)
ig_0/ResourceMMcalCore/ ResourceMAllocation	PWM_17_GTMCCU6_MAX_CHANNELS_CORE5	(OU)

MCAL Configuration Verification Manual for Pwm_17_GtmCcu6



Pwm_17_GtmCcu6 driver

1.1.25 Macro: PWM_17_GTMCCU6_MAX_CHANNELS

Table 25 PWM_17_GTMCCU6_MAX_CHANNELS

Name	PWM_17_GTMCCU6_MAX_CHANNELS		
Description	Indicates the total number o	Indicates the total number of PWM channels configured	
Verification method	The macro is generated as a numeric value which corresponds to the number of elements in the list 'PwmChannelConfigSet/PwmChannel'.		
Example(s)	Action	Generated output	
	Configure 3 PWM channels in 'PwmChannelConfigSet' container (PwmChannel_0 to PwmChannel_2)	<pre>#define PWM_17_GTMCCU6_MAX_CHANNELS (3U)</pre>	
	Configure 8 PWM channels in 'PwmChannelConfigSet' container (PwmChannel_0 to PwmChannel_7)	#define PWM_17_GTMCCU6_MAX_CHANNELS (8U)	

1.1.26 Macro: PWM_17_GTMCCU6_MAX_CORES

Table 26 PWM_17_GTMCCU6_MAX_CORES

Name	PWM_17_GTMCCU6_MAX_ CORES	
Description	Indicates the total number of cores available in the device	
Verification metho	The macro is generated as a numeric value which corresponds to the number of cores available in the device Note: The macro is not user configurable.	
Example(s)	Action Generated output	
	Number of cores available for the device is 6	#define PWM_17_GTMCCU6_MAX_CORES (6U)
	Number of cores available for the device is 3	#define PWM_17_GTMCCU6_MAX_CORES (3U)

1.1.27 Macro: PWM_17_GTMCCU6_GTM_TIMER_USED

Table 27 PWM_17_GTMCCU6_GTM_TIMER_USED

Name	PWM_17_GTMCCU6_GTM_TIN	PWM_17_GTMCCU6_GTM_TIMER_USED	
Description	Indicates that GTM channel/s	Indicates that GTM channel/s are configured in PWM	
Verification method	The macro is generated as STD_ON if one or more PWM channel have PwmAssignedHwUnit configuration parameter as 'GTM' else the macro is generated as STD_OFF.		
Example(s)	Action Generated output		
	 Configure 4 PWM channels in Pwm/PwmChannelConfig 	<pre>#define PWM_17_GTMCCU6_GTM_TIMER_USED (STD_ON)</pre>	

MCAL Configuration Verification Manual for Pwm_17_GtmCcu6



Pwm_17_GtmCcu6 driver

 (PwmChannel_0 to PwmChannel_3) Assign PwmAssignedHwUnit as GTM for PwmChannel_0 and PwmChannel_3 Assign PwmAssignedHwUnit as CCU6 for PwmChannel_1 and PwmChannel_2 	
 Configure 3 PWM channels in Pwm/PwmChannelConfig Set/PwmChannel (PwmChannel_0 to PwmChannel_2) Assign PwmAssignedHwUnit as CCU6 for PwmChannel_0, PwmChannel_1 and PwmChannel_2 	<pre>#define PWM_17_GTMCCU6_GTM_TIMER_USED (STD_OFF)</pre>

1.1.28 Macro: PWM_17_GTMCCU6_CCU6_TIMER_USED

Table 28 PWM_17_GTMCCU6_CCU6_TIMER_USED

able 28 PWM_17_GTMCCU6_CCU6_TIMER_USED		
Name	PWM_17_GTMCCU6_CCU6_TIMER_USED	
Description	Indicates that CCU6 channel/s are configured in PWM	
Verification method	The macro is generated as STD_ON if one or more PWM channel have PwmAssignedHwUnit configuration parameter as 'CCU6' else the macro is generated as STD_OFF.	
Example(s)	Action Ger	nerated output
	in Pwm/PwmChannelConfigS et/PwmChannel (PwmChannel_0 to PwmChannel_3).	efine PWM_17_GTMCCU6_CCU6_TIMER_USED TD_ON)
	PwmAssignedHwUnit as GTM for PwmChannel_0 and PwmChannel_3	
	Assign PwmAssignedHwUnit as CCU6 for PwmChannel_1 and PwmChannel_2	
	Configure 3 PWM channels #de	efine PWM_17_GTMCCU6_CCU6_TIMER_USED

MCAL Configuration Verification Manual for Pwm_17_GtmCcu6



Pwm_17_GtmCcu6 driver

in Pwm/PwmChannelConfigS et/PwmChannel (PwmChannel_0 to	(STD_OFF)
PwmChannel_2) • Assign PwmAssignedHwUnit as GTM for PwmChannel_0, PwmChannel_1 and PwmChannel_2	

Macro: Pwm_17_GtmCcu6Conf_PwmChannel_<channel name> 1.1.29

Table 29	wm_17_GtmCcu6Conf_PwmChannel_ <channel name=""></channel>		
Name	Pwm_17_GtmCcu6Conf_Pwm	Pwm_17_GtmCcu6Conf_PwmChannel_ <channel name=""></channel>	
Description		The macro is the symbolic name generated for the configuration parameter 'Pwm/PwmChannelConfigSet/PwmChannel'	
Verification method		The macro is generated as a numeric value which is configured in 'Pwm/PwmChannelConfigSet/PwmChannel'. <channel name=""> is the name of the PWM channel's container name.</channel>	
Example(s)	Action	Generated output	
	 Configure 4 PWM channels in Pwm/PwmChannelConfig Set/PwmChannel. Container PwmChannel for Channel ID 0 is named TOM1. 	<pre>#define Pwm_17_GtmCcu6Conf_PwmChannel_TOM1 (0U) #define Pwm_17_GtmCcu6Conf_PwmChannel_ATOM1 (1U) #define Pwm_17_GtmCcu6Conf_PwmChannel_CCU60_1(2U)</pre>	
	 Container PwmChannel for Channel ID 1 is named ATOM1. 	<pre>#define Pwm_17_GtmCcu6Conf_PwmChannel_TOM2 (3U)</pre>	
	 Container PwmChannel for Channel ID 2 is named CCU60_1 		
	 Container PwmChannel for Channel ID 3 is named TOM2 		

File: Pwm_17_GtmCcu6[_<variant>]_PBcfg.c 1.2

The generated file contains all post-build configuration parameters. Post-build time configuration mechanism allows configurable functionality of PWM driver that is deployed as object code. The file is generated in 'src' folder.

MCAL Configuration Verification Manual for Pwm_17_GtmCcu6



Pwm_17_GtmCcu6 driver

1.2.1 Structure: Pwm_17_GtmCcu6_Config[_<variant>]

Table 30 Pwm_17_GtmCcu6_Config[_<variant>]

Table 30 PWM	_17_GtmCcu6_Config[_ <varia< th=""><th>•</th></varia<>	•
Name	Pwm_17_GtmCcu6_Config[_ <variant>]</variant>	
Туре	Pwm_17_GtmCcu6_ConfigType	
Description	Root configuration structure of PWM driver which will be used during initialization.	
Verification method	The generated structure is present in Pwm_17_GtmCcu6[_ <variant>]_PBcfg.c file. The <variant> indicates the name of the post-build variant. For a variant-aware configuration the structure name is appended with the variant name. For variant-unaware configuration <variant> is ignored.</variant></variant></variant>	
Example(s)	Action	Generated output
	Allocate all PWM channels to Core0 (variant-unaware)	<pre>const Pwm_17_GtmCcu6_ConfigType Pwm_17_GtmCcu6_Config = { { (Pwm_17_GtmCcu6_CoreConfigType*)&Pwm_CoreConfigCore0,</pre>
		};
	Allocate all PWM channels to Core0 (variant-aware. Variant name is 'Petrol')	<pre>const Pwm_17_GtmCcu6_ConfigType Pwm_17_GtmCcu6_Config_Petrol = { { (Pwm_17_GtmCcu6_CoreConfigType*)&Pwm_CoreConfigCore0_Petrol,</pre>

MCAL Configuration Verification Manual for Pwm_17_GtmCcu6



Pwm_17_GtmCcu6 driver

1.2.1.1 Member: PwmCoreAdd[PWM_17_GTMCCU6_MAX_CORES]

Table 31 PwmCoreAdd[PWM 17 GTMCCU6 MAX CORES]

Table 31 PwmCo	reAdd[PWM_17_GTMCCU6_MA	X_CORES]
Name	PwmCoreAdd[PWM_17_GTMC	CCU6_MAX_CORES]
Туре	Pwm_17_GtmCcu6_CoreConfigType*	
Description	Array of core-specific configuration.	
Verification method	The generated structure member is present in the Pwm_17_GtmCcu6_Config[_ <variant>] structure. If a Core<x> is allocated at least one channel, then the element <x> shall be generated as a pointer to Pwm_17_GtmCcu6_CoreConfigType (&Pwm_CoreConfigCore<x>) else 'NULL_PTR' is generated. (x in range 0 to 5).</x></x></x></variant>	
Example(s)	Action	Generated output
	All the PWM channels are allocated to Core 0 (variant-unaware)	{ (Pwm_17_GtmCcu6_CoreConfigType*) & Pwm_CoreConfigCoreO,
	NULL_PTR, NULL_PTR, NULL_PTR, NULL_PTR, NULL_PTR	
	All the PWM channels are allocated to Core 0 (variant-aware. Variant name is 'Petrol')	{ (Pwm_17_GtmCcu6_CoreConfigType*)&Pwm_CoreConfigCore0_Petrol, NULL_PTR, NULL_PTR, NULL_PTR, NULL_PTR, NULL_PTR, NULL_PTR,
	All the PWM channels are	{

MCAL Configuration Verification Manual for Pwm_17_GtmCcu6



Pwm_17_GtmCcu6 driver

split between all cores except Core 0. (variant-unaware)	NULL_PTR,
os.e o. (variant anaware)	(Pwm_17_GtmCcu6_CoreConfigType*)&Pwm_CoreConfigCore1,
	(Pwm_17_GtmCcu6_CoreConfigType*)&Pwm_CoreConfigCore2,
	(Pwm_17_GtmCcu6_CoreConfigType*)&Pwm_CoreConfigCore3,
	(Pwm_17_GtmCcu6_CoreConfigType*)&Pwm_CoreConfigCore4,
	(Pwm_17_GtmCcu6_CoreConfigType*)&Pwm_CoreConfigCore5
	}

1.2.1.2 Member: Pwm_ChannelIndexMap

Table 32 PwmChannelIdxmap

Name	Pwm_ChannelIndexMap		
Туре	uint8*	uint8*	
Description	Pointer to channel index map.		
Verification method	The generated structure member contains the address of Pwm_ChannelIndexMap.		
Example(s)	Action Generated output		
	Configure one or more PWM channels in	(uint8*)&Pwm_ChannelIndexMap	

1.2.1.3 Member: PwmCcu6Chldx[MCU_17_CCU6_NO_OF_KERNELS]

Table 33 PwmCcu6Chldx[MCU_17_CCU6_NO_OF_KERNELS]

Name	PwmCcu6ChIdx[MCU_17_CCU6_NO_OF_KERNELS]
Туре	uint32
Description	Channel ID of CCU6 channels for a particular kernel.
Verification method	The generated structure member contains 2 array entries with each entry corresponding to CCU6 kernel. If the PWM channel is not configured '0xFFFFFFFFU' is generated, else the channel ID of CCU6 channels are generated. The structure member is generated as a value:
	1. Value = 0
	2. Value = Value CCU60 Channel ID

MCAL Configuration Verification Manual for Pwm_17_GtmCcu6



Pwm_17_GtmCcu6 driver		
	3. Value = Value CCU61 Channel ID << 8	
	4. Value = Value CCU62 Chan	nel ID << 16
Example(s)	Action	Generated output
	 Assign CCU6 to PwmAssignedHwUnit parameter for PwmChannel_4 with PwmChannelId 3 	{ Oxffffffffu, Oxffff03ffu }
	 Assign T12 to CCU6TimerUsed parameter and Cc61 to Cc6xChannel parameter in container 'PwmChannel/CCU6CC6C onfiguration' 	
	Assign /Mcu/Mcu/McuHardwareR esourceAllocationConf_0/ McuCcu6ModuleAllocatio nConf_1 to CCU6KernelUsed parameter in container 'PwmChannel/CCU6CC6C onfiguration' for PwmChannel_4	
	 Assign CCU6 to PwmAssignedHwUnit parameter for PwmChannel_0 with PwmChannelId 1 	{ Oxffff0401U, Oxffffffffu, }
	 Assign T12 to CCU6TimerUsed parameter and Cc60 to Cc6xChannel parameter in container 'PwmChannel/CCU6CC6C onfiguration' for PwmChannel_0 	
	 Assign CCU6 to PwmAssignedHwUnit parameter for PwmChannel_4 with PwmChannelId 4 	
	Assign T12 to CCU6TimerUsed parameter and Cc61 to Cc6xChannel parameter in container	

MCAL Configuration Verification Manual for Pwm_17_GtmCcu6



Pwm_17_GtmCcu6 driver

'PwmChannel/CCU6CC6C onfiguration' for PwmChannel_4	
 Assign /Mcu/Mcu/McuHardwareR esourceAllocationConf_0/ McuCcu6ModuleAllocatio nConf_0 to CCU6KernelUsed parameter in container 'PwmChannel/CCU6CC6C onfiguration' for PwmChannel_4 and PwmChannel_0 	

1.2.2 Structure: Pwm_CoreConfigCore_<x>[_<variant>]

Table 34 Pwm_CoreConfigCore_<x>[_<variant>]

Table 34 Pwm	_CoreConfigCore_ <x>[_<variant< th=""><th>:>]</th></variant<></x>	:>]
Name	Pwm_CoreConfigCore_ <x>[_<</x>	variant>]
Туре	Pwm_17_GtmCcu6_CoreConfigType	
Description	Configuration structure which holds the channel information for Core <x>, which will be referenced in root configuration structure. (x ranges from 0 to 5)</x>	
Verification method	The generated file has this structure if at least one channel is assigned to Core <x>. <variant> indicates the name of the post-build variant. For a variant aware configuration the structure name is appended with the variant name. For variant unaware configuration <variant> is ignored.</variant></variant></x>	
Example(s)	Action	Generated output
	Configure PWM channels to Core0 (variant-unaware).	<pre>static const Pwm_17_GtmCcu6_CoreConfigType Pwm_CoreConfigCore0 = { (Pwm_17_GtmCcu6_ChannelType)8U, (const Pwm_17_GtmCcu6_ChannelConfigType*)&Pwm_k ChannelConfigurationCore0 };</pre>
	Configure 4 PWM channels to Core0 and 3 channels to Core1 (variant-aware. Variant name is 'Petrol')	<pre>static const Pwm_17_GtmCcu6_CoreConfigType Pwm_CoreConfigCore0_Petrol = { (Pwm_17_GtmCcu6_ChannelType) 4U, (const Pwm_17_GtmCcu6_ChannelConfigType*) & Pwm_k ChannelConfigurationCore0_Petrol); static const</pre>

MCAL Configuration Verification Manual for Pwm_17_GtmCcu6



Pwm_17_GtmCcu6 driver

Pwm_17_GtmCcu6_CoreConfigType
<pre>Pwm_CoreConfigCore1_Petrol =</pre>
{
(Pwm_17_GtmCcu6_ChannelType)3U,
(const
<pre>Pwm_17_GtmCcu6_ChannelConfigType*) & Pwm_k</pre>
ChannelConfigurationCore1_Petrol
};

1.2.2.1 Member: Pwm_ChannelConfigPtr

Table 35 Pwm_ChannelConfigPtr

Table 35 Pwm_C	hannelConfigPtr	
Name	Pwm_ChannelConfigPtr	
Туре	Pwm_17_GtmCcu6_ChannelConfigType *	
Description	Pointer to the base of array which stores the data of each channel configured to Core <x></x>	
Verification method	The structure member is generated with base address of array which stores the channel data of Core <x>.</x>	
Example(s)	Example(s) Action Generated output	
	Configure at least 1 PWM channel to Core0 in ResourceM/ResourceMMcalC onfig/ResourceMMcalConfig_ 0/ResourceMMcalCore/ResourceMMcalCore_0/ResourceM Allocation/ResourceMAllocation_0	<pre>(const Pwm_17_GtmCcu6_ChannelConfigType*)&Pwm_k ChannelConfigurationCore0[0]</pre>
	Configure 6 PWM channels to Core0 in ResourceM/ResourceMMcalC onfig/ResourceMMcalConfig_ 0/ResourceMMcalCore/ResourceMMcalCore_0/ResourceM Allocation/ResourceMAllocation_0	<pre>(const Pwm_17_GtmCcu6_ChannelConfigType*)&Pwm_k ChannelConfigurationCore0[0]</pre>

1.2.2.2 Member: MaxChannels

Table 36 MaxChannels

Name	MaxChannels	
Туре	Pwm_17_GtmCcu6_ChannelType	
Description	Indicates the total number of channels assigned to Core <x>.</x>	
Verification method	The structure member is generated as total number of channels allocated to CORE <x>.</x>	

MCAL Configuration Verification Manual for Pwm_17_GtmCcu6



Pwm_17_GtmCcu6 driver

	Note: Channels not a (ResourceMMas	ssigned to any core are assigned to master core sterCore).
Example(s)	Action	Generated output
	 Configure 4 PWM channels in Pwm/PwmChannelConfig Set/PwmChannel. Allocate 3 channels to Core 0. Allocate 1 channel to Core 1. Output is shown for Core 0 	3
	 Configure 14 PWM channels in Pwm/PwmChannelConfig Set/PwmChannel. Allocate 3 channels to Core 1. ResourceMMasterCore is COREO. Do not allocate rest of the channels to any core. Output is shown for Core 0 	11

1.2.3 Structure: Pwm_kChannelConfigurationCore <x>[_<variant>]

Table 1 Pwm_kChannelConfigurationCore <x>[_<variant>]

Name	Pwm_kChannelConfigurationCore <x>[_<variant>]</variant></x>	
Туре	Pwm_17_GtmCcu6_ChannelConfigType	
Description	Configuration structure which holds the channel specific information belonging to Core <x> which will be referenced in core specific configuration structure. (x ranges from 0 to 5)</x>	
Verification method	The generated file has this structure if at least one channel is assigned to Core <x>. <variant> indicates the name of the post-build variant. For a variant aware configuration the structure name is appended with the variant name. For variant unaware configuration <variant> is ignored.</variant></variant></x>	
Example(s)	s) Action Generated output	
	Configure 1 PWM channel to Core0 in ResourceM/ResourceMMcalC onfig/ResourceMMcalConfig_ 0/ResourceMMcalCore/Resou rceMMcalCore_0/ResourceMA llocation	<pre>static const Pwm_17_GtmCcu6_ChannelConfigType Pwm_kChannelConfigurationCore0[] = { { 0, /* Pwm logical channel ID */</pre>

MCAL Configuration Verification Manual for Pwm_17_GtmCcu6



Pwm_17_GtmCcu6 driver

0, /* Timer used GTM:0/CCU6:1 */
<pre>Pwm_lConfigChannel(0U,/*Channel reset from other channel or not*/ PWM_17_GTMCCU6_FIXED_PERIOD,/*ChannelCla ss*/</pre>
PWM_17_GTMCCU6_COHERENT,/*Coherency*/
<pre>PWM_17_GTMCCU6_LOW, /*channel Idle state */</pre>
PWM_17_GTMCCU6_HIGH /* channel polarity */
),
(Pwm_17_GtmCcu6_PeriodType)0xea60, /*Default Period*/
(uint32)0x1999, /*Default Duty Cycle*/
(uint32)0x0, /*Shift Value*/
<pre>(const void*)&Pwm_kChannelConfigGtm_Core0[0]</pre>
}
}

1.2.3.1 Member: PwmChanneld

Table 2 PwmChanneld

Name	PwmChanneld		
Туре	Pwm_17_GtmCcu6_ChannelType		
Description	Indicates the channel ID of a PWM channel		
Verification method	The structure member is generated as a numeric value set in the configuration parameter 'PwmChannelConfigSet/PwmChannel/PwmChannel_ <x>/PwmChannelId'. (x is the configured channel number)</x>		
Example(s)	Action	Generated output	
	Configure an PWM channel with PwmChannelId = 7 in PwmChannelConfigSet/PwmChannel_1/PwmChannel_1/PwmChannelId'		

1.2.3.2 Member: PwmTimerUsed

Table 3 PwmTimerUsed

Name	PwmTimerUsed
Туре	uint8
Description	Hardware type selected for the PWM channel.
Verification method	The structure member is generated as the hardware type selected in PwmAssignedHwUnit

MCAL Configuration Verification Manual for Pwm_17_GtmCcu6



Pwm_17_GtmCcu6 driver

Example(s)	Action	Generated output
	Configure a PWM channel	0
	with PwmAssignedHwUnit=	
	GTM in	
	Pwm/PwmChannelConfigSet	
	/PwmChannel/PwmChannel	
	_1	
	Configure a PWM channel	1
	with PwmAssignedHwUnit=	
	CCU6 in in	
	Pwm/PwmChannelConfigSet	
	/PwmChannel/PwmChannel	
	_2	

1.2.3.3 Member: PwmNotification

Table 4 PwmNotification

iable 7 PWII	inotification	
Name	PwmNotification	
Туре	Pwm_17_GtmCcu6_NotifiPtrType	
Description	Pointer to the callback functions configured by the user.	
Verification method	This structure member holds the address of the notification function.	
Example(s)	Action	Generated output
Co Ch 'No Pw /Pv _7, Th ad fur Co Ch in Pw /Pv	Configure notification for Channel 7 with 'NotifyFunction' in Pwm/PwmChannelConfigSet /PwmChannel/PwmChannel _7/PwmNotification The output will show the address of the notification function 'NotifyFunction'	<pre>#if (PWM_17_GTMCCU6_NOTIFICATION_SUPPORTED == STD_ON) (Pwm_17_GtmCcu6_NotifiPtrType) &NotifyFun ction #endif</pre>
	Configure notification for Channel 5 with '0x800012ab' in Pwm/PwmChannelConfigSet /PwmChannel/PwmChannel _5/PwmNotification	<pre>#if (PWM_17_GTMCCU6_NOTIFICATION_SUPPORTED == STD_ON) (Pwm_17_GtmCcu6_NotifiPtrType) 0x800012ab #endif</pre>

1.2.3.4 Member: PwmChannelInfo

Table 5 PwmChannelInfo

Name	PwmChannelInfo
Туре	uint16
Description	The structure member contains the information about Polarity, Idlestate, Coherency,
-	Class, Shift reset and DsadcNotif value for a PWM channel.

MCAL Configuration Verification Manual for Pwm_17_GtmCcu6



Pwm_17_GtmCcu6 driver

Verification method

The structure member is generated as a value:

- 1. Value = 0
- 2. Value = Value | PwmPolarity
- 3. Value = Value | PwmIdleState << 1
- 4. Value = Value | PwmCoherentUpdate << 2
- 5. Value = Value | PwmChannelClass << 3
- 6. Value = Value | Shift Reset << 5
- 7. Value = Value | DsadcNotif << 6
 - a. Shift Reset = 0 if (PwmHandleShiftByOffset = 'False)' &&
 (PwmChannelClass = PWM_FIXED_PERIOD_SHIFTED or
 PWM_FIXED_PERIOD_CENTER_ALIGNED)
 - b. Shift Reset = 1 if (PwmHandleShiftByOffset = 'False)' && (PwmChannelClass = PWM_FIXED_PERIOD or PWM_VARIABLE_PERIOD)
 - c. Shift Reset = 0 if (PwmHandleShiftByOffset = 'True)' && (PwmChannelClass = PWM_FIXED_PERIOD or PWM_VARIABLE_PERIOD)
 - d. Shift Reset = 1 if (PwmHandleShiftByOffset = 'True)' &&
 (PwmChannelClass = PWM_FIXED_PERIOD_SHIFTED or
 PWM_FIXED_PERIOD_CENTER_ALIGNED)

Note: The configuration parameters PwmPolarity, PwmIdleState,

 $\label{lem:pwmCoherent} PwmCoherent Update\ and\ PwmChannelClass\ are\ present\ in\ container\ `PwmChannelConfigSet/PwmChannel/PwmChannel_< x>.\ (x\ is\ the$

configured channel number)

Note: The configuration parameter PwmCoherentUpdate is available only when

 $configuration\ parameter\ PwmChannel Coherent Selection\ is\ set\ to\ `True'.$

Note: DsadcNotif is set/reset by configuration parameter

McuAtomChannelEventHandledByDsadc/

McuTomChannelEventHandledByDsadc for ATOM/TOM channels respectively. It is available only when configuration parameter

PwmNotificationSupported is set to 'True' and

Pwm/PwmChannelConfigSet/PwmChannel/PwmChannel_x/

PwmAssignedHwUnit = GTM

Example(s)	Action	Generated output
	Configure a PWM channel	Pwm_lConfigChannel(
	with PwmPolarity = PWM_HIGH,	1U, /* The notification flag to enable GTM interrupts to trigger DSADC */
	PwmIdleState = PWM_LOW,	OU,/* Channel reset from other channel or not*/
	PwmCoherentUpdate = 'True', PwmChannelClass	PWM_17_GTMCCU6_FIXED_PERIOD,/* Channel Class */
	= PWM_FIXED_PERIOD, PwmHandleShiftByOffset	PWM_17_GTMCCU6_COHERENT,/* Coherency */
	= 'True'	PWM_17_GTMCCU6_LOW, /* channel Idle
	node:ref(./GtmTimerUsed	state */
)/McuAtomChannelEvent	PWM_17_GTMCCU6_HIGH /* channel polarity

MCAL Configuration Verification Manual for Pwm_17_GtmCcu6



Pwm_17_GtmCcu6 driver

HandledByDsadc = 'True' PwmAssignedHwUnit = GTM	*/)
Configure a PWM channel with PwmPolarity = PWM_HIGH, PwmIdleState = PWM_LOW, PwmCoherentUpdate = True', PwmChannelClass = PWM_FIXED_PERIOD, PwmHandleShiftByOffset = 'True' PwmAssignedHwUnit = CCU6	Pwm_lConfigChannel(OU, /* The notification flag to enable GTM interrupts to trigger DSADC */ OU, /* Channel reset from other channel or not*/ PWM_17_GTMCCU6_FIXED_PERIOD, /* Channel Class */ PWM_17_GTMCCU6_COHERENT, /* Coherency */ PWM_17_GTMCCU6_LOW, /* channel Idle state */ PWM_17_GTMCCU6_HIGH /* channel polarity */)
Configure a PWM channel with PwmPolarity = PWM_HIGH, PwmIdleState = PWM_LOW, PwmCoherentUpdate = True', PwmChannelClass = PWM_FIXED_PERIOD, PwmHandleShiftByOffset = 'True' PwmAssignedHwUnit = CCU6	Pwm_lConfigChannel(OU, /* The notification flag to enable GTM interrupts to trigger DSADC */ OU, /* Channel reset from other channel or not*/ PWM_17_GTMCCU6_FIXED_PERIOD, /* Channel Class */ PWM_17_GTMCCU6_COHERENT, /* Coherency */ PWM_17_GTMCCU6_LOW, /* channel Idle state */ PWM_17_GTMCCU6_HIGH /* channel polarity */)
Configure a PWM channel with PwmPolarity = PWM_HIGH, PwmIdleState = PWM_HIGH, PwmCoherentUpdate = True', PwmChannelClass = PWM_VARIABLE_PERIOD, PwmHandleShiftByOffset = 'False' PwmAssignedHwUnit = PWM_SignedHwUnit = PWM_SignedHwUnit = PWMASSignedHwUnit = PWMASSigned	Pwm_lConfigChannel(OU, /* The notification flag to enable GTM interrupts to trigger DSADC */ OU, /* Channel reset from other channel or not*/ PWM_17_GTMCCU6_VARIABLE_PERIOD, /* Channel Class */ PWM_17_GTMCCU6_COHERENT, /* Coherency */ PWM_17_GTMCCU6_HIGH, /* channel Idle state */ PWM_17_GTMCCU6_HIGH /* channel polarity */)
	Configure a PWM channel with PwmPolarity = PWM_HIGH, PwmCoherentUpdate = True', PwmChannelClass = PWM_FIXED_PERIOD, PwmHandleShiftByOffset = 'True' PwmAssignedHwUnit = CCU6 Configure a PWM channel with PwmPolarity = PWM_HIGH, PwmCoherentUpdate = True', PwmChannelClass = PWM_FIXED_PERIOD, PwmHandleShiftByOffset = 'True', PwmChannelClass = PWM_FIXED_PERIOD, PwmHandleShiftByOffset = 'True' PwmAssignedHwUnit = CCU6 Configure a PWM channel with PwmPolarity = PWM_HIGH, PwmCoherentUpdate = True', PwmChannelClass = PWM_HIGH, PwmCoherentUpdate = True', PwmChanne

MCAL Configuration Verification Manual for Pwm_17_GtmCcu6



Pwm_17_GtmCcu6 driver

C	Pwm_lConfigChannel(
with PwmPolarity = PWM_LOW, PwmIdleState	1U, /* The notification flag to enable GTM interrupts to trigger DSADC */
= PWM_LOW, PwmCoherentUpdate =	<pre>1U,/* Channel reset from other channel or not*/</pre>
'False', PwmChannelClass=PWM FIXED PERIOD SHI	<pre>PWM_FIXED_PERIOD_SHIFTED,/* Channel Class */</pre>
FTED, PwmHandleShiftByOffset	PWM_17_GTMCCU6_NON_COHERENT,/* Coherency */
= 'True'	PWM_17_GTMCCU6_LOW, /* channel Idle state */
node:ref(./GtmTimerUsed)/McuTomChannelEventH andledByDsadc = 'True'	PWM_17_GTMCCU6_LOW /* channel polarity */
PwmAssignedHwUnit = GTM	

1.2.3.5 Member: PwmPeriodDefault

Table 6 PwmPeriodDefault

Name	PwmPeriodDefault		
Туре	Pwm_17_GtmCcu6_PeriodTy	pe	
Description	Default period for PWM channel		
Verification method	parameter 'PwmChannelConfigSet/Pwm configured channel number)	erated as a numeric value set in the configuration Channel/PwmChannel_ <x>/PwmPeriodDefault'. (x is the value is fixed permanently for a PWM channel configured iod type.</x>	
Example(s)	(s) Action Generated output		
	 Configure a PWM channel with PwmPeriodDefault = 60000 in'PwmChannelConfigSet/ PwmChannel/PwmChann el_0/PwmPeriodDefault 	(Pwm_17_GtmCcu6_PeriodType)0xea60, /* Default Period */	

1.2.3.6 Member: PwmDutycycleDefault

Table 7 PwmDutycycleDefault

and it is a state of the state	
Name	PwmDutycycleDefault
Туре	uint32
Description	Default duty cycle for PWM channel
Verification	The structure member is generated as a numeric value set in the configuration

MCAL Configuration Verification Manual for Pwm_17_GtmCcu6



Pwm_17_GtmCcu6 driver

method	PwmDutycycleDefault'. (x is the Note: Value of PwmDu configuration po	gSet/PwmChannel/PwmChannel_ <x>/ e configured channel number) utycycleDefault is entered as a percentage when arameter PwmDutyShiftInTicks is set to 'False', else the I as absolute ticks.</x>
Example(s)	Action	Generated output
	 Configure a PWM channel with PwmDutycycleDefault = 6553 in PwmChannelConfigSet/P wmChannel/PwmChannel _0/ PwmDutycycleDefault' Parameter PwmDutyShiftInTicks = 'True' 	(uint32)0x1999, /* Default Duty Cycle */
	 Configure a PWM channel with PwmDutycycleDefault = 6553 in PwmChannelConfigSet/P wmChannel/PwmChannel _0/ PwmDutycycleDefault' Parameter PwmDutyShiftInTicks = 'False' 	(uint32)0x2ede, /* Default Duty Cycle */

1.2.3.7 Member: PwmShiftValue

Table 8 PwmShiftValue

1,10	te: Value (Value of PwmShiftValue is entered as a percentage when configuration	
	param	neter PwmDutyShiftInTicks is set to 'False', else the value in entered olute ticks.	
No	te: Config	uration parameter PwmShiftValue is available only when	

MCAL Configuration Verification Manual for Pwm_17_GtmCcu6



Pwm_17_GtmCcu6 driver

 Configure a PWM channel with PwmShiftValue = 20 in PwmChannelConfigSet/P wmChannel/PwmChannel _0/ PwmShiftValue Parameter PwmDutyShiftInTicks = 'True' 	(uint32)0x14, /* Shift Value*/
 Configure a PWM channel with PwmShiftValue = 20 in PwmChannelConfigSet/P wmChannel/PwmChannel _0/ PwmShiftValue Parameter PwmDutyShiftInTicks = 'False' 	(uint32)0x24, /* Shift Value*/

1.2.3.8 Member: PwmTimerPtr

Table 9 PwmTimerPtr

Name	PwmTimerPtr	PwmTimerPtr	
Туре	const void*		
Description	Pointer to GTM/CCU6 timer cl	nannel information.	
Verification method	The structure member is gene specific information for a cha	erated with pointer to a structure which holds the timer nnel.	
Example(s)	Action	Generated output	
	Configure a PWM channel in Core2 with PwmAssignedHwUnit = GTM in Pwm/PwmChannelConfigSet /PwmChannel	<pre>(const void*)&Pwm_kChannelConfigGtm_Core2[2]</pre>	
	Configure a PWM channel in Core1 with PwmAssignedHwUnit = CCU6 in in Pwm/PwmChannelConfigSet /PwmChannel		

1.2.4 Array: Pwm_ChannelIndexMap[_<variant>][PWM_17_GTMCCU6_MAX_CHANNELS]

Table 10 Pwm_ChannelIndexMap[_<variant>][PWM_17_GTMCCU6_MAX_CHANNELS]

	e.m.mex.mab[m.m=1[=1e.m.eeee_mmc_e.m.m=1]	
Name	Pwm_ChannelIndexMap[_ <variant>][PWM_17_GTMCCU6_MAX_CHANNELS]</variant>	

MCAL Configuration Verification Manual for Pwm_17_GtmCcu6



Pwm_17_GtmCcu6 driver

Туре	Pwm_17_GtmCcu6_ChannelConfigType
Description	This array holds index of each configured channel within the allocated core.
Verification method	Pwm_ChannelIndexMap[<x>] = Index of (PwmChannelId = <x>) in the allocated core. <variant> indicates the name of the post-build variant. For a variant aware configuration the structure name is appended with the variant name. For variant unaware configuration <variant> is ignored.</variant></variant></x></x>
Example(s)	Action Generated output
	 Configure 5 PWM channels in Pwm/PwmChannelConfig Set/PwmChannel (PwmChannel_0 to PwmChannel_4). Assign PwmChannel_0, PwmChannel_3 and PwmChannel_4 in CORE4 with PwmChannelld = 0, 3, 4 respectively Assign PwmChannel_1, PwmChannel_2 in CORE2 with PwmChannelId = 1
	<pre>. Configure 5 PWM channels in Pwm/PwmChannelConfig Set/PwmChannel</pre>
	 Configure 9 PWM channels in Pwm/PwmChannelConfig Set/PwmChannel (PwmChannel_0 to PwmChannel_8). Assign PwmChannel_0, PwmChannel_1 and PwmChannel_2 in CORE4 with PwmChannelId = 0, 1

MCAL Configuration Verification Manual for Pwm_17_GtmCcu6



Pwm_17_GtmCcu6 driver

,2 respectively	0x0U,
 Assign PwmChannel_3, 	0x1U,
PwmChannel_4 in CORE2	0x2U,
with PwmChannelId = 4 ,3 respectively	0x3U
 Assign PwmChannel_5, PwmChannel_6 	} ;
PwmChannel_7 and PwmChannel_8 in CORE5 with PwmChannelId = 8 ,7,6,5 respectively	
 This configuration is variant-aware. Variant name is 'Petrol' 	

Structure: Pwm_kChannelConfigGtm_Core<x> [_<variant>][<y>] 1.2.5

Name	Pwm_kChannelConfigGtm_Core <x> [_<variant>][<y>]</y></variant></x>
Туре	Mcu_17_Gtm_TomAtomChConfigType
Description	The configuration data of the all PWM GTM channels belonging to a Core
Verification method	Configuration structure holds the configuration data of the <y> PWM GTM channels belonging to Core <x>. <x> ranges from 0 to 5. <y> is the total number of GTM channels configured for Core<x>. <variant> indicates the name of the post-build variant. For a variant aware configuration the structure name is appended with the variant name. For variant unaware configuration <variant> is ignored. Note: The generated file has this structure if at least one GTM channel is assigned to Core <x>.</x></variant></variant></x></y></x></x></y>
Example(s)	
Example(s)	Action Generated output

MCAL Configuration Verification Manual for Pwm_17_GtmCcu6



Pwm_17_GtmCcu6 driver

```
0x1770U, /* CM0 in ticks */
with PwmAssignedHwUnit
= GTM in
                          0x2710U, /* CM1 in ticks */
Pwm/PwmChannelConfig
                          0x1770U, /* SR0 in ticks */
Set/PwmChannel/PwmCh
                          0x2710U, /* SR1 in ticks */
annel_0
                          0x80U /* Period, Duty Interrupt and
This configuration is
                      mode*/
variant-aware. Variant
name is 'Petrol'
                        },
                          MCU_GTM_TIMER_TOM, /* Timer Type
                      (TOM/ATOM) * \overline{/}
                           /* Bit[15:8] - Module number
                      Bit[7:0] - Channel number*/
                          0x50fU,
                          0x0U, /* Channel Control Register*/
                          0x0U, /* CNO in ticks */
                          0 \times 0 U, /* CMO in ticks */
                          0 \times 0 U, /* CM1 in ticks */
                          0x0U, /* SR0 in ticks */
                          0x0U, /* SR1 in ticks */
                          0x80U /* Period, Duty Interrupt and
                      mode*/
                        },
                      };
```

1.2.5.1 Member: TimerType

Table 12 TimerType

Name	TimerType	
Туре	Mcu_17_Gtm_TimerOutType	
Description	TOM/ATOM timer type	
Verification method		erated as the GtmTimerUsed selected in //PwmChannel/PwmChannel_ <x>/GtmTimerOutputModule outModuleConfiguration_0</x>
Example(s)	Action	Generated output
	Configure a PWM channel with GtmTimerUsed = '/Mcu/Mcu/McuHardwareRes ourceAllocationConf_0/McuG tmAllocationConf_0/McuG tmAtomChannelAllocationCo nf_1' in Pwm/PwmChannelConfigSet /PwmChannel/PwmChannel _0/GtmTimerOutputModuleC	

MCAL Configuration Verification Manual for Pwm_17_GtmCcu6



Pwm_17_GtmCcu6 driver

onfiguration/GtmTimerOutp	
utModuleConfiguration_0	
Configure a PWM channel	MCU GTM TIMER TOM
with GtmTimerUsed =	
'/Mcu/Mcu/McuHardwareRes	
ourceAllocationConf_0/McuG	
tmAllocationConf_0/McuGtm	
TomAllocationConf_3/McuGt	
mTomChannelAllocationCon	
f_10' in	
Pwm/PwmChannelConfigSet	
/PwmChannel/PwmChannel	
_0/GtmTimerOutputModuleC	
onfiguration/GtmTimerOutp	
utModuleConfiguration_0	

1.2.5.2 Member: TimerId

Table 13 TimerId			
Name	TimerId		
Туре	Mcu_17_Gtm_TimerChIdentifierType		
Description	Consists of TOM or ATOM module ID and channel ID		
Verification method	The structure member is generated as a value: 1. Value = 0		
	2. Value = Value Channel number		
	3. Value = Value Module number << 8		
Example(s)	Action	Generated output	
	Configure a PWM channel with GtmTimerUsed = '/Mcu/Mcu/McuHardwareRes ourceAllocationConf_0/McuGtmAllocationConf_0/McuGtmAtomChannelAllocationConf_4' in Pwm/PwmChannelConfigSet /PwmChannel/PwmChannel_0/GtmTimerOutputModuleConfiguration/GtmTimerOutputModuleConfiguration_0	0×4U	
	Configure a PWM channel with GtmTimerUsed = '/Mcu/Mcu/McuHardwareRes ourceAllocationConf_0/McuGtmAllocationConf_0/McuGtmTomAllocationConf_3/McuGtmTomChannelAllocationConf_10' in	0x030AU	

MCAL Configuration Verification Manual for Pwm_17_GtmCcu6



Pwm_17_GtmCcu6 driver

Pwm/PwmChannelConfigSet
/PwmChannel/PwmChannel
_0/GtmTimerOutputModuleC
onfiguration/GtmTimerOutp
utModuleConfiguration_0

Member: TimerChCtrlReg 1.2.5.3

Table 14 TimerChCtrlReg			
Name	TimerChCtrlReg		
Туре	uint32		
Description	TOM/ATOM channel control registers value		
Verification	Channel control register is generated in this structure member as a value:		
method	1. Value = 0		
	2. Value = Value Mode		
	If GtmTimerUsed = ATOM		
	Mode = 10 (SOMP mode)		
	else		
	Mode = 00		
	3. Value = Value Polarity << 11		
	If PwmPolarity = 'PWM_HIGH'		
	Polarity = 1		
	else		
	Polarity = 0		
	4. Value = Value CLK_SRC_SR << 12		
	The configuration parameter GtmTimerClockSelect value from GTM_CONFIGURABLE_CLOCK_0 to 7 corresponds to 000 to 111 values		
	5. Value = Value RST_CCU0 << 20		
	<pre>If ((PwmChannelClass = PWM_FIXED_PERIOD_SHIFTED&&</pre>		
	PwmHandleShiftByOffset = 'False') or (PwmChannelClass =		
	PWM_FIXED_PERIOD_CENTER_ALLIGNED))		
	RST_CCU0= 1		
	Else		
	RST_CCU0 = 0		
	6. Value = Value TrigOut << 24		
	If (PwmChannelClass of Channel A= PWM_FIXED_PERIOD) && (PwmHandleShiftByOffset = 'False') &&		
	(PwmChannelClass of Channel B = PWM_FIXED_PERIOD_SHIFTED) && (PwmReferenceChannel of Channel B = Channel A)		
	TrigOut = 1		

MCAL Configuration Verification Manual for Pwm_17_GtmCcu6



Pwm_17_GtmCcu6 driver

else if (PwmChannelClass of Channel A= PWM_FIXED_PERIOD) && (PwmChannelClass of Channel B = PWM_FIXED_PERIOD_CENTER_ALLIGNED && PwmReferenceChannel of Channel B = Channel A)

TrigOut = 1

	Ingout – 1	
	else	
	TrigOut = 0	
Example(s)	Action	Generated output
Example(s)	Configure a Pwm channel in Pwm/PwmChannel/PwmChannel/PwmChannel_1/GtmTimerOutput ModuleConfiguration/Gt mTimerOutputModuleConfiguration_0 with GtmTimerUsed = /Mcu/Mcu/McuHardwareR esourceAllocationConf_0/McuGtmAtlocationConf_0/McuGtmAtomAllocationConf_0/McuGtmAtomChannelAllocationConf_0 GtmTimerClockSelect = GTM_CONFIGURABLE_CLOCK_0=1 Configure channel in Pwm/PwmChannel/PwmChannel_1 with	0x81000002U
	1. PwmPolarity = PWM_LOW	
	2. PwmChannelClass = PWM_FIXED_PERIOD	
	 Configure parameter PwmHandleShiftByOffset = True 	
	 Configure a Pwm channel in Pwm/PwmChannelConfig Set/PwmChannel/PwmCh annel_0/GtmTimerOutput ModuleConfiguration/Gt mTimerOutputModuleConfiguration_0 with GtmTimerUsed = /Mcu/Mcu/McuHardwareResourceAllocationConf_0/McuGtmAllocationConf_0 	
	/McuGtmAtomAllocationC	36 of 63 Version 2.0

AURIX 2G Family

MCAL Configuration Verification Manual for Pwm 17 GtmCcu6



Pwm_17_GtmCcu6 driver

- onf_0/McuGtmAtomChan nelAllocationConf_0
- 2. GtmTimerClockSelect =
 GTM_CONFIGURABLE_CL
 OCK 0
- Configure channel in Pwm/PwmChannelConfig Set/PwmChannel/PwmCh annel 0 with
- PwmPolarity = PWM_HIGH
- PwmChannelClass = PWM_FIXED_PERIOD
- Configure parameter
 PwmHandleShiftByOffset
 = True
 This channel is used as a

This channel is used as a reference for the shifted period channel in the below example.

 Configure a Pwm channel in Pwm/PwmChannelConfig Set/PwmChannel/PwmCh annel_2/GtmTimerOutput ModuleConfiguration/Gt mTimerOutputModuleCo

nfiguration_0 with

- GtmTimerUsed =
 /Mcu/Mcu/McuHardwareR
 esourceAllocationConf_0/
 McuGtmAllocationConf_0
 /McuGtmAtomAllocationC
 onf_0/McuGtmAtomChan
 nelAllocationConf_2
- GtmTimerClockSelect = GTM_CONFIGURABLE_CL OCK_2
- Configure channel in Pwm/PwmChannelConfig Set/PwmChannel/PwmCh annel_2 with
- 5. PwmPolarity = PWM_LOW
- PwmChannelClass = PWM_FIXED_PERIOD_SHI FTED
- Configure parameter PwmHandleShiftByOffset

0x80002002U

MCAL Configuration Verification Manual for Pwm_17_GtmCcu6



Pwm_17_GtmCcu6 driver

= True	
The Fixed period channel in the example above is taken as a reference channel for this shifted channel.	
 Configure a Pwm channel in Pwm/PwmChannelConfig Set/PwmChannel/PwmCh annel_2/GtmTimerOutput ModuleConfiguration/Gt mTimerOutputModuleConfiguration_0 with GtmTimerUsed = /Mcu/Mcu/McuHardwareR esourceAllocationConf_0/McuGtmAtlocationConf_0/McuGtmAtomAllocationConf_0/McuGtmAtomChan nelAllocationConf_2 GtmTimerClockSelect = GTM_CONFIGURABLE_CL OCK_2 Configure channel in Pwm/PwmChannelConfig Set/PwmChannel/PwmCh annel_2 with PwmPolarity = PWM_LOW PwmChannelClass = PWM_FIXED_PERIOD_SHIFTED Configure parameter 	0x80102002U
PwmHandleShiftByOffset = False The Fixed period channel in the example above is taken as a reference channel for this shifted	
channel.	

1.2.5.4 Member: TimerChCN0Reg

Table 15 TimerChCN0Reg

I UDIC 13	mereneworkeg
Name	TimerChCN0Reg





	:+22	
Туре	uint32	
Description	TOM/ATOM channel CN0 register value	
Verification method	The structure member holds the counter value of the channel. if (PwmChannelClass = PWM_FIXED_PERIOD_SHIFTED)&& (PwmHandleShiftByOffset = 'True') CN0 Value = PwmPeriodDefault - PwmShiftValue if(PwmChannelClass = PWM_FIXED_PERIOD_SHIFTED)&& (PwmHandleShiftByOffset = 'False') CN0 Value = 0 Else if(PwmChannelClass = PWM_FIXED_PERIOD_CENTER_ALLIGNED) CN0 Value = 0 Else CN0 Value = PwmPeriodDefault	
Example(s)	Action	Generated output
	 Configure channel in Pwm/PwmChannelConfig Set/PwmChannel/PwmCh annel_0 with PwmAssignedHwUnit = GTM PwmPeriodDefault = 60000 PwmChannelClass = PWM_FIXED_PERIOD 	0xea60U
	 Configure channel in Pwm/PwmChannelConfig Set/PwmChannel/PwmCh annel_2 with 	0×0U
	 PwmAssignedHwUnit = GTM 	
	 PwmPeriodDefault = 60000(of the referenced channel) PwmShiftValue = 70 	
	4. PwmChannelClass = PWM_FIXED_PERIOD_SHI FTED	
	PwmHandleShiftByOffset = 'False'	
	Configure channel in Pwm/PwmChannelConfig Set/PwmChannel/PwmCh annel_2 with	0xea1aU
	5. PwmAssignedHwUnit = GTM6. PwmPeriodDefault =	

MCAL Configuration Verification Manual for Pwm_17_GtmCcu6



Pwm_17_GtmCcu6 driver

60000 (of the referenced channel)	
7. PwmShiftValue = 70	
8. PwmChannelClass = PWM_FIXED_PERIOD_SHI FTED	
PwmHandleShiftByOffset = 'True'	

1.2.5.5 Member: TimerChCM0Reg

Table 16 TimerChCM0Reg

Name	TimerChCM0Reg		
Туре	uint32		
Description	TOM/ATOM channel CM0 register value		
Verification method	The structure member holds the period match value of the channel.		
	If (PwmChannelClass = PWM_FIXED_PERIOD or PWM_VARIABLE_PERIOD) CM0 Value = PwmPeriodDefault		
	Else If((PwmChannelClass = PWM_FIXED_PERIOD_SHIFTED)&& (PwmHandleShiftByOffset = 'False')) or (PwmChannelClass = PWM_FIXED_PERIOD_CENTER_ALLIGNED) If(PwmDutycycleDefault = 0) CM0 Value= 0xFFFF (If GtmTimerUsed = TOM) CM0 Value= 0xFFFFFF (If GtmTimerUsed = ATOM) else if (PwmDutycycleDefault = max) CM0 Value=0 else		
	CM0 Value= PwmShiftValue endif		
	else CM0 Value= PwmPeriodDefault Endif Endif		
	Author Consultation to the		

	Liidii	
Example(s)	Action	Generated output
	 Configure channel in Pwm/PwmChannelConfi Set/PwmChannel/PwmC annel_0 with 	9
	 PwmAssignedHwUnit = GTM 	
	2. PwmDutycycleDefault = 6553	
	3. PwmPeriodDefault = 60000	
	4. PwmChannelClass =	

MCAL Configuration Verification Manual for Pwm_17_GtmCcu6



PWM_FIXED_PERIOD	
 Configure channel in Pwm/PwmChannelConfig Set/PwmChannel/PwmCh annel_0 with 	0×0U
 PwmAssignedHwUnit = GTM 	
PwmDutycycleDefault = 1677215	
 PwmPeriodDefault (of the referenced channel)= 60000 	
4. PwmShiftValue = 70	
5. PwmChannelClass = PWM_FIXED_PERIOD_SHI FTED	
PwmHandleShiftByOffset = 'False'	
 Configure channel in Pwm/PwmChannelConfig Set/PwmChannel/PwmCh annel_2 with 	0xffffffU
 PwmAssignedHwUnit = GTM 	
2. PwmDutycycleDefault = 0	
 PwmPeriodDefault (of the referenced channel)= 60000 	
4. PwmShiftValue = 70	
 Pwm/PwmChannelConfig Set/PwmChannel/PwmCh annel_2/GtmTimerOutput ModuleConfiguration/Gt mTimerOutputModuleCo nfiguration_0/GtmTimerU sed GtmTimerUsed = /Mcu/Mcu/McuHardwareR esourceAllocationConf_0/ McuGtmAllocationConf_0 /McuGtmAtomAllocationC onf_0/McuGtmAtomChan nelAllocationConf_2 PwmChannelClass = 	
PWM_FIXED_PERIOD_SHI FTED • PwmHandleShiftByOffset	
= 'False'	

MCAL Configuration Verification Manual for Pwm_17_GtmCcu6



Pwm_17_GtmCcu6 driver

 Configure channel in Pwm/PwmChannelConfig Set/PwmChannel/PwmCh annel_0 with 	0xea60U
 PwmAssignedHwUnit = GTM 	
PwmDutycycleDefault = 6777	
 PwmPeriodDefault (of the referenced channel)= 60000 	
4. PwmShiftValue = 70	
PwmChannelClass = PWM_FIXED_PERIOD_SHI FTED	
PwmHandleShiftByOffset = 'True'	

1.2.5.6 Member: TimerChCM1Reg

Table 17 TimerChCM1Reg

able 17 Tilliei	CICHIRES			
Name	TimerChCM1Reg			
Туре	uint32			
Description	TOM/ATOM channel CM1 register value			
Verification method				
	If (PwmChannelClass = PWM_FIXED_PERIOD or PWM_VARIABLE_PERIOD			
	CM1 Value= ScaledDuty			
	else			
	<pre>If((PwmChannelClass = PWM_FIXED_PERIOD_SHIFTED)&&</pre>			
	(PwmHandleShiftByOffset = 'False')) or (PwmChannelClass =			
	PWM_FIXED_PERIOD_CENTER_ALLIGNED)			
	If(PwmDutycycleDefault = 0)			
	CM1 Value = 0			
	else if (PwmDutycycleDefault = max)			
	CM1 Value= 0xFFFF (If GtmTimerUsed = TOM) CM1 Value= 0xFFFFFF (If GtmTimerUsed = ATOM)			
	else			
	CM1 Value= (PwmShiftValue + ScaledDuty) %			
	PwmDutycycleDefault			
	endif			
	else			
	CM1 Value= ScaledDuty			
	Endif			
	Endif			
Example(s)	Action	Generated output		
	Configure channel in	0x1999U		

AURIX 2G Family

MCAL Configuration Verification Manual for Pwm_17_GtmCcu6



Pwm/PwmChannelConfig Set/PwmChannel/PwmCh annel_0 with 1. PwmAssignedHwUnit = GTM 2. PwmDutycycleDefault = 6553 3. PwmPeriodDefault = 66000 4. PwmChannelClass = PWM_FIXED_PERIOD • Configure channel in Pwm/PwmChannelConfig Set/PwmChannel/PwmCh annel_0 with 1. PwmAssignedHwUnit = GTM 2. PwmDutycycleDefault = 1677215 3. PwmPeriodDefault (of the referenced channel)= 60000 4. Pwm/PwmChannelConfig Set/PwmChannel/PwmCh annel_0/GtmTimerOutput ModuleConfiguration/Gt mTimerOutputModuleCo nfiguration_O/StmTimerU sed GtmTimerUsed = //Mcu/Mcu/McuHardwareR esourceAllocationConf_0 //McuGtmAtomAllocationC onf_0/McuGtmAtomChan nelAllocationConf_0 //McuGtmAtomChan nelAllocationConf_0 //McuGtmAtomChan nelAllocationConf_0 //McuGtmAtomChan nelAllocationConf_0 //McuGtmAtomChan nelAllocationConf_0 //McuGtmAtomChan nelAllocationConf_2 5. PwmShifftyalue = 70 6. PwmChannelClass = PWM_FIXED_PERIOD_SHI FTED • PwmChannelClonfig Set/PwmChannel(PwmCh annel_2 with 1. PwmAssignedHwUnit = GTM 1. PwmAssignedHwUnit = GTM		
2. PwmDutycycleDefault = 6553 3. PwmPeriodDefault = 60000 4. PwmChannelClass = PWM_FIXED_PERIOD • Configure channel in Pwm/PwmChannelConfig Set/PwmChannel/PwmCh annel_O with 1. PwmAssignedHwUnit = GTM 2. PwmDutycycleDefault = 1677215 3. PwmPeriodDefault (of the referenced channel)= 60000 4. Pwm/PwmChannelConfig Set/PwmChannel/PwmCh annel_O/GtmTimerOutput ModuleConfiguration/Gt mTimerOutputModuleCo nfiguration_O/GtmTimerU sed GtmTimerUsed = //Mcu/Mcu/Mcu/HardwareR esourceAllocationConf_0 // McuGtmAllocationConf_0 // McuGtmAllocationConf_0 // McuGtmAllocationConf_0 // McuGtmAllocationConf_2 // Experiod // Experi	Set/PwmChannel/PwmCh annel_0 with 1. PwmAssignedHwUnit =	
3. PwmPeriodDefault = 60000 4. PwmChannelClass = PWM_FIXED_PERIOD • Configure channel in Pwm/PwmChannelConfig Set/PwmChannel/PwmChannelConfig Set/PwmChannel/PwmChannel_O with 1. PwmDstycycleDefault = 1677215 3. PwmPeriodDefault (of the referenced channel_)= 60000 4. Pwm/PwmChannelConfig Set/PwmChannel/PwmChannel_O/GtmTimerOutput ModuleConfiguration/Gt mTimerOutputModuleConfiguration/Gt mTimerOutputModuleConfiguration_O/GtmTimerU sed GtmTimerUsed = /Mcu/Mcu/McuHardwareR esourceAllocationConf_O/McuGtmAtomChannelAllocationConf_O/McuGtmAtomChannelAllocationConf_O /McuGtmAtomChannelAllocationConf_O PwmChannelClass = PWM_FIXED_PERIOD_SHIFTED • PwmChannelClass = PWM_FIXED_PERIOD_SHIFTED • PwmHandleShiftByOffset = "False" • Configure channel in Pwm/PwmChannel/PwmChannel_Pwm	2. PwmDutycycleDefault =	
4. PwmChannelClass = PWM_FIXED_PERIOD • Configure channel in Pwm/PwmChannelConfig Set/PwmChannel/PwmChannel_Owith 1. PwmAssignedHwUnit = GTM 2. PwmDutycycleDefault = 1677215 3. PwmPeriodDefault (of the referenced channel)= 60000 4. Pwm/PwmChannelConfig Set/PwmChannel/PwmChannel_O/GtmTimerOutput ModuleConfiguration_O/GtmTimerOutput ModuleConfiguration_O/GtmTimerU sed GtmTimerUsed = /Mcu/Mcu/Mcu/HardwareR esourceAllocationConf_O/McuGtmAllocationConf_O/McuGtmAllocationConf_O/McuGtmAtomAllocationConf_O/McuGtmAtomAllocationConf_O/McuGtmAtomAllocationConf_O/McuGtmAtomAllocationConf_O/McuGtmAtomChannelAllocationConf_O/McuGtmAtomChannelAllocationConf_O/McuGtmAtomChannelAllocationConf_O/McuGtmAtomChannelAllocationConf_O/McuGtmAtomChannelAllocationConf_O/McuGtmAtomChannelAllocationConf_O/McuGtmAtomChannelAllocationConf_O/McuGtmAtomChannelAllocationConf_O/McuGtmAtomChannelAllocationConf_O/McuGtmAtomChannelAllocationConf_O/McuGtmAtomChannelCayemChannelOffig Set/PwmChannelOffig Set/PwmChannel/PwmChannel/PwmChannel_O	3. PwmPeriodDefault =	
Pwm/PwmChannelConfig Set/PwmChannel/PwmCh annel_0 with 1. PwmAssignedHwUnit = GTM 2. PwmDutycycleDefault = 1677215 3. PwmPeriodDefault (of the referenced channel)= 60000 4. Pwm/PwmChannelConfig Set/PwmChannel/PwmCh annel_0/GtmTimerOutput ModuleConfiguration/Gt mTimerOutputModuleCo nfiguration_0/GtmTimerU sed GtmTimerUsed = //Mcu/Mcu/Mcu/HardwareR esourceAllocationConf_0/ McuGtmAtlocationConf_0/McuGtmAtlocationConf_0/McuGtmAtomAllocationConf_0/McuGtmAtomChan nelAllocationConf_2 5. PwmShiftValue = 70 6. PwmChannelClass = PWM_FIXED_PERIOD_SHI FTED • PwmHandleShiftByOffset = 'False' • Configure channel in Pwm/PwmChannelConfig Set/PwmChannelConfig Set/PwmChannelConfig Set/PwmChannelConfig Set/PwmChannelPymCh annel_2 with 1. PwmAssignedHwUnit =	4. PwmChannelClass =	
2. PwmDutycycleDefault = 1677215 3. PwmPeriodDefault (of the referenced channel)= 60000 4. Pwm/PwmChannelConfig Set/PwmChannel/PwmCh annel_0/GtmTimerOutput ModuleConfiguration/Gt mTimerOutputModuleCo nfiguration_0/GtmTimerU sed GtmTimerUsed = /Mcu/Mcu/Mcu/HardwareR esourceAllocationConf_0 /McuGtmAllocationConf_0 /McuGtmAtomChan nelAllocationConf_0 /McuGtmAtomChan nelAllocationConf_2 5. PwmShiftValue = 70 6. PwmChannelClass = PWM_FIXED_PERIOD_SHI FTED • PwmHandleShiftByOffset = 'False' • Configure channel in Pwm/PwmChannelConfig Set/PwmChannel/PwmChannel/PwmChannel_2 with 1. PwmAssignedHwUnit =	Pwm/PwmChannelConfig Set/PwmChannel/PwmCh annel_0 with 1. PwmAssignedHwUnit =	0×FFFFFU
3. PwmPeriodDefault (of the referenced channel)= 60000 4. Pwm/PwmChannelConfig Set/PwmChannel/PwmCh annel_0/GtmTimerOutput ModuleConfiguration/Gt mTimerOutputModuleCo nfiguration_0/GtmTimerU sed GtmTimerUsed = /Mcu/Mcu/McuHardwareR esourceAllocationConf_0/ McuGtmAllocationConf_0 /McuGtmAtomAllocationC onf_0/McuGtmAtomChan nelAllocationConf_2 5. PwmShiftValue = 70 6. PwmChannelClass = PWM_FIXED_PERIOD_SHI FTED • PwmHandleShiftByOffset = 'False' • Configure channel in Pwm/PwmChannelConfig Set/PwmChannelConfig Set/PwmChannel/PwmCh annel_2 with 1. PwmAssignedHwUnit =	2. PwmDutycycleDefault =	
Set/PwmChannel/PwmCh annel_0/GtmTimerOutput ModuleConfiguration/Gt mTimerOutputModuleCo nfiguration_0/GtmTimerU sed GtmTimerUsed = /Mcu/Mcu/McuHardwareR esourceAllocationConf_0/ McuGtmAllocationConf_0 /McuGtmAtomAllocationC onf_0/McuGtmAtomChan nelAllocationConf_2 5. PwmShiftValue = 70 6. PwmChannelClass = PWM_FIXED_PERIOD_SHI FTED • PwmHandleShiftByOffset = 'False' • Configure channel in Pwm/PwmChannelConfig Set/PwmChannel/PwmCh annel_2 with 1. PwmAssignedHwUnit =	PwmPeriodDefault (of the referenced channel)=	
Pwm/PwmChannelConfig Set/PwmChannel/PwmCh annel_2 with 1. PwmAssignedHwUnit =	Set/PwmChannel/PwmCh annel_0/GtmTimerOutput ModuleConfiguration/Gt mTimerOutputModuleCo nfiguration_0/GtmTimerU sed GtmTimerUsed = /Mcu/Mcu/McuHardwareR esourceAllocationConf_0/McuGtmAllocationConf_0/McuGtmAtomAllocationC onf_0/McuGtmAtomChan nelAllocationConf_2 5. PwmShiftValue = 70 6. PwmChannelClass = PWM_FIXED_PERIOD_SHI FTED • PwmHandleShiftByOffset	
1. PwmAssignedHwUnit =	Pwm/PwmChannelConfig Set/PwmChannel/PwmCh	0×0U
	PwmAssignedHwUnit =	





Pwm_17_GtmCcu6 driver

2.	PwmDutycycleDefault = 0	
3.	PwmPeriodDefault (of the referenced channel)= 60000	
4.	PwmShiftValue = 70	
5.	PwmChannelClass = PWM_FIXED_PERIOD_SHI FTED	
•	PwmHandleShiftByOffset = 'False'	
•	Configure channel in Pwm/PwmChannelConfig Set/PwmChannel/PwmCh annel_0 with	0x0U
1.	PwmAssignedHwUnit = GTM	
2.	PwmDutycycleDefault = 6777	
3.	PwmPeriodDefault (of the referenced channel)= 60000	
4.	PwmShiftValue = 70	
5.	PwmChannelClass = PWM_FIXED_PERIOD_SHI FTED	
•	PwmHandleShiftByOffset = 'True'	

1.2.5.7 Member: TimerChSR0Reg

Table 18 TimerChSR0Reg

Name	TimerChSR0Reg	TimerChSR0Reg		
Туре	uint32	uint32		
Description	TOM/ATOM channel SR0 regist	TOM/ATOM channel SR0 register value		
Verification method	The structure member is generated as the same value as structure member TimerChCM0Reg. Note: This structure member is not configurable by user.			
Example(s)	Action	Generated output		
	Configure a PWM channel in Pwm/PwmChannelConfigSet /PwmChannel/PwmChannel _2 with PwmAssignedHwUnit = GTM for the generated value of TimerChCM0Reg = 0xea60U	0xea60U		

MCAL Configuration Verification Manual for Pwm_17_GtmCcu6



Pwm_17_GtmCcu6 driver

1.2.5.8 Member: TimerChSR1Reg

Table 19 TimerChSR1Reg

Name	TimerChSR1Reg	TimerChSR1Reg	
Туре	uint32	uint32	
Description	TOM/ATOM channel SR1 regis	ter value	
Verification method	The structure member is generated as the same value as structure member TimerChCM1Reg. Note: This structure member is not configurable by user.		
Example(s)	Action	Generated output	
	Configure a PWM channel in Pwm/PwmChannelConfigSet /PwmChannel/PwmChannel _2 with PwmAssignedHwUnit = GTM for the generated value of TimerChCM1Reg = 0x1999U	0x1999U	

1.2.5.9 Member: TimerChIntEnMode

Table 20 TimerChIntEnMode

Name	TimerChIntEnMode	
Туре	uint8	
Description	This structure member consists of TOM/ATOM channel interrupt mode and enables/disables the CCU0-CCU1 interrupts	
Verification	The structure member is generated as a value:	
method	1. Value= 0	
	2. Value = Value CCU0 interrupt enable/disable	
	a. CCU0 interrupt enable = 1	
	b. CCU0 interrupt disable = 0	
	3. Value = Value CCU1 interrupt enable/disable << 1	
	a. CCU1 interrupt enable = 1	
	b. CCU1 interrupt disable = 0	
	4. Value = Value Interrupt Mode << 7	
	a. 00-Level Mode	
	b. 01-Pulse Mode	
	c. 10- Pulse Notify Mode	
	d. 11- Single Pulse Mode	
	Note: This structure member is not user configurable. By default CCU0 and CCU1 interrupts are disabled and the interrupt mode is set to Pulse Notify Mode.	
Example(s)	Action Generated output	

MCAL Configuration Verification Manual for Pwm_17_GtmCcu6



Pwm_17_GtmCcu6 driver

Pwm/PwmChannelConfigSet /PwmChannel/PwmChannel	0x80U
_2 with PwmAssignedHwUnit = GTM	

1.2.6 Structure: Pwm_kChannelConfigCcu6_Core<x> [_<variant>][<y>]

Name	Pwm_kChannelConfigCcu6_Co	Pwm_kChannelConfigCcu6_Core <x>[_<variant>][<y>]</y></variant></x>	
Туре	Mcu_17_Ccu6_TimerConfigType		
Description	The configuration data of the all PWM CCU6 channels belonging to a Core		
Verification method	Configuration structure holds the configuration data of the <y> PWM CCU6 channels belonging to Core <x>. <x> ranges from 0 to 5. <y> is the total number of CCU6 channels configured for Core<x>. <variant> indicates the name of the post-build variant. For a variant aware configuration the structure name is appended with the variant name. For variant unaware configuration <variant> is ignored. Note: The generated file has this structure if at least one CCU6 channel is assigned to Core <x>.</x></variant></variant></x></y></x></x></y>		
Example(s)	Action	Generated output	
	 Configure 5 PWM channel to Core2 in ResourceM/ResourceMMcalC onfig_<y>/ResourceMMcalC core/ResourceMMcalCore_<y>/ResourceMAllocation</y></y> Configure 1 PWM channel with PwmAssignedHwUnit = CCU6 in in Pwm/PwmChannelConfig Set/PwmChannel Configure 4 PWM channel with PwmAssignedHwUnit = GTM in in Pwm/PwmChannelConfig Set/PwmChannel/ This configuration is variant-aware. Variant name is 'Petrol' 	[7] - T12 Operating Mode T13 - [10-8] - Timer T13 Input Clock Select [11] - Timer T13	

MCAL Configuration Verification Manual for Pwm_17_GtmCcu6



Pwm_17_GtmCcu6 driver

```
T13 - [2]
                   - Passive state level
of output COUT63*/
   0x1U,
   0x0U, /* T12/T13 counter value */
    0x0U, /* Period */
   0x0U, /* Duty */
   0x1U, /* Compare mode */
   0x0U, /* Port in select */
   0x0U, /* Interrupt enable */
    0x5U /* Interrupt node Select */
 },
```

Member: TimerId 1.2.6.1

Table 22 T	TimerId		
Name		TimerId	
Туре		Mcu_17_Ccu6_TimerChIdentif	ierType
Description		CCU6 timer channel user identifier	
Verification		The structure member is generated as a value:	
method		1. Value = 0	
		2. Value = Value CCU6Timer L	Jsed
		If CCU6TimerUsed = T1	12 , Timer value = 0
		If CCU6TimerUsed = T1	13 , Timer value = 1
		3. Value = Value CCU6Kernel	Used << 8
		The value of Kernel can be 0 or 1 depending upon the configuration parameter CCU6KernelUsed	
		4. Value = Value Cc6xChannel << 16	
		If Cc6xChannel= Cc60 , Comparator value = 0	
		If Cc6xChannel= Cc61, Comparator value = 1	
		If Cc6xChannel= Cc62, Comparator value = 2	
		If CCU6TimerUsed = T13, Comparator value = 3 Cc6xChannel, CCU6KernelUsed and CCU6TimerUsed can be configured in container Pwm/PwmChannelConfigSet/PwmChannel/PwmChannel_ <x>/CCU6CC6Configuration_CU6CC6Configuration_0.</x>	
Example(s)		Action	Generated output
		Configure a Pwm channel in Pwm/PwmChannelConfigSet /PwmChannel/PwmChannel _0/CCU6CC6Configuration/C CU6CC6Configuration_0/CCU 6KernelUsed with CCU6TimerUsed = T12	0x20000





Pwm_17_GtmCcu6 driver

 CCU6KernelUsed =	
• Cc6xChannel = Cc62	
Configure a Pwm channel in Pwm/PwmChannelConfigSet /PwmChannel/PwmChannel _0/CCU6CC6Configuration/C CU6CC6Configuration_0/CCU6KernelUsed with	
 CCU6TimerUsed = T13 CCU6KernelUsed = /Mcu/Mcu/McuHardwareFesourceAllocationConf_0/ McuCcu6ModuleAllocationConf_1 	

1.2.6.2 Member: TimerCtrlReg0

Table 23 TimerCtrlReg0

Name	TimerCtrlReg0		
Туре	uint32		
Description	CCU6 Timer channel control register 0 contents		
Verification	The structure member is generated as a value:		
method	1. Value = 0		
	2. Value = Value Timer T12 Input Clock Select		
	The configuration parameter Ccu6TimerClockSelect value from		
	CCU6_CONFIGURABLE_CLOCK_0 to 7 corresponds to 000 to 111 values.		
	3. Value = Value Timer T12 Prescaler Bit << 3		
	If CCU6TimerPrescalarEnabled = 'True', Prescalar bit = 1		
	If CCU6TimerPrescalarEnabled = 'False', Prescalar bit = 0		
	4. Value = Value T12 Operating Mode << 7		
	Operating mode is not user configurable. It is by default value is set to 0 as times always works in edge aligned mode.		
	5. Value = Value Timer T13 Input Clock Select << 8		
	The configuration parameter Ccu6TimerClockSelect value from CCU6_CONFIGURABLE_CLOCK_0 to 7 corresponds to 000 to 111 values.		
	6. Value = Value Timer T13 Prescaler Bit << 11		
	If CCU6TimerPrescalarEnabled = 'True', Prescalar bit = 1		
	If CCU6TimerPrescalarEnabled = 'False', Prescalar bit = 0		
	Ccu6TimerClockSelect and CCU6TimerPrescalarEnabled can be configured in container Pwm/PwmChannelConfigSet/PwmChannel/PwmChannel_0/CCU6CC6Configuration/CCU6CC6Configuration_0.		

MCAL Configuration Verification Manual for Pwm_17_GtmCcu6



Pwm_17_GtmCcu6 driver

Example(s)	Action	Generated output
	Configure a Pwm channel in Pwm/PwmChannelConfigSet /PwmChannel/PwmChannel _0/CCU6CC6Configuration/C CU6CC6Configuration_0/CCU 6KernelUsed with	0x9
	 CCU6TimerClockSelect = CCU6_CONFIGURABLE_C LOCK_1 	
	• CCU6TimerPrescalarEnab led = 'True'	
	• CCU6TimerUsed = T12	
	Configure a Pwm channel in Pwm/PwmChannelConfigSet /PwmChannel/PwmChannel _0/CCU6CC6Configuration/C CU6CC6Configuration_0/CCU 6KernelUsed with	0x606
	 CCU6TimerClockSelect = CCU6_CONFIGURABLE_C LOCK_6 	
	• CCU6TimerPrescalarEnab led = 'False'	
	• CCU6TimerUsed = T13	

1.2.6.3 Member: ModCtrlReg

Table 24 ModCtrlReg

Name	ModCtrlReg	ModCtrlReg		
Туре	uint32	uint32		
Description	Enables/Disables modulation	for T12 and T13 timer		
Verification	The structure member is gene	rated as a value:		
method	1. Value = 0			
	2. Value = Value Timer T12 m	nodulation value (x=0,1,2)		
	Modulation enable for	Modulation enable for CC6x channel= 01		
	Modulation disable for	Modulation disable for CC6x channel= 00		
	Modulation enable for	Modulation enable for COUT6x and CC6x channel= 11		
	3. Value = Value Timer T13 m	3. Value = Value Timer T13 modulation value << 2		
	Modulation enable = 0	1		
	Modulation disable =0	0		
Example(s)	Action	Generated output		
	Configure a Pwm channel	0x1U		
	in			
	Pwm/PwmChannelConfi			
	gSet/PwmChannel/Pwm			

MCAL Configuration Verification Manual for Pwm_17_GtmCcu6



Pwm_17_GtmCcu6 driver

Channel_0/CCU6CC6Conf	
iguration/CCU6CC6Confi	
guration_0 with	
CCU6TimerUsed = T12	
• Configure a Pwm channel	
in	
Pwm/PwmChannelConfi	
gSet/PwmChannel/Pwm	
Channel_0/CCU6CC6Conf	
iguration/CCU6CC6Confi	
guration_0 with	
Cout6xChEnable = FALSE	
• Configure a Pwm channel	0x3U
in	
Pwm/PwmChannelConfi	
gSet/PwmChannel/Pwm	
Channel_0/CCU6CC6Con	
figuration/CCU6CC6Confi	
guration_0 with	
CCU6TimerUsed = T12	
• Configure a Pwm channel	
in	
Pwm/PwmChannelConfi	
gSet/PwmChannel/Pwm	
Channel_0/CCU6CC6Con	
figuration/CCU6CC6Confi	
guration_0 with	
Cout6xChEnable = TRUE	
• Configure a Pwm channel	0x4U
in	
Pwm/PwmChannelConfi	
gSet/PwmChannel/Pwm	
Channel_0/CCU6CC6Con	
figuration/CCU6CC6Confi	
guration_0/CCU6KernelU	
sed with CCU6TimerUsed	
= T13	

1.2.6.4 Member: PasStateLvlReg

Table 25 PasStateLvlReg

Name	PasStateLvlReg	
Туре	uint32	
Description	This represents the polarity of the PWM signal	
Verification	The structure member is generated as a value:	
method	1. Value = 0	
	2. Value = Value Timer T12 polarity (x=0,1,2)	
	Polarity of COUT6x channel LOW, CC6x channel LOW = 00	
	Polarity of COUT6x channel LOW, CC6x channel HIGH = 01	

AURIX 2G Family

MCAL Configuration Verification Manual for Pwm_17_GtmCcu6



Pwm_17_GtmCcu6 driver

Polarity of COUT6x channel HIGH, CC6x channel LOW = 10 Polarity of COUT6x channel HIGH, CC6x channel HIGH = 11

3. Value = Value | Timer T13 polarity << 2

	Polarity HIGH= 01	•
	Polarity LOW =00	
Example(s)	Action	Generated output
	Configure a Pwm channel in Pwm/PwmChannelConfig Set/PwmChannel/PwmCh annel_0/CCU6CC6Configuration/CCU6CC6Configura tion_0 with CCU6TimerUsed = T12	0×1U
	Configure COUT6x channel polarity in Pwm/PwmChannelConfig Set/PwmChannel/PwmCh annel_0/CCU6CC6Configuration/CCU6CC6Configuration_0 with Cout6xChPolarity = PWM_LOW Configure CC6x channel polarity in Pwm/PwmChannelConfig Set/PwmChannel/PwmCh annel_0 with PwmPolarity = PWM_HIGH	
	 Configure a Pwm channel in Pwm/PwmChannelConfig Set/PwmChannel/PwmCh annel_0/CCU6CC6Configuration_0 with CCU6TimerUsed = T12 Configure COUT6x channel polarity in Pwm/PwmChannelConfig Set/PwmChannel/PwmCh annel_0/CCU6CC6Configuration_0 with Cout6xChPolarity = PWM_HIGH 	0×2U

AURIX 2G Family

MCAL Configuration Verification Manual for Pwm_17_GtmCcu6



 Configure CC6x channel polarity in Pwm/PwmChannelConfig Set/PwmChannel/PwmCh annel_0 with PwmPolarity = PWM_LOW 	
 Configure a Pwm channel in Pwm/PwmChannelConfig Set/PwmChannel/PwmCh annel_0/CCU6CC6Configuration/CCU6CC6Configuration_0 with CCU6TimerUsed = T12 	0x3U
 Configure COUT6x channel polarity in Pwm/PwmChannelConfig Set/PwmChannel/PwmCh annel_0/CCU6CC6Configu ration/CCU6CC6Configura tion_0 with Cout6xChPolarity = PWM_HIGH 	
 Configure CC6x channel polarity in Pwm/PwmChannelConfig Set/PwmChannel/PwmCh annel_0 with PwmPolarity = PWM_HIGH 	
 Configure a Pwm channel in Pwm/PwmChannelConfig Set/PwmChannel/PwmCh annel_0/CCU6CC6Configuration/CCU6CC6Configuration_0/CCU6KernelUsed with CCU6TimerUsed = T13 	0×4U
 Configure channel polarity in Pwm/PwmChannelConfig Set/PwmChannel/PwmCh annel_0 with PwmPolarity = PWM_HIGH 	
 Configure a Pwm channel in 	0x0U

MCAL Configuration Verification Manual for Pwm_17_GtmCcu6



Pwm_17_GtmCcu6 driver

Pwm/PwmChannelConfig
Set/PwmChannel/PwmCh
annel_0/CCU6CC6Configu
ration/CCU6CC6Configura
tion_0/CCU6KernelUsed
with CCU6TimerUsed =
T12
 Configure COUT6x channel polarity in Pwm/PwmChannelConfig Set/PwmChannel/PwmCh annel_0/CCU6CC6Configu ration/CCU6CC6Configura tion_0 with Cout6xChPolarity = PWM_LOW
Configure CC6x channel polarity in Pwm/PwmChannelConfig Set/PwmChannel/PwmCh annel_0 with PwmPolarity = PWM_LOW

1.2.6.5 Member: TimerCntReg

Table 26 TimerCntReg

Example(s)	Action	Generated output	
		or PWM_FIXED_PERIOD_SHIFTED channels PwmPeriodDefault will be nme as the PwmPeriodDefault configured for its reference channel.	
	endif		
	Value =0		
	Else		
	Va	alue = PwmPeriodDefault – ScaledShiftValue	
	else		
	Va	alue = PwmPeriodDefault – PwmShiftValue	
	If PwmDı	utyShiftInTicks = 'True'	
	If PwmChannelCla	ass = PWM_FIXED_PERIOD_SHIFTED	
Verification method		cture member is generated as the counter value:	
Description	CCU6 timer chann	CCU6 timer channel counter	
Туре	uint32		
Name	TimerCntReg		

MCAL Configuration Verification Manual for Pwm_17_GtmCcu6



Configure channel in Pwm/PwmChannelConfig Set/PwmChannel/PwmCh annel_2 with PwmAssignedHwUnit = CCU6 PwmPeriodDefault = 0 (of the referenced channel) PwmShift/Value = 0 PwmDhift/Value = 0 PwmDhift/Sulue = 0 PwmPeriodDefault = 11125(of the referenced channel) PwmShift/Sulue = 20 PwmDhift/ShiftlnTicks = 'False' Configure channel in Pwm/PwmChannelConfig Set/PwmChannelConfig Se		
Pwm/PwmChannel/Config Set/PwmChannel/PwmCh annel_2 with 1. PwmAssignedHwUnit = CCU6 2. PwmPeriodDefault = 11125(of the referenced channel) 3. PwmShiftValue = 20 4. PwmChannelClass = PWM_FIXED_PERIOD_SHI FTED • PwmDutyShiftInTicks = 'False' • Configure channel in Pwm/PwmChannelConfig Set/PwmChannel/PwmCh annel_2 with 1. PwmAssignedHwUnit = CCU6 2. PwmPeriodDefault = 11125(of the referenced channel) 3. PwmShiftValue = 20 4. PwmChannelClass = PWM_FIXED_PERIOD_SHI FTED • PwmDutyShiftInTicks =	Pwm/PwmChannelConfig Set/PwmChannel/PwmCh annel_2 with 1. PwmAssignedHwUnit = CCU6 2. PwmPeriodDefault = 0 (of the referenced channel) 3. PwmShiftValue = 0 4. PwmChannelClass = PWM_FIXED_PERIOD_SHI FTED • PwmDutyShiftInTicks =	0×0U
2. PwmPeriodDefault = 11125(of the referenced channel) 3. PwmShiftValue = 20 4. PwmChannelClass = PWM_FIXED_PERIOD_SHIFTED • PwmDutyShiftInTicks = 'False' • Configure channel in Pwm/PwmChannelConfig Set/PwmChannel/PwmCh annel_2 with 1. PwmAssignedHwUnit = CCU6 2. PwmPeriodDefault = 11125(of the referenced channel) 3. PwmShiftValue = 20 4. PwmChannelClass = PWM_FIXED_PERIOD_SHIFTED • PwmDutyShiftInTicks =	Pwm/PwmChannelConfig Set/PwmChannel/PwmCh annel_2 with 1. PwmAssignedHwUnit =	0x2b6fU
 PwmDutyShiftInTicks = 'False' Configure channel in Pwm/PwmChannelConfig Set/PwmChannel/PwmCh annel_2 with PwmAssignedHwUnit = CCU6 PwmPeriodDefault = 11125(of the referenced channel) PwmShiftValue = 20 PwmChannelClass = PWM_FIXED_PERIOD_SHIFTED PwmDutyShiftInTicks = 	 PwmPeriodDefault = 11125(of the referenced channel) PwmShiftValue = 20 PwmChannelClass = PWM_FIXED_PERIOD_SHI 	
Pwm/PwmChannelConfig Set/PwmChannel/PwmCh annel_2 with 1. PwmAssignedHwUnit = CCU6 2. PwmPeriodDefault = 11125(of the referenced channel) 3. PwmShiftValue = 20 4. PwmChannelClass = PWM_FIXED_PERIOD_SHI FTED • PwmDutyShiftInTicks =	PwmDutyShiftInTicks =	
CCU6 2. PwmPeriodDefault = 11125(of the referenced channel) 3. PwmShiftValue = 20 4. PwmChannelClass = PWM_FIXED_PERIOD_SHI FTED • PwmDutyShiftInTicks =	Pwm/PwmChannelConfig Set/PwmChannel/PwmCh	0x2b61U
11125(of the referenced channel) 3. PwmShiftValue = 20 4. PwmChannelClass = PWM_FIXED_PERIOD_SHIFTED • PwmDutyShiftInTicks =	<u> </u>	
 4. PwmChannelClass = PWM_FIXED_PERIOD_SHI FTED PwmDutyShiftInTicks = 	11125(of the referenced	
PWM_FIXED_PERIOD_SHI FTED • PwmDutyShiftInTicks =	3. PwmShiftValue = 20	
	PWM_FIXED_PERIOD_SHI	
	PwmDutyShiftInTicks = 'True'	

MCAL Configuration Verification Manual for Pwm_17_GtmCcu6



Pwm_17_GtmCcu6 driver

1.2.6.6 Member: TimerPeriodReg

Table 27 TimerPeriodReg

able 27 TimerPeriodReg			
Name	TimerPeriodReg		
Туре	uint32		
Description	CCU6 timer channel period register contents		
Verification method	The structure member is generated as the period value set in the configuration parameter PwmPeriodDefault. Note: For PWM_FIXED_PERIOD_SHIFTED channels PwmPeriodDefault will be same as the PwmPeriodDefault configured for its reference channel.		
Example(s)	Action	Generated output	
	 Configure channel in Pwm/PwmChannelConfig Set/PwmChannel/PwmCh annel_2 with PwmAssignedHwUnit = CCU6 PwmPeriodDefault = 11125 (of the referenced channel) PwmChannelClass = PWM_FIXED_PERIOD_SHI FTED 	0x2b75U	
	 Configure channel in Pwm/PwmChannelConfig Set/PwmChannel/PwmCh annel_2 with PwmAssignedHwUnit = CCU6 PwmPeriodDefault = 60 PwmChannelClass = PWM_FIXED_PERIOD 	0x3CU	

1.2.6.7 Member: Ccu6ShadowReg

Table 28 Ccu6ShadowReg

Name	Ccu6ShadowReg	
Туре	uint32	
Description	CCU6 timer channel shadow register contents	
Verification method	The structure member holds the scaled duty value: if(PwmDutyShiftInTicks = 'False') Value = ScaledDuty	
	Else	

MCAL Configuration Verification Manual for Pwm_17_GtmCcu6



	Value = Pwm	DutycycleDefault	
	Endif		
	If (PwmPeriodDefault == 0)		
	Value = 0 Endif		
	If(Value >= PwmPeri	odDefault)	
Value = PwmPeriodDefault		PeriodDefault	
	Endif		
Example(s)	Action	Generated output	
	Configure channel in	0×0U	

	If(Value >= PwmPeriodDefault)	
	Value = PwmPe	eriodDefault
Example(s)	Endif Action	Generated output
Lxample(3)	 Configure channel in Pwm/PwmChannelConfig Set/PwmChannel/PwmCh annel_2 with PwmAssignedHwUnit = CCU6 PwmPeriodDefault = 0 (of the referenced channel) PwmDutycycleDefault = 16384 PwmChannelClass = PWM_FIXED_PERIOD_SHI FTED The output is same for 	0×0U
	PwmDutyShiftInTicks = 'False' and PwmDutyShiftInTicks = 'True' since period is zero.	
	 Configure channel in Pwm/PwmChannelConfig Set/PwmChannel/PwmCh annel_2 with PwmAssignedHwUnit = CCU6 	0xbb8U
	 PwmPeriodDefault = 6000 (of the referenced channel) 	
	3. PwmDutycycleDefault = 16384	
	4. PwmChannelClass = PWM_FIXED_PERIOD_SHI FTED	
	 The output is same for PwmDutyShiftInTicks = 'False' 	
	Configure channel in	0xc8bU

MCAL Configuration Verification Manual for Pwm_17_GtmCcu6



Pwm_17_GtmCcu6 driver

Pwm/PwmChannelConfig Set/PwmChannel/PwmCh annel_2 with	
1. PwmAssignedHwUnit = CCU6	
PwmPeriodDefault = 6000 (of the referenced channel)	
3. PwmDutycycleDefault =16384	
 PwmChannelClass = PWM_FIXED_PERIOD_SHI FTED 	
 The output is same for PwmDutyShiftInTicks = 'True' 	
 Configure channel in Pwm/PwmChannelConfig Set/PwmChannel/PwmCh annel_2 with 	
PwmAssignedHwUnit = CCU6	
PwmPeriodDefault = 6000 (of the referenced channel)	
3. PwmDutycycleDefault =5515	
4. PwmChannelClass = PWM_FIXED_PERIOD_SHI FTED	
 The output is same for PwmDutyShiftInTicks = 'True' 	

1.2.6.8 Member: TimerModeSelectReg

Table 29 TimerModeSelectReg

Example(s)	Action	Generated output	
	Note: This structure member is not user configurable.		
Verification method	The structure member holds the value 1 since the timers by default work in compare mode.		
Description	CCU6 timer mode select register contents for the input kernel		
Туре	uint8		
Name	TimerModeSelectReg		

MCAL Configuration Verification Manual for Pwm_17_GtmCcu6



Pwm_17_GtmCcu6 driver

	Configure channel in Pwm/PwmChannelConfigSet	0x1U
	/PwmChannel/PwmChannel	
-	_2 with PwmAssignedHwUnit	
:	= CCU6	

1.2.6.9 Member: PortInSelReg0

Table 30 PortInSelReg0

Tuble 50 Tole	msemego			
Name	PortInSelReg0	PortInSelReg0		
Туре	uint8	uint8		
Description	Port Input Select register cont	ents for a kernel		
Verification method	The structure member holds the value 0. Note: This structure member is not user configurable.			
Example(s)	Action	Generated output		
	Configure channel in Pwm/PwmChannelConfigSet /PwmChannel/PwmChannel _2 with PwmAssignedHwUnit = CCU6	0×0U		

1.2.6.10 Member: IntEnReg

Table 31 IntEnReg

Name	IntEnReg	IntEnReg			
Туре	uint8	uint8			
Description	CCU6 timer channel interrupt	CCU6 timer channel interrupt enable register contents			
Verification method	 Value = 0 Value = Value T12 or T13 Value = Value CCU6 rising Value = Value CCU6 falling Note: This structure	 Value = Value T12 or T13 period match Value = Value CCU6 rising edge interrupt or T13 compare match << 1 Value = Value CCU6 falling edge interrupt << 2 			
Example(s)	Action	Generated output			
	Configure a pwm channel in Pwm/PwmChannelConfigSet /PwmChannel/PwmChannel _2 with PwmAssignedHwUnit = CCU6				

MCAL Configuration Verification Manual for Pwm_17_GtmCcu6



Pwm_17_GtmCcu6 driver

1.2.6.11 Member: IntNodePointerReg

Table 32 IntNodePointerReg

Table 32 IIIIIN	oueroniterkeg				
Name	IntNodePointerReg	IntNodePointerReg			
Туре	uint8	uint8			
Description	Selects Interrupt Nodes for T12 and T13 Duty and Period match.				
Verification method	 Value = 0 Value = Value Interrupt node Value = Value (Interrupt node 	The structure member is generated as a value: 1. Value = 0 2. Value = Value Interrupt node for configured T12 Comparator: Duty Match 3. Value = Value (Interrupt node for T12: Period Match) or (Interrupt node for T13: Compare Match and Period Match) << 3			
	Value = 0x0U Else If Cc6xChannel = Cc60 Value = 0x04U Else If Cc6xChannel = Cc60 Value = 0x08U Else If Cc6xChannel = Cc60 Value = 0x05U Else If Cc6xChannel = Cc60 Value = 0x09U	Value = 0x0C Else If CCU6TimerUsed = T12 If Cc6xChannel = Cc60 && highest configured comparator in T12 = Cc60 Value = 0x0U Else If Cc6xChannel = Cc60 && highest configured comparator in T12 = Cc61 Value = 0x04U Else If Cc6xChannel = Cc60 && highest configured comparator in T12 = Cc62 Value = 0x08U Else If Cc6xChannel = Cc61 && highest configured comparator in T12 = Cc61 Value = 0x05U Else If Cc6xChannel = Cc61 && highest configured comparator in T12 = Cc62 Value = 0x09U Else If Cc6xChannel = Cc62 && highest configured comparator in T12 = Cc62 Value = 0x0AU			
	Cc6xChannel and CCU6TimerUsed can be configured in container Pwm/PwmChannelConfigSet/PwmChannel/PwmChannel_ <x>/CCU6CC6Configuration_C CU6CC6Configuration_0.</x>				
Example(s)	Action Ge	enerated output			
	 Configure 2 Pwm channel in Pwm/PwmChannelConfig Set/PwmChannel PwmChannel_0 and PwmChannel_1 Configure for PwmChannel_0 CCU6TimerUsed = T12 and Cc6xChannel = Cc60 in 	4U /* Interrupt node Select */			

AURIX 2G Family

MCAL Configuration Verification Manual for Pwm_17_GtmCcu6



Pwm_17_GtmCcu6 driver

Pwm/PwmChannelConfig Set/PwmChannel/PwmCh annel_0/CCU6CC6Configu ration/CCU6CC6Configura tion_0

 Configure for PwmChannel_1 CCU6TimerUsed = T12 and Cc6xChannel = Cc61 in Pwm/PwmChannelConfig Set/PwmChannel/PwmCh annel_1/CCU6CC6Configuration/CCU6CC6Configuration_0
 The output is for

0x9U /* Interrupt node Select */

 Configure 3 Pwm channel in Pwm/PwmChannelConfig Set/PwmChannel PwmChannel_0, PwmChannel_1 and

PwmChannel_0

PwmChannel_2

 Configure for PwmChannel_0 CCU6TimerUsed = T12 and Cc6xChannel = Cc60 in

Pwm/PwmChannelConfig Set/PwmChannel/PwmCh annel_0/CCU6CC6Configu ration/CCU6CC6Configura tion_0

PwmChannel_1
CCU6TimerUsed = T12
and Cc6xChannel = Cc61
in
Pwm/PwmChannelConfig
Set/PwmChannel/PwmCh
annel_1/CCU6CC6Configu
ration/CCU6CC6Configura
tion_0

Configure for

 Configure for PwmChannel_2 CCU6TimerUsed = T12 and Cc6xChannel = Cc62

MCAL Configuration Verification Manual for Pwm_17_GtmCcu6



Pwm_17_GtmCcu6 driver

Pwm/PwmChannelConfig
Set/PwmChannel/PwmCh
annel_2/CCU6CC6Configu
ration/CCU6CC6Configura
tion_0
The output is for
PwmChannel_1

1.3 File: Pwm_17_GtmCcu6[_<variant>]_PBcfg.h

The generated file contains the extern parameter for the root configuration structure. Post-build time configuration mechanism allows configurable functionality of PWM driver that is deployed as object code. The file is generated in 'inc' folder.

1.3.1 Extern: Pwm_17_GtmCcu6_Config[_<variant>]

Table 33 Pwm_17_GtmCcu6_Config[_<variant>]

Name	Pwm_17_GtmCcu6_Config[_ <variant>]</variant>		
Туре	Pwm_17_GtmCcu6_ConfigType		
Description	Extern for root configuration structure of PWM driver which will be used during initialization.		
Verification method	The generated variable is the extern of the structure which is present in Pwm_17_GtmCcu6[_ <variant>]_PBcfg.c file. The <variant> indicates the name of the post-build variant. For a variant-aware configuration the extern variable name is appended with the variant name. For variant-unaware configuration <variant> is ignored.</variant></variant></variant>		
Example(s)	Action	Generated output	
	PWM is configured and is variant-aware. Variant name is 'Petrol'	<pre>extern const Pwm_17_GtmCcu6_ConfigType Pwm_17_GtmCcu6_Config_Petrol;</pre>	
	PWM is configured and is variant-unaware	<pre>extern const Pwm_17_GtmCcu6_ConfigType Pwm_17_GtmCcu6_Config;</pre>	

AURIX 2G Family

MCAL Configuration Verification Manual for Pwm_17_GtmCcu6



Revision history

Revision history

Major changes since the last revision

Date	Version	Description	
2021-11-08	V2.0	Document is Released	
2021-11-02	V1.1	ModCtrlReg and PasStateLvlReg in the structure Pwm_kChannelConfigCcu6_Core <x> [_<variant>][<y>] are updated with Cout6xChEnable and Cout6xChPolarity to provide COUT feature support</y></variant></x>	
2020-11-05	V1.0	Document is Released	
2020-11-04	V0.1	 - Pwm_17_GtmCcu6 driver chapter moved from MC-ISAR_TC3xx_Config_Verification_Manual_BASIC.pdf to this document - Structure member TimerChPortOutConfig is deleted from structure Pwm_kChannelConfigGtm_Core<x></x> 	

Trademarks

All referenced product or service names and trademarks are the property of their respective owners.

Edition 2021-11-08 Published by Infineon Technologies AG 81726 Munich, Germany

© 2021 Infineon Technologies AG. All Rights Reserved.

Do you have a question about this document?

Email: erratum@infineon.com

Document reference Doc_Number

IMPORTANT NOTICE

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics ("Beschaffenheitsgarantie").

With respect to any examples, hints or any typical values stated herein and/or any information regarding the application of the product, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights of any third party.

In addition, any information given in this document is subject to customer's compliance with its obligations stated in this document and any applicable legal requirements, norms and standards concerning customer's products and any use of the product of Infineon Technologies in customer's applications.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer's technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

For further information on the product, technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies office (www.infineon.com).

WARNINGS

Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies' products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury.