Phase 1: Isolated Subsystem Prototyping	Phase 2: Subsystem Integration Pairing	Phase 3: Total Subsystem Integration	Phase 4: Subsystem Integration on PCB	Phase 5: Total System Integration on PCB
-ADS Eval kit is configured to find proper biasing of amplifier to match training data -STM32 FSM subroutines are designed and tested -Power delivery tested on breadboard with DC bench supply with voltage swing -Machine learning architecture is created and tested with existing dataset -SPI comms. Established verified by logic analyzer	-ADS and STM32 SPI comm. Established -ADS and STM32 powered with simulated computational load from power delivery circuit -Machine learning model (.tflite) uploaded to STM32 aiming to classify training data gestures via USB 2.0 -Simulator demonstrates proper articulation of poses	-Breadboard power system supplies to both eval kits, EMG measurements passed to STM, inference passed to simulator -Every subsystem is now connected as demonstrated within the main block diagram	-Development of PCB for each individual subsystem, with their respective I/O, or ESD considerations accounted for. Same system setup as phase 3 -multi-layer boards for high pin IC packages -heat dissipation assemblies for packages past ambient temperature dissipation threshold	-Total integration of all subsystems on one PCB -PCB subsystems routed with considerations for additional noise and heat -added layers