Altium PCB Tutorial

Table of Contents

Introduction

This tutorial will cover setting up your new PCB design, configuring the rules and layer settings, and drawing up a board outline. Then using placement and routing methods, the printed circuit board layout begins with reference to the schematic from tutorial one.

Useful PCB Editor Hotkeys

Function	Hotkey	Context
Pan the view	Right click drag	
Zoom the view	Middle click drag	
Place Menu	P	
Rotate component	SPACE	While dragging components
Change track direction	SPACE	While placing track
Change track elbow type	SHIFT + SPACE	While placing track
Change unit type mm/mil	Q	
Select grid size	G	
Highlight net	CTRL + Left Click	
Change component layer	L	While dragging components

The **"Panels"** button in the bottom right is where most information windows and properties are accessed. So if you cannot see a particular sub-window, check Panels and enable.

"Tab" key is used to access properties of highlighted/selected items. A paused symbol will appear in the middle of the screen. Once you have finished with the "Properties" window, click the pause symbol to return and continue editing your schematic or pcb.

Starting from Templates

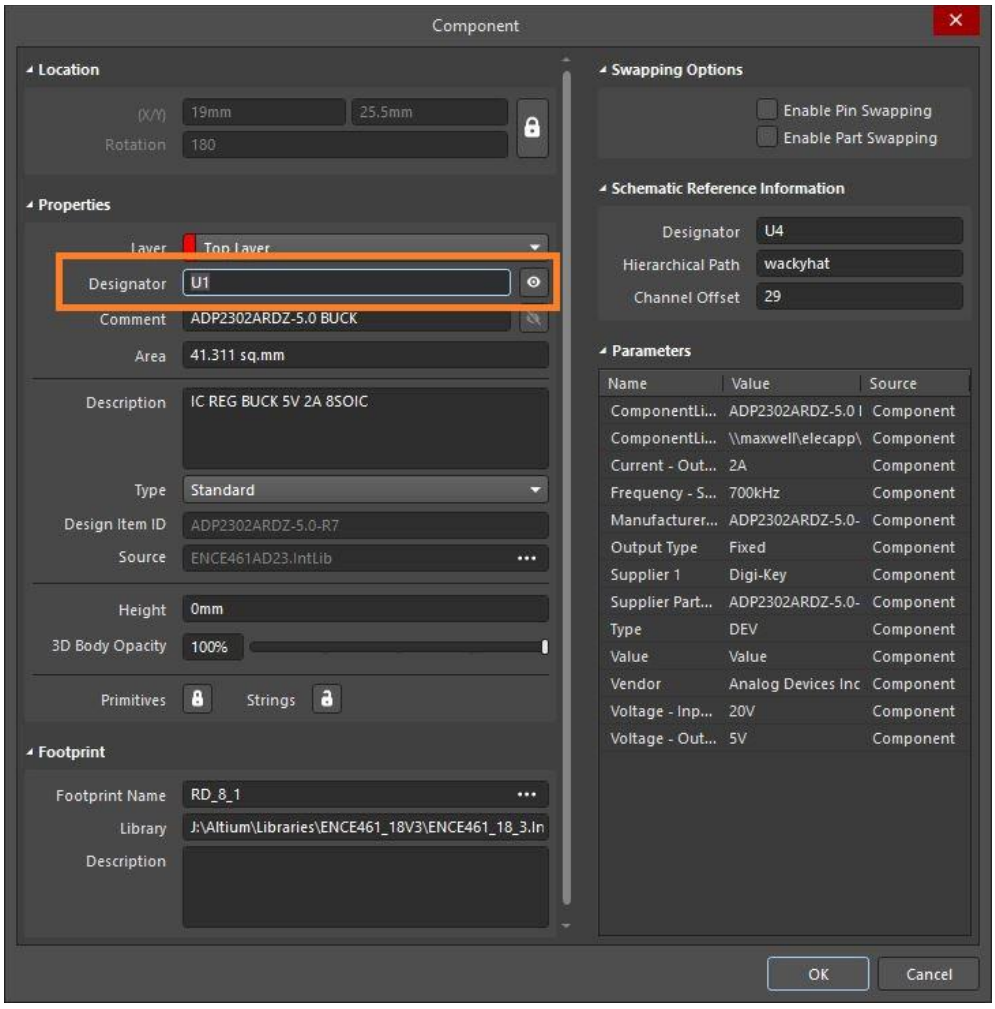
Templates

There are templates for the Wacky Racers Car and Hat PCBs located at *V:\AltiumDesigner\Templates\2026 Templates.* Copy/rename the appropriate .PcbDoc file into your project folder and add to your project, *Project->Add Existing to Project*. These files contain the board setup with a SAM4S, and all of the hard to solder packages already placed for you. Use these templates so our pre-made solder paste stencils align, and the paste can be screen printed onto these specific footprints (do not reposition locked footprints & do not alter the PCB size or modify layers).

The only thing you will need to do is manually change/match the existing footprint designators in the PCB template to the part in your schematic before importing any other components.

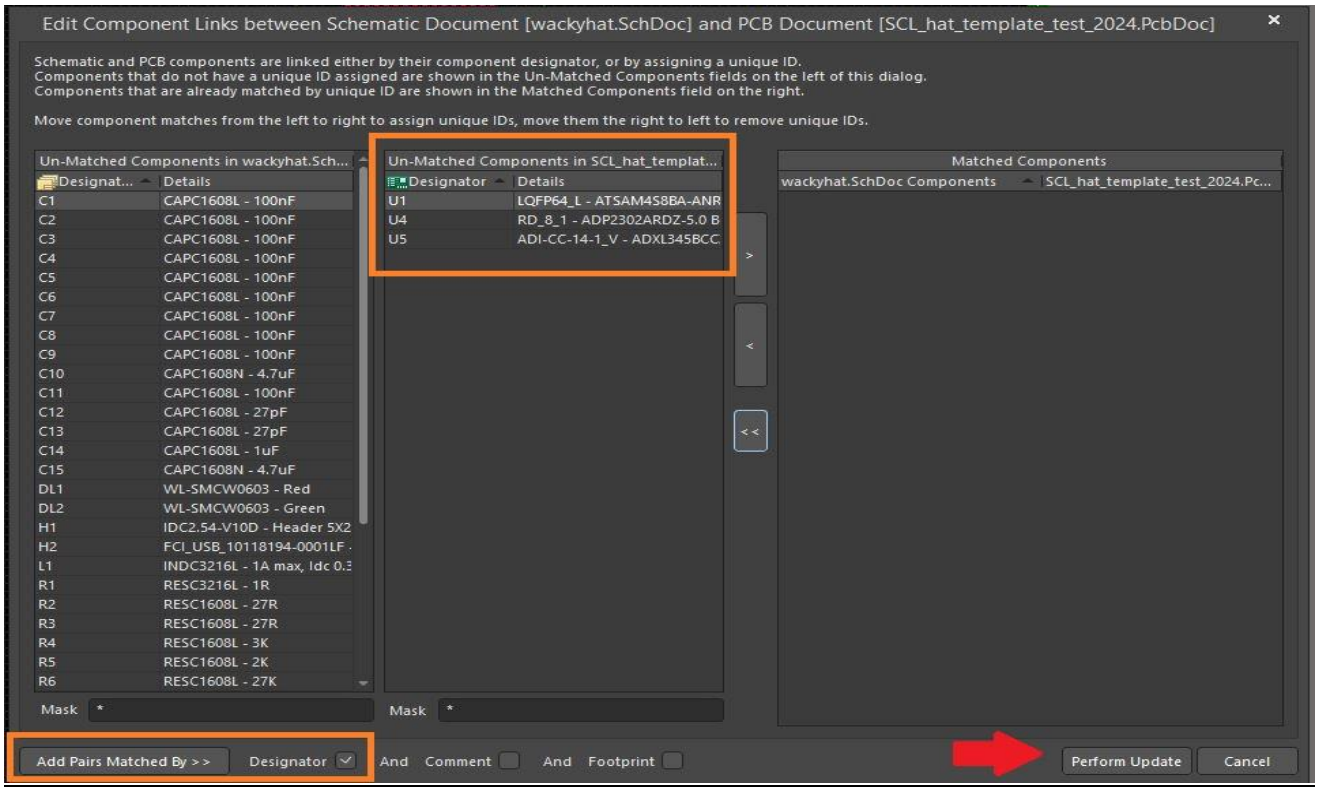
1: Identifying & note the designators in your Schematic for the SAM4S, Buck converter, H-bridge *(Car)* or Accelerometer *(Hat)*.

2: Edit the footprint designator in the pcb template by double clicking the footprint. Match it exactly to the schematic designator for reference.

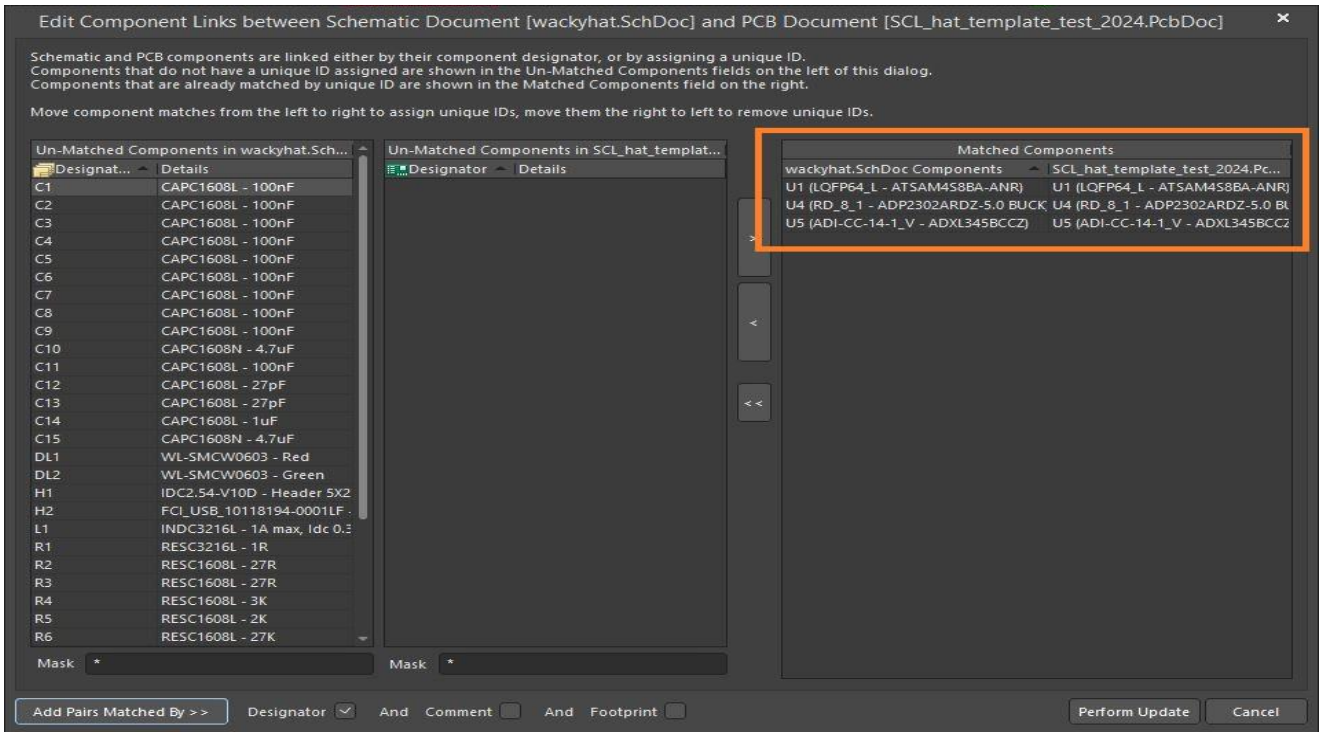


Designator U1 of the pcb footprint now matches the schematic symbol.

3: From PCB, *Project -> Component Links.* Check *Designator* box & then click *Add Pairs Matched By >>* ***Designator***. Check that only the components + 3 footprints you expect to link are listed. Then press *Perform Update.*



After the component link update the three locked footprints will be linked to your schematic symbols of the same designator (see below).

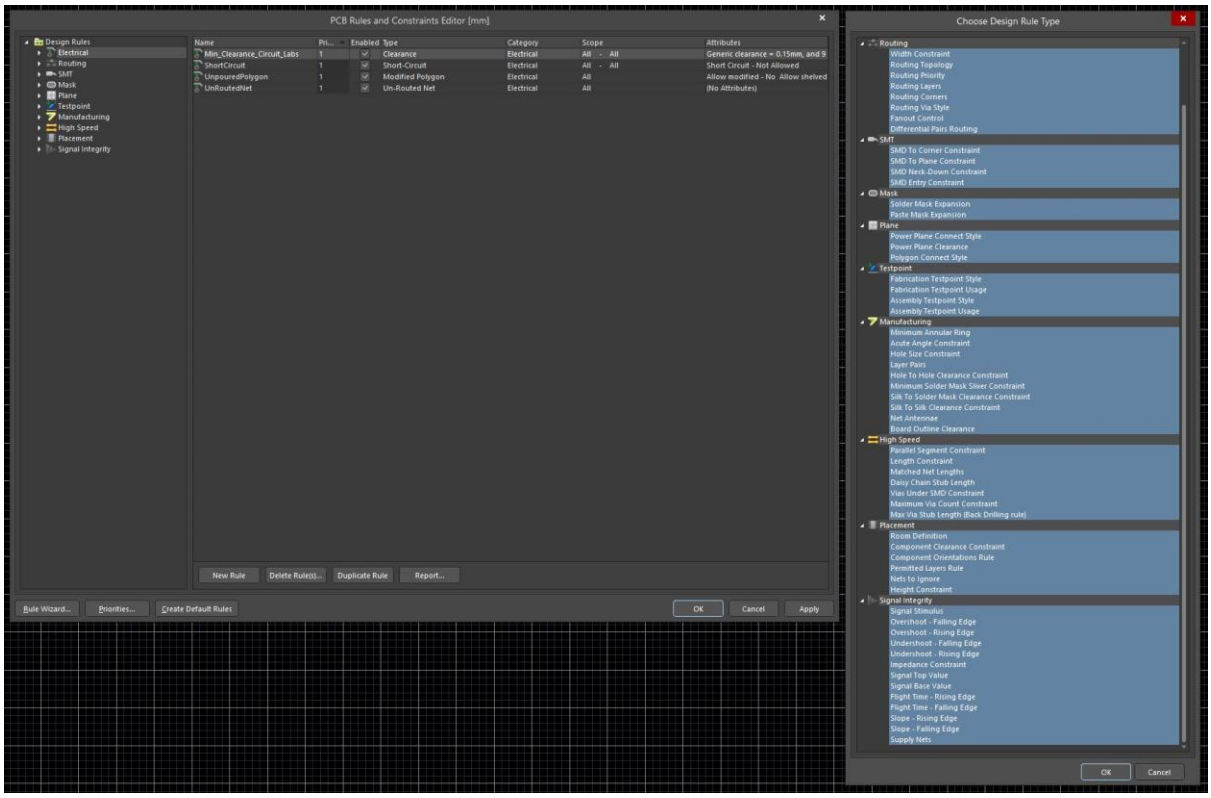


Once you have linked the above footprints in the template to the schematic, **do not** attempt to match any other nets, symbols or footprints manually.

When importing the other parts for the first time in the next sections of this tutorial, Altium will try and match what is in the file for you automatically, just click on the Automatic option.

Design Rules

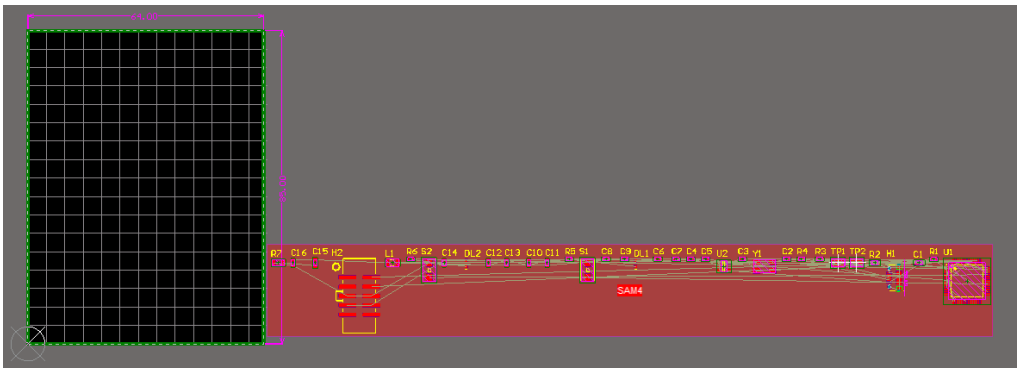
The next step is to setup the rules Altium will use to verify our designs. Bring up the *Design → Rules* window. Right click a rule in the left pane and choose *Import Rules*. We now need to select ALL of the rules in this list, do this by selecting the top rule, then shift clicking the bottom rule:



Select *OK* to bring up an *Import File* dialog. Navigate to your *Altium/Templates* directory and select the *ENCE461_20xx.RUL* file. This has the correct settings for the manufacturer we use. Select *Yes* to the confirmation then *OK* to close the PCB Rules window.

Importing your Components

We are now ready to import all of the components from your schematic design. Do this by using *Design → Import changes from …* This will present you with an Engineering Change Order (ECO). This is a tool that Altium uses to show you what changes it thinks are appropriate, allows you to validate the change without executing it, and then finally apply them. If you validate the ECO, you will see all of the "Add" actions are checked, but many others are not. This is because those actions require a specific component to exist, and as they have not yet been added (only validated) they fail. If you execute the order all of the actions should get a green tick in the done column. You can tick the "Only Show Errors" box to make sure nothing went wrong. There are a number of reasons why something here *might* go wrong so if that happens, ask a TA for assistance.

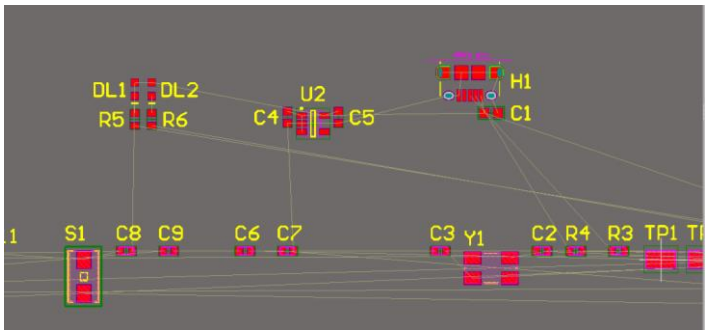


You should now see a group of your component footprints possibly inside a red box. The red box is called a room. Rooms group components from a single sheet or you can define components groups into rooms using other methods. Whilst very useful in larger designs, we will be ignoring them so just delete it. Do not move any objects prior to deleting the room(s) as this can move locked objects. Alternatively go to *Project->Project Options->Class Generation Tab* and uncheck *Generate Rooms* for all schematics listed. Remember **do not** change the template PCB size or reposition3 the locked components.

Note: the dashed line (in the middle of the thick green pcb boarder) is the true cut size of your PCB

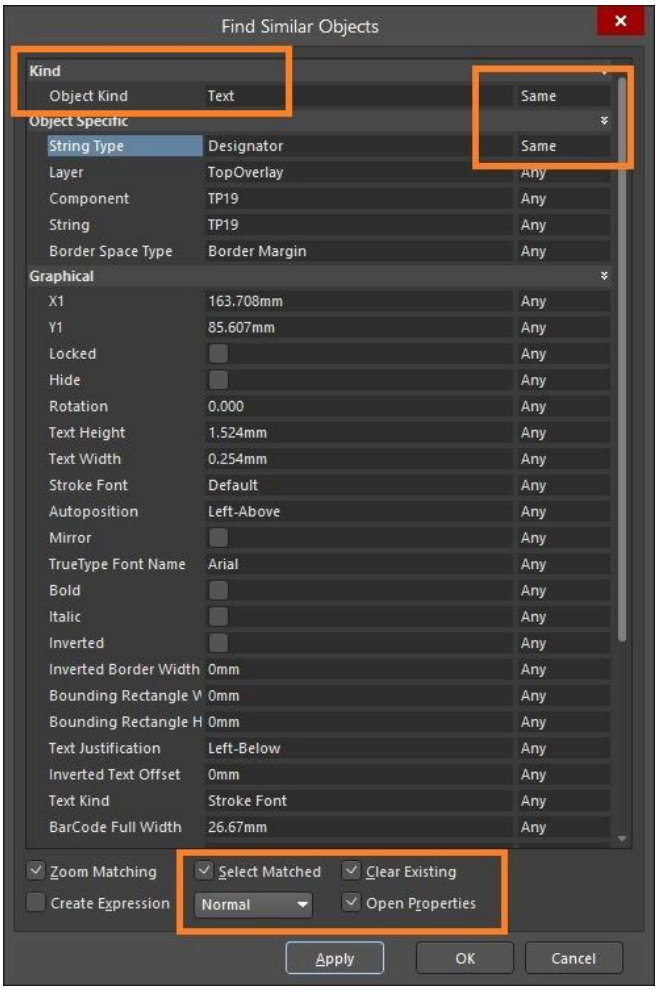
Placement

When placing your components, it is very useful to group them together into their functional groups: i.e. placing the 3.3 V regulator with its capacitors and making that group as compact as possible.

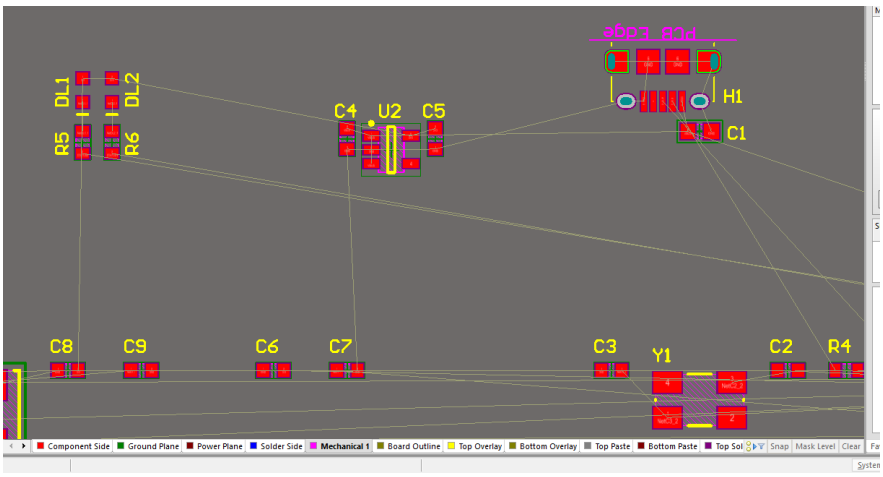


Note the pale lines, called airwires make up the ratsnest. These indicate pad connections that belong to the same net and need to be routed. When placing decoupling capacitors, care needs to be taken to make sure they are **as close as possible** to the pins they are decoupling. See C4 and C5 in the above image located near U2. <u>This is especially important around your microcontroller.</u>

You might find the silkscreen comments are quite large and get in the way. These can be shrunk by right clicking on one, and selecting *Find Similar Objects*. This dialog is used to automatically select objects using a filter. In this case the settings will be to select all objects that are of the same “Text” type AND same “Designator” type. Clicking apply will select all objects that match your settings. Clicking OK will select these and bring up the *Properties* window. This is used to modify the properties of *all* of the currently selected objects at the same time. Give the text a height of 0.8 mm and a stroke width of 0.15 mm. See next page.

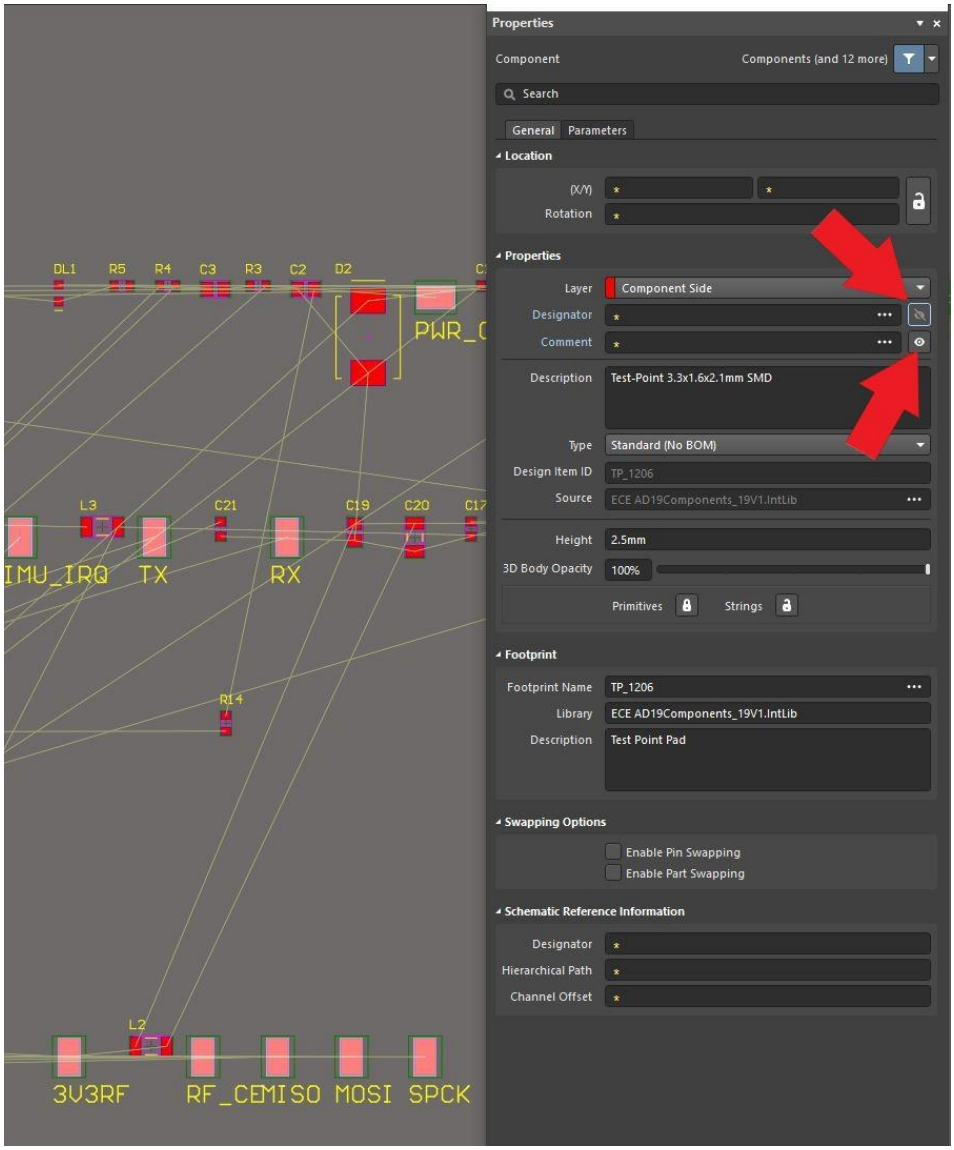


Group together related components and then arrange them close to other component groups or main components on the board. The goal here is to place the parts in a logical fashion that will simplify the ratsnest and hopefully reduce some of the crossovers. But do not get too worried about refining the ratnest as many of the airwires are GND and 3V3 which will have their own dedicated routing layers. If you need, you *can* place components on the bottom side of the PCB by pressing <L> while dragging them. However you will need to consider how the PCB will be built, especially with regard to using the reflow oven. Try your best to get most components on the top layer as this will speed up assembly. Just a few decoupling capacitors around the micro are acceptable & logical on the bottom side of the PCB.

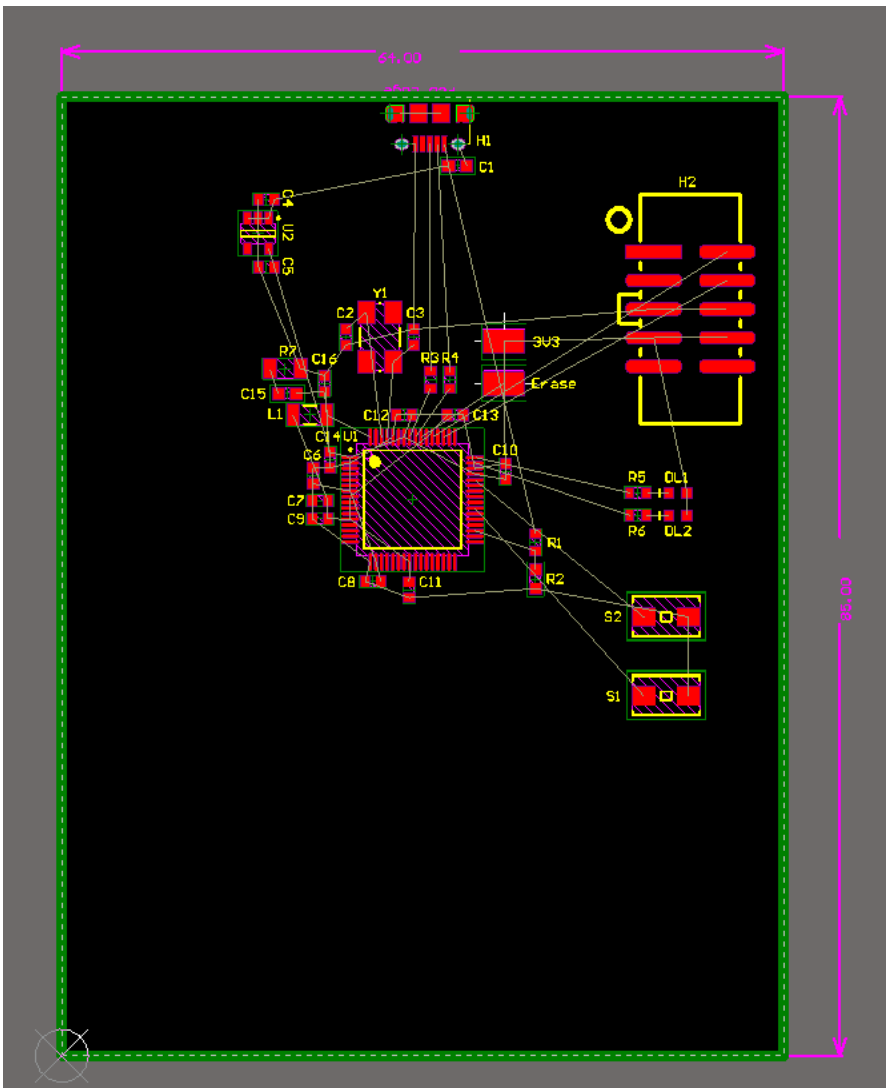


When moving parts around, you might see objects turn green. These are actually tiny green crosses you can see if you zoom in on the part. This is Altium telling you that this placement has violated one of its many rules (that we imported earlier). If you hold your mouse over the offending part, the HUD in the top left of the display will tell you what kind of error it is so you can fix it.

Hopefully all of your testpoints in your schematic diagrams have comments describing what they are: “3V3”; “Erase”; etc… To get these visible, drag a box around the testpoint (the pad AND its designator). From the *Properties* panel, hide the designator and unhide the comment. You can do this to multiple testpoints – use Shift + dragbox method.



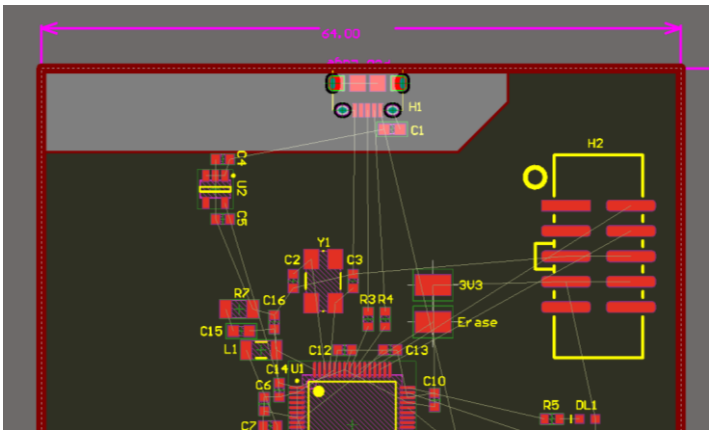
Below is an example of component placement of a simpler but similar board:



Your design does not need to be this compact, however shorter traces will help with signal integrity and also important for the microcontroller decoupling capacitors and crystal. Note: H2 header is surface mount on this design but we recommend using a through-hole header as they are stronger, more reliable & are easier to route on a multilayer PCB.

Power and Ground Planes

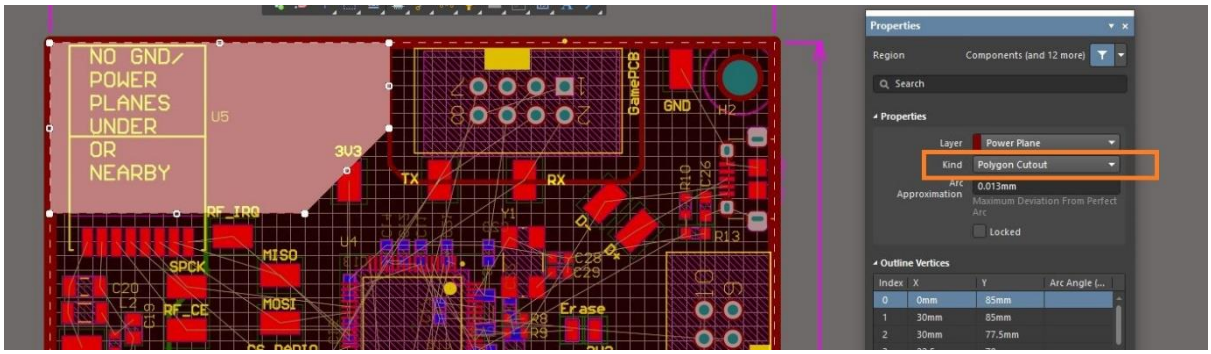
Our design template has two internal power planes called Ground and Power (these become the active edit layer by clicking the associated tabs at the bottom-left of the PcbDoc window). In Altium these internal layers are “inverted”, this means that there will be ***no*** copper where you draw a line. You partition & select the separate regions and assign them to nets. Do not partition your ground plane, this should be a single uninterrupted sheet of copper. You will want to add a region for 5V &/or VBatt and importantly 3V3 on the power plane.



Use the *Place → Line* tool to create this region. Use <SPACE> and <SHIFT+SPACE> to get the outline how you want it. Then double click the region and assign it to a net (eg. 5V, VBATT, VBUS). Assign the large remaining portion of the power plane to 3V3. **Make sure your ground plane is assigned to GND** (double click the "Ground Plane" tab & set the net to GND – (all layer tabs are at bottom of display). Then double click a proposed GND plane area within the PCB outline and set *Connect to net* = GND (in the "Split Plane" pop-up window).

A copper free zone also needs defining under and around the NRF24 radio module. This exclusion zone needs to be set on **each** copper layer (the power / ground planes AND top / bottom layers).

Use *Place->Solid Region, Kind = Polygon Cutout.* Remember press tab to change properties & press the pause symbol in middle of screen to return to editing.



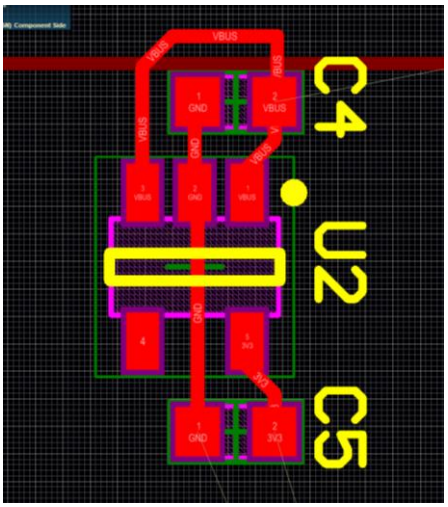
To check you have correctly created copper free zones under the NRF24 radio do the following:

Panels->View Configuration ('L' key) – then *View Options* tab. Under *General Settings*, select *3D On* and *Single Layer Mode ON.* Then from the main editing window tabs near the bottom of the screen, view each copper layer (top, bottom, ground and power) and ensure no visible copper is under the radio module. You can also view single layers in 2D view – switch between 2D & 3D by pressing *2* or *3* and use shortcut *(Shift + 'S')*.

Routing

READ the LAYOUT GUIDELINES section ahead before fully routing your PCB

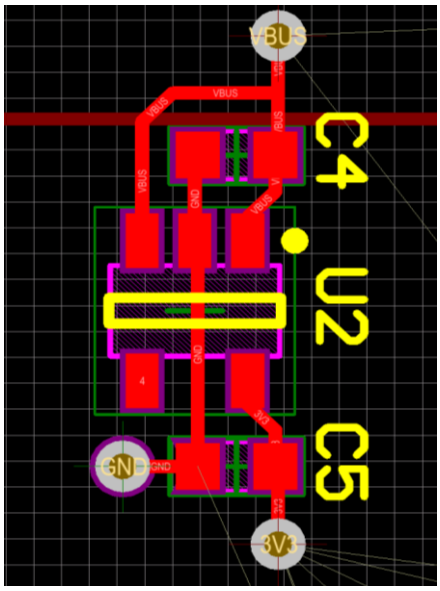
Go back to the top layer and let's start routing the 3.3V regulator. Use *Route → Interactive Routing* <U> → <T> and click on a pad, click when you want to add a new length of trace, and use <SPACE> to change the elbow direction or <SHIFT>+<SPACE> to change the elbow type. You can press TAB while placing tracks to open the properties panel. Here you can change track widths to suit the copper trace you are currently routing.



The snap grid size can be adjusted if need be with <G>.

Vias

Now add some vias to the internal planes or bottom layer by routing a track starting from a component pad, moving to empty space, and pressing <NUMPAD +> to switch layer. This will generate a via. Click to place it and then right click to stop. You will need to change back to the top layer after this. When Vias connect to internal planes, they display a thin coloured plus shape on the Via with the colour of the plane they have attached to. Sometimes they are too close to a border to properly connect and may need to be repositioned. While *Interactively Routing* <U> → <T>, you can adjust the size of the via by pressing *4* to toggle between design rule presets or press *TAB* to adjust routing properties v*ia hole + via diameter.* If you need to use smaller vias, a hole of 0.3mm and diameter of 0.8mm is acceptable **but you should try to use** 0.5mm hole & 1mm diameter typically or larger.



<u>Do not place *Blind Via's,*</u> this is not required in this design & will fail the manufacturers audit.

One thing to be mindful of is how much current each trace will need to carry. A useful tool to use is http://www.4pcb.com/trace-width-calculator.html. Set the thickness to 1 oz/ft^2 and check the results for external layers.

If you need to delete an entire trace, use <BACKSPACE> as it will delete the currently selected section, then automatically selects the next section to delete. After reading the next section, start routing the rest of your board.

Layout Guidelines

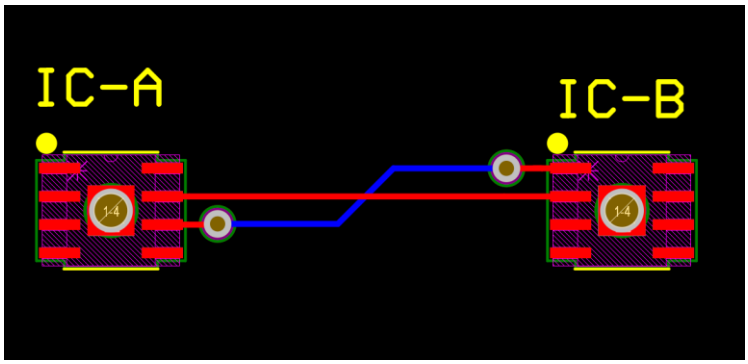
- Route high-speed (>50kHz) traces first on the top layer (USB, SPI, I2C, Led strip, Crystal). And keep them away from all other traces. A rule of thumb for this is the 3W rule , which means: the separation distance between two traces should be at least three times the width of the traces, centre to centre.

- Keep your traces short. When the length of your trace is becoming comparable to the wavelength of your signal, you need to start treating it like a transmission line. A general rule of thumb is to keep the trace shorter than $1/6^{th}$ λ, so you can ignore transmission line effects

  $$l < 1/6^{th}(c/f)$$

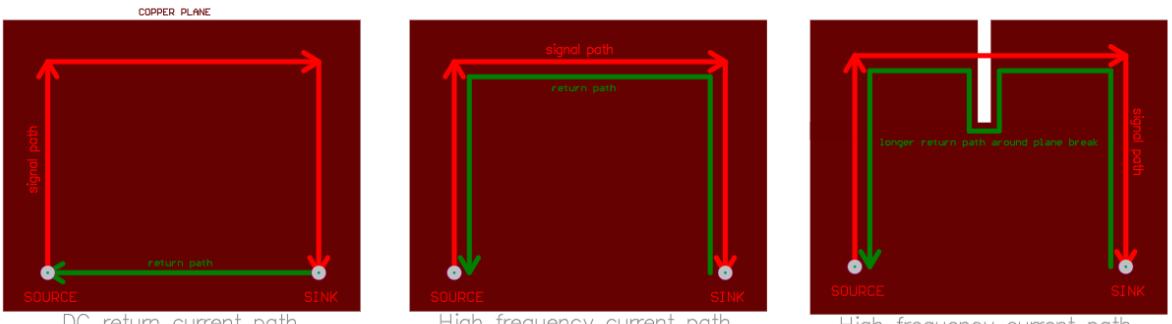
  Where c is the "speed of propagation" and f is the frequency of the signal (λ=c/f). Approximate speed of propagation in PCB FR4 traces is ~$1.5x10^8$ m/s (which is much slower than speed of light in free space). Line wavelength is less than free-space wavelength for any given frequency.

- If two high-speed traces need to cross, use "vias" at the start and end of second routed trace. Route most of the second trace on the bottom layer (blue). Ensure the bottom layer trace does not cross a gap in the power plane layer or cross over multiple different power planes (PCB high speed return paths will be fully explained during ENC461 lectures).



High speed traces that need to cross

- With DC, the return current takes the path back with the lowest resistance. With a higher frequency, the return current path flows along the lowest impedance. This is directly beside/under the signal. A routed trace over a power or ground plane gap creates large loop areas, because the return current cannot flow beside the signal, & so must find another path which can induce noise into the circuit.

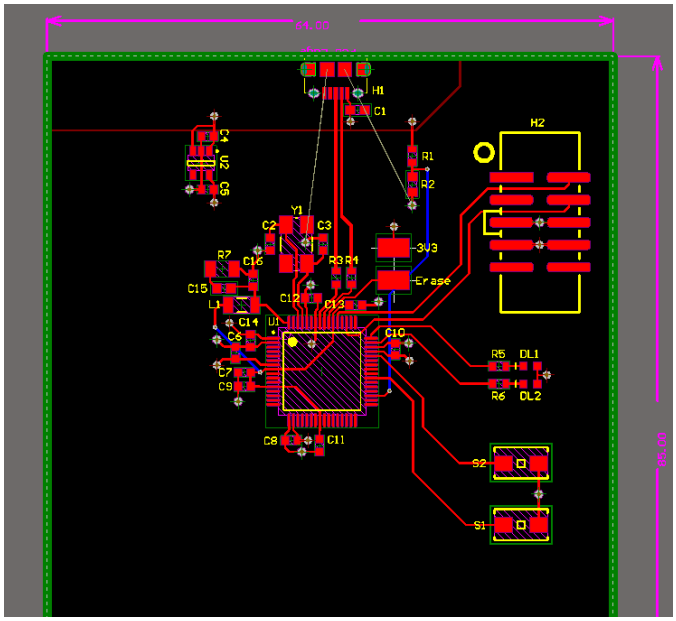


Return current via internal plane and resulting loop area

- Try not to route over gaps in the ground/power plane. The return current path for a fast signal is almost entirely underneath the trace being routed. If there were a partition in the internal plane beneath, the return path will have to go around that partition creating a large loop area which will couple noise into your system. It can be a struggle to avoid routing over gaps in your split power plane, but try your best to avoid this situation.

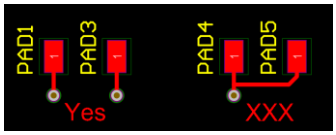
- Beware crosstalk! When two traces are running close and parallel, they will have capacitive & inductive coupling. This means that a high frequency signal can jump from one trace to another. High frequency traces should be kept apart where possible[1] (apply the 3W rule).

- Differential pairs are the exception to the cross talk rule. They should be routed next to each other and have their lengths matched as closely as possible. See the USB data lines in the following example. To route these use *Route->Interactive Differential Pair Routing*.



USB data lines routed

- Route analogue traces well away from high-speed traces, preferably on the bottom layer as the internal planes act as a shield.
- Route high current signals with short, wide traces to reduce resistance.
- Use vias generously to route directly to internal planes. No need to complicate trace routing by linking component pads to one shared via. It is a cost neutral design choice!



- Finally route the slow signals (buttons, led indicators etc). These can jump layers as required to fit in.

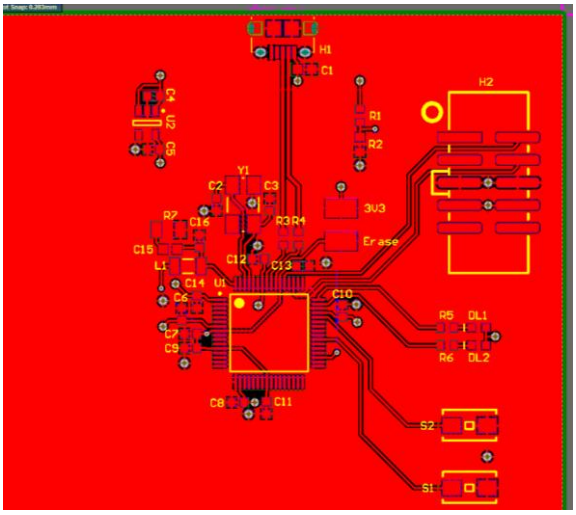
[1] It's not always possible to keep them apart, especially in a dense layout. But every attempt should be made.

Differential Pairs

As discussed in the previous section, route the usb data lines as a differential pair *Route->Interactive Differential Pair.*

Polygon Pours

Now we will add a polygon pour to the top and bottom layer and assign it to the ground net (This step is optional & is a considered design decision that you make if you wish to include full or partial GND polygons to your outer layers). This will act similarly to the internal ground plane and may improve the quality of your design. From the *Place* menu select a *Polygon Pour*. Draw the plane outline by clicking on the four corners of the board then right click to finish. Double click the polygon to bring up its properties and set the net to GND and ensure it is set to "pour over all same net objects". Also make sure that "Remove dead copper" is ticked. Click *OK*. Your PCB should now turn bright red:



Note: You may prefer to enter the *View Configurations* menu <L> and go to the *View Options* tab. Tick the checkbox for *Polygons* to *Draft* to view only the polygon outline. Repeat the pour for the bottom layer as required.

Design Rule Check (DRC)

Now that we have laid out the board, let's see how much Altium approves of it. Using the *Tools* → *Design Rule Check* tool, untick the "Create Report File" options and click *Run Design Rule Check*. The messages window should popup with a long list of rule violations. Some of these rules might seem arbitrary but they are setup so that if your design has no errors, then our PCB supplier should have no trouble manufacturing it. Go through and fix as many errors as possible. Some will come from pads designed in the footprints. Do not worry about these.

There is one other error that Altium incorrectly generates: SMD To Plane. This rule is to make sure any pad that is assigned to a net with an internal plane, has a route to that plane within a set distance. Longer routes could degrade the signal quality which is what we are trying to avoid. However, sometimes Altium cannot see a path to the ground plane through other component pads for example, when this happens it thinks there is an infinite distance to the SMD plane which it represents with 2539.975mm. This error **and only this error** can be safely ignored.

You can view the results of a DRC anytime by clicking *View->Panels -> PCB Rules and Violations.* From there you can view ALL rule violations or select a particular rule class to inspect the rule settings and any violations.

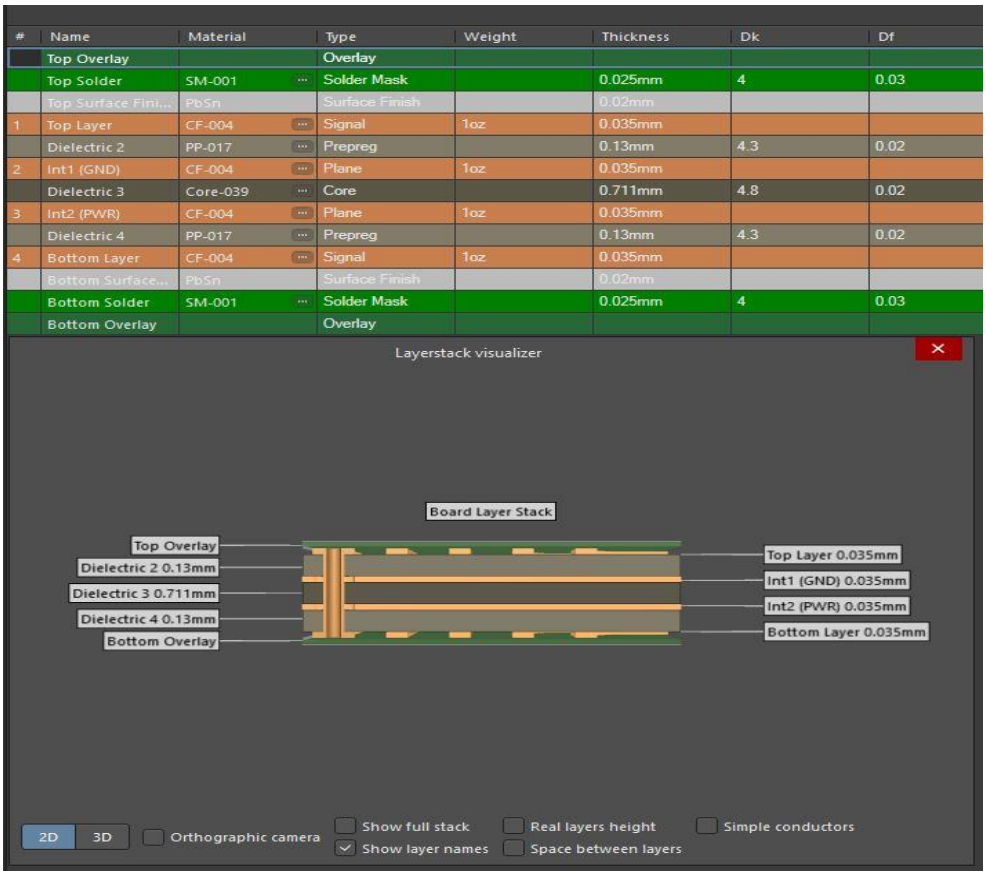
Useful Altium reference material (this is preset for ENCE461, you can skip down to the final section - PCB checklist)

Starting from Scratch

The following section is for your reference & to help you understand how the pcb template was created. This information will be useful if you intend designing more pcbs during the year. Or skip to Checklist at end of document.

Layer Stack

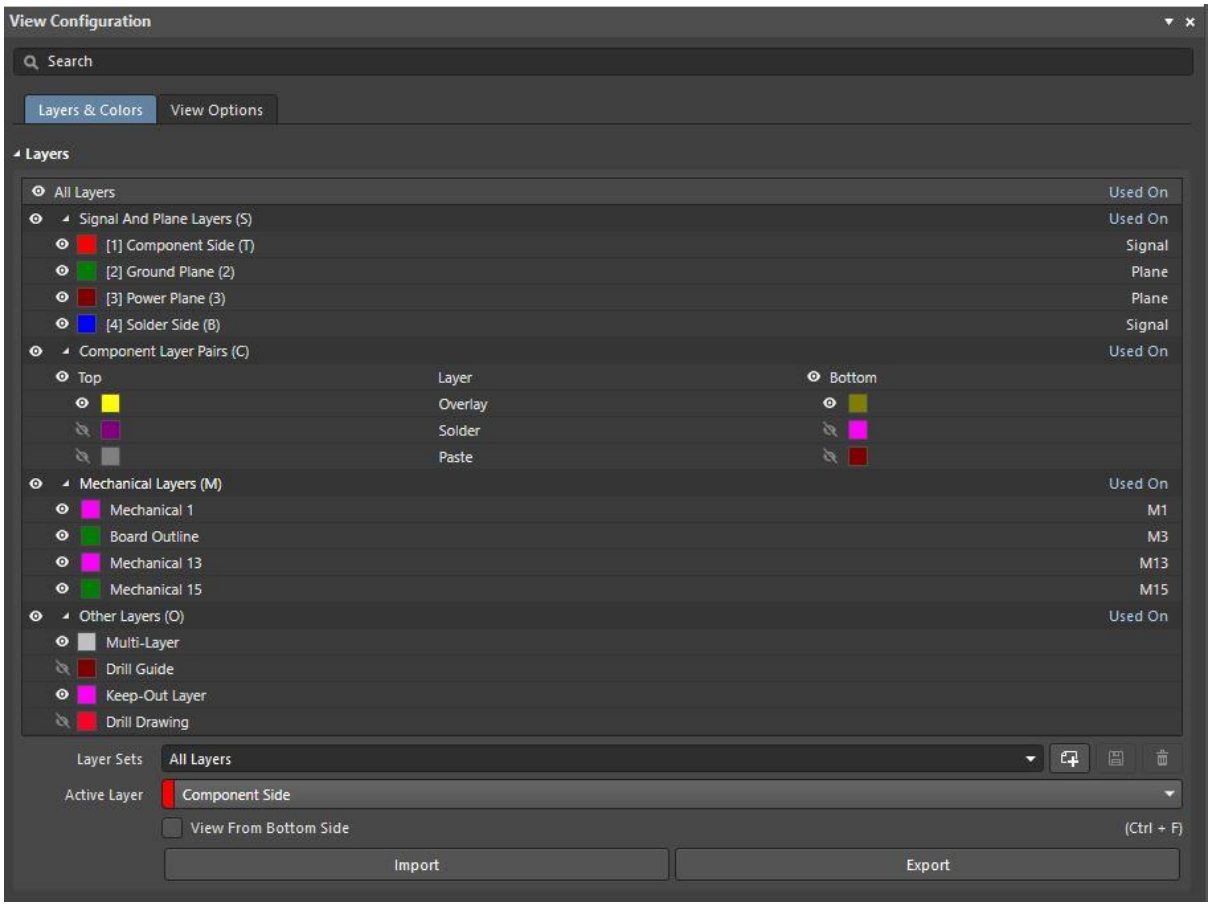
We will now configure the layer stack for our board. Bring up the manager with *Design → Layer Stack Manager*. From *Tools ->Presets* select *Four Layer*. From *Tools* you can select a visualiser which will be similar to below depending on what options are set.



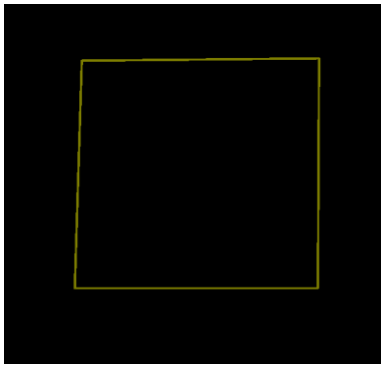
Press the save icon in upper left corner of screen and this will update your PCB design.

Board Outline

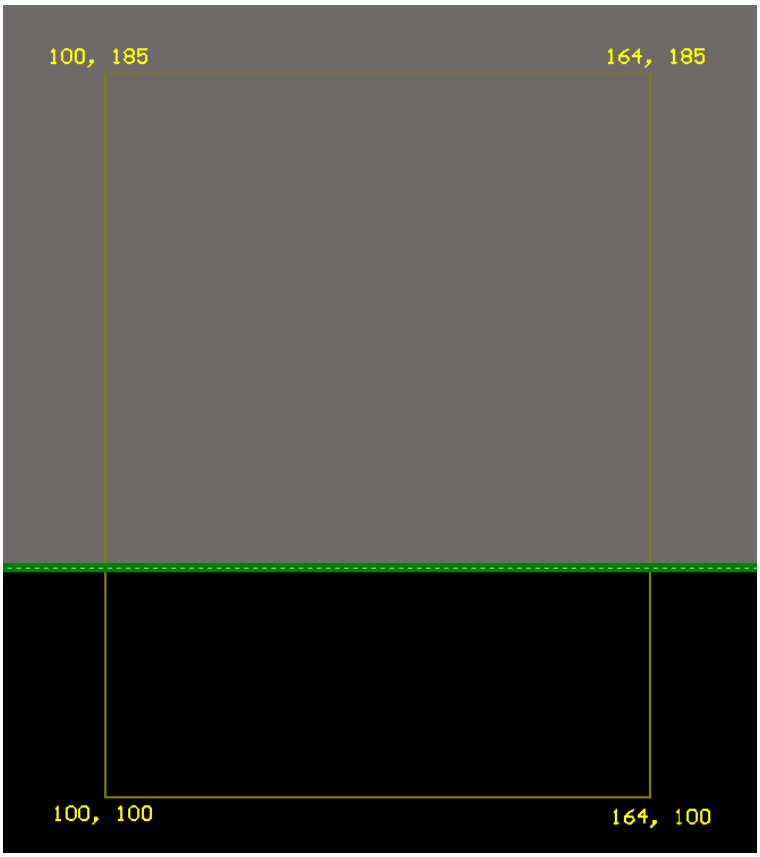
Now we will setup the outline of the board. Press *L* to bring up the *View Configuration* menu. From here you can configure how Altium displays the layers to you which can be quite useful. For now we want to add another Mechanical layer. Ensure the Mech Layers are visible, then right click in window and *Add Mechanical Layer*:



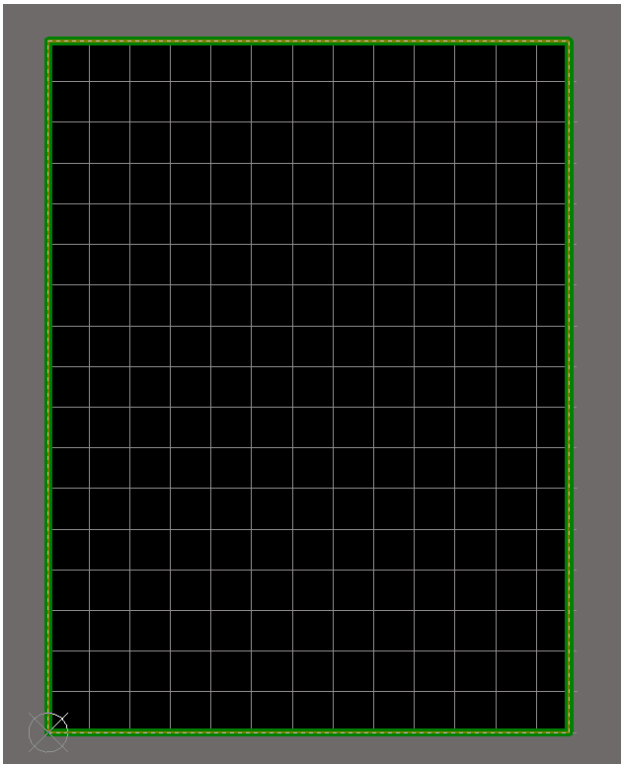
Create a mechanical layer (the course template uses Mechanical layer 3 for the board outline). Give it a name, i.e. “Board Outline”. Click *OK* to leave the menu. At the bottom of the screen, select your new layer tab. Now from the *Place* menu <P> use the Line tool to draw a square:



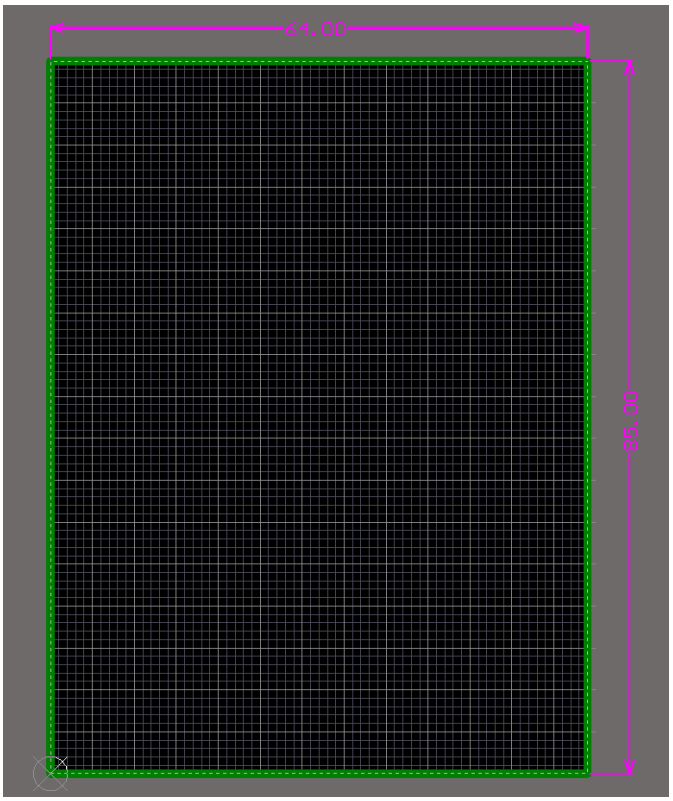
You can double click on the lines to set their x,y end points as required. Set them to be:



Now select all four lines and use the *Design → Board Shape → Define from selected objects* tool. Using the *Grid* menu <G> set your grid to be 1mm and using *Edit → Origin → Set,* place it on the bottom left corner (100, 100):



In the *Mechanical 1* layer, use the *Place → Dimension → Linear* tool to show the dimensions of the board. Make sure to edit them and set their unit to *mm*.



PCB Checklist (tick off prior to inspection)

- ☐ Ensure there is no copper under NRF24 radio module on any of the 4 copper layers
- ☐ Check locked components were not shifted AND that the PCB size was not altered
- ☐ Check that the majority of components are placed on top layer
- ☐ PCB is labelled on either silkscreen with at least your Group Number
- ☐ No silkscreen text covering pads or vias. Added graphics should be kept simple for manufacture.
- ☐ No tented or blind Vias
- ☐ Where possible, adjust to larger Vias (1mm Pad & 0.5mm hole).
- ☐ Critical Design Rules resolved. Other unimportant violations understood & ignored/accepted (TA's can advise)
- ☐ Add mounting holes. There are mounting hole parts in the Altium ECE library (add at least 3).