CS1320

THE UNIVERSITY OF WARWICK

First Year Examinations: Summer 2016

Computer Organisation and Architecture

Time allowed: 2 hours.

Answer **FOUR** questions.

Read carefully the instructions on the answer book and make sure that the particulars required are entered on **each** answer book.

Approved calculators are allowed.

---

1. (a) Explain the difference between value and representation, giving an example. [3]

   (b) i. Convert 48_{10} to an unsigned binary number. [2]

   ii. Show how -22_{10} can be represented using two's complement. [2]

   iii. Show how 22_{10} can be subtracted from 48_{10} using two's complement. [3]

   iv. Explain the concept of overflow in binary arithmetic, giving an example. [3]

   (c) i. Convert 4180_{10} to octal. [3]

   ii. Convert 1111101001101011_2 to hexadecimal. [3]

   iii. State whether $D2AF_{16}$ is a valid hexadecimal value. Justify your answer. [2]

   (d) Explain the difference between fixed point and floating point binary representation. Comment on the achievable precision and range of each representation. [4]

---

2. (a) Explain the difference between combinatorial logic and sequential logic. [3]

   (b) A 1-bit full-adder performs addition on two significant bits and a previous carry bit.

   i. Draw the truth table for a 1-bit full-adder. [4]

   ii. Design a logic circuit that implements the truth table of a 1-bit full-adder. [5]

   (c) D-type flip-flops are used in the design of many common sequential logic circuits.

   i. Draw and explain the truth table for a D-type flip-flop. [3]

   ii. Design an N-bit register using D-type flip-flops. Your design should be capable of storing N bits in response to a single clock cycle. State any assumptions. [5]

   iii. Design an N-bit binary counter using D-type flip-flops. Your design should give an explanation of how the circuit operates. State any assumptions. [5]

---

3. Karnaugh maps and Boolean algebra can be used to simplify logic functions.
   $F_1 = A.B + \bar{A}.B.\bar{C}.D + \bar{A}.B.C.D + A.\bar{B}.\bar{C}.\bar{D}$
   $F_2 = (A + \bar{B}).(\bar{A} + C).(B + \bar{C})$

   (a) Reduce F_1 to its simplest sum of products form using a Karnaugh map. [9]

   (b) Reduce F_2 to its simplest sum of products form using Boolean algebra. [9]

   (c) Design a logic circuit that implements F_1 using only NAND gates. [7]

4. (a) Caches have become fundamental to the performance of computer systems.

      i. Explain why memory access time is considered to have become a performance bottleneck in computer systems. [2]

      ii. Explain the role of caches in the memory heirarchy. Your answer should explain how caches exploit *spatial locality* and *temporal locality*. [6]

   (b) Explain how parity codes enable the detection of errors in the transmission of binary messages, giving a simple example that uses odd parity. [6]

   (c) Microprocessors consist of a set of components that interact to provide function.

      i. Explain what is meant by the term *von Neumann architecture*. [2]

      ii. Explain the roles of the arithmetic logic unit (ALU), program counter (PC) and instruction register (IR) in program execution. [5]

      iii. Explain how a control unit can be implemented using a hardwired approach, giving the advantages and disadvantages of the approach. [4]

5. (a) Explain the operation of the I/O mechanisms listed below. Your answers should identify the advantages and disadvantages of each mechanism, and use appropriate diagrams to illustrate your explanations.

      i. Memory mapped I/O. [5]

      ii. Polled I/O. [5]

      iii. Interrupt-driven I/O. [5]

   (b) Explain how context switching is related to interrupt-driven I/O. Comment on why context switching is required and how it is achieved. [4]

   (c) Explain how direct memory access (DMA) operates, giving details of when it is most appropriate to use DMA. [6]

End