DESIGN AND SIMULATION OF CMOS INVERTER

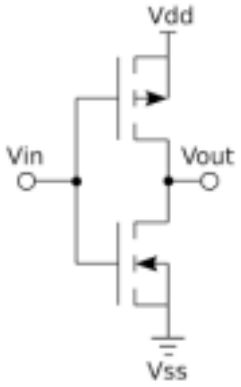
AIM :

To design and simulate CMOS Inverting amplifier using Cadence with 180nm technology

REQUIREMENTS:

EDA Tool: Cadence Virtuoso, Cadence Spectre

CIRCUIT DIAGRAM:



PROCEDURE :

- **SCHEMATIC ENTRY:** The CMOS circuit will be designed based on the specification and the design will be captured Virtuoso Schematic Editor.
- **SIMULATION:** Once the circuit is captured on the Virtuoso Schematic Editor, its functional behavior can be verified using Spectre.

PHASE I : Schematic entry in Virtuoso Schematic Editor.

1. Workspace creation
   - Make a right click on the Desktop and select the option “Create Folder”
   - Name the folder, for example, we have named it as “inverter”
   - Open the created folder, right click and “Open in terminal”
   - Type the command “csh” to initialize shell and source the cshrc file with the command “source /home/install/cshrc”
2. Invoke Virtuoso
   - Soon after we source the “cshrc” file, we get a display “Welcome to Cadence Tools Suite”.
   - Now invoke virtuoso using the command “virtuoso &” or “virtuoso”
   - We get a virtuoso window as given

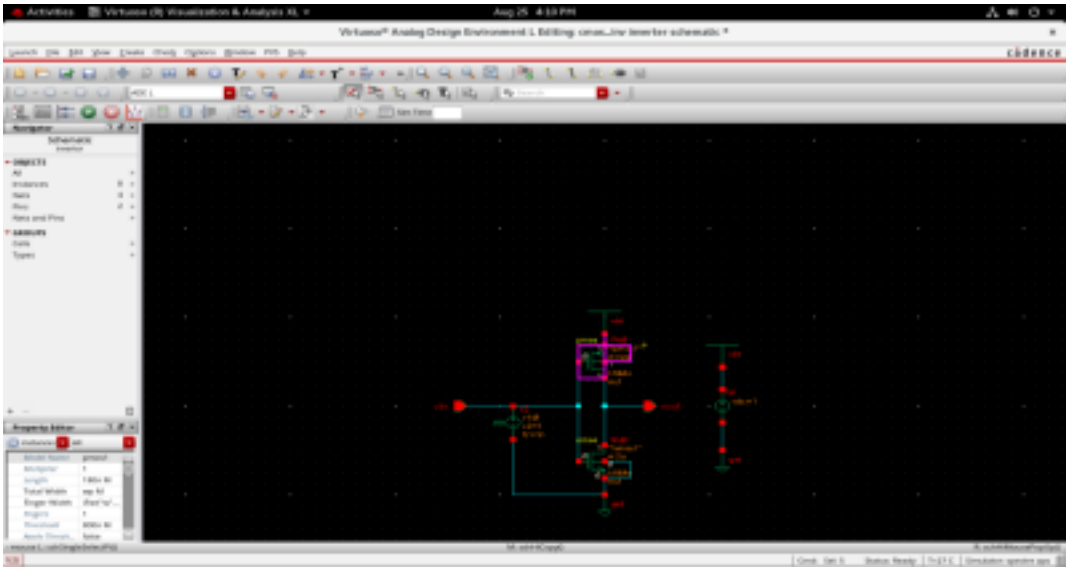
3. Creating a library
   - In virtuoso's top menu, select "Tools" and select "Library Manager". The Cadence Library Manager appears
   - From the top menu of the Library Manager, select "File -> New -> Library" to create a new library for a new design – "1-inv"
   - We'll get a "New Library" form where we can name the library that we create
   - Select the option "Attach to an existing technology library" – "gpdk180"
   - The created library is now available in the Library Manager under Library
4. Create a cell
   - Before creating a cell, make sure that the created library is selected. Only then the created cell can be viewed under the respective library.
   - To create a Cell View, select File -> New -> Cell View.
   - Name the cell – "inv-design"

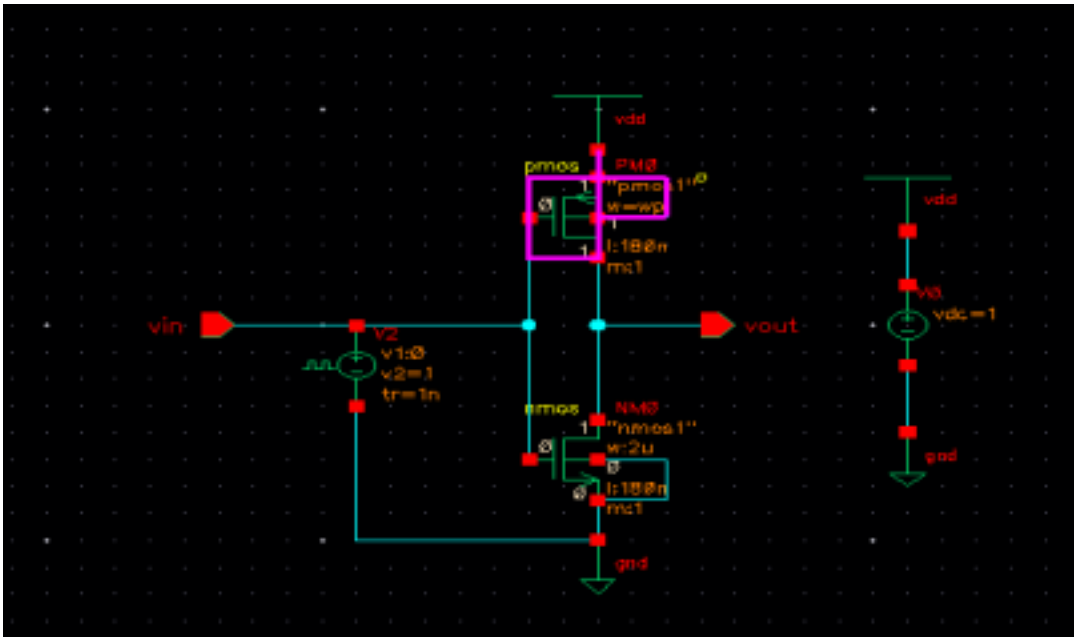
5. Virtuoso schematic editor will open
6. Add instances of PMOS,NMOS devices
7. Add instance of I/O pins VIN, VOUT
8. Add instances of Vdd and GND
9. Connect all instances using wire
10. Once wiring is done save the design

11. Supply voltage is added by adding instances of “vdc” from “analoglib” and give appropriate voltages based on specification or technology node.

12. For an input source, “vpulse” is considered and parameters likeVoltage 1, Voltage 2, Period, Delay time, Rise time, Fall time and Pulse width

Schematic :





PHASE II : Functional simulation using Spectre

1. Launch ADE L . make sure Spectre simulator is selected.
2. Model Libraries & Process Corners – to make sure that ".scs" file of the respective technology node has been selected – select "NN"
3. Setup Transient analysis, DC analyses
4. Select outputs to be plotted.
5. To run the simulation, select "Simulation" from ADE L and select the option "Netlist and Run"
6. Input signals and Output signals can be seen separately by selecting "Graph -> Split All Strips"
7. Save the state

Simulation output :