

DESIGN AND SIMULATION OF 4 BIT UNIVERSAL SHIFT REGISTER USING HDL

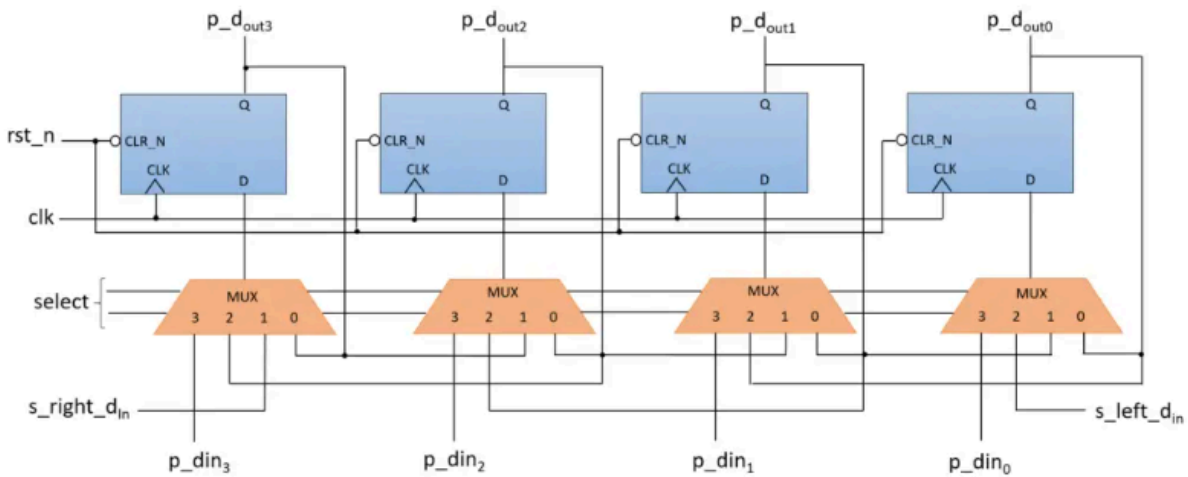
To design a 4-bit Universal Shift Register using Verilog HDL and to perform functional simulation. To synthesize the design and implement using Altera FPGA.

REQUIREMENTS:

EDA Tool: Altera Quartus Prime v17

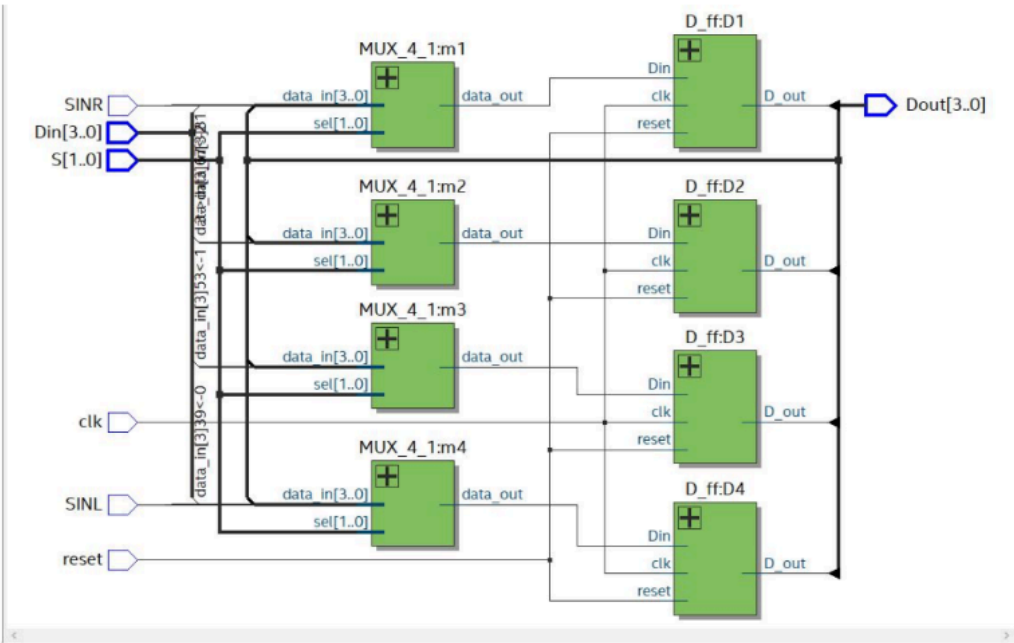
Hardware: DE1-SoC board

ARCHITECTURE :

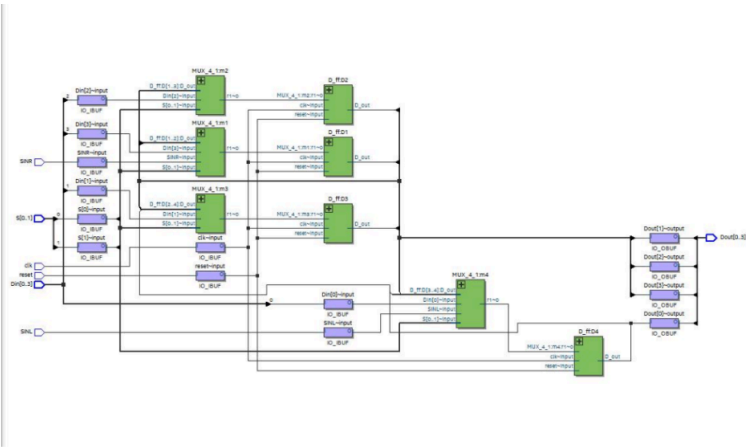


Mode Control		Register operation
S1	S0	
0	0	No change
0	1	Shift Right
1	0	Shift Left
1	1	Parallel Load

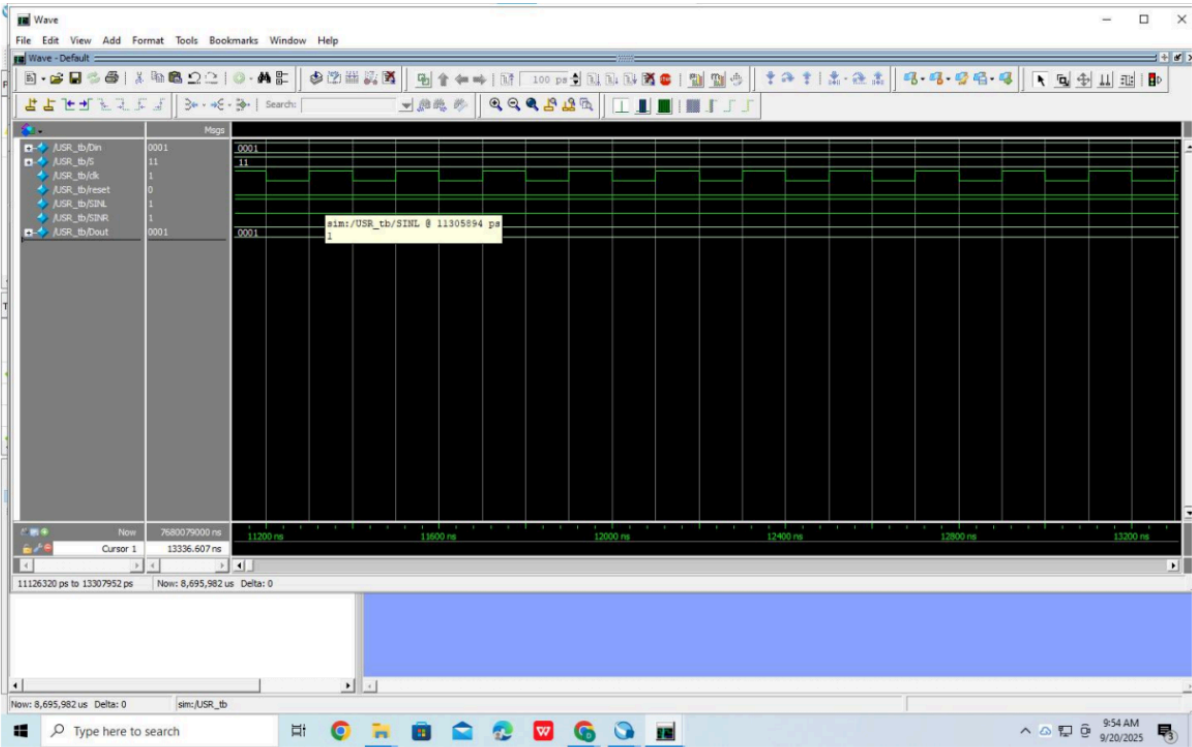
RTL SCHEMATIC:



TECHNOLOGY SCHEMATIC:



SIMULATION:



PIN CONFIGURATION & IMPLEMENTATION:

Pin Legend:

- Symbol: Pin Type
- User I/O
- User assigned I/O
- Filter assigned I/O
- Unbonded pad
- Reserved pin
- DEV_OE
- DIFF_n
- DIFF_p
- DIFF_n output

Node Name	Direction	Location	I/O Bank	VREF Group	Filter Location	I/O Standard	Reserved	Current Strength	Slew Rate	Differential Pair	analog Setting: SXB/VCCT_GXB1
Din[3]	Input	PIN_AB12	3A	B3A_NO	PIN_AB12	2.5 V		12mA (default)			
Din[2]	Input	PIN_AC12	3A	B3A_NO	PIN_AC12	2.5 V		12mA (default)			
Din[1]	Input	PIN_AF9	3A	B3A_NO	PIN_AF9	2.5 V		12mA (default)			
Din[0]	Input	PIN_AF10	3A	B3A_NO	PIN_AF10	2.5 V		12mA (default)			
Dout[3]	Output	PIN_V16	4A	B4A_NO	PIN_V16	2.5 V		12mA (default)	1 (default)		
Dout[2]	Output	PIN_W16	4A	B4A_NO	PIN_W16	2.5 V		12mA (default)	1 (default)		
Dout[1]	Output	PIN_V17	4A	B4A_NO	PIN_V17	2.5 V		12mA (default)	1 (default)		
Dout[0]	Output	PIN_V18	4A	B4A_NO	PIN_V18	2.5 V		12mA (default)	1 (default)		
S[0]	Input	PIN_AD11	3A	B3A_NO	PIN_AD11	2.5 V		12mA (default)			
SINL	Input	PIN_AE11	3A	B3A_NO	PIN_AE11	2.5 V		12mA (default)			
SINR	Input	PIN_AC9	3A	B3A_NO	PIN_AC9	2.5 V		12mA (default)			
clk	Input	PIN_AF14	3B	B3B_NO	PIN_AF14	2.5 V		12mA (default)			
reset	Input	PIN_AD10	3A	B3A_NO	PIN_AD10	2.5 V		12mA (default)			
ADC_CONVST	Unknown					3.3-V LVTTTL		16mA (default)			
ADC_DIN	Unknown					3.3-V LVTTTL		16mA (default)			
ADC_DOUT	Unknown					3.3-V LVTTTL		16mA (default)			
ADC_SCLK	Unknown					3.3-V LVTTTL		16mA (default)			
AUD_ADCDAT	Unknown					3.3-V LVTTTL		16mA (default)			
AUD_ADCLCK	Unknown					3.3-V LVTTTL		16mA (default)			
AUD_BCLK	Unknown					3.3-V LVTTTL		16mA (default)			
AUD_DACDAT	Unknown					3.3-V LVTTTL		16mA (default)			
AUD_DACLCK	Unknown					3.3-V LVTTTL		16mA (default)			