DESIGN AND SIMULATION OF 4 BIT UNIVERSAL SHIFT USING HDL

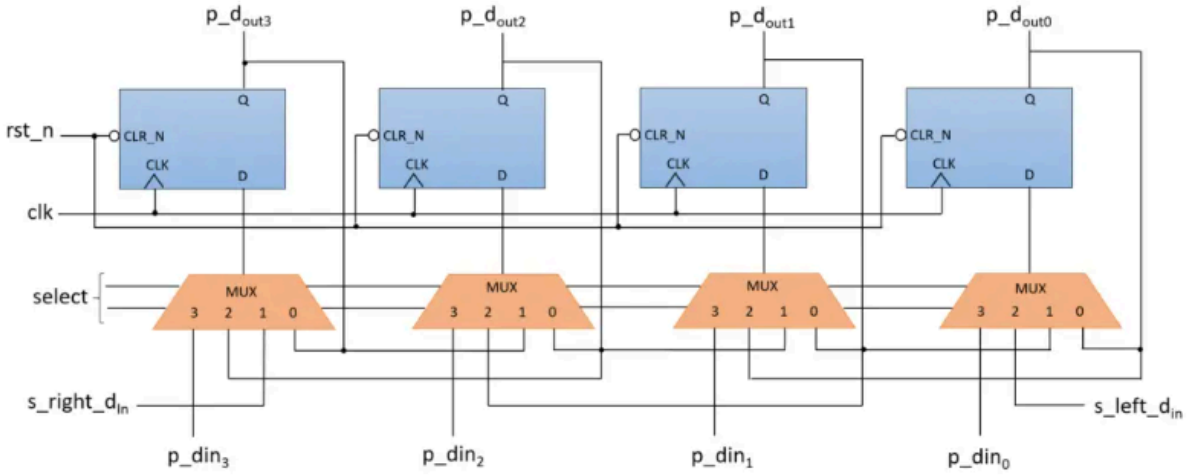
To design a 4-bit Universal Shift Register using Verilog HDL and to perform functional simulation. To synthesize the design and implement using Altera FPGA.

REQUIREMENTS:

EDA Tool: Altera Quartus Prime v17

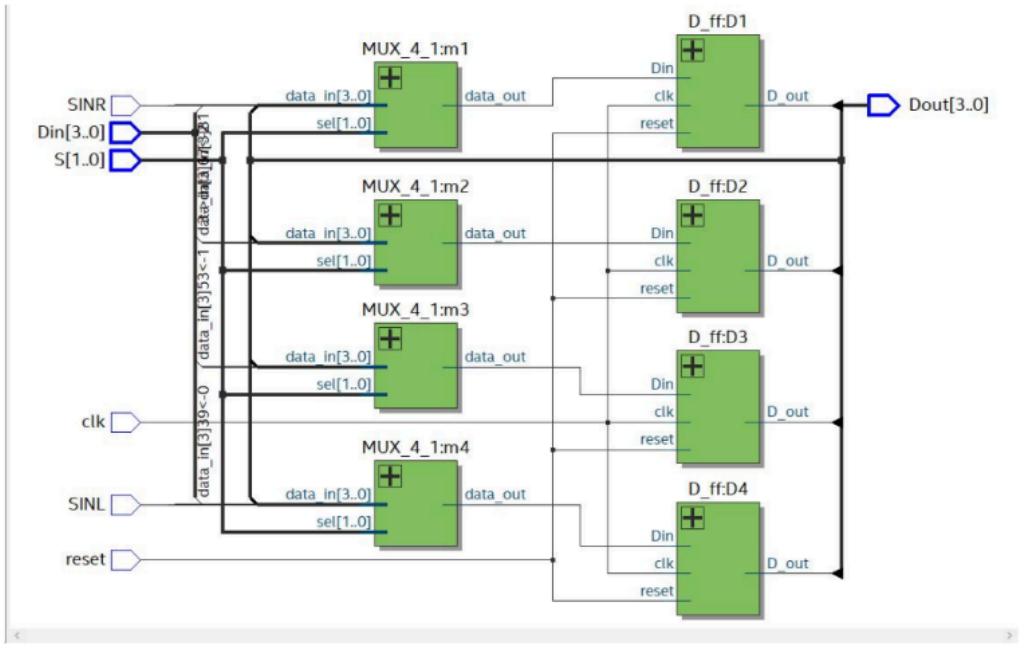
Hardware: DE1-SoC board

ARCHITECTURE :

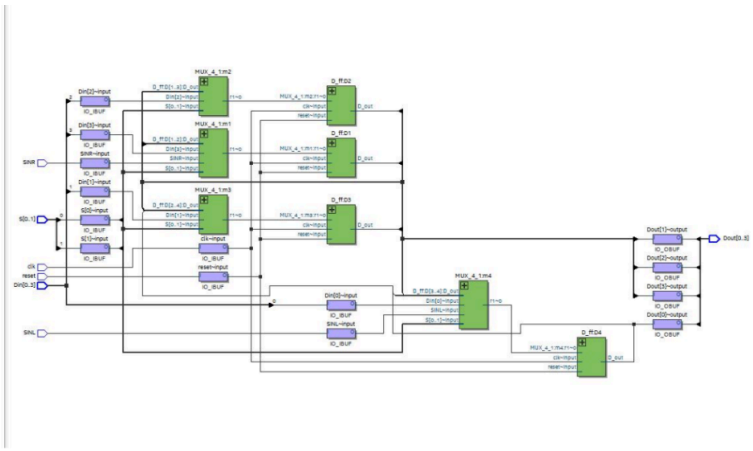


Mode Control		Register operation
S1	S0	
0	0	No change
0	1	Shift Right
1	0	Shift Left
1	1	Parallel Load

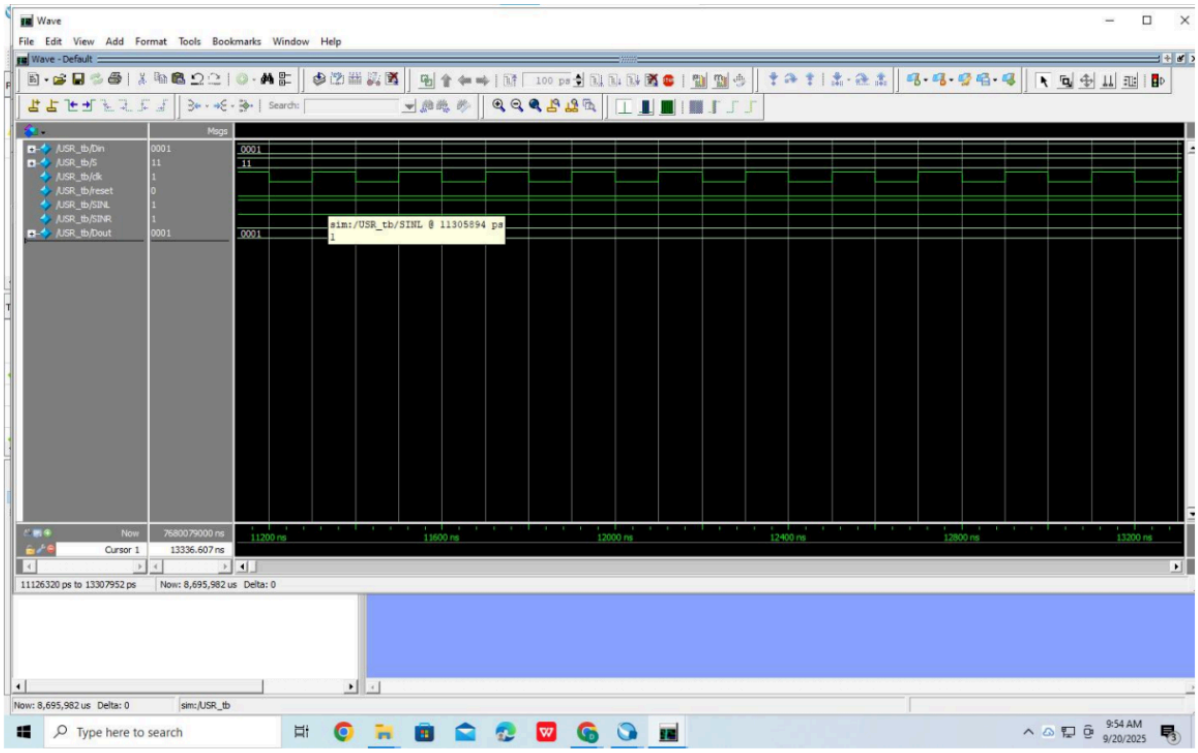
RTL SCHEMATIC:



TECHNOLOGY SCHEMATIC:



SIMULATION:



PIN CONFIGURATION & IMPLEMENTATION: