DESIGN, SIMULATION AND IMPLEMENTATION OF FLIPFLOPS USING ALTERA FPGA

To realize flip flops using Verilog HDL and to perform functional simulation. To synthesize the design and implement using Altera FPGA.

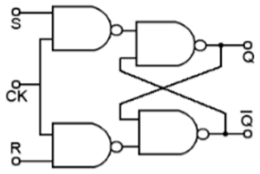
REQUIREMENTS:

EDA Tool: Altera Quartus Prime v17

Hardware: DE1-SoC board

FLIP FLOPS & CHARACTERISTIC EQUATIONS:

JK FLIP



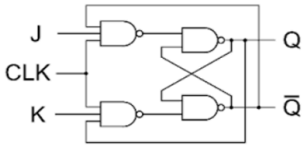
TRUTH TABLE

S	R	Q_N	Q_{N+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	-
1	1	1	-

.

$$Q_{N+1} = Q_N R' + SR'$$

SR FLIP-FLOP

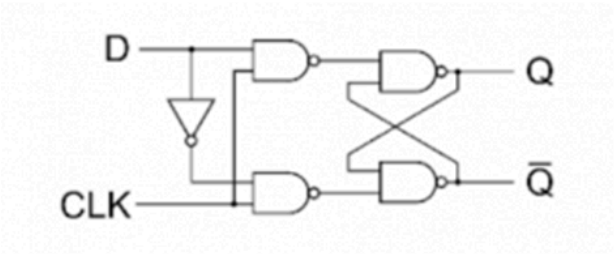


TRUTH TABLE

J	K	Q_N	Q_{N+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

$$Q_{N+1} = JQ'_N + K'Q_N$$

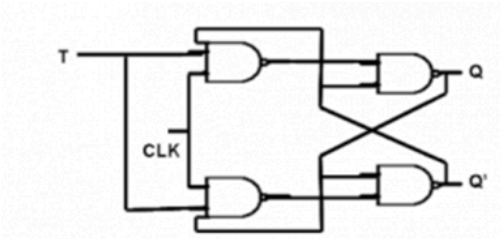
D-FLIP FLOP



Q	D	Q(t+1)
0	0	0
0	1	1
1	0	0
1	1	1

$$Q_{N+1} = D$$

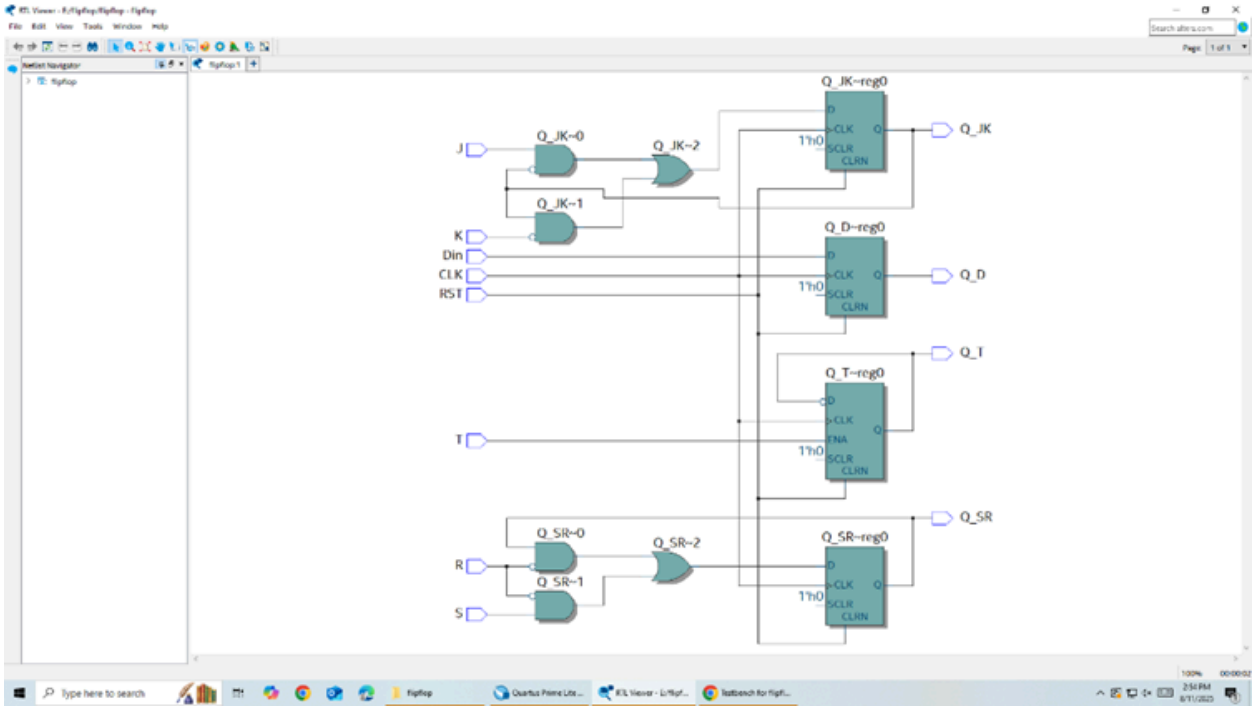
T-FLIP FLOP



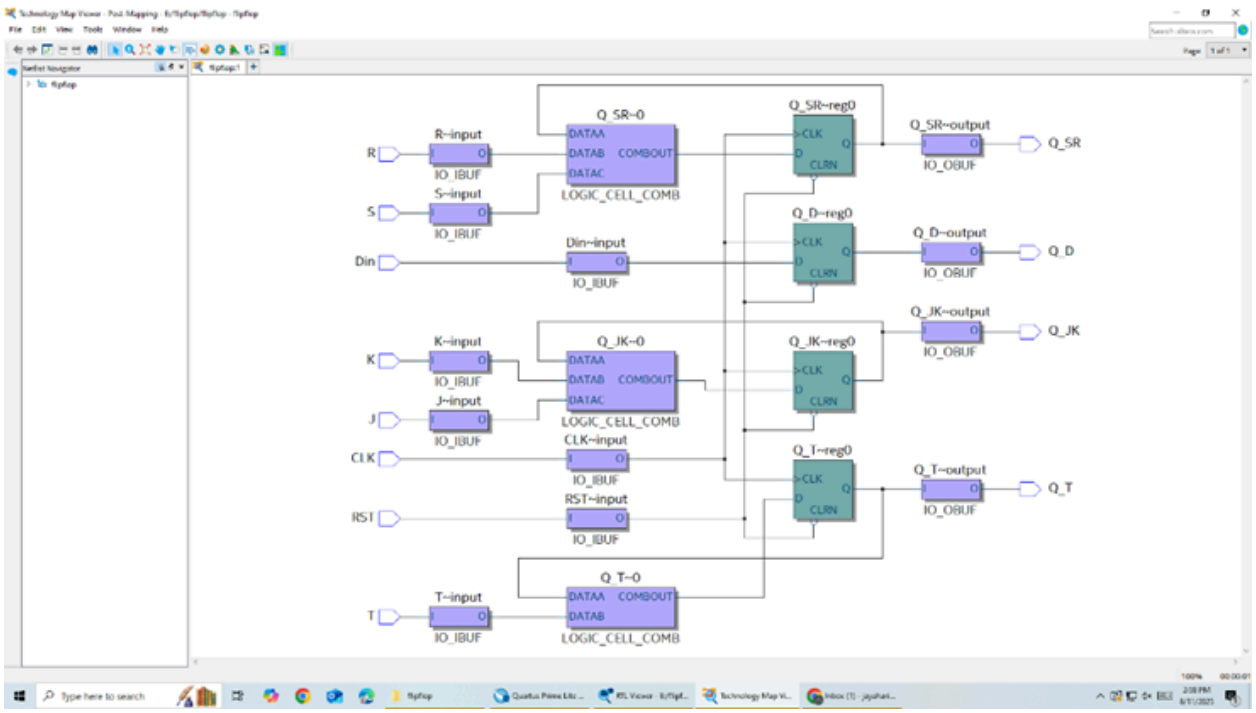
T	Q_n	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

$$Q_{N+1} = Q'_N T + Q_N T'$$

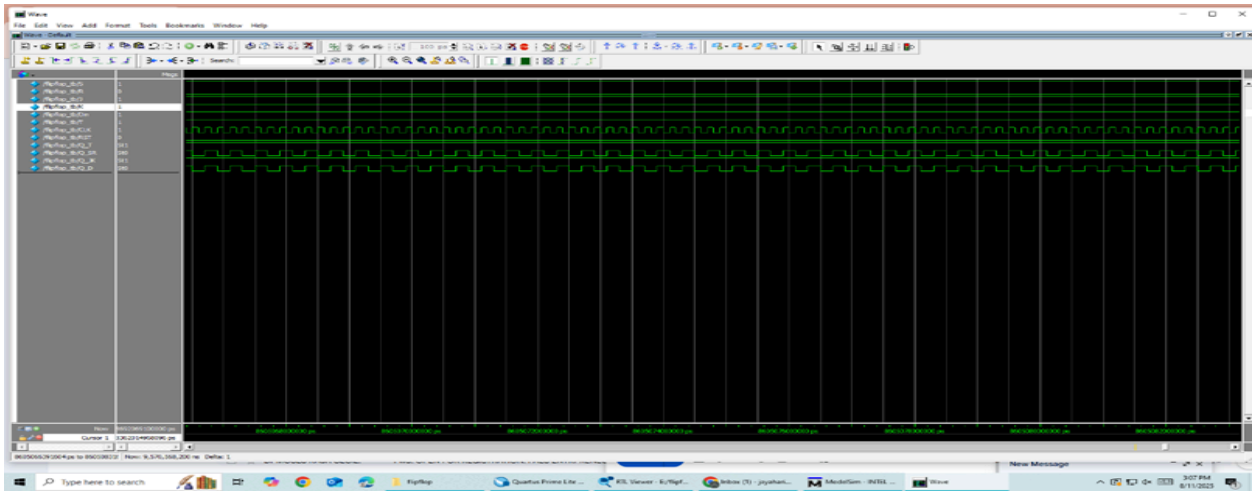
RTL SCHEMATIC:



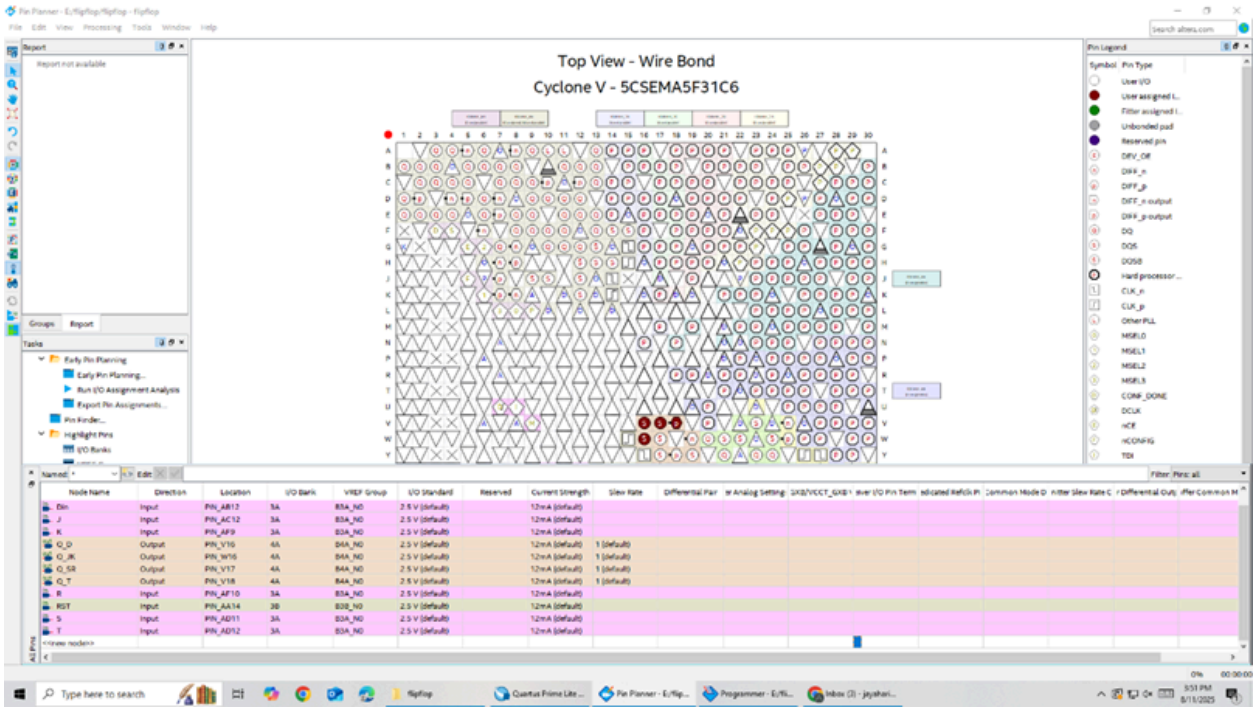
TECHNOLOGY SCHEMATIC:

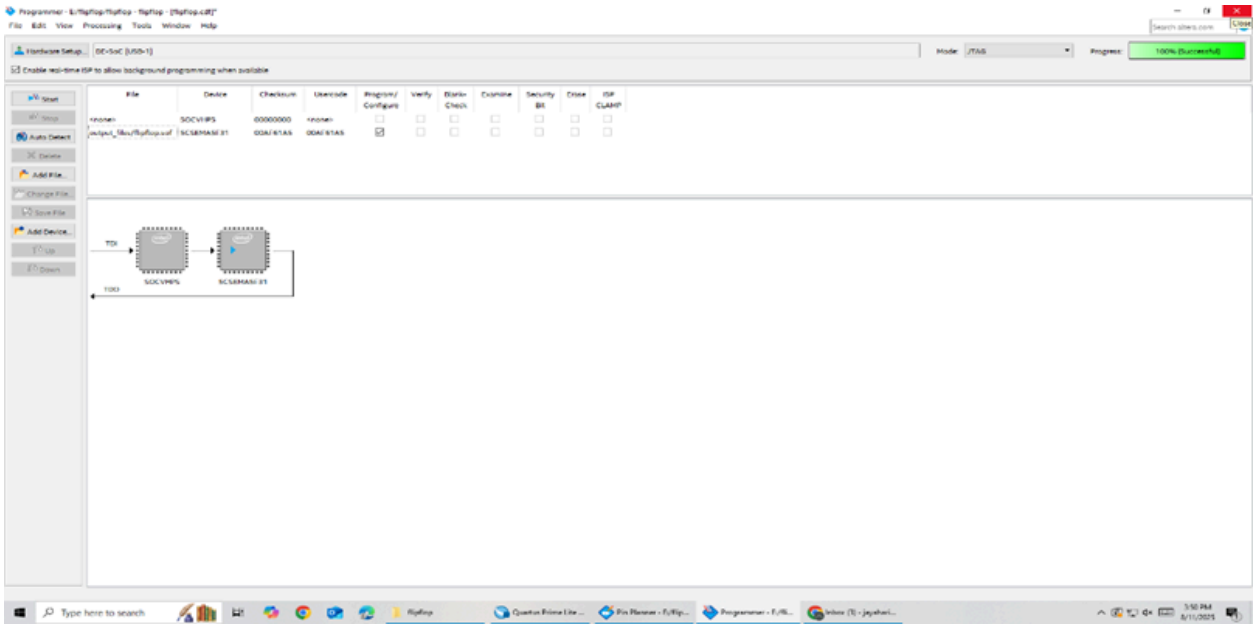


SIMULATION:



PIN CONFIGURATION & IMPLEMENTATION:




Programmer - E:/flipflop/flipflop - flipflop - [flipflop.cdf]*
File Edit View Processing Tools Window Help
Hardware Setup...
DE-SoC [USB-1]
Mode: JTAG
Progress:
100% (Successful)
Enable real-time ISP to allow background programming when available
Start
Stop
Auto Detect
Delete
Add File...
Change File...
Save File
Add Device...
Up
Down
File
Device
Checksum
Usercode
Program/ Configure
Verify
Blank-Check
Examine
Security Bit
Erase
ISP CLAMP
<none>
SOCVHPS
00000000
<none>
output_files/flipflop.sof
5CSEMA5E31
00AE61A5
00AE61A5
TDI
SOCVHPS
5CSEMA5E31
TDO
Type here to search
5:50 PM
6/11/2025