DESIGN, SIMULATION AND IMPLEMENTATION OF
4-BIT WALLACE TREE MULTIPLIER USING ALTERA FPGA

To design a 4-bit Wallace Tree multiplier using Verilog HDL and to perform functional simulation.

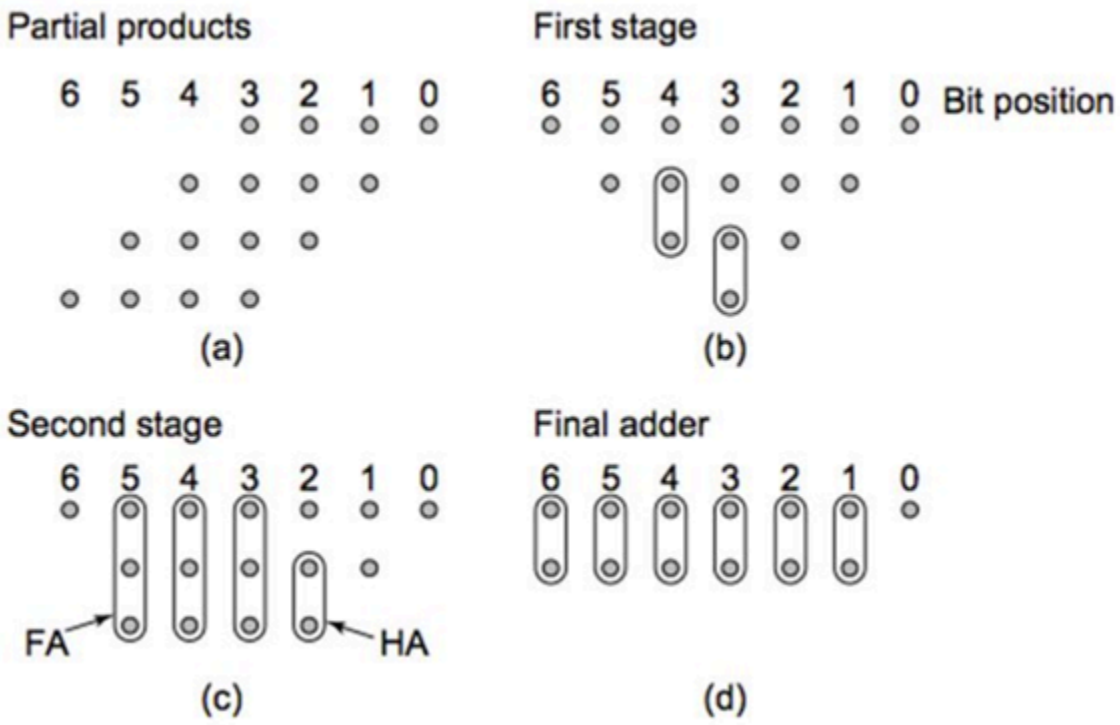
To synthesize the design and implement using Altera FPGA.

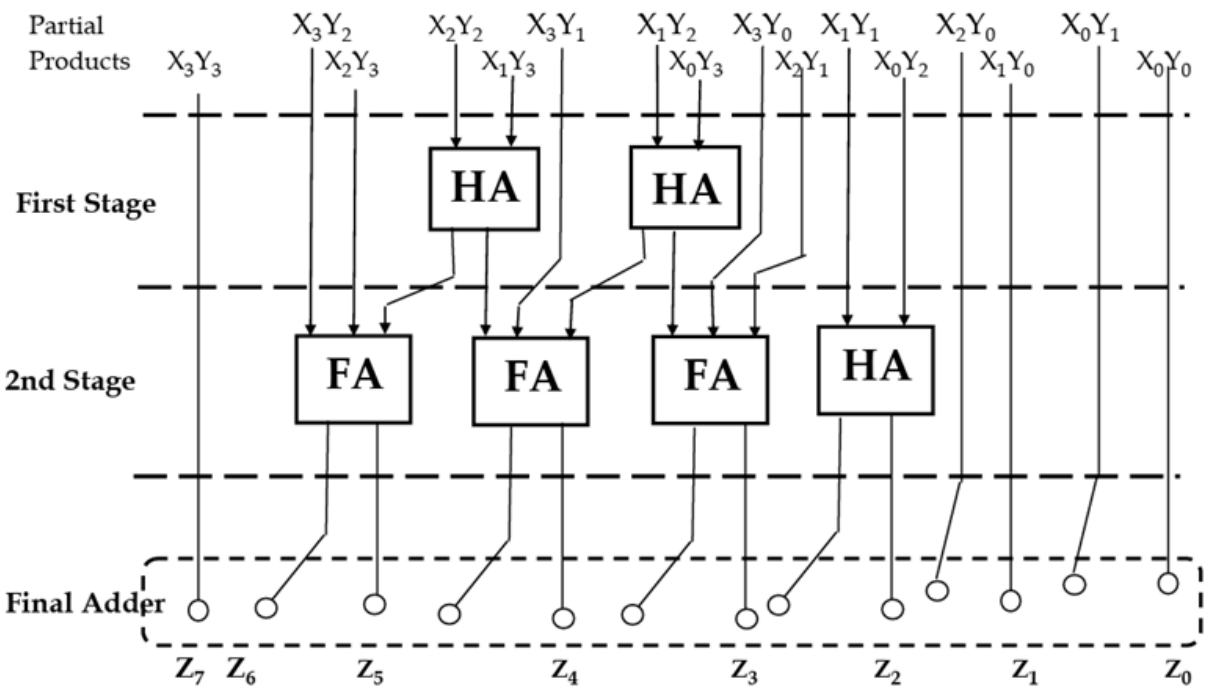
REQUIREMENTS:

EDA Tool: Altera Quartus Prime v17

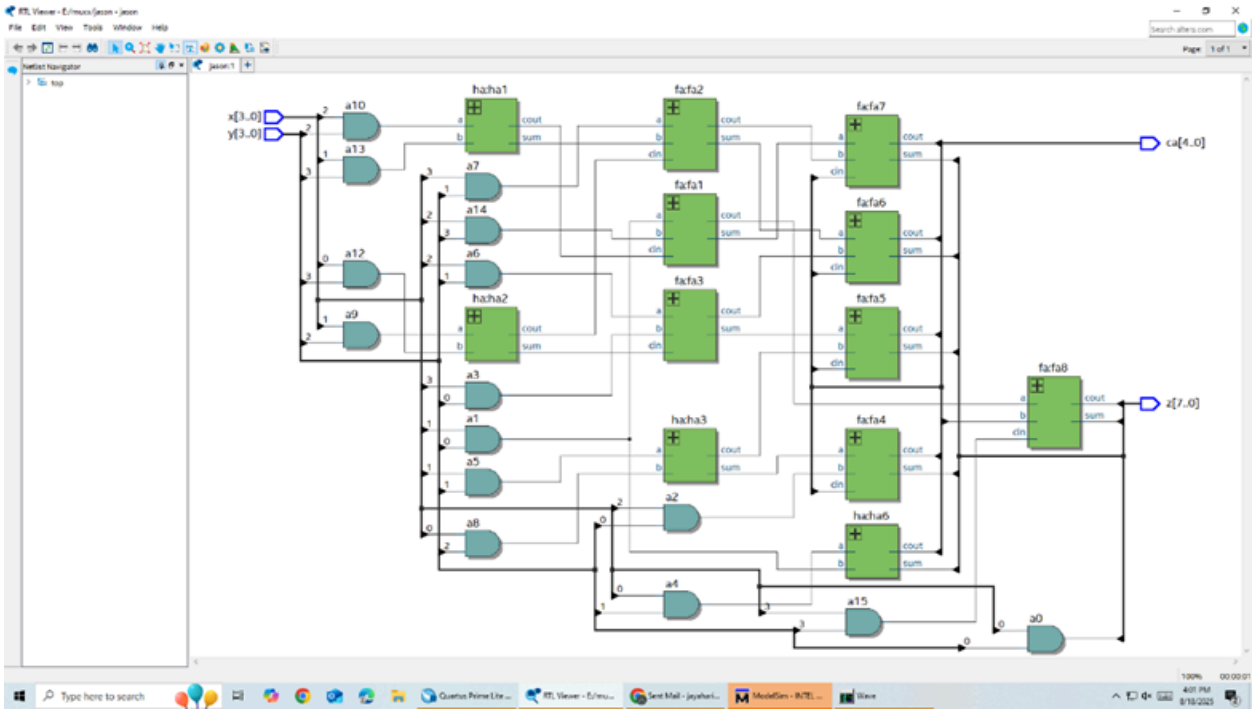
Hardware: DE1-SoC board

ARCHITECTURE :

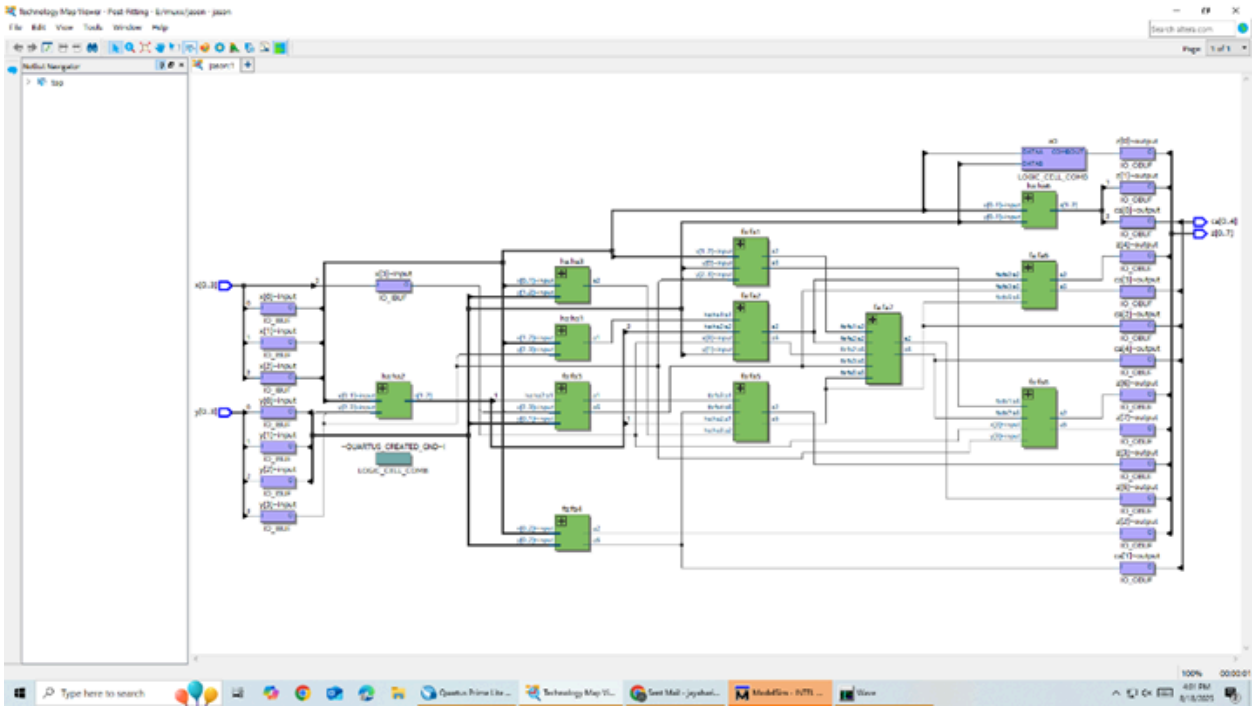




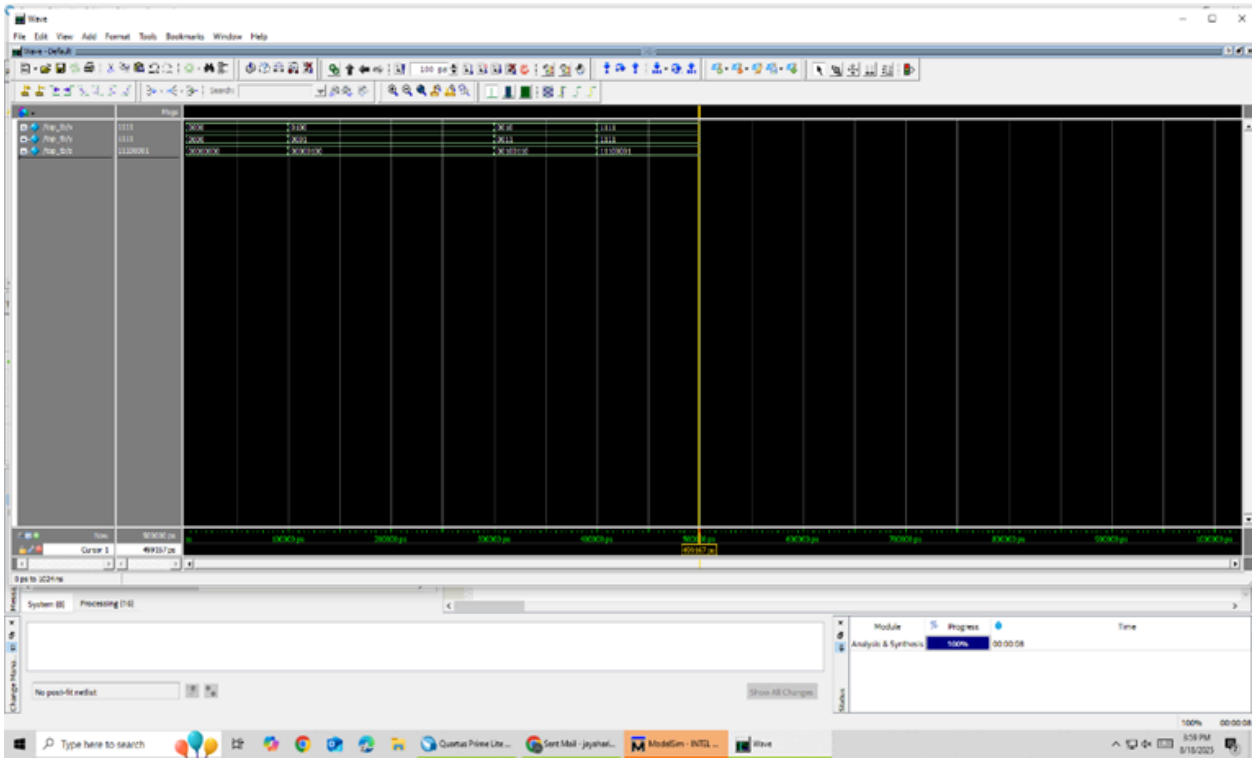
RTL SCHEMATIC:



TECHNOLOGY SCHEMATIC:



SIMULATION:



PIN CONFIGURATION & IMPLEMENTATION: