DESIGN , SIMULATION AND IMPLEMENTATIONOFDate:
SYNCHRONOUS SINGLE PORT RAM

• To design a 32 x 8 bit(256 bit) synchronous single port RAM using Verilog HDL and toperform functional simulation.

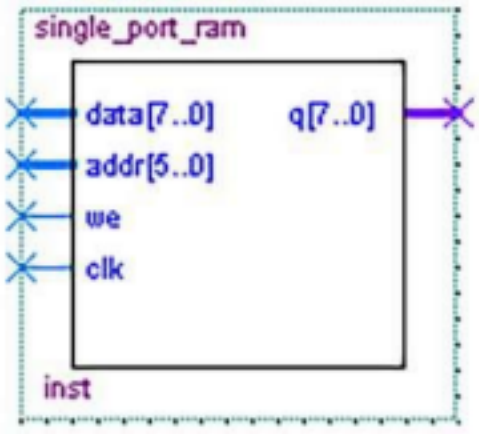
• To synthesize the design and implement using Altera FPGA.

REQUIREMENTS:

EDA Tool: Altera Quartus Prime v17

Hardware: DE1-SoC board

ARCHITECTURE :



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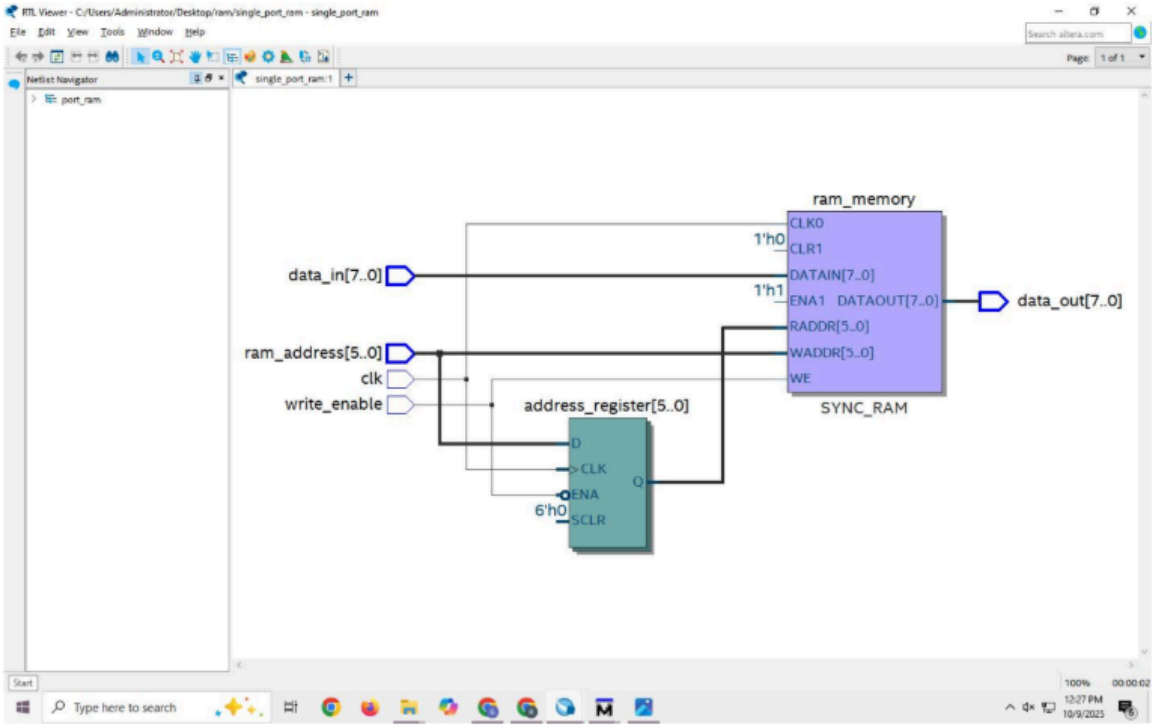
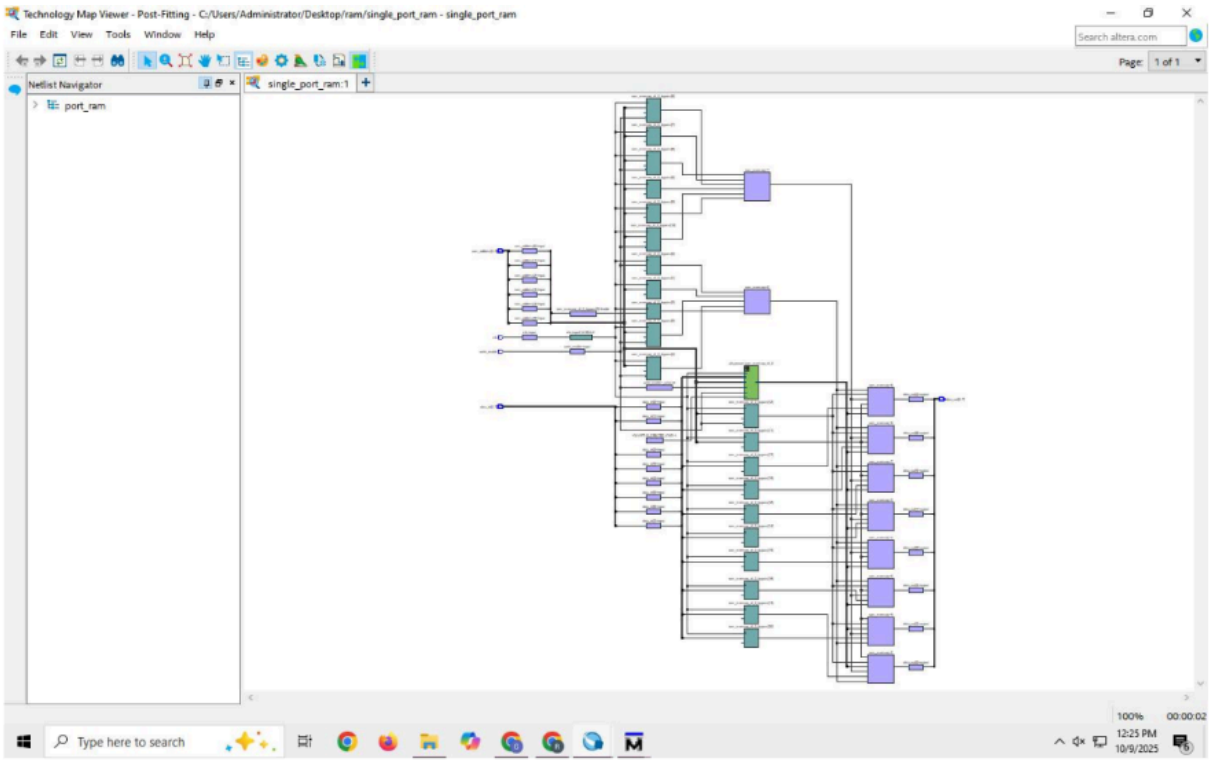
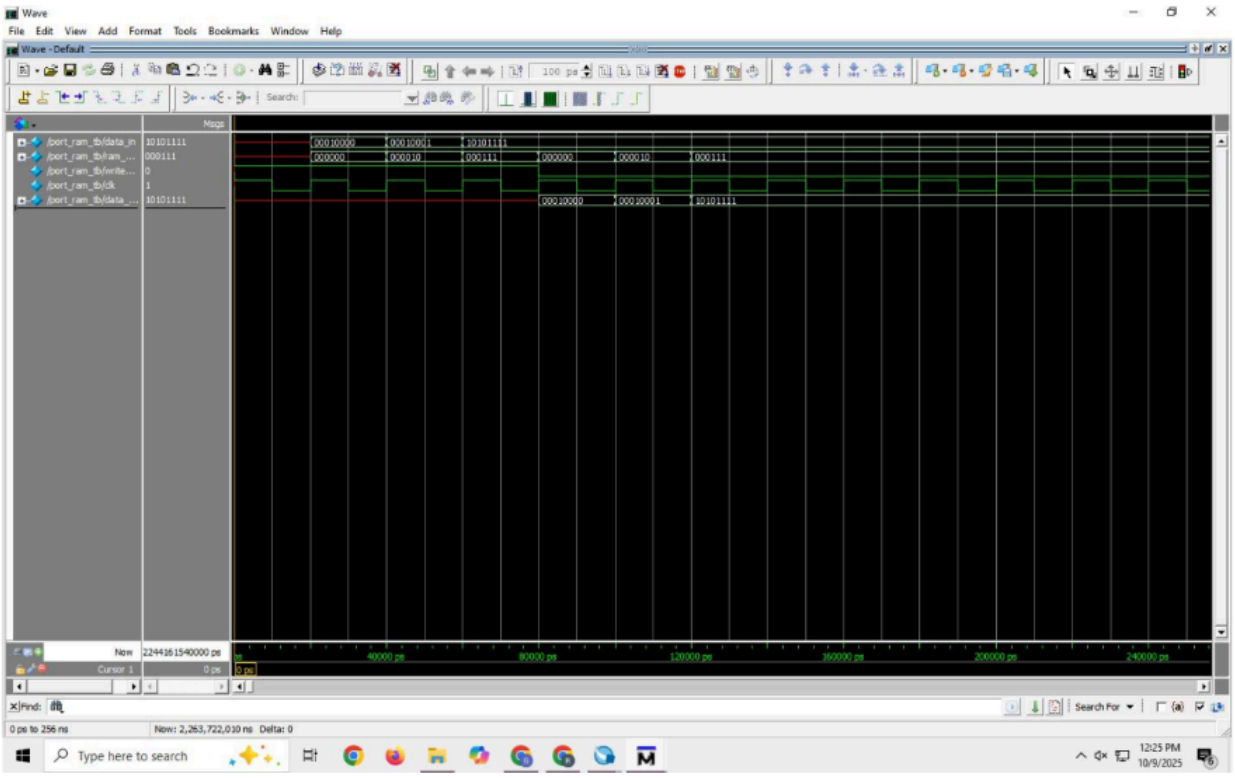


TECHNOLOGY SCHEMATIC:



SIMULATION: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/port_ram_tb/write...
/port_ram_tb/clk
/port_ram_tb/data_...
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40000 ps
80000 ps
120000 ps
160000 ps
200000 ps
240000 ps
Find:
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Now: 2,263,722,010 ns Delta: 0
Type here to search
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10/9/2025