

# DESIGN, SIMULATION AND IMPLEMENTATION OF 1-BIT FULL ADDER USING ALTERA FPGA

To design a 1-BIT FULL ADDER using Verilog HDL and to perform functional simulation. To synthesize the design and implement using Altera FPGA.

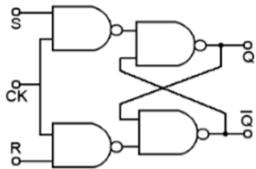
## **REQUIREMENTS:**

EDA Tool: Altera Quartus Prime v17

Hardware: DE1-SoC board

## **FLIP FLOPS & CHARACTERISTIC EQUATIONS:**

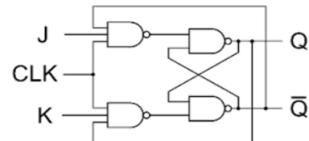
**JK FLIP**



**TRUTH TABLE**

S	R	$Q_N$	$Q_{N+1}$
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	-
1	1	1	-

**SR FLIP-FLOP**



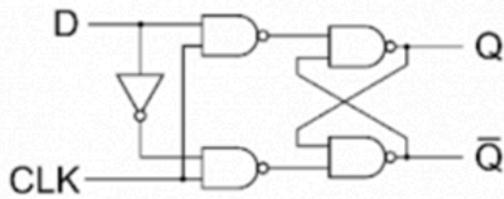
**TRUTH TABLE**

J	K	$Q_N$	$Q_{N+1}$
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

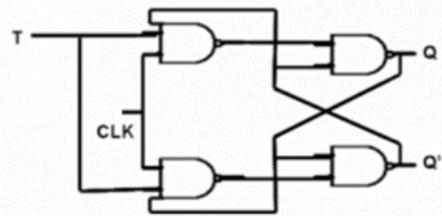
$$Q_{N+1} = Q_N R' + S R'$$

$$Q_{N+1} = J Q'_N + K' Q_N$$

**D-FLIP FLOP**



**T-FLIP FLOP**



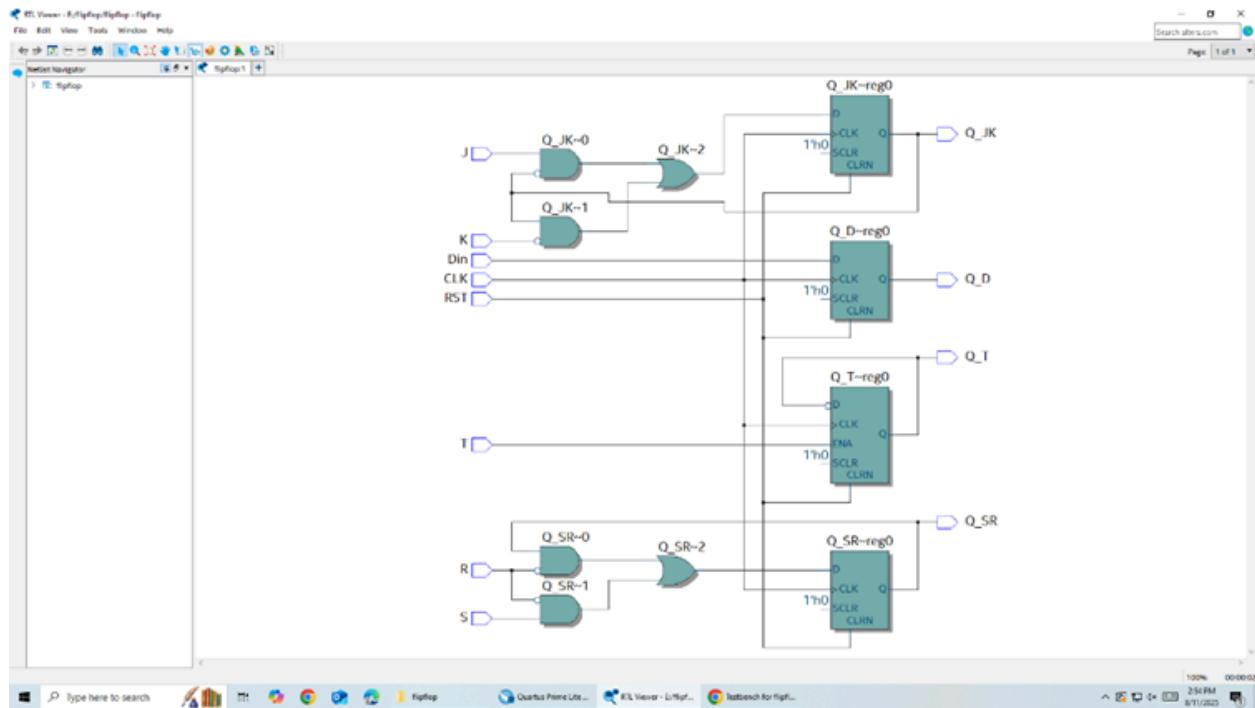
Q	D	Q(t+1)
0	0	0
0	1	1
1	0	0
1	1	1

T	Q <sub>n</sub>	Q <sub>n+1</sub>
0	0	0
0	1	1
1	0	1
1	1	0

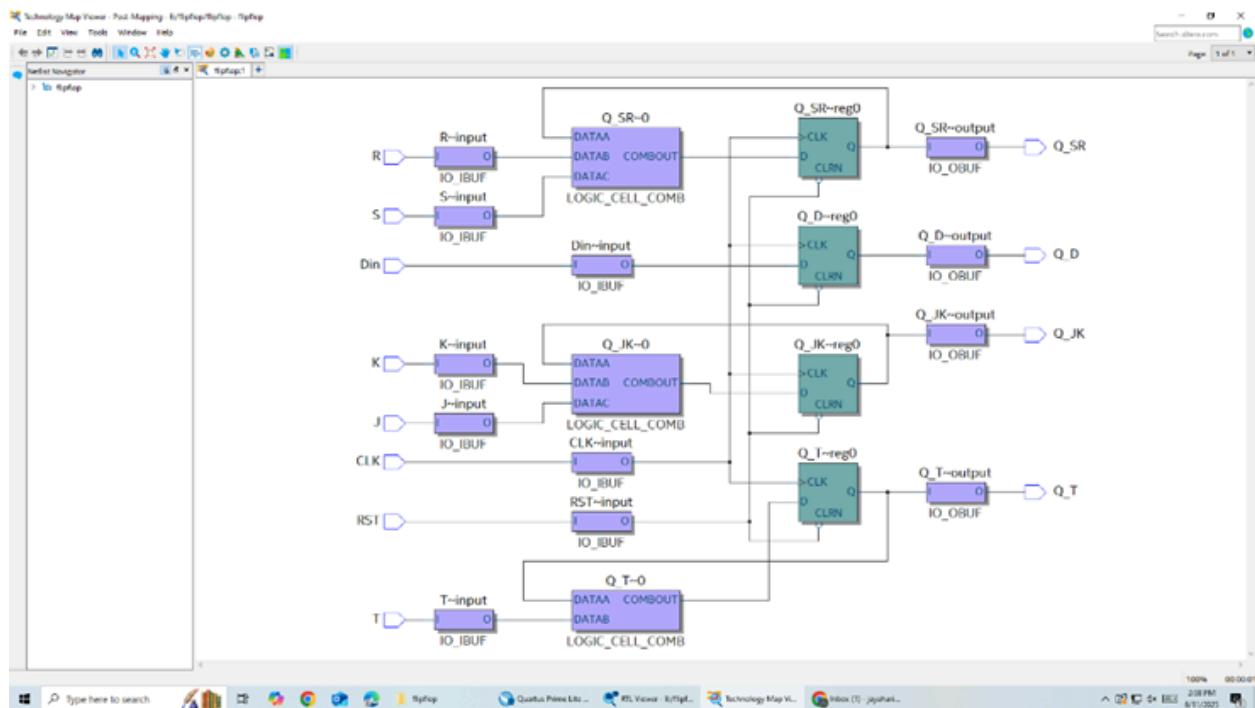
$$Q_{N+1} = D$$

$$Q_{N+1} = Q'_N T + Q_N T'$$

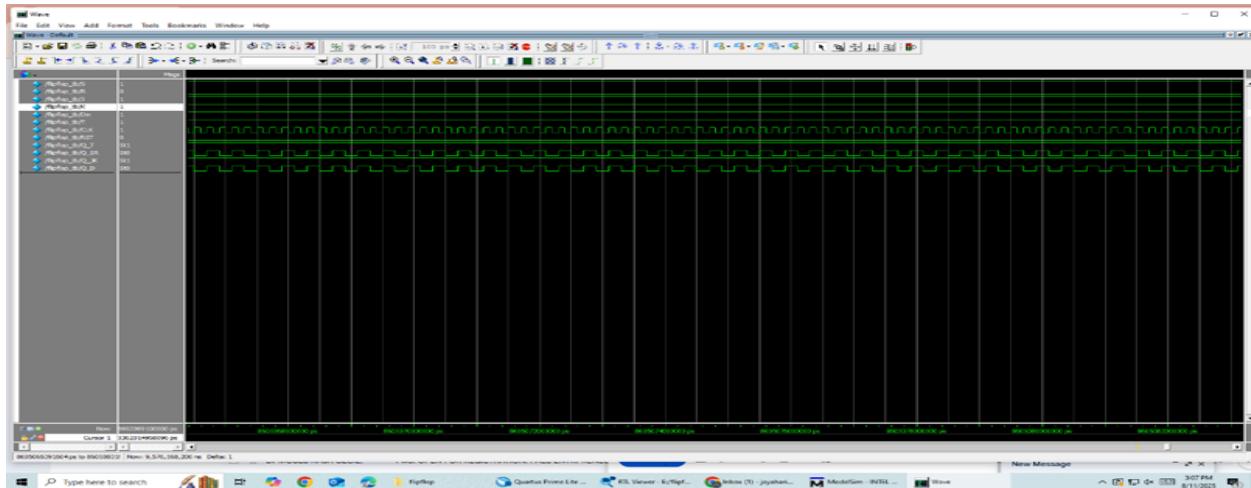
## RTL SCHEMATIC:



## TECHNOLOGY SCHEMATIC:



## SIMULATION:



## **PIN CONFIGURATION & IMPLEMENTATION:**

