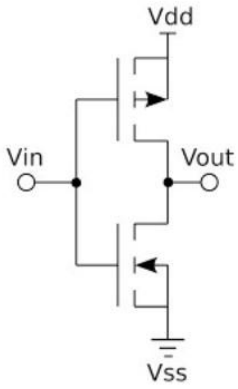
DESIGN OF LAYOUT - CMOS INVERTER

AIM:

To design and simulate CMOS Inverting amplifier using Cadence with 180nm technology

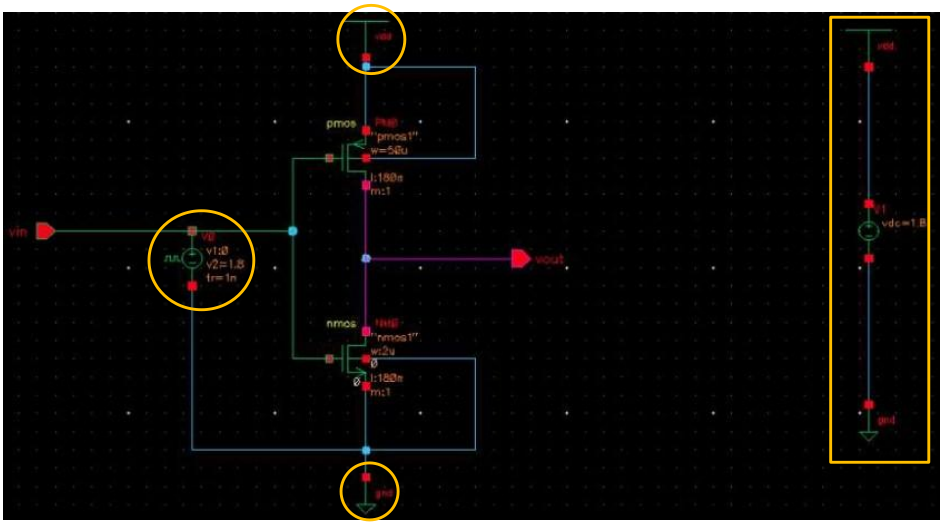
SOFTWARE: Cadence Virtuoso, Cadence spectre

CIRCUIT DIAGRAM:

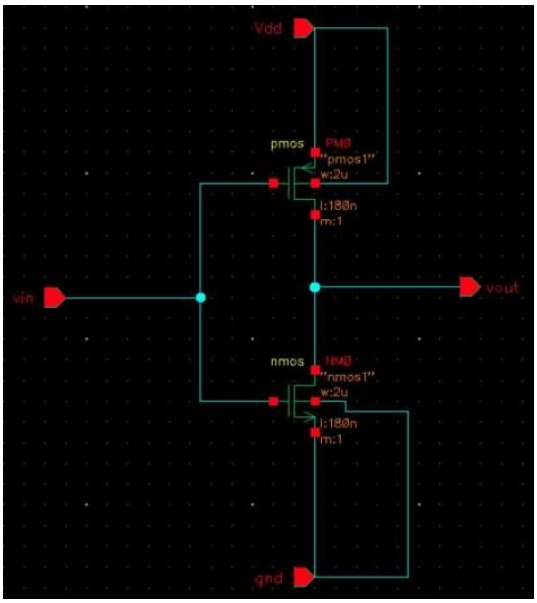


PROCEDURE:

1. **Open Existing CMOS Inverter Design.**
    - Launch Cadence Virtuoso.
    - Open the CMOS Inverter design created in Experiment 5 from the Library Manager.



2. **Modify Power Supply Connections in the Schematic.**
    - **Remove** the existing **Vdd, GND**, and any **power supply blocks** (*marked using yellow square or circle*).
    - **Add ports** for **Vdd** and **GND:**
        - Go to: ***Create > Pin***
        - Add **input/output** pins as needed (set direction to input/output accordingly).
        - Name them as **Vdd** and **GND**.



3. **Launch the Layout Editor**
   - In the schematic window, go to the top-left corner:
     - ***Launch > Layout XL***
     - Choose "**Create New File**" when prompted.
     - Click **OK** to open the new layout view.

4. **Generate Layout from Schematic.**
   - In the Layout Editor, go to:
     - ***Connectivity > Generate > All from Source***
   - In the dialog box:
     - Set **Distance** to **0.12**
     - Check the box **"In-Boundary"**
     - Click **OK**
5. **Display Full Layout Details**
   - Press Shift + F to view the full layout with boundaries and device details.
   - **To edit transistor properties**:
     - Right-click on a **PMOS** or **NMOS** → Select **Properties**
     - Under **Parameters**:
       - Set **Bodytype** to detached (to separate the bulk terminal)
       - Check the **Left Tap** option
6. **Connect Same Layer Wires**
   - Press the key **P** to draw paths (wires) between **same layers** (e.g., poly to poly or metal1 to metal1).
7. **Add Vias (Different Layer Connections)**
   - To connect **different layers**, use **vias**:
     - Go to: ***Create > Via***
     - OR press the shortcut key **O**
     - Choose **Via Type**: e.g., M1-Poly (to connect metal1 to poly layer)

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8. **Access Technology Path (for DRC/LVS)**

- In the **Linux file explorer**:
  - Navigate to:
    Home > Install > Foundry > Analog > 180nm > Ausra-tech-lib
  - Right-click on the appropriate technology folder → **Properties**
  - **Copy the full path** of the technology file

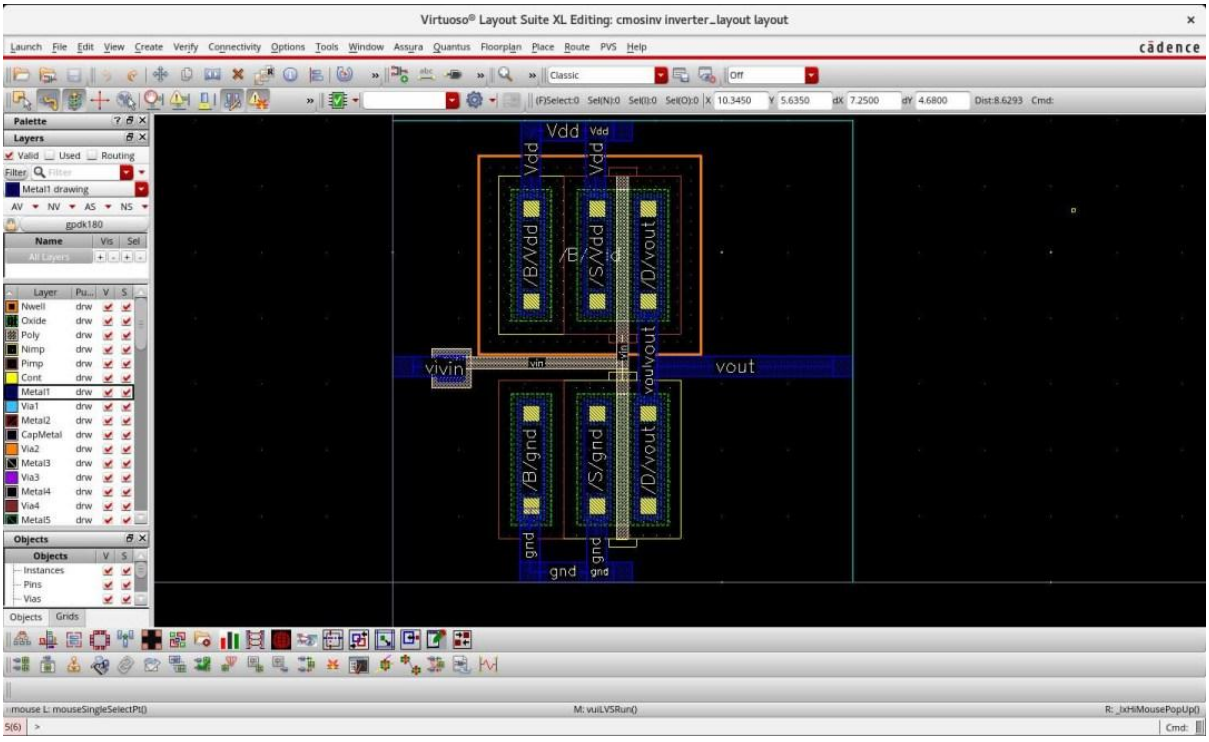
9. **Run DRC (Design Rule Check)**

- In the layout window, go to:
  - ***Asura > Run DRC***
- In the DRC window:
  - Paste the **technology path** copied earlier
  - Set **Technology** to GDPK 180
  - Click **Apply** to run DRC and fix any design rule violations

10. **Run LVS (Layout vs Schematic)**

- After successful DRC:
  - Go to: ***Asura > Run LVS***
  - Again, paste the **technology path**
  - Set **Technology** to GDPK 180
  - Click **Apply**
- LVS will compare the layout with the schematic to ensure both are equivalent.

LAYOUT OUTPUT:



SUMMARY OF LVS: