DESIGN, SIMULATION AND IMPLEMENTATION OF 1-BIT FULL ADDER USING ALTERA FPGA

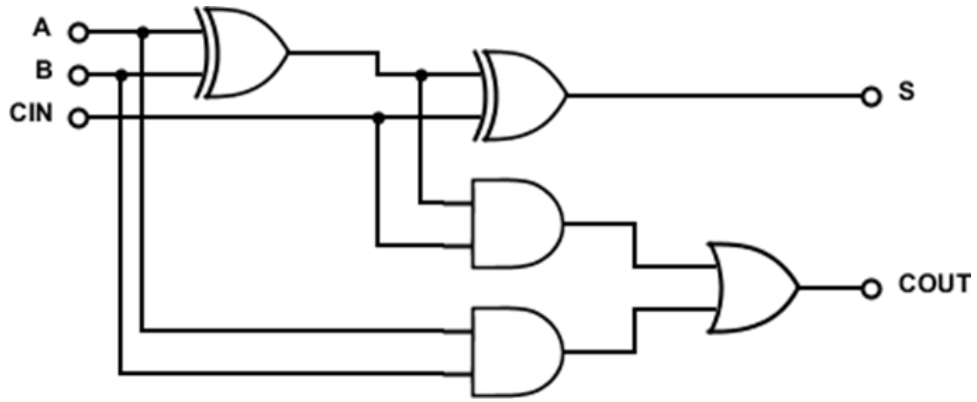
To design a 1-BIT FULL ADDER using Verilog HDL and to perform functional simulation.To synthesize the design and implement using Altera FPGA.

REQUIREMENTS:

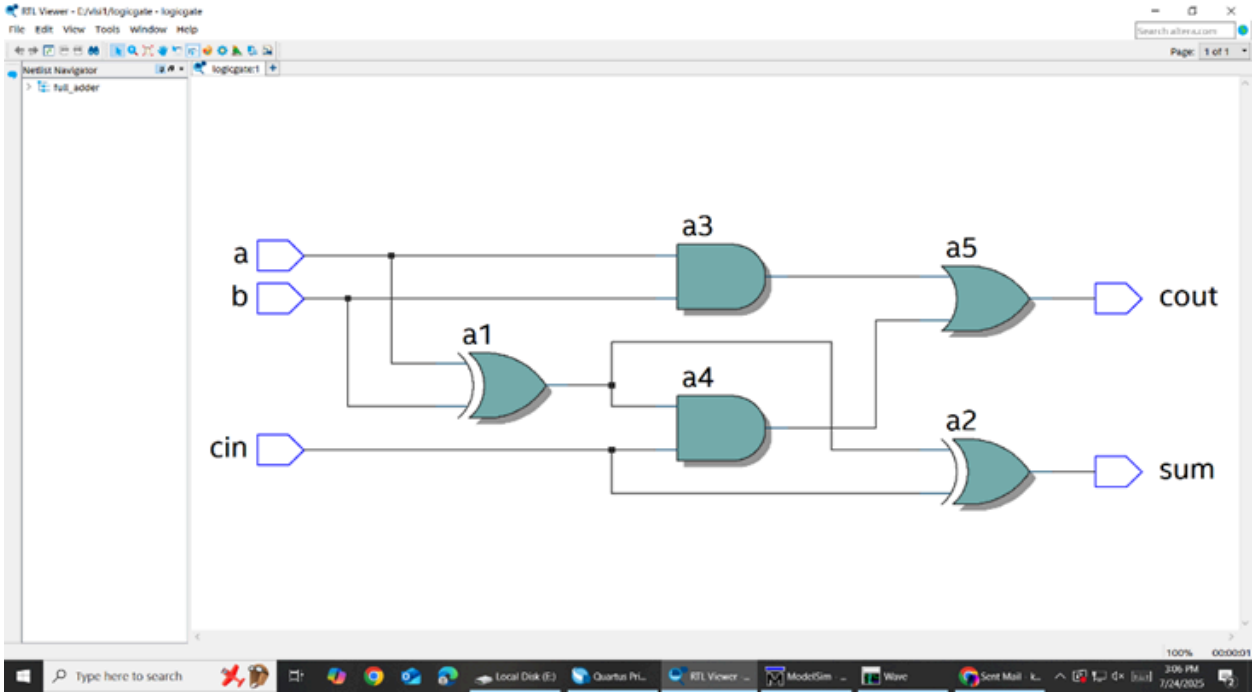
EDA Tool: Altera Quartus Prime v17

Hardware: DE1-SoC board

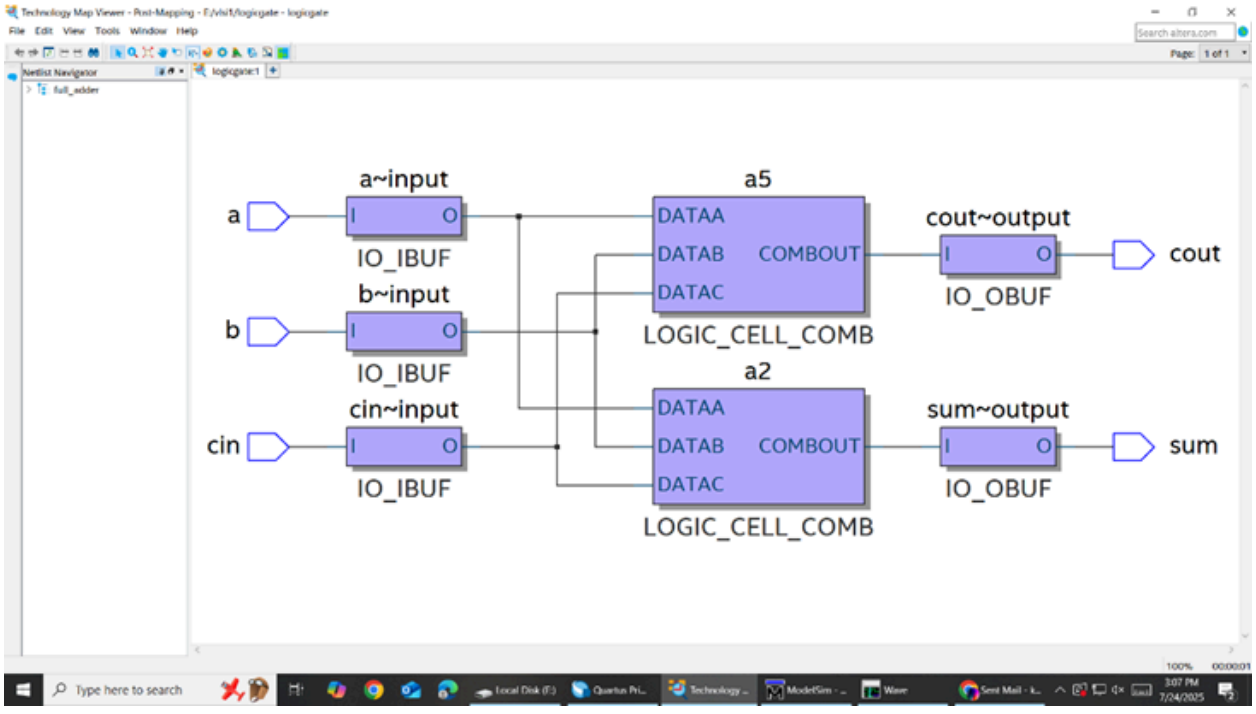
LOGIC DIAGRAM:



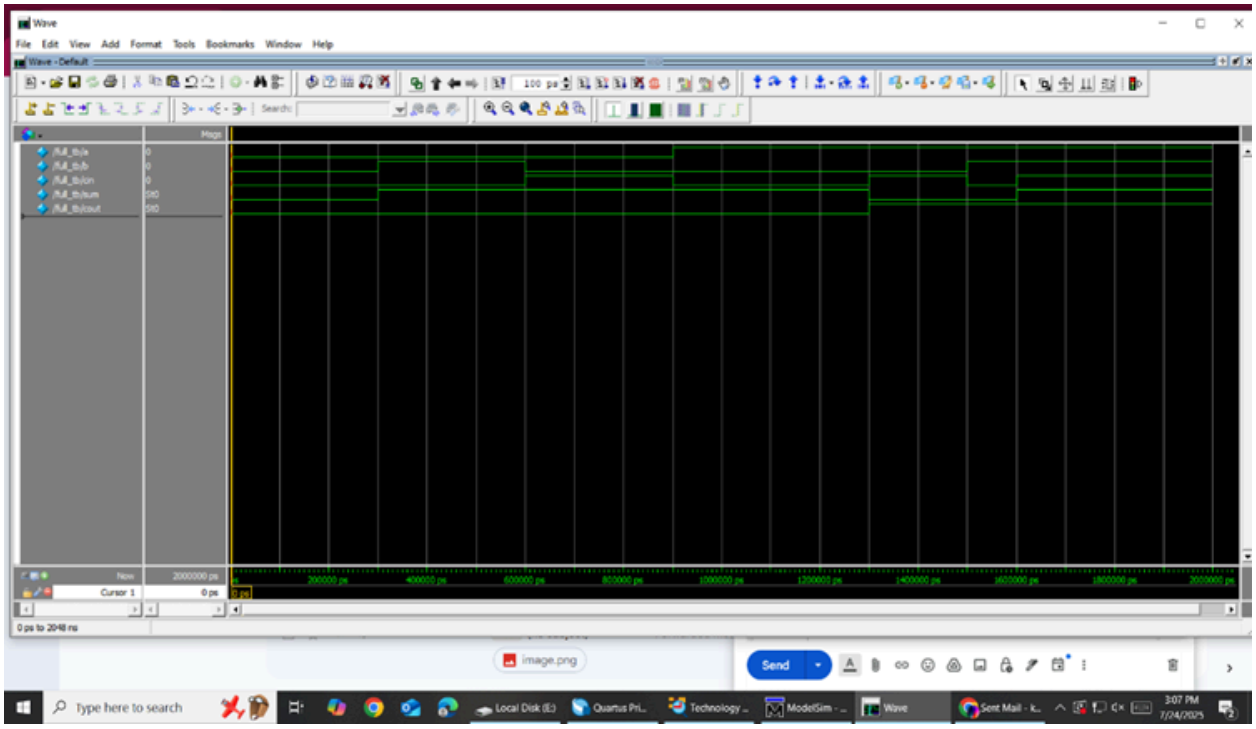
RTL SCHEMATIC:



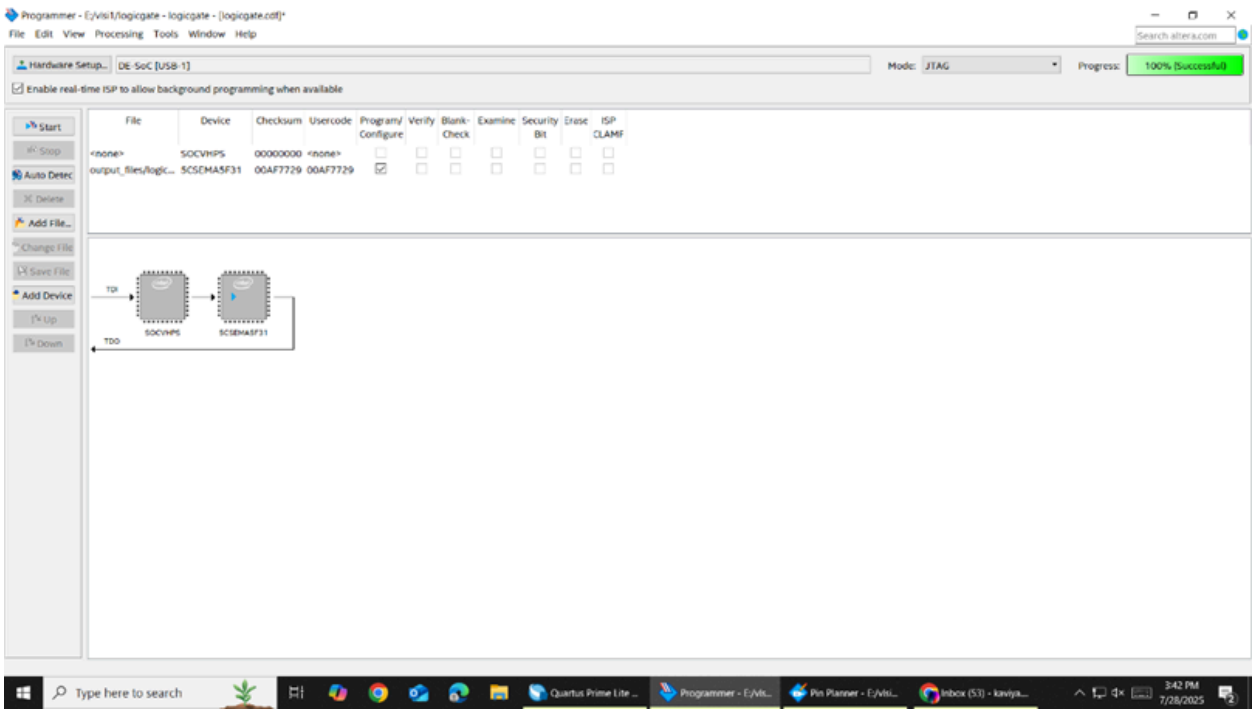
TECHNOLOGY SCHEMATIC:



SIMULATION:



PIN CONFIGURATION & IMPLEMENTATION:



PIN_AB12-a(sw0)

PIN_AC12-b(sw1)

PIN_AF9 -c(sw2)

PIN_V16-carry(led0)

PIN_W16-sum(led1)