Lecture 14

CHAPTER 6

SYNCHRONOUS COUNTERS

- Synchronous counters are different from ripple counters in that clock pulses are applied to the inputs of all flip-flops.
- A common clock triggers all flip-flops simultaneously, rather than one at a time in succession as in a ripple counter.
- The decision whether a flip-flop is to be complemented is determined from the values of the data inputs, such as *T* or *J* and *K* at the time of the clock edge.
- If $T = 0$ or $J = K = 0$, the flip-flop does not change state.
- If $T = 1$ or $J = K = 1$, the flip-flop complements.

Binary Counter

- The design of a synchronous binary counter is so simple that there is no need to go through a sequential logic design process.
- In a synchronous binary counter, the flip-flop in the least significant position is complemented with every pulse.
- *A flip-flop in any other position is complemented when all the bits in the lower significant positions are equal to 1* .
- For example, if the present state of a four-bit counter is *A*3*A*2*A*1*A*0 = 0011, the next count is 0100.
- *A*0 is always complemented.
- *A*1 is complemented because the present state of *A*0 = 1.
- *A*2 is complemented because the present state of *A*1*A*0 = 11.
- However, *A*3 is not complemented, because the present state of *A*2*A*1*A*0 = 011, which does not give an all-1's condition.

Binary Counter

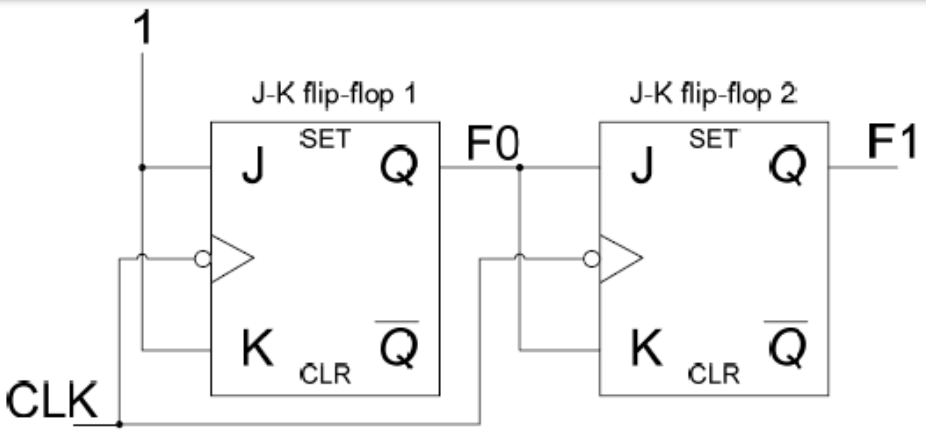


Figure 27.3a 2-bit Synchronous Counter

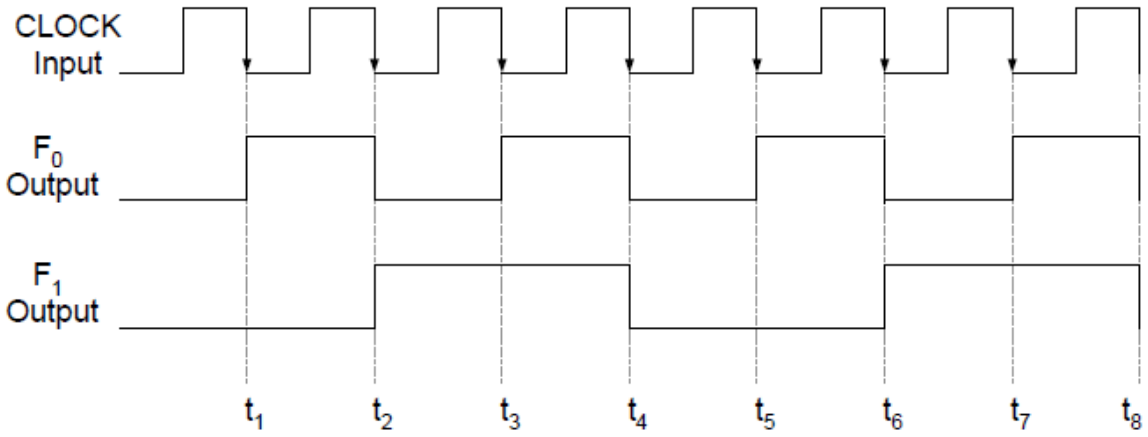


Figure 27.3b Timing diagram of a 2-bit Synchronous Counter

Binary Counter

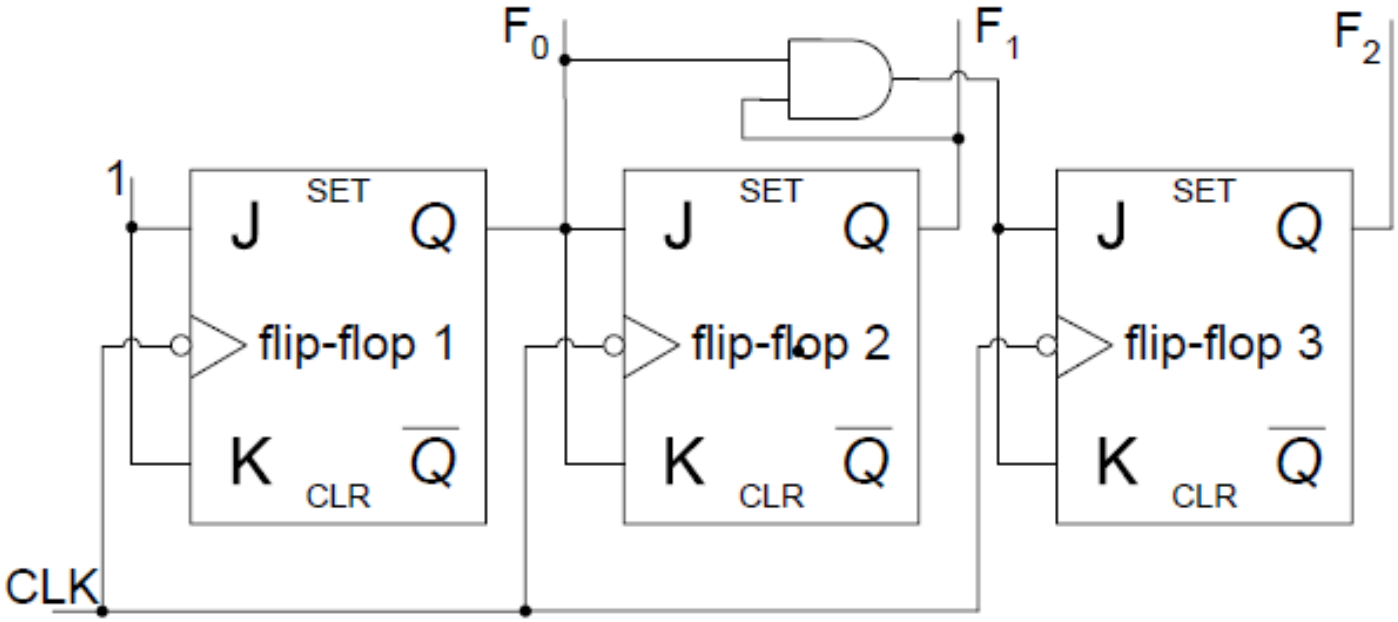


Figure 27.4a A 3-bit Synchronous Counter

Binary Counter

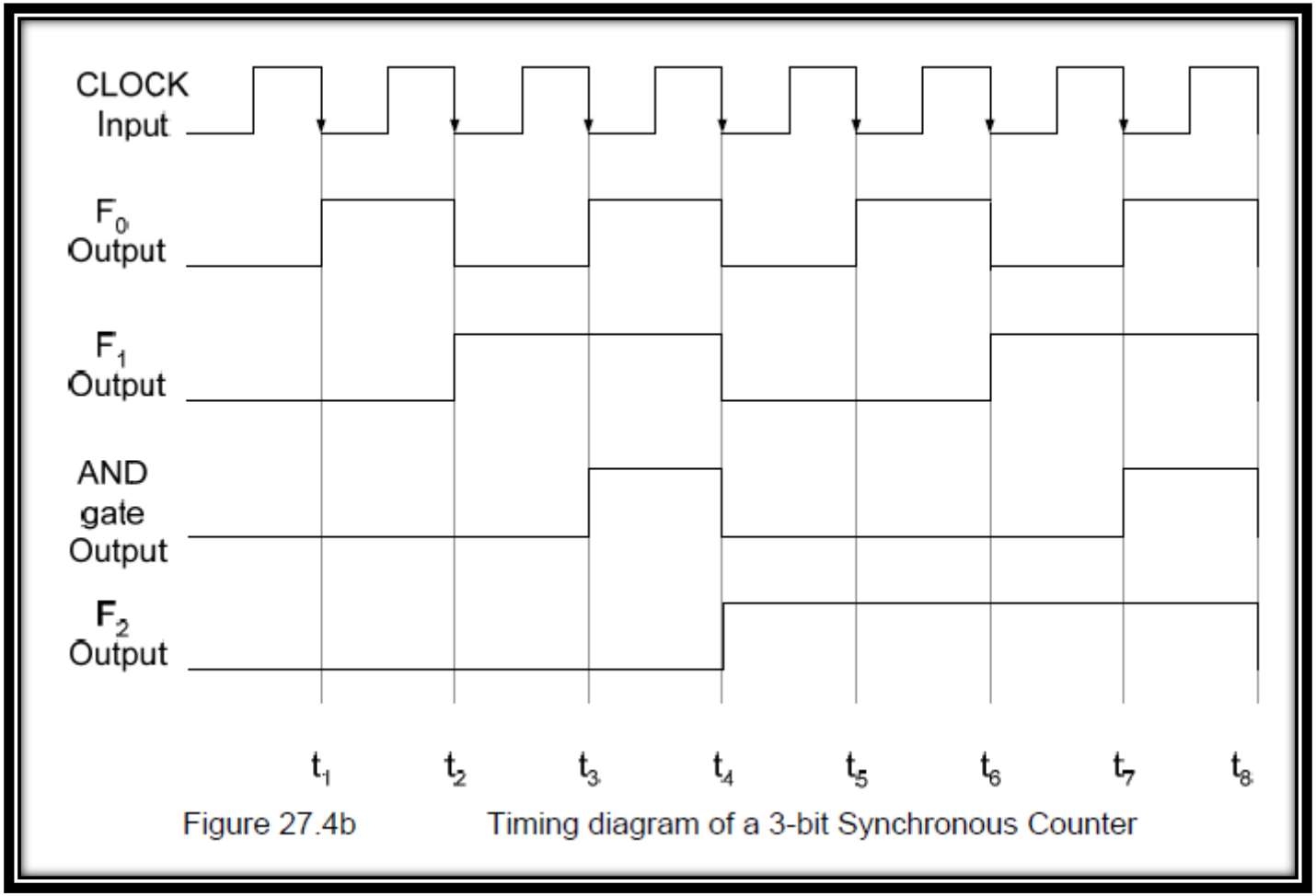


Figure 27.4b Timing diagram of a 3-bit Synchronous Counter

Binary Counter

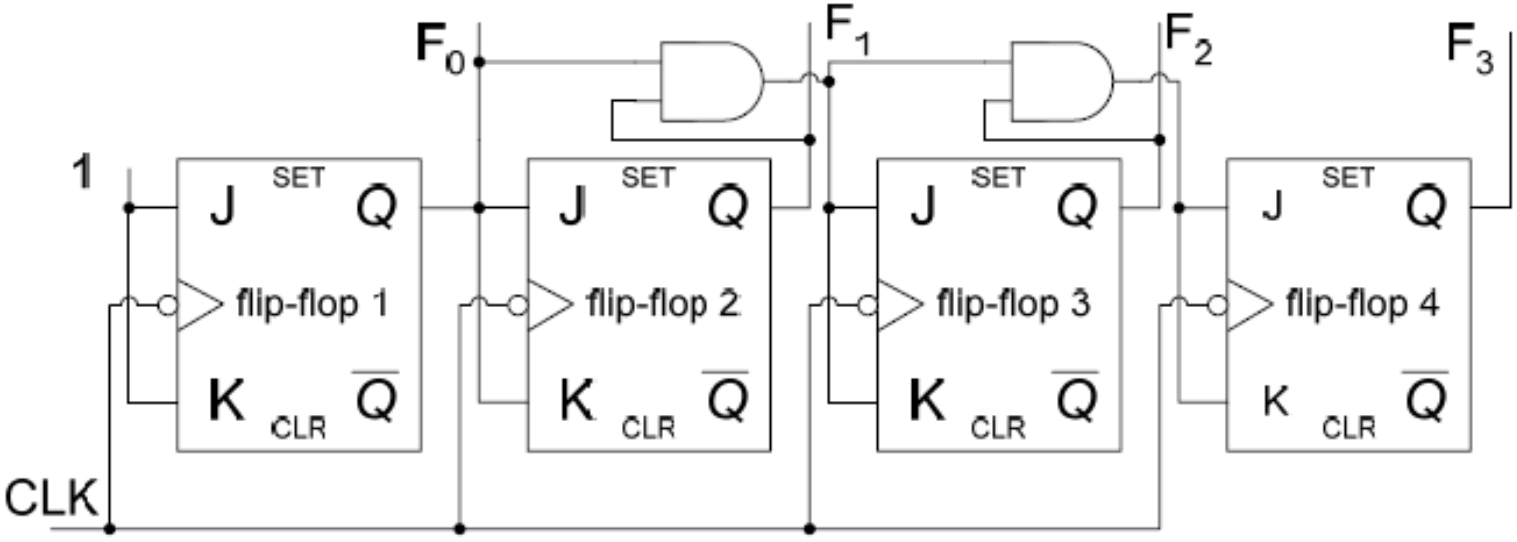


Figure 27.5 4-bit Synchronous Binary Counter

Binary Counter

- Synchronous binary counters have a regular pattern and can be constructed with complementing flip-flops and gates.
- The regular pattern can be seen from the four-bit counter depicted in Fig. 6.12 .
- The *C* inputs of all flip-flops are connected to a common clock.
- The counter is enabled by *Count_enable*.
- If the enable input is 0, all *J* and *K* inputs are equal to 0 and the clock does not change the state of the counter.
- The first stage, *A*0, has its *J* and *K* equal to 1 if the counter is enabled.

Binary Counter

- The other *J* and *K* inputs are equal to 1 if all previous least significant stages are equal to 1 and the count is enabled.
- The chain of AND gates generates the required logic for the *J* and *K* inputs in each stage.
- The counter can be extended to any number of stages, with each stage having an additional flip-flop and an AND gate that gives an output of 1 if all previous flip-flop outputs are 1.

Binary Counter

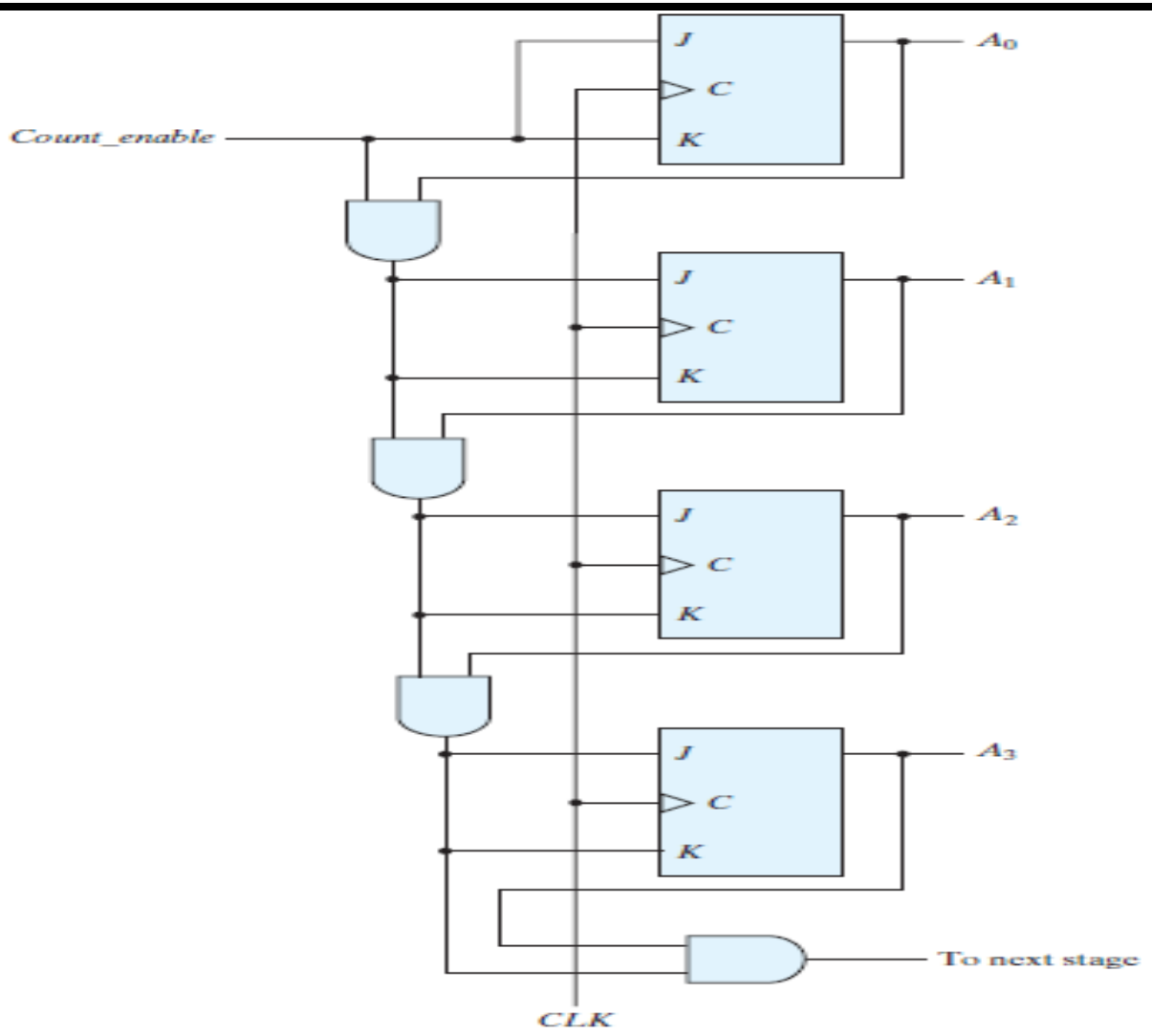


FIGURE 6.12
Four-bit synchronous binary counter

Up–Down Binary Counter

- A synchronous countdown binary counter goes through the binary states in reverse order, from 1111 down to 0000 and back to 1111 to repeat the count.
- It is possible to design a countdown counter in the usual manner, but the result is predictable by inspection of the downward binary count.
- The bit in the least significant position is complemented with each pulse.
- *A bit in any other position is complemented if all lower significant bits are equal to 0.*
- For example, the next state after the present state of 0100 is 0011.

Up–Down Binary Counter

- The least significant bit is always complemented.
- The second significant bit is complemented because the first bit is 0.
- The third significant bit is complemented because the first two bits are equal to 0.
- But the fourth bit does not change, because not all lower significant bits are equal to 0.
- The two operations can be combined in one circuit to form a counter capable of counting either up or down.
- The circuit of an up–down binary counter using *T* flip-flops is shown in Fig. 6.13 .

Up–Down Binary Counter

- It has an up control input and a down control input.
- When the up input is 1, the circuit counts up, since the *T* inputs receive their signals from the values of the previous normal outputs of the flip-flops.
- When the down input is 1 and the up input is 0, the circuit counts down, since the complemented outputs of the previous flip-flops are applied to the *T* inputs.
- When the up and down inputs are both 0, the circuit does not change state and remains in the same count.
- When the up and down inputs are both 1, the circuit counts up.
- This set of conditions ensures that only one operation is performed at any given time.

Up–Down Binary Counter

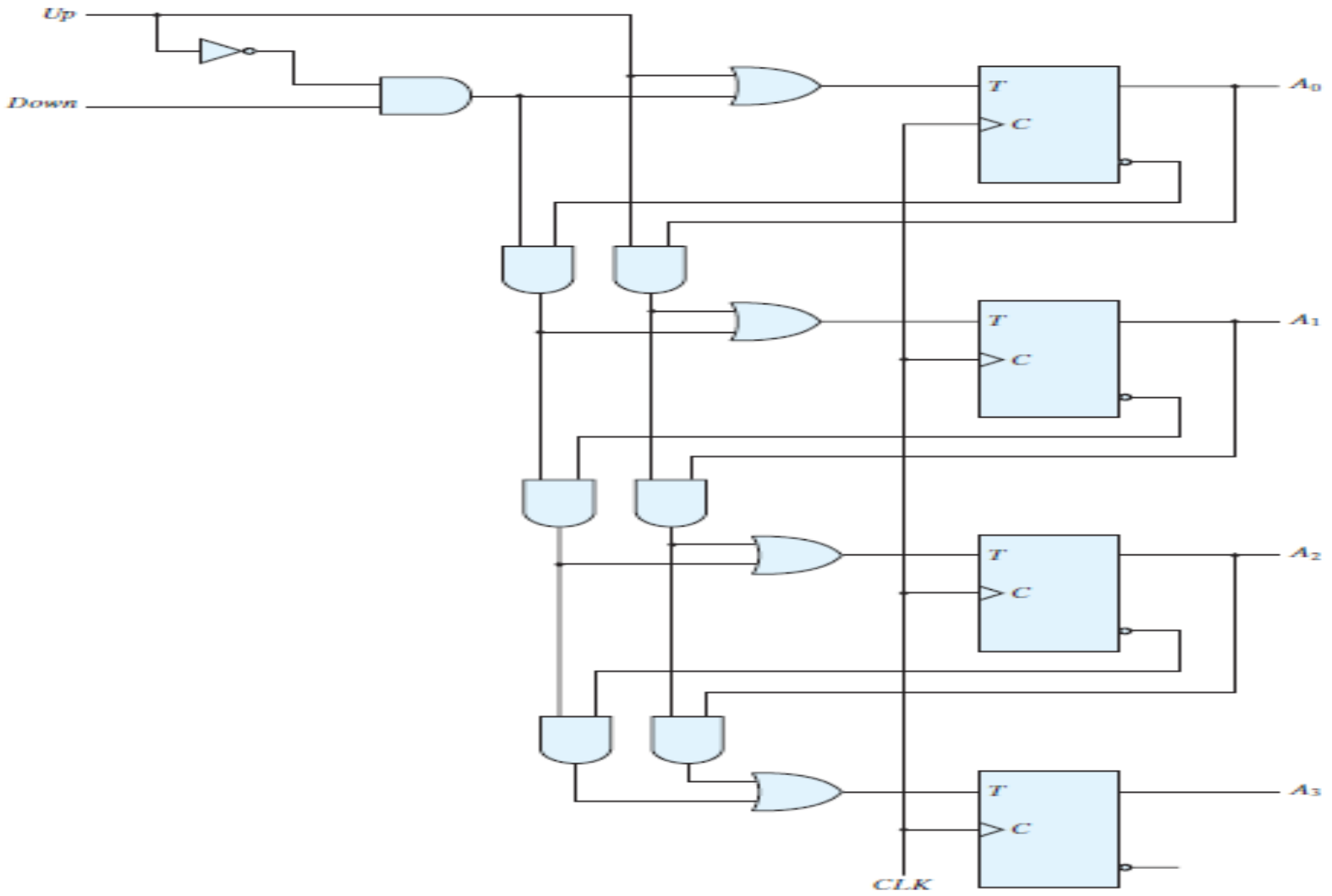


FIGURE 6.13
Four-bit up–down binary counter

BCD Counter

- A BCD counter counts in binary-coded decimal from 0000 to 1001 and back to 0000.
- Because of the return to 0 after a count of 9, a BCD counter does not have a regular pattern, unlike a straight binary count.
- To derive the circuit of a BCD synchronous counter, it is necessary to go through a sequential circuit design procedure.
- The state table of a BCD counter is listed in Table 6.5 .
- The input conditions for the *T* flip-flops are obtained from the present- and next-state conditions.
- Also shown in the table is an output *y*, which is equal to 1 when the present state is 1001.

BCD Counter

- In this way, *y* can enable the count of the next-higher significant decade while the same pulse switches the present decade from 1001 to 0000.
- The simplified functions are:

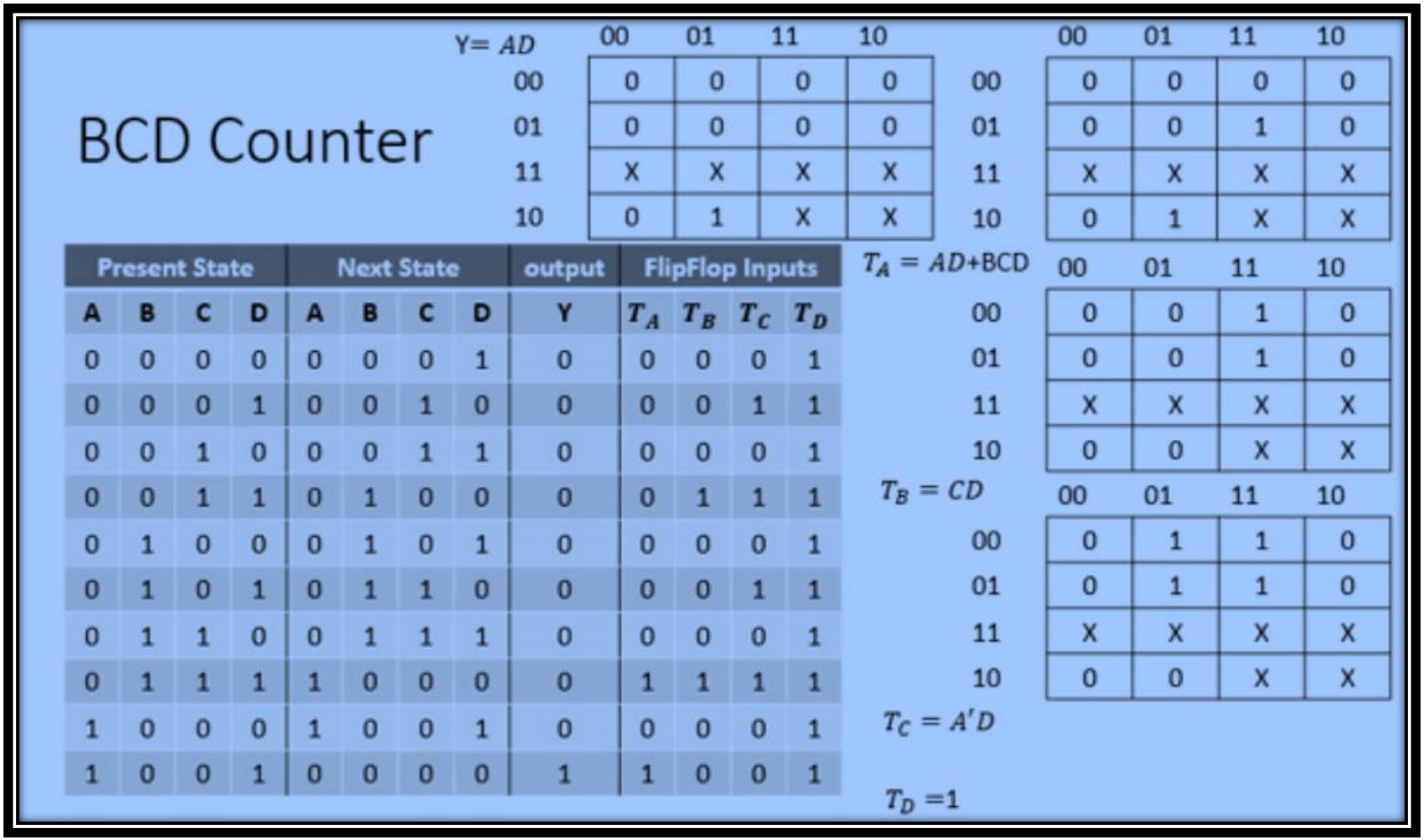
$$T_{Q1} = 1$$
$$T_{Q2} = Q'_8 Q_1$$
$$T_{Q4} = Q_2 Q_1$$
$$T_{Q8} = Q_8 Q_1 + Q_4 Q_2 Q_1$$
$$y = Q_8 Q_1$$

BCD Counter

Table 6.5
State Table for BCD Counter

Present State				Next State				Output	Flip-Flop Inputs			
Q_8	Q_4	Q_2	Q_1	Q_8	Q_4	Q_2	Q_1	y	TQ_8	TQ_4	TQ_2	TQ_1
0	0	0	0	0	0	0	1	0	0	0	0	1
0	0	0	1	0	0	1	0	0	0	0	1	1
0	0	1	0	0	0	1	1	0	0	0	0	1
0	0	1	1	0	1	0	0	0	0	1	1	1
0	1	0	0	0	1	0	1	0	0	0	0	1
0	1	0	1	0	1	1	0	0	0	0	1	1
0	1	1	0	0	1	1	1	0	0	0	0	1
0	1	1	1	1	0	0	0	0	1	1	1	1
1	0	0	0	1	0	0	1	0	0	0	0	1
1	0	0	1	0	0	0	0	1	1	0	0	1

BCD Counter



$Y = AD$

	00	01	11	10
00	0	0	0	0
01	0	0	0	0
11	X	X	X	X
10	0	1	X	X

	00	01	11	10
00	0	0	0	0
01	0	0	1	0
11	X	X	X	X
10	0	1	X	X

Present State				Next State				output	FlipFlop Inputs			
A	B	C	D	A	B	C	D	Y	T_A	T_B	T_C	T_D
0	0	0	0	0	0	0	1	0	0	0	0	1
0	0	0	1	0	0	1	0	0	0	0	1	1
0	0	1	0	0	0	1	1	0	0	0	0	1
0	0	1	1	0	1	0	0	0	0	1	1	1
0	1	0	0	0	1	0	1	0	0	0	0	1
0	1	0	1	0	1	1	0	0	0	0	1	1
0	1	1	0	0	1	1	1	0	0	0	0	1
0	1	1	1	1	0	0	0	0	1	1	1	1
1	0	0	0	1	0	0	1	0	0	0	0	1
1	0	0	1	0	0	0	0	1	1	0	0	1

$T_A = AD$+BCD

	00	01	11	10
00	0	0	1	0
01	0	0	1	0
11	X	X	X	X
10	0	0	X	X

$T_B = CD$

	00	01	11	10
00	0	1	1	0
01	0	1	1	0
11	X	X	X	X
10	0	0	X	X

$T_C = A'D$

$T_D = 1$

BCD Counter

BCD Counter

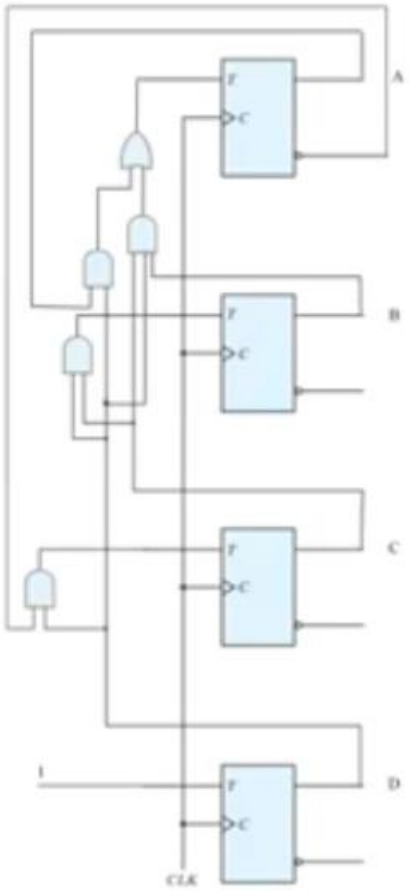
$T_A = AD$+BCD

$T_B = CD$

$T_C = A'D$

$T_D = 1$

Y= AD



Binary Counter with Parallel Load

- Counters employed in digital systems quite often require a parallel-load capability for transferring an initial binary number into the counter prior to the count operation.
- Figure 6.14 shows the top-level block diagram symbol and the logic diagram of a four-bit register that has a parallel load capability and can operate as a counter.
- When equal to 1, the input load control disables the count operation and causes a transfer of data from the four data inputs into the four flip-flops.
- If both control inputs are 0, clock pulses do not change the state of the register.

Binary Counter with Parallel Load

- The operation of the counter is summarized in Table 6.6 .
- The four control inputs— *Clear*, *CLK*, *Load*, and *Count* — determine the next state.
- The *Clear* input is asynchronous and, when equal to 0, causes the counter to be cleared regardless of the presence of clock pulses or other inputs.
- This relationship is indicated in the table by the X entries, which symbolize don't-care conditions for the other inputs.
- The *Clear* input must be in the 1 state for all other operations.
- With the *Load* and *Count* inputs both at 0, the outputs do not change, even when clock pulses are applied.

Binary Counter with Parallel Load

- A *Load* input of 1 causes a transfer from inputs *I*0 - *I*3 into the register during a positive edge of *CLK* .
- The input data are loaded into the register regardless of the value of the *Count* input, because the *Count* input is inhibited when the *Load* input is enabled.
- The *Load* input must be 0 for the *Count* input to control the operation of the counter.

Table 6.6
Function Table for the Counter of Fig. 6.14

Clear	CLK	Load	Count	Function
0	X	X	X	Clear to 0
1	↑	1	X	Load inputs
1	↑	0	1	Count next binary state
1	↑	0	0	No change

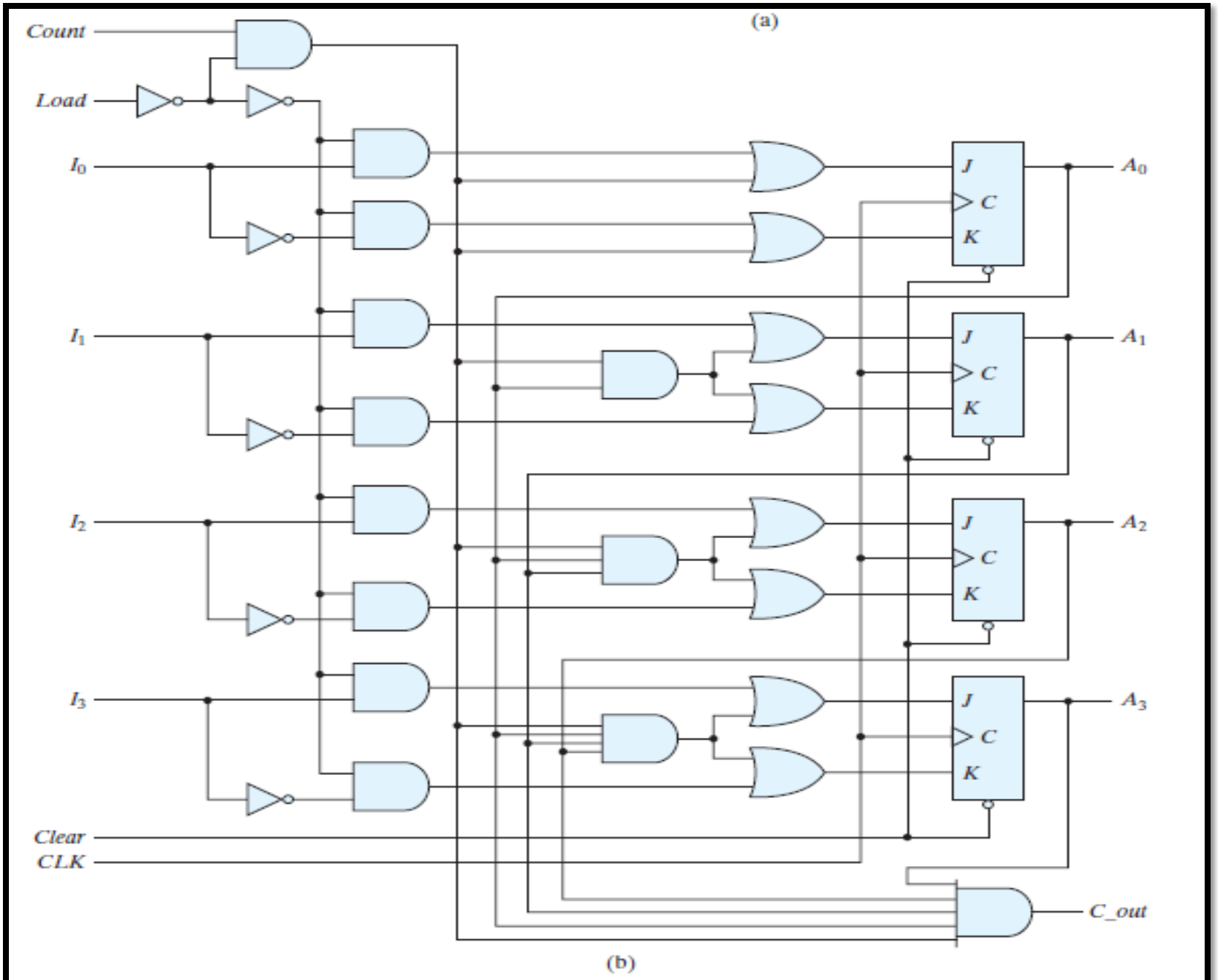


FIGURE 6.14
Four-bit binary counter with parallel load

OTHER COUNTERS

- Counters can be designed to generate any desired sequence of states.
- A divide-by- *N* counter (also known as a modulo- *N* counter) is a counter that goes through a repeated sequence of *N* states.
- The sequence may follow the binary count or may be any other arbitrary sequence.
- Counters are used to generate timing signals to control the sequence of operations in a digital system.
- Counters can also be constructed by means of shift registers.
- In this section, we present a few examples of non-binary counters.

Counter with Unused States

- A circuit with *n* flip-flops has 2^n binary states.
- There are occasions when a sequential circuit uses fewer than this maximum possible number of states.
- States that are not used in specifying the sequential circuit are not listed in the state table.
- In simplifying the input equations, the unused states may be treated as don't-care conditions.
- It is important to realize that once the circuit is designed and constructed, outside interference during its operation may cause the circuit to enter one of the unused states.
- In that case, it is necessary to ensure that the circuit eventually goes into one of the valid states so that it can resume normal operation.

Counter with Unused States

- As an illustration, consider the counter specified in Table 6.7.
- The count has a repeated sequence of six states, with flip-flops *B* and *C* repeating the binary count 00, 01, 10, and flip-flop *A* alternating between 0 and 1 every three counts.
- The simplified equations are
- $J_A = B$ $K_A = B$
- $J_B = C$ $K_B = 1$
- $J_C = B$ $K_C = 1$
- The logic diagram of the counter is shown in Fig. 6.16 (a). Since there are two unused states, we analyze the circuit to determine their effect.

Counter with Unused States

- If the circuit happens to be in state 011 because of an error signal, the circuit goes to state 100 after the application of a clock pulse.
- This action may be determined from an inspection of the logic diagram by noting that when *B* = 1, the next clock edge complements *A* and clears *C* to 0, and when *C* = 1, the next clock edge complements *B.*
- In a similar manner, we can evaluate the next state from present state 111 to be 000.

Counter with Unused States

Table 6.7
State Table for Counter

Present State			Next State			Flip-Flop Inputs					
A	B	C	A	B	C	J_A	K_A	J_B	K_B	J_C	K_C
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	0	0	X	1	X	X	1
0	1	0	1	0	0	1	X	X	1	0	X
1	0	0	1	0	1	X	0	0	X	1	X
1	0	1	1	1	0	X	0	1	X	X	1
1	1	0	0	0	0	X	1	X	1	0	X

Counter with Unused States

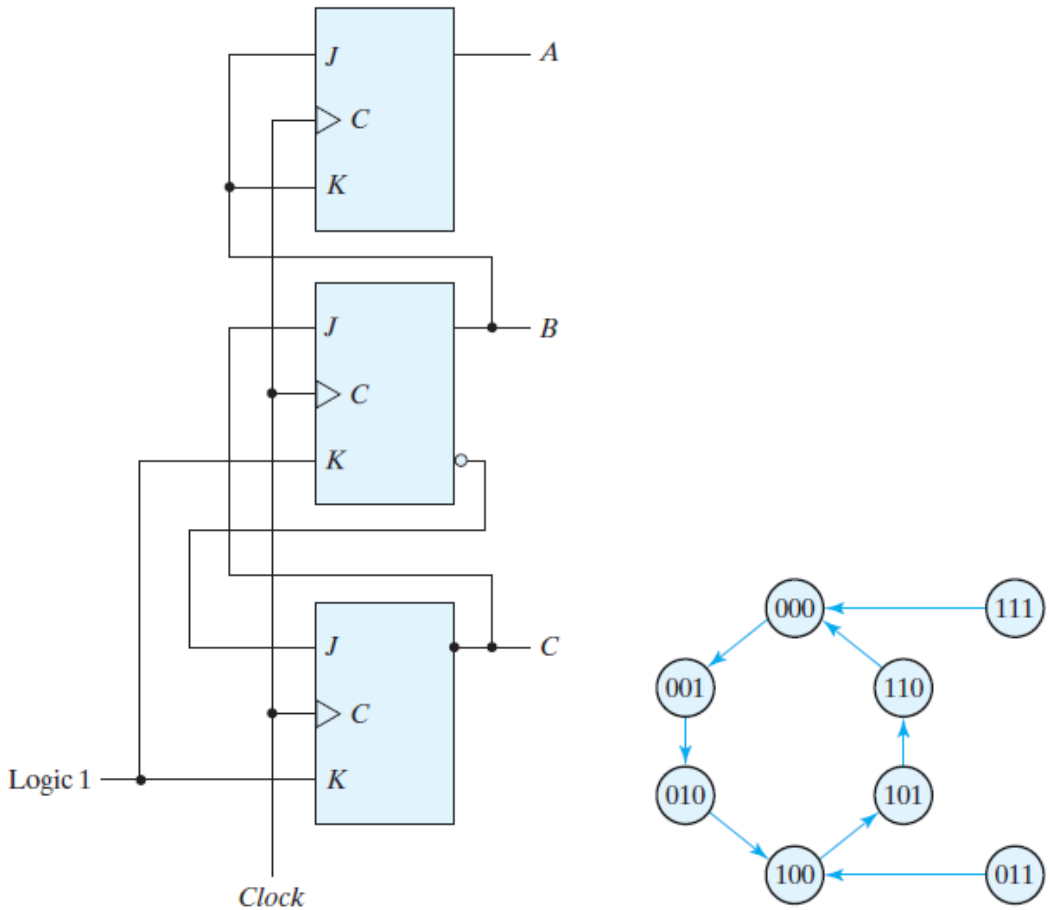


FIGURE 6.16
Counter with unused states

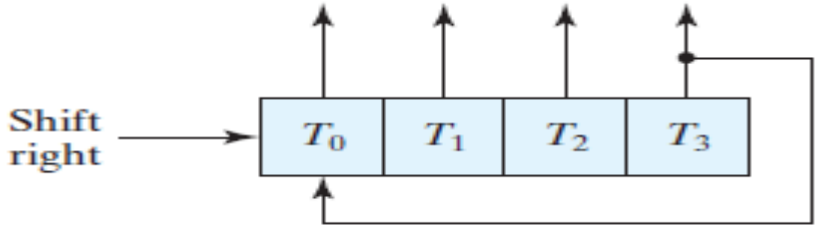
Ring Counter

- Timing signals that control the sequence of operations in a digital system can be generated by a shift register or by a counter with a decoder.
- A *ring counter* is a circular shift register with only one flip-flop being set at any particular time; all others are cleared.
- The single bit is shifted from one flip-flop to the next to produce the sequence of timing signals.
- Figure 6.17 (a) shows a four-bit shift register connected as a ring counter.
- The initial value of the register is 1000 and requires Preset/Clear flip-flops.

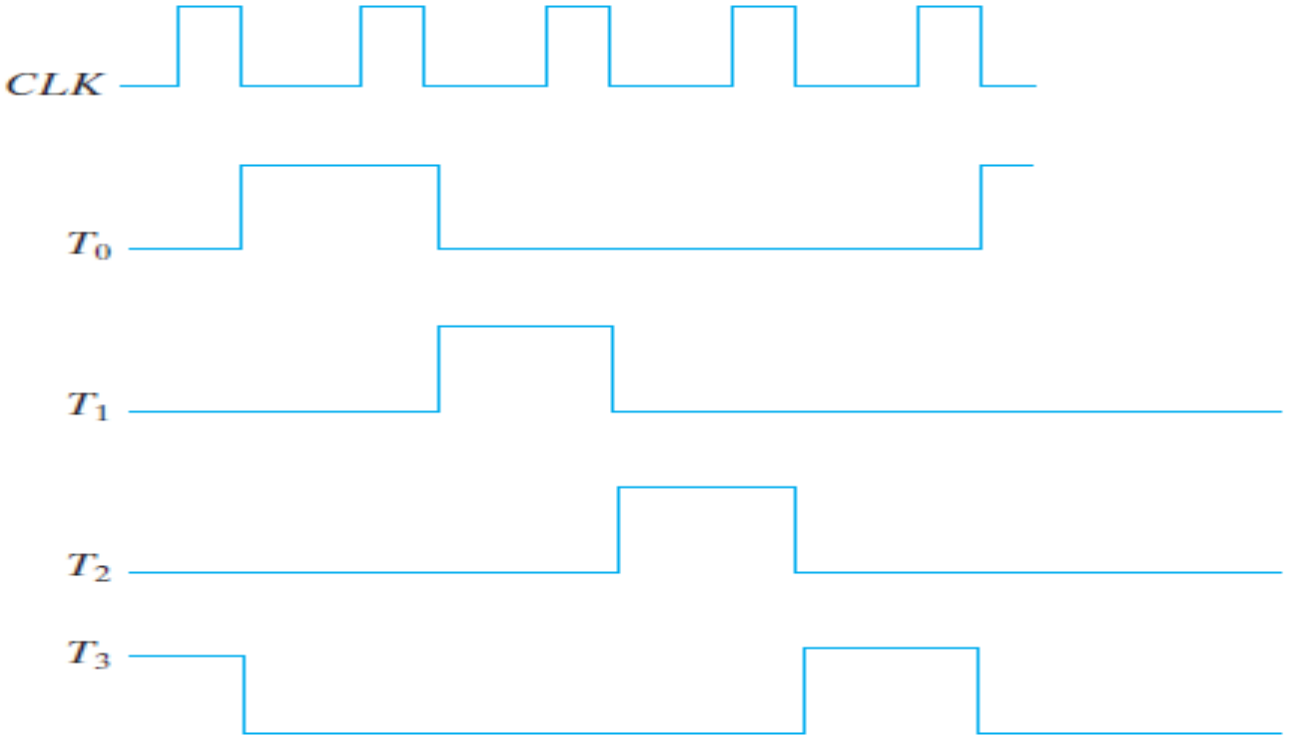
Ring Counter

- The single bit is shifted right with every clock pulse and circulates back from *T*3 to *T*0.
- Each flip-flop is in the 1 state once every four clock cycles and produces one of the four timing signals shown in Fig. 6.17 (b).
- Each output becomes a 1 after the negative-edge transition of a clock pulse and remains 1 during the next clock cycle.

Ring Counter



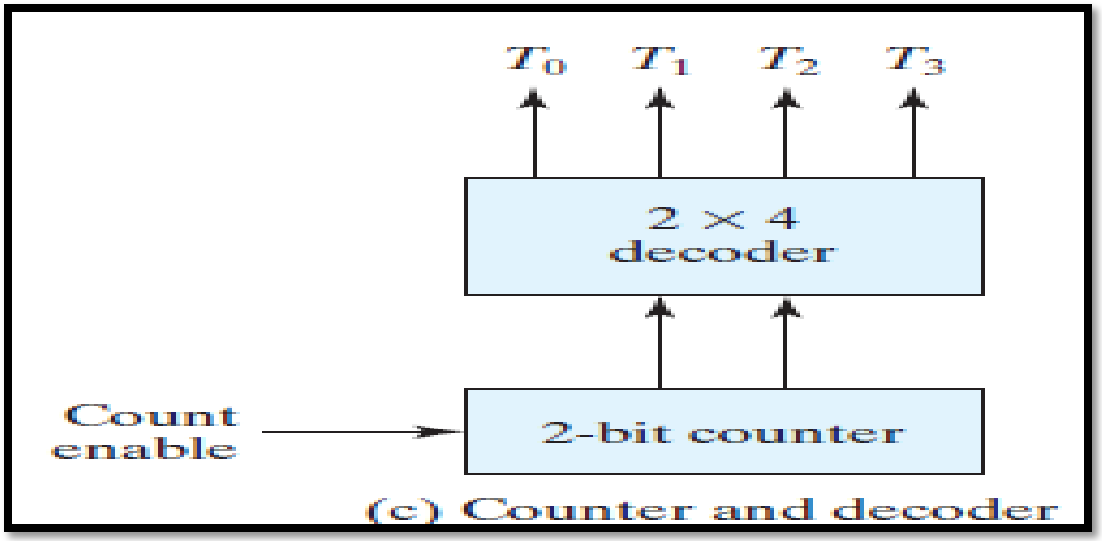
(a) Ring-counter (initial value = 1000)



(b) Sequence of four timing signals

Ring Counter

- For an alternative design, the timing signals can be generated by a two-bit counter that goes through four distinct states.
- The decoder shown in Fig. 6.17 (c) decodes the four states of the counter and generates the required sequence of timing signals. To generate 2^n timing signals, we need either a shift register with 2^n flip-flops or an n -bit binary counter together with an n -to-2^n -line decoder.



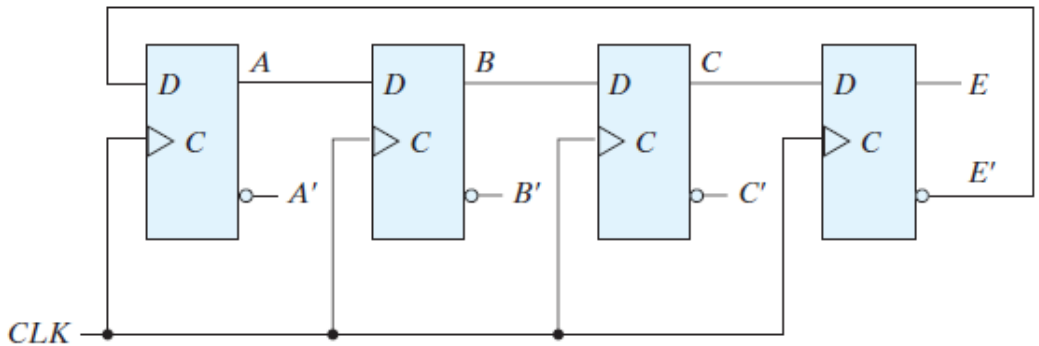
Johnson Counter

- A *k* -bit ring counter circulates a single bit among the flip-flops to provide *k* distinguishable states.
- The number of states can be doubled if the shift register is connected as a *switch-tail* ring counter.
- A switch-tail ring counter is a circular shift register with the complemented output of the last flip-flop connected to the input of the first flip-flop.
- Figure 6.18 (a) shows such a shift register.
- The circular connection is made from the complemented output of the rightmost flip-flop to the input of the leftmost flip-flop.

Johnson Counter

- The register shifts its contents once to the right with every clock pulse, and at the same time, the complemented value of the *E* flip-flop is transferred into the *A* flip-flop.
- Starting from a cleared state, the switch-tail ring counter goes through a sequence of eight states, as listed in Fig. 6.18 (b).
- In general, a *k* -bit switch-tail ring counter will go through a sequence of 2*k* states.
- A Johnson counter is a *k* -bit switch-tail ring counter with 2*k* decoding gates to provide outputs for 2 *k* timing signals.
- The decoding gates are not shown in Fig. 6.18 , but are specified in the last column of the table.

Johnson Counter



(a) Four-stage switch-tail ring counter

Sequence number	Flip-flop outputs A	B	C	E	AND gate required for output
1	0	0	0	0	$A'E'$
2	1	0	0	0	AB'
3	1	1	0	0	BC'
4	1	1	1	0	CE'
5	1	1	1	1	AE
6	0	1	1	1	$A'B$
7	0	0	1	1	$B'C$
8	0	0	0	1	$C'E$

(b) Count sequence and required decoding

FIGURE 6.18
Construction of a Johnson counter