CECS 341 - Lab 4

"ALU Structural Model"

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I certify that this submission is my original work

Lab Report: Lab Assignment X - "Lab title"

1. **Goal:** To learn how to use and setup an ALU in Vivado
2. **Steps:** Followed the procedures for creating a design and test bench module and filled the missing alu op codes.
3. **Results:** The results were 72 cases of various output code
4. **Conclusion:** I learned more about verilog and the challenges were figuring out how some syntax functioned.

Appendix:

Design module:

```
`timescale 1ns/100ps

module alu#(parameter width = 8)

 (

   input [width-1:0] a,b,

   input [2:0] aluop,

   output reg [width-1:0] y,

   output reg c,n,z,p

 );


   always @(a,b,aluop)
```

```verilog
    begin
      {y,c,n,z,p} = 0;
      case(aluop)
        0: {c,y} = a + b;
        1: {c,y} = a + 1;
              2: y = a & b;
        3: y = a | b;
              4: y = a ^ b;
        5: y = !a;
        6: {c,y} = a<<1;
        7: y =0;
        default: y = 32'bZ;
      endcase
      n = y[width-1];
      z = !y;
      p = ^y;
    end
  endmodule
```

Output:

Test case   0

aluop = 000   a = 1100   b = 0011   y = 1111

c = 0, n = 1, z= 0, p = 0

Test case   1

aluop = 000   a = 0101   b = 1001   y = 1110

c = 0, n = 1, z= 0, p = 1

Test case   2

aluop = 000   a = 1101   b = 0000   y = 1101

c = 0, n = 1, z= 0, p = 1

Test case   3

aluop = 000   a = 1011   b = 1010   y = 0101

c = 1, n = 0, z= 0, p = 0

Test case   4

aluop = 000   a = 1000   b = 1101   y = 0101

c = 1, n = 0, z= 0, p = 0

Test case   5

aluop = 000   a = 0001   b = 0000   y = 0001

c = 0, n = 0, z= 0, p = 1

Test case   6

aluop = 000   a = 1100   b = 1011   y = 0111

c = 1, n = 0, z= 0, p = 1

Test case   7

aluop = 000   a = 0100   b = 0000   y = 0100

c = 0, n = 0, z= 0, p = 1

Test case   8

aluop = 000   a = 1001   b = 1001   y = 0010

c = 1, n = 0, z= 0, p = 1

Test case   9

aluop = 001   a = 1101   b = 0000   y = 1110

c = 0, n = 1, z= 0, p = 1