Lesson Timers

What is a timer?

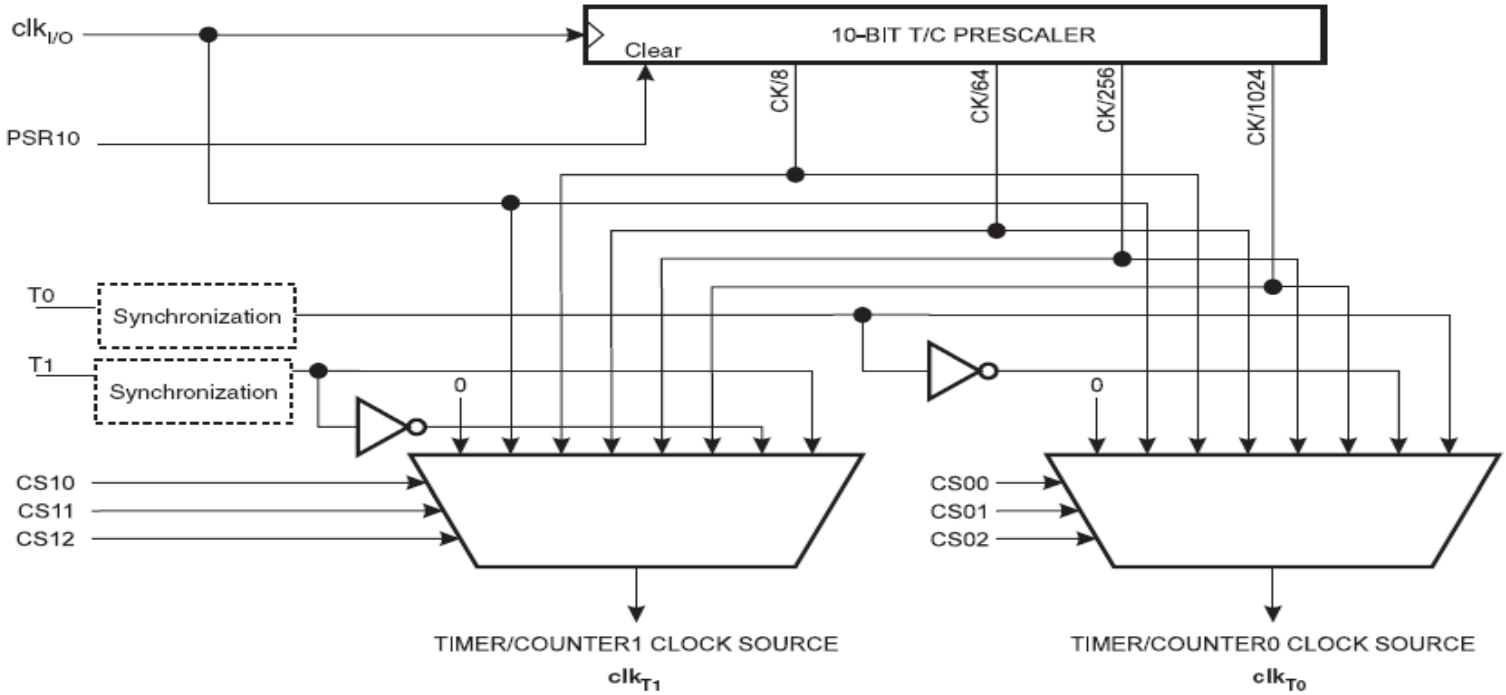
- Probably the most used peripherals in a microcontroller
- A simple binary up or down counter
- Counts on events
  - Clock ticks
  - External inputs
- Generates events
  - External outputs
  - Interrupts
- No software/CPU involved

Timers on ATMEGA1280

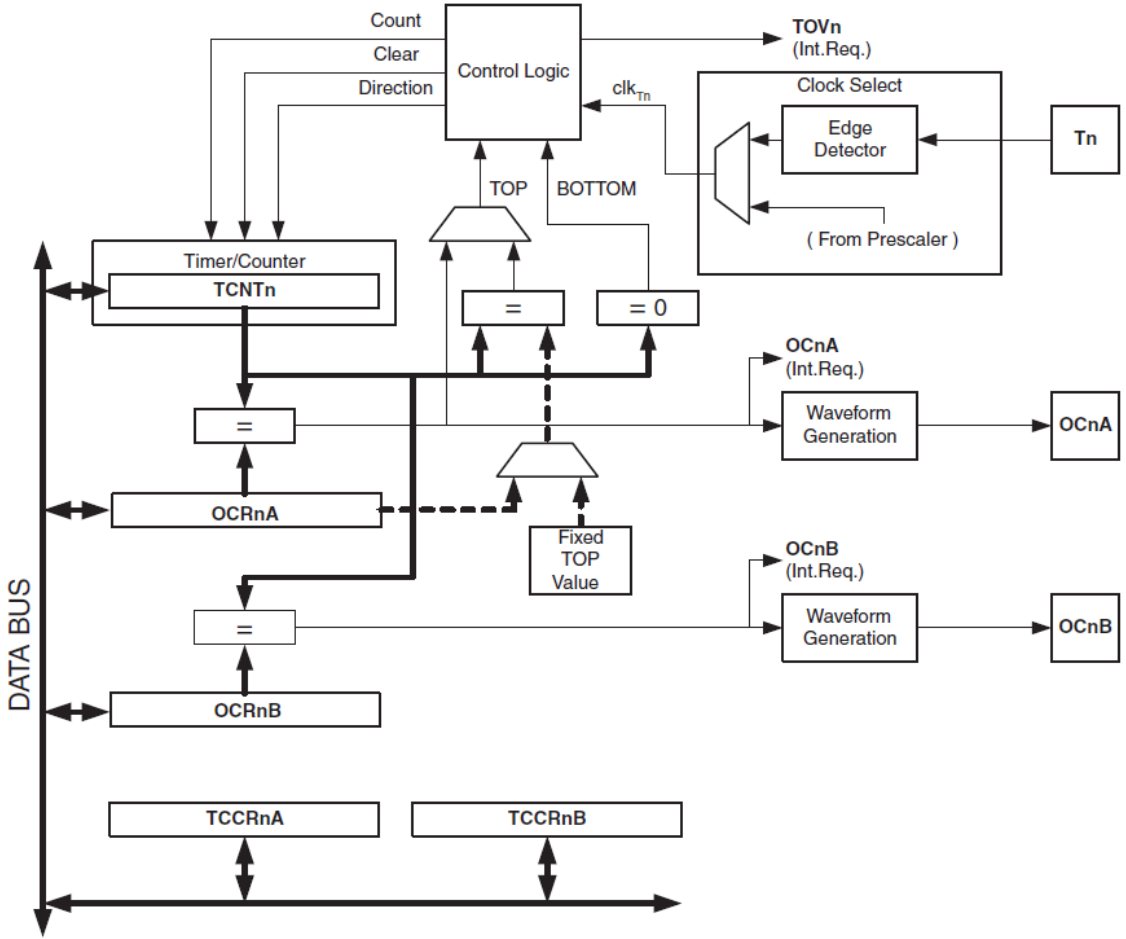
- Number and type of timers depends on MCU type
- Two 8-bit Timer/Counters with Separate Prescaler and Compare Mode
- Four 16-bit Timer/Counter with Separate Prescaler, Compare- and Capture Mode
- Real Time Counter with Separate Oscillator
- Four 8-bit PWM Channels
- Twelve PWM Channels with Programmable Resolution from 2 to 16 Bits
- Output Compare Modulator

Pre-scalers

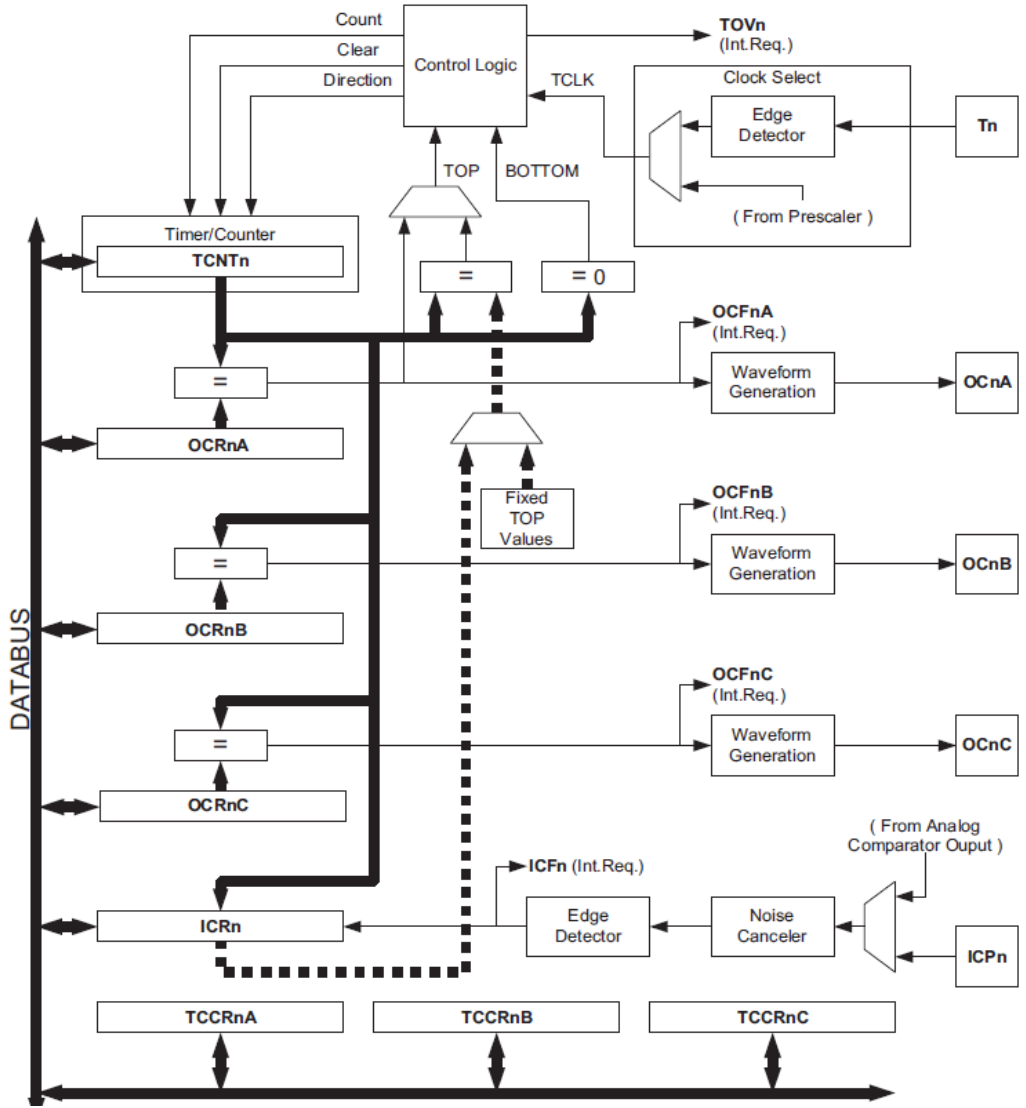
Divide the system clock by 8/64/256/1024



8-bit Timer/Counter0 with PWM

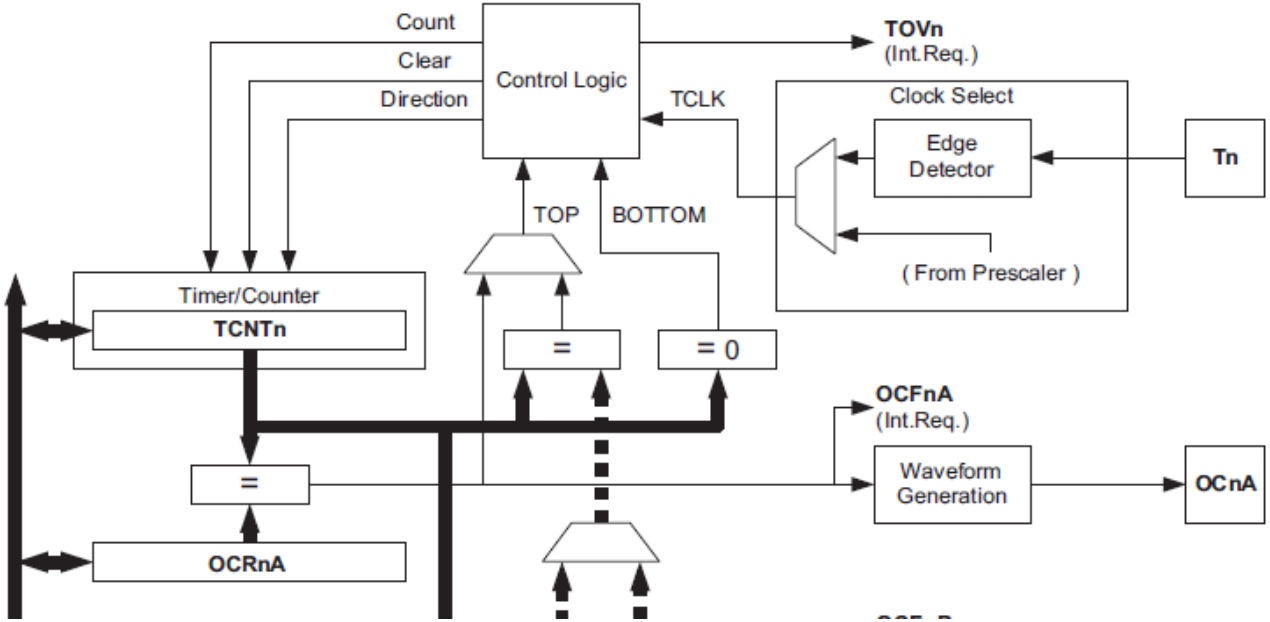


16-bit Timer/ Counter1,3,4,5



The software setup

- Let's setup Timer4 16-bit timer to control the output level of one of the port pins.
- First we take a look at the timers control register



Timer control register

Bit	7	6	5	4	3	2	1	0	
(0xA0)	COM4A1	COM4A0	COM4B1	COM4B0	COM4C1	COM4C0	WGM41	WGM40	TCCR4A
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	
Bit	7	6	5	4	3	2	1	0	
(0xA1)	ICNC4	ICES4	–	WGM43	WGM42	CS42	CS41	CS40	TCCR4B
Read/Write	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

17.9 Modes of Operation

The mode of operation, that is, the behavior of the Timer/Counter and the Output Compare pins, is defined by the combination of the *Waveform Generation mode* (WGMn3:0) and *Compare Output mode* (COMnx1:0) bits. The Compare Output mode bits do not affect the counting sequence, while the Waveform Generation mode bits do. The COMnx1:0 bits control whether the PWM output generated should be inverted or not (inverted or non-inverted PWM). For non-PWM modes the COMnx1:0 bits control whether the output should be set, cleared or toggle at a compare match. See “Compare Match Output Unit” on page 147.

This is default so we do not need setup these bits

Table 17-2. Waveform Generation Mode Bit Description[1]

Mode	WGMn3	WGMn2 (CTCn)	WGMn1 (PWMn1)	WGMn0 (PWMn0)	Timer/Counter Mode of Operation	TOP	Update of OCRnX at	TOVn Flag Set on
0	0	0	0	0	Normal	0xFFFF	Immediate	MAX
1	0	0	0	1	PWM, Phase Correct, 8-bit	0x00FF	TOP	BOTTOM
2	0	0	1	0	PWM, Phase Correct, 9-bit	0x01FF	TOP	BOTTOM
3	0	0	1	1	PWM, Phase Correct, 10-bit	0x03FF	TOP	BOTTOM
4	0	1	0	0	CTC	OCRnA	Immediate	MAX

Timer control register A

TCCR4A – Timer/Counter 4 Control Register A

Bit	7	6	5	4	3	2	1	0	
(0xA0)	COM4A1	COM4A0	COM4B1	COM4B0	COM4C1	COM4C0	WGM41	WGM40	TCCR4A
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

```
// Setup OC4A to toggle on compare match
TCCR4A |= _BV(COM4A0);
```

Table 17-3. Compare Output Mode, non-PWM

COMnA1 COMnB1 COMnC1	COMnA0 COMnB0 COMnC0	Description
0	0	Normal port operation, OCnA/OCnB/OCnC disconnected
0	1	Toggle OCnA/OCnB/OCnC on compare match
1	0	Clear OCnA/OCnB/OCnC on compare match (set output to low level)
1	1	Set OCnA/OCnB/OCnC on compare match (set output to high level)

Timer control register B

TCCR4B – Timer/Counter 4 Control Register B

Bit	7	6	5	4	3	2	1	0	
(0xA1)	ICNC4	ICES4	–	WGM43	WGM42	CS42	CS41	CS40	TCCR4B
Read/Write	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

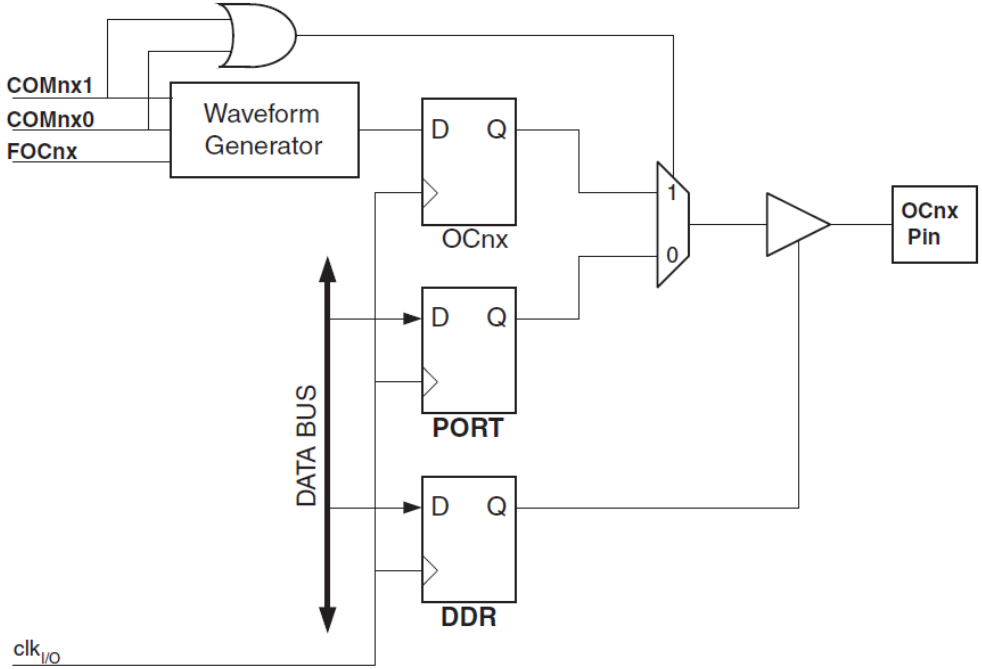
Table 17-6. Clock Select Bit Description

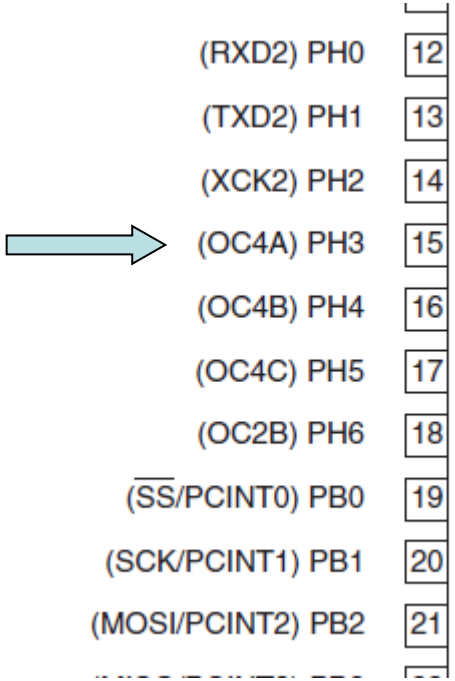
CSn2	CSn1	CSn0	Description
0	0	0	No clock source. (Timer/Counter stopped)
0	0	1	$clk_{I/O}$/1 (No prescaling
0	1	0	$clk_{I/O}$/8 (From prescaler)
0	1	1	$clk_{I/O}$/64 (From prescaler)
			edge
1	1	1	External clock source on Tn pin. Clock on rising edge

```
// Setup Timer 4 prescaler to clk/8
TCCR4B |= _BV(CS41);
```

Finally we need to setup the port pin to output

Figure 17-5. Compare Match Output Unit, Schematic






```
// Setup PH3 to output
DDRH |= _BV(DDH3);
```

The complete software for setting up a free running timer

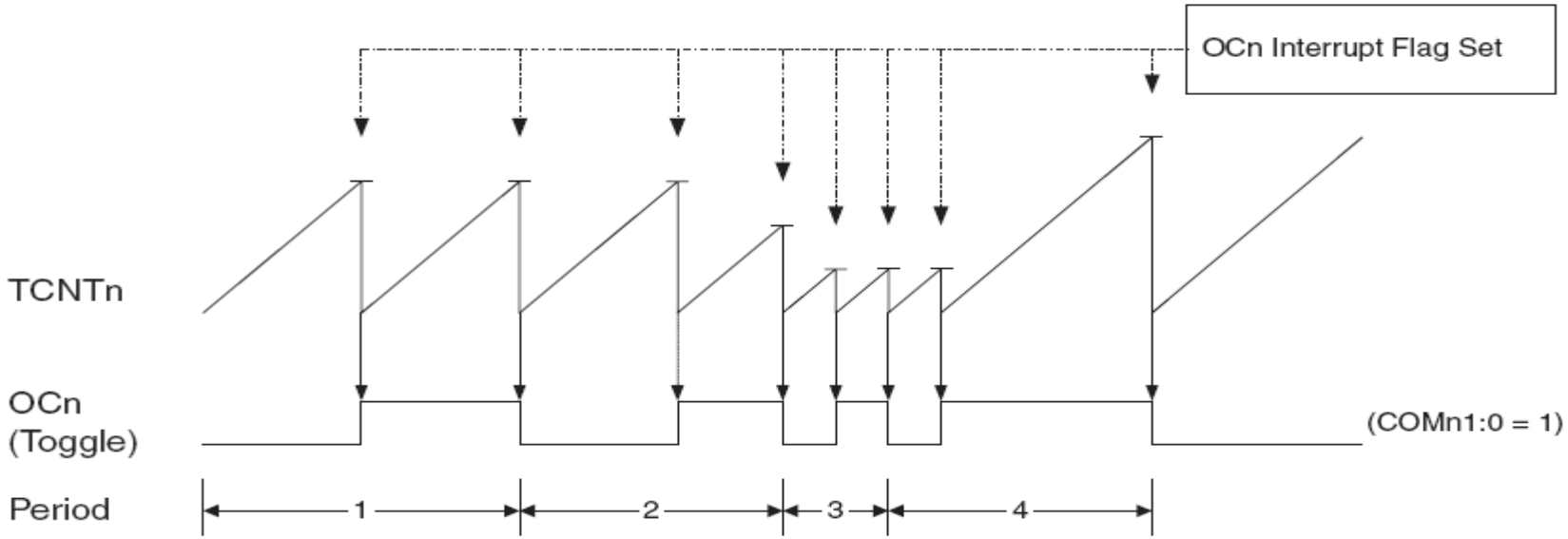
```
/**
 * Setup timer 4 to free running with a prescaler of
 * 8 on the system clock.
 * Toggles PH3 each time the timer reach the TOP
 * value (65535).
 */
void init_timer4( void ) {
  // Setup OC4A to toggle on compare match
  TCCR4A |= _BV(COM4A0);
  // Setup Timer 0 prescaler to clk/8
  TCCR4B |= _BV(CS41);
  // Setup PH3 to output
  DDRH |= _BV(DDH3);
}
```

Exercise

- Setup the Timer 4 to toggle OC4A/PH3 when it reach the value you set in OCR4A instead of TOP.

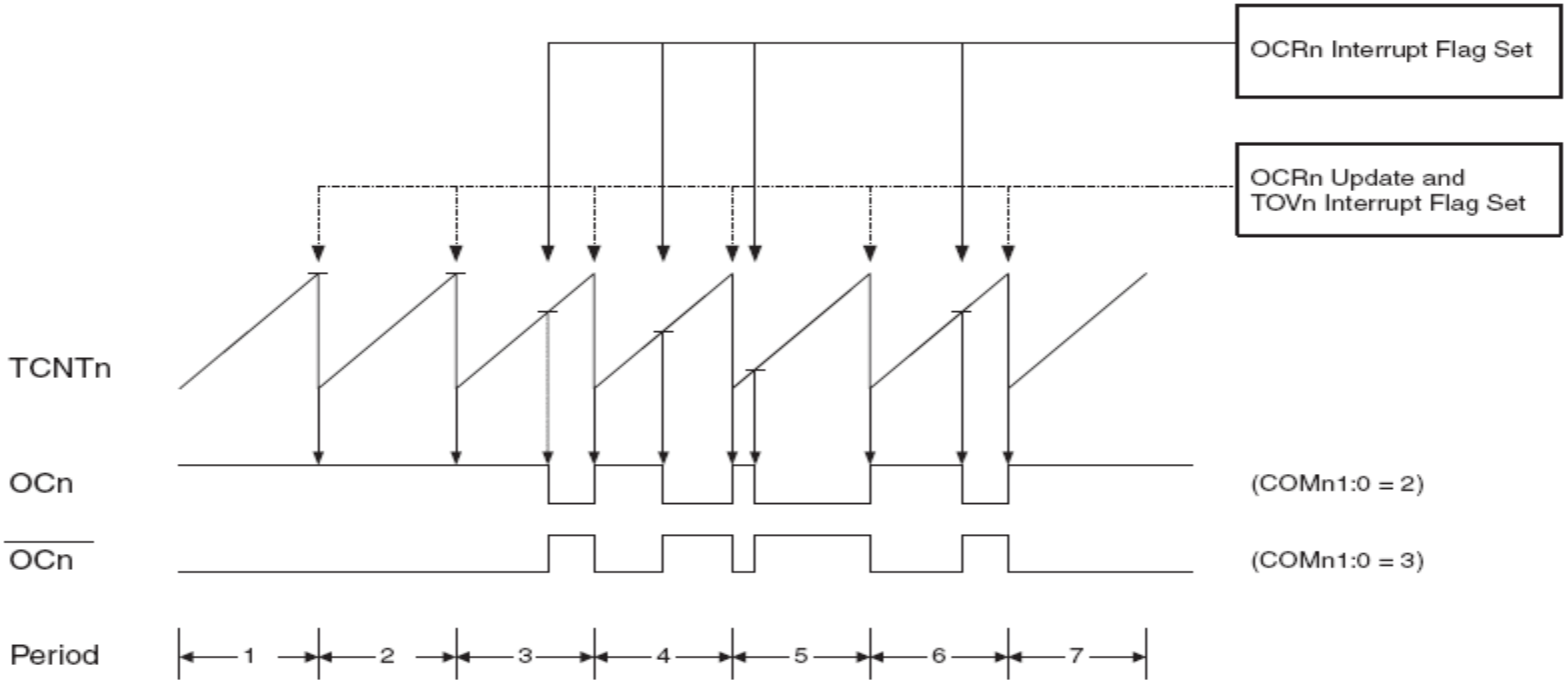
Clear Timer on Compare match

Figure 31. CTC Mode, Timing Diagram



Pulse Width Modulation (PWM)

Figure 32. Fast PWM Mode, Timing Diagram



The PWM frequency for the output can be calculated by the following equation:

$$f_{OCnPWM} = \frac{f_{clk\_I/O}}{N \cdot 256}$$

The N variable represents the prescale factor (1, 8, 64, 256, or 1024).

Exercise

- Setup a timer to interrupt for every 1 sec
- Implement an ISR that handle the interrupt and toggle PH1 every time the interrupt occurs