

[illegible]

Pin Mapping

The diagram illustrates the pin mapping for two components: **key matrix** and **analog**.

key matrix (File: key_matrix.kicad_sch) has the following pins and connections:

- Inputs:** C13, A2, A6, C14.
- Internal Components:** ROW0, ROW1, ROW2, ROW3.
- Outputs:** COL0, COL1, COL2, COL3, COL4, COL5, COL6, COL7, COL8, COL9, COL10, COL11, COL12.

analog (File: analog.kicad_sch) has the following pins and connections:

- Inputs:** B1, B0, B11, B10, B2.
- Internal Components:** APLEX0_EN, APLEX1_EN, APLEX_SELO, APLEX_SEL1, APLEX_SEL2, DISCHARGE, ADC.
- Outputs:** A4, A3.

Connections:

- COL0 connects to APLEX0_3.
- COL1 connects to APLEX0_0.
- COL2 connects to APLEX0_1.
- COL3 connects to APLEX0_2.
- COL4 connects to APLEX0_4.
- COL5 connects to APLEX0_6.
- COL6 connects to APLEX1_3.
- COL7 connects to APLEX1_0.
- COL8 connects to APLEX1_1.
- COL9 connects to APLEX1_2.
- COL10 connects to APLEX1_4.
- COL11 connects to APLEX1_6.
- COL12 connects to APLEX1_5.

Unified daughterboard Legacy C3 connector

SM04B-SR55-TB(LF)(SN)

Legacy unfilled daughterboard C
JST-SH

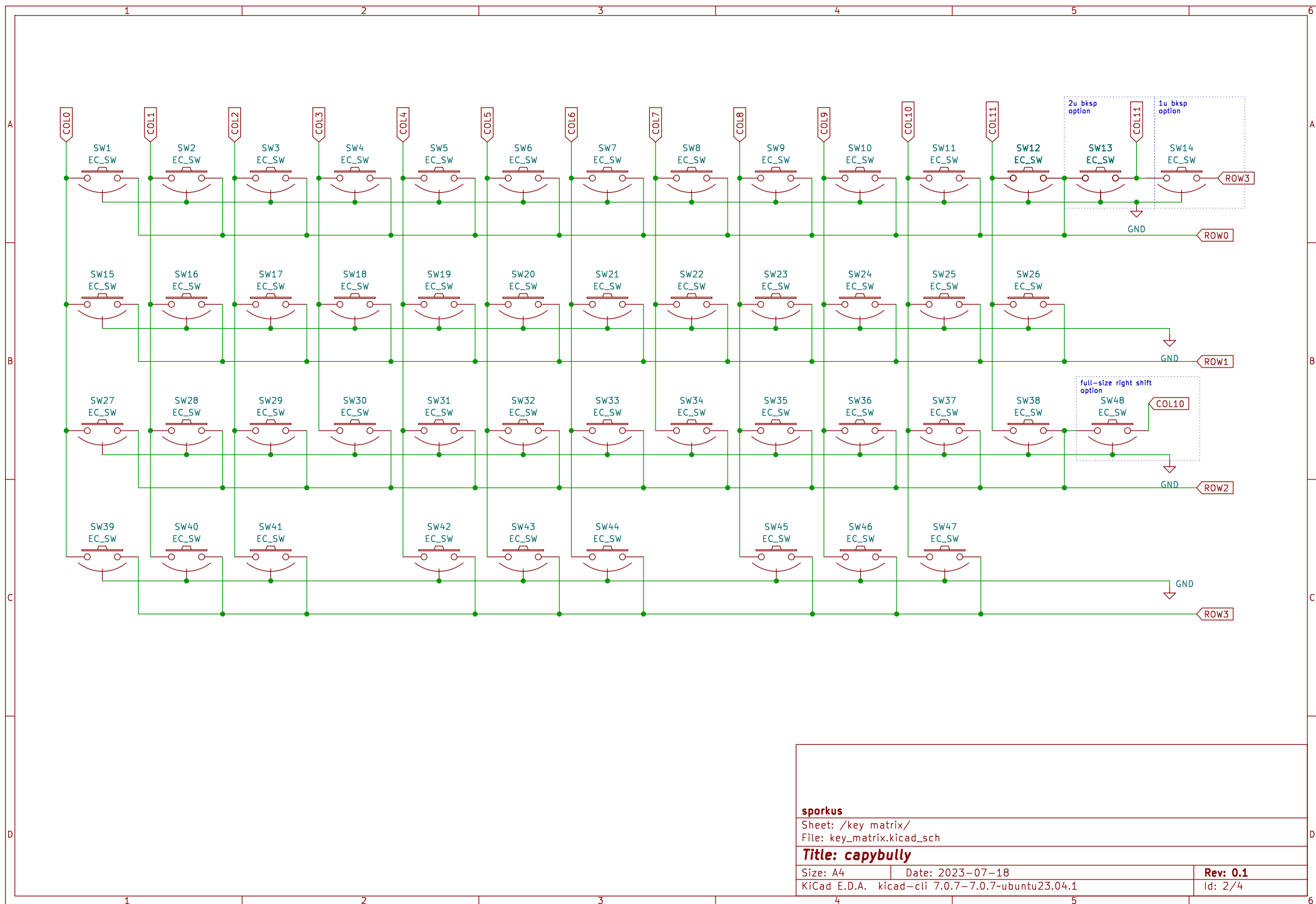
usb signal impedance ref:
4 layer PCB, stack up: JLC04161H-7628
coplanar differential pair
signal spacing: 0.2mm
signal to ground spacing: 0.2mm
signal trace width: 0.2644mm

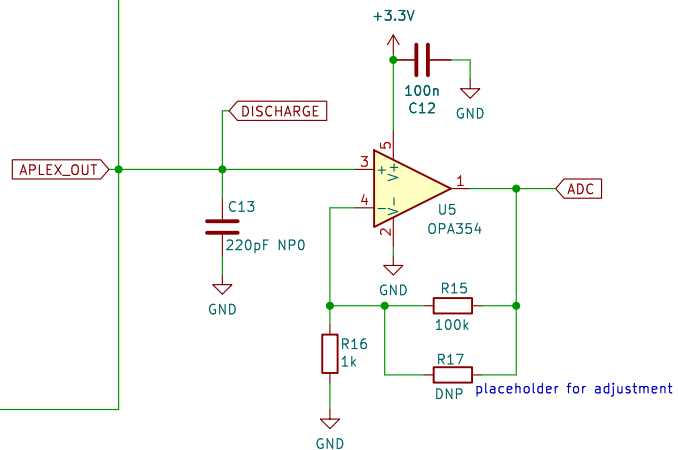
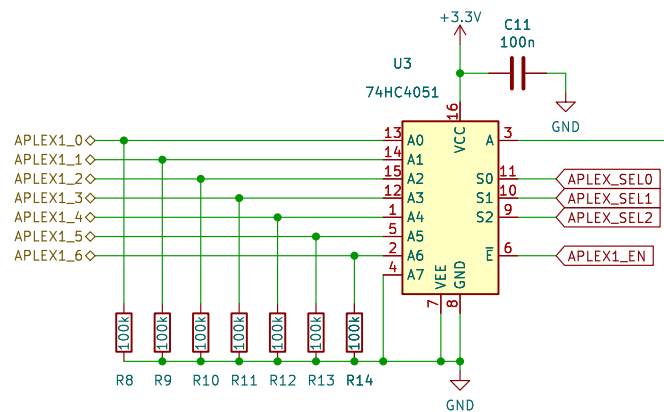
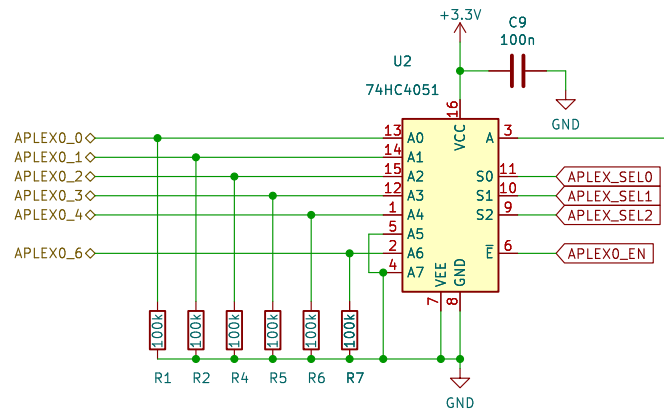
3V3 LDO

mounting_holes.kicad_sch

sporkus	
Sheet: /	
File: capybully.kicad_sch	
Title: capybully	
Size: A4	Date: 2023-07-18
KiCad E.D.A. kicad-cli 7.0.7-7.0.7-ubuntu23.04.1	Rev: 0.1
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Alternatives:
SC-70-6
OPA358AIDCKR
LMV861

SOT-23-5 seems to have better availability
OPA354 to 358 seems ok

sporkus

Sheet: /analog/
File: analog.kicad_sch

Title: capybully

Size: A4 Date: 2023-07-18

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Rev: 0.1

Id: 3/4

