

[illegible]

## Pin Mapping

The diagram illustrates the pin mapping for two components: **key matrix** and **analog**.

**key matrix** (File: key\_matrix.kicad\_sch) has the following pins and connections:

- Inputs:** C13, A2, A6, C14.
- Internal Labels:** ROW0, ROW1, ROW2, ROW3.
- Outputs:** COL0, COL1, COL2, COL3, COL4, COL5, COL6, COL7, COL8, COL9, COL10, COL11, COL12.

**analog** (File: analog.kicad\_sch) has the following pins and connections:

- Inputs:** B1, B0, B11, B10, B2.
- Internal Labels:** APLEX0\_EN, APLEX1\_EN, APLEX\_SELO, APLEX\_SEL1, APLEX\_SEL2.
- Outputs:** DISCHARGE, ADC.

**Connections:**

- COL0 connects to APLEX0\_3.
- COL1 connects to APLEX0\_0.
- COL2 connects to APLEX0\_1.
- COL3 connects to APLEX0\_2.
- COL4 connects to APLEX0\_4.
- COL5 connects to APLEX0\_6.
- COL6 connects to APLEX1\_3.
- COL7 connects to APLEX1\_0.
- COL8 connects to APLEX1\_1.
- COL9 connects to APLEX1\_2.
- COL10 connects to APLEX1\_4.
- COL11 connects to APLEX1\_6.
- COL12 connects to APLEX1\_5.

# Unified daughterboard Legacy C3 connector

SM04B-SRSS-TB(LF)(SN)

1  
2  
3  
4

+5V

D\_N  
D\_P

J1

GND

Legacy unified daughterboard C  
JST-SH

usb signal impedance ref:  
4 layer PCB, stack up: JLC04161H-7628  
coplanar differential pair  
signal spacing: 0.2mm  
signal to ground spacing: 0.2mm  
signal trace width: 0.2644mm

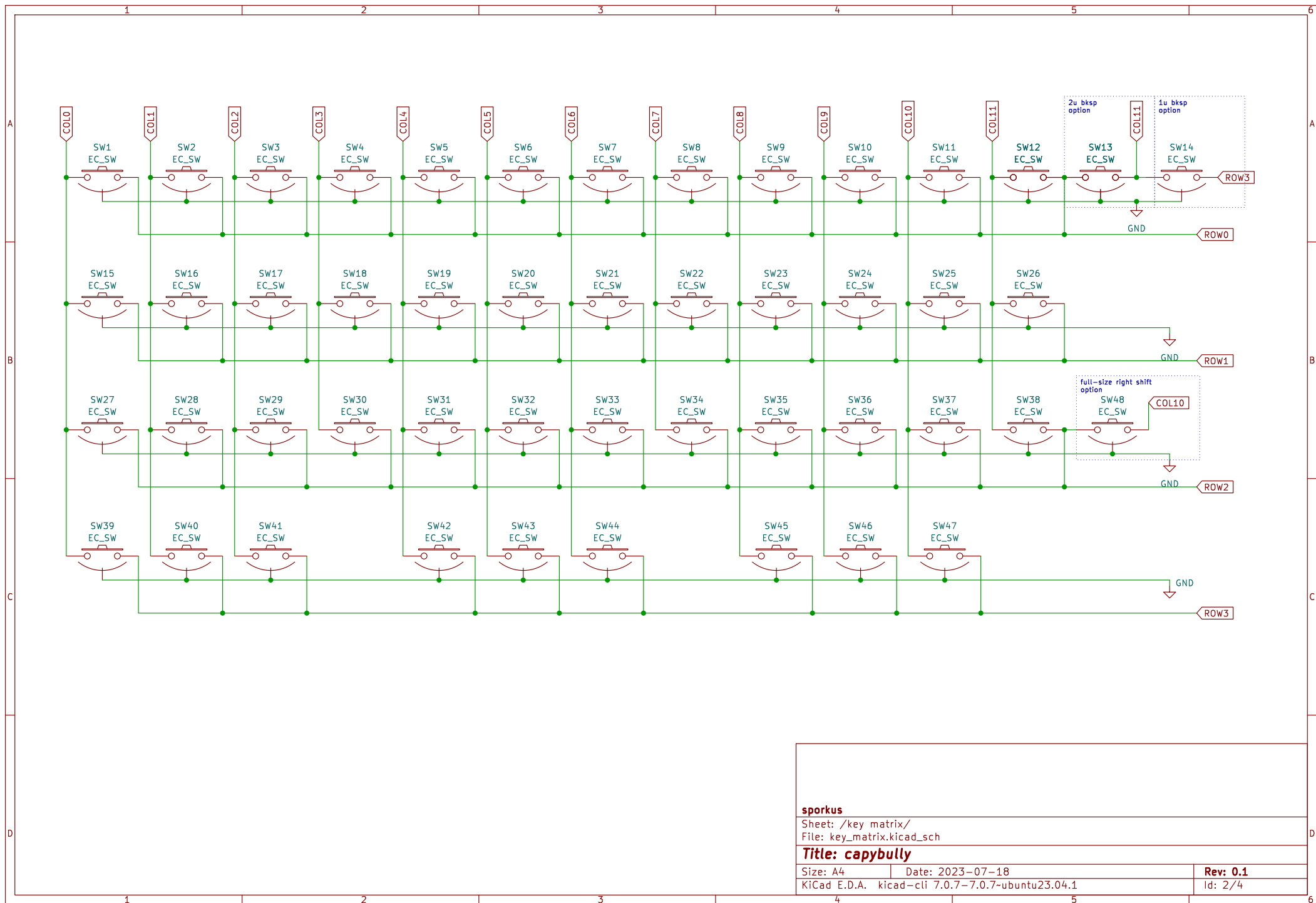
### 3V3 LDO

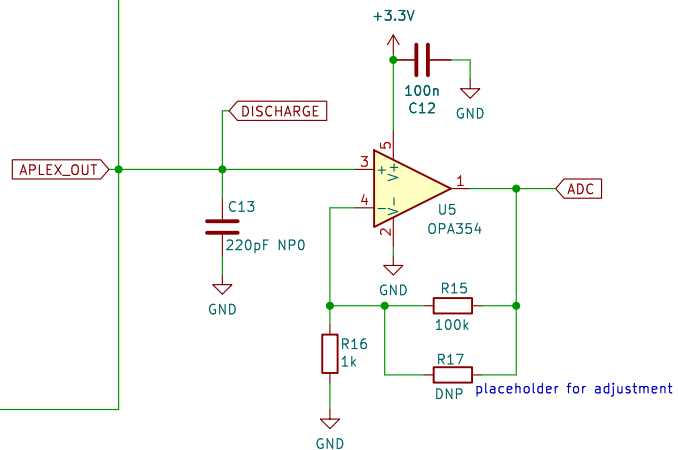
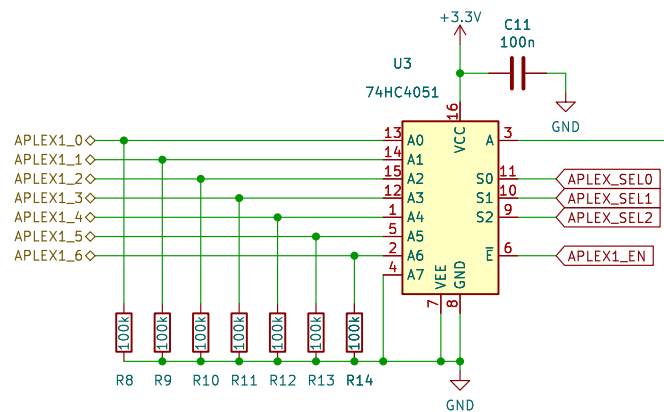
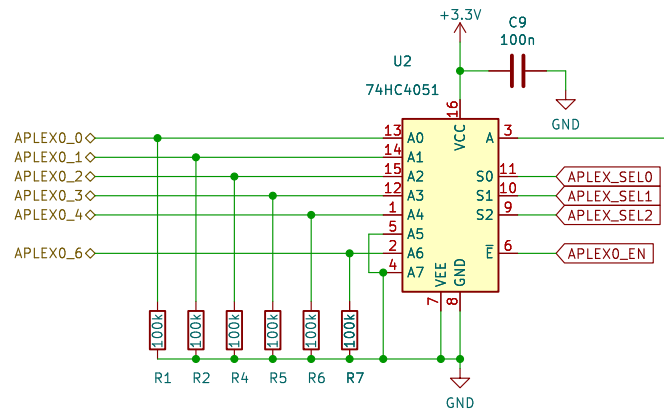
mounting\_holes.kicad\_sch

File: mounting\_holes.kicad\_sch

<b>sporkus</b>		
Sheet: /		
File: capybully.kicad_sch		
<b>Title: capybully</b>		
Size: A4	Date: 2023-07-18	Rev: 0.1
KiCad E.D.A. kicad-cli 7.0.7-7.0.7-ubuntu23.04.1		Id: 1/4

Rev: 0.1  
Id: 1/4





Alternatives:  
SC-70-6  
OPA358AIDCKR  
LMV861

SOT-23-5 seems to have better availability  
OPA354 to 358 seems ok

sporkus

Sheet: /analog/  
File: analog.kicad\_sch

Title: capybully

Size: A4 Date: 2023-07-18  
KiCad E.D.A. kicad-cli 7.0.7-7.0.7-ubuntu23.04.1

Rev: 0.1  
Id: 3/4

