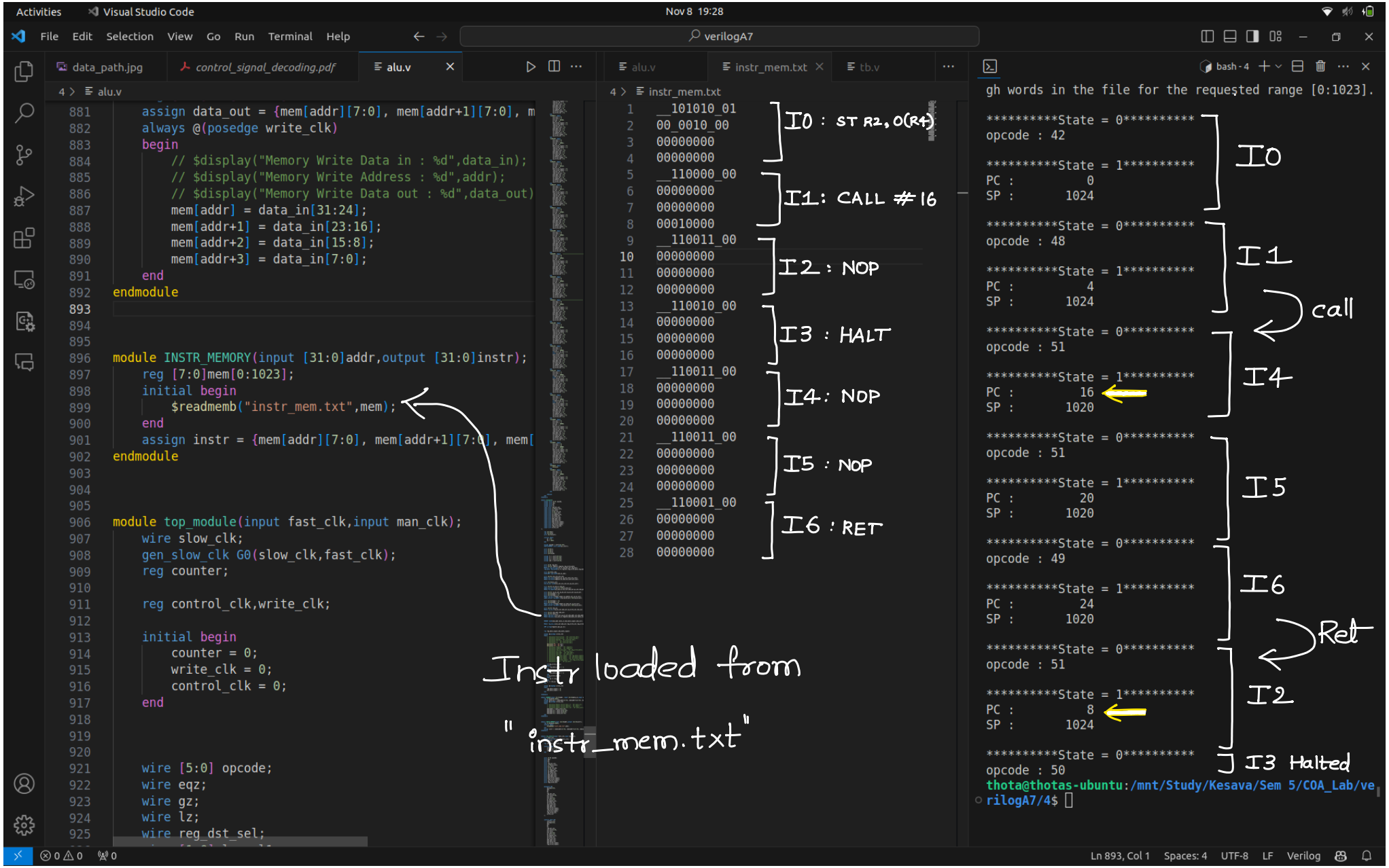
Activities
Visual Studio Code
Nov 8 19:28
File Edit Selection View Go Run Terminal Help
verilogA7
data_path.jpg
control_signal_decoding.pdf
alu.v
instr_mem.txt
tb.v
bash - 4
assign data_out = {mem[addr][7:0], mem[addr+1][7:0], m
always @(posedge write_clk)
begin
// $display("Memory Write Data in : %d",data_in);
// $display("Memory Write Address : %d",addr);
// $display("Memory Write Data out : %d",data_out)
mem[addr] = data_in[31:24];
mem[addr+1] = data_in[23:16];
mem[addr+2] = data_in[15:8];
mem[addr+3] = data_in[7:0];
end
endmodule
module INSTR_MEMORY(input [31:0]addr,output [31:0]instr);
reg [7:0]mem[0:1023];
initial begin
$readmemb("instr_mem.txt",mem);
end
assign instr = {mem[addr][7:0], mem[addr+1][7:0], mem[
endmodule
module top_module(input fast_clk,input man_clk);
wire slow_clk;
gen_slow_clk G0(slow_clk,fast_clk);
reg counter;
reg control_clk,write_clk;
initial begin
counter = 0;
write_clk = 0;
control_clk = 0;
end
wire [5:0] opcode;
wire eqz;
wire gz;
wire lz;
wire reg_dst_sel;
__101010_01
00_0010_00
00000000
00000000
__110000_00
00000000
00000000
00010000
__110011_00
00000000
00000000
00000000
__110010_00
00000000
00000000
00000000
__110011_00
00000000
00000000
00000000
__110001_00
00000000
00000000
00000000
I0 : ST R2, 0(R4)
I1: CALL #16
I2 : NOP
I3 : HALT
I4: NOP
I5 : NOP
I6 : RET
Instr loaded from
" instr_mem.txt"
gh words in the file for the requested range [0:1023].
*********State = 0*********
opcode : 42
*********State = 1*********
PC : 0
SP : 1024
*********State = 0*********
opcode : 48
*********State = 1*********
PC : 4
SP : 1024
*********State = 0*********
opcode : 51
*********State = 1*********
PC : 16
SP : 1020
*********State = 0*********
opcode : 51
*********State = 1*********
PC : 20
SP : 1020
*********State = 0*********
opcode : 49
*********State = 1*********
PC : 24
SP : 1020
*********State = 0*********
opcode : 51
*********State = 1*********
PC : 8
SP : 1024
*********State = 0*********
opcode : 50
thota@thotas-ubuntu:/mnt/Study/Kesava/Sem 5/COA_Lab/verilogA7/4$
I0
I1
call
I4
I5
I6
Ret
I2
I3 Halted
Ln 893, Col 1 Spaces: 4 UTF-8 LF Verilog