

Activities Visual Studio Code Nov 8 19:28

File Edit Selection View Go Run Terminal Help

data_path.jpg control_signal_decoding.pdf alu.v

4 > alu.v

```
881 assign data_out = {mem[addr][7:0], mem[addr+1][7:0], m
882 always @(posedge write_clk)
883 begin
884 // $display("Memory Write Data in : %d",data_in);
885 // $display("Memory Write Address : %d",addr);
886 // $display("Memory Write Data out : %d",data_out)
887 mem[addr] = data_in[31:24];
888 mem[addr+1] = data_in[23:16];
889 mem[addr+2] = data_in[15:8];
890 mem[addr+3] = data_in[7:0];
891 end
892 endmodule
893
894
895
896 module INSTR_MEMORY(input [31:0]addr,output [31:0]instr);
897 reg [7:0]mem[0:1023];
898 initial begin
899 $readmemb("instr_mem.txt",mem);
900 end
901 assign instr = {mem[addr][7:0], mem[addr+1][7:0], mem[
902 endmodule
903
904
905
906 module top_module(input fast_clk,input man_clk);
907 wire slow_clk;
908 gen_slow_clk G0(slow_clk,fast_clk);
909 reg counter;
910
911 reg control_clk,write_clk;
912
913 initial begin
914 counter = 0;
915 write_clk = 0;
916 control_clk = 0;
917 end
918
919
920
921 wire [5:0] opcode;
922 wire eqz;
923 wire gz;
924 wire lz;
925 wire reg_dst_sel;
```

4 > instr_mem.txt

```
1 101010 01 I0 : ST R2,0(R4)
2 00 0010 00
3 00000000
4 00000000
5 110000 00 I1: CALL #16
6 00000000
7 00000000
8 00010000
9 110011 00
10 00000000 I2 : NOP
11 00000000
12 00000000
13 110010 00
14 00000000 I3 : HALT
15 00000000
16 00000000
17 110011 00
18 00000000 I4: NOP
19 00000000
20 00000000
21 110011 00
22 00000000 I5 : NOP
23 00000000
24 00000000
25 110001 00
26 00000000 I6 : RET
27 00000000
28 00000000
```

gh words in the file for the requested range [0:1023].

```
*****State = 0*****
opcode : 42

*****State = 1*****
PC : 0
SP : 1024 I0

*****State = 0*****
opcode : 48

*****State = 1*****
PC : 4
SP : 1024 I1
call

*****State = 0*****
opcode : 51

*****State = 1*****
PC : 16
SP : 1020 I4
←

*****State = 0*****
opcode : 51

*****State = 1*****
PC : 20
SP : 1020 I5

*****State = 0*****
opcode : 49

*****State = 1*****
PC : 24
SP : 1020 I6
Ret

*****State = 0*****
opcode : 51

*****State = 1*****
PC : 8
SP : 1024 I2
←

*****State = 0*****
opcode : 50
thota@thotas-ubuntu: /mnt/Study/Kesava/Sem 5/COA_Lab/ve
rilogA7/4$ I3 Halted
```

Instr loaded from "instr_mem.txt"

Ln 893, Col 1 Spaces: 4 UTF-8 LF Verilog