CPET-233

Digital Systems Design

Fall 2019

Study Topics for Exam 1

Closed book – Closed Notes

The following syntax guide will be provided:

VHDL Syntax Sheet

Concurrent Statements		Sequential Statements
Concurrent Signal Assignment (dataflow model)		**Signal Assignment**
`target <= expression;`		`target <= expression;`
`A <= B AND C;` `DAT <= (D AND E) OR (F AND G);`		`A <= B AND C;` `DAT <= (D AND E) OR (F AND G);`
Conditional Signal Assignment (dataflow model)		***if* statements**

`target <= expressn when condition else`
`expressn when condition else`
`expressn;`
		`if (condition) then`
		`{ sequence of statements }`
		`elsif (condition) then`
		`{ sequence of statements }`
		`else --(the else is optional)`
		`{ sequence of statements }`
		`end if;`

Selective Signal Assignment (dataflow model)		***case* statements**

`with chooser_expression select`
`target <= expression when choices,`
`expression when choices;`
		`case (expression) is`
		`when choices =>`
		`{sequential statements}`
		`when choices =>`
		`{sequential statements}`
		`when others => -- (optional)`
		`{sequential statements}`
		`end case;`

Book sections covered on this exam:

Ch. 1, Ch. 2 sections 1-5

Ch. 3 section 6, Ch. 5 sections 1-4

Ch. 6 sections 3-4, 7-9

Ch. 10 sections 1-2, 5-8

Lectures covered:

Lecture 1 – Lecture 6

Homework covered:

HW #1 – HW #3

Labs covered:

Lab 1 – Lab 3

1. Know binary and hexadecimal numbering systems. Be able to convert between decimal and the other two. There is a powerpoint presentation on number systems posted with this study guide
2. Lecture 1 - Be familiar with the digital review. Be sure to know all of the gate and how they function. Know how to generate the un-simplified expression from a truth table. You will not have to do a Boolean reduction with algebra (yay!)
3. Lecture 2 – Know how to turn on specific segments in a common anode 7-segment display. Know which bit in the HEXn output vector correspond to the segments a-g. Understand waveform simulation and how to read a waveform to verify if an output is correct.
4. Know the purpose of simulation.
5. Understand what synthesis is.
6. Lecture 3 - Know what VHDL is, what it is used for, and the main parts of a module. Know the purpose for the entity and the architecture and the information contained in each. You do not have to memorize libraries. Know what signals are and how and where they are declared.
7. Lecture 4 - Understand the data types STD_LOGIC and STD_LOGIC_VECTOR and what they represent. Know how to write:
    a. Simple assignment statement
    b. Selected signal assignment
    c. Conditional signal assignment

    Be sure that you understand the concept of concurrency with regards to VHDL.

8. Lecture 5 – Know what a constant is and how to declare a constant. How does a constant differ from a signal (in use and assignment)? Understand what a process is and why it is used. How are statements evaluated inside a process? When are signal inside a process assigned their value? Know what a sensitivity list is and which signals belong in the sensitivity list. Be able to write:
    a. Case statement
    b. If/then/else statement

9. Lecture 6 - You will not have to write or use a test bench. However, you should be familiar with what a test bench is, what it is used for and how it is different from synthesizable VHDL. What statements can you use in a testbench that you cannot use in synthesizable VHDL.