Technical Objective:

Today, programmable devices can be used to replace many SSI devices. Prior to implementation in a programmable device, digital circuits can be designed and tested using a hardware description language (HDL) such as VHDL. In this lab, various VHDL implementations of the same circuit will be investigated. Additionally, the use of VHDL for simulation will be introduced.

Pre-Laboratory: (20%)

In this lab the **Phone Number Displayer** from labs 2 and 3 will be implemented using sequential VHDL, specifically a CASE and an IF statement. This lab can further be simplified with the use of CONSTANTS and grouping all seven outputs into a single STD_LOGIC_VECTOR.

1. Open a new project in Quartus

2. Write the VHDL entity and architecture for the **Phone Number Displayer** of lab 2 and lab 3 using a case statement. This implementation will have four inputs, but only one output. The output will be a STD_LOGIC_VECTOR that represents segments g-a of the seven segment display. Think about how you can use constants and the vector output to simplify the problem

3. Compile this implementation. Review the compilation errors and warnings and fix any problems.

4. Add another vector output to the entity. Drive this output with an implementation for the **Phone Number Displayer** that uses an If/then/elsif statement. Again use constants to simplify the problem.

5. Compile this implementation. Review the compilation errors and warnings and fix any problems.

6. Submit to the dropbox prior to lab:
    - Final VHDL of both implementations

Procedure: (60%)

1. Compile the VHDL version of the **Phone Number Displayer.**

2. Edit the testbench provided to match your implementation of the Phone Number Displayer. You must change the component and the port map.

3. Using the Modelsim tutorial from MyCourses, simulate your Phone Number

Displayer using the testbench provided.

4. Obtain a signoff for the simulation when you are sure it is correct.

5. Assign pins, download your design and verify operation on DE0-CV board. Assign the inputs to four switches and the outputs to two HEX displays. If the circuit does not perform as expected, your implementation could be wrong. Troubleshoot the circuit and make any necessary changes. Obtain a signoff for the working board.

Documentation: (20%)

This will be a formal lab report that covers labs **2, 3 and 4**. Your report must include the following:

- Abstract – objective, how the objective was met, summary of result
- Detailed discussion. This includes all pertinent design work
  - Truth tables, k-maps
  - Schematics
  - VHDL code
  - Modelsim waveforms
  - Other data collected
- Discussion and conclusion section that includes, but is not limited to, a comparison of the different implementations and the two simulation methods. What conclusion can you draw from this lab?
- Include all three signoff sheets

Signoffs and Grade:

Please submit with Lab 4 Report

Name:_____

Component	Signoff	Date	Time
Functional Simulation (30 pts)			
Working Board (30 pts)			

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Component	Received	Possible
Prelab		20
Signoff		60
Report		20
Penalties • after the first 15 minutes of lab session 5: -10 • after the first 15 minutes of lab session 6: -25 • no signoffs after the first 15 minutes of lab session 7:	-	
Total		100