Technical Objective:

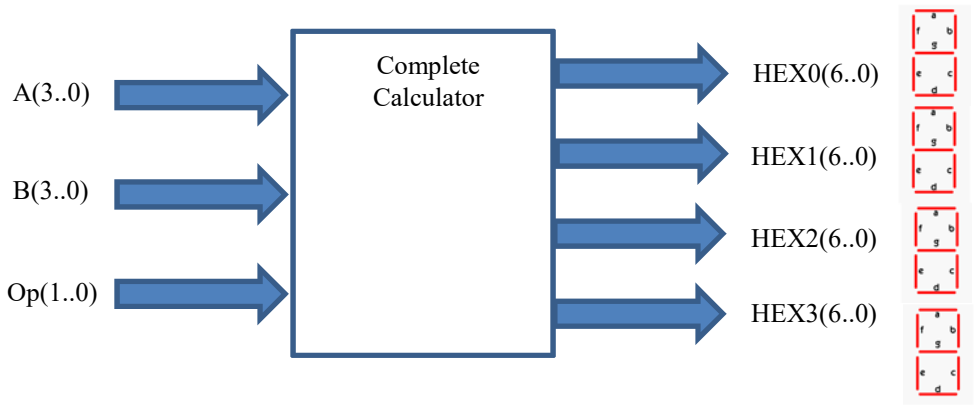
In hierarchical design a complex system is partitioned into functional modules. These functional modules are then interconnected to accomplish the system's overall operation. One advantage to this design approach is that each functional module can be fully tested for logical correctness prior to its integration into the overall system.

The purpose of this lab is to investigate hierarchical design. To accomplish this objective, the four-function calculator from lab 5 will be integrated with the display driver from lab 6 to create a four-function calculator that displays its results on four seven segment displays.

Pre-Laboratory: (20%)

1. Create a hierarchical VHDL module that combines the four-function calculator from lab 5 with the display driver from lab 6. **Your VHDL must use components.**
   a. Create a new project
   b. Add your Calculator.vhd and Display.vhd files to the directory
   c. Create a top level VHDL that contains two components, the calculator and the display driver. **You must use components.**
   d. The results of arithmetic operations should be displayed in signed decimal on the seven segment displays

2. The ports of the top level are illustrated below:



3. Submit your VHDL code to the dropbox prior to your lab section.

Procedure: (60%)

1. Download the Full_Calculator_tb.VHD file from MyCourses. Open the file and edit such that the component in the testbench matches exactly with your entity. If your port names are different than the ones on the component in the testbench, you will have to edit the port map as well.
2. Open a project in Modelsim and include ALL .vhd files from labs 5, 6 and 7 in addition to the testbench file. Simulate your Complete ALU design
3. Verify the operation of your module by inspecting the output waveform. Remember that the outputs you will be looking at are the constants needed to illuminate the correct segments on the display. They will not make sense in decimal radix. Run the wave.do file from lab 6 and change the radix of the outputs to get around this problem.
4. Print and annotate comments onto the Modelsim waveform printouts.
5. Obtain a signoff when you are sure your simulation is correct.
6. In Quartus, assign pins for the DE2 board.
7. Recompile the project with the pin assignments. Program the board.
8. Verify that your board is working and get a signoff.

Documentation: (20%)

This will be a formal lab report that covers labs 5, 6 and 7. Your report must include the following:

- Abstract – objective, how the objective was met, summary of result
- Detailed discussion. This includes all pertinent design work
  - Vhdl code
  - Modelsim waveforms
  - Other data collected
- Discussion and conclusion section. Are there practical applications for what you did? How can this lab be expanded?

Signoffs and Grade:

Please submit with Lab 7 Report

Name:_____

Component	Signoff	Date	Time
Functional Simulation (30 pts)			
Working Board (30 pts)			

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Component	Received	Possible
Prelab		20
Signoff		60
Report		20
Penalties • after the first 15 minutes of lab session 8: -10 • after the first 15 minutes of lab session 9: -25 • no signoffs after the first 15 minutes of lab session 10:	-	
Total		100