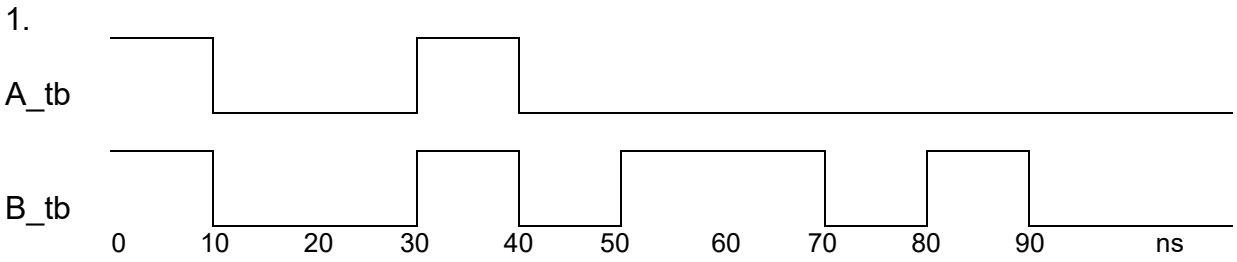
Homework #4 – Due 9/25/19
Please submit a hard copy or put in the Dropbox in MyCourses

1.



Assume A_tb and B_tb are signals declared inside of a testbench architecture. Using assignment statements and wait statements, write the testbench process to generate the waveforms shown above. Submit the VHDL code of the process.

2. Consider the 4-input 1-output function Prime that you designed in Homework #3. The output is a 1 if the binary number formed by the 4 inputs is a prime number. Write the VHDL code for a testbench that simulates Prime. The testbench should include a loop that applies all possible input combinations of the 4 inputs. Use the example in lectures and the testbench provided with lab 4 as a guide. Submit the VHDL code for the testbench

3. Use Modelsim to simulate the Prime circuit from HW #3 using the testbench you wrote in question #2. Verify all of the outputs are correct. Submit the waveforms.

4. Assume a prime number generator that determines if a binary number formed by 6 inputs is prime. Rewrite the loop from the testbench in question 2 to simulate the 6-bit prime number generator. Submit the loop code.