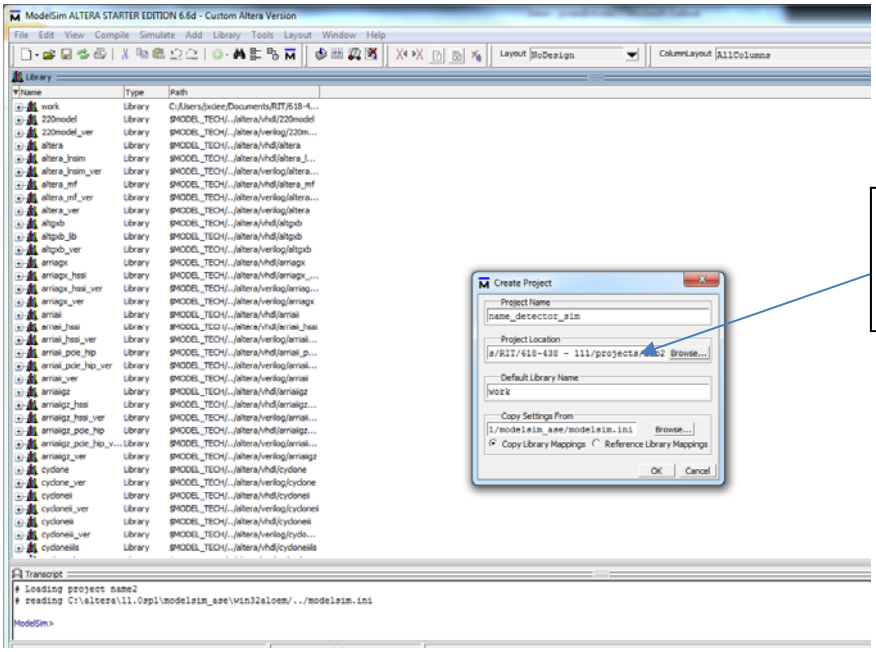
Using Modelsim

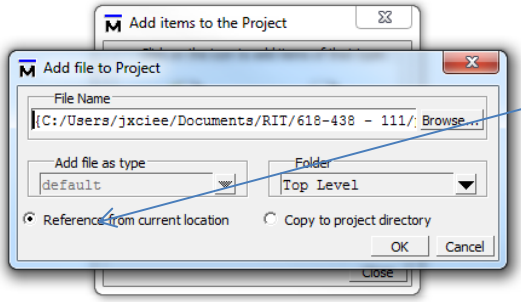
*note: this tutorial was written using Modelsim V6.6. The screen shots may vary slightly from other versions of the software

1. Invoke the Modelsim program
2. Click on File > New > Project
3. In the pop-up box, give the project a name and specify a location. It is best to keep it within the Quartus project already created. **Do not store your personal files on the C: drive.**



This should be on your S: drive with the rest of the project

4. Click OK
5. In the pop-up box, click on Add Existing File. Browse to your Quartus directory and select the design.vhd and the design_tb.vhd files



Make sure to leave this selected. You do not want to copy the files because then there will be two copies of the files

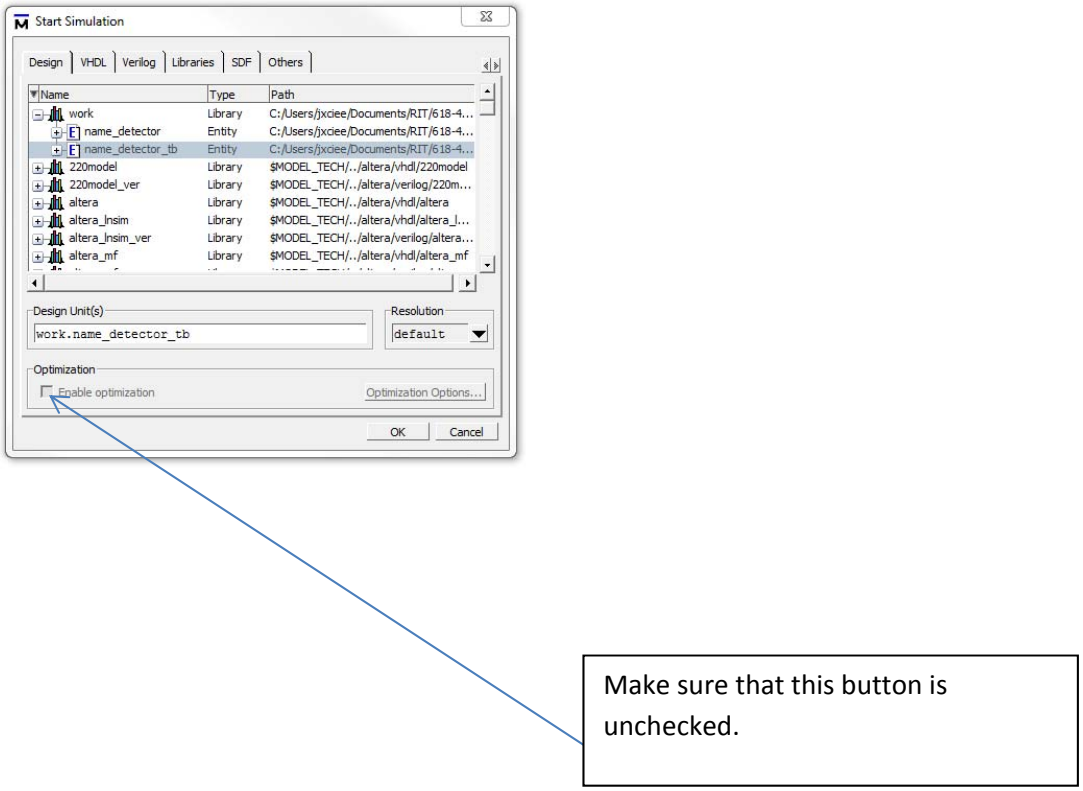
6. Click OK and then close

7. Notice that both file names have question marks after them. The question mark indicates that the file has not been compiled.

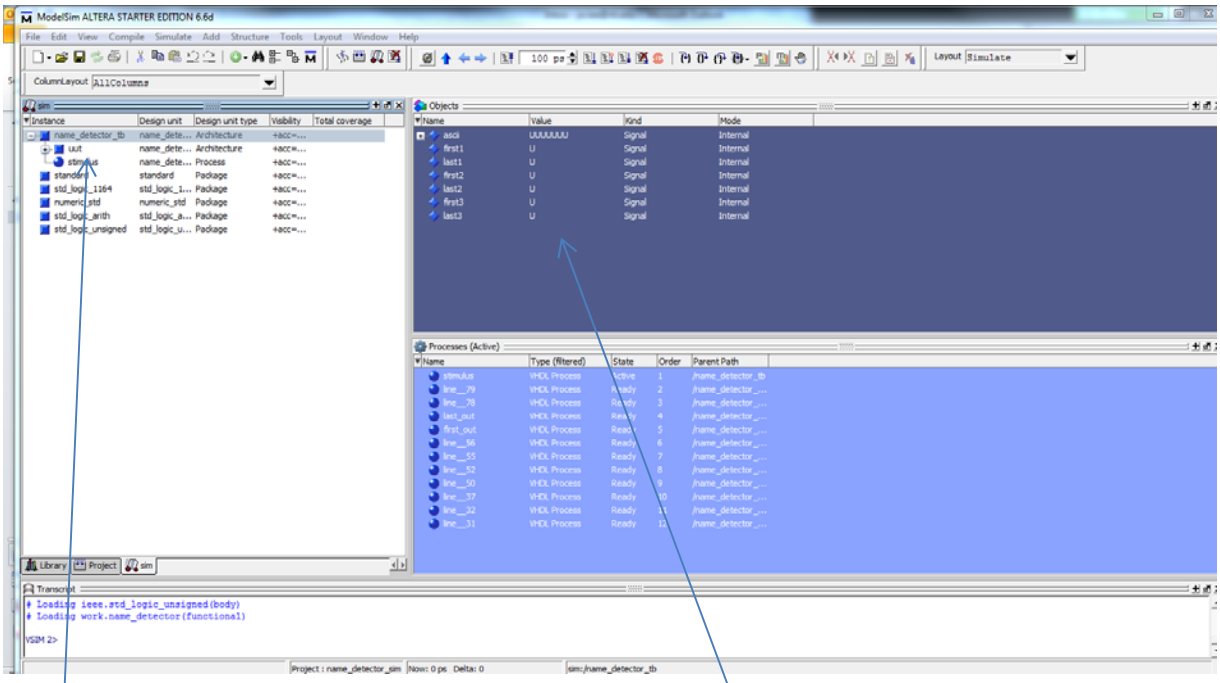
*note to the wise: Compiling VHDL files in Modelsim is faster than compiling in Quartus. The reason for this is that Modelsim simply compiles the file while Quartus synthesizes and prepares the design for implementation in the FPGA.

*Second note: testbench files will not compile in Quartus because they are not synthesizable.

8. Choose Compile > Compile All.
9. If the compile fails, double click on the error message and then double click again to open the file for editing.
10. Repeat steps 9 and 10 until both files compile
11. Click on Simulate > Start Simulation
12. In the pop-up box click on the + next to 'work' and then the tb file



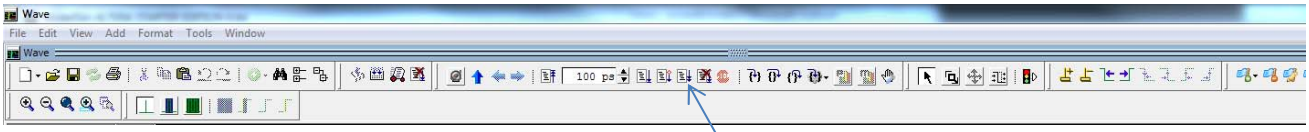
13. Click OK
14. Your workspace should look similar to this:



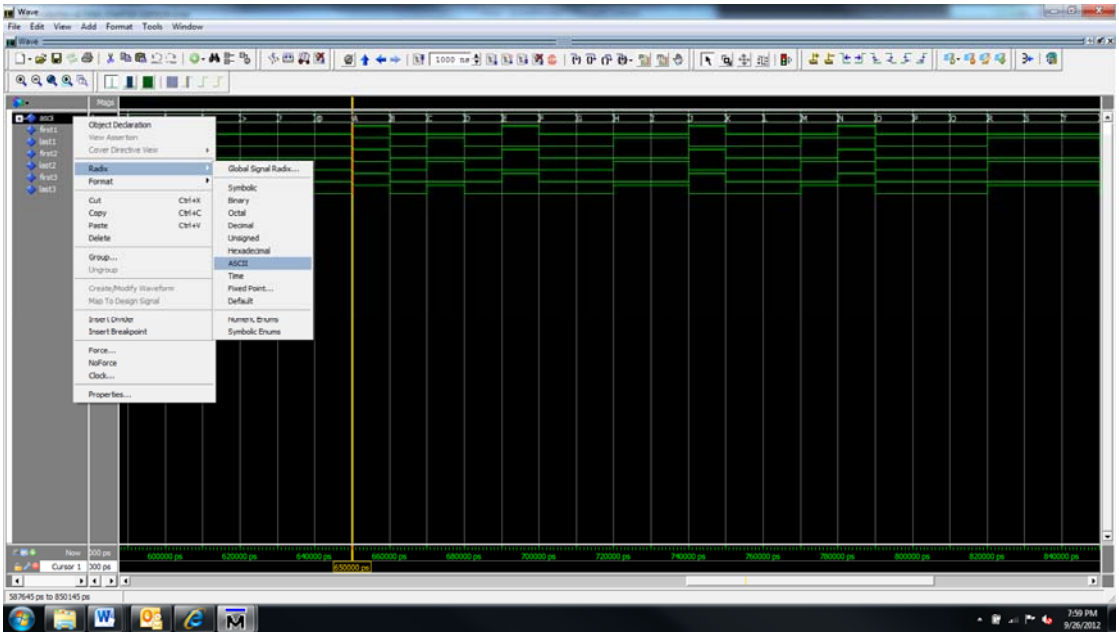
These should be the signals that you declared in the testbench.

Under the testbench file name, you should see 'uut'. If not, your testbench is not connected to the module it is testing and the sim will fail.

15. Select all of the signals in the Objects window (upper blue window), right click and choose add > to wave > selected signals.
16. Move the wave window to the second monitor and enlarge
17. Click on the third icon to the right of the time box. (-run all)

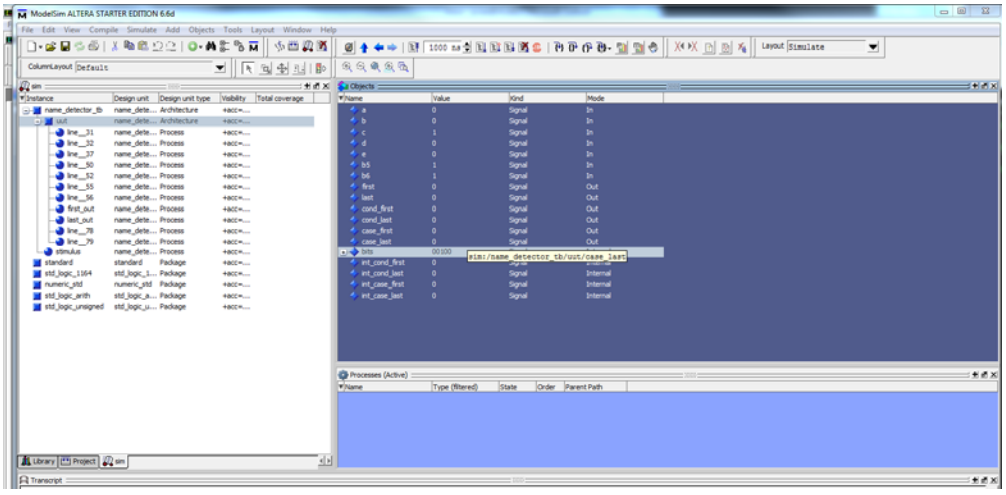


18. Right click in the waveform area to zoom in and out.
19. Visually inspect the waveforms for correctness.

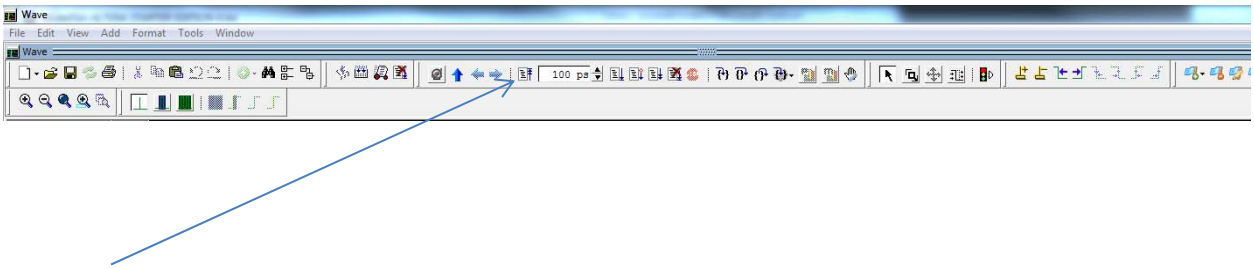


You can change the radix to integer or hex to make verifying the results easier.

20. If the results are not correct, you will need to go back to you original VHDL file to find the error.
21. To monitor internal signals during the simulation, click on ‘uut’ as shown below and the internal signals will be displayed in the ‘objects’ window. Choose the signal you would like to monitor and add it to the waveform.



22. Once you add a new signal, there will not be any history for it. Click on the icon to the left of the time box



23. Click OK in the pop up box. Click on the run icon to rerun the simulation/.
24. If you edit your design.vhd file, you will need to recompile it and reset the simulation prior to resimulating.