Hierarchical Design and Components II

Announcements

- Homework #6 due Wednesday
- Quiz Wednesday on hierarchical design and components
- If you haven't already done so, please submit your team evaluations.

Lab 6 Intro

- REM
  - Synthesizable for unsigned type
  - x REM y returns the remainder of x/y , with the sign of x

- When doing VHDL arithmetic you can use integer operands
  - Ex: abs_num REM 100
  - Ex: count <= count + 1;

Practice problems

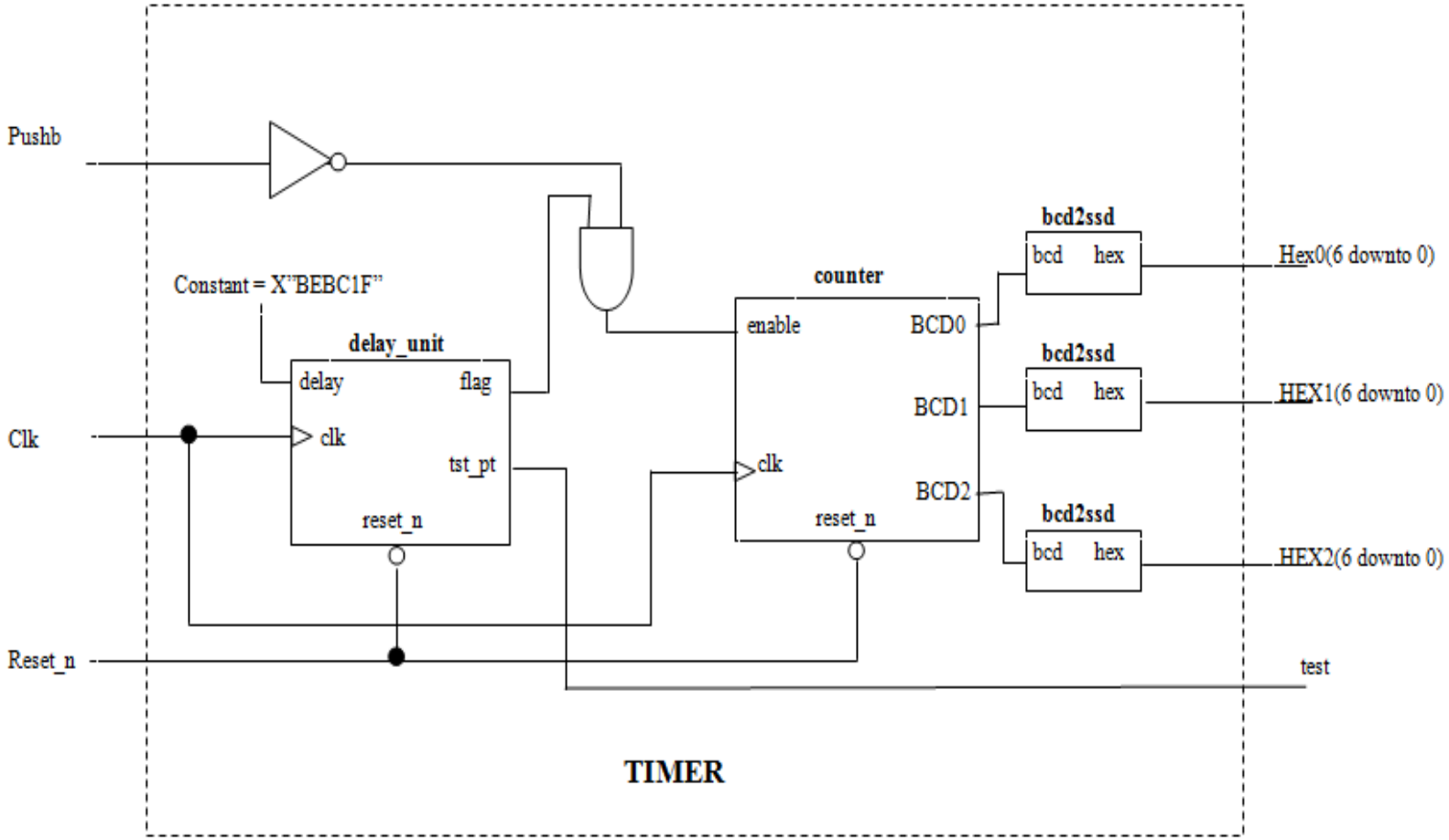
For the design description that follows, draw the corresponding logic diagram:

```
ENTITY gate_ckt IS
            PORT(a, b, c : IN STD_LOGIC;
                       F      : OUT STD_LOGIC);
END gate_ckt;

ARCHITECTURE structure OF gate_ckt IS
    SIGNAL s1, s2 : STD_LOGIC;
    COMPONENT nand_2 IS
            PORT(i1, i2      : IN STD_LOGIC;
                       o1         : OUT STD_LOGIC);
            END COMPONENT;

    COMPONENT invert IS
            PORT(i1           : IN STD_LOGIC;
                       o1         : OUT STD_LOGIC);
          END COMPONENT;

   BEGIN
          U0: nand_2 PORT MAP(i1 => a,
                                          i2 => b,
                                          o1 => s1);
          U1: nand_2 PORT MAP(i1 => s1,
                                          i2 => s2,
                                          o1 => f);
          U2: invert PORT MAP(i1 => c,
                                         o1 => s2);
END structure;
```


Pushb
Constant = X"BEBC1F"
delay_unit
delay
flag
clk
tst_pt
reset_n
Clk
Reset_n
counter
enable
BCD0
BCD1
BCD2
clk
reset_n
bcd2ssd
bcd
hex
bcd2ssd
bcd
hex
bcd2ssd
bcd
hex
Hex0(6 downto 0)
HEX1(6 downto 0)
HEX2(6 downto 0)
test
TIMER