VHDL Practice Problems

Announcements

- Homework #3 due today
- Homework #4 is posted
- Exam #1 on Monday 9/23!

Save the Date!!!

DSD Exam #1 Study Jam

Sunday September 22nd

12-4 pm

GOL - 1360

Led by past students

3-to-8 Decoder

Input			Output							
S2	S1	S0	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

Note: The selected output goes HIGH.

1. Create the entity
2. Create 4 architectures : selected signal assignment, conditional signal assignment, case, if/then/else

AOI Equations and Circuits

A	B	C	F_4
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0

1. Create the unsimplfied SOP equation.
2. Find the most reduced equation.
3. Draw the AOI circuit for F_4
4. Write the VHDL architecture to drive output F_4. You may choose your statement type.