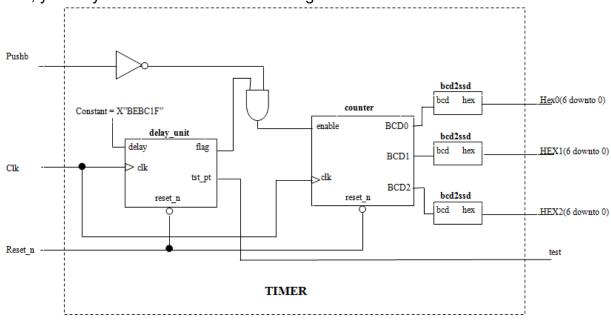


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Homework #7 – Due 10/16/19 Please submit a hard copy or put in the Dropbox in MyCourses

1. Using the diagram of a digital system shown below, complete the structural VHDL. For this problem you only have to write the top level architecture. You do not have to write the code for the delay_unit, counter and bcd2ssd. Remember, you can port map to a constant, but you cannot port map to an expression. As such, you may need to add some internal signals.



ENTITY TIMER IS

PORT (Pushb, clk, reset_n : IN STD_LOGIC; Test : OUT STD LOGIC;

HEX0, HEX1, HEX2 : OUT STD_LOGIC_VECTOR(6 downto 0));

END TIMER;

ARCHITECTURE structure OF timer IS

COMPONENT delay unit IS

PORT(delay : IN STD LOGIC VECTOR(23 downto 0);

clk, reset_n : IN STD_LOGIC;

flag, tst pt : OUT STD LOGIC);

END COMPONENT;

COMPONENT counter IS

PORT(enable, clk, reset n : IN STD LOGIC;

BCD0,BCD1,BCD2 : OUT STD LOGIC VECTOR(3 DOWNTO 0));

END COMPONENT;

COMPONENT bcd2ssd IS

PORT(bcd : IN STD_LOGIC_VECTOR(3 DOWNTO 0); Hex : OUT STD_LOGIC_VECTOR(6 DOWNTO 0));

END COMPONENT;



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2. Write the VHDL to implement a hexadecimal display driver. This system has one input which is and 8-bit std_logic_vector and 2 7-bit outputs that drive the seven segment displays. You must use components. Hint: you already wrote code that takes in a 4-bit binary number and outputs the constants to display the 16 hexadecimal digits on the seven segment displays. Submit your top level code and for any components you instantiate.

Example: 11010001 = D110100100 = A4

3. Use the testbench provided to simulate your system in Modelsim. Change the radix of the input number to hexadecimal. Run the wave.do file and change the radix of the hex outputs to radix_ssd to make verification easier. Zoom in a sufficient amount so that the waveform is readable and take several screen shots. Submit the screen shots.