CPET-233 Digital Systems Design
Fall 2019

Homework #11 – Due 11/20/19
Please submit a hard copy or put in the Dropbox in MyCourses

1. Using the traffic light controller state transition diagram created in class, write the full VHDL for the state machine. Assume that the input called ‘timer’ is a std_logic_vector coming from an external counter and it increments every second. The timer will be reset on every state transition.

   After compiling the VHDL choose tools > Netlist Viewers > State Machine Viewer. Compare the resulting state transition diagram to your original. If they don’t match, you did something wrong in the code. Submit the original state transition diagram, your code and the Quartus generated diagram.

2. Using the washing machine controller state transition diagram from HW #10, write the full VHDL for the state machine. Assume that the input called ‘timer’ is a std_logic_vector coming from an external counter and it increments every minute. The timer will be reset on every state transition

   After compiling the VHDL choose tools > Netlist Viewers > State Machine Viewer. Compare the resulting state transition diagram to your original. If they don’t match, you did something wrong in the code. Submit the original state transition diagram, your code and the Quartus generated diagram.
   *Note: the code for this question will be graded based on the state transition diagram you submit. If the diagram was wrong, you will not lose credit as long as the code matches the diagram.