CPET-231 Exam #3

Monday, November 18, 2019

In Class

~ Closed books ~ Closed Notes ~ Calculators are allowed ~

Book sections covered on this exam:

Ch. 6 section 2

Ch. 13, sections 1-2, 4-5

Ch. 11 Sections 1-4

Lectures covered:

Lecture 11 – Lecture 17

Homework covered:

HW #8 – HW #11

Labs covered:

Lab 7 – Lab 10

All material from exams 1 & 2

1. Lecture 11
   - Understand how to write VHDL for synchronous systems
   - Be able to create a synchronous VHDL with a synchronous or asynchronous reset. Be sure you know what it means
   - Be able to write the VHDL for a flip flop
   - Understand what a latch is, how it is inferred and how it differs from a flip-flop

2. Lecture 12
   - Understand what a register is and how to write the VHDL for a register of any size
   - Know how to create a counter of any size that counts either up or down
   - Know how to create a counter that stops at any value and how to use a counter to create a delay
   - Understand how an enable works for any synchronous component and be able to create a synchronous component with an enable
   - Be familiar with BCD counters and how they differ from binary counters. Think about why you would use one over the other

3. Lecture 13
   - Understand the difference between a regular register and a shift register in terms of operation and design
   - Know how shift registers work and how to create one in VHDL. Be sure you know how to load and how to shift in either direction.
   - Be sure to understand the difference between serial and parallel data and how a shift register is used to convert between the two formats.
   - Pay careful attention to the feedback on HW 9.

4. Lecture 14
    - Know how to declare an array type for a one-dimensional and a two-dimensional array.
    - Understand what arrays are and how to assign values to a complete array and individual elements in an array
    - Know how to create a lookup table with an array
    - You will not have to create RAM, but you need to understand how a two-dimensional array is used to create one

5. Lecture 15 - 17
    - Review carefully the lecture notes on state machines
    - Understand the difference between Mealy and Moore state machines. You will not have to design a Mealy state machine
    - Understand the relationship between the state machine VHDL code and the synthesized hardware, although you will not have to design a state machine with gates (only VHDL).
    - Understand what one-hot encoding means and the relationship between number of states and number of flip-flops
    - For the VHDL, understand enumerated types and also the purpose of the 3(+) processes used in a state machine. Be able to write all 3(+) processes.
    - Be able to create a state transition diagram and write VHDL code from a given state transition diagram

Review homework and lab assignments. Anything covered on either is fair game for a question.