Homework #10 – Due 11/13/19
Please submit a hard copy or put in the Dropbox in MyCourses

1. Textbook exercise 11.5 (page 314) parts a and b (one-hot only). Submit the state transition diagram and flip- flop estimate.
2. Textbook exercise 11.10 on page 315. The figure being referenced is on page 316. Submit the new state transition diagram. You do not have to write any code.
3. What determines the minimum length of time a fully synchronous state machine remains in a state? How can such a state machine remain in the same state for a longer period of time? Submit your answers.
4. Create a state transition diagram for a washing machine controller.

   The states are as follows:
   - Idle – machine stays in idle until start is pressed
   - Fill – machine stays in fill until the drum is full
   - Agitate – machine stays in Agitate for 7 minutes
   - Drain – machine stays in drain until the drum is empty
   - Rinse – machine stays in rinse until the drum is full
   - Spin – the machine stays in spin until 10 minutes have passed and the drum is empty

   The inputs are:
   - Start (1 if the start button is pressed, 0 if not pressed)
   - Full (1 if the drum is full, 0 if it is not full)
   - Empty (1 if the drum is empty, 0 if not empty)
   - Minute timer (This input comes from an external timer. The timer starts at 0 each time a new state is entered)

   The outputs are:

STATE	FILL_VALVE	DRUM_MOTOR	EMPTY_VALVE
Idle	Off	Off	Off
Fill	On	Off	Off
Agitate	Off	On	Off
drain	Off	Off	On
rinse	On	Off	Off
spin	Off	On	On

   Submit the state transition diagram.

5. If you create a RAM in VHDL that is 2K x 8 (2K locations that are 8 bits wide), how many of the FPGA flip flops will be used?