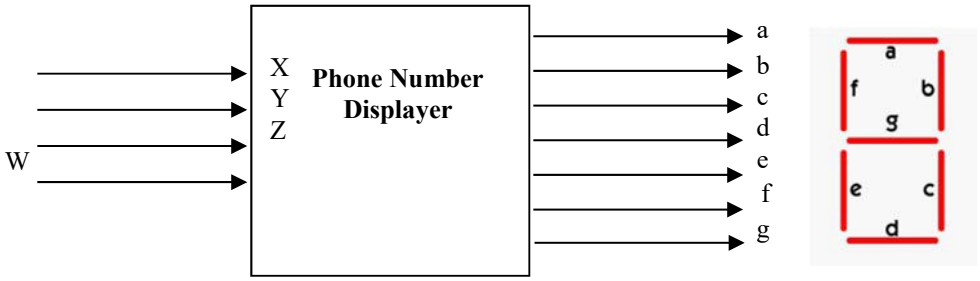
Technical Objective:

Modern digital circuits are no longer designed using schematics of discrete gates. Instead, a hardware description language such as VHDL is used to describe the structure and/or behavior of the circuit. A synthesizer then converts the description to the underlying logic equations. This lab investigates the VHDL implementation of a logic circuit previously designed with discrete gates.

Pre-Laboratory: (30% of grade)

The block diagram shown below represents the **Phone Number Displayer** that has four inputs and seven outputs. The four inputs, X, Y, Z and W select which digit of the phone number is displayed. The seven outputs, a, b, c, d, e, f and g drive the segments of a common anode seven segment display.



1. In lab 2 you generated the simplified equations for the 7 outputs. Using simple VHDL concurrent signal assignment statements (AND, OR, etc) design the multiple-output function implementation for the **Phone Number Displayer** using the equations you obtained in lab 2.

2. Compile this implementation. Review the compilation errors and warnings and fix any problems.

3. Add another seven outputs to the entity. Name them a_cond, b_cond, c_cond, etc. Drive these outputs with an implementation for the **Phone Number Displayer** that uses Conditional Signal Assignments (WHEN..ELSE). This implementation can be in the same architecture as the implementation in step 1.

4. Compile this implementation. Review the compilation errors and warnings and fix any problems.

5. Add another seven outputs to the entity. Name them a_sel, b_sel, etc. Drive these outputs with an implementation for the **Phone Number Displayer** that uses Selected Signal Assignments (WITH..SELECT). This implementation can be in the same architecture as the other two implementations

6. Compile this implementation. Review the compilation errors and warnings and fix any problems.

7. Submit to the dropbox prior to lab:
   - Final VHDL file with all three implementations in one architecture.

Procedure: (70% of grade)

1. Compile the VHDL version of the **Phone Number Displayer.**

2. Create an input waveform file to verify operation of the design for all possible combinations of inputs. Use the Altera waveform simulator to simulate the design. Verify that all three implementations produce the correct outputs. Annotate comments to the output waveforms and obtain a signoff.

3. Assign pins, download your design and verify operation on DE0-CV board. You will need to use 3 different seven segment displays. If the circuit does not perform as expected, your implementation could be wrong. Troubleshoot the circuit and make any necessary changes. Obtain a signoff for the working board.

Documentation:

There is no lab report for this lab. Save all of your work and your signoffs as it will become part of the documentation for lab #4.

Signoffs and Grade:

Please submit with Lab 4 Report

Name:_____

Component	Signoff	Date	Time
Functional Simulation (35 pts)			
Working Board (35 pts)			

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Component	Received	Possible
Prelab		30
Signoff		70
Penalties • after the first 15 minutes of lab session 4: -10 • after the first 15 minutes of lab session 5: -25 • no signoffs after the first 15 minutes of lab session 6:	-	
Total		100