8M MINI SOM

Table of Content

Page 1	Cover
Page 2	Block Diagram
Page 3	PWR TREE
Page 4	CPU PWR
Page 5	LPDDR4
Page 6	CPU IO
Page 7	CPU PHY
Page 8	CPU MISC
Page 9	eMMC//QSPI
Page 10	WIFI/BT Module
Page 11	BOOT CFG
Page 12	PMIC
Page 13	SOM Interface

Revision History

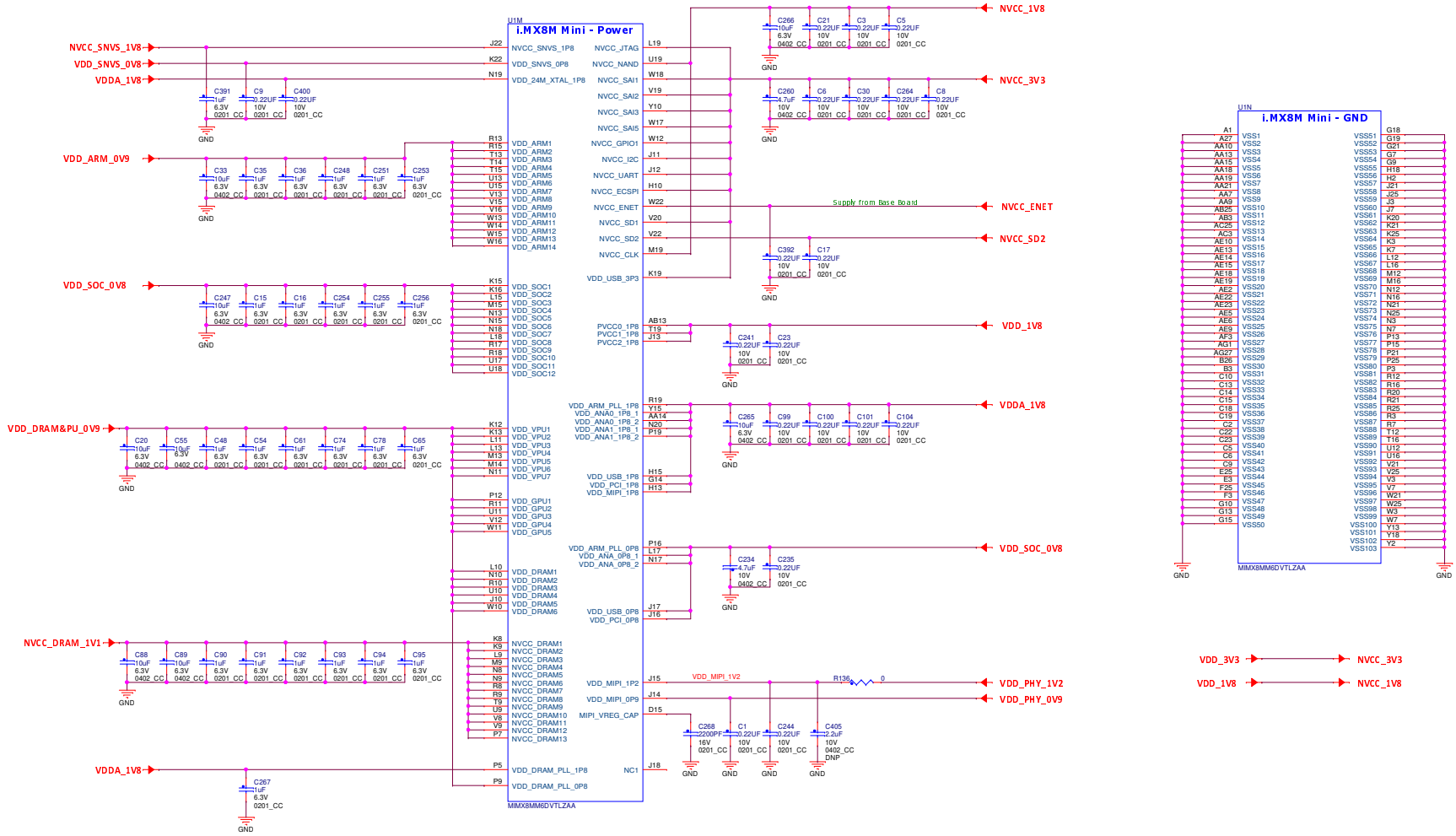
Rev. Code	Date	By	Description
1A	2019-12-12	AB	Initial version based on SCH-31399 Rev C2
2A	2020-06-15	AB	All the I2C pull-ups were reconnected from 1V8 to 3V3

EMCRAFT SYSTEMS LLC
5621 Palmer Way, Suite A
Carlsbad, CA 92010

ICAP Classification: CP: IUO: PUBI: X

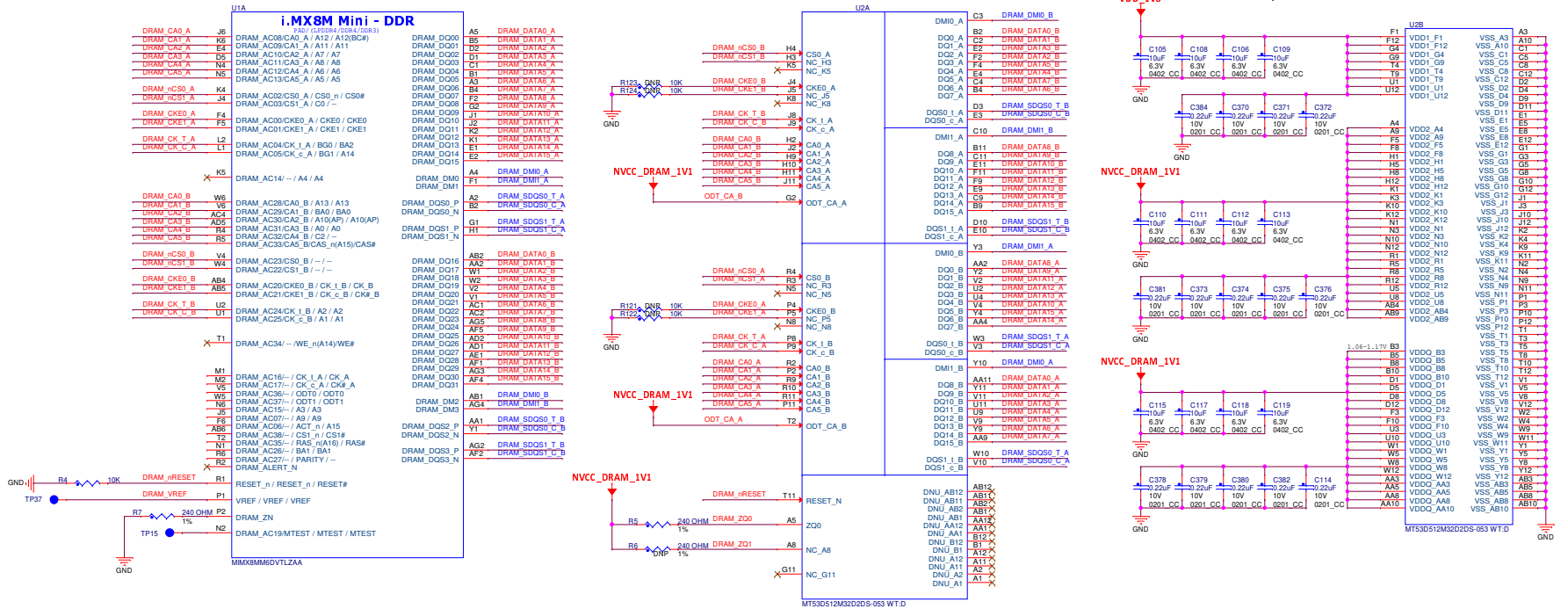
Designer: <Designer>	Drawing Title: 8M LPDDR4 SOM	
Drawn by: <DrawnBy>	Page Title: Title and Rev History	
Approved: <Approver>	Size B / Document Number <Doc>	Rev 2A
	Date: Wednesday, June 24, 2020	Sheet 1 of 11

i.MX8M Mini PWR



EmCraft systems	EMCRAFT SYSTEMS LLC 5621 Palmer Way, Suite A Carlsbad, CA 92010	
This document contains information proprietary to Emcraft and shall not be used for engineering design, procurement or manufacture in whole or in part without the express written permission of Emcraft Systems LLC.		
	ICAP Classification: CP: IUO: PUBL X	
Designer: <Designer>	Drawing Title: 8M LPDDR4 SOM	
Drawn by: <DrawnBy>	Page Title: CPU Power	
Approved: <Approver>	Size C / Document Number <Doc>	Rev 2A
	Date: Wednesday, June 24, 2020	Sheet 2 of 11

LPDDR4 2GB



Data Bus

Pin Name	LPDDR4	DDR4
DRAM_D00_P	DQ0_L_A	DQ0_L_A
DRAM_D00_N	DQ0_C_A	DQ0_C_A
DRAM_D00	DMI0_A	DMI_L_A / DBI_n_A
DRAM_D00	DQ0_A	DQ0_A
DRAM_D01	DQ1_A	DQ1_A
DRAM_D02	DQ2_A	DQ2_A
DRAM_D03	DQ3_A	DQ3_A
DRAM_D04	DQ4_A	DQ4_A
DRAM_D05	DQ5_A	DQ5_A
DRAM_D06	DQ6_A	DQ6_A
DRAM_D07	DQ7_A	DQ7_A
DRAM_DQS1_P	DQS1_L_A	DQS1_L_A
DRAM_DQS1_N	DQS1_C_A	DQS1_C_A
DRAM_DM1	DMI1_A	DMI_L_A / DBI_n_A
DRAM_D08	DQ8_A	DQ0_A
DRAM_D09	DQ9_A	DQ1_A
DRAM_D10	DQ10_A	DQ2_A
DRAM_D11	DQ11_A	DQ3_A
DRAM_D12	DQ12_A	DQ4_A
DRAM_D13	DQ13_A	DQ5_A
DRAM_D14	DQ14_A	DQ6_A
DRAM_D15	DQ15_A	DQ7_A
DRAM_DQS2_P	DQS2_L_A	DQS0_L_B
DRAM_DQS2_N	DQS2_C_A	DQS0_C_B
DRAM_DM2	DMI2_A	DMI_L_B / DBI_n_B
DRAM_D16	DQ0_B	DQ0_B
DRAM_D17	DQ1_B	DQ1_B
DRAM_D18	DQ2_B	DQ2_B
DRAM_D19	DQ3_B	DQ3_B
DRAM_D20	DQ4_B	DQ4_B
DRAM_D21	DQ5_B	DQ5_B
DRAM_D22	DQ6_B	DQ6_B
DRAM_D23	DQ7_B	DQ7_B
DRAM_DQS3_P	DQS3_L_B	DQS1_L_B
DRAM_DQS3_N	DQS3_C_B	DQS1_C_B
DRAM_DM3	DMI3_B	DMI_L_B / DBI_n_B
DRAM_D24	DQ08_B	DQ0_B
DRAM_D25	DQ09_B	DQ1_B
DRAM_D26	DQ10_B	DQ2_B
DRAM_D27	DQ11_B	DQ3_B
DRAM_D28	DQ12_B	DQ4_B
DRAM_D29	DQ13_B	DQ5_B
DRAM_D30	DQ14_B	DQ6_B
DRAM_D31	DQ15_B	DQ7_B

Command/Address

Pin Name	LPDDR4	DDR4
DRAM_RESET_N	RESET_N	RESET_n
DRAM_ALERT_N	MTEST1	ALERT_n / MTEST1
DRAM_AC00	CKE0_A	CKE0
DRAM_AC01	CKE1_A	CKE1
DRAM_AC02	CS0_A	CS0_n
DRAM_AC03	CS1_A	C0
DRAM_AC04	CK_t_A	BG0
DRAM_AC05	CK_c_A	BG1
DRAM_AC06	/	ACT_n
DRAM_AC07	/	A9
DRAM_AC08	CA0_A	A12
DRAM_AC09	CA1_A	A11
DRAM_AC10	CA2_A	A7
DRAM_AC11	CA3_A	A8
DRAM_AC12	CA4_A	A6
DRAM_AC13	CA5_A	A5
DRAM_AC14	/	A4
DRAM_AC15	/	A3
DRAM_AC16	/	CK_t_A
DRAM_AC17	/	CK_c_A
DRAM_AC19	MTEST	MTEST
DRAM_AC20	CKE0_B	CK_t_B
DRAM_AC21	CKE1_B	CK_c_B
DRAM_AC22	CS0_B	/
DRAM_AC23	CS1_B	/
DRAM_AC24	CK_t_B	A2
DRAM_AC25	CK_c_B	A1
DRAM_AC26	/	BA1
DRAM_AC27	/	PARITY
DRAM_AC28	CA0_B	A13
DRAM_AC29	CA1_B	BA0
DRAM_AC30	CA2_B	A10 / AP
DRAM_AC31	CA3_B	A0
DRAM_AC32	CA4_B	C2
DRAM_AC33	CA5_B	CAS_n / A15
DRAM_AC34	/	WE_n / A14
DRAM_AC35	/	RAS_n / A16
DRAM_AC36	/	ODT0
DRAM_AC37	/	ODT1
DRAM_AC38	/	CS1_n
DRAM_ZN	ZQ	ZQ
DRAM_VREF	VREF	VREF

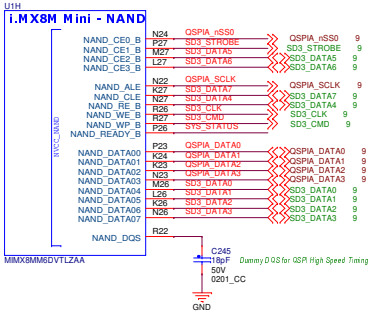
EMCRAFT SYSTEMS LLC
5621 Palmer Way, Suite A
Carlsbad, CA 92010

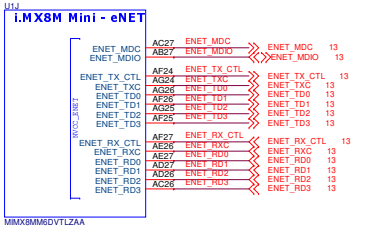
ICAP Classification: CP: IUO: PUBL: X

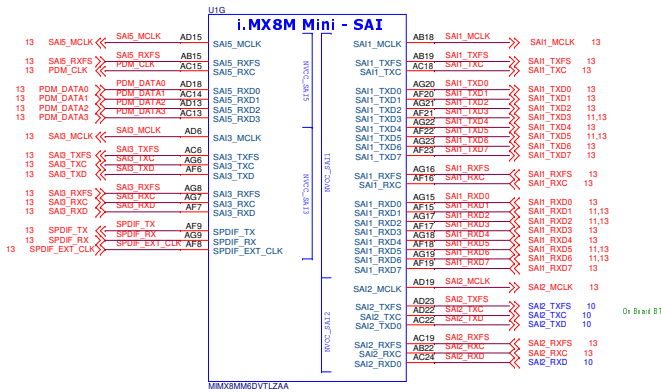
Designer: <Designer>	Drawing Title: 8M LPDDR4 SOM	
Drawn by: <DrawnBy>	Page Title: 32-bit LPDDR4	
Approved: <Approver>	Size: C	Document Number: <Doc> Rev: 2A
	Date: Wednesday, June 24, 2020	Sheet 3 of 11

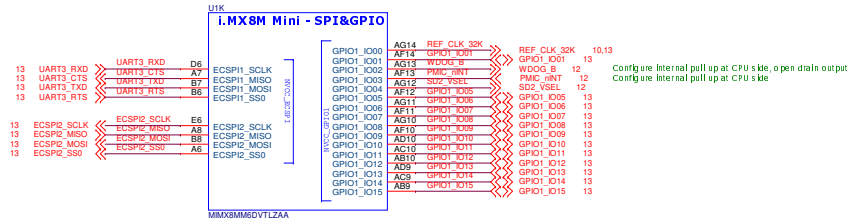
i.MX8M Mini IO Interface

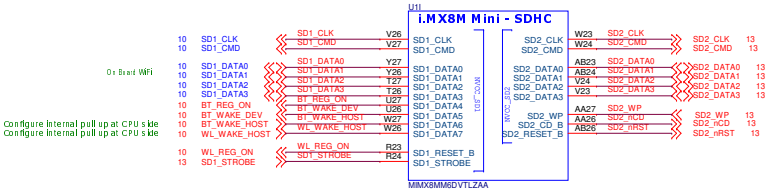
Caution:
IO internal pull up/down is not supported in 3.3V mode, must disable the internal pull up/down via software and use external pull up/down resistors instead.
All IO pin groups are impacted except for XTAL, DDR, PCI, USB and MIPI PHY IO's.
See Errata e50080 for detailed information.

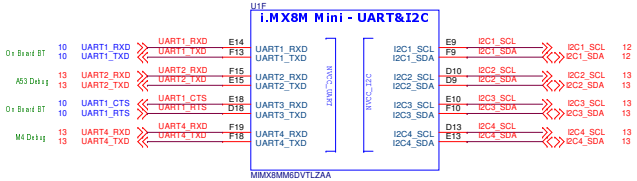


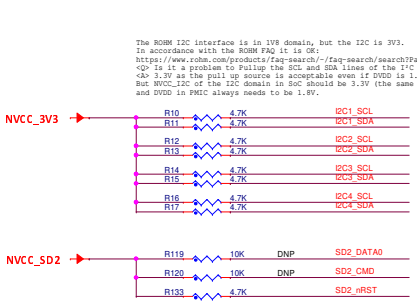


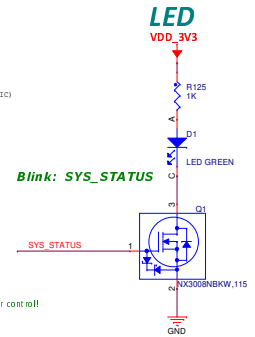






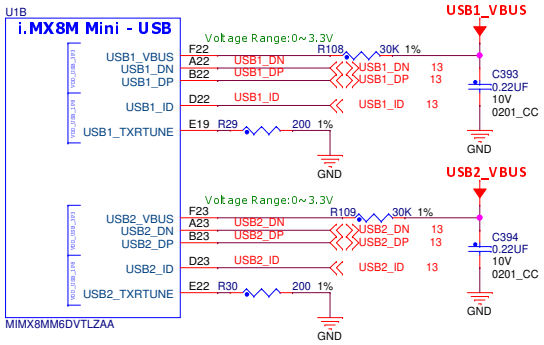


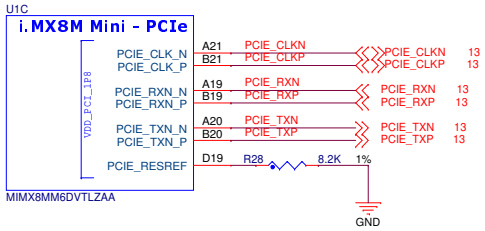


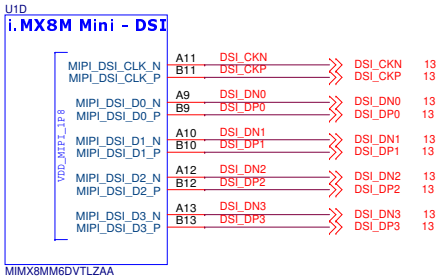


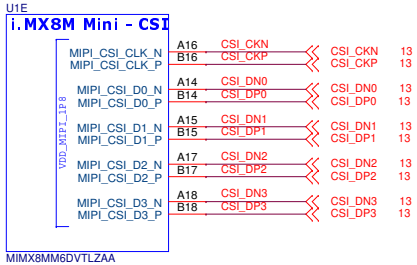
EMCRAFT SYSTEMS LLC 5821 Palmer Way, Suite A Carlsbad, CA 92010		
This document contains information proprietary to Emcraft and shall not be used for engineering design, procurement or manufacture in whole or in part without the express written permission of Emcraft Systems LLC.		
	ICAP Classification: CP: IUO: PUBL X	
Designer: <Designer>	Drawing Title: 8M LPDDR4 SOM	
Drawn by: <DrawnBy>	Page Title: IMX8M IO	
Approved: <Approver>	Size C / Document Number <Doc>	Rev 2A
	Date: Wednesday, June 24, 2020	Sheet 4 of 11

i.MX8M Mini PHYs









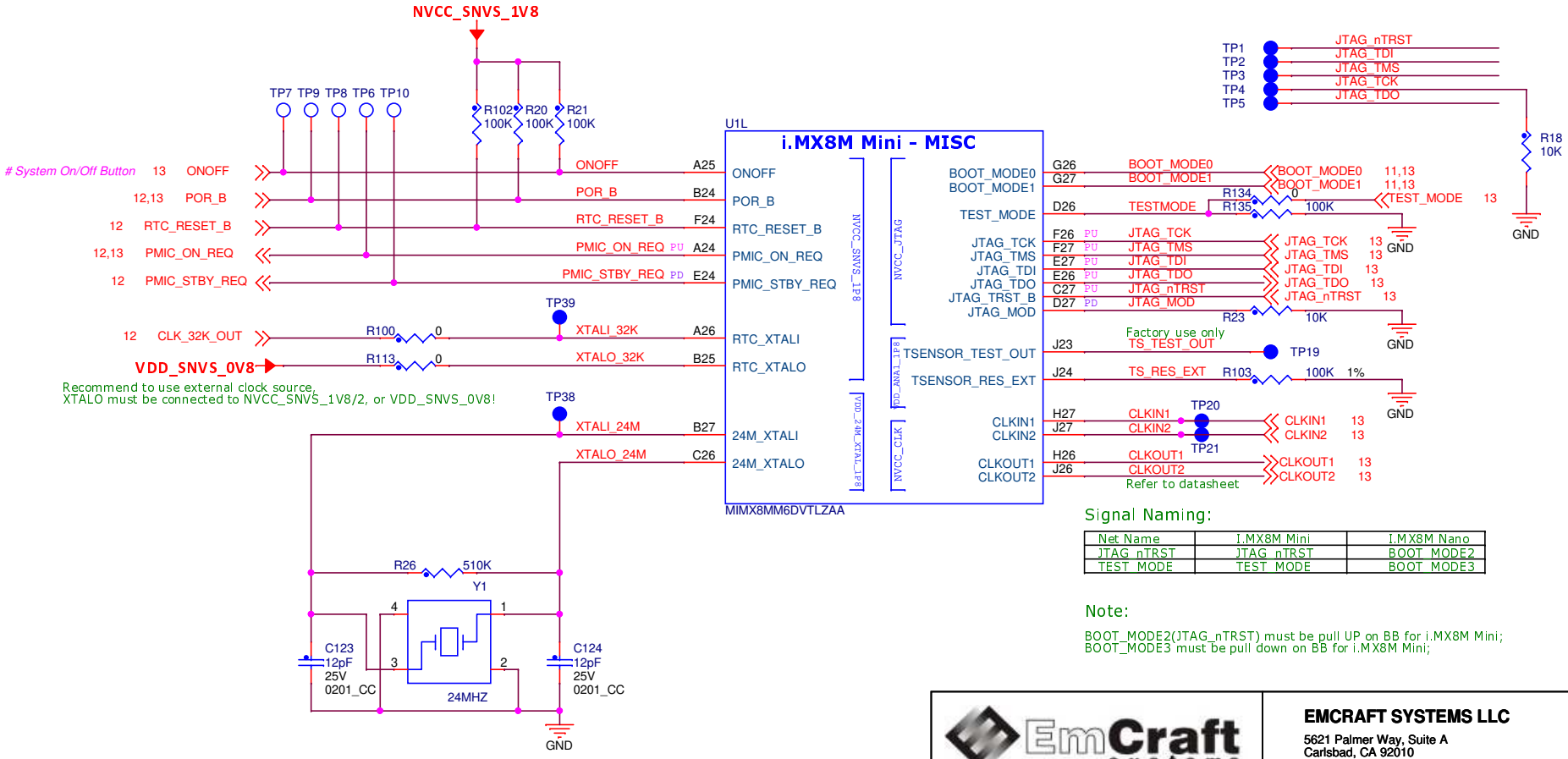
EMCRAFT SYSTEMS LLC
5621 Palmer Way, Suite A
Carlsbad, CA 92010

ICAP Classification: CP: IUO: PUBI: X

Designer: <Designer>	Drawing Title: 8M LPDDR4 SOM	
Drawn by: <DrawnBy>	Page Title: IMX8M PHY	
Approved: <Approver>	Size B / Document Number <Doc>	Rev 2A
	Date: Wednesday, June 24, 2020	Sheet 5 of 11

i.MX8M Mini MISC

JTAG Debug



Signal Naming:

Net Name	I.MX8M Mini	I.MX8M Nano
JTAG_nTRST	JTAG_nTRST	BOOT_MODE2
TEST_MODE	TEST_MODE	BOOT_MODE3

Note:

BOOT_MODE2(JTAG_nTRST) must be pull UP on BB for i.MX8M Mini;
BOOT_MODE3 must be pull down on BB for i.MX8M Mini;

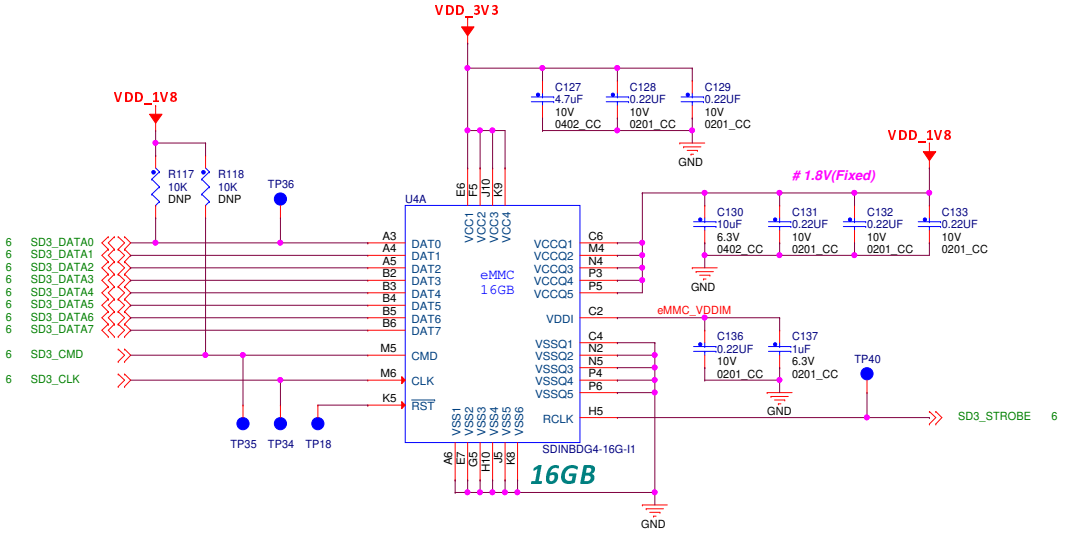
EMCRAFT SYSTEMS LLC
5621 Palmer Way, Suite A
Carlsbad, CA 92010

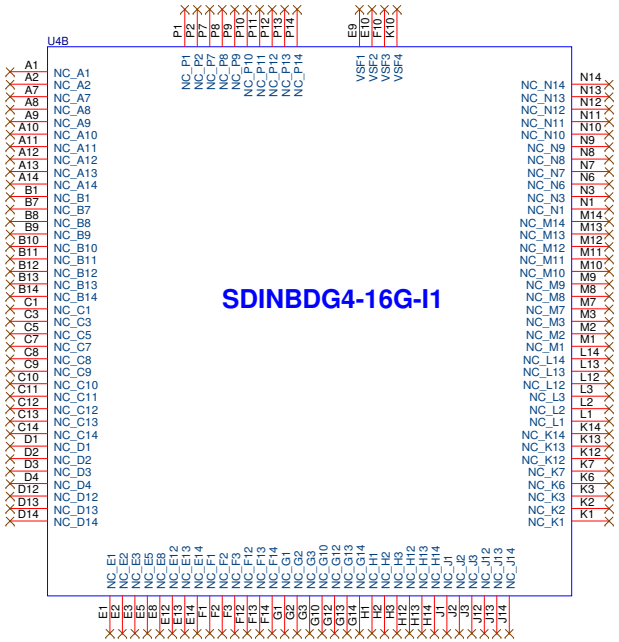
ICAP Classification: CP: ____ IUO: ____ PUBI: _X_

Designer: <Designer>	Drawing Title: 8M LPDDR4 SOM		
Drawn by: <DrawnBy>	Page Title: IMX8M MISC		
Approved: <Approver>	Size A4	Document Number <Doc>	Rev 2A
	Date: Wednesday, June 24, 2020	Sheet 6 of 11	

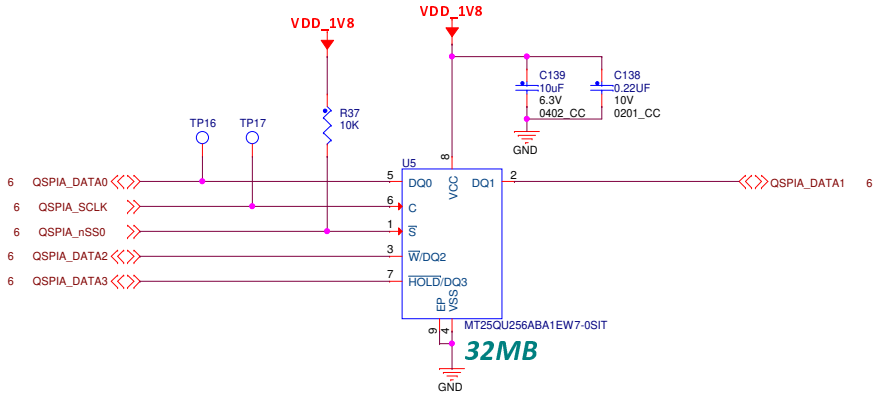
Storage

eMMC





QSPI Flash

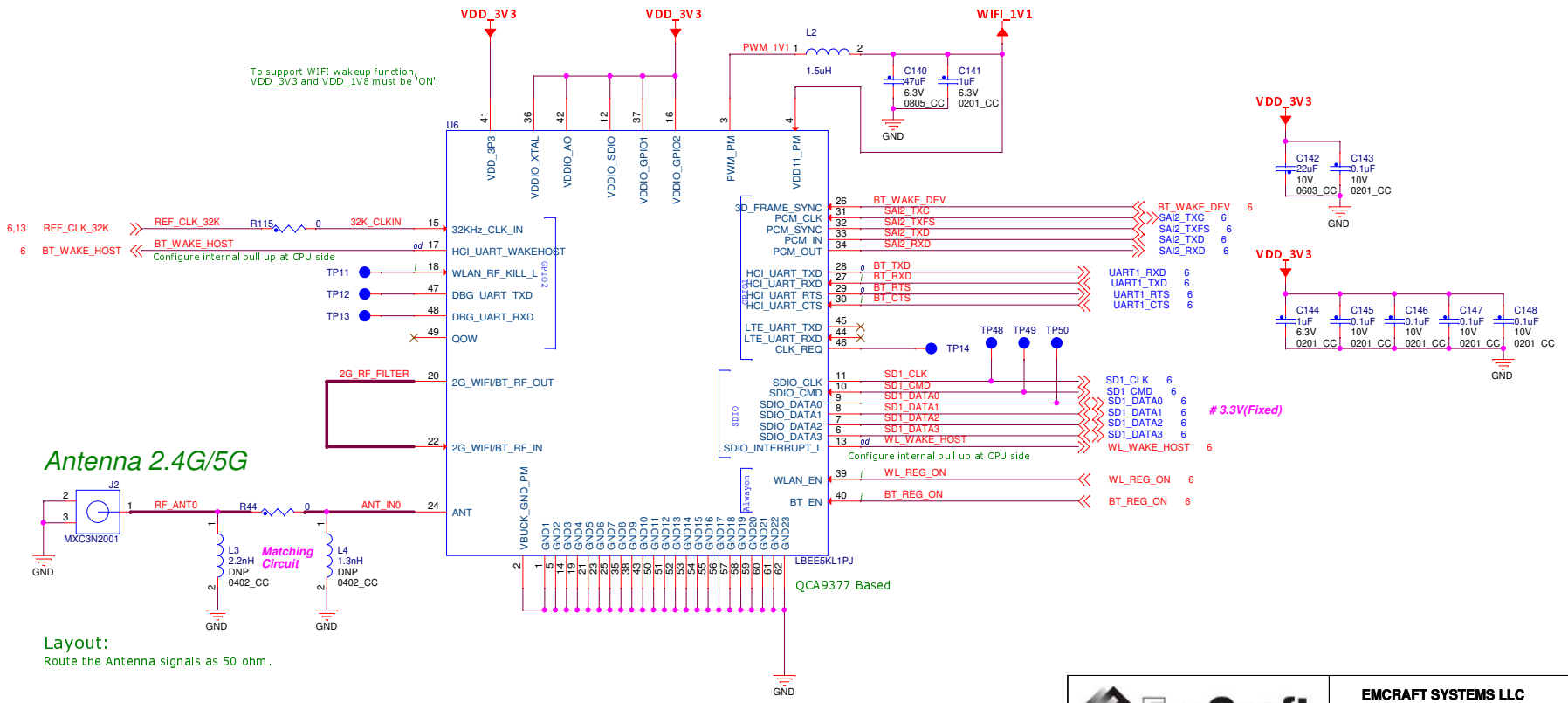


EMCRAFT SYSTEMS LLC
5621 Palmer Way, Suite A
Carlsbad, CA 92010

ICAP Classification: CP: IUO: PUBI: X

Designer: <Designer>	Drawing Title: 8M LPDDR4 SOM	
Drawn by: <DrawnBy>	Page Title: eMMC / qSPI	
Approved: <Approver>	Size: B	Document Number: <Doc> — Rev: 2A
	Date: Wednesday, June 24, 2020	Sheet 7 of 11

2.4G/5G WIFI/BT Module



Antenna 2.4G/5G

Layout:
Route the Antenna signals as 50 ohm.

Power Sequence

EmCraft systems	**EMCRAFT SYSTEMS LLC** 5621 Palmer Way, Suite A Carlsbad, CA 92010

ICAP Classification: CP: IUO: PUBI: X

Designer: <Designer>	Drawing Title: **8M LPDDR4 SOM**	
Drawn by: <DrawnBy>	Page Title: **WiFi a/b/g/n/ac & BT 5.0**	
Approved: <Approver>	Size B / Document Number <Doc>	Rev 2A
	Date: Wednesday, June 24, 2020	Sheet 8 of 11

Boot Mode and CFG Switch

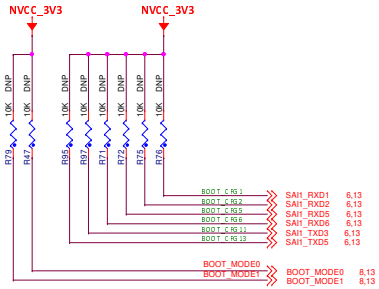
Caution:
IO internal pull up/down is not supported in 3.3V mode, must disable the internal pull up/down via software and use external pull up/down resistors instead.
All IO pin groups are impacted except for XTAL, DDR, PCI, USB and MIPI PHY IO's.
See Errata e50080 for detailed information.

i.MX8M Mini ROM Fuse

	Address	7	6	5	4	3	2	1	0
	0x470[15:8]	BOOT_CFG[15]	BOOT_CFG[14]	BOOT_CFG[13]	BOOT_CFG[12]	BOOT_CFG[11]	BOOT_CFG[10]	BOOT_CFG[9]	BOOT_CFG[8]
	0x470[15:8]	Infinit-Loop (Debug USE only) 0 - Disable 1 - Enable	001 - SD/eSD			Port Select: 00 - uSDHC1 01 - uSDHC2 10 - uSDHC3		Power Cycle Enable '0' - No power cycle '1' - Enabled via	SD Loopback Clock Source Sel (for SDR50 and SDR104 only) '0' - through SD pad '1' - direct
	0x470[15:8]		010 - MMC/eMMC						
	0x470[15:8]		011 - NAND			Pages In Block: 00 - 128 01 - 64 10 - 32 11 - 256		Nand_Row_address_bytes: 00 - 3 01 - 2 10 - 4 11 - 5	
	0x470[15:8]		100 - QSPI			Flash Auto Probe	FLASH_TYPE 000-Device supports 3B read by default 001-Device supports 4B read by default 010-HyperFlash 1V8 011-HyperFlash 3V3 100-MXIC Octal DDR		
	0x470[15:8]		110 - SPI NOR			Port Select: 000 - eCSPI1 001 - eCSPI2 010 - eCSPI3			SPI Addressing: 0 - 3-bytes (24-bit) 1 - 2-bytes (16-bit)
	0x470[15:8]	Others - Reserved for future use							
		BOOT_CFG[7]	BOOT_CFG[6]	BOOT_CFG[5]	BOOT_CFG[4]	BOOT_CFG[3]	BOOT_CFG[2]	BOOT_CFG[1]	BOOT_CFG[0]
SD/eSD	0x470[7:0]	Fast Boot: 0 - Regular 1 - Fast Boot	Reserved	Reserved	Bus Width: 0 - 1-bit 1 - 4-bit	Speed 000 - Normal/SDR12 001 - High/SDR25 010 - SDR50 011 - SDR104 101 - Reserved for DDR50 Others - Reserved			Reserved
MMC/eMMC	0x470[7:0]		Bus Width: 000 - 1-bit 001 - 4-bit 010 - 8-bit 101 - 4-bit DDR (MMC4.4) 110 - 8-bit DDR (MMC4.4) Else - reserved.			Speed 00 - Normal 01 - High 10 - Reserved for HS200 11 - Reserved		USDHC IO VOLTAGE SELECTION For Normal Boot Mode 0 - 3.3V 1 - 1.8V	USDHC IO VOLTAGE SELECTION For Manufacture Mode 0 - 3.3V 1 - 1.8V
NAND	0x470[7:0]	BT_TOGGLE MODE	BOOT_SEARCH_COUNT: 00 - 2 01 - 2 10 - 4 11 - 8		Toggle Mode 33MHz Preamble Delay, Read Latency: '000' - 16 GPMICLK cycles. '001' - 1 GPMICLK cycles. '010' - 2 GPMICLK cycles. '011' - 3 GPMICLK cycles. '100' - 4 GPMICLK cycles. '101' - 5 GPMICLK cycles. '110' - 6 GPMICLK cycles. '111' - 7 GPMICLK cycles. '1111' - 15 GPMICLK cycles.			Reserved
FlexSPI	0x470[7:0]	HOLD TIME: 00 - 500us 01 - 1ms 10 - 3ms 11 - 10ms		FLASH Auto Probe Type		FlexSPI FLASH Dummy Cycle			
SPINOR	0x470[7:0]	CS select SPI only: 00 - CS#0 default 01 - CS#1 10 - CS#2 11 - CS#3	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

BT_CFG Pins:

SAI1_RXD0	BOOT_CFG0
SAI1_RXD1	BOOT_CFG1
SAI1_RXD2	BOOT_CFG2
SAI1_RXD3	BOOT_CFG3
SAI1_RXD4	BOOT_CFG4
SAI1_RXD5	BOOT_CFG5
SAI1_RXD6	BOOT_CFG6
SAI1_RXD7	BOOT_CFG7
SAI1_RXD8	BOOT_CFG8
SAI1_RXD9	BOOT_CFG9
SAI1_RXD10	BOOT_CFG10
SAI1_RXD11	BOOT_CFG11
SAI1_RXD12	BOOT_CFG12
SAI1_RXD13	BOOT_CFG13
SAI1_RXD14	BOOT_CFG14
SAI1_RXD15	BOOT_CFG15



Note:

1. Bootcfg/SAI1 singals have internal PD before and after POR_B reset is deasserted!

2. Standalone SOM board can support eMMC/SDHC3 boot, by populating R71, R72, R75, R76, R79, R95, R97!

3. When using Base Board for Multi boot selection, you must keep the resistors DNP on SOM board!

Boot Mode

BOOT_MODE1	BOOT_MODE0

BOOT TYPE:

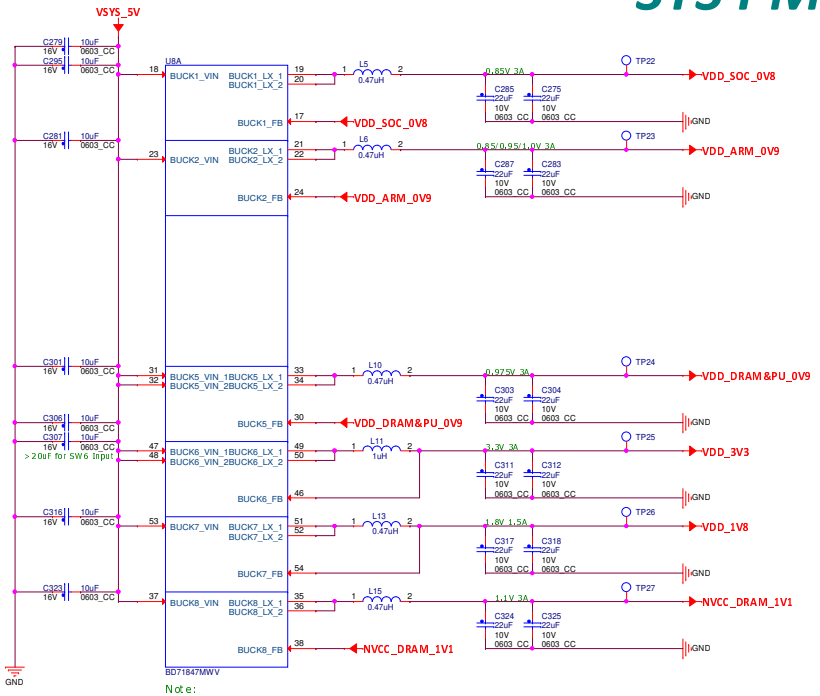
00 Boot From Fuses
01 Serial Downloader
10 Internal Boot (Development)
11 Reserved

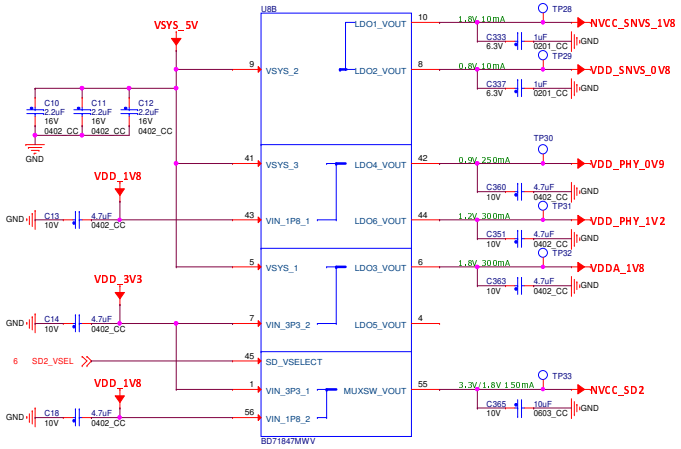
EMCRAFT SYSTEMS LLC
5621 Palmer Way, Suite A
Carlsbad, CA 92010

ICAP Classification: CP: IUO: PUBL X

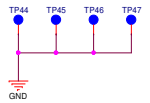
Designer: <Designer>	Drawing Title: 8M LPDDR4 SOM	
Drawn by: <DrawnBy>	Page Title: IMX8M BOOT	
Approved: <Approver>	Size C	Document Number <Doc> Rev 2A
	Date: Wednesday, June 24, 2020	Sheet 9 of 11

SYS PMIC



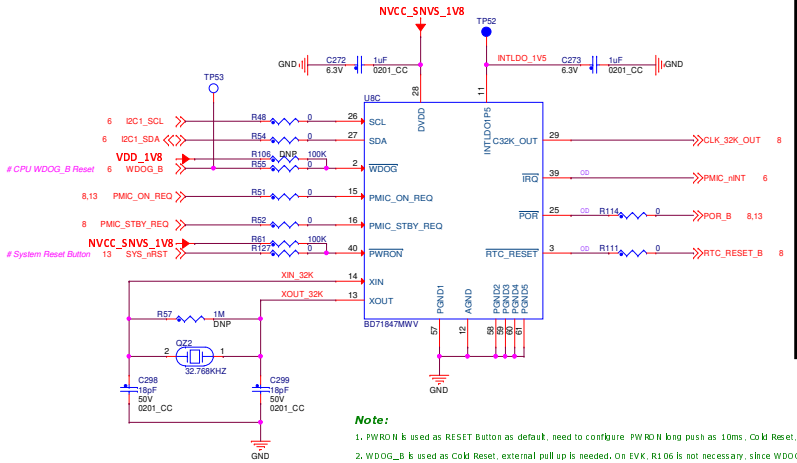


GND Testpoints



Note:

BUCK1 default output voltage is 0.8V. Software will change it to 0.85V in SPL before DDR initialization.
BUCK5 default output voltage is 0.9V. Software will change it to 0.975V(BD71847 BUCK5 doesn't support 0.95V output) in SPL before DDR initialization.
BUCK2 default output voltage is 0.9V. Software will change it to 0.85V for 1.2GHz operation, 0.95V for 1.6GHz, 1.0V for 1.8GHz.



Note:

1. PWRON is used as RESET Button as default, need to configure PWRON long push as 10ms, Cold Reset, and short push detect should be disabled !
2. WDOG_B is used as Cold Reset, external pull up is needed. On EVK, R106 is not necessary, since WDOG_B/GPIO1_IO02 of CPU has internal pull up.

i.MX8M Mini LPDDR4 EVK Power Sequence

SEQ	PWR/Signal	REG	MIN	TYP	MAX	Max Current(mA)
1	NVCC_SNVS_1V8	LDO1	1.62	1.8	1.98	10
2	VDD_SNVS_0V8	LDO2	0.76	0.8	0.9	10
3	RTC_RESET_B	RTC_RESET_B	--	--	--	--
4	CLK_32K_OUT	RTC_CLK	--	--	--	--
5	VDD_SOC_0V8	BUCK1	0.78/0.805	0.82/0.85	0.9	3000
6	VDD_DRAM&PU_0V9	BUCK5	0.805/0.855	0.85/0.95	0.9/1.0	3000
6	VDD_PHY_0V9	LDO4	0.855	0.9	1.0	250
7	VDD_ARM_0V9	BUCK2	0.805/0.9/0.95	0.85/0.95/1.0	0.95/1.0/1.05	3000
7	VDDA_1V8	LDO3	1.71	1.8	1.89	300
8	VDD_1V8/NVCC_1V8	BUCK7	1.65	1.8	1.95	1500
9	NVCC_DRAM_1V1	BUCK8	1.06	1.1	1.14	3000
10	VDD_3V3/NVCC_3V3	BUCK6	3	3.3	3.6	3000
10	NVCC_SD2	MUXSW	3.0/1.65	3.3/1.8	3.6/1.95	150
11	VDD_PHY_1V2	LDO6	1.14	1.2	1.26	300
12	POR_B	POR_B	--	--	--	--

EMCRAFT SYSTEMS LLC
5621 Palmer Way, Suite A
Carlsbad, CA 92010

ICAP Classification: CP: IUO: PUBL X

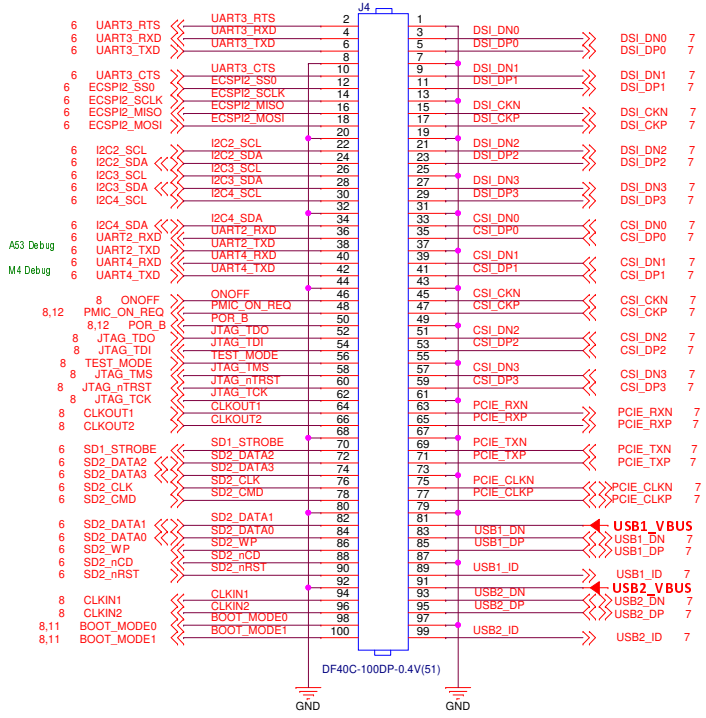
Designer: <Designer>	Drawing Title: 8M LPDDR4 SOM	
Drawn by: <DrawnBy>	Page Title: ROHM PMIC	
Approved: <Approver>	Size C	Document Number <Doc> Rev 2A
	Date: Wednesday, June 24, 2020	Sheet 10 of 11

B2B Connector for CPU Board

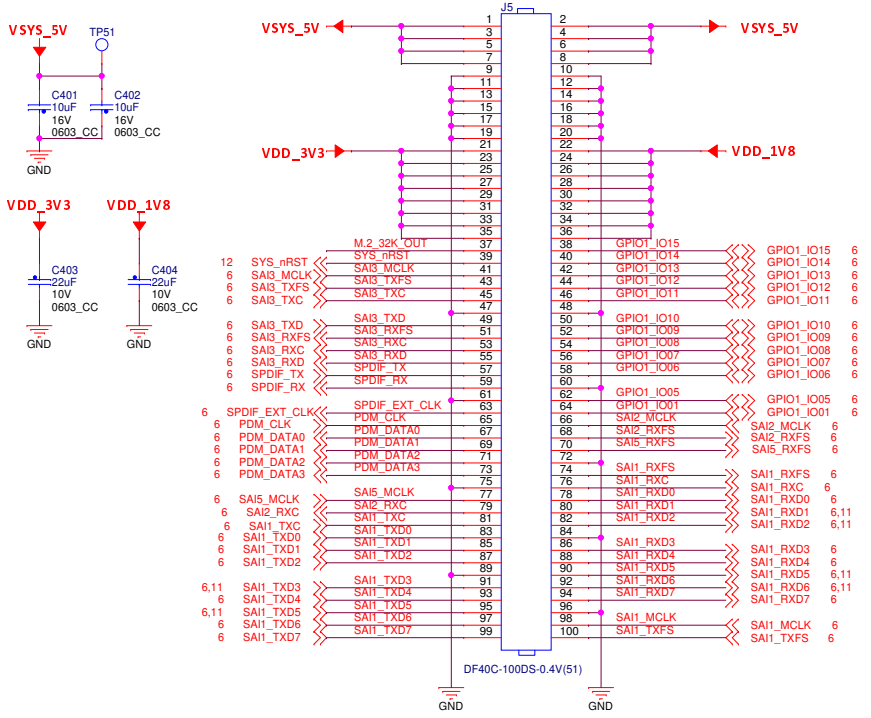
Caution:

IO internal pull up/down is not supported in 3.3V mode, must disable the internal pull up/down via software and use external pull up/down resistors instead.
All IO pin groups are impacted except for XTAL, DDR, PCI, USB and MIPI PHY IO's.
See Errata e50080 for detailed information.

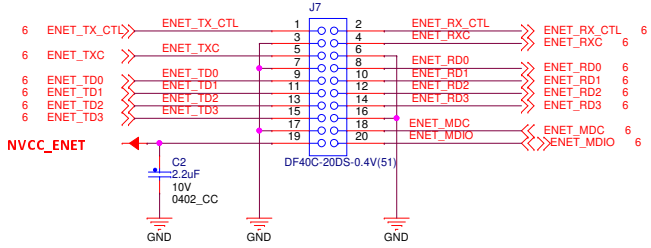
Header

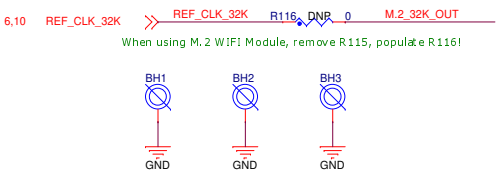


Receptacle



Receptacle





EMCRAFT SYSTEMS LLC
5621 Palmer Way, Suite A
Carlsbad, CA 92010

ICAP Classification: CP: IUO: PUBI: X

Designer: <Designer>	Drawing Title: 8M LPDDR4 SOM		
Drawn by: <DrawnBy>	Page Title: SOM Connectors		
Approved: <Approver>	Size B	Document Number <Doc>	Rev 2A
	Date: Wednesday, June 24, 2020	Sheet 11 of 11	