Computer Science 605.611

Problem Set 11

1. The read access delay for an I/O system is defined as the time required for the device to receive and process an I/O request, acquire the requested data and prepare to start transmitting the data. The data transfer rate for an I/O device is defined as the number of bytes per second that it can transmit once the requested data has been acquired.
The read access delay and data transfer rate for two different I/O systems A and B are given the table below:

I/O System	Read access delay	Data transfer rate
A	5 seconds	5120 bytes/sec
B	3 seconds	3072 bytes/sec

Both systems employ an 8-bit bus to transfer I/O data. Each system is used to transfer a series of data blocks each of which contains 15360 data bytes. The read access and data transfer for each block occur sequentially. What is the minimum time between consecutive interrupts on:

a) (3) System A that employs a DMA controller? Minimum time = 8s

Interrupts only occur at the end of transmission, thus
5s + 15360 / 5120 = 8s

b) (3) System B which, once the data has been acquired, employs interrupt driven I/O using a single I/O port to transfer the data one byte at a time?
Minimum time = .0003255s

Interrupts occur every time a byte is transferred, and 3072 bytes are transferred per second. Thus 1/3073 = .0003255s

2. A certain processor consumes 1000 cycles to perform the context switch required to transfer control to the interrupt handler for an I/O device that triggers an interrupt. The interrupt handler takes an additional 10,000 cycles to service the device request. Once the device has been serviced, another 1000 cycles are required to perform the context switch needed to return from the interrupt handler back to the program that was running. The processor's clock rate is 3 GHz.

a) (5) What is the maximum number of requests per second that a device can generate if the system must complete all activity associated with one interrupt before the next interrupt occurs?

1000 + 10000 + 1000 = 12,000 cycles per requests
3GHz = 3 * 10 ^ 9 cycles/second
3 * 10 ^ 9 / 12,000 = 250,000 requests/s

(over)

b) (5) The registers used in managing exceptions and interrupts on our MIPS processor are described in the sub-module "2.2 Interrupt Driven Input/Output" as well as in section A.7 of the textbook.
Write down a short sequence of MIPS assembly language instructions to place just the current exception code right justified into CPU register $t0.

```
# cause register is register $13 on exception coprocessor
# exception code is stored in bits 2-6 in the cause register

mfc $t0, $13          # move cause register to $t0
sll $t0, $t0, 25      # drop leftmost 25 bits
srl, $t0, $t0, 27     # drop rightmost 2 bits and right-justify exception code
```

3. (5) A disk rotates at a rate of 7200 revolutions per minute. Seek operations (i.e., moving the access head to a desired track) take on average 20 milli-seconds. Once the access head is on the appropriate track, it takes an average of one half revolution of the disk to get to the beginning of a requested sector. Each track contains 128 sectors and each sector contains 512 bytes of data. How long on average does it take to get the access head to the beginning of a randomly selected sector on a randomly selected track? Express your answer in micro-seconds (not seconds or milli-seconds).

20 milli-seconds = 20000 micro-seconds

$$\frac{1\ minute}{7200\ revs} * \frac{60\ s}{1\ minute} * \frac{.5\ avg\ rev}{beg.sector} = .0041667 \frac{s}{beg.sector}$$
$$= 4166.7\ micro - seconds$$

20000 + 4166.7 = 24166.7 micro-seconds

4. Assume that the 4 data strips (also called data blocks) within a certain stripe on a RAID 5 system are designated B0, B1, B2 and B3. The corresponding parity block P_{old} for this stripe is computed as the cumulative XOR of the 4 data strips within the stripe: P_{old} =B0 ^ B1 ^ B2 ^ B3. Hence each stripe contains a parity block and 4 data blocks. Block B2 is to be overwritten with the new contents designated as $B2_{new}$. None of the parity or data on the disk is currently known or in memory.

a) (5) Write down an expression for the corresponding new parity block P_{new} that requires reading no more than two blocks of any type from the 5 blocks in the stripe.

P_{old} =B0 ^ B1 ^ $B2_{old}$ ^ B3
P_{old} ^ $B2_{old}$ =B0 ^ B1 ^ $B2_{old}$ ^ $B2_{old}$ ^ B3
P_{old} ^ $B2_{old}$ = B0 ^ B1 ^ B3
P_{new} = B0 ^ B1 ^ $B2_{new}$ ^ B3
P_{new} = $B2_{new}$ ^ P_{old} ^ $B2_{old}$
(reading only from stripes P and B2)

b) (5) Write down a different alternate expression for the new parity block P_{new} if there are no restrictions on the number or type of blocks read from the stripe.

P_{new} = B0 ^ B1 ^ $B2_{new}$ ^ B3

5. (10) A disk system is to be constructed using some number of identical disk drives each of which holds 16 terabytes of data. A large database of size 96 terabytes is to be stored on the disk system. What is the minimum number of disks (data disks plus parity disks) that are required for the system if the disk system is a:

96 terabytes / 16 terabytes = 6 disks

a) RAID6 system?

RAID6 provides dual-redundancy, thus needs 6 + 2 = 8 disks

b) RAID5 system?

RAID5 provides one redundant disk, thus needs 6 + 1 = 7 disks

c) RAID4 system?

RAID4 provided one redundant disk, thus needs 6 + 1 = 7 disks

d) RAID1 system?

RAID1 provides redundancy by duplicating each data disk, thus needs 6 * 2 = 12 disks

e) RAID0 system?

RAID0 provides no redundancy, thus would need just 6 disks

6. Sixty percent of the time required to complete a program on a certain computer system corresponds to the execution of code not related to I/O. The remaining 40% of the time required is due to I/O operations. The total time required to complete the entire workload is 480 seconds. This total time is to be reduced by 160 seconds by either improving CPU speed or by improving I/O.

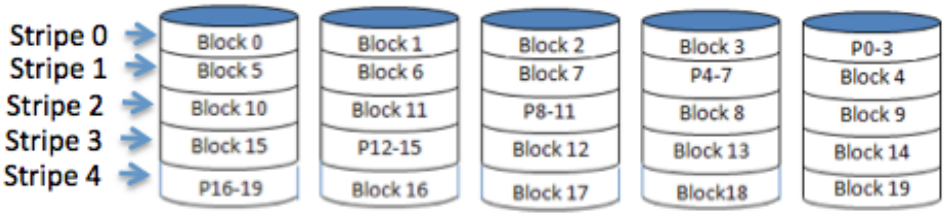
a) (5) If the CPU is made N times as fast as the original CPU, what value of N yields the desired 160-second reduction in the total time consumed by the program? N = 2.25 Express your answer to two decimal places (dddd.dd).

480 total seconds
60% of 480 = 288s not related to I/O
speedup = 288 / (288-160) = 2.25

b) (5) If instead of making the CPU faster, the I/O is made M times as fast as the original I/O, what value of M yields the desired 160-second reduction in the total time consumed by the program? M= 6.00. Express your answer to two decimal places (dddd.dd).

480 total seconds
40% of 480 = 192s related to I/O
speedup = 192 / (192-160) = 6.00

7. Shown below is the diagram of a RAID system.



None of the information contained on the disks is currently in memory.

a) (5) What is the minimum number of disk blocks of any type that must be read to determine whether there is an error in some block within stripe 1?

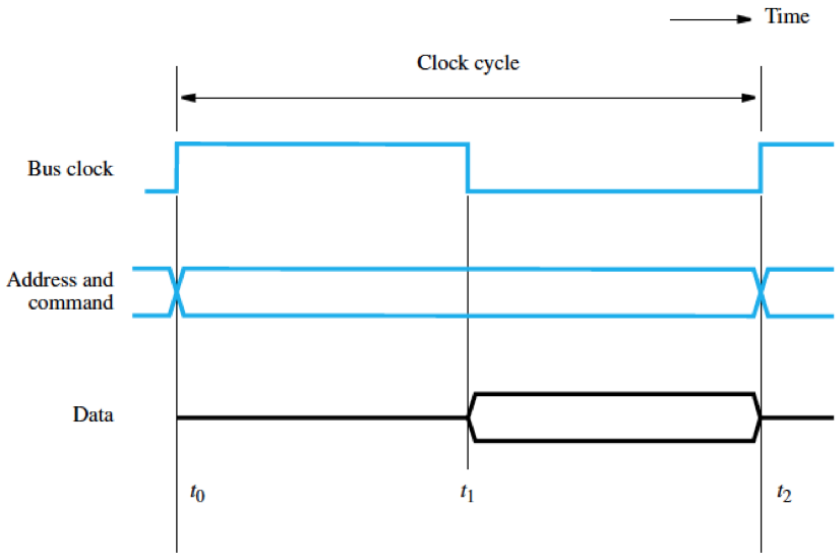
5 – to check if there is an error in stripe 1 one must check if:
block4 ^ block5 ^ block6 ^ block7 = P4-7

b) (9) Block 2 within stripe 0 is to be updated and overwritten, while minimizing the number of blocks that are read and the number of blocks that are written. List the disk blocks of any type that must be read and those that must be written to accomplish this. For example: Block6, Block12, P15-16, etc.

Similar to problem 4a, given the data to be written in memory we only must read $Block2_{old}$ and $P0\text{-}3_{old}$ and write $Block2_{new}$ and $P0\text{-}3_{new}$. After reading $Block2_{old}$ and $P0\text{-}3_{old}$ we can write $P0\text{-}3_{new}$ as
$P0\text{-}3_{new} = Block2_{new} \wedge P0\text{-}3_{old} \wedge Block2_{old}$
and then $Block2 = Block2_{new}$.

Thus
Read: Block2 and P0-3
Write: Block2 and P0-3

8. (10) Shown below is a copy of the simplified timing diagram from module 10 for a read operation over a synchronous bus.



Assume that zero wait states are required and that the bus clock has a 50% duty cycle; a 50% duty cycle means that the high and the low phases of the clock are of equal duration. The bus master takes 1.5 ns to place an address on the address lines. Once a slave device receives an address, it requires 3 ns to decode the address and a maximum of 5 ns to place the requested data on the data lines. The maximum propagation delay (the time required for information to pass from one device to another) on the data lines of the bus is 4 ns. Once the data arrives at the requesting device, it takes 1ns to transfer the data from

the bus into the device's data register. What is the maximum bus clock rate that can be used with this system?

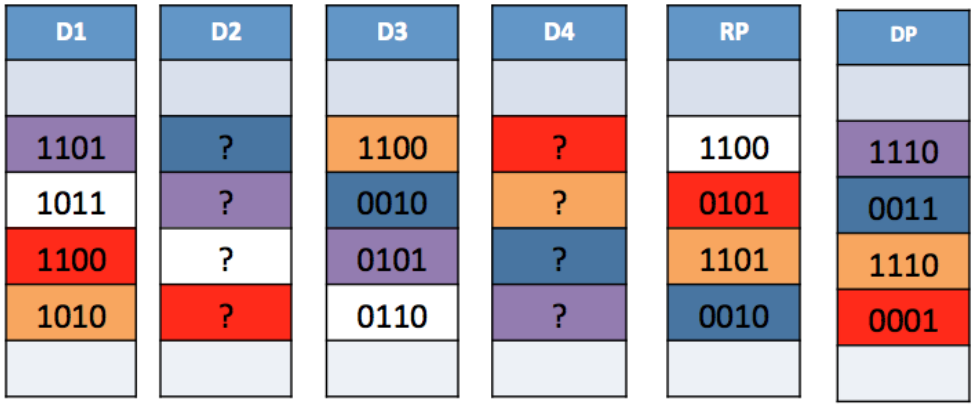
t0-t1 (put data on data lines)	t1-t2
1.5 ns – place address on address lines	5 ns – place data on data lines
3 ns – decode address	4 ns – propagation delay
	1 ns – bus to data register

t1-t2 is the longer cycle, thus is the limiting cycle.
t1-t2 takes 10 ns, thus one cycle must be a total of 20 ns.
clock rate = 1 / cycle time = 1 / (20 * 10 ^-9) = 0.05 * 10 ^ 9 Hz or 0.05 GHz

9. (16) Shown below is a RAID-DP (i.e., RAID6 with dual parity) disk system. D1, D2, D3 and D4 are the data disks. RP is the horizontal or row parity disk and DP is the diagonal parity disk. For the purposes of this problem, each strip or block on a disk is a 4-bit pattern. Two of the disks, D2 and D4 have crashed so their data contents are unknown.
Module 10 example set 7 illustrates a technique to reconstruct blocks on up to 2 disks that have failed and are unavailable. Use the scheme described in the example set, substituting exclusive-OR in place of addition, to reconstruct the contents of the two missing disks by determining the 4-bit pattern for each of the following:

D2_blue =	0100	D4_red=	1001
D2_purple=	1001	D4_orange=	0101
D2_white=	0011	D4_blue=	0111
D2_red=	0001	D4_purple=	1111

List your answers in the order shown above.
Orange DP -> 1010 ^ 1100 ^ 1101 ^ 1110 = D4_orange = 0101
RP row 2 -> 1011 ^ 0010 ^ 0101 ^ 0101 = D2_purple = 1001
Purple DP -> 1101 ^ 1001 ^ 0101 ^ 1110 = D4_purple = 1111
RP row 4 -> 1010 ^ 0110 ^ 1111 ^ 0010 = D2_red = 0001
Red DP -> 1100 ^ 0001 ^ 0101 ^ 0001 = D4_red = 1001
RP row 1-> 1101 ^ 1100 ^ 1001 ^ 1100 = D2_blue = 0100
Blue DP -> 0100 ^ 0010 ^ 0010 ^ 0011 = D4_blue = 0111
RP row 3 -> 1100 ^ 0101 ^ 0111 ^ 1101 = D2_white = 0011



10. Shown below is a bus system with a central arbiter that handles four devices. The device priorities range from highest for Device 4 down to the lowest for Device 1. The arbiter grants access to the highest priority request that is present. Each device has a separate request and grant line. The total available bus bandwidth that must be shared by the devices is 80 MB/s. Each device wants to use 30MB/s of bus bandwidth. All of the devices continuously compete for use of the bus and transmit blocks of the same size for each transaction. If a device is not granted access to the bus, it tries again as soon as the bus is not busy and keeps trying until it gets access. How much bus bandwidth is Device 1 able to use and how much bus bandwidth is Device 3 be able to use if:

a) (5) Bus access is granted strictly on a priority basis?

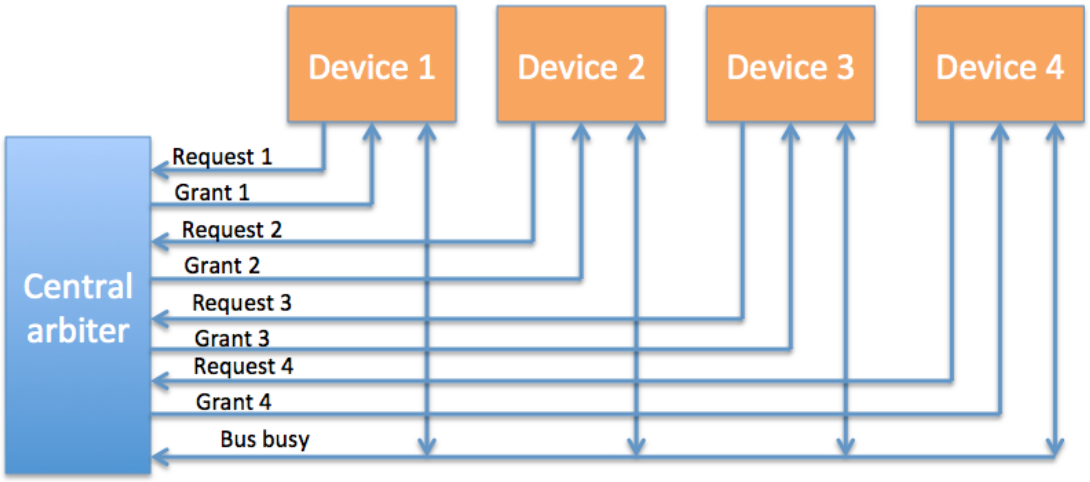
On a strictly priority basis, device 4 will always use 30 MB/s of bandwidth, as will device 3. Since there is only 20 MB/s of bandwidth remaining, device 2 uses 20 MB/s, and device 1 gets no bandwidth. Device 1 receiving no bandwidth is often referred to as starvation.

Device 1 bandwidth = 0 MB/s Device 3 bandwidth = 30 MB/s

b) (4) Instead of strict priority, the bus arbiter uses a fairness policy to give each device an equal chance to use the bus?

Since each device gets a fair chance to use the bus, each device splits the 80 MB/s bandwidth 4 ways, resulting in all devices using 20 MB/s of bandwidth.

Device 1 bandwidth = 20 MB/s Device 3 bandwidth = 20 MB/s


Device 1
Device 2
Device 3
Device 4
Central arbiter
Request 1
Grant 1
Request 2
Grant 2
Request 3
Grant 3
Request 4
Grant 4
Bus busy