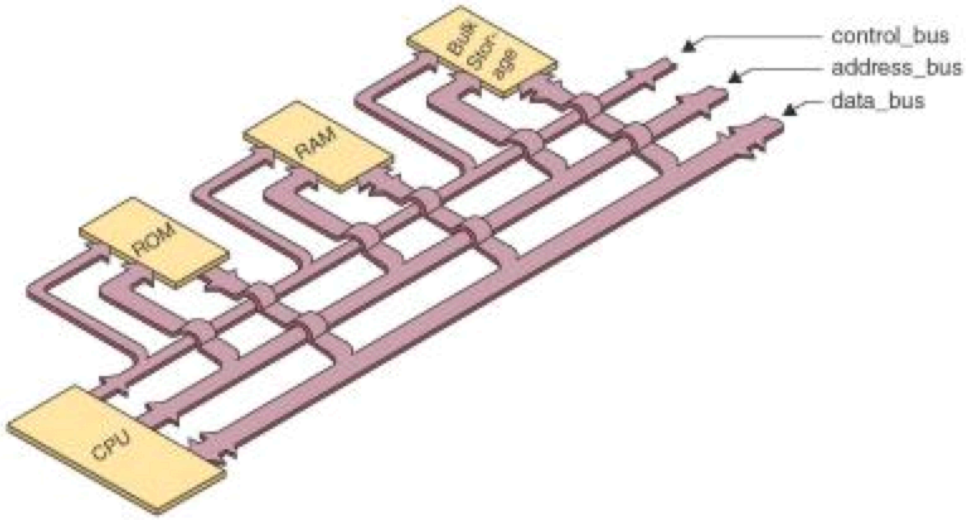
Memory Organization

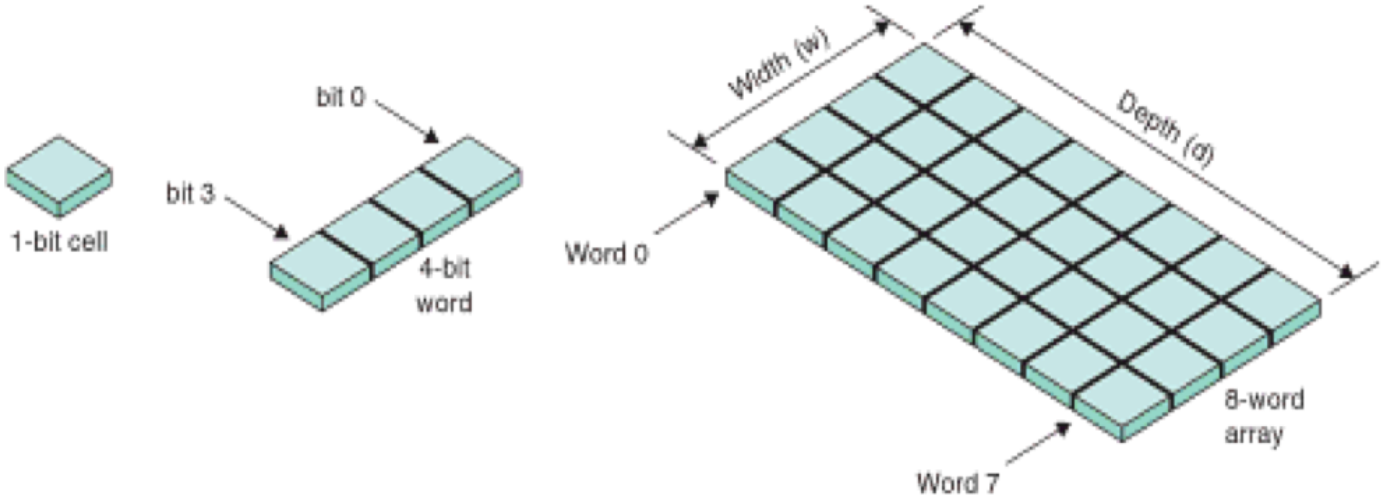
- The CPU obtains instructions and data from memory
  - Sends address over address bus
  - Sends or receives data over data bus
  - Sends read/write and other control signals over control bus



- A bus is a set of wires or electrical traces

Memory Organization

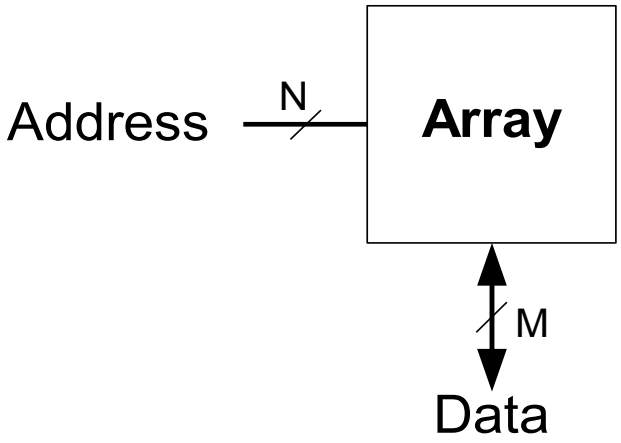
- A memory word is a group of 1-bit storage cells
- Each word has a unique address (from 0 up to some maximum)



- Number of bits per word defines its width
- Number of words in memory device defines its depth or height

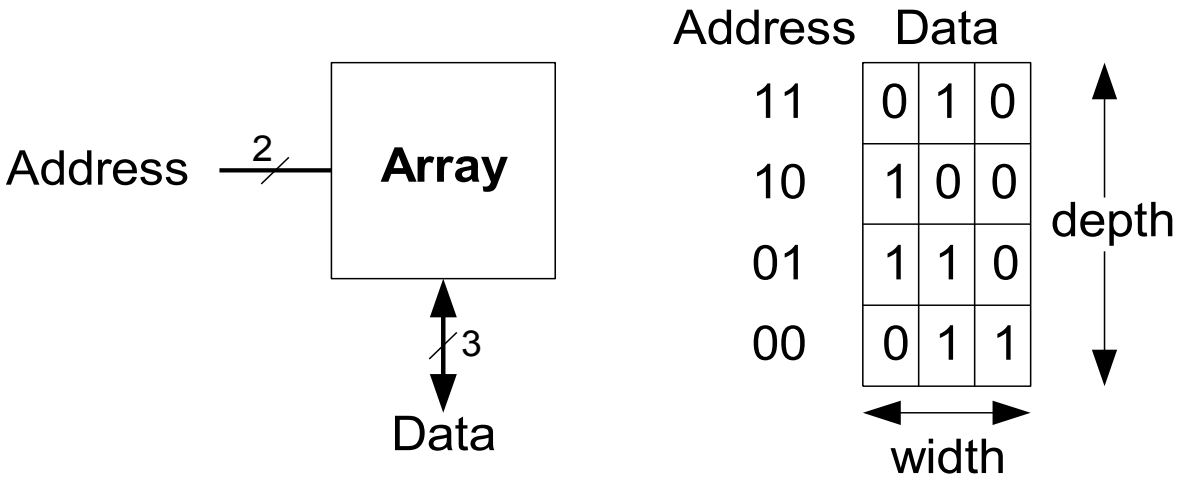
Memory Array

- The previous diagram shows a memory array
- The array contains 3-bit rows (words)
- In general, the array size = $2^N \times M$
  - N is the number of bits in the address
  - M is the number of bits per word



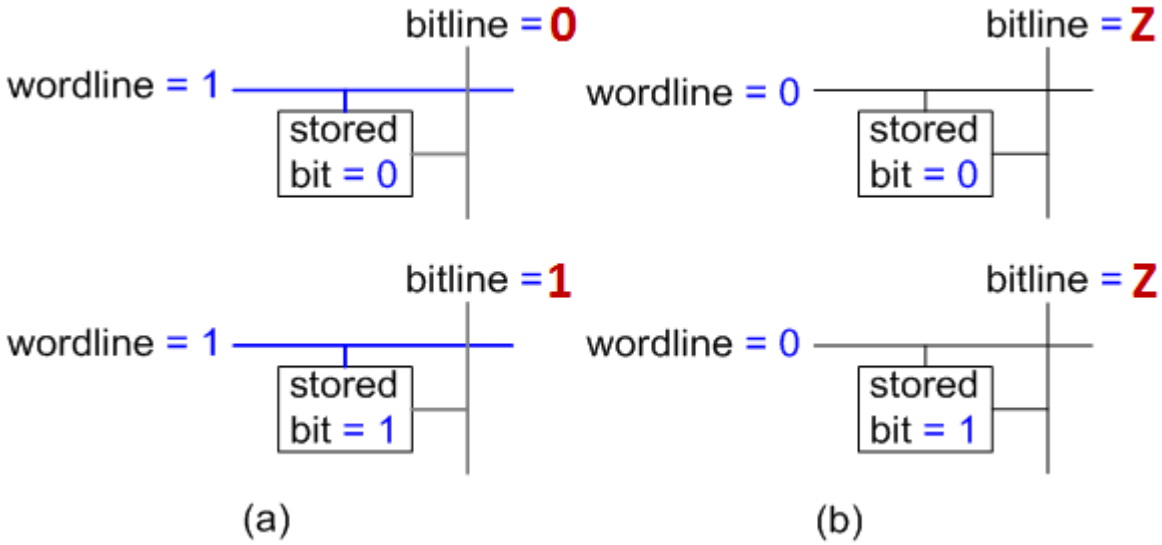
Memory Array Example

- $2^2 \times 3$-bit array
- Number of words: 4
- Word size: 3-bits
- For example, the 3-bit word stored at address 10 is 100

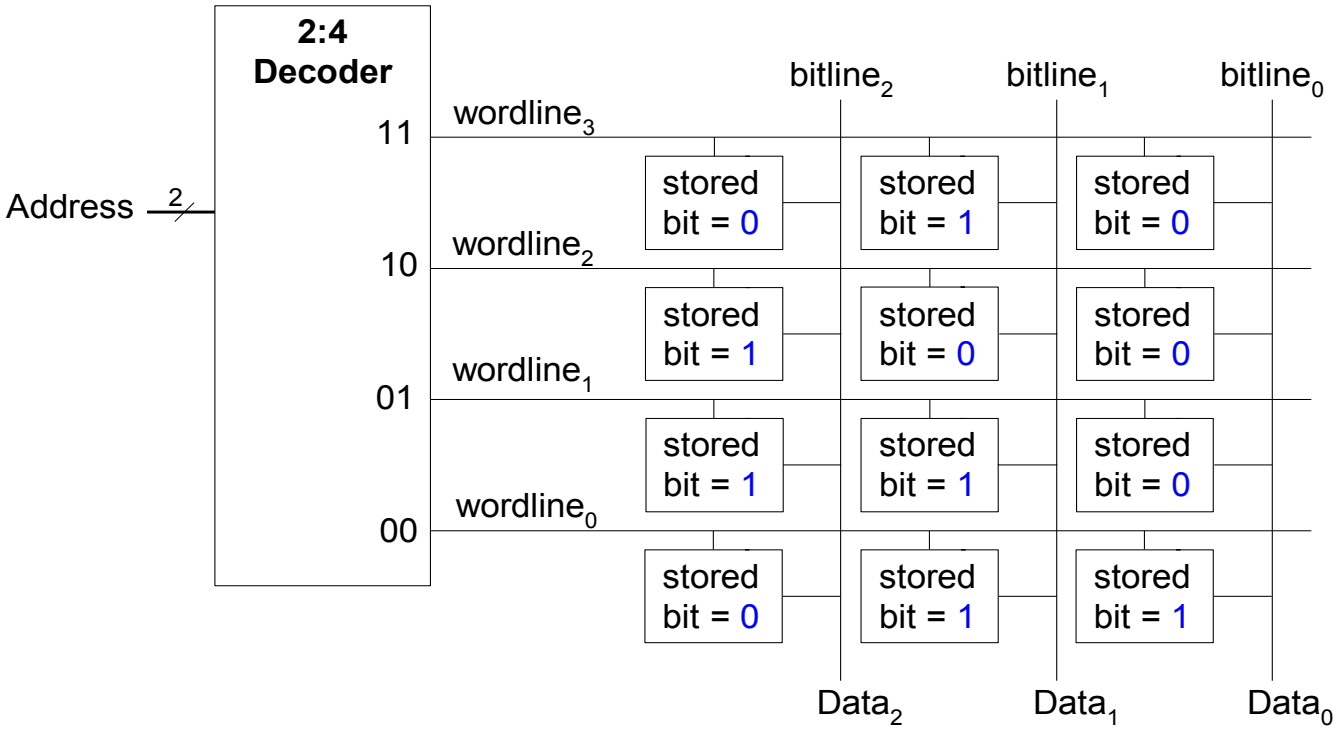


Memory Array Bit Cells

Wordline selects all bit cells within the specified word
Stored bit is transferred to or from bitline if wordline=1
Bits cells disconnected from bitline if wordline=0
Z represents the disconnected state

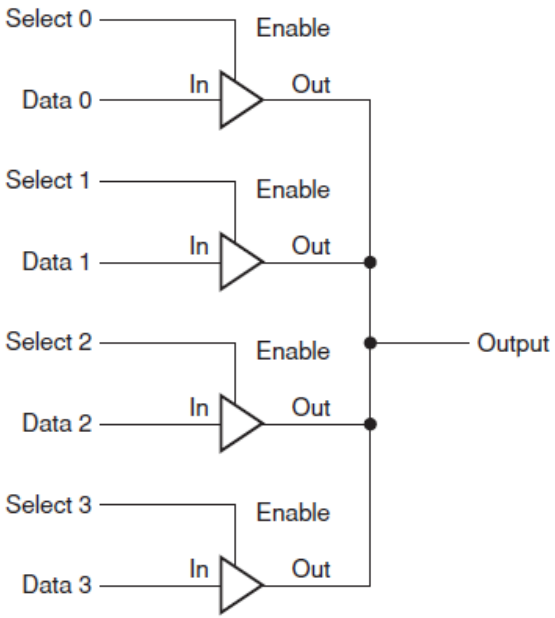


- **Wordline:**
  - like an enable
  - single row in memory array read/written
  - corresponds to unique address
  - only one wordline HIGH at once



Tri-State Buffers

The unselected words are detached from the bitlines



When enabled the tri-state buffer passes the data input through
When disabled, the tri-state buffer has a high impedence output
The output is thus disconnected from the bitline