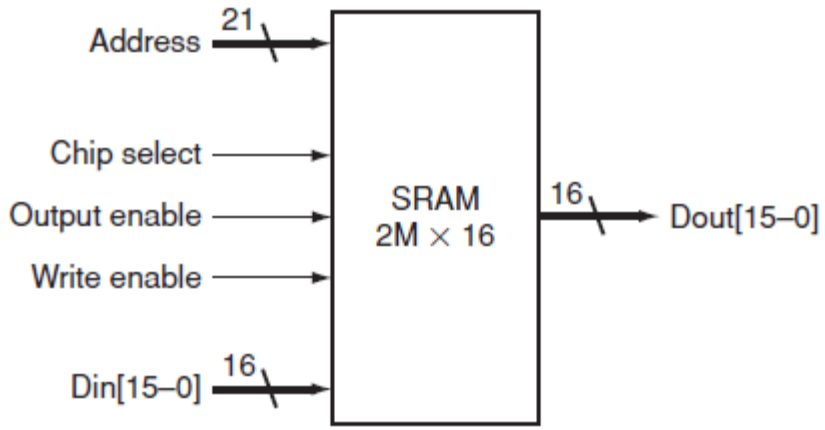
Larger Memories

- Each memory array is contained in a separate chip
- Multiple chips are grouped to provide the desired memory size
- Chip select signals determine which chip to access
- The read/write enables determine the direction of data transfer
- The address determines which word or row to access
- Write data goes through data-in port
- Read data is copied out through data-out port
- Each chip performs only one read or write at a time

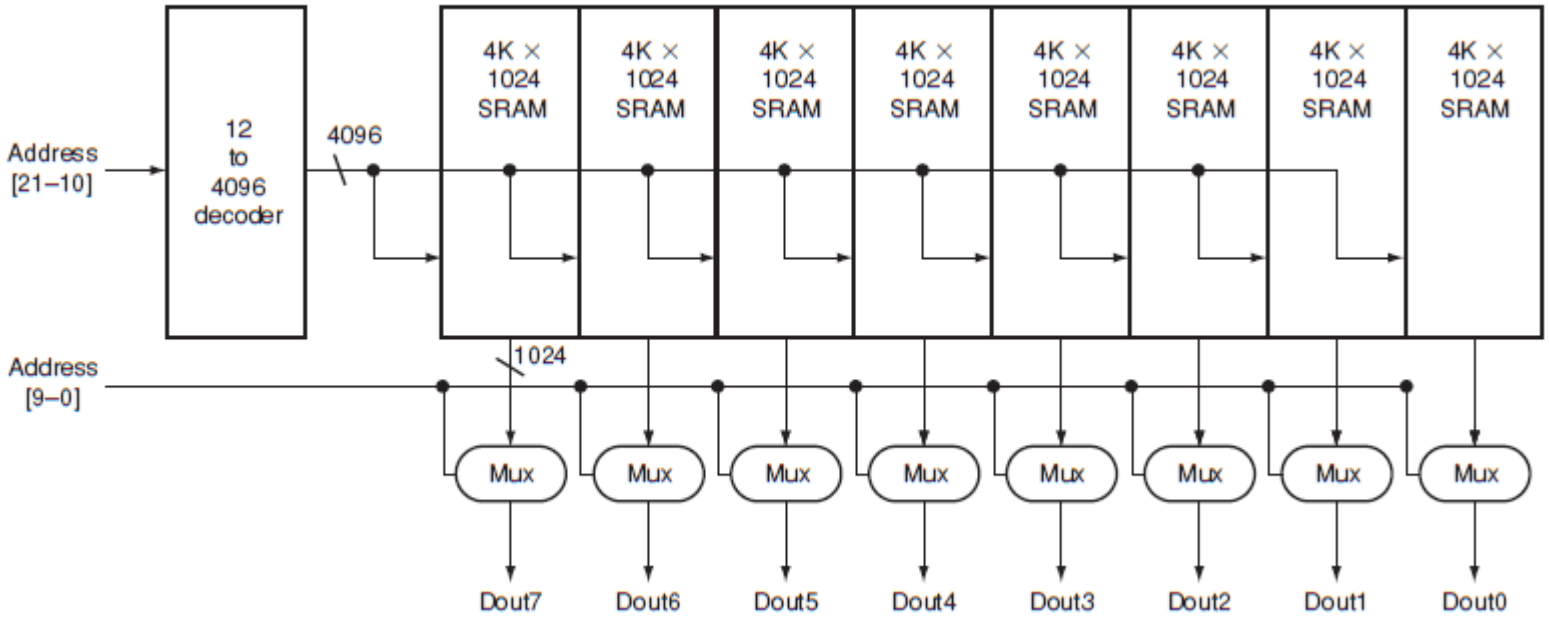
SRAM Example



- 2M (2^{21}) words, each 16 bits (2 bytes) wide
- Total size = 2097152*2 = 4194304 bytes
- A decoder could map the address onto the proper wordline

SRAM Example

- A 21-to-2097152 address decoder is needed in the previous case
- A more practical approach uses a 2-step decoding scheme



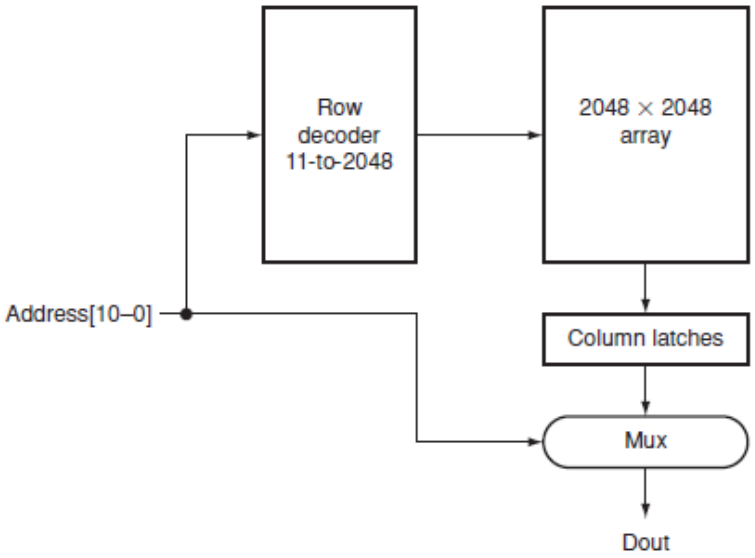
- 12-to-4096 decoder selects same row in every array
- 1024-to-1 Mux selects bit from each of the columns

DRAM Arrays

- DRAMs use a two-level decoding scheme to save on cost
- Same lines carry the row address and later the column address
- Row address determines which wordline is asserted
- Column address selects the data from the column latches
- Uses Row address (RAS) and Column address (CAS) strobes
- Refresh reads columns into latches and rewrites same values
- Entire row is refreshed in one cycle
- Memory controller handles refresh independently of CPU

DRAM Example

4M x 1 DRAM



11-bit row address selects one of 2048 rows (RAS)
Entire 2048-bit wide row is read into column latches
11-bit column address then selects one of 2048 latches (CAS)

Synchronous RAM

SDRAM and SSRAM transfer data in bursts

Burst is defined by starting address and a length

A clock is used to transfer successive bits in the burst

Multiple transfers occur without having to update the address

Significantly improves the rate of data transfer

SDRAM is the most popular choice for central memory

Other DRAM Types

DDRAM stands for double data rate RAMs (DDR)

DDRAM transfers data on both the rising and falling clock edge

DDR was standardize in 2000 and ran at 100 to 200 MHz

Later standards use increasingly higher speeds (≥ 1 GHz)

DDR2, DDR3 and DDR4