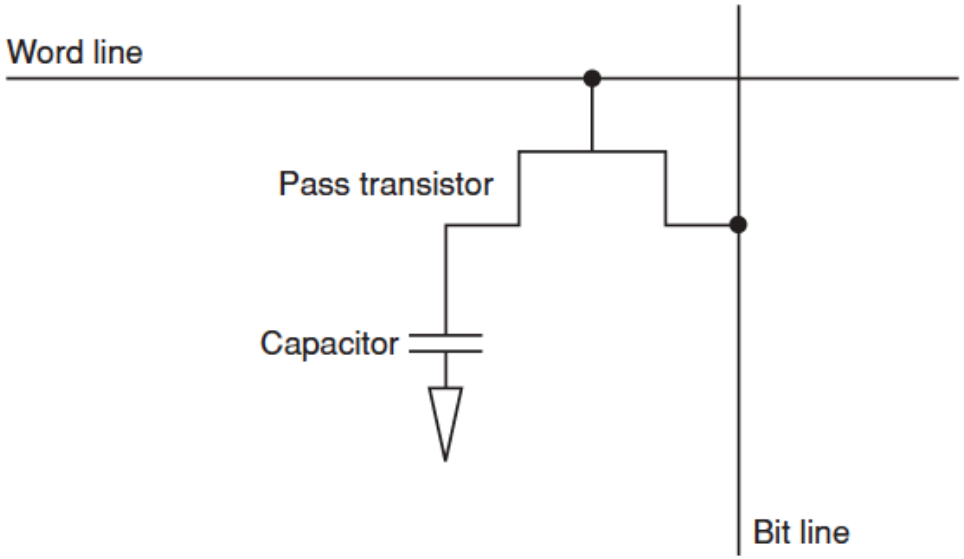
DRAM

With dynamic RAM, the bit is stored as charge on a capacitor
A transistor switch allows the bit to be read or written



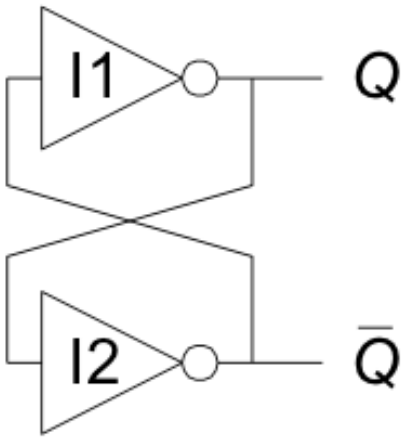
Asserting word line closes switch allowing access via bit line

Presence of charge represents 1
Absence of charge represents 0
Must refresh every few milliseconds to maintain the charge

1- Bit Storage Cell

Storage cells must have 2 stable states: 0 and 1 (*bi-stable*)

Another possible implementation uses cross-strapped inverters:

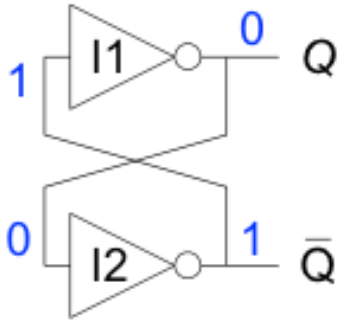


Stable output Q defines the state
State does not change

1- Bit SRAM

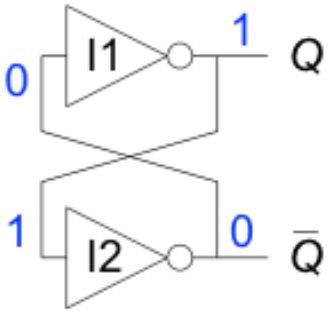
$Q = 0$:

then $\overline{Q} = 1$, $Q = 0$ (consistent)



$Q = 1$:

then $\overline{Q} = 0$, $Q = 1$ (consistent)

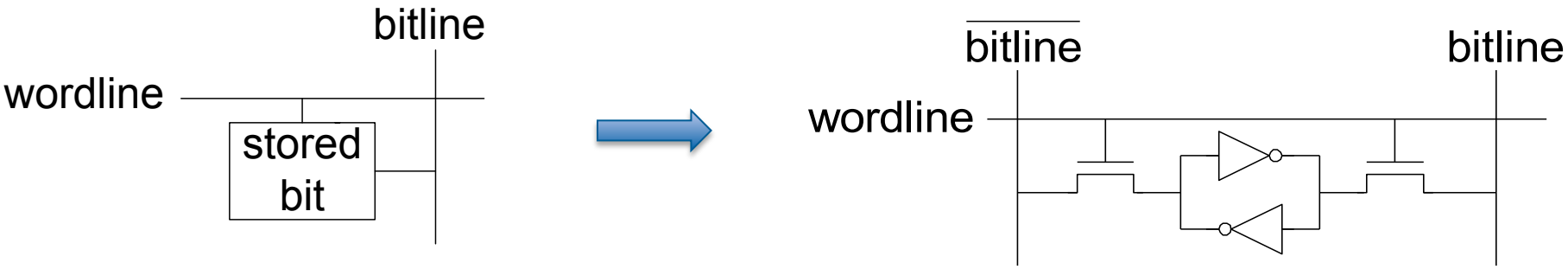


Stores 1 bit of state in the state variable, Q (or $\overline{Q}$)

No refresh is required

1- Bit SRAM

Wordline and bitline allow access to the stored bit



Both switches turn on when wordline is asserted
Stored bit can be transferred to or from bitline or $\overline{\text{bitline}}$

Memory Comparison

Larger storage cells can be built using these single-bit devices

Flip-flops require more transistors to build

Cost, power and area consumed increases with more transistors

Memory Type	Transistors per bit	Latency
Flip-flop	20 or more	fast
SRAM	6	medium
DRAM	1	slow

Memory Comparison

Latency = time required to perform a read or write

Throughput = number of bits that can be accessed per unit time

Flip-flops have very short latencies and high throughput

SRAM has higher throughput and lower latency than DRAM

DRAM must wait for charge to move to bitline

DRAM must be refreshed periodically and after each read

In general, latency increases with larger memory sizes