Computer Science 605.611

Problem Set 9

(Recall that by default the MIPS system uses big endian storage order for memory)

1. The addresses and 8-bit contents of four consecutive memory bytes on a system that uses big endian storage order are shown below:

Address	Contents
0x10040006	0xF1
0x10040007	0xF2
0x10040008	0xF3
0x10040009	0xF4

Register $6 contains the 32-bit address 0x10040006.

a) (3) Show (in hex 0xdddddddd) the 32-bit contents of register $2 after executing the instruction:

lh $2,2($6) $2 = 0xFFFFF3F4

b) (3) Show (in hex 0xdddddddd) the 32-bit contents of register $3 after executing the instruction:

lhu $3,0($6) $3= 0x0000F1F2

2. An integer array that contains two 32-bit elements is declared as:
unsigned integer idata[2];
The element idata[0] contains the value 0x07176305
The element idata[1] contains the value 0x60151930

The memory address of element idata[0] is 0x100900C0. The address of idata[1] is 0x100900C4. Indicate in hex, the contents of the single 8-bit memory byte located at each address listed in the tables below for:

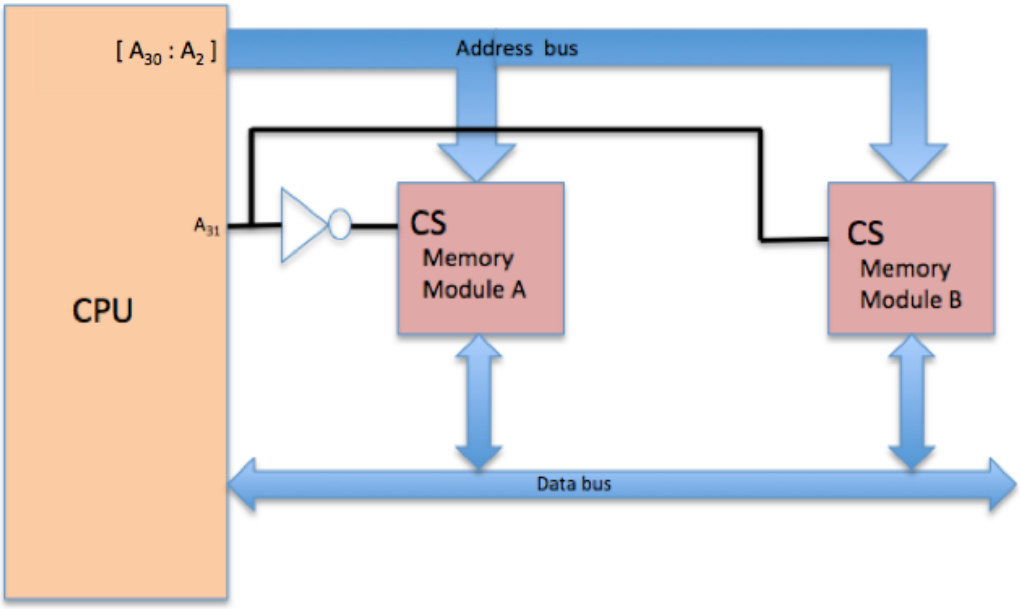
a) (8) a little endian memory system

Address	8-bit Contents
0x100900C1	0x63 = 01100011
0x100900C4	0x30 = 00110000

b) (8) a big endian memory system

Address	8-bit Contents
0x100900C2	0x63 = 01100011
0x100900C6	0x19 = 00011001

3. The memory system shown below consists of two modules (A and B). Each module has a depth of 536870912 and a width of 32. That is, each cell is 32 bits wide and there are 536870912 cells in each module. The memory storage cells within each module are numbered starting from 0. The system employs 32-bit addresses (A31 – A0). However since each memory cell is 4 bytes wide, the 2 low bits of the memory address for each cell are always 00. So bits A1 and A0 are not used on the address bus.



The chip select (CS) is active high. That is, to select a chip, its CS input must =1.

536,870,912 = 2^29

a) (3) What is indicated by the bit pair A0 and A1 within the 32-bit memory address on this system?

The lower 2 bits would indicate which byte within memory word to access

b) (3) What is the minimum number of bytes transferred from memory to the CPU for a single read operation?

32

c) (3) What is the total number of bytes contained in module B?

Total bytes = width # depth = 536,870,912 cells * 4 byte depth = 2,147,483,648

d) (3) What is the 32-bit hex address of cell 7 (the 8th cell) within module A?

Lower 2 bits are 00

8 = 1000

Module A indicated by leading 0

Address = 00000000000000000000100000 = 0x00000030

e) (3) What is the 32-bit hex address of the next to last cell within module B?

Lower 2 bits are 00

Last cell is at 11111111111111111111111111111 (29 1's)

Next to last cell is at 11111111111111111111111111110

Module B is indicated by a leading 1

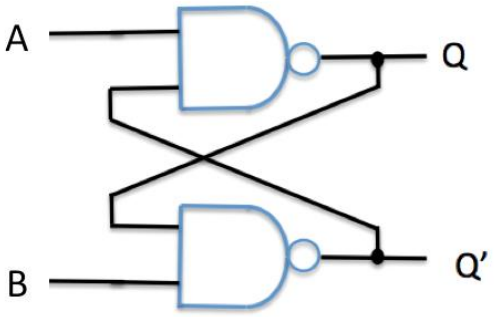
Address = 11111111111111111111111111111000 = 0xFFFFFFF8

f) (4) If register $4 contains 0x80000000, which module and which byte within the module (byte 0 is the 1st, byte 1 is the 2nd byte, etc) is referenced by the instruction:

lbu $6,5($4)

0x80000000 = 10000000000000000000000000000000 references the first cell in module B. The first cell in module B references the first byte, thus an offset of 5 would reference the 6th byte.

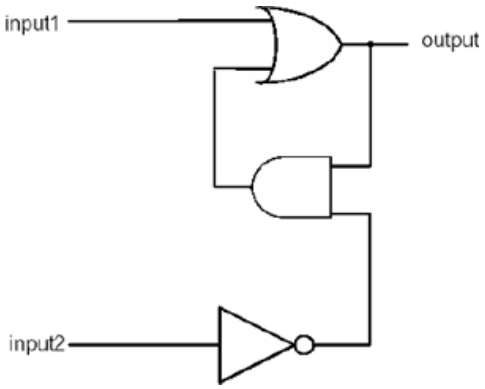
4. (8) Complete the characteristic table for the circuit shown below by filling in the column for Q(t+1), the output in the next cycle, given that Q(t) is the output in the current cycle and the digital inputs in the current cycle are A and B. If there is no change then Q(t+1)=Q(t), otherwise Q(t+1) = 0 or Q(t+1) = 1.



A	B	Q(t+1)
0	0	
0	1	
1	0	
1	1	

A	B	Q(t+1)
0	0	? unpredictable
0	1	1
1	0	0
1	1	!Q(t) (opposite of Q(t)

5. (5) Which one of the following (a. through e.) best describes the circuit below? Explain your answer.



a. D Latch
b. D Flip-flop
c. S-R Latch
d. S-R Flip-flop
e. Comparator

Characteristic Table:

input1	input2	output
0	0	Q(t)
0	1	0
1	0	1
1	1	1

This is the same behavior of the S-R Latch, except that supplying 11 as input produces a positive signal for the output rather than an unpredictable signal.

6. Recall that performing a read from a dynamic RAM (DRAM) requires that the chip pre-charge before it can supply the requested data. Assume that it takes 10ns to pre-charge and 15ns to either output the requested data in response to a read operation or to store the input data for a write operation. Also recall that our MIPS pipeline system employs a Harvard Architecture, transfers 32 bits at a time between the CPU and memory, and each pipeline stage consumes one clock cycle.

   a) (5) If the memory stage is the most time consuming stage, what is the maximum clock rate (expressed in GHz) that can be used for our 5-stage pipelined system using this type of DRAM memory?

Clock rate = 1 / clock cycle time
Clock cycle time is the time of the slowest operation,
Clock rate = 1 / 25 ns = .04 GHz

   b) (5) The instruction memory contains one machine instruction per cell and is implemented as a single memory module with a storage capacity of 268435456 bytes, what is the width and depth of the module?

The length of one machine instruction is 32 bits, therefore the width of the module must be 32 bits = 4 bytes. The depth of the memory module times the width of the module must equal the size of the module, thus the depth of the module = 268,435,456 * 8 / 32 = 67,108,864 bytes, or 536,870,912 bits

7. The diagram below shows the 32-bit address format used for a particular byte addressable memory system containing 16 modules:

31 28	27 1	0
Module#	Cell number	offset within cell

a) (3) What is the width in bits of each memory module? Width = _____ bits.

width = 2^{27} = 134,217,728 bytes = 1,073,741,824 bits

b) (4) How many memory modules must be accessed to read a single 32-bit word from address 0x00408000 with this memory system?

0x00408000 = 0000 0000 0100 0000 1000 0000 0000 0000
One memory module

c) (4) How many memory modules must be accessed to read a single 32-bit word from address 0x3FFFFFFE with this memory system?

0xFFFFFFFE = 1111 1111 1111 1111 1111 1111 1111 1110
This address will access the last byte in memory module 32, and the first 3 bytes in memory module 1, thus must access two memory modules.

8. (9) Our byte addressable MIPS system employs a 32-bit CPU-to-memory bus as well as memory cells that are 32 bits wide. Recall that an aligned memory access is one for which the memory address used for the read or write is a multiple of the size (in bytes) of the item that is being transferred.
Ignoring any exceptions that may occur, how many data memory cells must be read by each of the following instructions if the contents of register $8 = 0xB003D8E0 ?

0xB003D8E0 is a multiple of 4, thus references the beginning of a single memory word.

An offset of 54 will reference the 16th index of a 32 bit memory word, as there are 4 bytes in a 32 bit word (54 % 4 = 2).

Thus lb/lh instructions will only have to reference one individual data memory cell, while lw will have to reference two individual data memory cells.

I. lb $t0,54($8)

1

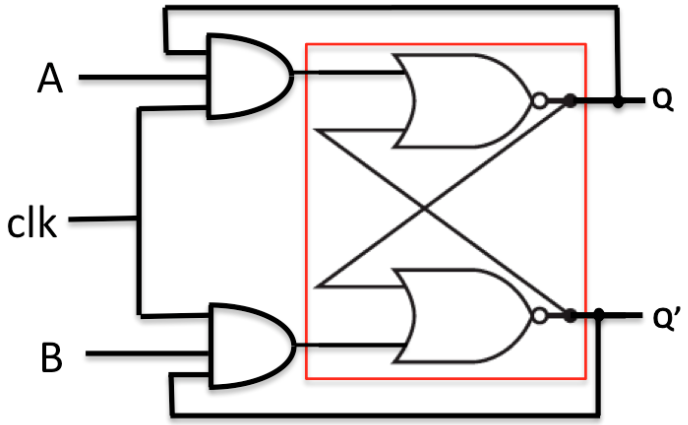
II. lh $t0,54($8)

1

III. lw $t0,54($8)

2

9. (8) Complete the characteristic table for the circuit shown below by filling in the column for Q(t+1), the output in the next cycle, given that Q(t) is the output in the current cycle and the digital inputs in the current cycle are A and B which take effect when the clock signal (clk) pulses from low to high and back to low. The width of the pulse is such that the outputs Q and Q' only change once. If there is no change then Q(t+1)=Q(t), otherwise Q(t+1) = 0 or Q(t+1) = 1.



A	B	Q(t+1)
0	0	
0	1	
1	0	
1	1	

A	B	A(t+1)
0	0	Q(t)
0	1	1
1	0	0
1	1	!Q(t) (opposite of Q(t))

10. A computer system designed and built in the 1970's made use of a single 8-bit CPU-to-memory data bus and a single separate address bus. Suppose that such a system contained 4 memory modules or chips, each of which was 8 bits wide with a depth of 16777216. A memory access for each module consisted of only two phases: an addressing phase in which an address is sent to select a specific memory module and cell within the module; and a data transfer phase in which the selected data item is read from or written into. Each phase takes 40 nano-seconds to complete. What is the minimum time (in nano-seconds) required to read a single 32-bit data item from this memory system if it employs:

A single memory module can perform either an addressing phase or a data transfer phase at one time.

a) (4) high order interleaving

High order interleaving means that consecutive memory addresses are in the same memory module. Thus each of the 4 bytes required to read a single 32 bit data item from memory would take four times the time to read a single instruction (80ns), thus the total time is 320ns.

b) (4) low order interleaving

Low order interleaving means that consecutive memory addresses are in different memory modules. Thus, each of the 4 bytes required to read a single 32 bit item from memory would take the same amount of time that it takes to read a single instruction (80ns) since the modules can operate in parallel, thus the total time is 80ns.