Computer Science 605.611

Problem Set 13 Answers

1. a) (5) Show a pair of Intel IA-32 instructions that place the 64-bit two's complement equivalent of the integer -763 (negative 763) into registers EAX and EDX (with the high part in EDX).

```
MOV   EAX,-763      put -763 into EAX
CDQ                 convert 32-bit value in EAX into 64-bits in EDX,EAX
```

b) (5) Show a pair of SparcV8 instructions that place the 64-bit two's complement equivalent of the integer -763 (negative 763) into registers %o4 and %o5 (with the high part in %o5).

```
add    %g0,-763,%o4
add    %g0,-1,%o5
```

2. A function or procedure that is called usually performs some task and returns control to the caller. Indicate where (i.e., in which register of memory location) the return address is saved by each of the following processor instructions:

a) (5) SparcV8 instruction: call sqrt

Register %o7 (linkage register) is used for the return address = %o7+8

b) (5) Intel IA-32 instruction: call sqrt

The return address is pushed onto the stack.

c) (5) ARM instruction: BL sqrt

The return address is placed into R14, the linkage register.

3. a) (4) Show a MIPS true-op instruction that implements the nop synthetic or pseudo-instruction.

```
sll    $0,$0,0
```

b) (4) Show a SparcV8 true-op instruction that implements the nop synthetic or pseudo-instruction.

```
sethi  %hi(0),%g0
```

4. (5) The IEEE-754 single precision and double precision floating point formats provide 7 and 15 decimal digits of accuracy, respectively. How many decimal places are provided by the Intel internal 80-bit extended precision floating point format?

Show how you arrived at your answer.

One bit is used for the sign and 15 bits are used for the exponent. One bit is used to indicate whether the number is normalized or denormalized. This leaves 63 bits for the value which corresponds to $63*\log_{10}(2) = 63*0.30103 = 18.965$ (i.e., about 19 decimal places).

5. (5) Manually generate (i.e., by hand) the 80-bit extended precision floating point representation of the negative value: -4.87493 on an IA-32 processor. Show your answer as a sequence of hex digits.

The integer part in binary is 100.

0. 87493 * 2^{64} = 16139609792410697728 = 0xDFFB69984A0E4000

So decimal -4.87493 = - 0x4.DFFB69984A0E4000 = negative binary

$1.0011011111111110110110100110011000010010100000111001000000000000000 * 2^2$

The excess-16383 representation of the exponent is 16383+2 = 16385 = binary 100000000000001.

The 80-bit pattern is:

1100 0000 0000 0001 1001 1011 1111 1111 0110 1101 0011 0011 0000 1001 0100 0001 1100 1000 0000 000

= 0xC0019BFF6D330941C800

6. (5) The following MIPS instruction sequence saves MIPS registers $2, $4 and $6 on the stack:

```
add   $sp,$sp,-12
sw    $2,8($sp)
sw    $4,4($sp)
sw    $6,0($sp)
```

Show a single (i.e., one) complete ARM assembly language instruction that similarly saves ARM registers R2, R4 and R6 on the stack.

STMFD R13! , {R2, R4, R6}

7. a) (5) Show one MIPS true-op instruction that has the same effect as the instruction: LEA EAX,[EBX + 44] on the Intel IA-32 processor. Use $8 as the result register and $9 as the base register in the MIPS instruction.

addiu $8,$9,44

b) (5)) Show one ARM true-op instruction that has the same effect as the instruction: LEA EAX,[EBX + 44] on the Intel IA-32 processor. Use R4 as the result register and R5 as the base register in the ARM instruction.

ADD R4,R5,#44

8. (5) The following ARM processor instruction: MVN R2,#3 places a bit pattern into register R2. If the resulting bit pattern is interpreted as a two's complement format signed integer, what signed decimal (i.e., base 10) value does it represent?

Contents of R2 represents: – 4_____ Bit pattern = __0xFFFFFFFC _

9. The acronym IBM stands for International Business Machines. What does each of the following acronyms stand for? Each acronym relates to one of the processors described in this course.

a) (1) MIPS - Microprocessor without Interlocking Pipeline Stages

b) (1) ARM - Advanced RISC Machine

c) (1) IA-32 - Intel Architecture 32

d) (1) Sparc - Scalable Process Architecture

10. Assume that the MMX registers MM2 and MM4 on an IA-32 processor contain the 64-bit patterns 0xA0A1A2A3A4A5A6A7 and 0xB0B1B2B3B4B5B6B7, respectively. Assume also that the MIPS registers $2, $3, $4 and $5 contain the following bit patterns:

$2	$3	$4	$5
0xA0A1A2A3	0xA4A5A6A7	0xB0B1B2B3	0xB4B5B6B7

a) (5) Show, in hex, the contents of register MM2 after the IA-32 instruction
PADDB MM2,MM4 is executed. Result in hex = 0x50525456585A5C5E.

b) (5) Show, in hex, the contents of MIPS registers $2 and $3 after the following two MIPS instructions are executed:
addu $2,$2,$4
addu $3,$3,$5
$2 in hex = 0x51535556___ $3 in hex = __0x595B5D5E___.

11. A machine instruction stores the 32-bit contents of a register into memory at address 0x80084004. Show the contents of the single byte at location 0x80084006 if the store instruction is executed on:

a) (5) an IA-32 processor and the register that is stored contains 0xFEEDBEEF ?
Contents of byte in hex = 0xED
The IA-32 system employs little-endian memory storage order, so byte 0 from the register (the low byte) which contains 0xEF is stored at 0x80084004 , and byte 2 which contains 0xED is stored at location 0x80084006

b) (5) a SparcV8 processor and the register that is stored contains 0xA1C0FFEE ?
Contents of byte in hex = 0xFF
The Sparc employs big-endian memory storage order, so the high byte from the register (which contains 0xA1) is stored at 0x80084004 and the byte that contains 0xFF is stored at location 0x80084006.

12. a) As described in module 13, what is the maximum number of CPU registers contained in each of the following processors?

- (2) IA-32 8 operand registers: EAX, ECX, EBX, EDX, EBP, ESP, EDI and ESI

  (2) ARM 16 operand registers: R0 – R15 used in the User/System mode. Additional "banked" registers are available in each of the 5 exception modes. The additional registers are outlined in blue in the diagram below. These replace some of the corresponding user/system registers depending on the exception mode: 7 for FIQ and 2 for each of the other four modes. Hence the total number of registers that can by used as operands by the ARM CPU = 16 + 7 + 2 + 2 + 2 +2 = 31.

Accessible registers in different modes of the ARM processor.

User/System	FIQ	IRQ	Supervisor	Abort	Undefined
R0	R0	R0	R0	R0	R0
R1	R1	R1	R1	R1	R1
R2	R2	R2	R2	R2	R2
R3	R3	R3	R3	R3	R3
R4	R4	R4	R4	R4	R4
R5	R5	R5	R5	R5	R5
R6	R6	R6	R6	R6	R6
R7	R7	R7	R7	R7	R7
R8	R8_fiq	R8	R8	R8	R8
R9	R9_fiq	R9	R9	R9	R9
R10	R10_fiq	R10	R10	R10	R10
R11	R11_fiq	R11	R11	R11	R11
R12	R12_fiq	R12	R12	R12	R12
R13	R13_fiq	R13_irq	R13_svc	R13_abt	R13_und
R14	R14_fiq	R14_irq	R14_svc	R14_abt	R14_und
R15	R15	R15	R15	R15	R15

- (4) Sparc_v8 There are 8 global registers (%g0 - %g7). The first window contains 8 in registers (%i0 - %i7), 8 local registers (%l0 - %l7), and 8 out registers (%o0 - %o7). For each window after the first, the in registers (%i0 - %i7) overlap with and are the same as the out registers (%o0 - %o7) of the previous window. Hence each window after the first requires 16 new registers. Windows 2 through 31 contain 24 registers (8 are from the previous window and 16 are new).
  So the total (for 32 register windows) is 8 + 8 + 8+ 8 + 31*16 = 528.

b) The PC (program counter) is to be incremented by 16 using a single ADD instruction. For each of the processors listed below, indicate whether the processor can or cannot accomplish this.

- (2) ARM processor Yes. R15 is used as the program counter, so it can be incremented using an ADD instruction.
- (2) MIPS processor No. The PC can't be used as an operand on the MIPS. So an ADD instruction can't be used to increment it by 16.
- (2) IA-32 processor No. The IA-32 EIP register is the program counter and can't be used as an operand for an ADD instruction.
- (2) Sparc V8 processor No, the Sparc processor can't use the PC as an ALU operand.