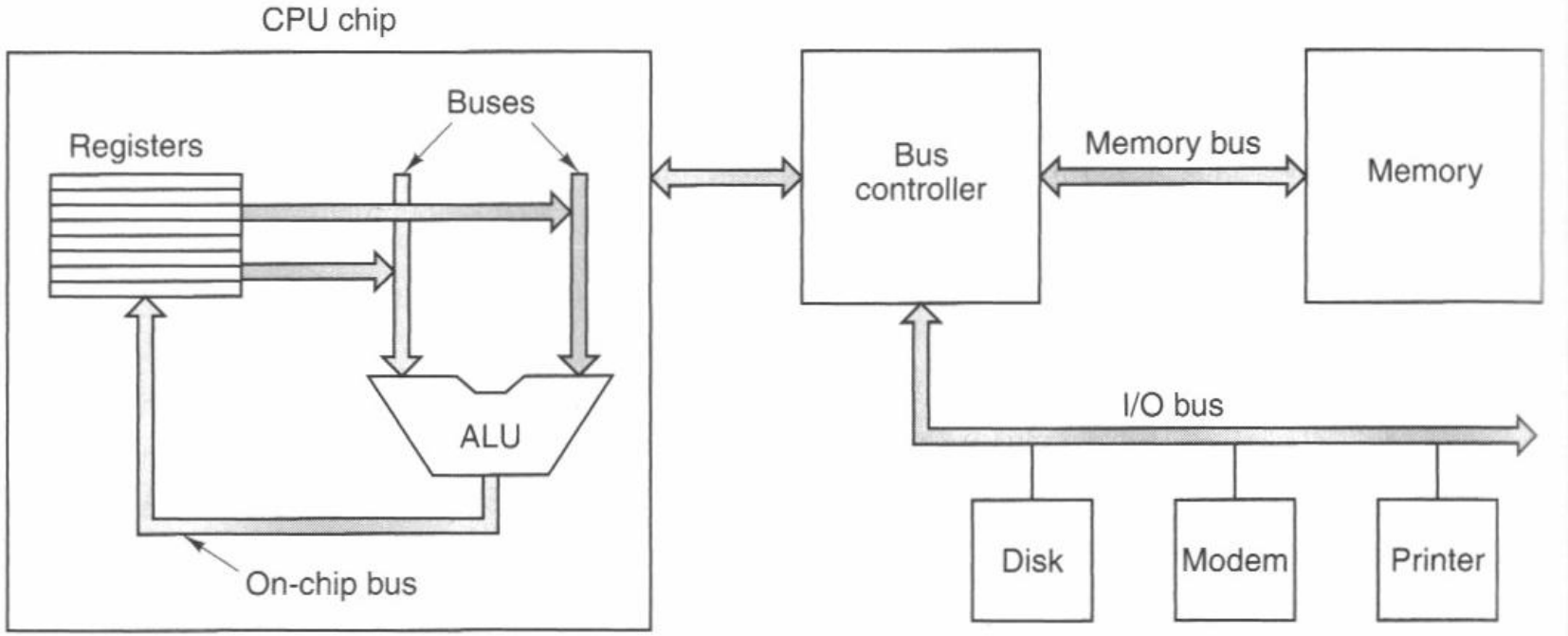
Bus Systems

- Components exchange information via buses
  - A bus is a set of shared lines or electrical traces
  - Chips have pins that connect to these shared lines
- Computers use a hierarchy of buses
  - Some are internal to the CPU
  - External buses are used for I/O
- Bus protocols are rules for using the bus
  - specify timing techniques
  - Arbitration rules to resolve conflicting requests
  - Synchronous versus asynchronous communication

Bus Systems

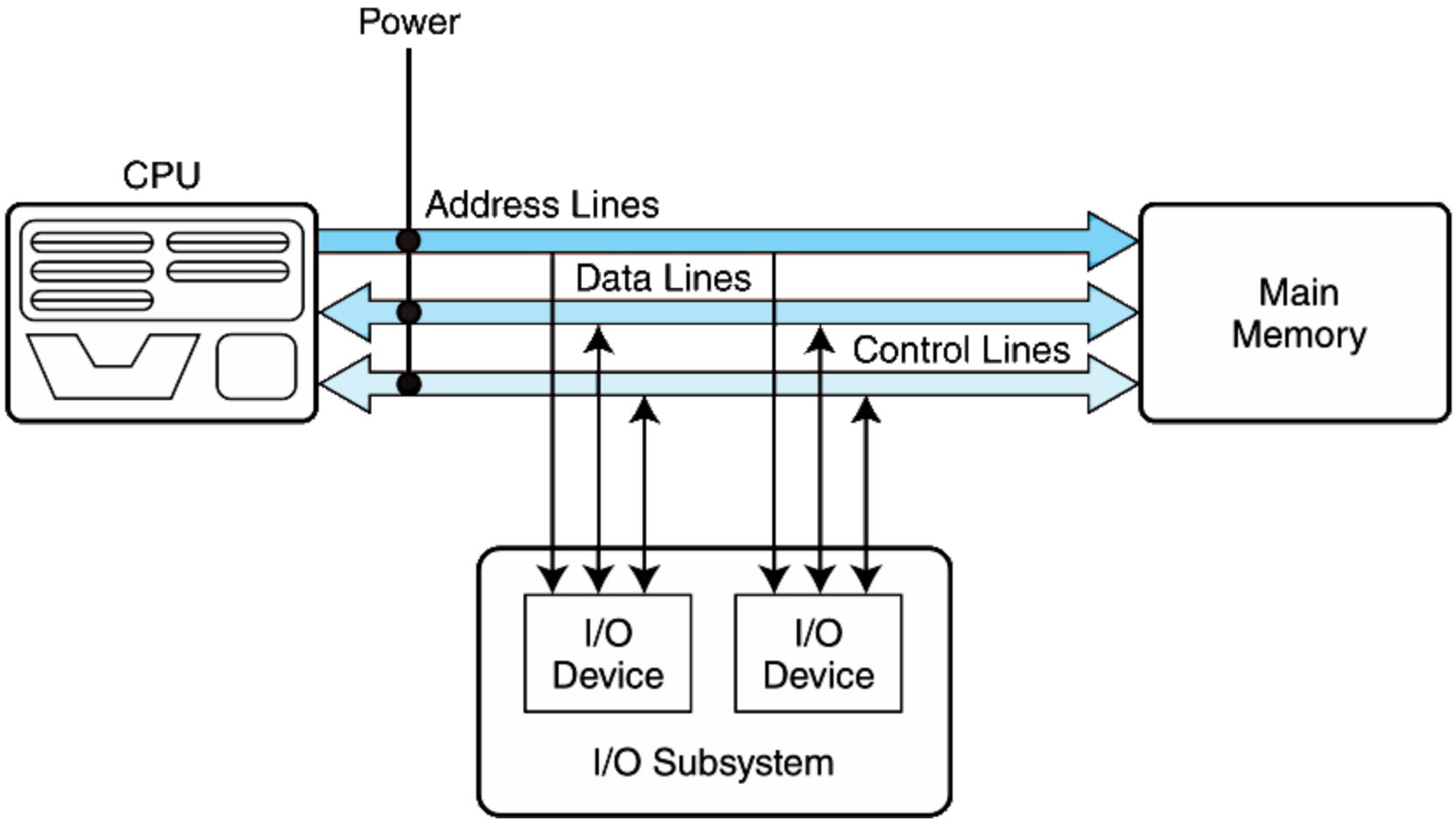


- CPU-to-memory buses are parallel synchronous buses
  - Operate at higher rates than I/O buses
  - Clock signals synchronize the exchanges
- I/O buses can be parallel or serial
  - Operate at rates that match slow I/O device speeds
  - Communicate asynchronously using handshake signals

Bus Systems

- Buses consist of:
  - data lines
  - control lines
  - address lines
- Data lines convey bits from one device to another
- Signals on control lines determine:
  - the direction of data flow
  - when each device can access the bus
- Address lines determine the location of the source or destination of the data

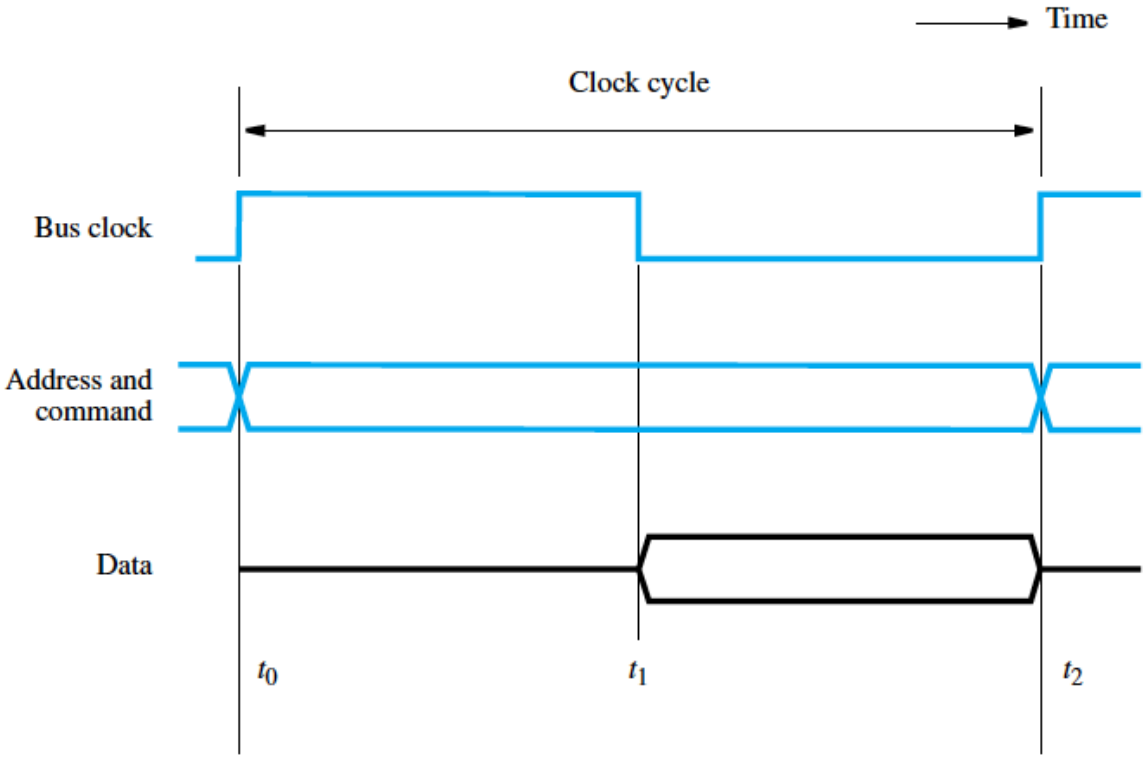
Bus Systems


Power
CPU
Address Lines
Data Lines
Control Lines
Main Memory
I/O Device
I/O Device
I/O Subsystem

Bus Systems

- Buses may be serial or parallel
  - Bits are sent simultaneously along each parallel bus line
  - Bits are sent one after the other along a serial bus line
- Bus bandwidth = amount of data transferred per unit time
  - Depends on width (number of data lines)
  - Depends on cycle time and number of cycles used
- A common clock signal is used by *synchronous* buses
  - Transactions adhere to a bus schedule
    - The schedule must accommodate the slowest device
    - Slowest device dictates the cycle time
  - Clock skew can be a problem
    - Different devices may not see the clock signal at the exact same time

Synchronous Bus Read



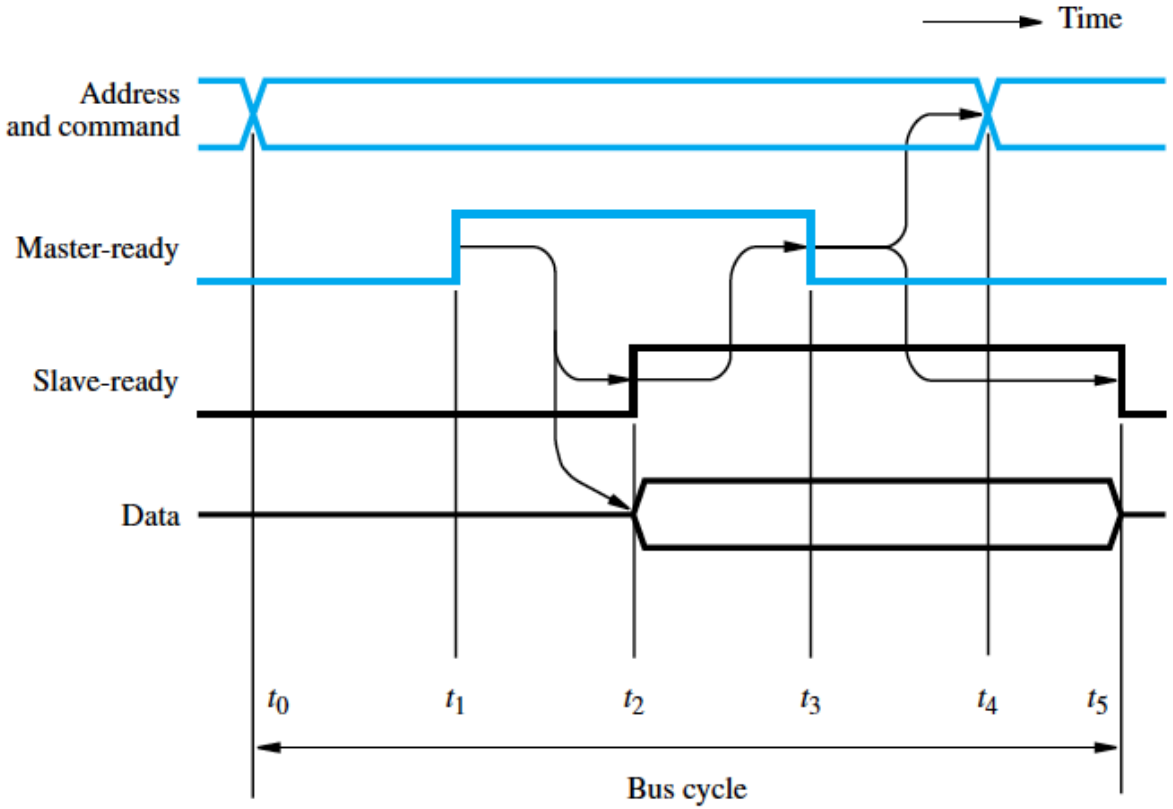
Data requested from the specified address is available at t_1

If data cannot be provided in time, “wait states” are inserted

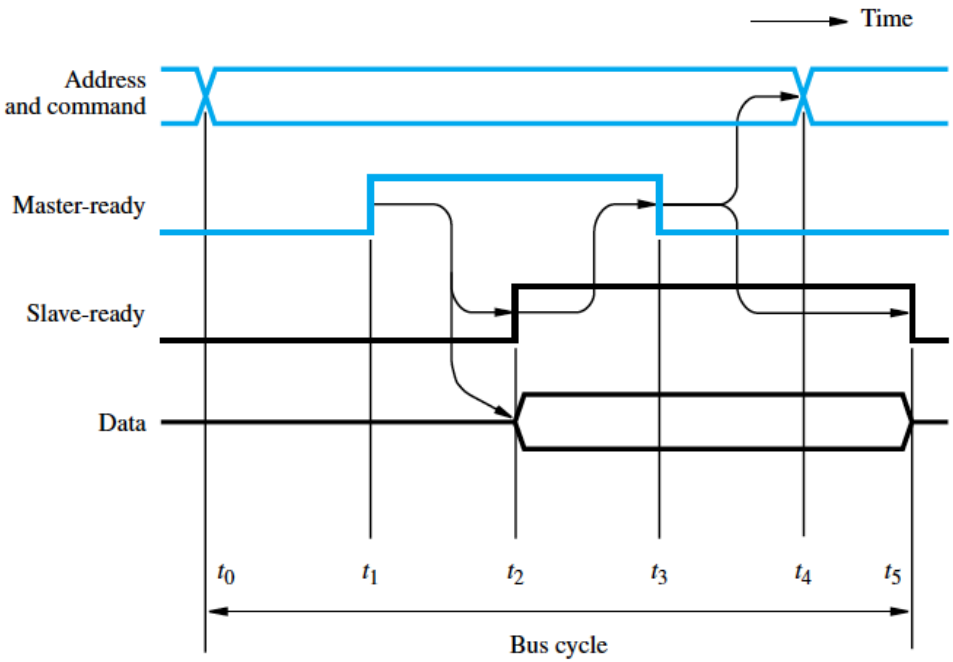
Wait states are additional complete clock cycles

Bus Systems

- *Asynchronous* buses exchange handshake signals
  - Each step in the transaction requires a signal or response
  - transaction speed varies with the devices involved (self-paced)



Asynchronous Bus Read



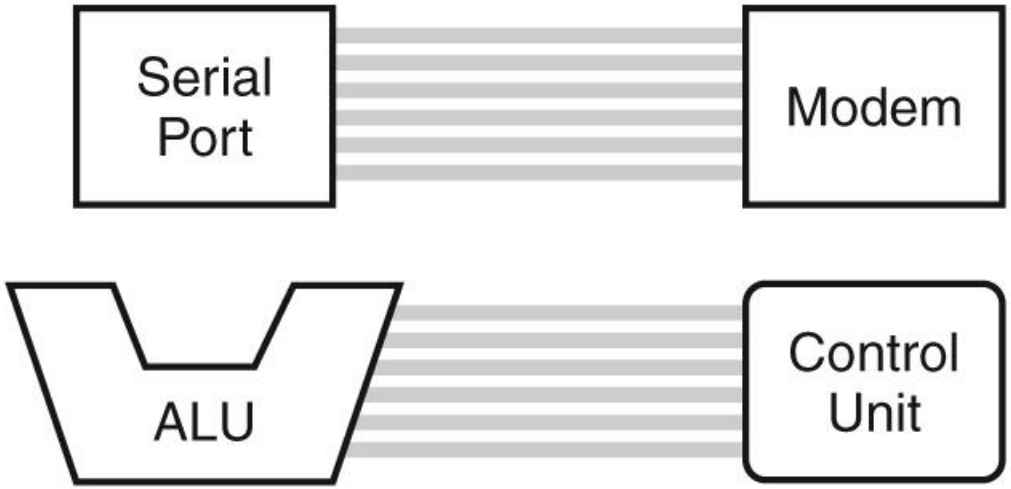
Master-ready is asserted to signal valid address and command
Slave-ready is asserted when requested data is available
master-ready is de-asserted in response to receiving the data
Slave-ready is de-asserted to allow next transaction to begin

A positive action is required to proceed to the next step

Bus Systems

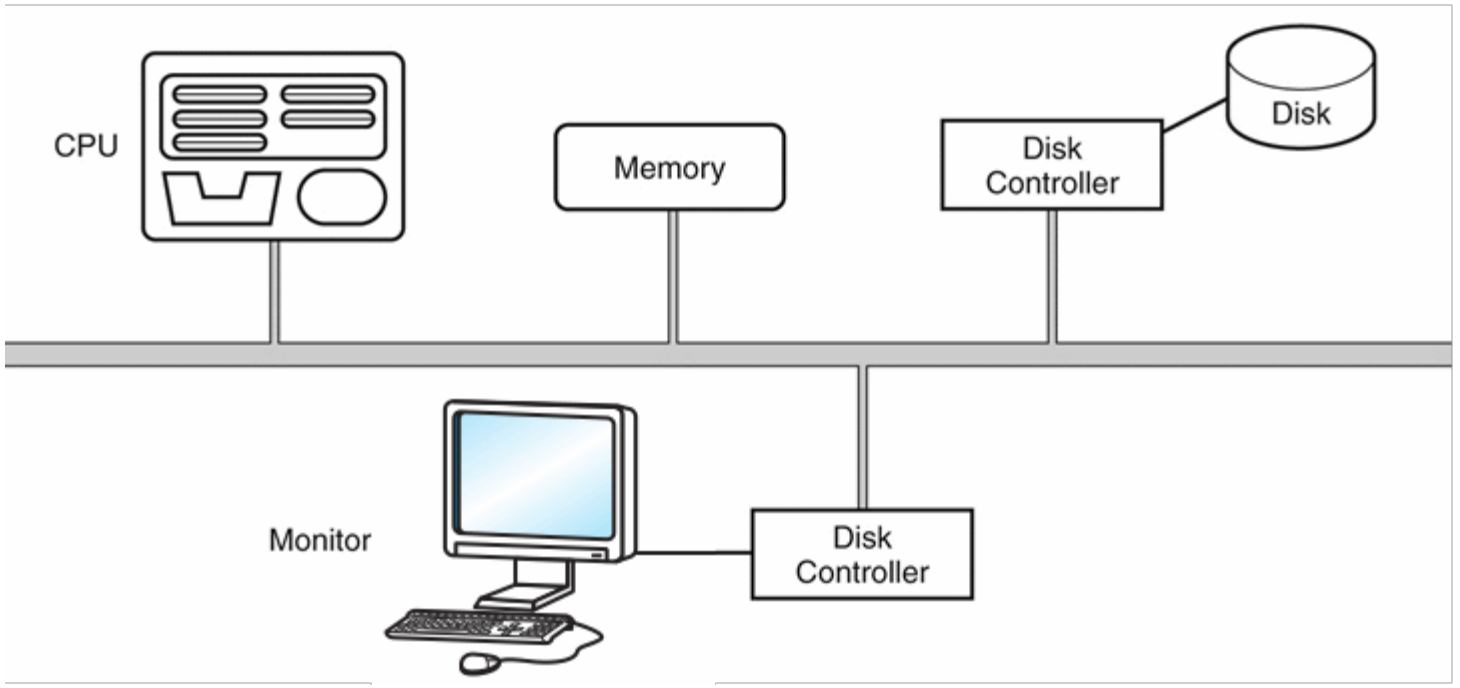
- Two types of buses are commonly found in computer systems: *point-to-point*, and *multipoint* buses.

These are point-to-point buses:



Bus Systems

- A multipoint bus is a shared resource
- Protocols can be built into the hardware
  - They control access to the bus



Bus Systems

- Bus transactions:
  - All the actions needed to exchange information
  - Occurs in a “bus cycle”
    - May correspond to multiple clock cycles
- Only one device at a time controls the bus
  - Called an “initiator” or “master”
  - Initiator or master communicates with “target” or “slave”
- Arbitration resolves competing requests for control