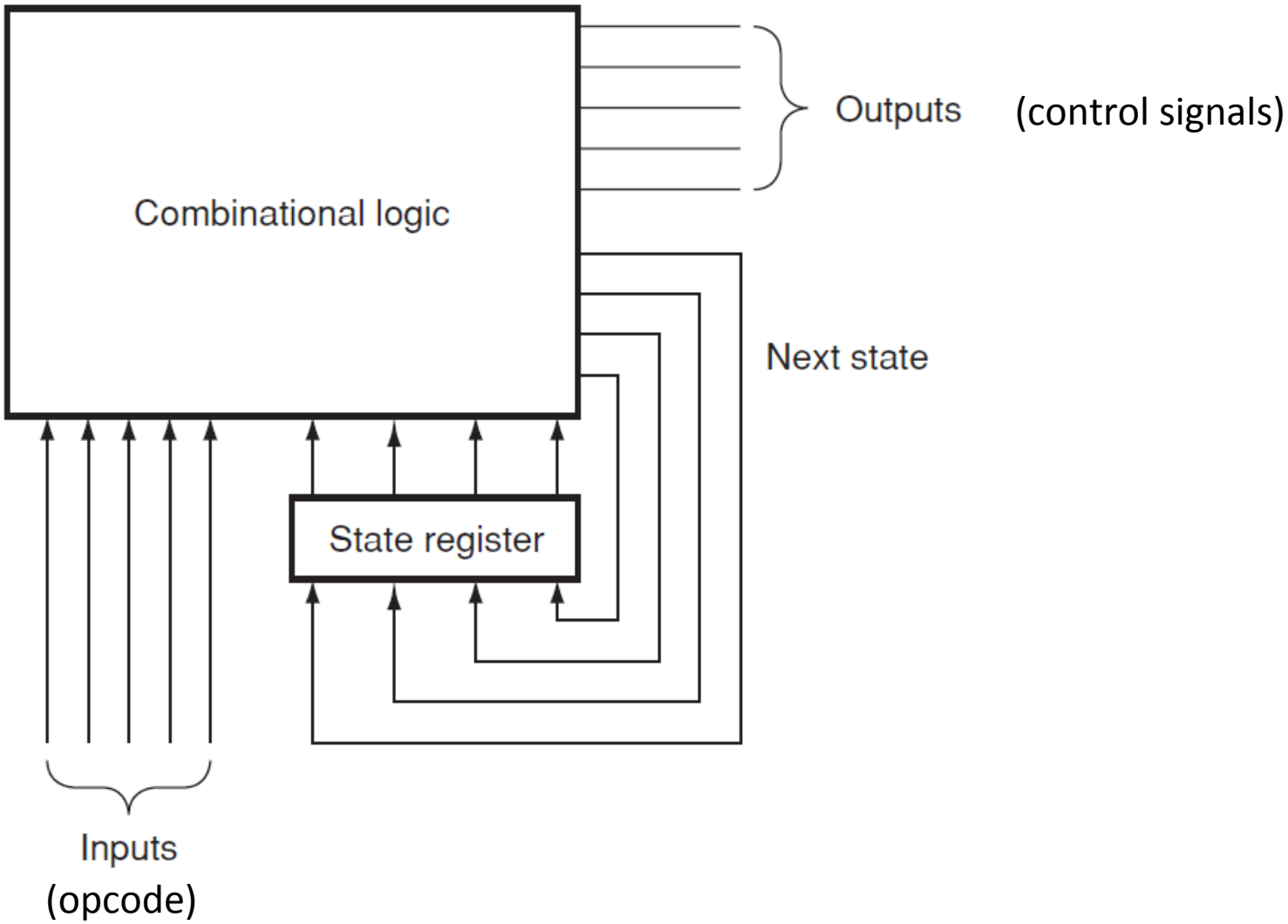
FSM for MIPS Control Unit

- Set of inputs are the opcode bits
- Set of outputs are the control signals
- Next-state function is implemented with combinational logic
- New state is computed synchronously with clock cycle

FSM for MIPS Control Unit



FSM for Multicycle Control

MIPS core instruction subset requires 10 states