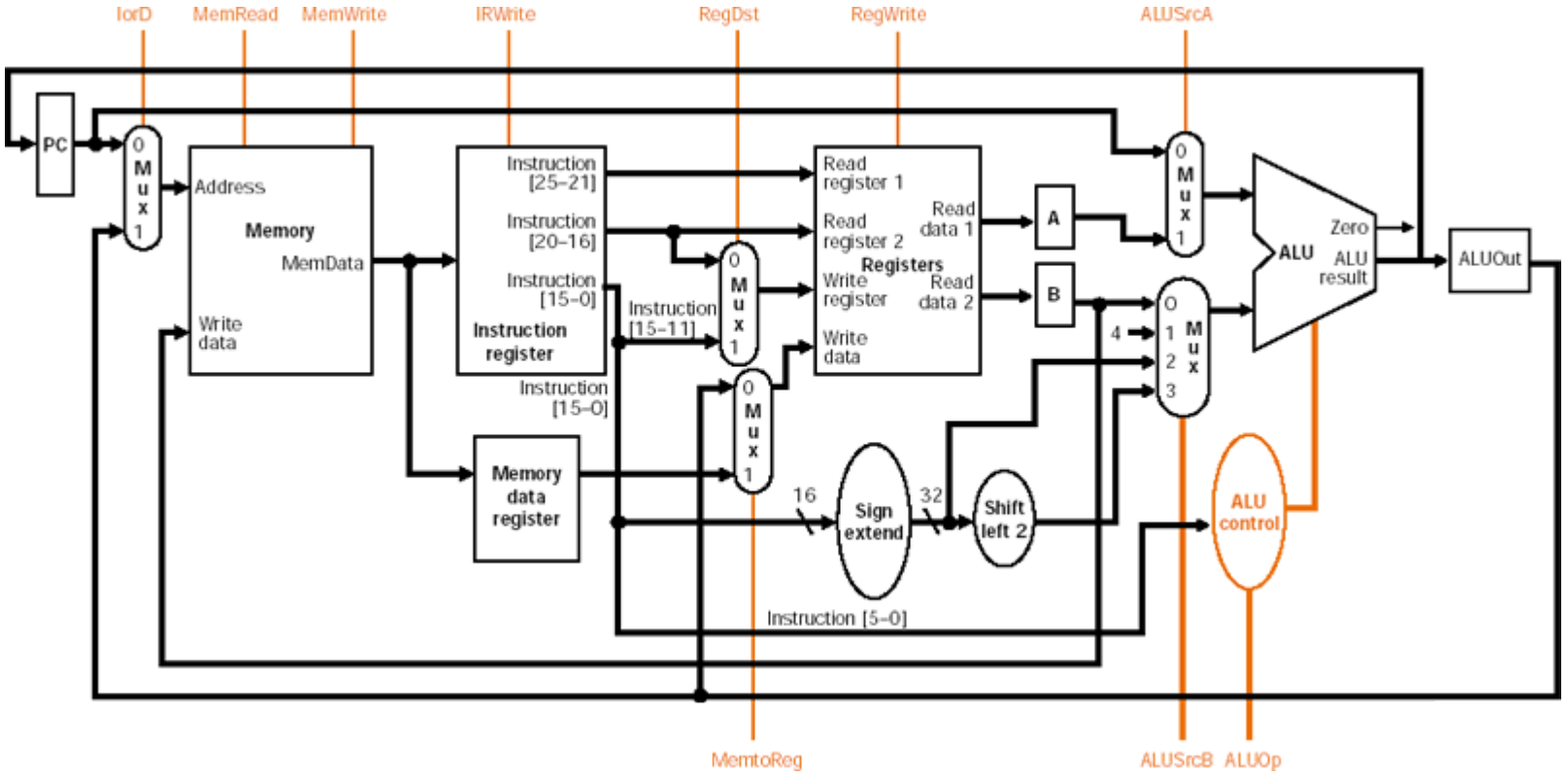
Other Control Implementations

- Instructions can be executed in multiple steps
- Longest step determines clock period
  - Critical path: memory access time
  - Each step takes one clock cycle
- Different control signals are generated in different clock cycles
- Change in state occurs with each cycle
- Sequential logic contains state
- Finite-state machine can model behavior

Multi-cycle Datapath



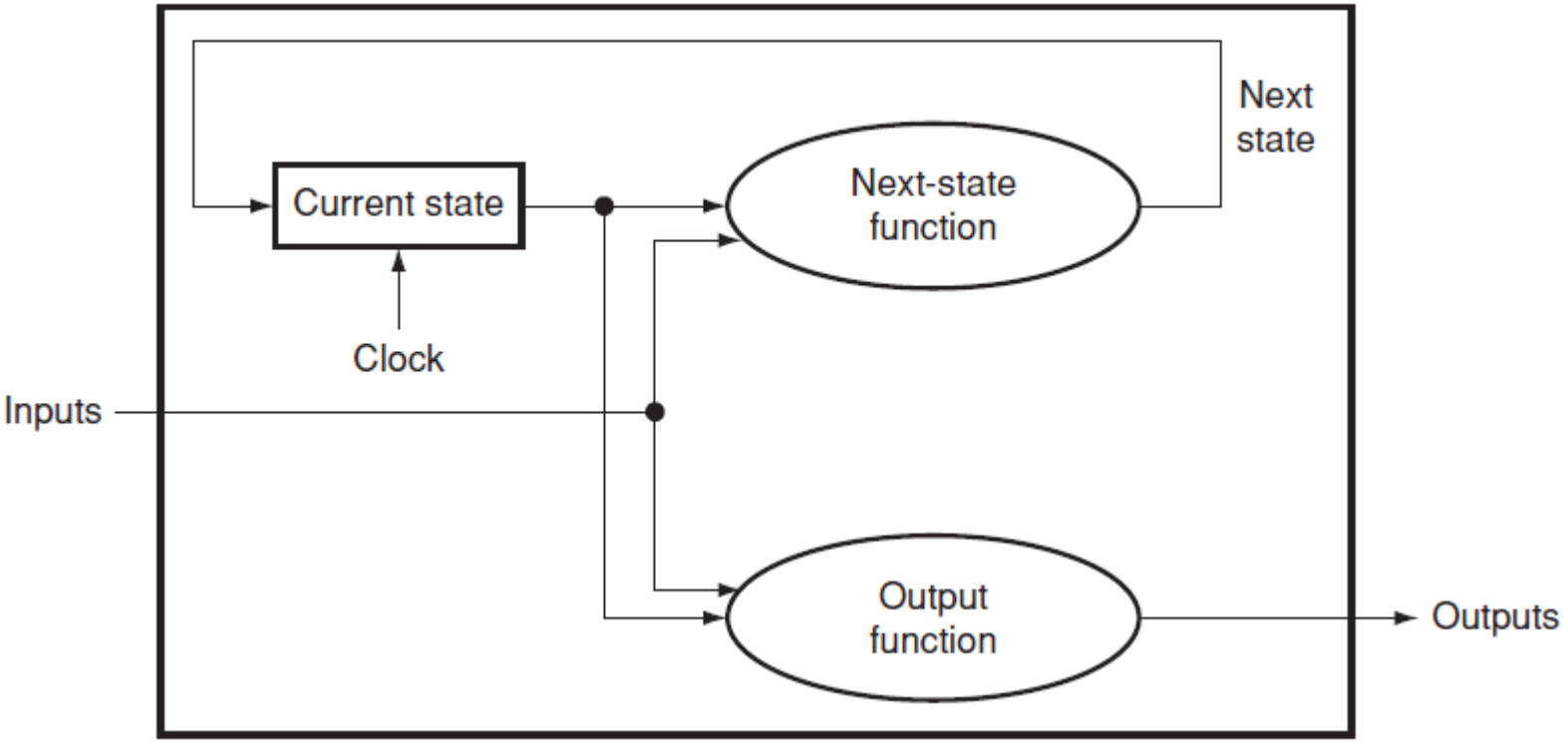
- Component re-use eliminates duplication and reduces cost

Finite State Machine Control

Also called “state machine” or FSM and contains:

- Set of states (one of which is the initial start state)
- Set of inputs
- Set of outputs
- Next-state function maps current state and inputs to a new state (state transition)
- Output function maps current state to set of outputs
  - Outputs may also depend on inputs
  - “Moore machine” outputs depend only on state
  - “Mealy machine” outputs depend on state and inputs

Finite State Machine Control



Sequential logic, internal storage contains the state information