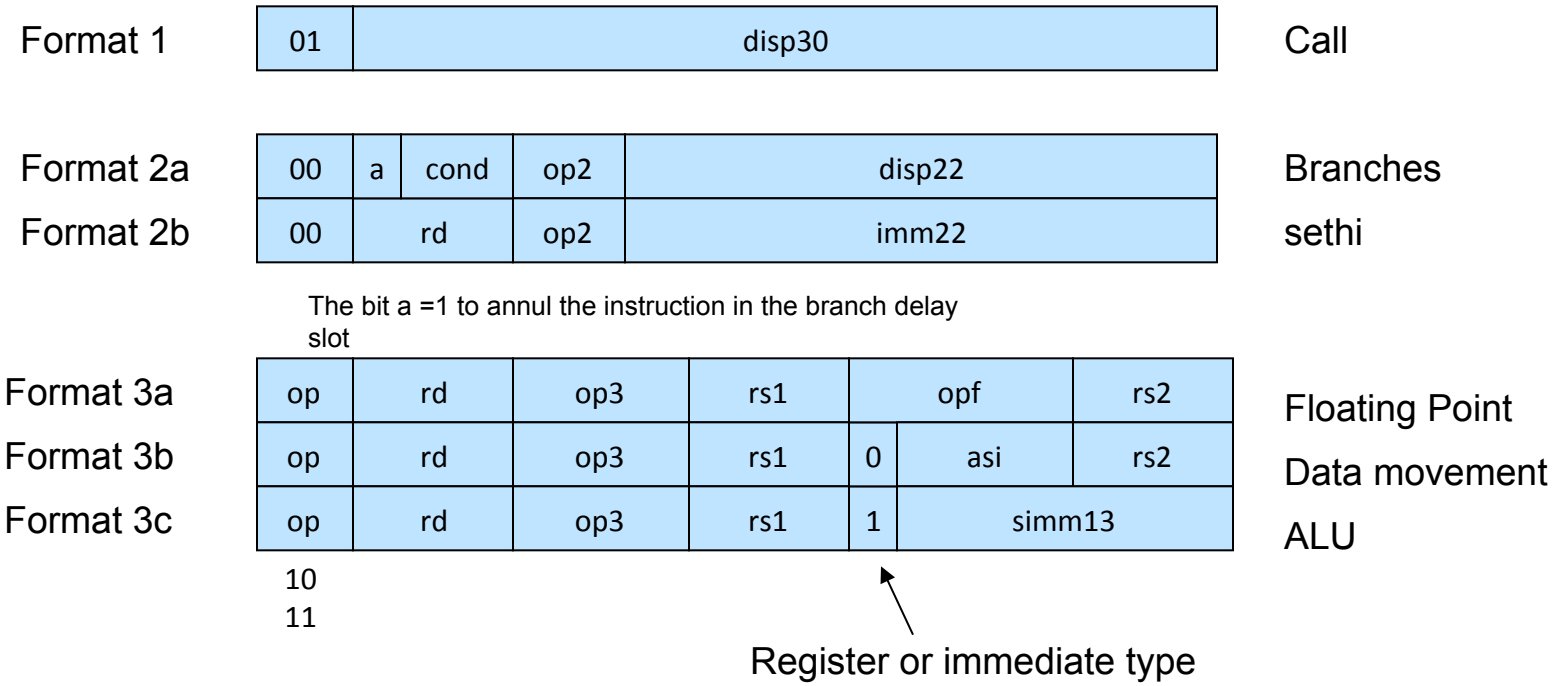
Sparc Machine Instructions

- There are 3 machine instruction formats



The leftmost 2 bits indicate to which of the 3 groups the instruction belongs.

Sparc Machine Instructions

The CALL instruction contains a 30-bit PC-relative displacement to the target location.

npc = (instruction<29:0> << 2) + pc generates address of function to be called

Using the pc-relative displacement instead of the direct address makes the CALL instruction position-independent.

Sparc Machine Instructions

Format 2a

Branches

Branch instructions contains a 22-bit PC-relative displacement to the target location.

Limits branch range to $\pm 2^{21}$ instructions from program counter

Op2 = 010 indicates a conditional branch

4-bit cond field indicates condition that causes branch to be taken

Annul bit (a) prevents execution of instruction in delay slot when branch is not taken

Sparc Machine Instructions

Format 2b

sethi

The sethi instruction has op2 = 100 & contains a 22-bit immediate value

Value is loaded into upper 22 bits of rd register and low 10 bits are cleared to 0

Can be combined with “or” instruction to fill rd with a 32-bit constant

facilitated by %hi(x) and %lo(x) assembler operators

```
sethi   %hi(x),  %o1          ; puts upper 22 bits of address x into %o1 reg.
or      %o1, %lo(x), %o1      ; merges in low 10 bits of address x
```

Sparc Machine Instructions

Arithmetic/logic instructions use one of two formats.

Format 3b	10	rd	op3	rs1	0		rs2
Format 3c	10	rd	op3	rs1	1	simm13	

ALU

Rd is destination result register

Op3 indicates the operation

1st source register is rs1

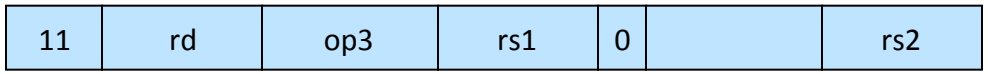
If bit13 = 0 the rs2 is the 2nd source register

If bit13 = 1 the second source operand is a 13-bit signed immediate value

Sparc Machine Instructions

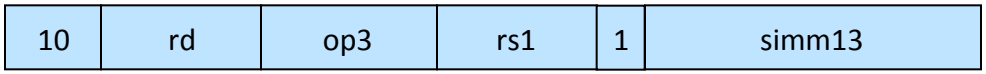
Load & store instructions access memory

Format 3b



Data movement

Format 3c



Op3 indicates type of data movement instruction (6 bits)

Loads read from memory into the rd register

Stores write contents of rd register into memory

Memory address accessed = [rs1] + [rs2] if bit13=0

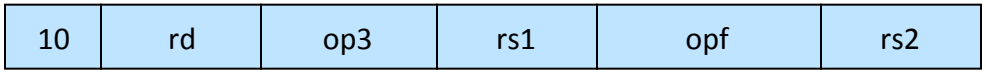
= [rs1] + simm13 if bit13 = 1 (-4096 ≤ offset ≤ 4095)

if rs2 = %g0, this is effectively register indirect addressing for the memory operand

Sparc Machine Instructions

Floating Point machine instruction format

Format 3a



Op3 = 110100 indicates Floating Point instruction

Opf indicates floating point operation

FP result register is rd, source registers are rs1 and rs2