



MIPS Instruction Types

- R-type employs register operands
- I-type contains a literal (immediate value)
- J-type contains part of the jump address



MIPS Instruction Summary

Instruction type	Examples
arithmetic	add, sub, addu, subu, mult, multu, div, divu
Logical	and, andi, or, ori, xor, xori, nor, sll, srl, sra, sllv, srlv, srav
Data transfer	lw, lh, lb, sw, sh, sb, lui, mfhi, mflo, mthi, mtlo
Conditional branch	beq, bne, bltz, blez, bgtz, bgez
Unconditional branch	b, j, jr, jal
Comparison	slt, slti, sltu, sltiu



Addressing Modes

The MIPS only supports the following addressing modes:

1. Register mode (operands in registers)
2. Immediate mode (literal contained in instruction)
3. Base relative mode (offset + contents of base register give the memory address of the operand)



4. PC-relative: $PC + (4 \times \text{displacement})$ gives the branch target address)
5. Pseudo-direct (rightmost 26 bits with machine instruction is multiplied by 4 and concatenated with upper 4 bits of PC to yield the jump address)



- The 16-bit immediate values are sign-extended to 32 bits by the arithmetic, load/store and branch instructions.
- The logical instructions (e.g. AND, OR, etc.) generate the 32-bit immediate operand by zero-extending the 16-bit immediate field contained in the machine instruction.

Addressing Mode Summary

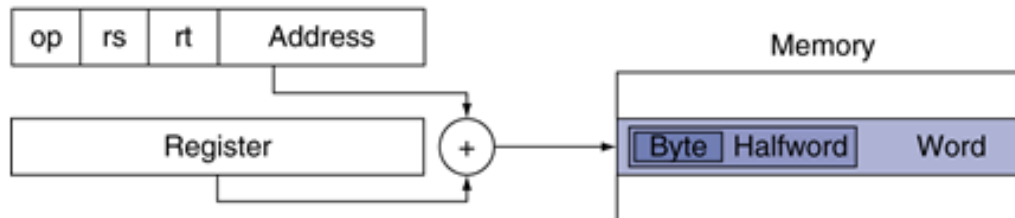
1. Immediate addressing



2. Register addressing

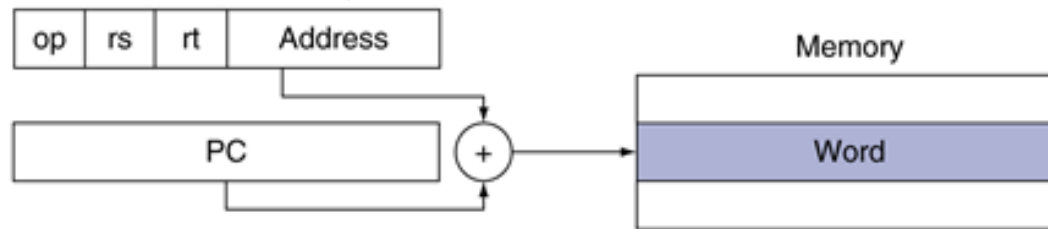


3. Base addressing

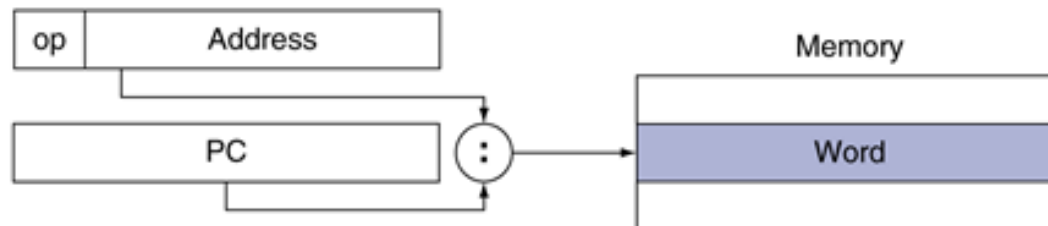


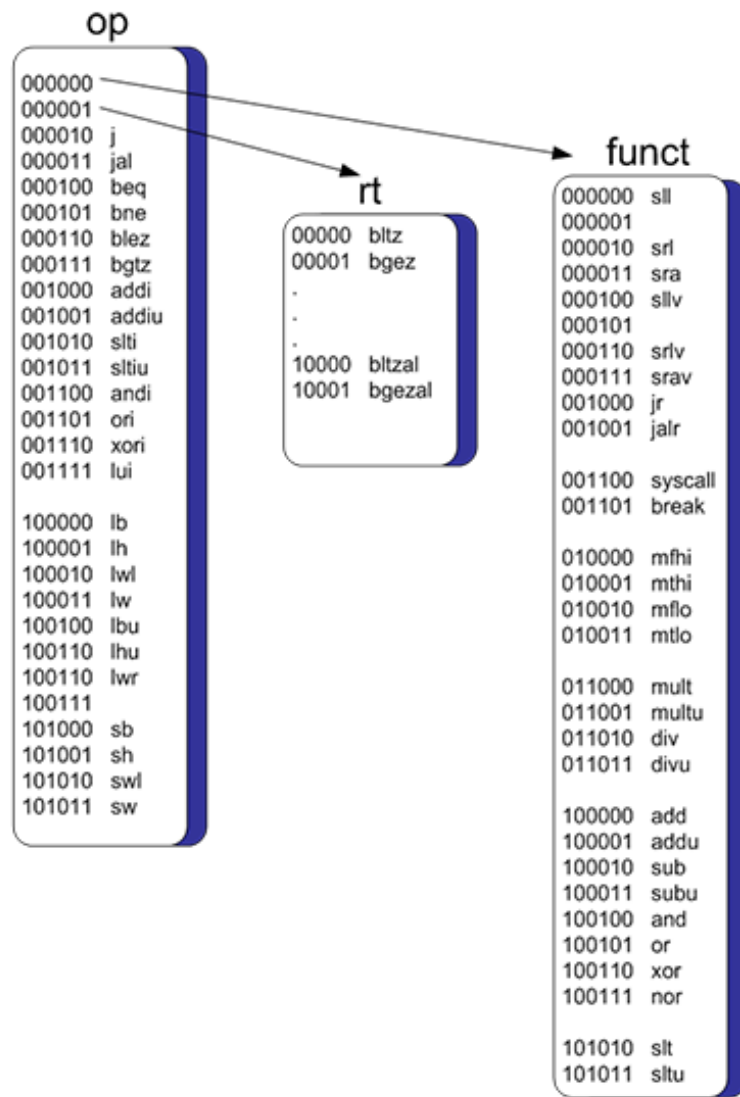
Addressing Mode Summary

4. PC-relative addressing



5. Pseudodirect addressing





Their fixed size and regularity make it easier and faster for the control unit to interpret the machine instructions.

The opcode is always the leftmost 6 bits.

When the opcode is 0, the operation is determined by rt field.

When the opcode is 1, the operation is determined by function code field in the rightmost 6 bits.



Load/Store Architecture

- Compilers that generate code for RISC processors try to maximize and optimize the use of registers
- Only the load and store instructions can access memory operands
- Registers are faster to access than memory
- Less frequently used variables are spilled to memory
- This improves performance and makes the common case fast