Multimedia & Vector Instructions

- IA-32 has Vector or SIMD instructions
  - Images can be represented as matrices of pixels
    - Color & brightness are encoded in each element
    - Multiple pixels can be packed into a single elements
    - Simple arithmetic & logic operations are applied
    - SIMD instructions act on multiple pixels in parallel

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- IA-32 has multimedia extensions (MMX)
  - Multiple data elements are packed into 64-bit quadwords
  - Operands can be in memory or in FPU registers
    - FPU registers correspond to MM0 – MM7
      - Lowermost 64 bits within each 80-bit register are used
    - MMX registers are not managed as a stack
  - Example MMX instructions
    - MOVQ MM0,[EAX] loads 64 bits from memory
    - MOVQ MM3,MM4 copies MM4 into MM3

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- Example MMX arithmetic instructions
  - PADDB MM2,[EBX] add packed bytes
    - adds 8 memory bytes to corresponding bytes in MM2
    - The sums are computed in parallel
    - B suffix indicates 8 bytes
    - W indicates four 16-bit words
    - D indicates two 32-bit doublewords
    - Q indicates single 64-bit quadword
  - Other operations are also available:
    - PSUB
    - PMUL
    - PMADD
    - PAND
    - POR
    - PXOR

Multimedia & Vector Instructions

- Streaming SIMD extensions (SSE)
  - Handle packed 128-bit double quadwords
  - 8 additional 128-bit registers XMM0 to XMM7
  - MOVAPS & MOVUPS transfer between memory and registers
    - PS suffix indicates packed single-precision float values
    - A or U indicates aligned or unaligned (16-bit word aligned)
- Examples:
  - MOVUPS XMM3,[EAX]
    - Copies 4 32-bit floats from memory into XMM3
  - MOVUPS XMM4,XMM5 copies XMM5 into XMM4
  - ADDPS XMM0,XMM1
    - Adds 4 corresponding pairs of 32-bit floats
    - SUBPS, MULPS & DIVPS are also available