Computer Science 605.611

Problem Set 11 Answers

1. The read access delay for an I/O system is defined as the time required for the device to receive and process an I/O request, acquire the requested data and prepare to start transmitting the data. The data transfer rate for an I/O device is defined as the number of bytes per second that it can transmit once the requested data has been acquired.
The read access delay and data transfer rate for two different I/O systems A and B are given the table below:

I/O System	Read access delay	Data transfer rate
A	5 seconds	5120 bytes/sec
B	3 seconds	3072 bytes/sec

Both systems employ an 8-bit bus to transfer I/O data. Each system is used to transfer a series of data blocks each of which contains 15360 data bytes. The read access and data transfer for each block occur sequentially. What is the minimum time between consecutive interrupts on:

a) (3) System A that employs a DMA controller? Minimum time = ___8 seconds___
One interrupt is generated at the conclusion of each block with DMA. The time interval between consecutive blocks on system A is 5 + 15360/5120 = 8 seconds.

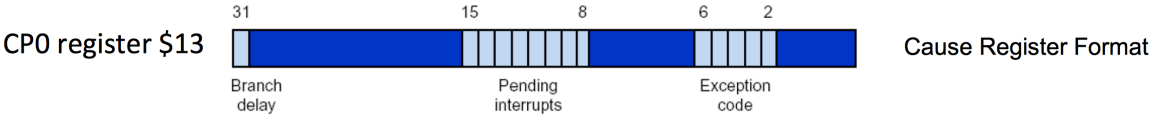
b) (3) System B which, once the data has been acquired, employs interrupt driven I/O using a single I/O port to transfer the data one byte at a time?
Minimum time = _325.52 micro-seconds __
System B takes 3 seconds to acquire the data, which it then transfers one byte at a time with an interrupt after each byte. System B transfers 3072 bytes per second. Therefore the minimum time between consecutive interrupts = 1/3072 = 325.52 micro-seconds.

2. A certain processor consumes 1000 cycles to perform the context switch required to transfer control to the interrupt handler for an I/O device that triggers an interrupt. The interrupt handler takes an additional 10,000 cycles to service the device request. Once the device has been serviced, another 1000 cycles are required to perform the context switch needed to return from the interrupt handler back to the program that was running. The processor's clock rate is 3 GHz.

a) (5) What is the maximum number of requests per second that a device can generate if the system must complete all activity associated with one interrupt before the next interrupt occurs?
Each interrupt requires 1000 + 10000 + 1000 = 12000 cycles. So no more than one request every 12000 cycles can be supported. Hence the upper limit is one request every 12000/3*10^9 = 4 micro-seconds which is 250000 requests per second.

(over)

b) (5) The registers used in managing exceptions and interrupts on our MIPS processor are described in the sub-module "2.2 Interrupt Driven Input/Output" as well as in section A.7 of the textbook.
Write down a short sequence of MIPS assembly language instructions to place just the current exception code right justified into CPU register $t0.
The exception code is contained within the cause register ($13) of coprocessor 0 (CP0).



The following instructions put the exception code into $t0:

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mfc0    $t0,$13         ; copy cause register into $t0
sll     $t0,$t0,25      ; shift out bits on the left of the exception code field
srl     $t0,$t0,27      ; right justify the 5-bit exception code within $t0
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3. (5) A disk rotates at a rate of 7200 revolutions per minute. Seek operations (i.e., moving the access head to a desired track) take on average 20 milli-seconds. Once the access head is on the appropriate track, it takes an average of one half revolution of the disk to get to the beginning of a requested sector. Each track contains 128 sectors and each sector contains 512 bytes of data. How long on average does it take to get the access head to the beginning of a randomly selected sector on a randomly selected track? Express your answer in micro-seconds (not seconds or milli-seconds).
The total average time required to get the access head to the beginning of a randomly selected sector = the average seek time + the average rotational latency
The time required for one revolution is 60/7200 seconds. On average the disk must make ½ rotation to get to a randomly selected sector. So the average time required to rotate to a random sector = ½ * (60/7200) = 4166.67 micro-seconds.
Therefore the total time = 20000 + 4166.67 = 24166.67 micro-seconds.

4. Assume that the 4 data strips (also called data blocks) within a certain stripe on a RAID 5 system are designated B0, B1, B2 and B3. The corresponding parity block P_{old} for this stripe is computed as the cumulative XOR of the 4 data strips within the stripe: P_{old} =B0 ^ B1 ^ B2 ^ B3. Hence each stripe contains a parity block and 4 data blocks. Block B2 is to be overwritten with the new contents designated as $B2_{new}$. None of the parity or data on the disk is currently known or in memory.

a) (5) Write down an expression for the corresponding new parity block P_{new} that requires reading no more than two blocks of any type from the 5 blocks in the stripe.
P_{new} = $B2_{old}$ ^ P_{old} ^ $B2_{new}$ ____ (where B2 $_{old}$ and P_{old} are the two blocks read).

b) (5) Write down a different alternate expression for the new parity block P_{new} if there are no restrictions on the number or type of blocks read from the stripe.
P_{new} = __ B0 ^ B1^ $B2_{new}$ ^ B3_ (B0, B1, and B3 are read. B2new is already known)

5. (10) A disk system is to be constructed using some number of identical disk drives each of which holds 16 terabytes of data. A large database of size 96 terabytes is to be stored on the disk system. What is the minimum number of disks (data disks plus parity disks) that are required for the system if the disk system is a:

a) RAID6 system? 8 disks (96/16 = 6 for data plus 2 for parity)
b) RAID5 system? 7 (containing data and distributed parity)
c) RAID4 system? 7 (6 for data and one for parity)
d) RAID1 system? 12 (6 for the data and 6 for the mirror images)
e) RAID0 system? 6 (6 for the data and none for parity)

6. Sixty percent of the time required to complete a program on a certain computer system corresponds to the execution of code not related to I/O. The remaining 40% of the time required is due to I/O operations. The total time required to complete the entire workload is 480 seconds. This total time is to be reduced by 160 seconds by either improving CPU speed or by improving I/O.

a) (5) If the CPU is made N times as fast as the original CPU, what value of N yields the desired 160-second reduction in the total time consumed by the program? N= _2.25_. Express your answer to two decimal places (dddd.dd).

Reducing the total time by 160 seconds takes it down to 320 seconds.
The speedup S = 480.0/320.0 = 1.5
Let k be the improvement factor for the modified feature (CPU or the I/O system) and let f be the fraction of the workload performed by the modified feature. From Amdahl's law we know that the speedup S = T/ ((1-f) + f/k)T = 1/ ((1-f) + f/k)
So (1-f) + f/k = 1/S = 1/1.5
f/k = 1/S – (1-f)
k = f / (1/S – (1-f)) = 0.6 / (1/1.5 – 0.4) = 0.6 / (2/3 – 4/10) = 0.6 / (20/30 – 12/30) = 0.6 / (8/30) = 18/8 = 2.25
So the CPU would have to be 2.25 times as fast.

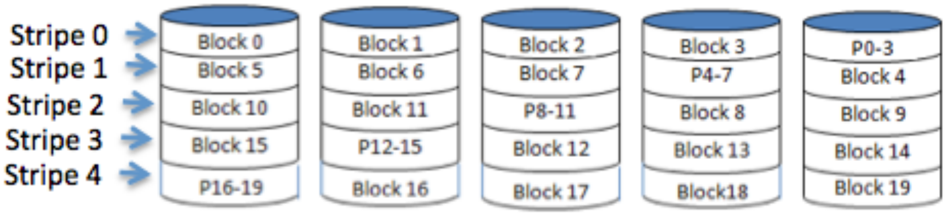
Alternatively, the time due to the execution of the code is 480*0.6 = 288
288/(288-160) = 288/128 = 2.25

b) (5) If instead of making the CPU faster, the I/O is made M times as fast as the original I/O, what value of M yields the desired 160-second reduction in the total time consumed by the program? M= _6_. Express your answer to two decimal places (dddd.dd).

Again k = f / (1/S – (1-f)) = 0.4 / (1/1.5 – 0.6) = 0.4 / (2/3 – 6/10)
= 0.4 / (20/30 – 18/30) = 0.4 / (2/30) = 12/2 = 6
So the I/O would have to be 6 times as fast.

Alternatively, the time due to I/O is 480*0.4 = 192
192/(192-160) = 192/32 = 6.00

7. Shown below is the diagram of a RAID system.

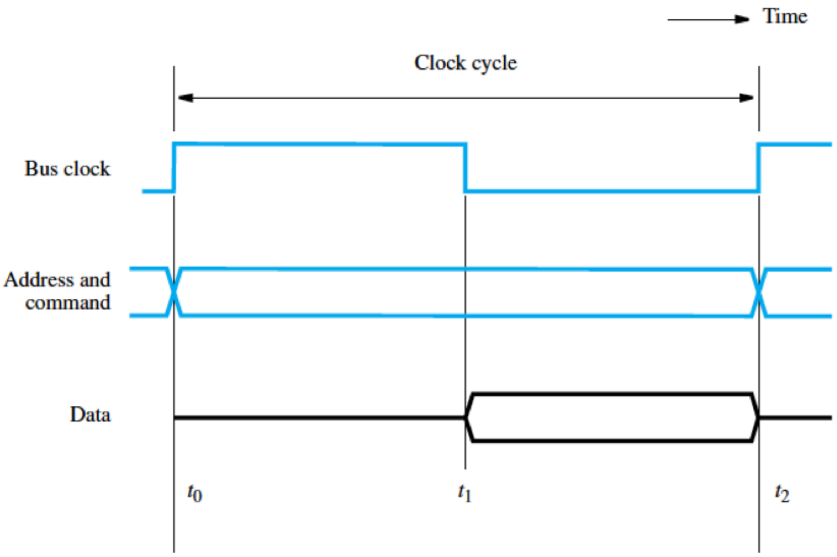


None of the information contained on the disks is currently in memory.

a) (5) What is the minimum number of disk blocks of any type that must be read to determine whether there is an error in some block within stripe 1?
All five blocks within the stripe would have to be read. The parity for the stripe can be computed based on blocks 4, 5, 6, and 7 and the result can be compared with the contents of the parity block P4-7 that was read from the stripe. A non-zero difference indicates that there is an error within the stripe.

b) (9) Block 2 within stripe 0 is to be updated and overwritten, while minimizing the number of blocks that are read and the number of blocks that are written. List the disk blocks of any type that must be read and those that must be written to accomplish this. For example: Block6, Block12, P15-16, etc.
Two blocks must be read: the old block2 and the parity block P0-3. The new parity is computed as old_block2 ^ old P0-3 ^ new block2. Two blocks must then be written: the new block2 and the new P0-3.

8. (10) Shown below is a copy of the simplified timing diagram from module 10 for a read operation over a synchronous bus.



Assume that zero wait states are required and that the bus clock has a 50% duty cycle; a 50% duty cycle means that the high and the low phases of the clock are of equal duration. The bus master takes 1.5 ns to place an address on the address lines. Once a slave device receives an address, it requires 3 ns to decode the address and a maximum of 5 ns to place the requested data on the data lines. The maximum propagation delay (the time required for information to pass from one device to another) on the data lines of the bus is 4 ns. Once the data arrives at the requesting device, it takes 1 ns to transfer the data from the bus into the device's data register. What is the maximum bus clock rate that can be used with this system?

The maximum bus clock rate would be the reciprocal of the minimum time interval from t_0 to t_2. The minimum time for the high phase of the clock is the time for the address to be placed on the address lines, arrive at the slave and be decoded (1.5 + 4 + 3 = 8.5 ns).

The minimum time for the low phase of the clock is the time for the slave to acquire and place the requested data on the data lines, for the data to arrive at the master and for the master to transfer the data into its device register. The total time required for phase two is 5 + 4 + 1 = 10 ns. Since the two phases must be equal (by definition of the 50% duty cycle), they both must be allocated the larger time (10 ns).
So the minimum value for the interval t_0 to t_2 = 2 * 10 ns = 20 ns.
Therefore the maximum bus clock rate is 1/20ns = 50 MHz.

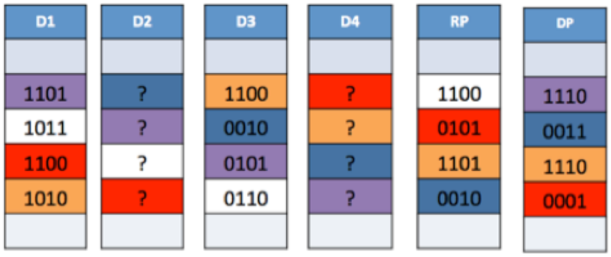
9. (16) Shown below is a RAID-DP (i.e., RAID6 with dual parity) disk system. D1, D2, D3 and D4 are the data disks. RP is the horizontal or row parity disk and DP is the diagonal parity disk. For the purposes of this problem, each strip or block on a disk is a 4-bit pattern. Two of the disks, D2 and D4 have crashed so their data contents are unknown.

Module 10 example set 7 illustrates a technique to reconstruct blocks on up to 2 disks that have failed and are unavailable. Use the scheme described in the example set, substituting exclusive-OR in place of addition, to reconstruct the contents of the two missing disks by determining the 4-bit pattern for each of the following:

D2_blue = _0100_
D2_purple= _1001__
D2_white= _0011__
D2_red= _0001__

D4_red= __1001_
D4_orange= __0101_
D4_blue= __0111_
D4_purple= __1111_

List your answers in the order shown above.



D1	D2	D3	D4	RP	DP
1101	?	1100	?	1100	1110
1011	?	0010	?	0101	0011
1100	?	0101	?	1101	1110
1010	?	0110	?	0010	0001

D4_orange = 1010 ^ 1100 ^ 1101 ^ 1110 = 0101
D2_purple = 1011 ^ 0010 ^ 0101 ^ 0101 = 1001
D4_purple = 1101 ^ 1001 ^ 0101 ^ 1110 = 1111
D2_red = 1010 ^ 0110 ^ 1111 ^ 0010 = 0001
D4_red = 1100 ^ 0001 ^ 0101 ^ 0001 = 1001
D2_blue = 1101 ^ 1100 ^ 1001 ^ 1100 = 0100
D4_blue = 0100 ^ 0010 ^ 0010 ^ 0011 = 0111
D2_white = 1100 ^ 0101 ^ 0111 ^ 1101 = 0011

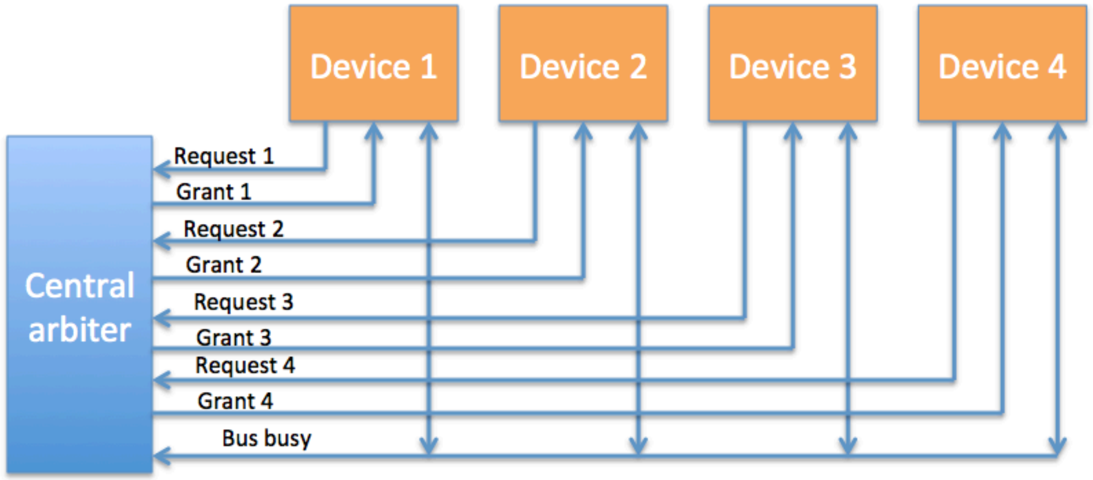
10. Shown below is a bus system with a central arbiter that handles four devices. The device priorities range from highest for Device 4 down to the lowest for Device 1. The arbiter grants access to the highest priority request that is present. Each device has a separate request and grant line. The total available bus bandwidth that must be shared by the devices is 80 MB/s. Each device wants to use 30MB/s of bus bandwidth. All of the devices continuously compete for use of the bus and transmit blocks of the same size for each transaction. If a device is not granted access to the bus, it tries again as soon as the bus is not busy and keeps trying until it gets access. How much bus bandwidth is Device 1 able to use and how much bus bandwidth is Device 3 be able to use if:

a) (5) Bus access is granted strictly on a priority basis?
Device 1 bandwidth = ____0___ Device 3 bandwidth = ___30MB/s_____
Device 4 has the highest priority and gets all of the 30 MB/s bandwidth that it requests. This leaves 80 – 30 = 50 MB/s for the others. Device 3 will get its 30 MB/s leaving only 20 MB/s for Device 2. Device 1 gets no bandwidth since none is leftover.

b) (4) Instead of strict priority, the bus arbiter uses a fairness policy to give each device an equal chance to use the bus?

Device 1 bandwidth = __20 MB/s__ Device 3 bandwidth = __20 MB/s__

With the fair bus arbitration policy, any device that is not given access will have higher priority than the device it lost to until it gets a chance to use the bus. Access to the bus will be granted on a round robin basis. Hence, the 80 MB/s of available bandwidth will be evenly divided between the four devices and each will get (80 / 4) = 20 MB/s of bus bandwidth.


Device 1
Device 2
Device 3
Device 4
Central arbiter
Request 1
Grant 1
Request 2
Grant 2
Request 3
Grant 3
Request 4
Grant 4
Bus busy