

Assignment:

1.2 Note: This is to be a 'best fit' for all the ideas solution set

1.4

1.5

1.7

1.10.1 and 1.10.2

1.14.1; 1.14.2; and 1.14.3

1.2 [5] <§1.2> The eight great ideas in computer architecture are similar to ideas from other fields. Match the eight ideas from computer architecture, “Design for Moore’s Law”, “Use Abstraction to Simplify Design”, “Make the Common Case Fast”, “Performance via Parallelism”, “Performance via Pipelining”, “Performance via Prediction”, “Hierarchy of Memories”, and “Dependability via Redundancy” to the following ideas from other fields:

- a.** Assembly lines in automobile manufacturing
- b.** Suspension bridge cables
- c.** Aircraft and marine navigation systems that incorporate wind information
- d.** Express elevators in buildings
- e.** Library reserve desk
- f.** Increasing the gate area on a CMOS transistor to decrease its switching time
- g.** Adding electromagnetic aircraft catapults (which are electrically-powered as opposed to current steam-powered models), allowed by the increased power generation offered by the new reactor technology
- h.** Building self-driving cars whose control systems partially rely on existing sensor systems already installed into the base vehicle, such as lane departure systems and smart cruise control systems

- a. Performance via Pipelining
- b. Dependability via Redundancy
- c. Performance via Prediction
- d. Make the common case fast
- e. Hierarchy of Memories
- f. Performance via Parallelism
- g. Design for Moore’s Law
- h. Using Abstraction to Simplify Design

1.4 [2] <§1.4> Assume a color display using 8 bits for each of the primary colors (red, green, blue) per pixel and a frame size of 1280×1024 .

- a.** What is the minimum size in bytes of the frame buffer to store a frame?
b. How long would it take, at a minimum, for the frame to be sent over a 100 Mbit/s network?

- a. $\text{bytes/pixel} = (8 \times 3) = 3 \text{ bytes}$
 $\text{pixels/screen} = (1280 \times 1024) = 1,310,720 \text{ pixels}$
 $\text{bytes/screen} = 3 \times 1,310,720 = 3,932,160 \text{ bytes}$
b. $(3,932,160 / 100,000,000) = 0.03932 \text{ seconds}$

1.5 [4] <§1.6> Consider three different processors P1, P2, and P3 executing the same instruction set. P1 has a 3 GHz clock rate and a CPI of 1.5. P2 has a 2.5 GHz clock rate and a CPI of 1.0. P3 has a 4.0 GHz clock rate and has a CPI of 2.2.

- a.** Which processor has the highest performance expressed in instructions per second?
b. If the processors each execute a program in 10 seconds, find the number of cycles and the number of instructions.
c. We are trying to reduce the execution time by 30% but this leads to an increase of 20% in the CPI. What clock rate should we have to get this time reduction?

- a. $\text{instructions/second} = (\text{clock rate} / \text{CPI})$
 $P1 = (3 / 1.5) = 2.0 \times 10^9 \text{ instructions/s}$
 $P2 = (2.5 / 1) = 2.5 \times 10^9 \text{ instructions/s}$
 $P3 = (4 / 2.2) = 1.82 \times 10^9 \text{ instructions/s}$
Processor 2 has the highest number of instructions executed per second
b. $\# \text{ cycles} = (\text{execution time} \times \text{clock rate})$
 $\# \text{ instructions} = (\# \text{ cycles} / \text{CPI})$
 $P1 \text{ cycles} = (10 \times 3) = 3 \times 10^9 \text{ cycles}$
 $P1 \text{ instructions} = (3 \times 10^9 / 1.5) = 2 \times 10^9 \text{ instructions}$
 $P2 \text{ cycles} = (10 \times 2.5) = 2.5 \times 10^9 \text{ cycles}$
 $P2 \text{ instructions} = (2.5 \times 10^9 / 1) = 2.5 \times 10^9 \text{ instructions}$
 $P3 \text{ cycles} = (10 \times 4) = 4 \times 10^9 \text{ cycles}$
 $P3 \text{ instructions} = (4 \times 10^9 / 2.2) = 1.82 \times 10^9 \text{ instructions}$
c. $\text{clock rate} = \# \text{ instructions} \times \text{CPI} / \text{time}$
 $\text{clock rate(A)} = 2 \times 10^9 \times (1.5 \times 1.2) / 0.7 = 5.14 \text{ GHz}$
 $\text{clock rate(B)} = 2.5 \times 10^9 \times (1.0 \times 1.2) / 0.7 = 4.28 \text{ GHz}$
 $\text{clock rate(C)} = 1.82 \times 10^9 \times (2.2 \times 1.2) / 0.7 = 6.75 \text{ GHz}$

1.7 [15] <§1.6> Compilers can have a profound impact on the performance of an application. Assume that for a program, compiler A results in a dynamic instruction count of $1.0E9$ and has an execution time of 1.1 s, while compiler B results in a dynamic instruction count of $1.2E9$ and an execution time of 1.5 s.

a. Find the average CPI for each program given that the processor has a clock cycle time of 1 ns.

b. Assume the compiled programs run on two different processors. If the execution times on the two processors are the same, how much faster is the clock of the processor running compiler A's code versus the clock of the processor running compiler B's code?

c. A new compiler is developed that uses only $6.0E8$ instructions and has an average CPI of 1.1 . What is the speedup of using this new compiler versus using compiler A or B on the original processor?

- CPI = (execution time / (instruction count * clock cycle time))
 Compiler A CPI = $(1.1 / (1 \cdot 10^9 \cdot 1 \cdot 10^{-9})) = 1.1$ instructions/cycle
 Compiler B CPI = $(1.5 / (1.2 \cdot 10^9 \cdot 1 \cdot 10^{-9})) = 1.25$ instructions/cycle
- Comp A Clock Cycle / Comp B Clock Cycle = (# instructions(B) * CPI(B) / (# instructions(A) * CPI(A)) = $(1.2 \cdot 1.25 / 1 \cdot 1.1) = 1.37$ * faster
 Comp A Clock Cycle / Comp B Clock Cycle = $1.25 / 1.1 = 1.136$ * faster
- Depends on the clock cycle time. Assuming a clock cycle time of 1 ns (all run on the same processor):
 execution time = instructions * cycles per instruction * seconds per cycle

Compiler A execution time	Compiler B execution time	New compiler time
1.1s	1.5s	.66s

1.10 Assume a 15 cm diameter wafer has a cost of 12 , contains 84 dies, and has 0.020 defects/cm². Assume a 20 cm diameter wafer has a cost of 15 , contains 100 dies, and has 0.031 defects/cm².

1.10.1 [10] <§1.5> Find the yield for both wafers.

1.10.2 [5] <§1.5> Find the cost per die for both wafers.

- Yield = $1 / (1 + (\text{defects per area} \cdot \text{die area} / 2))^{1/2}$
 die area (15cm) = $\pi \cdot r^2 / 84 = 2.1 \text{ cm}^2$
 die area (20cm) = $\pi \cdot r^2 / 100 = 3.14 \text{ cm}^2$
 Yield(15cm) = $1 / (1 + (0.02 \cdot 2.1 / 2))^{1/2} = .9593$
 Yield(20cm) = $1 / (1 + (0.031 \cdot 3.14 / 2))^{1/2} = .9093$
- Cost per die = cost per wafer / (dies per wafer * yield)
 Cost(15cm) = $12 / (84 \cdot .9593) = .1489$
 Cost(20cm) = $15 / (100 \cdot .9093) = .165$

1.14 Assume a program requires the execution of 50×10^6 FP instructions, 110×10^6 INT instructions, 80×10^6 L/S instructions, and 16×10^6 branch instructions. The CPI for each type of instruction is 1, 1, 4, and 2, respectively. Assume that the processor has a 2 GHz clock rate.

1.14.1 [10] <§1.10> By how much must we improve the CPI of FP instructions if we want the program to run two times faster?

1.14.2 [10] <§1.10> By how much must we improve the CPI of L/S instructions if we want the program to run two times faster?

1.14.3 [5] <§1.10> By how much is the execution time of the program improved if the CPI of INT and FP instructions is reduced by 40% and the CPI of L/S and Branch is reduced by 30%?

1. execution time = (instructions / (CPI * clock rate))
execution time (FP) = $(50 \times 10^6) / (2 \times 10^9) = 2.65 \times 10^{-6}$ seconds
execution time (INT) = $(110 \times 10^6) / (2 \times 10^9) = 5.85 \times 10^{-6}$ seconds
execution time (L/S) = $(80 \times 10^6) / (4 \times 2 \times 10^9) = 1.06 \times 10^{-6}$ seconds
execution time (branch) = $(16 \times 10^6) / (2 \times 2 \times 10^9) = 4.24 \times 10^{-7}$ seconds
total execution time = 9.984 seconds
CPI of FP instructions must improve by more than infinity – impossible
2. $\frac{1}{2} \times$ total execution time = 4.992×10^{-6} seconds
execution time (INT) to achieve that time is $.858 \times 10^{-6}$ seconds
 $5.85 / 0.85$ gives a 6.88 times improvement in CPI of the L/S instructions
3. $((2.65 \times .6) + (5.85 \times .6) + (1.06 \times .7) + (.424 \times .7)) / 9.984$
= runs in 61.49 % of original execution time