

Computer Science 605.611

Problem Set 13

1. a) (5) Show a pair of Intel IA-32 instructions that place the 64-bit two's complement equivalent of the integer -763 (negative 763) into registers EAX and EDX (with the high part in EDX).

763 = 0000 0000 0000 0000 0000 0010 1111 1011 (32 bit representation)

```
MOV  EAX,-763    # populate low part of 2's complement with -763
MOV  EDX,0        # populate upper part of 2's complement with 0
```

b) (5) Show a pair of (i.e., two) SparcV8 instructions that place the 64-bit two's complement equivalent of the integer -763 (negative 763) into registers %o4 and %o5 (with the high part in %o5).

```
set -763, %o4     # populate low part of 2's complement with -763
set 0, %o5        # populate upper part of 2's complement with 0
```

2. A function or procedure that is called usually performs some task and returns control to the caller. Indicate where (i.e., in which register of memory location) the return address is saved by each of the following processor instructions:

a) (4) SparcV8 instruction: `call sqrt`

%o7 (link register)

b) (4) Intel IA-32 instruction: `call sqrt`

ESP – this register points to the top of the return address stack

c) (4) ARM instruction: `BL sqrt`

R14 (the link register)

3. a) (4) Show a MIPS true-op instruction that implements the **nop** synthetic or pseudo-instruction.

```
add 0, 0, 0
```

b) (4) Show a SparcV8 true-op instruction that implements the **nop** synthetic or pseudo-instruction.

```
sethi 0,%g0
```

4. (5) The IEEE-754 single precision and double precision floating point formats provide 7 and 15 decimal digits of accuracy, respectively. How many decimal places are provided by the Intel internal 80-bit extended precision floating point format?

Show how you arrived at your answer.

80-bit extended precision floating point has 63 significand bits.

$$2^{-63} = 1.084 \times 10^{-19}$$

or

$$\log(2^{63}) = 18.965$$

Thus 80-bit extended has 18 decimal bits of accuracy

5. (5) Manually generate (i.e., by hand) the 80-bit extended precision floating point representation of the negative value: -4.87493 on an IA-32 processor. Show your answer as a sequence of hex digits.

$$\text{Floor}(\log_2(4.87493)) = \text{Floor}(2.28) = 2$$

$$4.87493 / 2^2 = 1.2187325$$

$$.2187325 * 2^{63} = 2.01745122405133724942336 \times 10^{18}$$

$$= 2.01745122405133724942336 \times 10^{18} \rightarrow 2017451224051337249$$

$$= 001\ 1011\ 1111\ 1111\ 0110\ 1101\ 0011\ 0011\ 0000\ 1001\ 0100\ 0001\ 1100\ 1000\ 0010$$

0001 (this represents the fraction)

$$\text{Characteristic} = 2 + 16383 = 16385 = 1000000000000001$$

Sign: 1

Integer part: 1

Full binary: 1100 0000 0000 0001 1001 1011 1111 1111 0110 1101 0011 0011 0000

1001 0100 0001 1100 1000 0010 0001

= 0xC0019BFF6D330941C821

6. (5) The following MIPS instruction sequence saves MIPS registers \$2, \$4 and \$6 on the stack:

```
add    $sp,$sp,-12
sw     $2,8($sp)
sw     $4,4($sp)
sw     $6,0($sp)
```

Show a single (i.e., one) complete ARM assembly language instruction that similarly saves ARM registers R2, R4 and R6 on the stack.

R13! is the stack register

Instruction:

STMFD R13! {R2, R4, R6}

7. a) (5) Show one MIPS true-op instruction that has the same effect as the instruction: `LEA EAX,[EBX + 44]` on the Intel IA-32 processor. Use \$8 as the result register and \$9 as the base register in the MIPS instruction.

LEA is short for load effective address, but is essentially just a shift + add operation. Thus an equivalent MIPS operation would be:
addi \$8, \$9, 44

b) (5) Show one ARM true-op instruction that has the same effect as the instruction: `LEA EAX,[EBX + 44]` on the Intel IA-32 processor. Use R4 as the result register and R5 as the base register in the ARM instruction.

Add R5, R4, #44
*****8

8. (5) The following ARM processor instruction: `MVN R2,#3` places a bit pattern into register R2. If the resulting bit pattern is interpreted as a two's complement format signed integer, what signed decimal (i.e., base 10) value does it represent?

MVN moves the 1's complement representation into the result register, thus R2 will contain the 1's complement representation of 3

3 = 0011
Contents of R2 represents: 3 Bit pattern = 0000 0000 0000 0000 0000 0000 0000 0011 or 0x00000003

9. The acronym IBM stands for International Business Machines. What does each of the following acronyms stand for? Each acronym relates to one of the processors described in this course.

- (1) MIPS – Million Instructions Per Second
- (1) ARM – Advanced RISC Machine
- (1) IA-32 – Intel Architecture 32 bit
- (1) Sparc – Scalable Processor Architecture

10. Assume that the MMX registers MM2 and MM4 on an IA-32 processor contain the 64-bit patterns 0xA0A1A2A3A4A5A6A7 and 0xB0B1B2B3B4B5B6B7, respectively. Assume also that the MIPS registers \$2, \$3, \$4 and \$5 contain the following bit patterns:

\$2	\$3	\$4	\$5
0xA0A1A2A3	0xA4A5A6A7	0xB0B1B2B3	0xB4B5B6B7

a) (5) Show, in hex, the contents of register MM2 after the IA-32 instruction `PADB MM2,MM4` is executed. Result in hex = 0x70727476787A7C7E

0xA0A1A2A3A4A5A6A7 = 1010 0000 1010 0001 1010 0010 1010 0011 1010 0100
1010 0101 1010 0110 1010 0111

0xB0B1B2B3B4B5B6B7 = 1011 0000 1011 0001 1011 0010 1011 0011 1011 0100
1011 0101 1011 0110 1011 0111

No carry between bytes gives simplifications:

A + B = 1010 + 1011 = 0111 = 7

0 + 0 = 0000

1 + 1 = 0001 + 0001 = 2 = 0010

2 + 2 = 4 = 0100

3 + 3 = 6 = 0110

4 + 4 = 8 = 1000

5 + 5 = A = 1010

6 + 6 = C = 1100

7 + 7 = E = 1110

0xA0A1A2A3A4A5A6A7 + 0xB0B1B2B3B4B5B6B7 =
0x70727476787A7C7E

b) (5) Show, **in hex**, the contents of MIPS registers \$2 and \$3 after the following two MIPS instructions are executed:

addu \$2,\$2,\$4

addu \$3,\$3,\$5

\$2 in hex = 0x51535556 \$3 in hex = 0x595B5D5E

0xA0A1A2A3 + 0xB0B1B2B3 =

```
      1010 0000 1010 0001 1010 0010 1010 0011
+     1011 0000 1011 0001 1011 0010 1011 0011   =
-----
      0101 0001 0101 0011 0101 0101 0101 0110
= 0x51535556
```

0xA4A5A6A7 + 0xB4B5B6B7 =

```
      1010 0100 1010 0101 1010 0110 1010 0111
+     1011 0100 1011 0101 1011 0110 1011 0111   =
-----
      0101 1001 0101 1011 0101 1101 0101 1110
=0x595B5D5E
```

11. A machine instruction stores the 32-bit contents of a register into memory at address 0x80084004. Show the contents of the single byte at location 0x80084006 if the store instruction is executed on:

a) (5) an IA-32 processor and the register that is stored contains 0xFEEDBEEF ?
Contents of byte in hex = 0xEF

IA-32 is little-endian (not like MIPS)
Last 2 hex's are the byte at 0x80084006 -> 0xEF

b) (5) a SparcV8 processor and the register that is stored contains 0xA1C0FFEE ?
Contents of byte in hex = 0xA1

SparcV8 is big-endian (like MIPS)
First 2 hex's are the byte at 0x80084006 -> 0xA1

12. a) As described in module 13, what is the maximum number of CPU registers contained in each of the following processors?

- (2) IA-32 – contains only 8 general purpose registers
- (2) ARM – 16 registers (R0-R15)
- (4) Sparc_v8 – There can be up to 32 register windows, which each contain 24 registers = 768 registers, as well as 8 global registers = 774 registers.

b) The PC (program counter) is to be incremented by 16 using a single ADD instruction. For each of the processors listed below, indicate whether the processor can or cannot accomplish this.

- (2) ARM processor – yes
- (2) MIPS processor – no
- (2) IA-32 processor – yes
- (2) Sparc V8 processor – no