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JHU Computer Architecture
Problem Set 1
Fall 2019

Computer Science 605.611

Problem Set 1

1. (4) The average CPI (cycles per instruction) for a certain program is 1.6. If the native MIPS rating for the program is 12.5, what is the corresponding CPU clock cycle time (i.e., the clock period) in units of nano-seconds (i.e., 10^-9 seconds)?

$$MIPS = \frac{Clock\ Rate}{CPI\ x\ 10^6}$$

$$12.5 = \frac{Clock\ Rate}{1.6\ x\ 10^6}$$

$$Clock\ Rate = 7.813\ x\ 10^{-6}$$

$$Cycle\ Time = 7813\ nanoseconds$$

2. Assume that MIPS instructions are processed in only 2 phases (a fetch phase and an execute phase). Each phase takes one clock cycle and, when possible, the fetch phase of one instruction is overlapped with the execute phase of another instruction. Consider the following instruction sequence:

```
lui     $2,0x4000       ; put the address 0x40000000 into register $2
lw      $8,4($2)        ; load the contents of a memory word into $8
lw      $9,8($2)        ; load the contents of another memory word into $9
add     $9,$9,$8        ; compute the sum of the two words
sw      $9,12($2)       ; store the sum into a third memory word
```

What is the total number of clock cycles required to execute this sequence of five instructions on:

a) (4) a MIPS system with a von Neumann architecture?

For each of the 5 instructions, the von Neumann architecture takes 2 phases, one to fetch the instruction, and one to execute the instruction. Therefore, this block of instructions takes 10 cycles.

b) (4) a MIPS system with a Harvard architecture?

The Harvard architecture takes the same number of phases as the von Neumann architecture, but can overlap the fetch and store/read phases into one phase. Since there are 4 store/read operands in the block, the Harvard architecture should save 4 clock cycles by doing fetch and store/read at the same time, so the block would be reduced to 6 clock cycles.

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3. (4) Which is more likely to adhere to a load/store architecture: a RISC processor or a CISC processor? Explain your answer.

A RISC processor is more likely than a CISC processor to adhere to a load/store architecture. This is because the instructions in a RISC processor are generally simpler instructions, specifically one instruction per cycle. These simple instructions are more suited to a load/store architecture. CISC instructions can generally reference memory, therefore are less likely to use a load/store architecture, as that would be inefficient for the CISC processor.

4. A certain program runs on a MIPS processor executing a total of 7 million instructions. The CPU clock rate is 4 GHz and the average CPI for the program is 2.5.

a) (3) What is the CPU clock cycle time?

$$Clock\ Cycle\ Time = \frac{1}{Clock\ Rate}$$

$$Clock\ Cycle\ Time = \frac{1}{4 * 10^9}$$

$$Clock\ Cycle\ Time = 2.5 * 10^{-10}\ s = .25\ ns$$

b) (4) What is the execution time required for the program? Express your answer in micro-seconds.

$$CPU\ Time = CPU\ CLock\ Cycles * Clock\ Cycle\ Time$$
$$= \#\ Instructions * CPI * Clock\ Cycle\ Time$$

$$CPU\ Time = 7{,}000{,}000 * 2.5 * (2.5 * 10^{-10})$$

$$CPU\ Time = .004375\ s = 4375\ \mu s$$

c) (4) What is the numeric value for the expression: clock_rate / (CPI*10^6) for this program?

$$\frac{Clock\ Rate}{(CPI * 10^6)} = \frac{4 * 10^9}{(2.5 * 10^6)} = 1600$$

d) (4) Evaluate the expression IC / (execution_time*10^6) for this program (where IC is the instruction count).

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$$\frac{IC}{(execution\ time * 10^6)} = \frac{7{,}000{,}000}{(0.004375 * 10^6)} = 1600$$

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5. (5) The table below shows the number of clock cycles required to execute various types of instructions on a version of our MIPS processor:

Instruction type	Cycles consumed by the instruction
R-type	4
lw	5
sw	4
beq	3
j	3

A certain program that executes on this version of the processor executes 782000 R-type instructions, 43506 lw instructions, 36897 sw instructions, 21300 beq instructions and 7200 j (jump) instructions.
If the native MIPS rating for the program is 448, what is the corresponding CPU clock rate?

$$Avg\ CPI = \frac{\sum instruction\ type * \#\ cycles}{\#\ instructions}$$

$$CPI = \frac{(782000 * 4) + (43506 * 5) + (36897 * 4) + (21300 * 3) + (7200 * 3)}{782000 + 43506 + 36897 + 21300 + 7200}$$

$$CPI = 4.02$$

6. (10) A program that executes forty million instructions runs on a uni-processor system with a fixed clock rate of 3.333 GHz. All instructions are executed one at a time and each instruction requires an integral (i.e., whole) number of clock cycles. The average CPI rating for the instructions is 3 cycles per instruction. What is the speedup for the program obtained by reducing the average CPI from 3 down to 2?

$$Speedup = \frac{CPI_x}{CPI_y}$$

$$Speedup = \frac{3}{2} = 1.5$$

7. A number of instructions from five different instruction classes are executed for a program that runs on a certain processor. The five classes along with the number of instructions executed from each class and the CPI for each class are shown in the table below:

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Class	Instruction type	CPI	Millions of instructions executed
A	R-type	8	20
B	lw	12	18
C	sw	10	12
D	beq	6	10
E	j	4	6

a) (5) What is the average CPI for the program?

$$Avg\ CPI = \frac{\sum instruction\ type * \#\ cycles}{\#\ instructions}$$

$$CPI = \frac{(20 * 8) + (18 * 12) + (12 * 10) + (10 * 6) + (6 * 4)}{20 + 18 + 12 + 10 + 6}$$

$$CPI = 8.79$$

b) (10) If each beq instruction takes 12 nano-seconds to execute, what is the total execution time for the program?

$$CPU\ Time = CPU\ Clock\ Cycles * Clock\ Cycle\ Time$$

$$CPU\ Time_{beq} = 12 * 10^{-9} = 6 * Clock\ Cycle\ Time$$

$$Clock\ Cycle\ Time = 2 * 10^{-9}$$

$$CPU\ Time_{tot} = (20 + 18 + 12 + 10 + 6) * 10^{6} * 2 * 10^{-9}$$

$$CPU\ Time_{tot} = .132\ s$$

c) (5) Assume that you have the option of improving only one of the instruction classes. If the improvement is by a factor of 2, which class should be chosen for improvement to achieve the greatest speedup for the program?

$$CPU\ Time\ \alpha\ CPU\ Clock\ Cycles\ \ (where\ \alpha\ represents\ "is\ proportional\ to")$$

$$CPU\ Time_{r-type}\ \alpha\ 8 * 20\ \alpha\ 160$$

$$CPU\ Time_{lw}\ \alpha\ 12 * 18\ \alpha\ 216$$

$$CPU\ Time_{sw}\ \alpha\ 10 * 12\ \alpha\ 120$$

Since lw is the operation that takes the longest, this is the instruction class that should be targeted with an improvement factor, since this will achieve the greatest speedup for the program

d) (10) If only the class A instructions are improved in the original program, what improvement factor for class A is required to yield a speedup of 1.2608695 for the program?

$$CPI = 8.79$$

$$CPI_{improved} = \frac{CPI}{improvement\ factor} = 6.971379$$

$$CPI_{improved} = 6.971379 = \frac{(20 * x) + (18 * 12) + (12 * 10) + (10 * 6) + (6 * 4)}{20 + 18 + 12 + 10 + 6}$$

$$x = 2.005553 = CPI_{a,improved}$$

$$improvement\ factor = \frac{CPI}{CPI_{improved}} = \frac{8.79}{2.005553} = 4.382831$$

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8. The sub-module on Computer performance metrics defines the geometric mean and the harmonic mean as alternatives to the arithmetic mean as techniques for comparing CPU performance. Some processors, especially those used in laptops or mobile devices, are able to throttle their speed as a means of conserving power and extending battery charge. Suppose that such a processor runs in the slower low power mode executes 2,890,000 instructions for a program in 14.45 milli-seconds. Next the processor switches to the higher speed mode and executes the same program again in only 7.225 milli-seconds. Answer the following questions and show how you obtained your answer for each:

a) (4) What is the MIPS rating for the first execution of the program?

$$MIPS = \frac{instruction\ count}{execution\ time}$$

$$MIPS = \frac{2890000}{14.45 * 10^{-3}} = 2 * 10^8$$

b) (4) What is the MIPS rating for the second execution of the program?

$$MIPS = \frac{instruction\ count}{execution\ time}$$

$$MIPS = \frac{2890000}{7.225 * 10^{-3}} = 4 * 10^8$$

c) (4) What is the arithmetic mean of the MIPS ratings for the two executions of the program?

$$Arithmatic\ mean = \frac{\sum vals}{\#\ vals} = \frac{4+2}{2} = 3 * 10^8$$

d) (4) What is the geometric mean of the two MIPS ratings?

$$geometric\ mean = \sqrt[\#\ vals]{\prod vals} = \sqrt[2]{2 * 4} = 2.83 * 10^8$$

e) (4) What is the harmonic mean of the two MIPS ratings?

$$harmonic\ mean = \frac{\#\ vals}{\sum_{i=1}^{\#\ vals} val_i} = \frac{2}{\frac{1}{2} + \frac{1}{4}} = 2.67 * 10^8$$

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f) (4) What is the MIPS rating for the two executions of the program if it is computed based on the total combined number of instructions in the two executions of the program and on the total combined times consumed for the two executions of the program?

$$MIPS = \frac{instruction\ count}{execution\ time}$$

$$MIPS = \frac{2890000 * 2}{14.45 * 10^{-3} + 7.225 * 10^{-3}} = 2.67 * 10^{8}$$

(same as the harmonic mean)