Module 11 Example Set 4

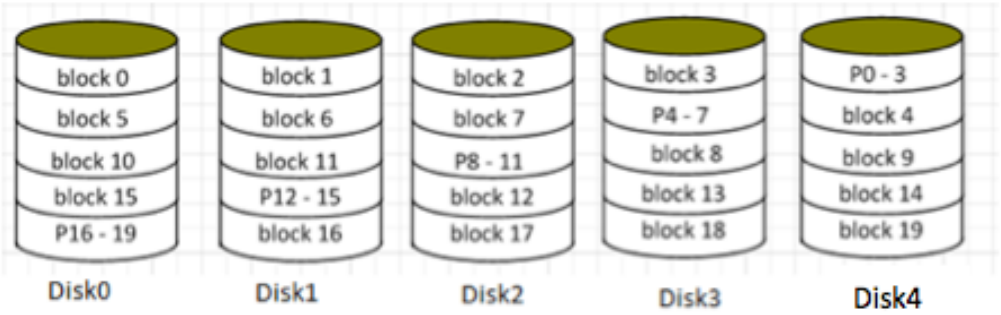
1. An Intel 80386 processor employs a bus cycle consisting of 2 clock cycles to access memory (i.e. to read or write to memory) over a 32-bit non-multiplexed data bus. If this system is driven by a 33-MHz clock, what is the bus bandwidth for:

a) a zero-wait state memory b) a one-wait state memory

a) A 33MHz clock rate corresponds to a cycle time of 30ns. With zero wait states the memory cycle time is 2*30ns=60ns. This corresponds to a bus bandwidth of 4bytes/60ns or 66.67 million bytes per second.

b) With one wait state the memory cycle time is 90ns which corresponds to a bus bandwidth of 4bytes/90ns = 44.44 million bytes per second.

2. Consider the following RAID5 system that uses a simple bit-wise XOR parity scheme:



Suppose that disk2 fails and is replaced by a new blank disk which is to be written with the information that had been on the original disk2.

a) Write down an expression for the parity block and for each of the four data blocks that should be written to the new disk2.

P8-11 = _____block10 XOR block11 XOR block8 XOR block9_____
Block2 = ____block0 XOR block1 XOR block3 XOR P0-3___
Block7 = ____ block5 XOR block6 XOR block4 XOR P4-7_____
Block12 = ___ block15 XOR block14 XOR block13 XOR P12-15_____
Block17 = ___ block16 XOR block18 XOR block19 XOR P16-19___

b) Assume that a disk read or write operation takes T time units and that the time to compute the XOR of two or more strips is also T time units. What is the minimum total number of time units required to reconstruct the complete new disk2 image? That is, if the minimum total time required to reconstruct disk2 is N*T, what value is N?

Blocks on separate disks can be read in parallel (T units since each block is read from a different disk), the XOR takes T units (they are done in parallel), then the reconstructed block is written to disk2 (T units). Therefore a minimum of 3T units are required to reconstruct and write each of the missing blocks. Hence a total of 5*3T = 15T is required. So N=15.

3. Explain which type of bus (synchronous or asynchronous) would be most appropriate for handling communications between the CPU and:
a) a mouse – **an asynchronous bus would work best in this case since the input from the mouse occurs at unpredictable times and only a small amount of data is transmitted by the mouse.**

b) a memory controller – **information must be transmitted between memory and the CPU at a relatively high rate to keep the CPU from stalling. Synchronous buses avoid the overhead of the handshake signals used with an asynchronous bus and so would be better in this case.**

4. Explain whether bus skew is more of a problem for
a) serial bus or for a parallel bus – **this would be more of a problem for parallel buses, since all of the bits within a byte or word would be sent at the same time over separate pathways. The difference in the travel time for the various bits would have to be below a specified value if the information content is to be correctly interpreted. With a serial bus there would only be one pathway over which all of the bits travel one after the other.**

b) a synchronous bus or for an asynchronous bus – **with a synchronous bus, each step in the transaction is expected to occur after at a specific time, but for the asynchronous bus handshake signals are exchanged to insure that each step has completed before the next step begins. Hence bus skew would be more of a problem for the synchronous bus since differences in the travel time between the bits that are transmitted could violate the fixed bus schedule. With the asynchronous bus, there is no preset schedule- the handshake signals control the progress of the transaction.**