Computer Science 605.411

Final Example Set 4

1. How could performing memory-mapped I/O on an IA-32 processor cause data to be missed when used in conjunction with a data cache?

If the memory block that contains the device status and data registers is brought into the data cache, thereafter any references to those registers would obtain possibly stale information from the cache rather than current data from the actual device register. Accesses to the cache made by I/O devices do not go through the cache, so the CPU may read information from cache that falsely indicates the current state of the I/O device.

2. Which of the following processors employs port-mapped I/O?

a) SparcV8
b) ARM
[✓ c) IA-32]
d) MIPS

3. How does the ARM exception vector table differ from the trap vector table used on the SparcV8.

The ARM exception vector table begins at address 0 and contains 7 entries (one for each of the seven exception types). Each 4-byte entry contains an instruction that transfers control to a routine designed to handle the particular type of exception.
The SparcV8 trap table is located in memory at the address indicated by the contents of the trap base register (TBR). The trap type (tt) field within the TBR indicates the nature of the trap and identifies one of 256 entries, each of which is four words in size and contains the first 4 instructions of the corresponding trap handling routine.

4. How does the trap vector table used on the SparcV8 differ from the interrupt vector table used on an IA-32 processor?

The IA-32 interrupt vector table typically resides at address 0 in RAM and contains 256 entries each of which is 4 bytes in size. Each entry contains the address of the routine designed to handle the particular type of interrupt.
The SparcV8 trap table is located in memory at the address indicated by the contents of the trap base register (TBR). The trap type (tt) field within the TBR indicates the nature of the trap and identifies one of 256 entries, each of which is four words in size and contains the first 4 instructions of the corresponding trap handling routine.

5. What is the purpose of the LDMIA instruction on the ARM processor?
This instruction reads multiple words from memory into a specified list of registers. A base register contains the beginning address of the block of memory words and is incremented by 4 after each word is transferred.

6. What is the LOOP instruction on an IA-32 processor?
This instruction decrements the count register, tests the result and branches to the indicated destination if the count register does not contain zero.

7. Can an IA-32 processor only perform port-mapped I/O?
IA-32 processors can perform memory-mapped as well as port-mapped I/O.

8. What is the purpose of the "save" instruction on a SparcV8 processor?
The save instruction causes the register window to slide to reveal a new group of 24 registers. The first 8 registers (the 'in' registers i0 through i7) overlap with the 'out' registers o0 through o7 of the previous window. The next 8 register in the window are new local registers l0 through l7. The third group of 8 registers are the out registers (o0 through o7) for the current window.
The same 8 global registers are shared by all register windows. The save instruction can also allocate stack space by decrementing the stack pointer by an specified amount.

9. What value will be in the PC when an ARM instruction whose address is 0x80040600 is executed?
Due to the 3-stage ARM pipeline, when an instruction at address A is fetched, the PC is incremented to A+4, then the execution of the instruction begins. Before the execution of the instruction completes, the next instruction is fetched from A+4 and the PC is incremented by 4 to A+8. Hence, when an instruction at address 0x80040600 executes, the PC will contain 0x80040600 +8 = 0x80040608.

10. Explain how the ARM beq instruction behaves differently on the ARM processor compared to how the MIPS beq instruction behaves on the MIPS processor.
The ARM beq instruction employs a 24-bit two's complement displacement that is shifted left 2 bits, sign-extended to 32 bits and added to the updated PC to obtain the branch target address. The branch is taken if the condition codes = 0000.
The MIPS beq instruction employs a 16-bit two's complement displacement that is shifted left 2 bits, sign-extended to 32 bits and added to the updated PC to obtain the branch target address. The branch is taken if the zero flag = 1.