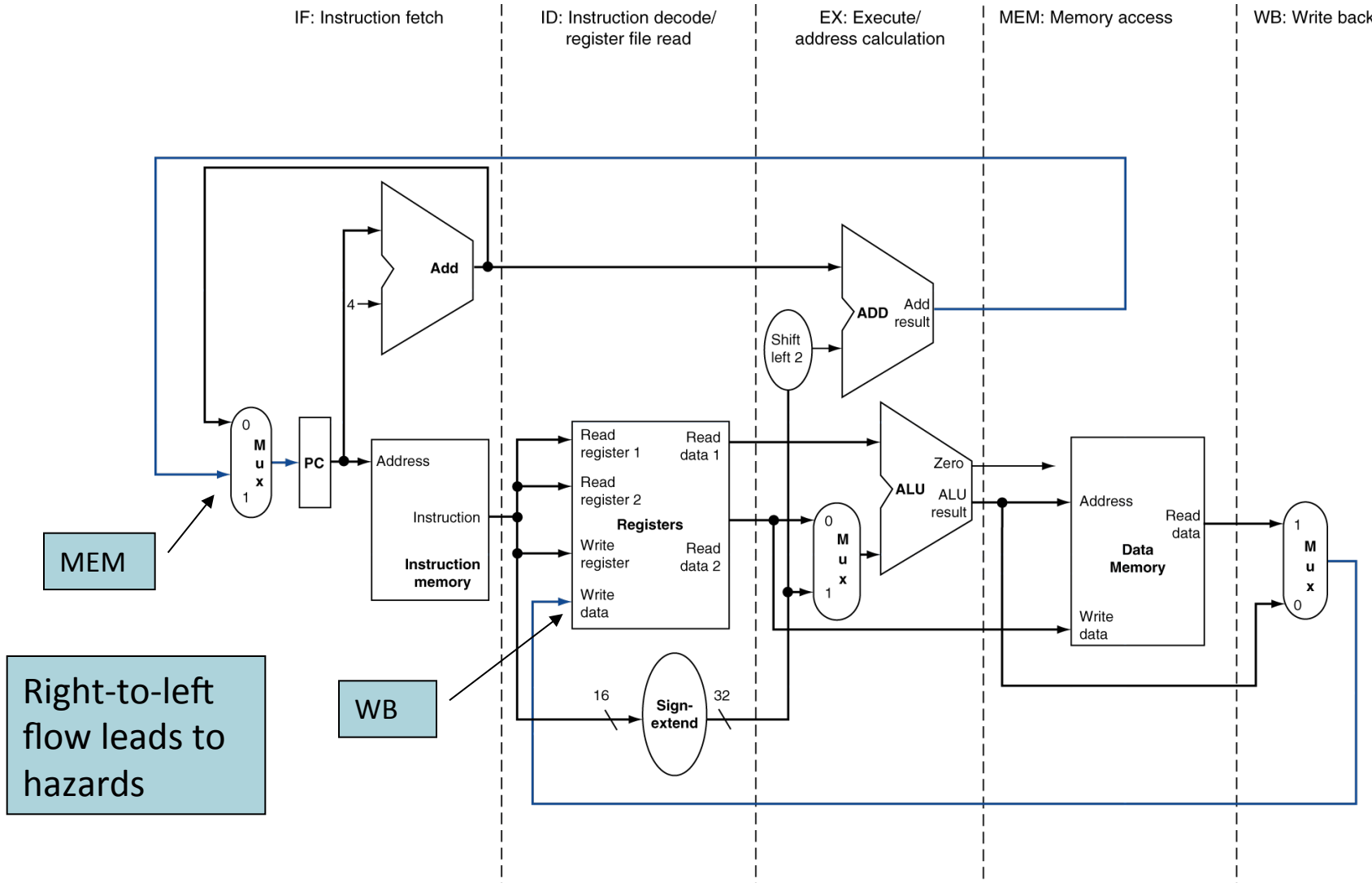


IF: Instruction fetch

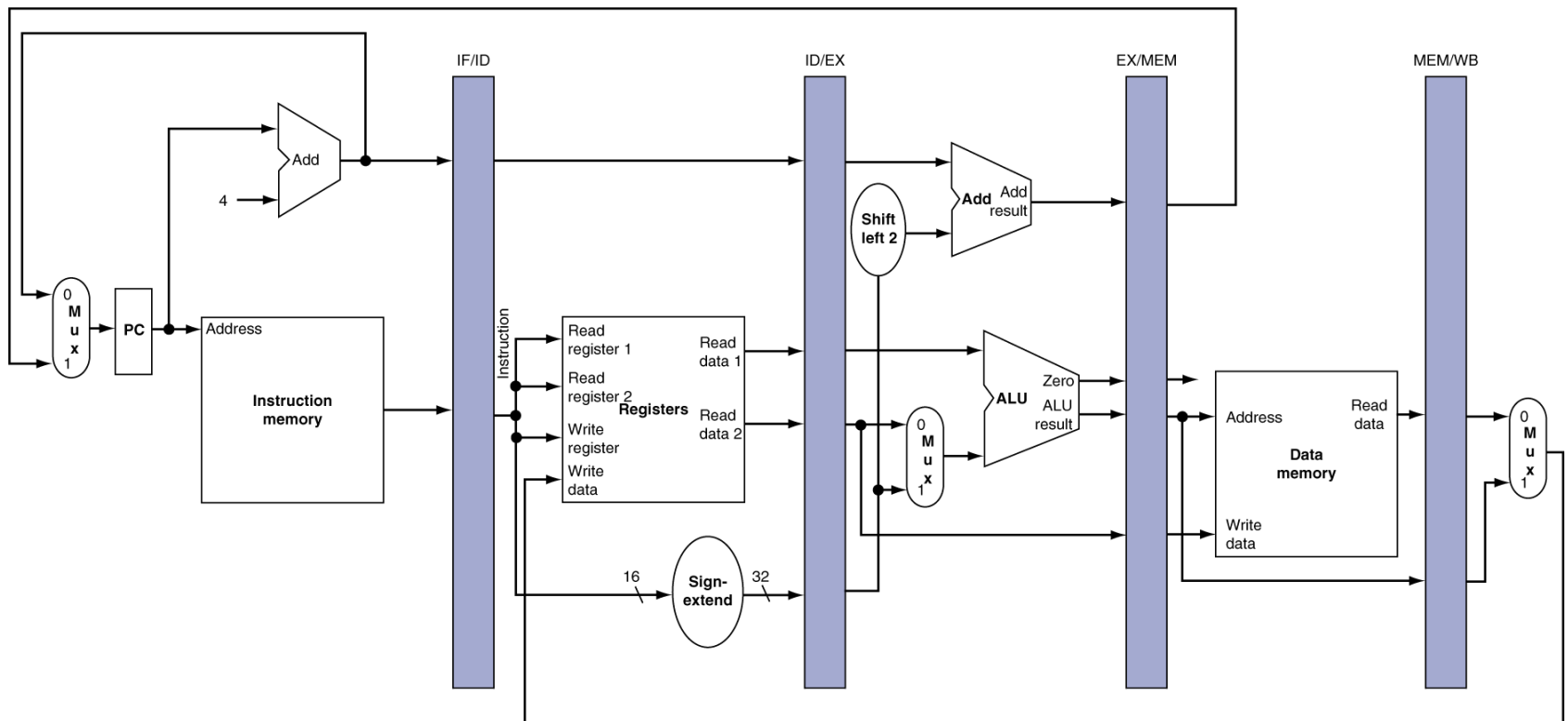
ID: Instruction decode/
register file readEX: Execute/
address calculation

MEM: Memory access

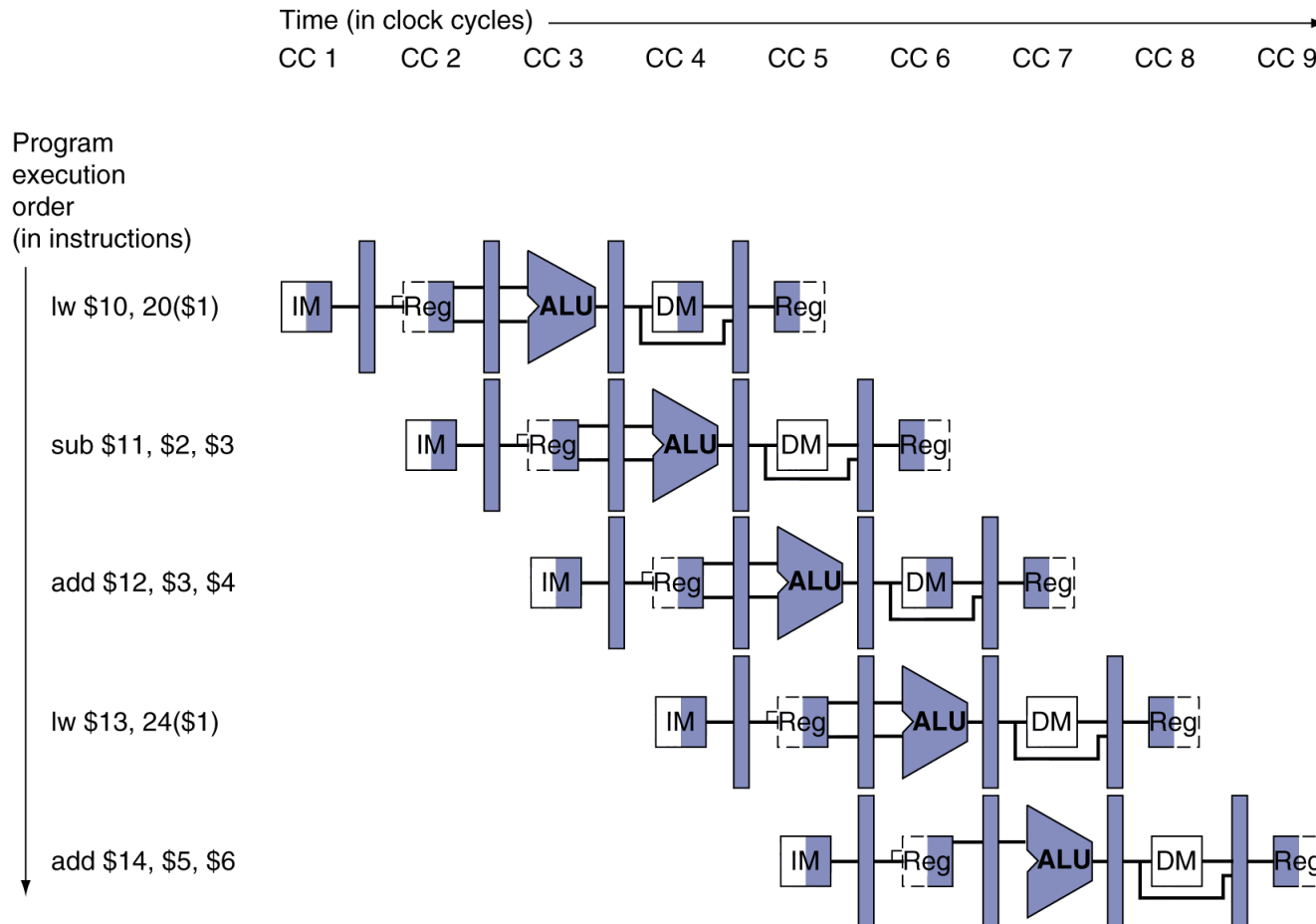
WB: Write back



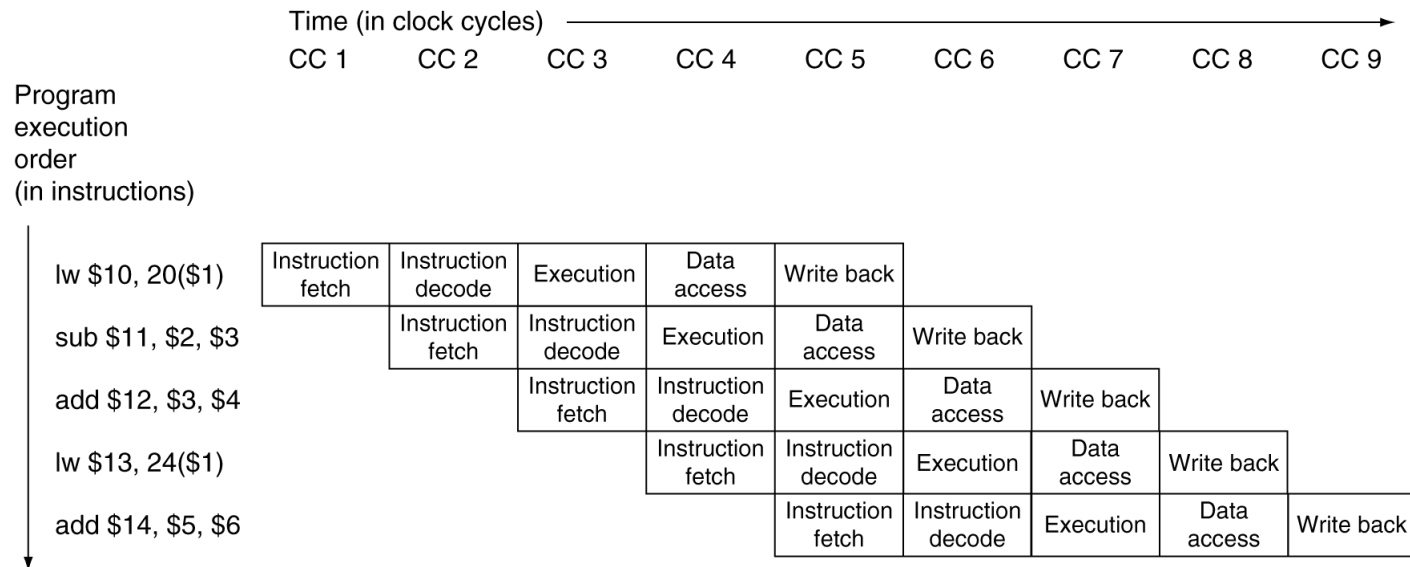
- Need registers between stages
 - To hold information produced in previous cycle



■ Form showing resource usage

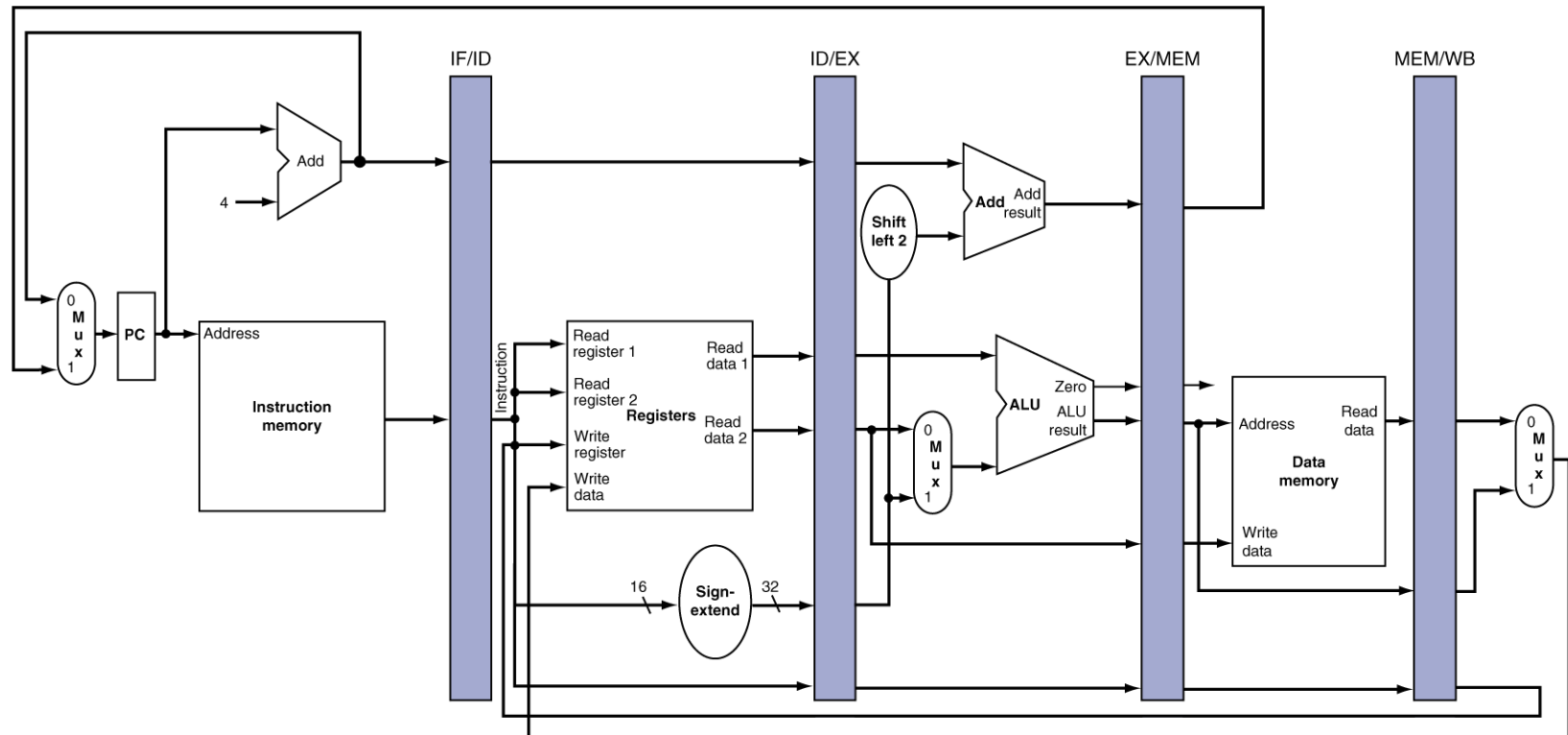


■ Traditional form

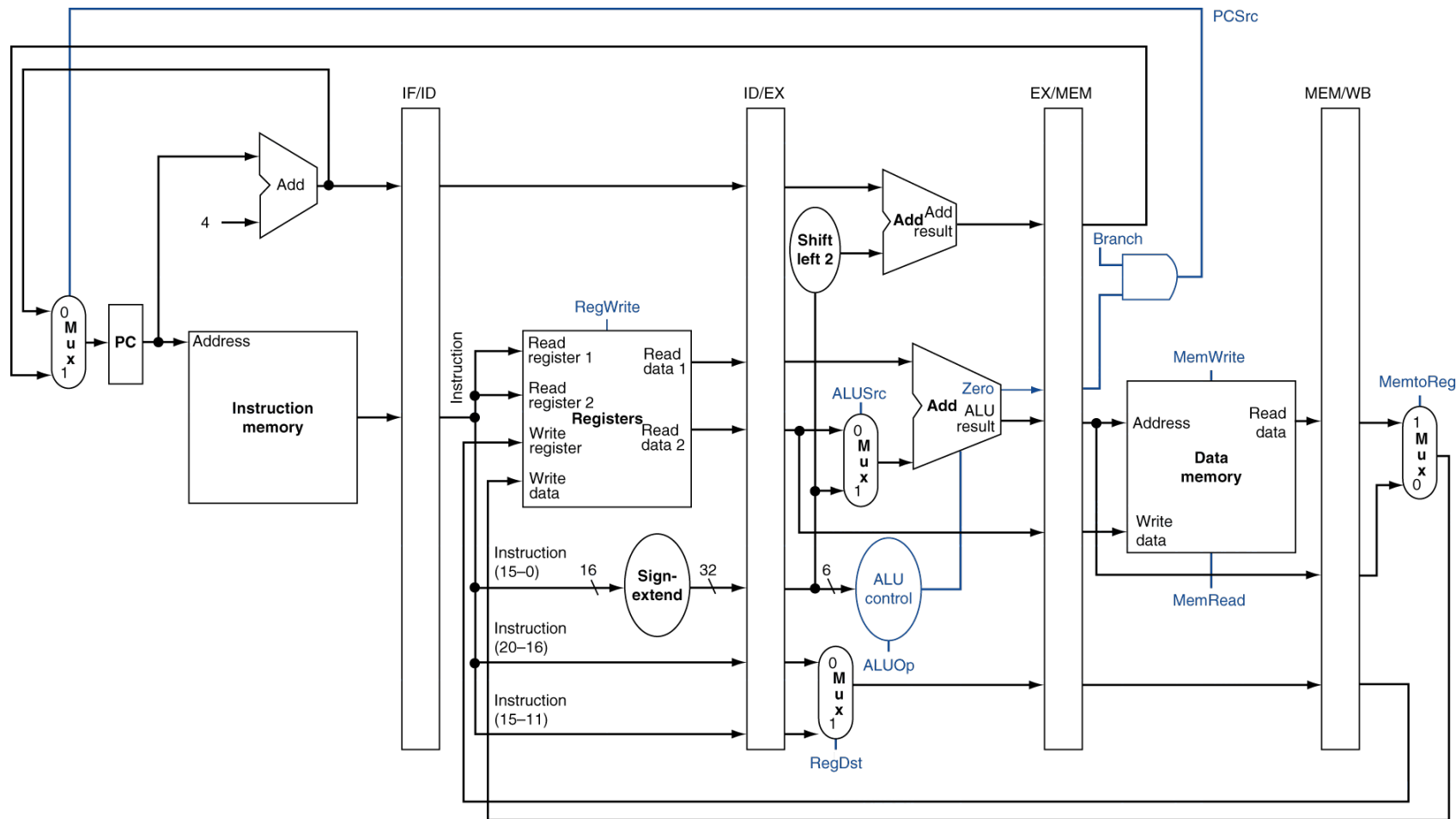


State of pipeline in a given cycle

add \$14, \$5, \$6	lw \$13, 24 (\$1)	add \$12, \$3, \$4	sub \$11, \$2, \$3	lw \$10, 20(\$1)
Instruction fetch	Instruction decode	Execution	Memory	Write-back



Pipelined Control



- Control signals derived from instruction
 - As in single-cycle implementation

