Sparc V8 Overview

- **SPARC** stands for **S**calable **P**rocessor **Arc**hitecture.
- developed by Sun Microsystems in the 1980s.
- based on the RISC II designed at UC Berkeley in early 1980s
- "Scalable" from embedded systems to servers
- RISC design that shares many features with the MIPS system
- There are some major differences between Sparc V8 & MIPS
- Sparc V8 is the only version examined here

Sparc V8 Overview

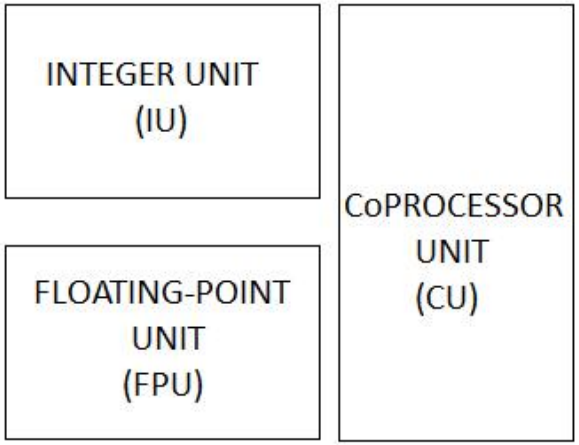
- Features Shared with MIPS:
  - 32-bit registers and addresses
    - Register 0 is hardwired to 0
  - Byte-addressable memory
    - 8-bit bytes, 16-bit halfwords and 32-bit words
  - Load/store architecture
  - Enforces memory alignment
  - Employs big-endian memory storage order
  - Delayed branches
  - Passes arguments via registers
    - Using stack when needed

Sparc V8 Overview

- Features that differ from MIPS:
  - May have hundreds of registers
  - Registers are grouped into “windows”
    - 32 registers are visible at one time
    - Windows slide and overlap to pass arguments
  - Branch delay slot can be “annulled”
  - Has next PC (NPC) as well as PC (program counter)
    - PC points to current instruction
    - NPC points to instruction to be executed next
  - Instructions can set condition codes or not

Sparc V8 Overview

- Sparc V8 Organization



  - Units have separate register sets
  - Units operate in parallel
  - FPU has 32 floating point registers (not windowed)