DMA Devices

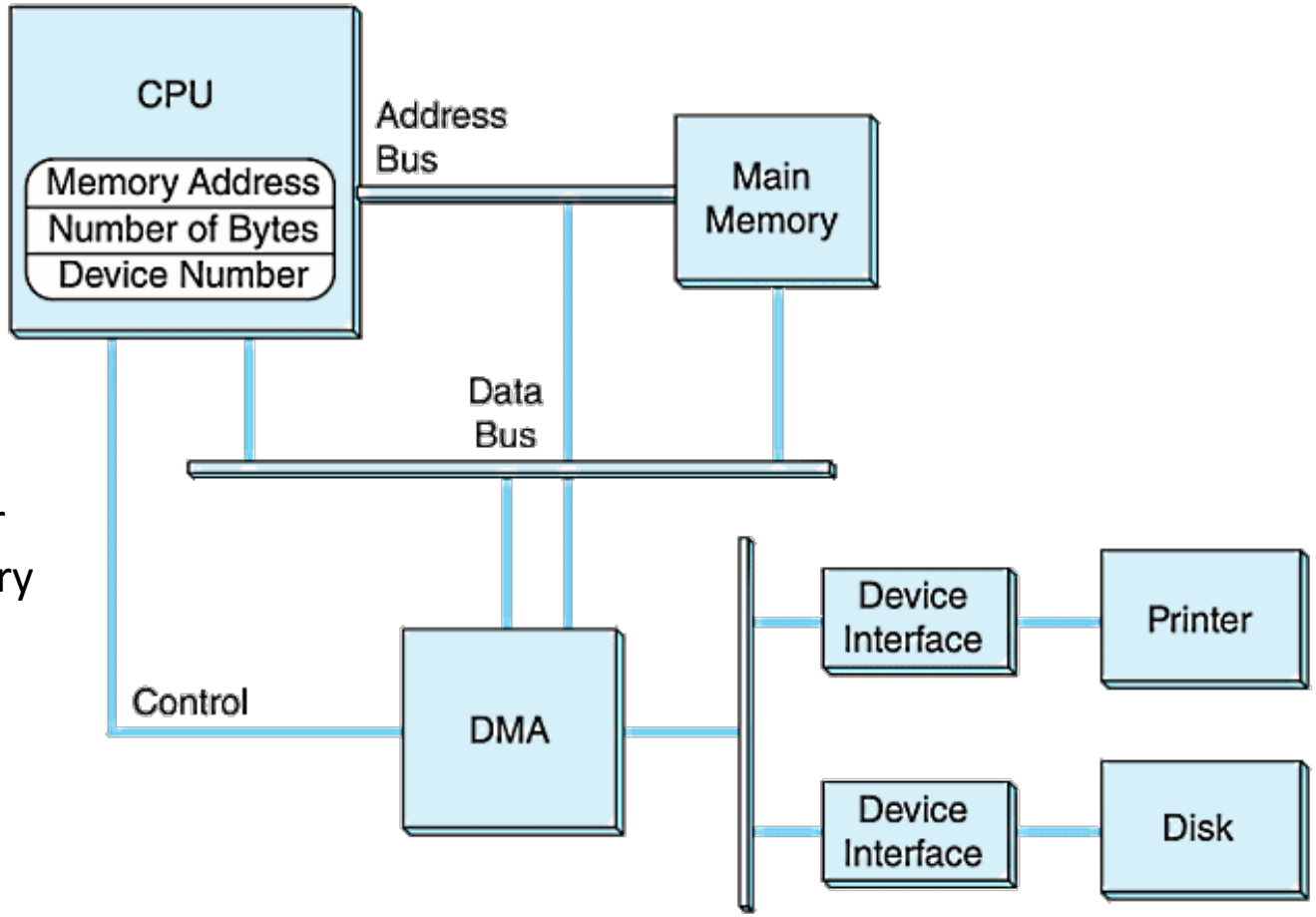
- Some devices can directly access memory
  - Bypasses the CPU and goes directly to memory
- The CPU is only involved at the beginning and at the end
  - DMA Device ID or address
  - Memory address (source or destination of data)
  - Size of block transfer
  - Direction (input or output)
- A single interrupt occurs at the end of the transaction
  - DMA controller decrements count and adjusts pointer to memory
  - Consumes less CPU time than with interrupt after each byte or word

DMA Devices

This is a DMA configuration.

Notice that the DMA and the CPU share the bus.

The DMA runs at a higher priority and steals memory cycles from the CPU.



The DMA does not go through the cache, so the cache contents could be made stale.

DMA Modes

Ways CPU and DMA device can share memory bus:

- Transparent mode
  - Bus is used for DMA only when not needed by CPU
  - This is the ideal theoretical case
  - Can't really predict when CPU will not need the bus
- Cycle stealing mode
  - CPU frees bus long enough for DMA of one data unit
  - Cycles are given up by CPU to allow DMA transfers
- Burst mode
  - CPU relinquishes bus long enough for a block transfer
  - Feasible if CPU is actively getting cache hits

I/O Processors (IOP)

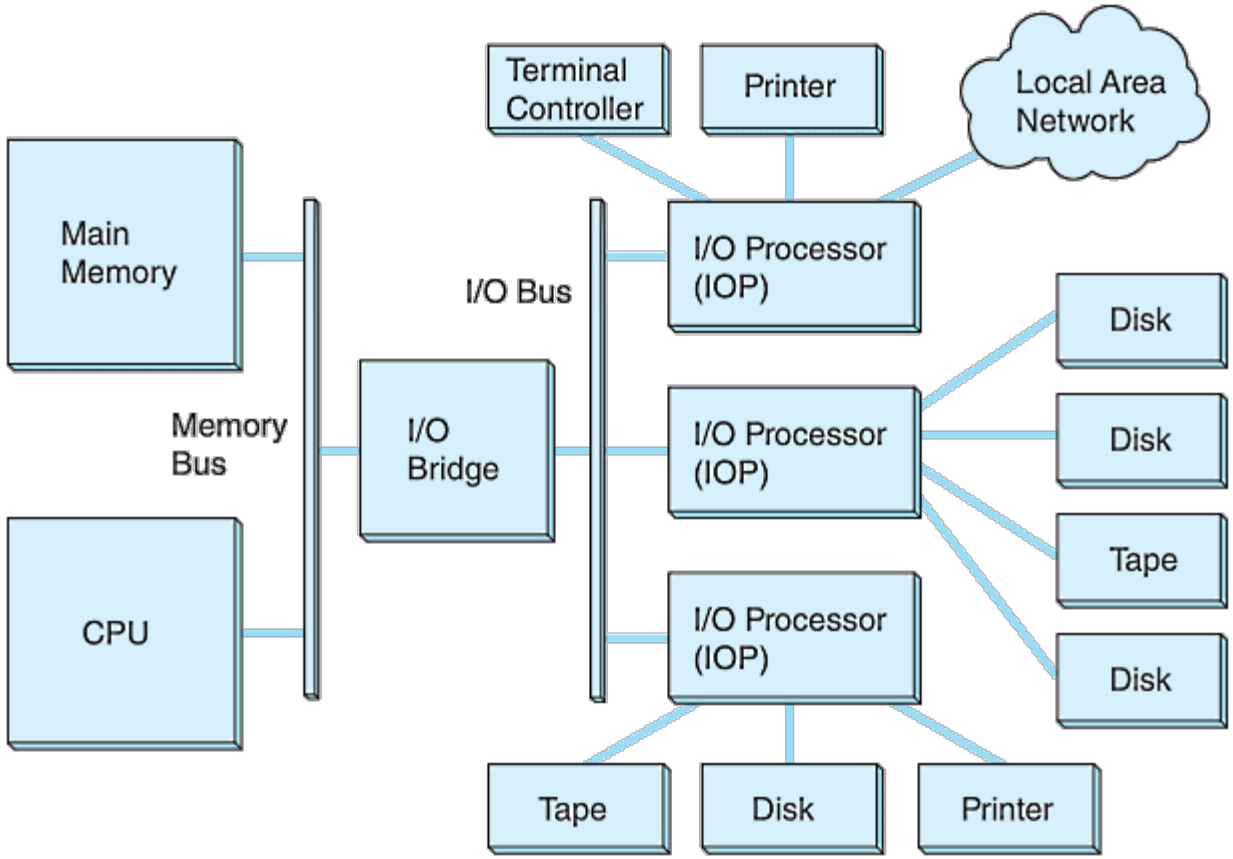
- IOPs are also known as I/O channels
  - They have their own instruction set tailored for I/O
  - They can carryout a series of multi-step transactions
  - They run in parallel with and independent of the CPU
  - They transfer entire files or groups of files
- “channel command” IBM’s term for I/O instruction
- Intel 8086 had a companion 8089 I/O processor
- Relieves the CPU of most I/O duties
  - Less burden on CPU than interrupts or DMA

I/O Processors (IOP)

- IOPs have more intelligence than DMA controllers
  - They negotiate protocols
  - issue device commands
  - translate storage coding to memory coding
  - transfer entire files or groups of files independently of the host CPU
- The host CPU creates the I/O program
  - These are I/O specific instructions
  - CPU tells IOP where to find the I/O program

I/O Processors (IOP)

- This is a channel I/O configuration.



Issues with I/O and Cache

- Memory mapped device registers are accessed like any other data items.
  - Copies of the registers in the cache may be stale
  - CPU accesses go through the cache
  - I/O device accesses do not go through the cache
- DMA controllers use physical addresses
  - Network packet buffers could be a problem if cached
  - DMA transfer goes directly to memory
  - If the buffer maps to cache, the CPU may be unaware

Issues with I/O and Cache

- Some CPUs have a cache flush instruction
  - This invalidates one or more the cache lines
  - References to the items then go directly to memory
- An alternative is to use uncached areas
  - Specified address ranges used by the CPU do not go through cache
  - I/O device registers and I/O buffers could be assigned to these uncached areas

Conclusion

- Next we will examine bus systems in more detail
  - Buses are required to access memory and I/O devices
- We will also examine disk arrays (RAID systems)