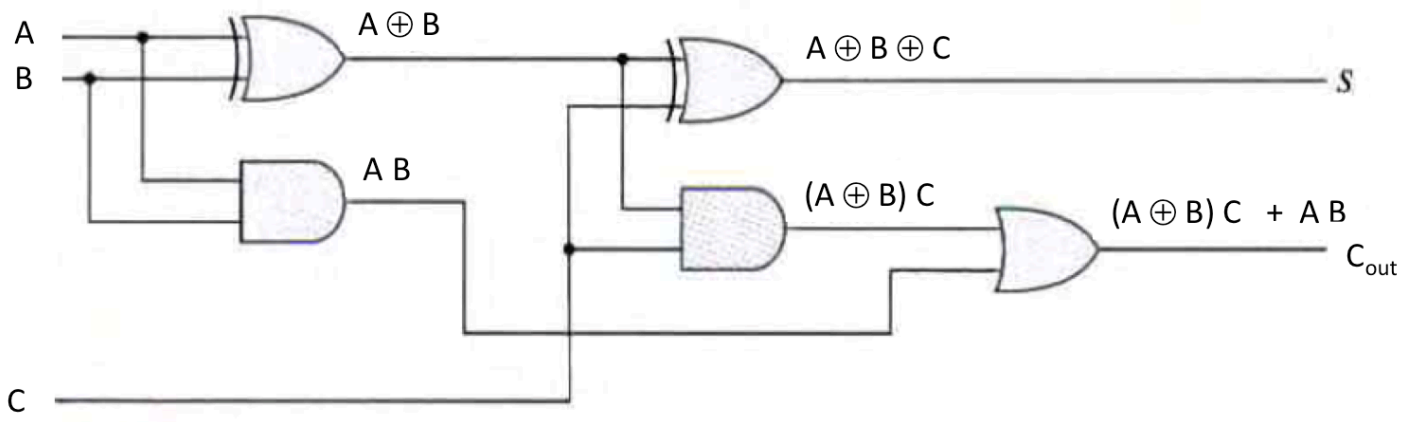
Full Adder



A ⊕ B and A•B can be generated in parallel for each position

S is then generated as A ⊕ B ⊕ C (where C is the carry-in)

Hence S_0, the LSB of the sum requires 2 gate delays

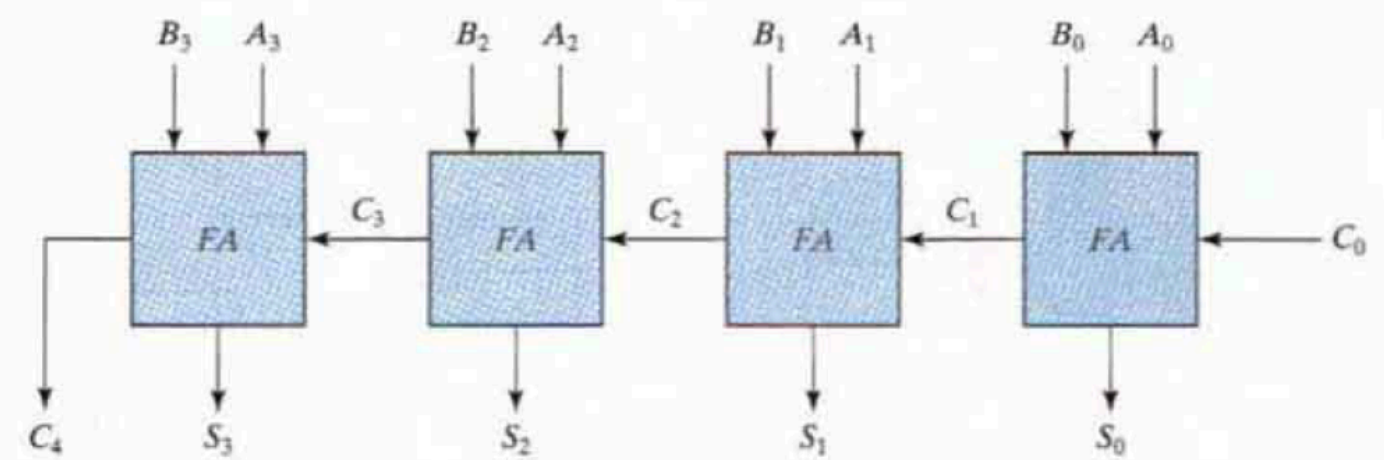
C_{OUT} is available after 3 gate delays

Other sum bits need the carry from the bit position on the right

S = A ⊕ B ⊕ C, so another gate delay is needed once C is available

C_{out} = (A ⊕ B) C + A B , and requires 2 more gate delays

Four-bit Ripple Carry Adder



S_0 is available after 2 delays
C_1 is available after 3 delays
S_1 is available after 1 + 3 = 4 delays
C_2 is available after 2 + 3 = 5 delays
S_2 is available after 1 + 5 = 6 delays
C_3 is available after 2 + 5 = 7 delays
S_3 is available after 1 + 7 = 8 delays
C_4 is available after 2 + 7 = 9 delays

Faster Addition

Recall that for the full adder:

CarryOut = (a • b) + (a ⊕ b) • CarryIn

If a and b are both 1, they generate a CarryOut when added

If either a or b is 1, Carryin is propagated to CarryOut

In general: $c_{i+1} = (a_i \bullet b_i) + (a_i + b_i) \bullet c_i = g_i + p_i \bullet c_i$

$g_i = a_i \bullet b_i$ and $p_i = a_i \oplus b_i$ the subscript indicates the bit position

C_0 is the input carry for bit 0, the LSB

$C_0 = 0$ for addition

$C_0 = 1$ for subtraction

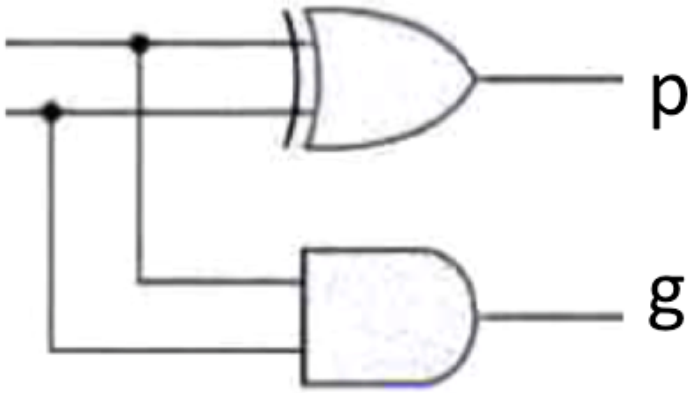
Faster Addition

recurrence relation for all of the output carries:

$c1 = g0 + p0 \bullet c0$

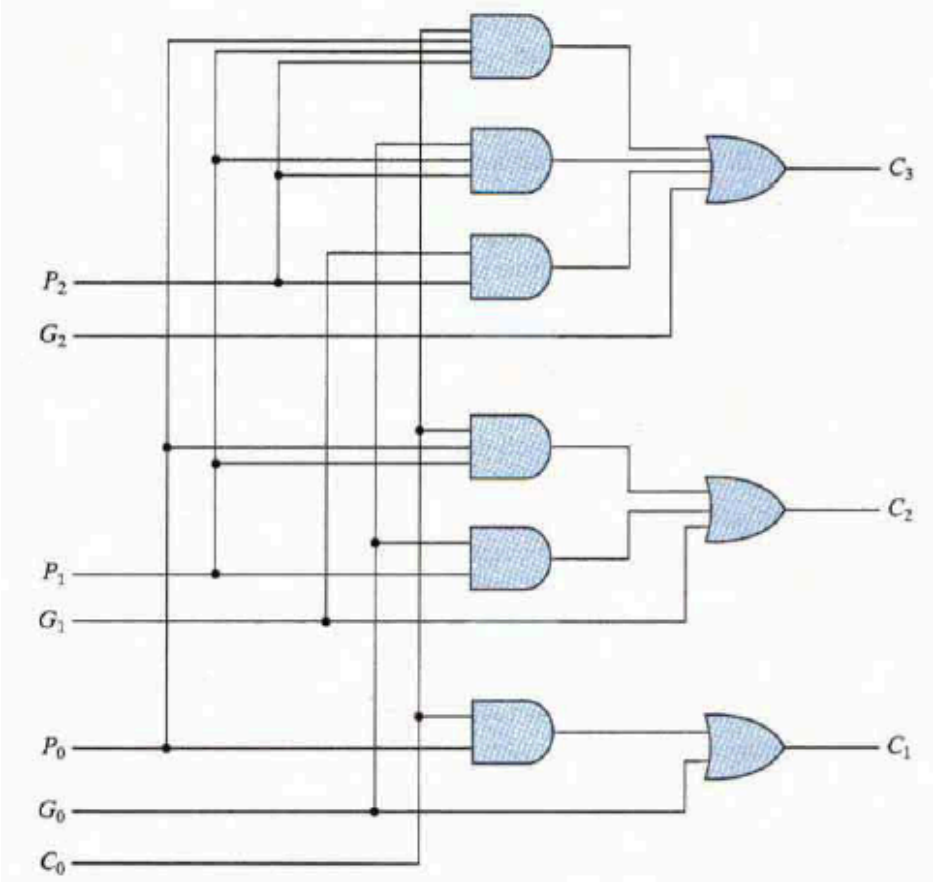
$c2 = g1 + p1 \bullet c1$

$c_i = g_{i-1} + p_{i-1} \bullet c_{i-1}$ (for i>0)



Inputs are the data bits for each position

Faster Addition

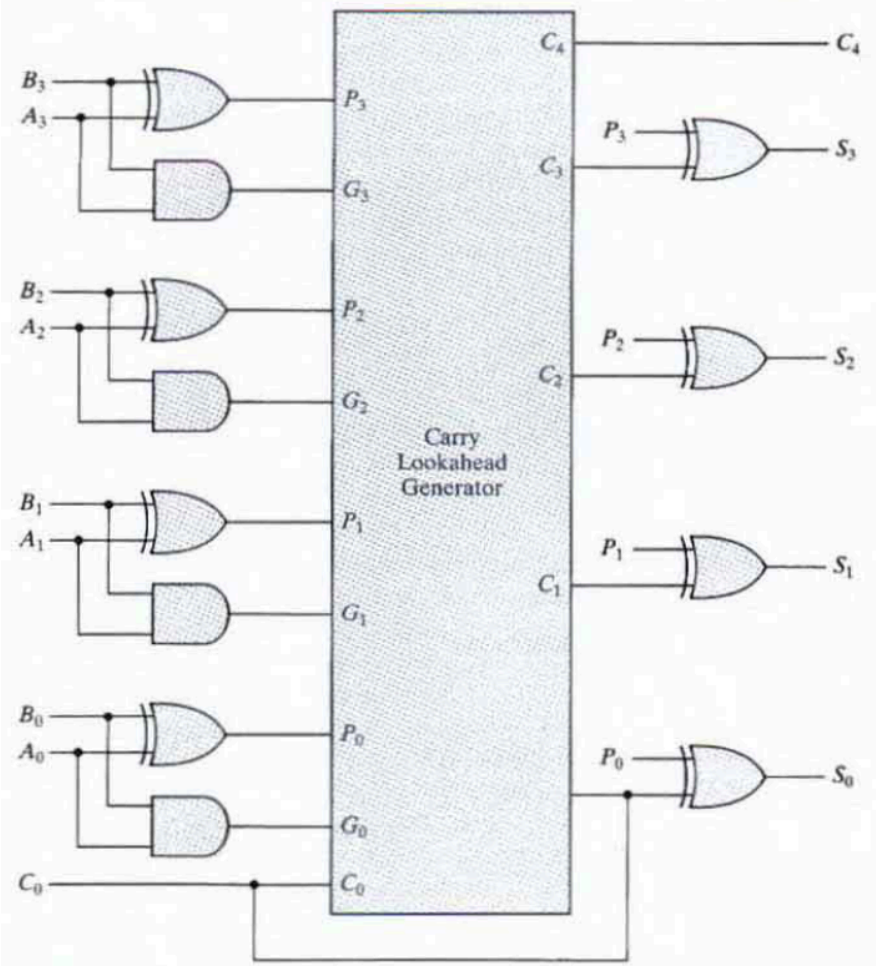


Propagate & generate bits are used to produce carry bits

Carries require 2 gate delays and are produced in parallel

Lookahead carry generator circuit

Faster Addition



Bits in sum are available after 1+2+1 = 4 gate delays

4-bit adder with lookahead carry

Look Ahead Carry Adder

- c0 and all of the a_i and b_i bits are known up front
- All of the p_i and g_i can be generated in parallel (1 delay)
- All carry bits c_i are generated in parallel (2 more delays)
- All sum bits are produced in parallel (1 more delay)
- This is faster than the ripple carry adder
- Ripple carry adder computes each sum sequentially from LSB to MSB