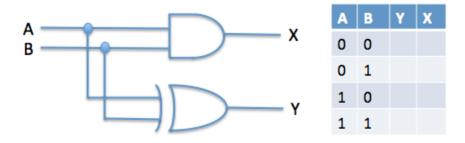
Computer Science 605.611

Problem Set 3

[For this problem set, use "*" to denote logical AND, "+" to denote logical OR, "^" to denote exclusive-OR and the apostrophe " " to denote NOT (e.g., N' means NOT N).]

1. a) (5) Complete the truth table below by filling in the columns for the circuit outputs Y and X as a function of the inputs A and B.



A	В	Y	X
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

b) (5) To what arithmetic functions do the outputs Y and X correspond?

X corresponds to AND (*), while Y corresponds to XOR (^)

2. (10) Consider the following truth table that defines the output C as a function of the two inputs A & B:

Inputs		Output
Α	В	C
0	0	0
0	1	1
1	0	1
1	1	0

Use only Boolean identities (not truth tables) to show that the logical sum of the non-zero minterms for this function is equivalent to the logical product of the zero-maxterms.

A	В	zero maxterm	non-zero-	С
			minterm	

0	0	A + B	A * B	0
0	1	'A + B	'A * B	1
1	0	A + 'B	A * 'B	1
1	1	'A + 'B	'A * 'B	0

- 3. Recall that the modulo function L MOD N is defined as the remainder produced when L is divided by N.
- a) (5) Write down a series of MIPS true-op instructions that use the integer divide instruction to produce in register \$8, the result of the function \$8 MOD \$4.

div \$8 \$4 # Hi contains remainder, Lo contains quotient mfhi \$8 # remainder moved to \$8

b) (5) Write down a single (i.e., one) MIPS logical instruction that produces in register \$9 the result of the function \$9 MOD 256.

rem \$9, \$9, 256

4. (5) Consider the circuit:

Write down an equivalent logic function involving only the operators * for AND, + for OR and ' for NOT. X = A * B

- 5. An encoder generates an output that identifies which one of its inputs is active. The output is in effect the index of the single active input.
- a) (5) How many outputs are required for an encoder that has 8 inputs?

$$3(2^3 = 8)$$

b) (5) If a decoder like that described in module 3 has 4 outputs, how many inputs should it have?

$2 \land 4 = 16$ outputs

6. (5) Suppose the register \$7 contains a single precision IEEE 754 floating point number. Write down a series of MIPS integer instructions that changes the floating point number in \$7 into its arithmetic negative.

```
srl $0, $7, 31  # isolate sign bit

xor $0, $0, $zero  # flip sign bit

sll $0, $0, 31  # move sign bit to sign location

sll $1, $7, 1

srl $1, $1, 1  # isolate exponent and mantissa

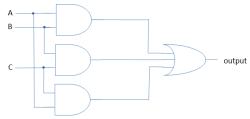
add $7, $0, $1  # adding sign bit and exponent/mantissa produces

arithmetic negative
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7. (5) How can the same full adders used to generate the sum of two integers N+M be used instead to generate their difference N-M?

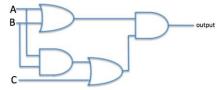
A full adder can be modified by chaning the X input to the AND gate to X'. Instead of the "Carry" output, this becomes "Borrow". By changing the X input to its opposite in both half-adders that make up the full adder, the sign of the expression is essentially flipped, allowing us to implement a "full subtracter".

8. a) (5) Write down a logic expression for the output generated by the following circuit:



output =
$$(A * B) + (B * C) + (A * C)$$

b) (5) Write down a logic expression for the output generated by the circuit below:



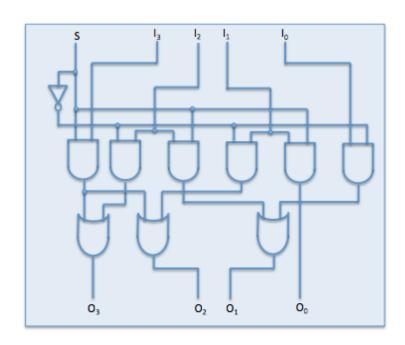
output =
$$(A + B) * ((A * B) + C)$$

c) (5) Use Boolean identities (not truth tables) to show that the expression you obtained for part b) can be transformed into the expression you obtained for part a). That is, the expression for part b) can be rewritten as the expression for part a).

$$(A + B) * ((A * B) + C)$$

= $(A + B) * ((A + C) * (B + C))$ distributive law
= $(A + B) * (A + C) * B + C)$ associative law

9. Consider the following circuit:



a) (5) If S=0 show the outputs if initially I_3 , I_2 , I_1 I_0 = 0101.

(Where row 1 is input row, row 2 is input to the AND gates, row 3 is output from AND gates, row 4 is output from OR gates, and row 5 is output, and entries are from left to right) – attempt to show work.

Row 1: 00101

Row 2: 001110100011

Row 3: 010001

Row 4: 101

Row 5: 1010

 $O_{3} = 1$

 $O_2 = 0$

 $O_1 = 1$

 $O_0 = 0$

b) (5) If S=1 show the outputs if initially I_3 , I_2 , I_1 $I_0 = 1110$.

Row 1: 11110

Row 2: 1101111011100

Row 3: 101010

Row 4: 111

Row 5: 1111

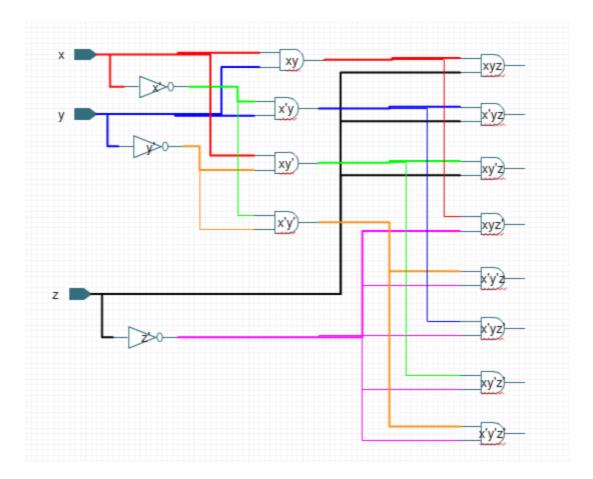
 $O_3 = 1$

 $O_2 = 1$

 $O_1 = 1$

 $O_0 = 1$

10. (10) Consider a CPU that uses 3-bit opcodes. Draw a logic circuit containing only discrete NOT gates together AND each of which uses only 2 inputs; the circuit should implement a decoder for the 3-bit opcode. Your circuit should contain the minimum number of NOT gates and the minimum number of 2-input AND gates.



11. (5) The following boolean expression defines Z as a function of four inputs A, B, C and D:

$$Z = A*D*(B+C) + B*C*(A+D)$$

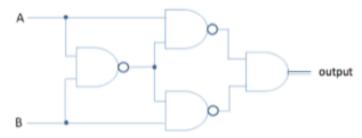
where "*" denotes a logical AND operator and "+" denotes a logical OR operator. Which of the following types or circuits best matches this function? Explain why.

- I. Comparator (Z=1 if all the inputs are equal)
- II. Majority vote (Z=1 if more than half of the inputs are set)

If A,B,C are 1 and D is 0, Z is 1 If A,B,D are 1 and C is 0, Z is 1 If A,C,D are 1 and B is 0, Z is 1 If B,C,D are 1 and A is 0, Z is 1 If A,B,C,D are 1, Z is 0

II Majority vote

12. (5) Consider the logic circuit shown below:



Which one of the following individual logic gates is equivalent to this circuit (i.e., generates the same output for the same inputs)?

- a) AND
- d) NAND
- b) OR
- e) XNOR
- c) NOR
- f) XOR

Truth Table:

A	В	Output
0	0	0
0	1	0
1	0	0
1	1	1

Answer: a) AND