Computer Science 605.411

Module 11 Example Set 3

1. A processor has eight interrupt lines (numbered 0 – 7) from highest (0) to lowest (7) priority. Initially, no interrupts are pending and the following sequence of interrupts then occurs: 4, 7, 1, 3, 0, 5, 6, 4, 2, 1. Once an interrupt occurs, no further interrupts can get in until the processing of the current interrupt has been completed. That is, interrupts simply pend until the interrupt handler returns. Upon return from the interrupt handler, the highest priority pending interrupt would be serviced next. If the time required to handle an interrupt is such that two additional interrupts occur while the current interrupt is being serviced, in what order would the ten interrupts be serviced? Write down the interrupt numbers in the order in which the interrupts would be serviced.

Interrupt 4 is handled first. By the time processing for interrupt 4 is complete, interrupts 7 and 1 will have arrived, so interrupt 1 gets handled. By the time processing is complete for interrupt 1, interrupts 7, 3 and 0, will be pending; so interrupt 0 is handled next. Upon completing interrupt 0, interrupts 7, 3, 5 and 6 will be pending and interrupt 3 is handled next. At the end of interrupt 3, interrupts 7, 5, 6, 4 and 2 will be pending and interrupt 2 is handled next. While processing interrupt 2, interrupt 1, the final interrupt arrives so interrupts 7, 5, 6, 4 and 1 will be pending. These five interrupts will be handled in priority order. Hence the ten interrupts would be serviced in the order: 4, 1, 0, 3, 2, 1, 4, 5, 6, 7.

2. An I/O device transfers input data at the rate of $10^7$ bytes per second over an I/O bus with a total bandwidth of $100 * 2^{20}$ bytes per second. The input data consists of 2500 independent pages each of which is 4096 bytes in size. The CPU for this system has a clock rate of 200 MHz (i.e. 200 million cycles per second) and the memory system is fast enough to sustain these transfer rates.

a) During each I/O transfer, the processor performs no other activity than that required to receive the input data. If the arrival of each data byte causes an interrupt, what is the maximum number of clock cycles that the CPU can consume in responding to and handling the interrupts from the device if it is to avoid the loss of data?

To avoid the loss of data, the time required to respond the each interrupt and input the data byte must be less than the time interval between consecutive bytes. The limiting factor is the speed at which the device transfers data since the bus bandwidth is 10 times the device's data rate.

The I/O device transfers data at a rate of $10^7$ bytes per second , so the interval between bytes is $10^{-7}$ seconds which corresponds to $10^{-7} / (5*10^{-9}) = 20$ CPU clock cycles. So no more than 20 cycles must be consumed between the arrival of adjacent bytes.

b) When a DMA controller is used to perform the transfer, 1000 CPU cycles are required to set up and initiate the DMA transaction and an additional 1500 CPU cycles are required to respond to the interrupt when the DMA transfer completes. What fraction of the available CPU cycles would be consumed to perform a DMA transfer of a single page?

With the DMA controller, the processor only consumes cycles for the purpose of I/O when it is setting up the DMA transfer and when it is responding to the interrupt at the conclusion of the DMA transfer.
The time required for the device to transfer a page is
$4096 * 10^{-7}$ seconds $= 4096 * 10^{-7} / 5 * 10^{-9} = 81920$ cycles.
The CPU consumes 1000 cycles to setup the DMA transaction + 1500 cycles to service the interrupt at the conclusion of the transfer for a total of 2500 cycles.
The total time required to complete the all activity required to transfer a single page corresponds to 1000 + 81920 + 1500 = 84420 cycles. However, the CPU is only active during 2500 of these cycles for the purpose of the transfer.
This corresponds to 2500/84420 = 2.96 per cent of the available CPU cycles.

3. The read access delay for an I/O system is defined as the time required for the device to acquire the requested data and prepare to start transmitting the data. The data transfer rate for an I/O device is defined as the number of bytes per second that it can transmit. Suppose that there are two different I/O systems A and B. System A has a data transfer rate of 5120 bytes per second and has an access delay of 5 seconds. System B has a data transfer rate of 3072 bytes per second and has an access delay of 4 seconds.

a) How long will each system require to complete a 3145728-byte I/O request?
**System A: 5 + (3145728 / 5120) = 619.4 seconds**
**System B: 4 + (3145728 / 3072) = 1028 seconds**

b) It is observed that for an I/O request of size N bytes, the two systems require the same amount of time to complete the request. What value is N?
**$5 + (N / 5120) = 4 + (N / 3072) \Rightarrow 5 - 4 = (N / 3072) - (N / 5120) = (5N - 3N) / 15360, \Rightarrow 1 = 2N / 15360 = N / 7680 \Rightarrow N =$ 7680 bytes.**

4. "Cycle stealing" is one mode of operation used by a DMA controller in performing I/O transfers. What are two other modes that could be used by the DMA controller?

**The two other modes are transparent and burst (i.e. block) transfer mode.**