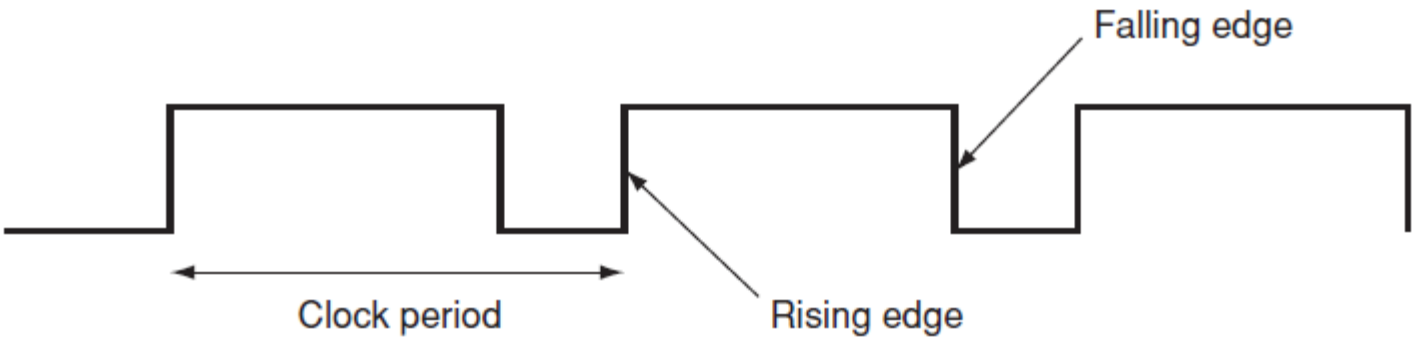
Datapath Timing

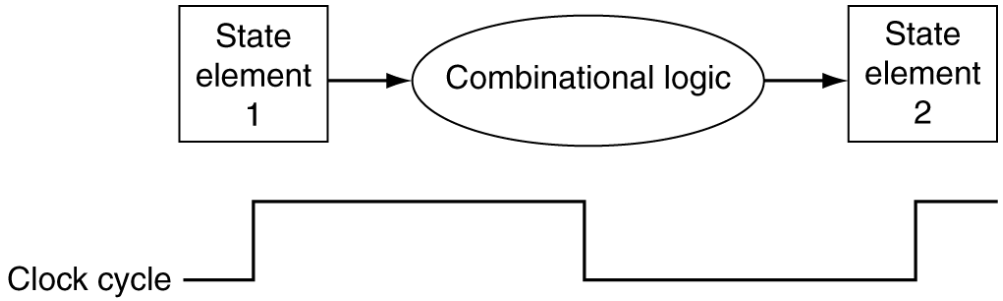
- Operations are synchronized to a clock
  - For example, when a register is written
  - Instructions complete at clock edges

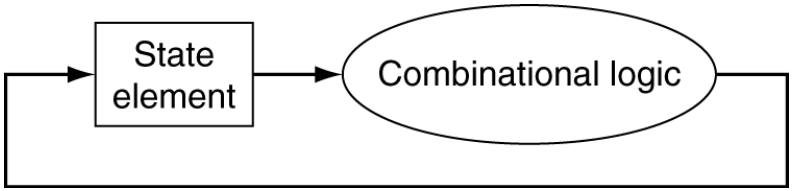


- Clock signal oscillates between high and low values
- Clock period is one full clock cycle
- State changes only on clock edge (either rising of falling edge)

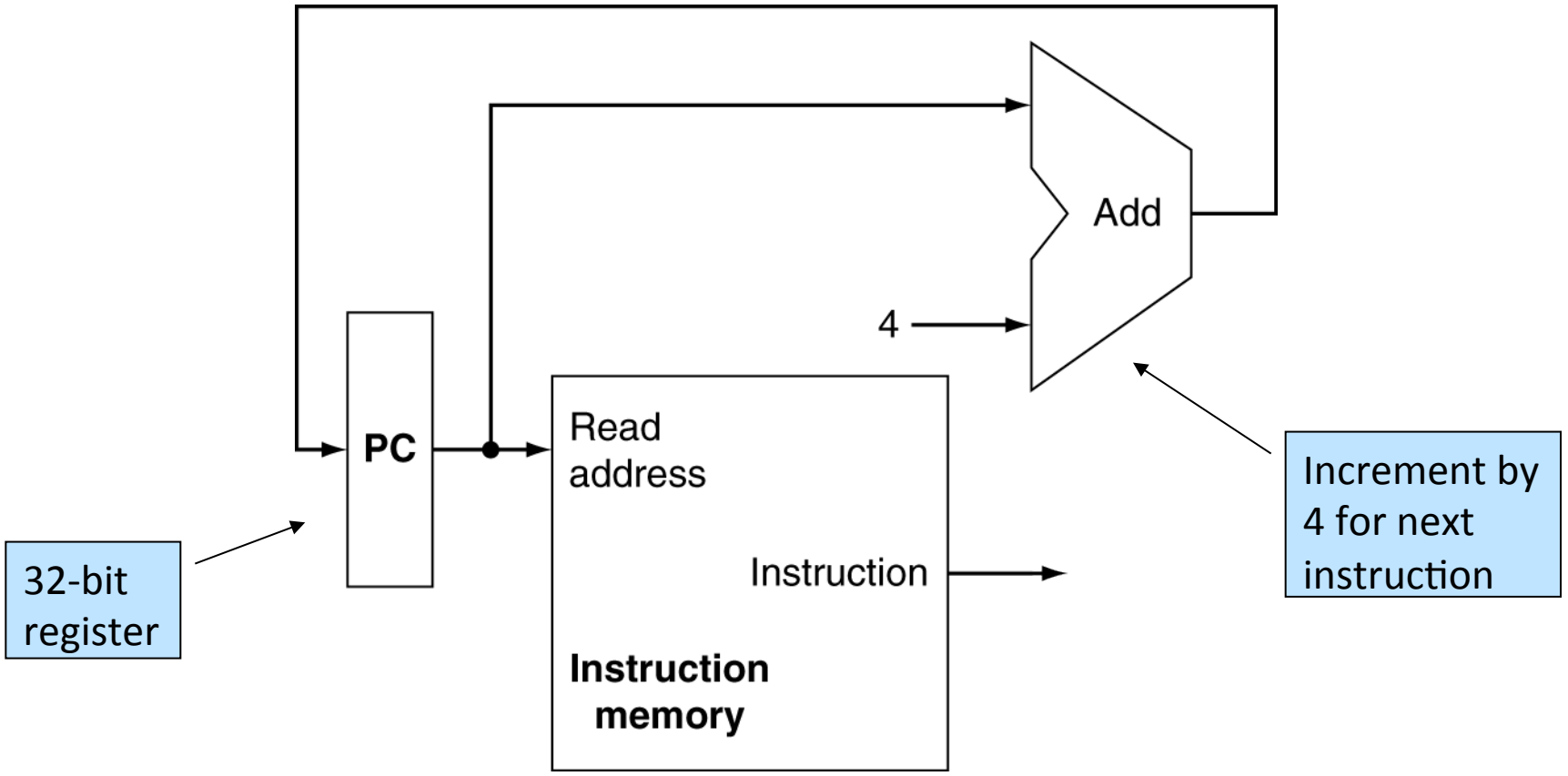
Datapath Timing

- Combinational logic transforms data during clock cycles
  - Between clock edges
  - Inputs come from state elements
  - Outputs go to state elements
  - Longest delay determines minimum clock period





Building a Datapath

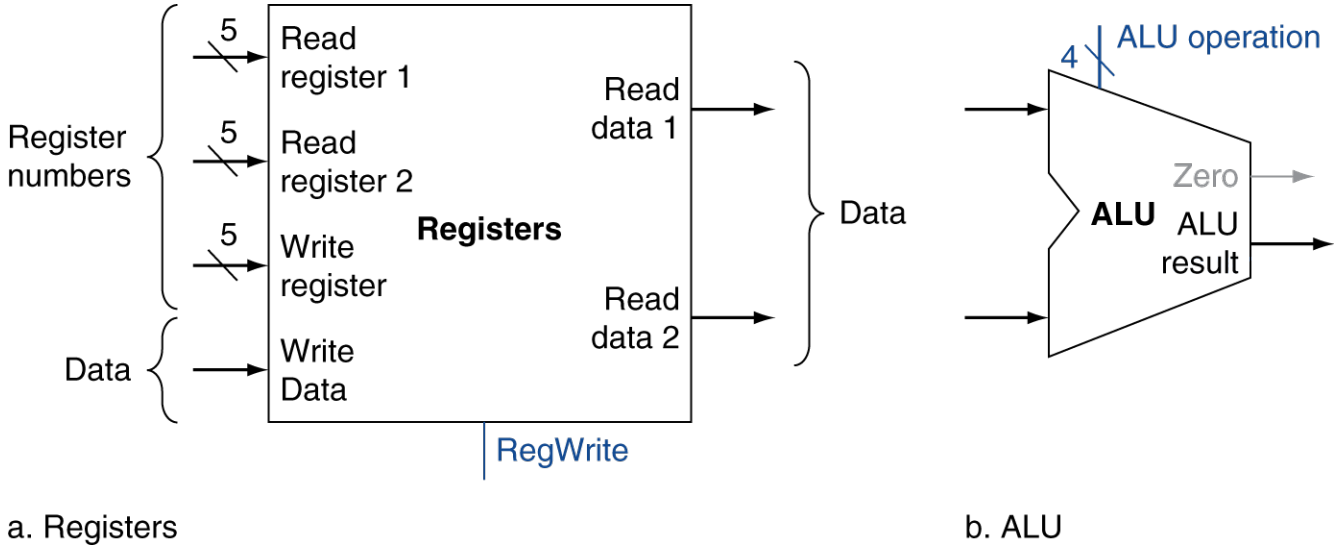


Performs Instruction Fetch

Building a Datapath

R-Format Instructions

- Read two register operands
- Perform arithmetic/logical operation
- Write register result



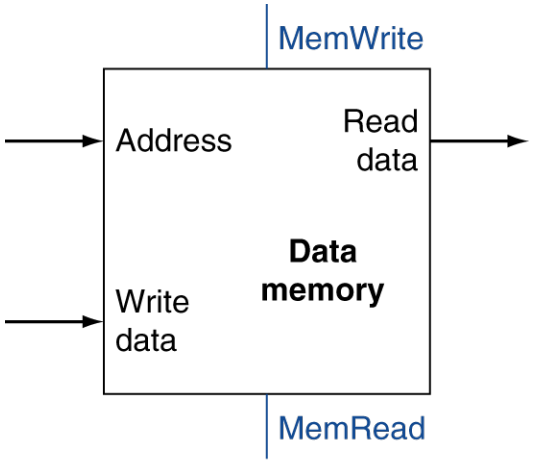
a. Registers

b. ALU

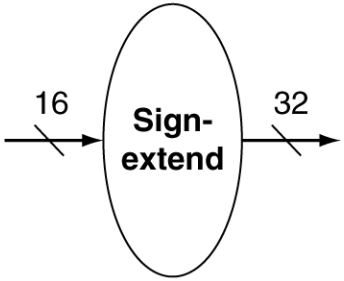
Building a Datapath

Load/Store Instructions

- Read register operands
- Calculate address using 16-bit offset
  - Use ALU, but sign-extend offset
- Load: Read memory and update register
- Store: Write register value to memory



a. Data memory unit

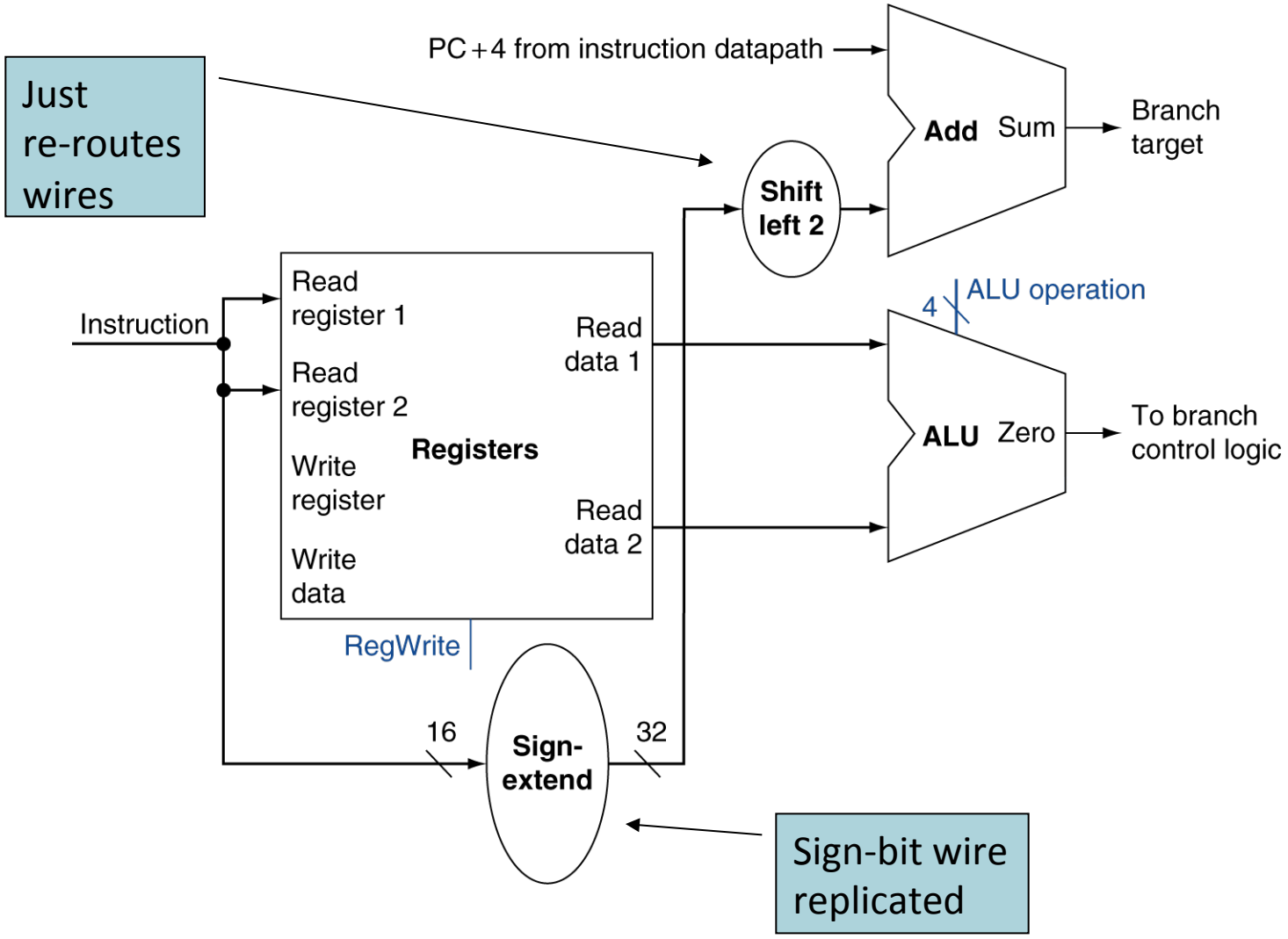


b. Sign extension unit

Branch Instructions

- Read register operands
- Compare operands
  - Use ALU, subtract and check Zero output
- Calculate target address
  - Sign-extend displacement
  - Shift left 2 places (word displacement)
  - Add it to PC
    - PC already incremented by instruction fetch

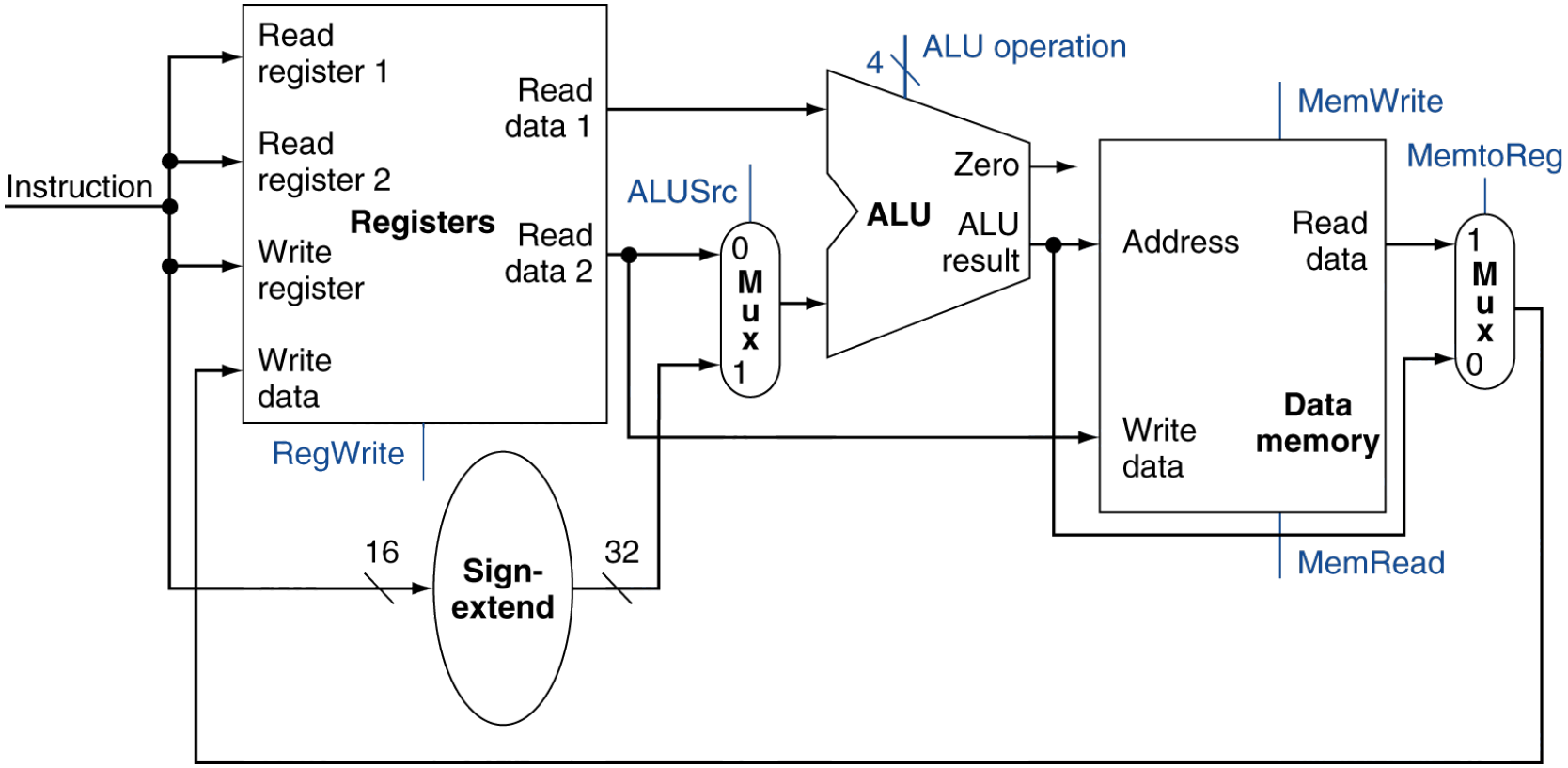
Building a Datapath



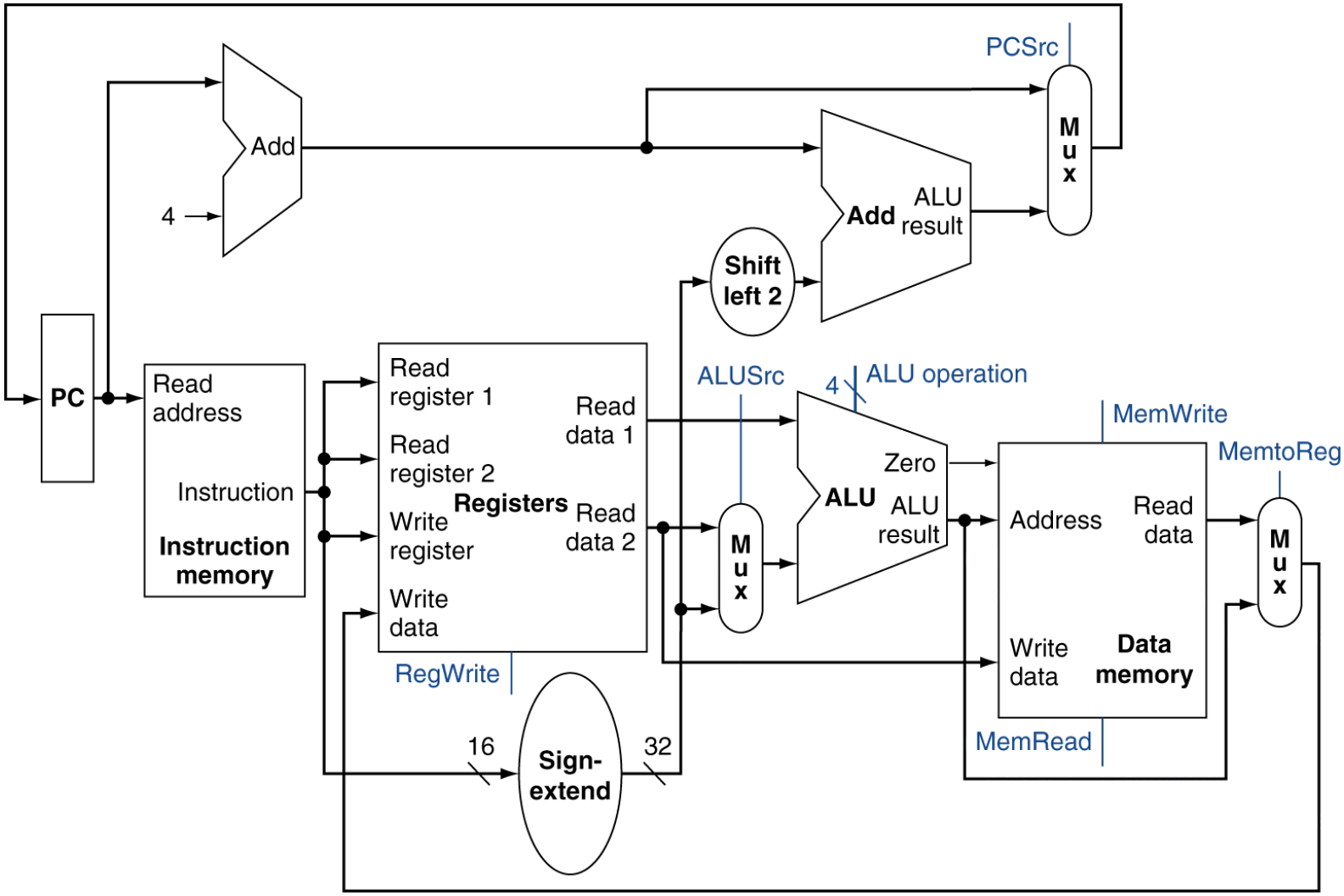
Single Cycle Execution

- One option is for the datapath to execute an instruction in one clock cycle
  - Each datapath element can only do one function at a time
  - Hence, we need separate instruction and data memories (Harvard Architecture)
- Use multiplexers where alternate data sources are used for different instructions

R-Type/Load/Store Datapath



Full Datapath



Conclusion

- The datapath components have now been described
- Next, the ALU will be examined in more detail
- We will also see how the control unit produces the required signals