Brian Loughran
Intro to Computer Architecture
Johns Hopkins
Module 1 Homework

Assignment:

1.2 Note: This is to be a 'best fit' for all the ideas solution set
1.4

1.5

1.7
1.10.1 and 1.10.2
1.14.1; 1.14.2; and 1.14.3

1.2 [5] <§1.2> The eight great ideas in computer architecture are similar to ideas from other fields. Match the eight ideas from computer architecture, “Design for Moore’s Law”, “Use Abstraction to Simplify Design”, “Make the Common Case Fast”, “Performance via Parallelism”, “Performance via Pipelining”, “Performance via Prediction”, “Hierarchy of Memories”, and “Dependability via Redundancy” to the following ideas from other fields:
a. Assembly lines in automobile manufacturing
b. Suspension bridge cables
c. Aircraft and marine navigation systems that incorporate wind information
d. Express elevators in buildings
e. Library reserve desk
f. Increasing the gate area on a CMOS transistor to decrease its switching time
g. Adding electromagnetic aircraft catapults (which are electrically-powered as opposed to current steam-powered models), allowed by the increased power generation offered by the new reactor technology
h. Building self-driving cars whose control systems partially rely on existing sensor systems already installed into the base vehicle, such as lane departure systems and smart cruise control systems

a. Performance via Pipelining
b. Performance via Parallelism
c. Performance via Prediction
d. Make the common case fast
e. Hierarchy of Memories
f. Use Abstraction to Simplify Design
g. Dependability via Redundancy
h. Design for Moore’s Law

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1.4 [2] <§1.4> Assume a color display using 8 bits for each of the primary colors (red, green, blue) per pixel and a frame size of 1280 × 1024.
a. What is the minimum size in bytes of the frame buffer to store a frame?
b. How long would it take, at a minimum, for the frame to be sent over a 100 Mbit/s network?

a. bits/pixel = (8*3) = 24 bits
   pixels/screen = (1280*1024) = 1,310,720 pixels
   bits/screen = (24*1,310,720) = 31,457,280 bits
b. (31,457,280/1,000,000) = 34.5 seconds

1.5 [4] <§1.6> Consider three different processors P1, P2, and P3 executing the same instruction set. P1 has a 3 GHz clock rate and a CPI of 1.5. P2 has a 2.5 GHz clock rate and a CPI of 1.0. P3 has a 4.0 GHz clock rate and has a CPI of 2.2.
a. Which processor has the highest performance expressed in instructions per second?
b. If the processors each execute a program in 10 seconds, find the number of cycles and the number of instructions.
c. We are trying to reduce the execution time by 30% but this leads to an increase of 20% in the CPI. What clock rate should we have to get this time reduction?

a. instructions/second = (clock rate / CPI)
   P1 = (3/1.5) = 1.5*10^9 instructions/s
   P2 = (2.5/1) = 2.5*10^9 instructions/s
   P3 = (4/2.2) = 1.82*10^9 instructions/s
   Processor 2 has the highest number of instructions executed per second
b. # cycles = (execution time * clock rate)
   # instructions = (# cycles/CPI)
   P1 cycles = (10*3) = 3*10^10 cycles
   P1 instructions = (30/1.5) = 2*10^10 instructions
   P2 cycles = (10*2.5) = 2.5*10^10 cycles
   P2 instructions = (25/1) = 2.5*10^10 instructions
   P3 cycles = (10*4) = 40*10^10 cycles
   P3 instructions = (40/2.2) = 1.82*10^10 instructions
c. CPU time α (CPI / Clock rate) – where α designates “proportional to”
   0.7 = (1.2/x)
   Clock rate must increase by a factor of 1.714

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1.7 [15] <§1.6> Compilers can have a profound impact on the performance of an application. Assume that for a program, compiler A results in a dynamic instruction count of 1.0E9 and has an execution time of 1.1 s, while compiler B results in a dynamic instruction count of 1.2E9 and an execution time of 1.5 s.
a. Find the average CPI for each program given that the processor has a clock cycle time of 1 ns.
b. Assume the compiled programs run on two different processors. If the execution times on the two processors are the same, how much faster is the clock of the processor running compiler A's code versus the clock of the processor running compiler B's code?
c. A new compiler is developed that uses only 6.0E8 instructions and has an average CPI of 1.1. What is the speedup of using this new compiler versus using compiler A or B on the original processor?

a. CPI = (execution time / (instruction count * clock cycle time)
   Compiler A CPI = (1.1 / (1*10^9 * 1*10^-9) = 1.1 instructions/cycle
   Compiler B CPI = (1.5 / (1.2*10^9 * 1*10^-9) = 1.25 instructions/cycle
b. Comp A Clock Cycle / Comp B Clock Cycle = Comp B instructions per cycle / Comp A instructions per cycle
   Comp A Clock Cycle / Comp B Clock Cycle = 1.25/1.1 = 1.136 * faster
c. Depends on the clock cycle time. Assuming a clock cycle time of 1 ns (all run on the same processor):
   execution time = instructions * cycles per instruction * seconds per cycle

Compiler A execution time	Compiler B execution time	New compiler time
1.1s	1.5s	.66s

1.10 Assume a 15 cm diameter wafer has a cost of 12, contains 84 dies, and has 0.020 defects/cm^2. Assume a 20 cm diameter wafer has a cost of 15, contains 100 dies, and has 0.031 defects/cm^2.
1.10.1 [10] <§1.5> Find the yield for both wafers.
1.10.2 [5] <§1.5> Find the cost per die for both wafers.

1. Yield = 1/(1+(defects per area * die area/2))^2
   15cm wafer has an area of 176.71 cm^2
   20 cm wafer has an area of 314.59 cm^2
   Yield(15cm) = 1/(1+(0.02 * 176.71/2))^2 = .13
   Yield(20cm) = 1/(1+(0.031 * 314.59/2))^2 = .029

2. Cost per die = cost per wafer / (dies per wafer * yield)
   Cost(15cm) = 12 / (84 * .13) = 1.10
   Cost(20cm) = 15 / (100 * .029) = 5.17

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1.14 Assume a program requires the execution of 50 × 106 FP instructions, 110 × 106 INT instructions, 80 × 106 L/S instructions, and 16 × 106 branch instructions. The CPI for each type of instruction is 1, 1, 4, and 2, respectively. Assume that the processor has a 2 GHz clock rate.
1.14.1 [10] <§1.10> By how much must we improve the CPI of FP instructions if we want the program to run two times faster?
1.14.2 [10] <§1.10> By how much must we improve the CPI of L/S instructions if we want the program to run two times faster?
1.14.3 [5] <§1.10> By how much is the execution time of the program improved if the CPI of INT and FP instructions is reduced by 40% and the CPI of L/S and Branch is reduced by 30%?

1. execution time = (instructions / (CPI * clock rate)
   execution time (FP) = (50*106) / 2*10^9 = 2.65*10^-6 seconds
   execution time (INT) = (110*106) / 2*10^9 = 5.85*10^-6 seconds
   execution time (L/S) = (80*106) / (4 * 2*10^9) = 1.06*10^-6 seconds
   execution time (branch) = (16*106) / (2 * 2*10^9) = 4.24*10^-7 seconds
   total execution time = 9.984 seconds
   CPI of FP instructions must improve by more than infinity – impossible
2. ½ * total execution time = 4.992*10^-6 seconds
   execution time (INT) to achieve that time is .858*10^-6 seconds
   5.85/0.85 gives a 6.88 times improvement in CPI of the L/S instructions
3. ((2.65*.6) + (5.85*.6) + (1.06*.7) + (.424*.7))/9.984
   = runs in 61.49 % of original execution time