Superpipelining

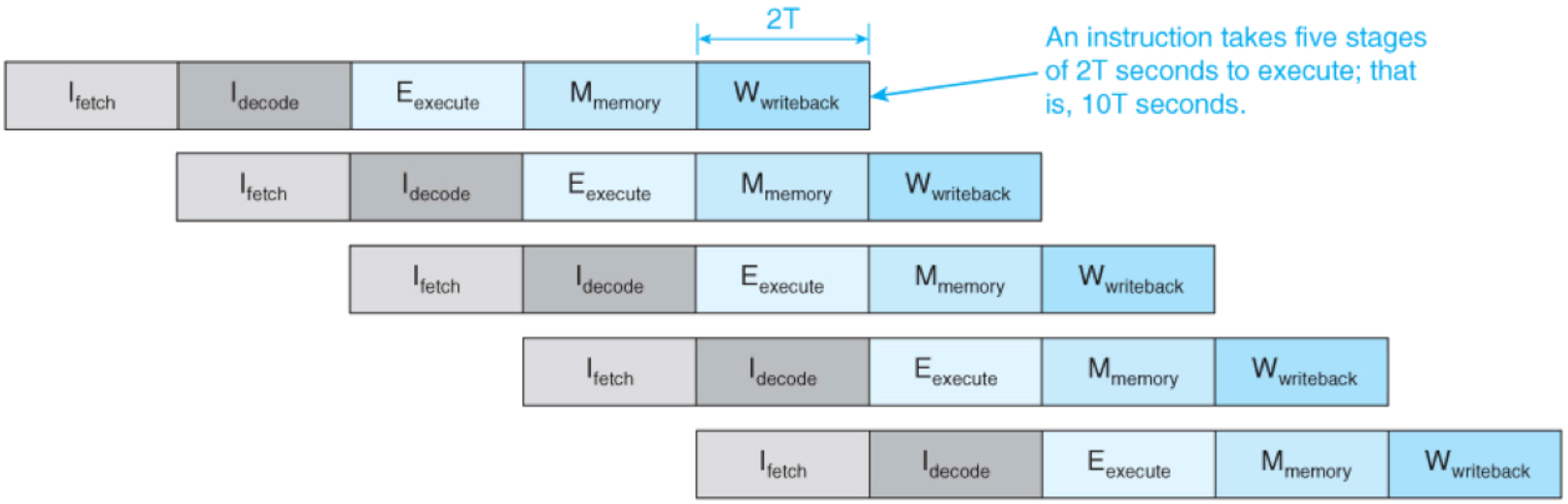
Superpipelining allows more instructions to be overlapped

Operations may not all require a complete clock cycle
- register reads or writes
- check for hits in cache
- decoding an opcode

The pipeline can run faster than the external clock rate

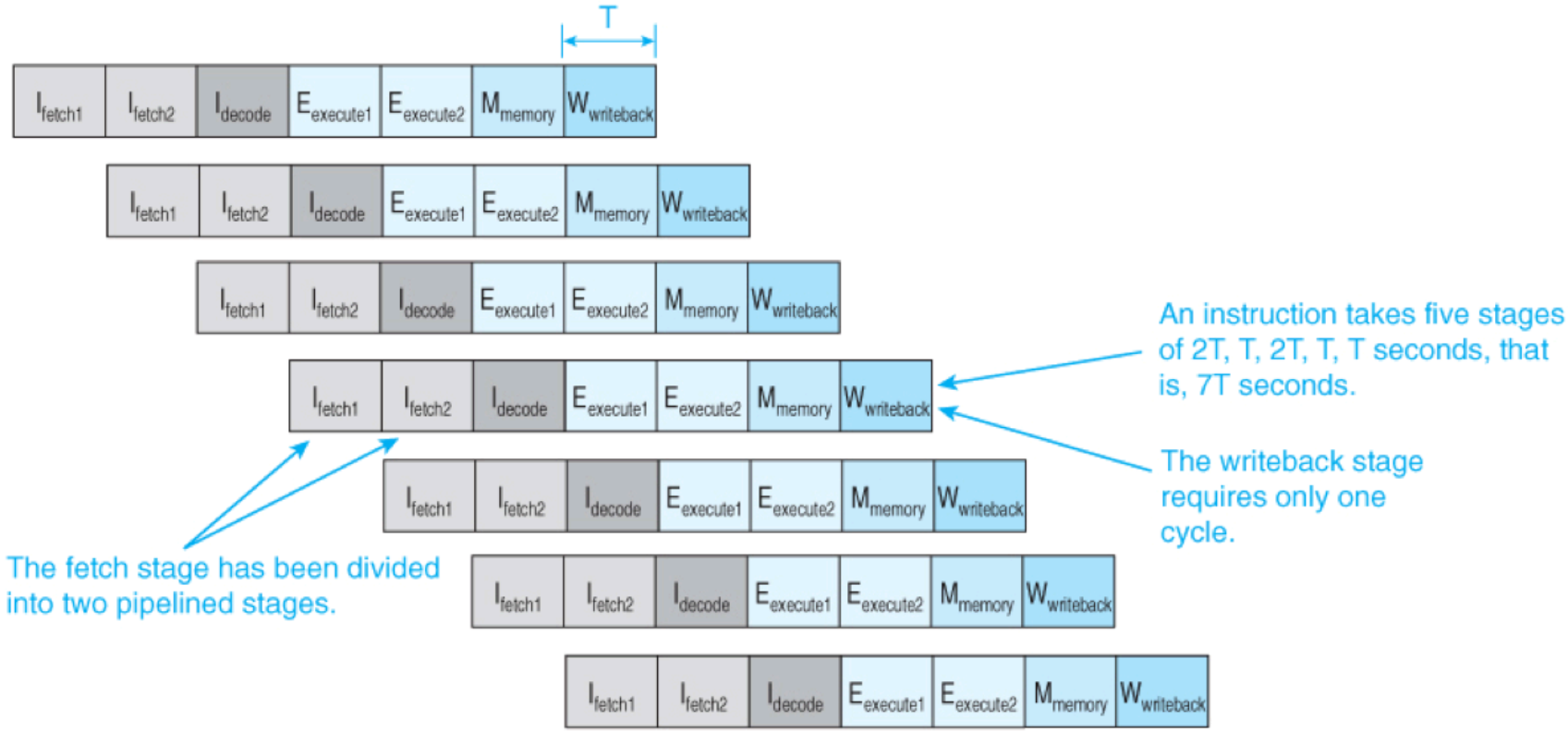
Superpipelines have some stages subdivided
- a different instruction is in each phase with a stage

Superpipelining



Conventional pipeline with cycle time = 2T

Superpipelining



Speedup = 10/7 = 1.43

Superpipeline with cycle time = T (twice the rate)

Superpipelining

Superpipelines use finer granularity
  instruction throughput increases
  the cost is a higher clock rate

Other parts of the datapath may require a slower rate
    precludes running the entire system at a higher clock rate

Hazards & mispredictions have a greater impact
    more stages have to be flushed

More stages cause more interstage delays
    more pipeline registers

Superpipelining

Superpipelines overlap more instructions

Superpipelining provides a modest performance increase

Superscalar provides a greater benefit

Superscalar systems can include superpipelining