Supported Modes:

- Source operands are on left, result on right in assembly instructions
- Register mode (all operands in registers)

■ add
$$\%g2,\%o4,\%o1$$
 [\%g2] + [\%o4] \rightarrow \%o1

$$[\%g2] + [\%o4] \rightarrow \%o1$$

Immediate mode

■ sub
$$\%$$
o2, 23, $\%$ g4 $[\%$ o2] $-$ 23 \rightarrow $\%$ g4

$$[\%o2] - 23 \rightarrow \%g4$$

Base register with displacement

■ Id
$$[\%g2 + 8]$$
, %o3 $[\%g2 + 8] \rightarrow \%o3$

$$[\%g2 + 8] \rightarrow \%o3$$

Register indirect with index

■ stb
$$\%$$
o4, $[\%$ g4 + $\%$ o2] $[\%$ o4] \rightarrow $[\%$ g4 + $\%$ o2]

$$[\%o4] \rightarrow [\%g4 + \%o2]$$

■ stb
$$\%$$
o4, $[\%$ g4 + $\%$ g0] $[\%$ o4] \rightarrow $[\%$ g4] ($\%$ g0 always 0)

$$[\%o4] \rightarrow [\%g4]$$

Sparc V8 Addressing Modes

Loading a 32-bit constant or address into a register

To load an address into %g2:

sethi %hi(X), %g2 high 22 bits of address or %g2, %lo(X), %g2 merge in low 10 bits

To load the constant 0x4A3C4098 into %o2:

0100101000111100010000 0010011000

sethi 0x128F10, %o4 high 22 bits or %o4, 0x98, %o4 low 10 bits

Synthetic instructions: set X, %g2

set 0x4A3C4098, %o4

%hi() and %lo() are implemented by the assembler

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