Module 9 Example Set 1.

1. One meg equals what numeric value when used for:
a) memory storage capacity 1 MB = 2^{20} bytes (i.e. 1048576 bytes)
b) Clock rate 1 MHz = 1000000 cycles per second.

2. What determines how much data a memory system must supply in response to a read request?
The width of the data bus (the pathway between the CPU and the memory) determines the amount of data that the memory must supply in response to a read request. The memory returns 1 byte at a time for an 8-bit bus, two bytes at a time for a 16-bit bus, 4 bytes at a time for a 32-bit bus, etc.

3. What is meant by the "width" of a particular memory chip or module?
The width is defined as the number of data bits output from or taken into the chip for a single read or write operation. The number of data pins on the chip is equal to its width.

4. What is meant by the "depth" of a particular memory chip or module?
The depth is defined as the number of separate storage cells available within the chip. Each cell contains a number of bits equal to the width of the memory chip.

5. What is the total storage capacity of a memory chip that has a width of 16 and a depth of 1048576?
The total number of bits in the chip = 16 * 1048576 or 16 mega-bits. This is equivalent to (16 * 1048576)/8 = 2 mega-bytes.

6. How many address bits are required to reference a storage cell within a memory chip that is 32 bits wide and has a depth of 262144?
The number of address bits required to reference an individual 32-bit cell within the chip = $\log_2(262144) = 18$. Eighteen bits can cover the address range 0 to $2^{18} - 1$ (i.e. 0 to 262143).

7. On a byte-addressable memory system that employs 32-bit wide chips, how are the low order address bits used in reading a byte from memory?
Since the memory chips are 32 bits wide, 4 bytes are transferred for each access. Since each cell contains 4 bytes, the bits to the left of the two LSBs would be used to identify which cell to access within a chip. The two LSBs of the address would then be used to select the appropriate byte from the 4-byte group to send to the CPU.

8. A 32-bit CPU-to-memory data bus is used with a memory system made up of a collection of chips each of which has a width of 8 bits and a depth of 2^{24}. How many chips would have to be accessed in response to a single read request?
A group of 4 chips would be required to supply the 32-bit data (since 4*8 = 32).

9. What is the purpose of a chip select signal and how is it derived?
The chip select signal identifies which chips should respond to a requested memory operation. It is derived from one or more of the address bits used to the reference the memory system.

10. Suppose that our MIPS processor and a memory system communicate over a 16-bit bus. The memory system is made up of 512 memory chips each of which has a width of 1 and a depth of 2097152.

a) How many data transfers would be required in executing a lw instruction?
The lw instruction requires 32 bits of data from memory. Since the bus is only 16 bits wide, two separate 16-bit transfers are needed to obtain the 32 bits of data.

b) How many chips would have to respond to each read request?
Since each chip supplies only 1 bit, a group of 16 chips would each provide 1 of the bits for each 16-bit transfer.

c) How many of the address bits would be used in generating the chip select signal?
Since there are 16 chips in each group and there is a total of 512 chips, the number of groups = 512/16 = 32. So 5 of the address bits would be used to generate the chip select signal which would activate all 16 chips within a group.

d) How many of the address bits would be used to identify the storage cell within each chip? Since the depth of each chip is 2097152, the number of address bits needed to identify the cell to be accessed within each chip is $\log_2(2097152) = 21$. Note that the total storage capacity of the memory is 512 * 1 * 2097152 = 1073741824 bits or 64 MB. This requires 26 address bits, so only the low 26 bits of the 32-bit addresses generated by the processor will ever be non-zero. That is, the upper 6 bits of the 32-bit address register can be ignored or always set to zero.

11. If the CPU-to-memory bus is B bits wide and is driven by a clock with frequency F, what would be the bandwidth for the bus if one transfer per cycle is performed?
"Bandwidth" is defined as the amount of data transmitted per unit time. Hence the bandwidth = B*F, since F = 1/T where T is the clock period.