Computer Science 605.611

Problem Set 1 Answers

1. (4) The average CPI (cycles per instruction) for a certain program is 1.6. If the native MIPS rating for the program is 12.5, what is the corresponding CPU clock cycle time (i.e., the clock period) in units of nano-seconds (i.e., 10^-9 seconds)?

The Native MIPS = clock_rate / (10^6 * CPI_{avg})

So clock_rate = Native MIPS * (10^6 * CPI_{avg}) = 12.5 *(10^6 * 1.6) = 20 MHz.

Cycle time = 1/clock_rate = 1/20MHz = 0.5 * 10^-7 seconds = 50 nano-seconds.

2. Assume that MIPS instructions are processed in only 2 phases (a fetch phase and an execute phase). Each phase takes one clock cycle and, when possible, the fetch phase of one instruction is overlapped with the execute phase of another instruction. Consider the following instruction sequence:

```
lui     $2,0x4000       ; put the address 0x40000000 into register $2
lh      $8,4($2)        ; load the contents of a memory halfword into $8
lw      $9,8($2)        ; load the contents of a memory word into $9
add     $9,$9,$8        ; compute the sum of the two words
sw      $9,12($2)       ; store the sum into a third memory word
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What is the total number of clock cycles required to execute this sequence of five instructions on:

a) (4) a MIPS system with a von Neumann architecture?

A von Neumann has one memory that contains both instructions and memory data operands. Hence the execution of a memory access instruction (such as lw or sw) can't be overlapped with the fetch of any other instruction. So the instructions are processed as follows:

cycle	action
1	fetch lui
2	fetch lh and execute lui
3	execute lh $8
4	fetch lw
5	execute lw
6	fetch add
7	execute add and fetch sw
8	execute sw

So 8 clock cycles are needed.

b) (4) a MIPS system with a Harvard architecture?
The Harvard architecture includes separate instruction and data memories, each with a separate CPU to memory bus. This allows the fetch of any instruction to be overlapped with the execution of another instruction.
So the instructions are processed as follows:

cycle	action
1	fetch lui
2	fetch lh and execute lui
3	execute lh $8 and fetch lw
4	execute lw and fetch add
5	execute add and fetch sw
6	execute sw

Only 6 cycles are required to complete the entire group of the instructions.

3. (4) Which is more likely to adhere to a load/store architecture: a RISC processor or a CISC processor? Explain your answer.
Since the emphasis is on maximum speed with RISC processors and instructions that employ memory operands take longer to execute due to the time it takes to access the data memory, a RISC processor is more likely to adhere to a load/store architecture so that access to the data memory is restricted to just the load/store type instructions. This also makes the common case fast since most RISC instructions do not reference memory operands. The emphasis with CISC processors is more on flexibility, so they are more likely to use arithmetic and logic instructions that employ memory data operands.

4. A certain program runs on a MIPS processor executing a total of 7 million instructions. The CPU clock rate is 4 GHz and the average CPI for the program is 2.5.

a) (3) What is the CPU clock cycle time?
Cycle_time = 1/clock_rate = 1/(4 GHz) = 1/ $(4 * 10^{9}) = 0.25 * 10^{-9}$ or 0.25 nano-seconds

b) (4) What is the execution time required for the program? Express your answer in micro-seconds.
Execution time = IC*CPI/clock_rate = $(7*10^{6} * 2.5)/4*10^{9}$ = 4.375*10-3 seconds = 4375 micro-seconds.

c) (4) What is the numeric value for the expression: clock_rate / $(CPI*10^{6})$ for this program?
Clock_rate/$(CPI*10^{6}) = 4*10^{9}/(2.5*10^{6})$ = 4000/2.5 = 1600, which is the MIPS rating.

d) (4) Evaluate the expression IC / (execution_time$*10^{6}$) for this program (where IC is the instruction count).
$7*10^{6}/(4375*10^{-6}*10^{6}) = 7*10^{6}/4375 = 1600$

5. (5) The table below shows the number of clock cycles required to execute various types of instructions on a version of our MIPS processor:

Instruction type	Cycles consumed by the instruction
R-type	4
lw	5
sw	4
beq	3
j	3

A certain program that executes on this version of the processor executes 782000 R-type instructions, 43506 lw instructions, 36897 sw instructions, 21300 beq instructions and 7200 j (jump) instructions.
If the native MIPS rating for the program is 448, what is the corresponding CPU clock rate?
Cycles consumed = 4*782000 + 5*43506 + 4*36897 +3*21300 + 3*7200 = 3578618
CPI_{avg} = 3578618/890903 = 4.017
The Native MIPS = clock_rate / (10^6 * CPI_{avg})
So clock_rate = Native MIPS * (10^6 * CPI_{avg}) = 448 * 4.017 * 10^6 = 1799.6 * 10^6 = 1.7996 GHz

6. (10) A program that executes forty million instructions runs on a uni-processor system with a fixed clock rate of 3.333 GHz. All instructions are executed one at a time and each instruction requires an integral (i.e., whole) number of clock cycles. The average CPI rating for the instructions is 3 cycles per instruction. What is the speedup for the program obtained by reducing the average CPI from 3 down to 2?
Answer: The 3.333 GHz clock rate corresponds to a cycle time of 1/3.333GHz = 0.3 nano-seconds. If the average CPI is 3, then the execution time for the program is 3*4*10^7 * 0.3 nano-seconds = 3.6*10^7 nano-seconds. Reducing the average CPI by 1 taking it from 3 to 2 would yield an execution time of 2*4*10^7 * 0.3 nano-seconds = 2. 4*10^7 nano-seconds. Hence the speedup is 3.6/2.4 = 1.5. Speedup is the ratio of the execution time before the improvement divided by the execution time after the improvement.

7. A number of instructions from five different instruction classes are executed for a program that runs on a certain processor. The five classes along with the number of instructions executed from each class and the CPI for each class are shown in the table below:

Class	Instruction type	CPI	Millions of instructions executed
A	R-type	8	20
B	lw	12	18
C	sw	10	12
D	beq	6	10
E	j	4	6

a) (5) What is the average CPI for the program?
The total number of cycles (in millions) consumed
= 8*20 + 12*18 + 10*12 + 6*10 + 4*6 = 580
The total number of instructions executed = 20+18+12+10+6 = 66 million
So the average CPI = 580/66 = 8.79

b) (10) If each beq instruction takes 12 nano-seconds to execute, what is the total execution time for the program?
Since the beq instruction takes 6 cycles, the CPU clock period = 12ns/6 = 2ns
The execution time = number of cycles consumed * clock period (i.e., cycle time)
Execution time = 580 million * 2 ns = $580*10^6 * 2 * 10^{-9} = 1160 * 10^{-3}$ seconds
= 1.16 seconds.

c) (5) Assume that you have the option of improving only one of the instruction classes. If the improvement is by a factor of 2, which class should be chosen for improvement to achieve the greatest speedup for the program?
Improving class A by a factor of 2 would save 4*20 = 80 million cycles
Improving class B by a factor of 2 would save 6*18 = 108 million cycles
Improving class C by a factor of 2 would save 5*12 = 60 million cycles
Improving class D by a factor of 2 would save 3*10 = 30 million cycles
Improving class E by a factor of 2 would save 2*6 = 12 million cycles

Hence class B should be improved.

d) (10) If only the class A instructions are improved in the original program, what improvement factor for class A is required to yield a speedup of 1.2608695 for the program?
Speedup = T_{before} / T_{after} = $(cycles_{before})$*cycle_time / $(cycles_{after})$*cycle_time
= $cycles_{before} / cycles_{after}$ = 580 / ((8/K)*20 + 12*18 + 10*12 + 6*10 + 4*6)
= 580 / ((160/K) + 420) = 1.2608695
So (160/K) + 420 = 580/1.2608695 = 460
160/K = 460 – 420 = 40
The required improvement factor K = 160/40 = 4
So class A must be improved by a factor of 4.

8. The sub-module on Computer performance metrics defines the geometric mean and the harmonic mean as alternatives to the arithmetic mean as techniques for comparing CPU performance. Some processors, especially those used in laptops or mobile devices, are able to throttle their speed as a means of conserving power and extending battery charge. Suppose that such a processor runs in the slower low power mode executes 2,890,000 instructions for a program in 14.45 milli-seconds. Next the processor switches to the higher speed mode and executes the same program again in only 7.225 milli-seconds. Answer the following questions and show how you obtained your answer for each:

a) (4) What is the MIPS rating for the first execution of the program?
MIPS for first execution = $(2890000 / 10^6) / (14.45*10^{-3}) = 200$

b) (4) What is the MIPS rating for the second execution of the program?
MIPS for second execution = $(2890000 / 10^6) / (7.225 *10^{-3}) = 400$

c) (4) What is the arithmetic mean of the MIPS ratings for the two executions of the program?
Arithmetic mean = (200 + 400)/2 = 300

d) (4) What is the geometric mean of the two MIPS ratings?
Geometric mean = square root(200 * 400) = 282.843

e) (4) What is the harmonic mean of the two MIPS ratings?
Harmonic mean = 2 / ((1/200) + (1/400))
= 2 * 200 * 400 / 200+400 = 160000/600 = 266.67

f) (4) What is the MIPS rating for the two executions of the program if it is computed based on the total combined number of instructions in the two executions of the program and on the total combined times consumed for the two executions of the program?
MIPS = $((2890000 + 2890000) / 10^6) / (14.45*10^{-3} + 7.225*10^{-3}) = 266.67$