Sparc V8 registers

Names of registers visible to a user program at any one time:

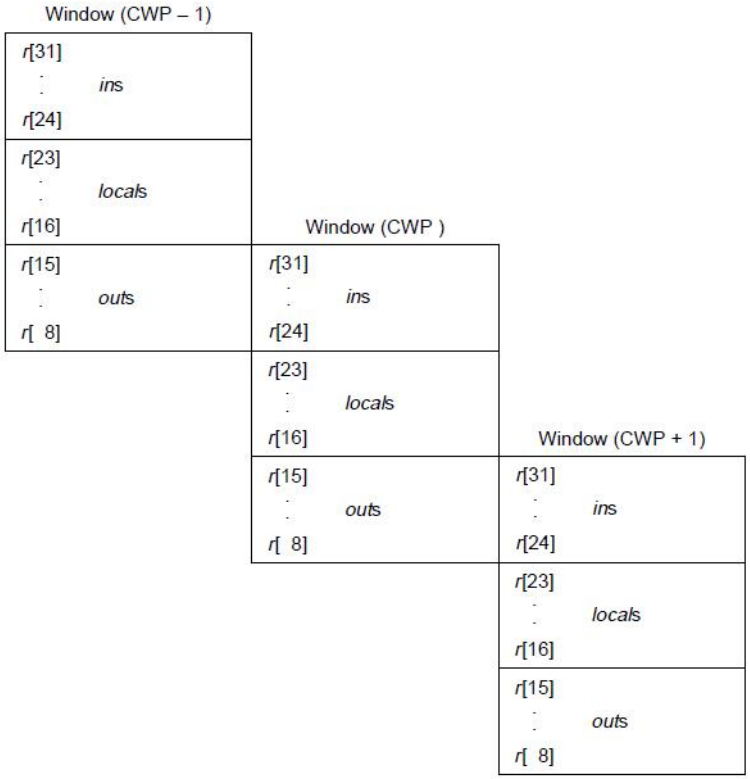
Register	Alias	Usage
%g0	%r0	Hardwired to zero
%g1	%r1	The next seven are global registers
%g2	%r2	
%g3	%r3	
%g4	%r4	
%g5	%r5	
%g6	%r6	
%g7	%r7	
%o0	%r8	First of six registers for local data and subroutine arguments
%o1	%r9	
%o2	%r10	
%o3	%r11	
%o4	%r12	
%o5	%r13	
%sp	%r14, %o6	Stack pointer
%o7	%r15	Linkage register containing subroutine return address
%l0	%r16	First of eight registers for local variables
%l1	%r17	
%l2	%r18	
%l3	%r19	
%l4	%r20	
%l5	%r21	
%l6	%r22	
%l7	%r23	

Sparc V8 registers

Caller	Callee	Usage
%o0	%i0	first argument
%o1	%i1	second argument
%o2	%i2	third argument
%o3	%i3	fourth argument
%o4	%i4	fifth argument
%o5	%i5	sixth argument
%o6	%i6	frame pointer
%o7	%i7	return address

Register Window

- Current window pointer *(CWP)*



There can be up to 32 register windows

Each window contains 24 registers

Windows can slide to pass arguments

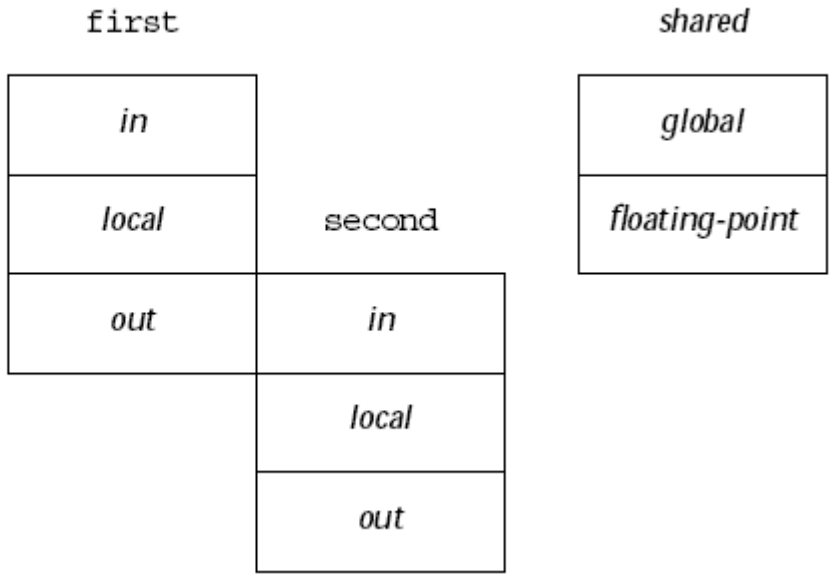
Windows overlap

CWP identifies current window

Register Window

- Example: function first calls second:

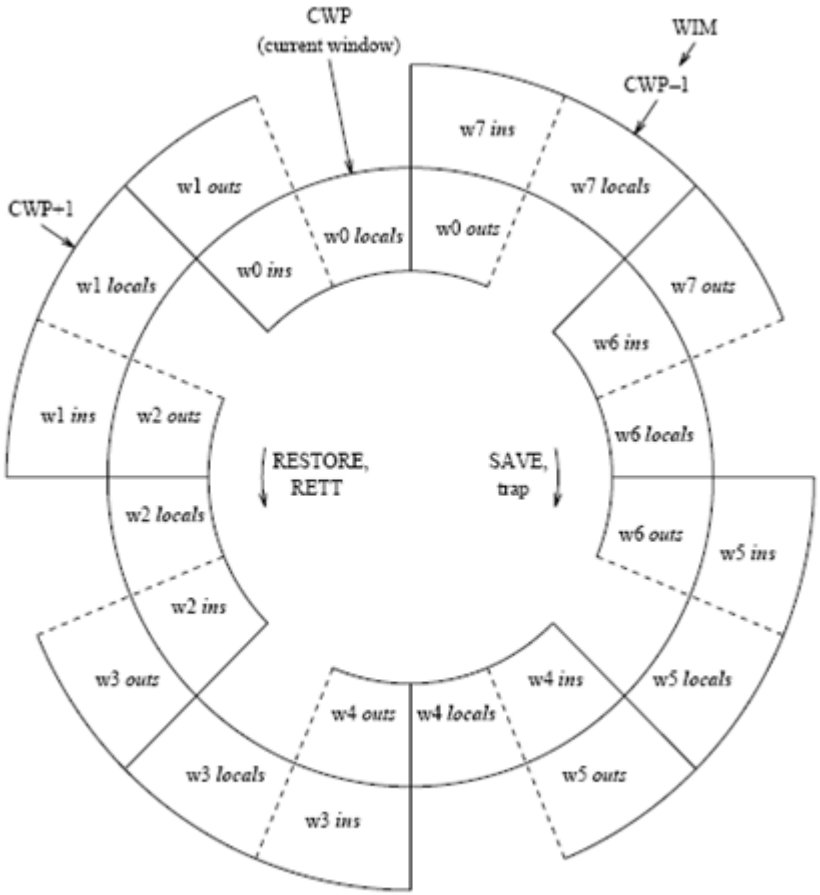
```
first()
{
    ...
    second();
    ...
}
```




```
second:
        save    %sp, -80, %sp
```

restore instruction is used to unwind stack and slide window back

Register Window



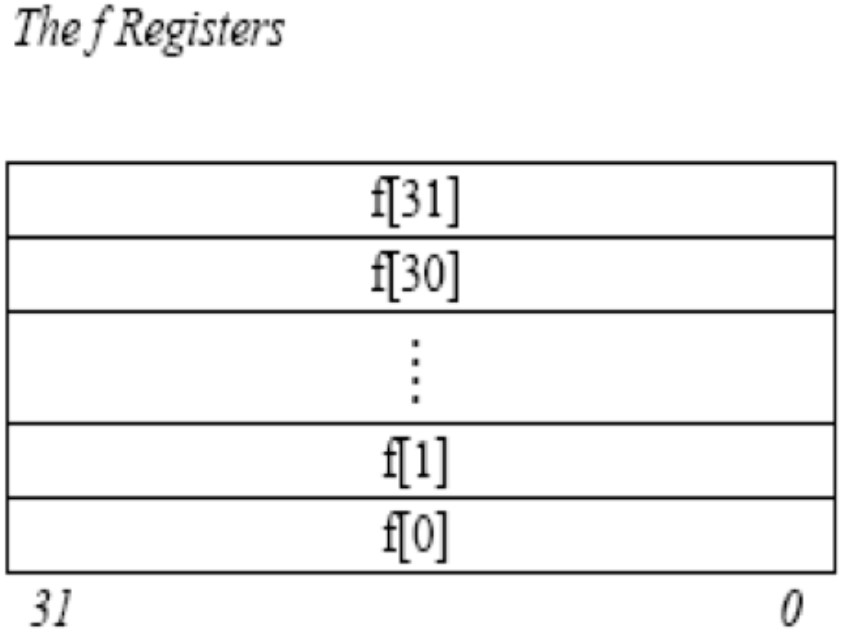
Sparc V8 registers

Special-purpose registers

PC	program counter	Holds the address of the currently executing instruction
nPC	next PC	Holds address used to fetch next instruction to be executed
PSR	processor state register	Holds state of CPU, condition codes, mode, trap enable, bit, etc.
WIM	window-invalid mask	Indicates when window underflow or overflow should occur
TBR	trap base register	Holds address of trap table and indicates trap type
Y	Y register	High part of product for mul ; high part of dividend for div
FSR	floating point state	Holds floating point mode and status, controls rounding and floating point traps

Floating Point registers

Floating point unit has a single set of 32 floating point registers



Each float register is 32 bits wide.