Memory Interleaving

A single memory module can perform 1 read or 1 write at a time

This limits performance, especially for narrow widths

Interleaving refers to how consecutive locations are distributed

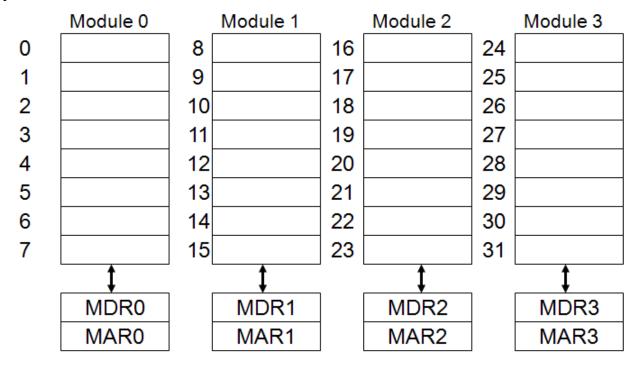
High order interleaving consecutive locations are in the same module the high order address bits indicate the module number

Module number

Offset within module

Consecutive locations must be accessed sequentially

Example: if each module is 8 bits wide, reading a 4-byte word could require 4 separate reads from the same module.



MAR is memory address register.

MDR is memory data register.

Memory Interleaving

Low order interleaving

consecutive locations are in different modules low order address bits indicate the module number high order address bits give offset into module

Offset within module

Module number

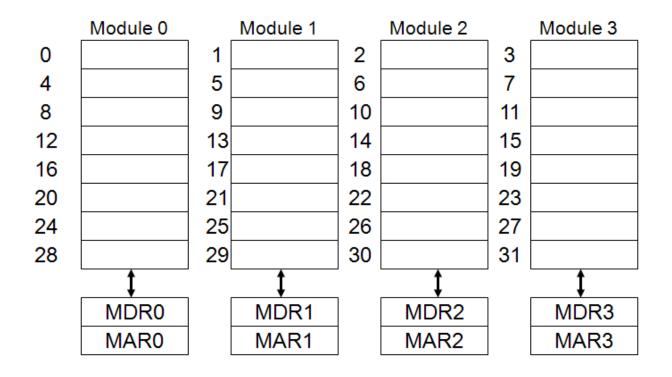
Consecutive locations can be accessed in parallel

High performance systems favor low order interleaving

Low order interleaving example:

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Bytes within each word have the same offset All four modules are read in parallel to obtain the word