Computer Science 605.411

Final Example Set 2

1. Consider a quad-core system in which each core has a separate L1 cache with a miss penalty of 20 cycles. The cores share a common L2 cache with a miss penalty of 200 cycles. Suppose that one of the cores experiences an L1 miss ratio of 5% and an L2 miss ratio of 0.5%. The core has a CPI of 1 in the absence of cache misses.

a) What is the average CPI of the core when these cache miss rates are taken into account?
The average number of cycles per instruction would be 1 plus the penalty per instruction due to the cache misses.
So the average CPI = 1 + 0.05*(20 + 0.005*200) = 1 + 1.05 = 2.05

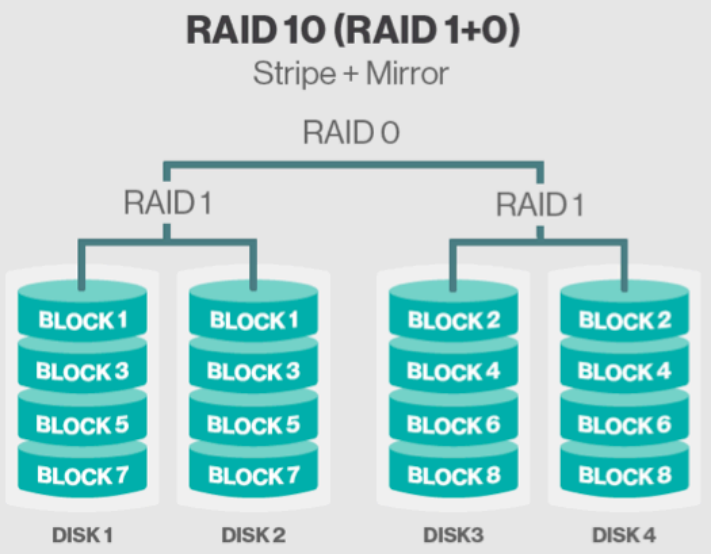
b) Suppose that miss occurs in the L1 cache every 100 cycles, how many cycles would this miss L1 rate add to the base CPI of 1?
For a base CPI of 1, an L1 miss every 100 cycles would be a miss every 100 instructions. Hence every 100 instructions would take 100 + 20 = 120 cycles which corresponds to an extra 0.2 cycles per instruction.

c) Suppose that a miss occurs in the L2 cache every 400 cycles, how many cycles would this L2 miss rate add to the base CPI of 1?
For a base CPI of 1, an L2 miss every 400 cycles would be a miss every 400 instructions. Hence for every 400 instructions the L2 miss rate would add an extra 200 cycles or 0.5 cycles per instruction. Recall that only the references that miss in the L1 cache are sent to the L2 cache.

2. How many bits would be required for each set in an 8-way set associative cache to implement a pseudo-LRU replacement algorithm?
The eight ways in a set can be viewed as a pair of 4-way groups. We know that a 3-bit pseudo-LRU scheme can be used for each group of 4 ways. A separate bit can be used to indicate which of the two 4-way groups is least recently used. Hence a total of 7 pseudo-LRU bits are required.

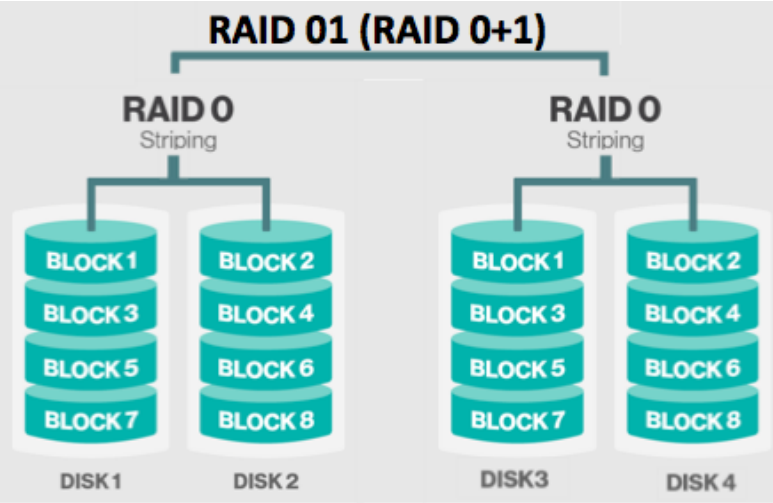
3. For processors that require one or more cycles to execute each instruction, the performance can be defined in terms of the average number of cycles per instruction (CPI). However, for processors that execute more than one instruction per cycle, a better definition of performance would be based on the average number of instructions completed per cycle (IPC) . Write down an expression for performance as a function of IPC, clock rate(CR) and instruction count (IC).
Performance = ___(IPC*CR) / IC ___
By definition performance = 1/execution_time = 1/(IC*CPI*cycle_time)
= 1/(IC * CPI * 1/CR) = 1/ (IC * 1/IPC * 1/CR) = 1/(IC/(IPC*CR))
= (IPC*CR) / IC

4. Suppose that each of the 4 processors in an SMP (shared memory multi-processor) system is rated at 200 MIPS, what would be the apparent MIPS rating for a program that can be partitioned into four independent parts (A, B, C and D) where part A accounts for 35% of the instructions in the program, part B accounts for 48%, part C accounts for 12%, and Part D accounts for 5%?
The four parts would be executed in parallel. The time required to execute the program would correspond to the longest part (part A), which is T= 0.48*IC/200 MIPS. So the apparent MIPS rating would be IC/T = 200 MIPS/0.48 = 416.67 MIPS.5. a) How many stripe controllers and how many mirror controllers are required for the RAID 10 system shown below?



Two mirror controllers are required (one for each of the two mirrored pairs) and one stripe controller is required to manage the RAID 0 striping.

b) How many stripe controllers and how many mirror controllers are required for the RAID 01 system shown below?



Two stripe controllers are required (one for each of the two RAID 0 systems) and one mirror controller for the RAID 0 mirror images.

c) How many disks would the operating system see with the RAID10 and RAID01 systems shown above?

Although each strip controller sees two disks and each mirror controller sees two disks, each system will appear as a single disk to the operating system.