Module 12

Operating System

Module Twelve

- Operating System - Part Two
- In this presentation, we are going to talk about :

  Interrupt Processing

Overview

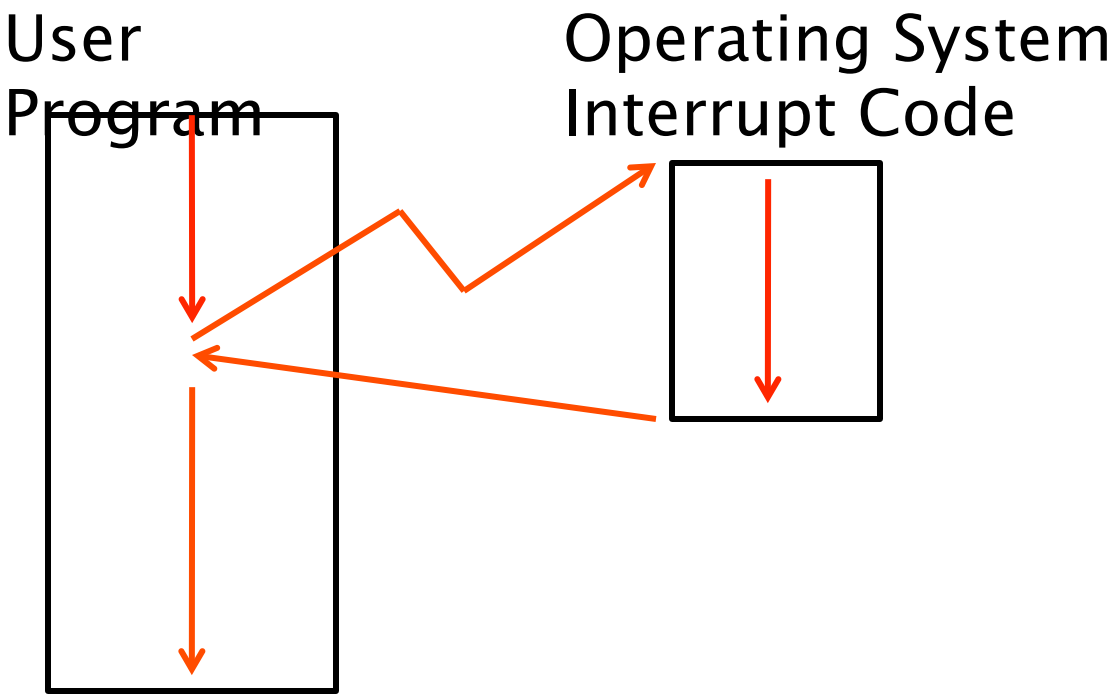
- Previously we talked about:
  - Basic Operating System Functions
  - Components

Now: Interrupt Processing

Interrupt

- An Interrupt is an external signal that an event has occurred.
- In the computer, the interrupt causes the normal flow of instruction processing to be changed.
- Control of the CPU is transferred to the interrupt processing routine of the Operating System.
- Asynchronous

Interrupt Process

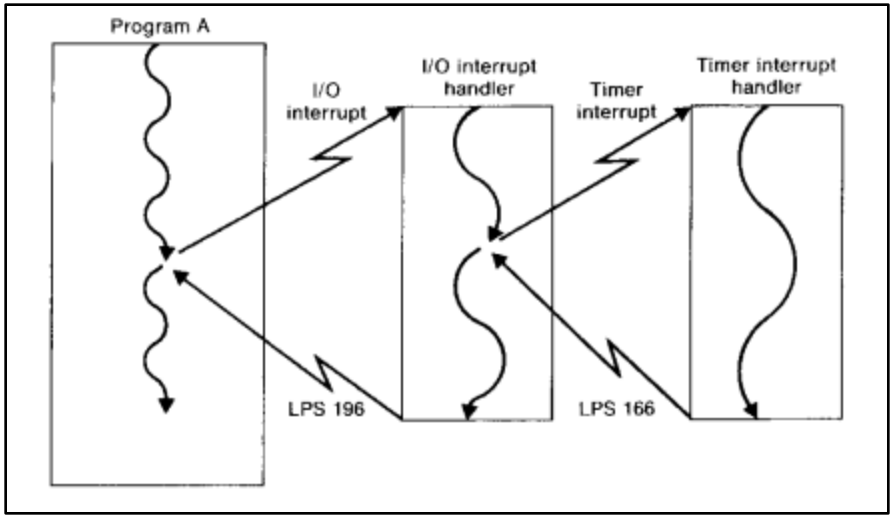


Interrupt

- An Interrupt is an external signal that an event has occurred
- Asynchronous
- Hardware saves the program status and register contents.
- Interrupt processing routine completes.
- Control is returned to the program.

Classes of Interrupts

- While the I/O interrupt handler code is processing, the Timer interrupt happens.
- Higher priority
- Switch to that handler code.
- Then complete I/O interrupt.

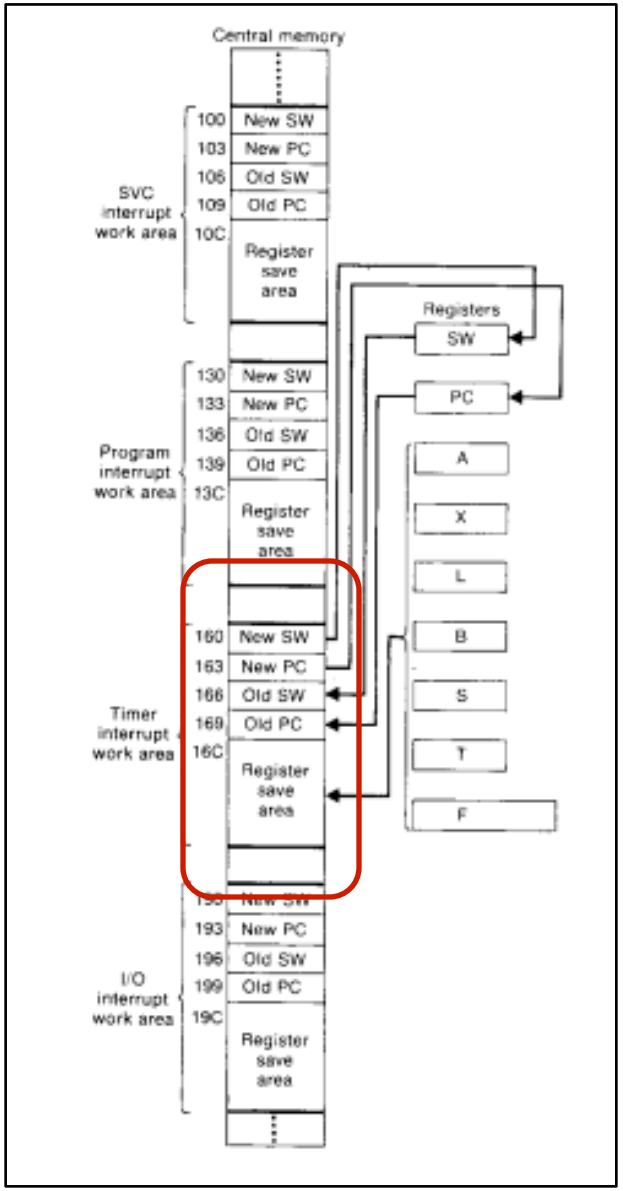


Classes of Interrupts

- As an example:
  - 1 - SVC — request a service from the Operating System
  - 2 - Program — program execution error / fault / exception
  - 3 - Timer — time slice timer runs out and ‘rings’
  - 4 - I / O — input or output request complete

Interrupt Processing

- Fixed work area in main memory
- Register content stored
- Status Word and Program Counter loaded
- Processing of the interrupt
- Load Processor Status instruction used to send control to interrupt handler program



MIPS Program Status Word Details

- From Appendix B (p.B-33)

- Status register
- Interrupt enable
- Exception level
- User mode
- Interrupt Mask - which interrupts to allow

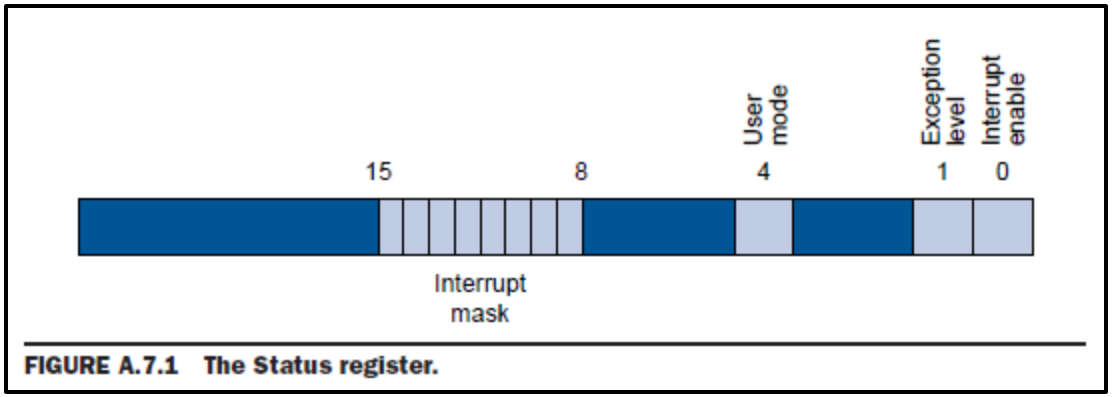


FIGURE A.7.1 The Status register.

More MIPS Details

- What is the reason? How to process

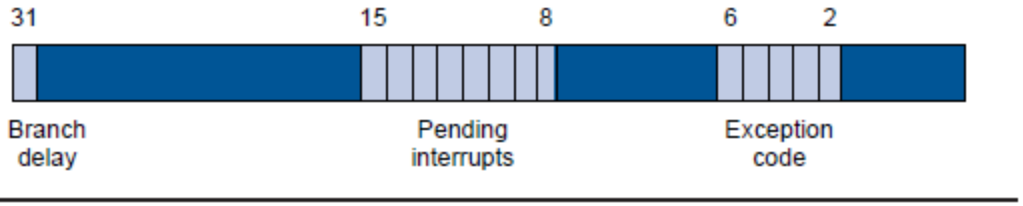


FIGURE A.7.2 The Cause register.

Number	Name	Cause of exception
0	Int	interrupt (hardware)
4	AdEL	address error exception (load or instruction fetch)
5	AdES	address error exception (store)
6	IBE	bus error on instruction fetch
7	DBE	bus error on data load or store
8	Sys	syscall exception
9	Bp	breakpoint exception
10	RI	reserved instruction exception
11	CpU	coprocessor unimplemented
12	Ov	arithmetic overflow exception
13	Tr	trap
15	FPE	floating point

Summary

- An Interrupt is an external signal that an event has occurred.
- Asynchronous – not predictable in real time.
- Hardware saves the program status and register contents.
- Control of the processor is transferred to the interrupt processing routine code of the Operating System.
- Interrupt processing routine completes.
- Operating System returns processor control to the program.

- Next: Process Scheduling

  I/O Supervision