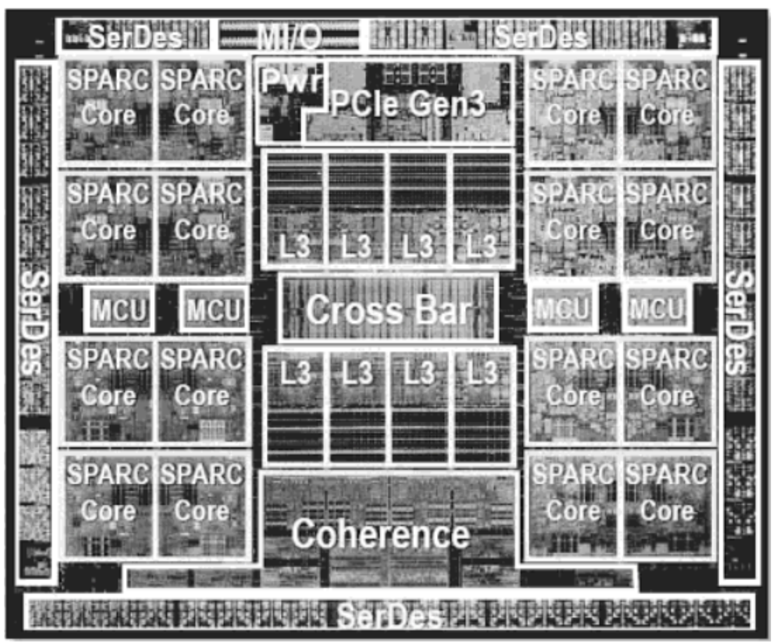
Example Set 6

1. What is a multi-core architecture?

A multi-core architecture is one in which multiple processor cores are integrated on a single die (i.e., chip).

A processor core or CPU is a processing element capable of independently fetching and executing instructions from at least one instruction stream. The core typically includes logic such as an instruction fetch unit, a program counter, instruction scheduler, functional units, register file, etc.

An example of a multi-core system (the Oracle T5) with 16 cores on a single die is shown below:



2. What is a parallel architecture computer?

A parallel computer is a collection of processing elements that communicate and co-operate to solve a large problem fast.

The processing elements can be CPU's where each CPU is a separate chip or they may correspond to separate cores on a single chip. Early parallel computers employed separate CPU chips because the density of transistors on chips was relatively low compared to more recent modern systems.

3. What is the main characteristic of a vector processor or core?

The main characteristic is that the core applies the same operation to multiple data items simultaneously. It fetches instructions using a single program counter. For example, a vector addition instruction reads elements from two arrays and performs a pairwise add of elements from the two arrays and writes the sums into a third array.

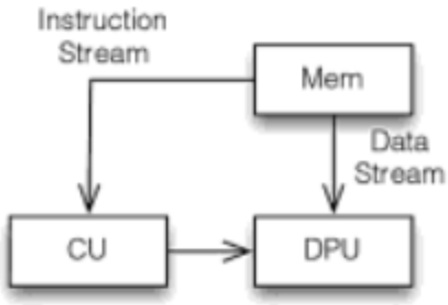
4. What are the categories defined by Flynn's taxonomy of parallel computers?

They are SISD, SIMD, MISD and MIMD as shown below:

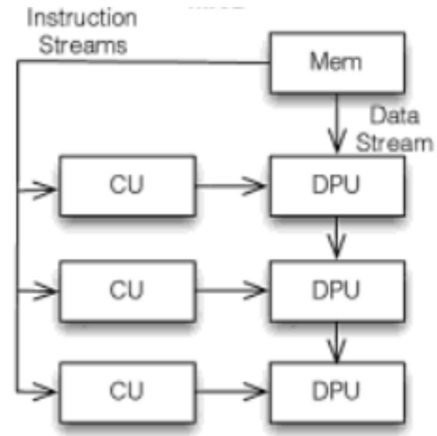
		Number of Data Streams	
		Single	Multiple
Number of Instruction Streams	Single	***SISD***	***SIMD***
	Multiple	***MISD***	***MIMD***

5. Label each of the diagrams below, as a SISD, SIMD, MISD or MIMD system. “CU” means control unit and “DPU” means data processing unit.

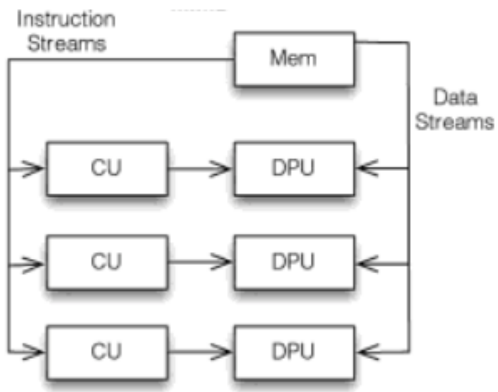
a)



b)



c)



d)

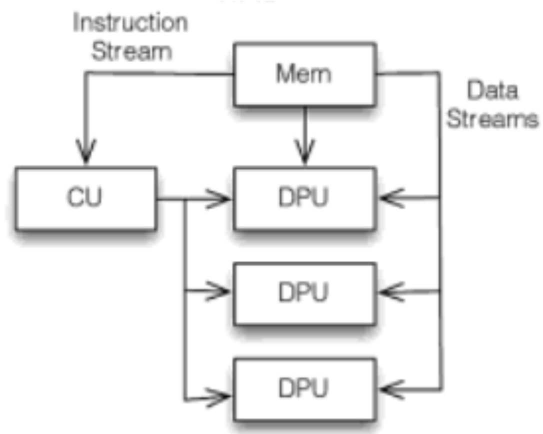
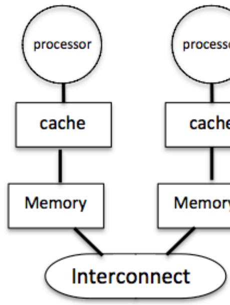
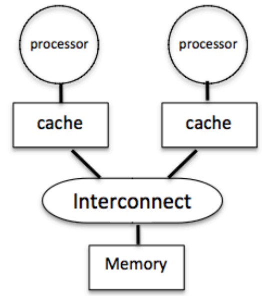


Diagram a) is corresponds to SISD, b) corresponds to MISD, c) corresponds to MIMD and d) corresponds to SIMD.

6. Each of the following diagrams represents a version of a MIMD system. Label each one as UMA, NUMA or NORMA.

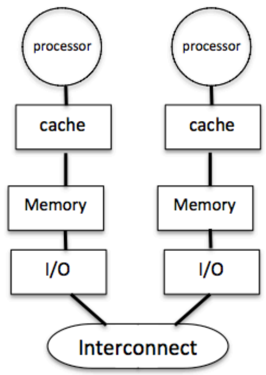
a)

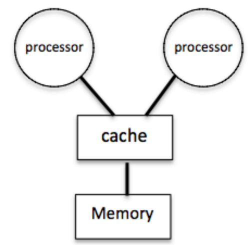




b)

c)





d)

a) NUMA (non-uniform memory access) Accessing memory via the interconnect takes longer than not using the interconnect.

b) UMA (uniform memory access) Each processor takes the same time to access memory.

c) NORMA (no remote memory access, also called a cluster or distributed processing system). Each processor must issue a request to access the memory owned by a remote processor. It can only directly access is own local memory.

d) UMA (uniform memory access with a shared cache). The processors take the same amount of time to access a shared memory and cache.

7. What are some of the factors that motivated the switch to multi-core processors?

Over the years a number of techniques and approaches have been used to increase the performance of single processors. These include pipelining and superscalar operation. The faster switching speeds and higher densities of transistors that can be implemented on a chip made it possible to greatly increase the processor's clock rate. It also made it possible to implement the complex logic needed to manage the dynamic instruction scheduling required for the out-of-order issue and completion of instructions.

The time and effort required to design, test and verify these complex logic systems grew to the point that incremental improvements in the performance became too costly for many systems.

The power consumed by such high-speed logic and the heat produced became a limiting factor. In some cases the power consumption and required heat dissipation increased by a factor of 100 or more.

Multi-core (also called chip multiprocessor or CMP) systems offered an alternative use for the higher transistor densities. Instead of using the logic to implement sophisticated highly pipelined dynamic instruction scheduling superscalar systems, multiple copies of processors with simpler designs that took less time and effort to design and verify were simply stamped onto a single chip. These "cores" run at lower clock rates, have pipelines with fewer stages, and do not require special cooling to keep them operating correctly. Comparable throughput and performance can be achieved with these multi-core or CMP systems as with the more costly high-end single processor superscalar systems.