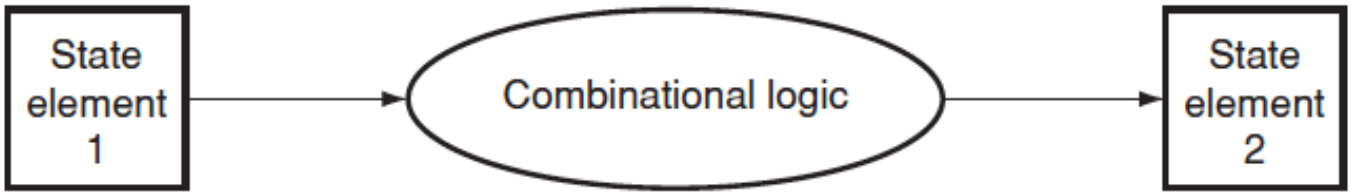
Memory Implementation

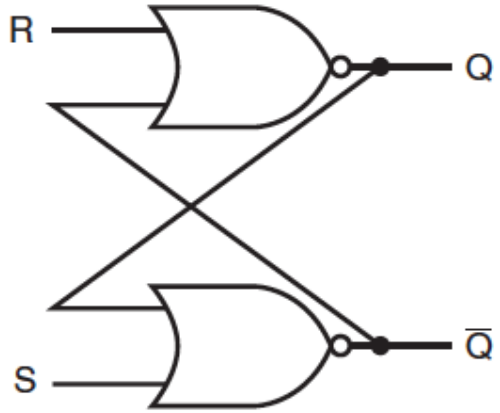
- Combinational logic circuits need state elements to:
  - provide inputs
  - store the output
- State elements are sequential logic devices
  - Their output depends on the history of the inputs
- Combinational logic output depends only on current inputs



- State changes occur at clock edges

S-R Latch

A 1-bit memory device must capture and store its input



Cross coupled NOR gates

S and R are the inputs

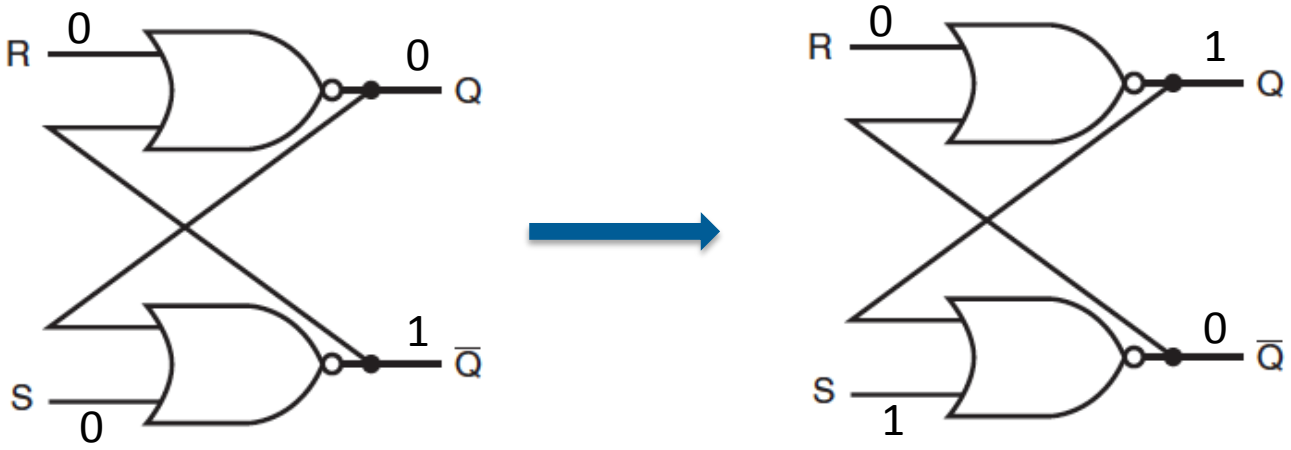
The value of the output Q defines the state (0 or 1)

$\overline{Q}$ (NOT Q) is the other output

Outputs do not change as long as S and R are both 0

S-R Latch

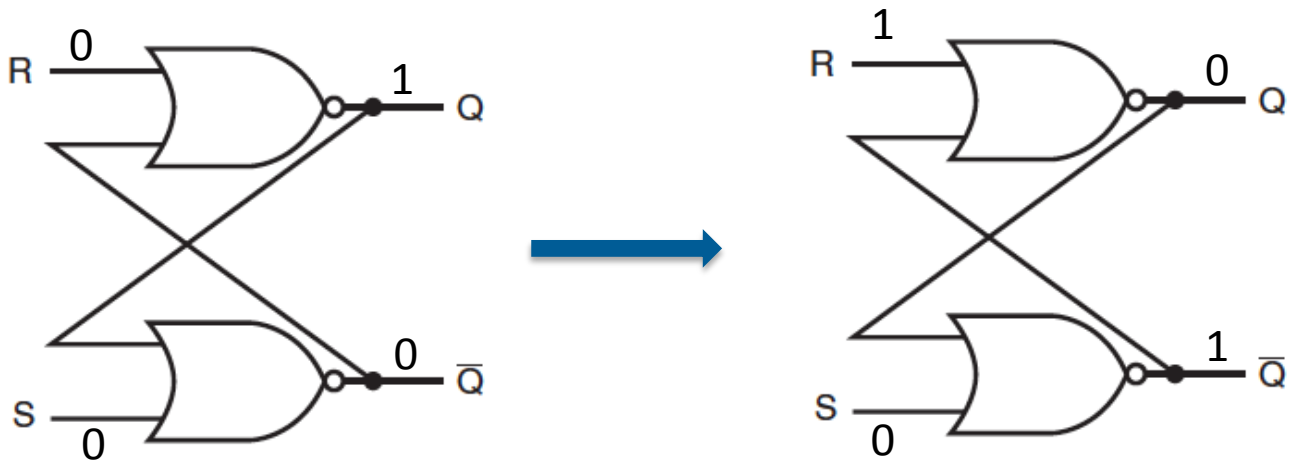
In state 0, if S changes from 0 to 1, Q becomes 1



When S goes back to 0, Q retains its new value of 1

S-R Latch

In state 1, if R changes from 0 to 1, Q resets to 0



When R goes back to 0, Q retains its new value of 0

S-R Latch

Behavior of the S-R Latch is described by a *characteristic table*
Defines output at t+1 (next cycle) as function of inputs at t

S	R	Q(t+1)
0	0	Q(t) no change
0	1	0
1	0	1
1	1	? unpredictable

Differs from truth table which shows output for current cycle

S-R Flip-Flop

S-R Latch

- Sets Q = 1 if S is asserted while clock is asserted
- Sets Q = 0 if R is asserted while clock is asserted

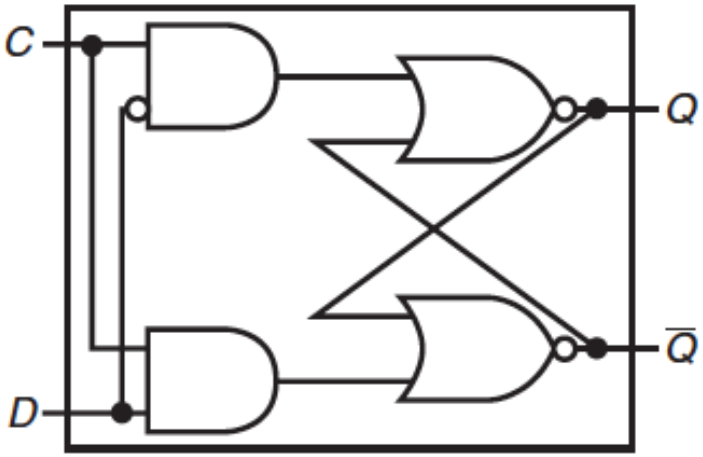
S-R flip-flop

- Sets Q = 1 if S is asserted at clock edge
- Sets Q = 0 if R is asserted at clock edge

D Latch

What is needed for single bit storage device is a D latch or flip-flop

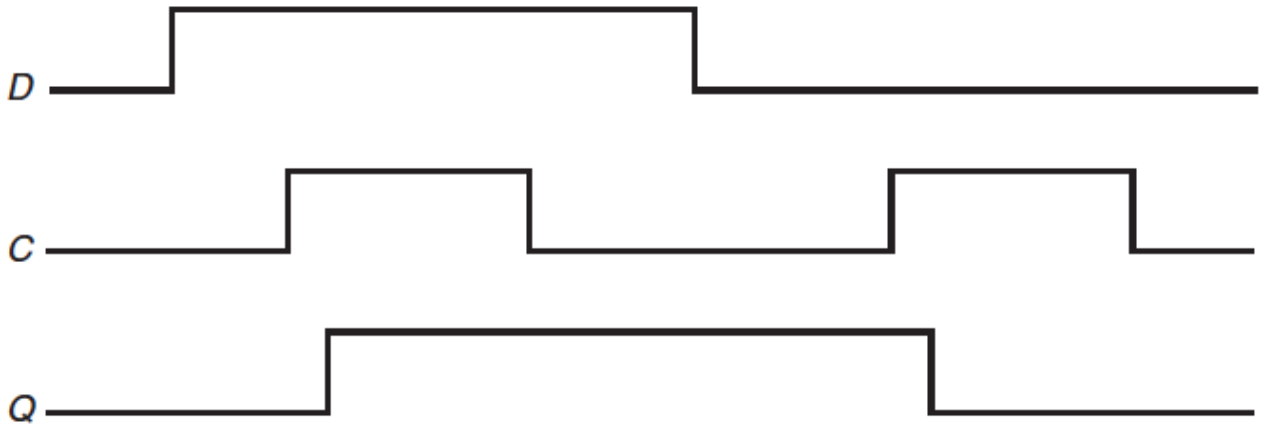
D Latch has single data input and a clock input



The two AND gates open when C (clock) is high

Setting D=1 has same effect as S=1 and R=0 with S-R latch
Setting D=0 has same effect as R=1 and S=0 with S-R latch

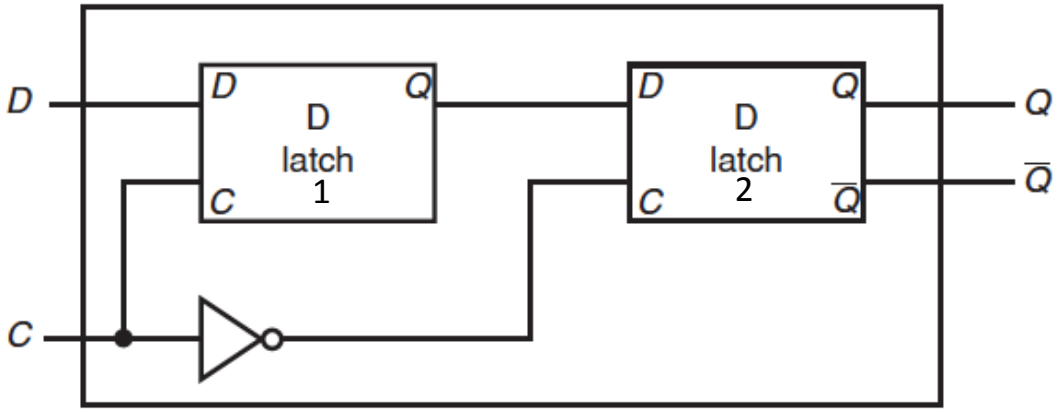
D Latch Behavior



When C, the clock, is high, Q takes on the same value as D

D Flip-Flop

D flip-flop (with falling edge trigger)



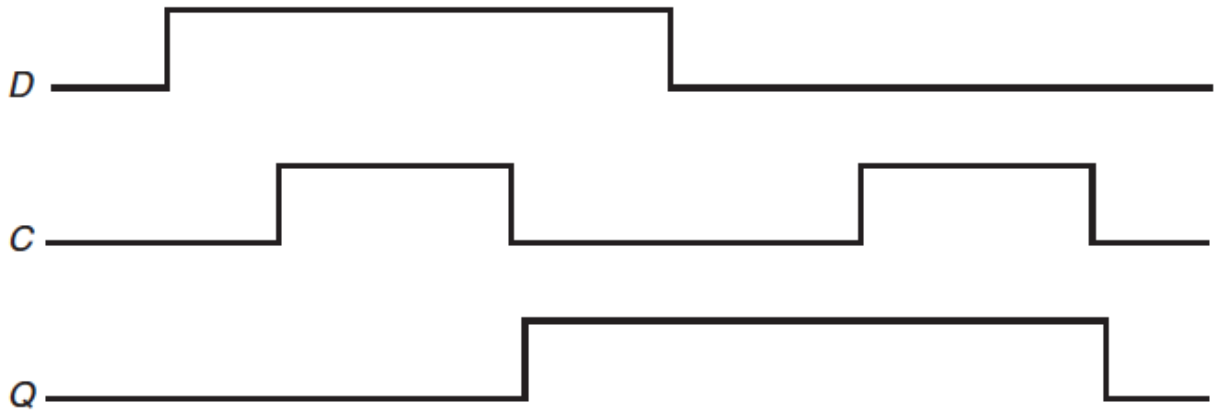
When C is high, latch 1 passes its input (D) to its output

When C goes low:

- output from latch 1 is retained
- Latch 2 passes output from latch 1 on to latch 2's output

Q only changes when clock goes high and back low

D Flip-Flop Behavior



Output Q changes at trailing clock edge in this example

The alternative would be leading edge trigger

As long as power is applied, the stored bit is retained