lab6 - [C:/Xilinx_projects/lab6/lab6.xpr] - Vivado 2019.1.3

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Implementation Complete

10 us

Default Layout

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SIMULATION | Behavioral Simulation - Functional - sim_1 - c17_tb | Post-Implementation Simulation - Timing - sim_1 - c17_tb

Objects | Protocol Instances | Scope | Sources

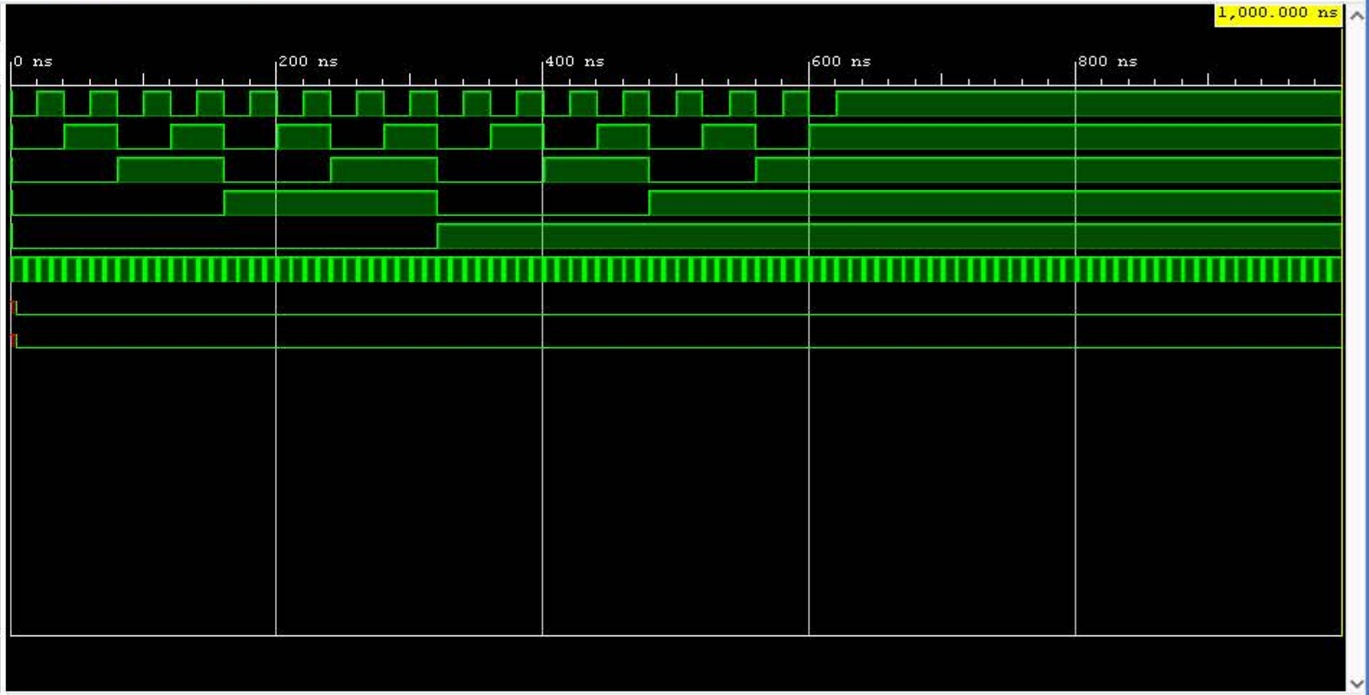
c17.v | c17_tb.v

C:/Xilinx_projects/lab6/lab6.srcs/sources_1/new/c17

```
1  `timescale 1ns / 1ps
2
3  //Design 1 of 4 - No pipelining
4
5  module c17 (N1,N2,N3,N6,N7,N22,N23);
6  input N1,N2,N3,N6,N7;
7  output N22,N23;
8  wire N10,N11,N16,N19;
9  nand NAND2_1 (N10, N1, N3);
10 nand NAND2_2 (N11, N3, N6);
11 nand NAND2_3 (N16, N2, N11);
12 nand NAND2_4 (N19, N11, N7);
13 nand NAND2_5 (N22, N10, N16);
14 nand NAND2_6 (N23, N16, N19);
15
16
17 //Design 2 of 4 - Single stage pipel
18 /*
19 module c17(N1,N2,N3,N6,N7,N22q,N23q,
20 input N1,N2,N3,N6,N7,clk;
21 output N22q,N23q;
22 wire N10,N11,N16,N19;
23 reg N1q,N3q,N6q,N2q,N7q,N22q,N23q;
24 wire N22,N23;
25 nand NAND2_1 (N10, N1q, N3q);
26 nand NAND2_2 (N11, N3q, N6q);
```

Untitled 8

#	Name	Value
1	N1	1
2	N2	1
3	N3	1
4	N6	1
5	N7	1
6	clk	0
7	N22	0
8	N23	0



Tcl Console | Messages | Log

```
# run 1000ns
INFO: [USF-XSim-96] XSim completed. Design snapshot 'c17_tb_time_impl' loaded.
INFO: [USF-XSim-97] XSim simulation ran for 1000ns
launch_simulation: Time (s): cpu = 00:00:05 ; elapsed = 00:00:09 . Memory (MB): peak = 2012.176 ; gain = 0.000
```

Type a Tcl command here

Sim Time: 1 us

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Implementation Complete

10 us

Default Layout

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SIMULATION | Behavioral Simulation - Functional - sim_1 - c17_tb | Post-Implementation Simulation - Timing - sim_1 - c17_tb

Objects | Protocol Instances | Scope | Sources

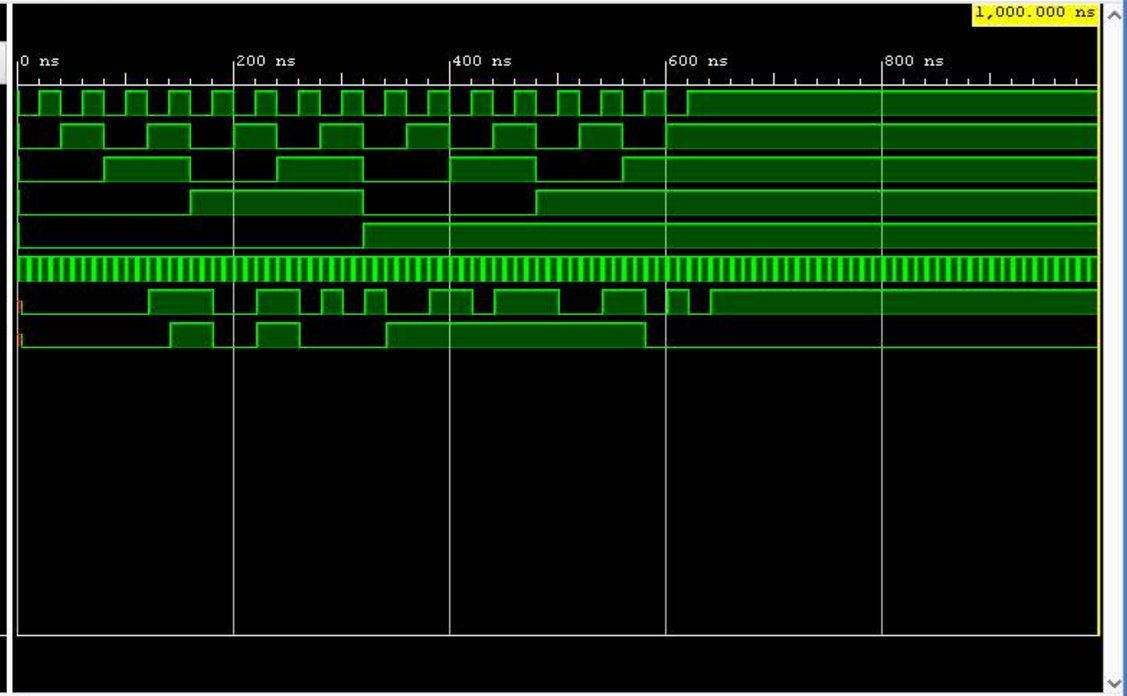
c17.v

C:/Xilinx_projects/lab6/lab6.srcs/sources_1/new/c17.v

```
18
19  //Design 2 of 4 - Single stage pipeline (at inputs and outpu
20
21  module c17(N1,N2,N3,N6,N7,N22q,N23q,clk);
22  input N1,N2,N3,N6,N7,clk;
23  output N22q,N23q;
24  wire N10,N11,N16,N19;
25  reg N1q,N3q,N6q,N2q,N7q,N22q,N23q;
26  wire N22,N23;
27  nand NAND2_1 (N10, N1q, N3q);
28  nand NAND2_2 (N11, N3q, N6q);
29  nand NAND2_3 (N16, N2q, N11);
30  nand NAND2_4 (N19, N11, N7q);
31  nand NAND2_5 (N22, N10, N16);
32  nand NAND2_6 (N23, N16, N19);
33  always @ (posedge clk) begin
34      N1q <= N1;
35      N3q <= N3;
36      N6q <= N6;
37      N2q <= N2;
38      N7q <= N7;
39      N22q <= N22;
40      N23q <= N23;
41  end
42
43
```

Untitled 2

#	Name	Value
1	N1	1
2	N2	1
3	N3	1
4	N6	1
5	N7	1
6	clk	0
7	N22q	1
8	N23q	0



Tcl Console | Messages | Log

```
# run 1000ns
INFO: [USF-XSim-96] XSim completed. Design snapshot 'c17_tb_time_impl' loaded.
INFO: [USF-XSim-97] XSim simulation ran for 1000ns
launch_simulation: Time (s): cpu = 00:00:18 ; elapsed = 00:00:16 . Memory (MB): peak = 2009.086 ; gain = 176.871
```

Type a Tcl command here

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SIMULATION | Behavioral Simulation - Functional - sim_1 - c17_tb | Post-Implementation Simulation - Timing - sim_1 - c17_tb

Objects | Protocol Instances | Scope | Sources

c17.v | c17_tb.v

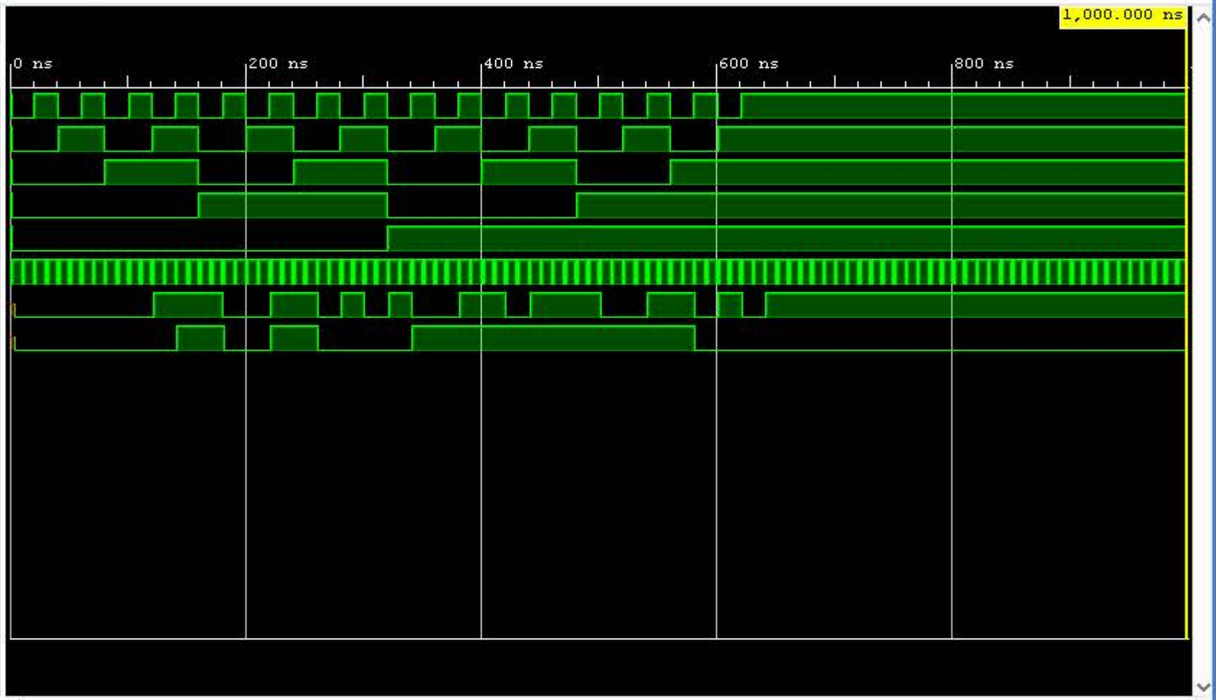
C:/Xilinx_projects/lab6/lab6.srcs/sources_1/new/c17.v

```
43
44  //Design 3 of 4 - Two pipeline stages (additionall
45
46  module c17(N1,N2,N3,N6,N7,N22q,N23q,clk);
47  input N1,N2,N3,N6,N7,clk;
48  output N22q,N23q;
49  wire N10,N11,N16,N19;
50  wire N22,N23;
51  reg N1q,N3q,N6q,N2q,N7q,N22q,N23q,N10q,N11q,N19q;
52  nand NAND2_1 (N10, N1q, N3q);
53  nand NAND2_2 (N11, N3q, N6q);
54  nand NAND2_3 (N16, N2q, N11q);
55  nand NAND2_4 (N19, N11q, N7q);
56  nand NAND2_5 (N22, N10q, N16);
57  nand NAND2_6 (N23, N16, N19q);
58  always @ (posedge clk) begin
59      N1q <= N1;
60      N3q <= N3;
61      N6q <= N6;
62      N2q <= N2;
63      N7q <= N7;
64      N22q <= N22;
65      N23q <= N23;
66      N10q <= N10;
67      N11q <= N11;
68      N19q <= N19;
```

Untitled 4

1,000.000 ns

#	Name	Value
1	N1	1
2	N2	1
3	N3	1
4	N6	1
5	N7	1
6	clk	0
7	N22q	1
8	N23q	0



Tcl Console | Messages | Log

```
# run 1000ns
INFO: [USF-XSim-96] XSim completed. Design snapshot 'c17_tb_time_impl' loaded.
INFO: [USF-XSim-97] XSim simulation ran for 1000ns
launch_simulation: Time (s): cpu = 00:00:04 ; elapsed = 00:00:09 . Memory (MB): peak = 2012.176 ; gain = 0.000
```

Type a Tcl command here

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SIMULATION | Behavioral Simulation - Functional - sim_1 - c17_tb | Post-Implementation Simulation - Timing - sim_1 - c17_tb

Objects | Protocol Instances | Scope | Sources

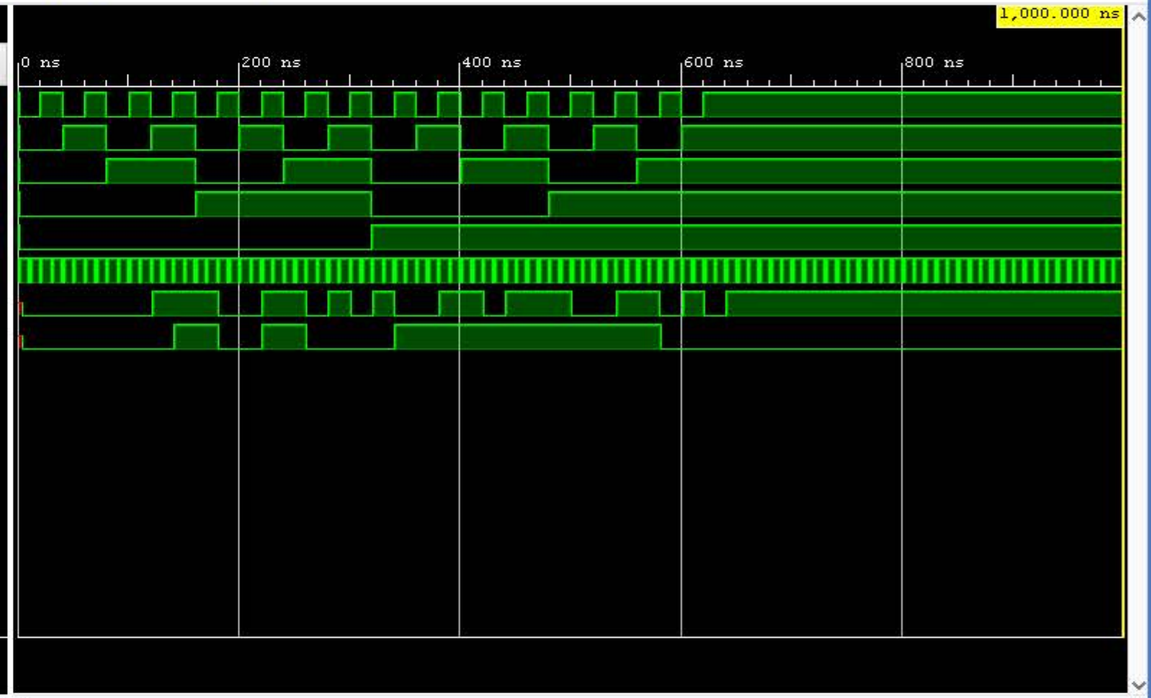
c17.v | c17_tb.v

C:/Xilinx_projects/lab6/lab6.srcs/sources_1/new/c17.v

```
73
74  module c17(N1,N2,N3,N6,N7,N22q,N23q2,clk);
75  input N1,N2,N3,N6,N7,clk;
76  output N22q,N23q2;
77  reg N1q,N3q,N6q,N2q,N7q,N22q,N10q,N11q,N19q,N16q,N23q1,N2
78  wire N10,N11,N16,N19;
79  wire N22,N23;
80  nand NAND2_1 (N10, N1q, N3q);
81  nand NAND2_2 (N11, N3q, N6q);
82  nand NAND2_3 (N16, N2q, N11q);
83  nand NAND2_4 (N19, N11q, N7q);
84  nand NAND2_5 (N22, N10q, N16q);
85  nand NAND2_6 (N23, N16q, N19q);
86  always @ (posedge clk) begin
87      N1q <= N1;
88      N3q <= N3;
89      N6q <= N6;
90      N2q <= N2;
91      N7q <= N7;
92      N22q <= N22;
93      N23q1 <= N23;
94      N23q2 <= N23q1;
95      N10q <= N10;
96      N11q <= N11;
97      N19q <= N19;
98      N16q <= N16;
```

Untitled 6

#	Name	Value
1	N1	1
2	N2	1
3	N3	1
4	N6	1
5	N7	1
6	clk	0
7	N22	1
8	N23	0



Tcl Console | Messages | Log

```
# run 1000ns
INFO: [USF-XSim-96] XSim completed. Design snapshot 'c17_tb_time_impl' loaded.
INFO: [USF-XSim-97] XSim simulation ran for 1000ns
launch_simulation: Time (s): cpu = 00:00:15 ; elapsed = 00:00:14 . Memory (MB): peak = 2012.176 ; gain = 0.000
```

Type a Tcl command here

Sim Time: 1 us