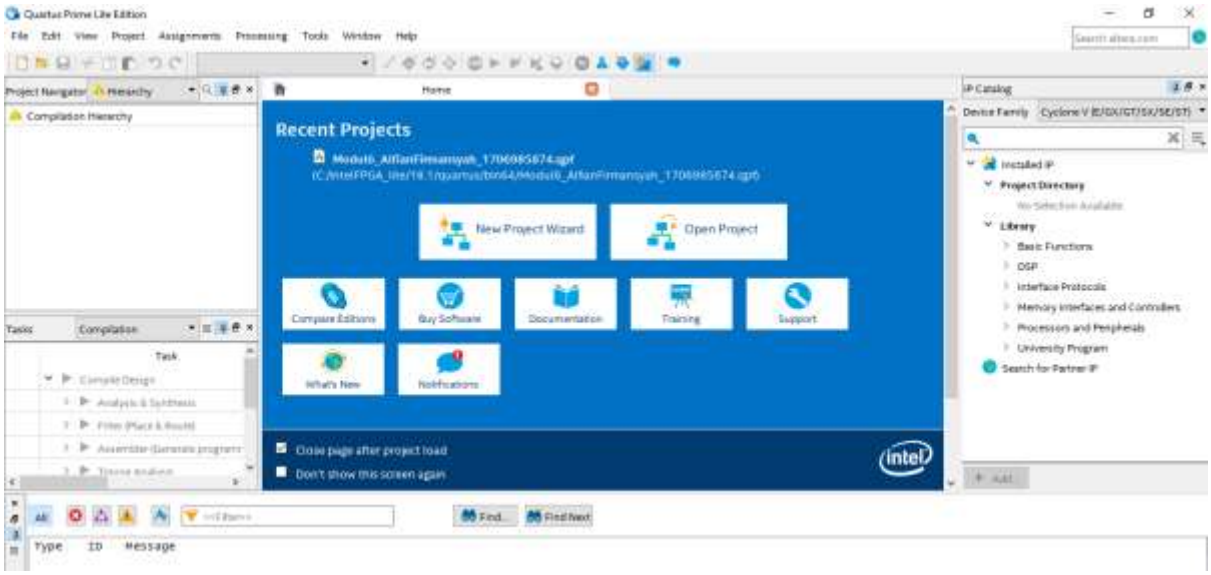
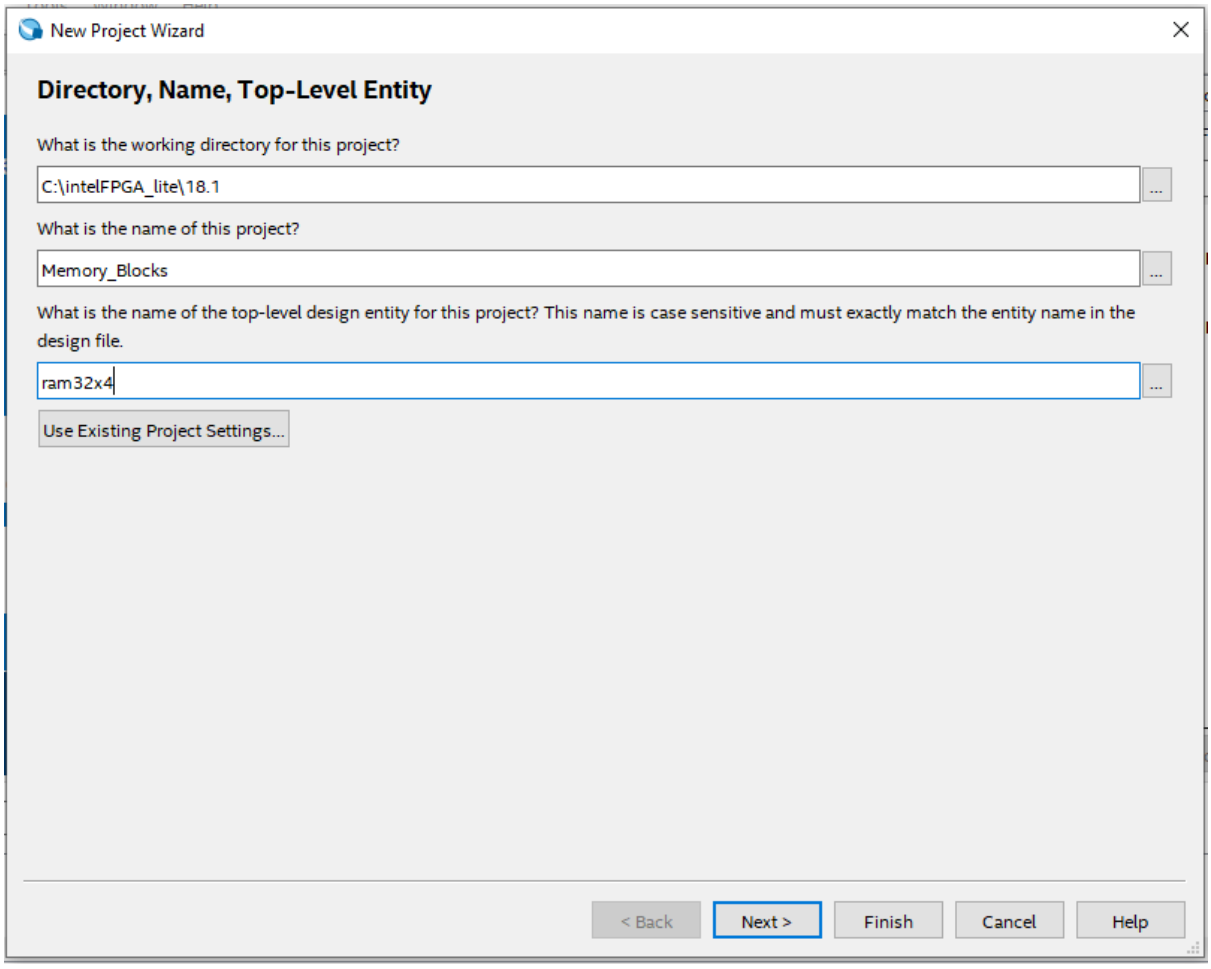
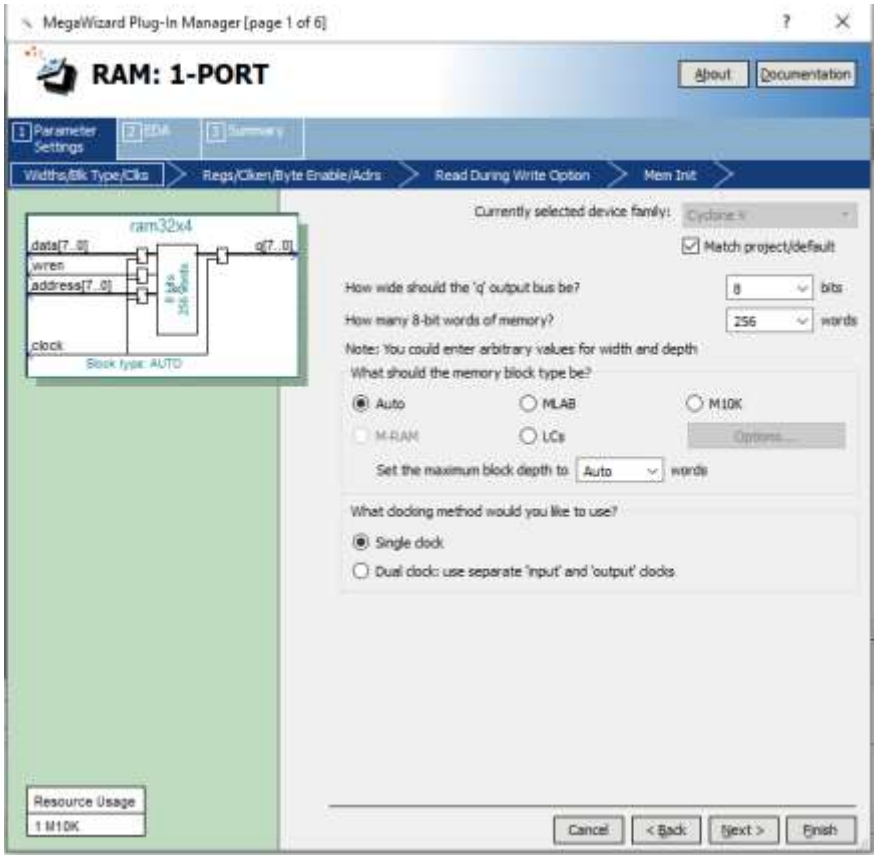
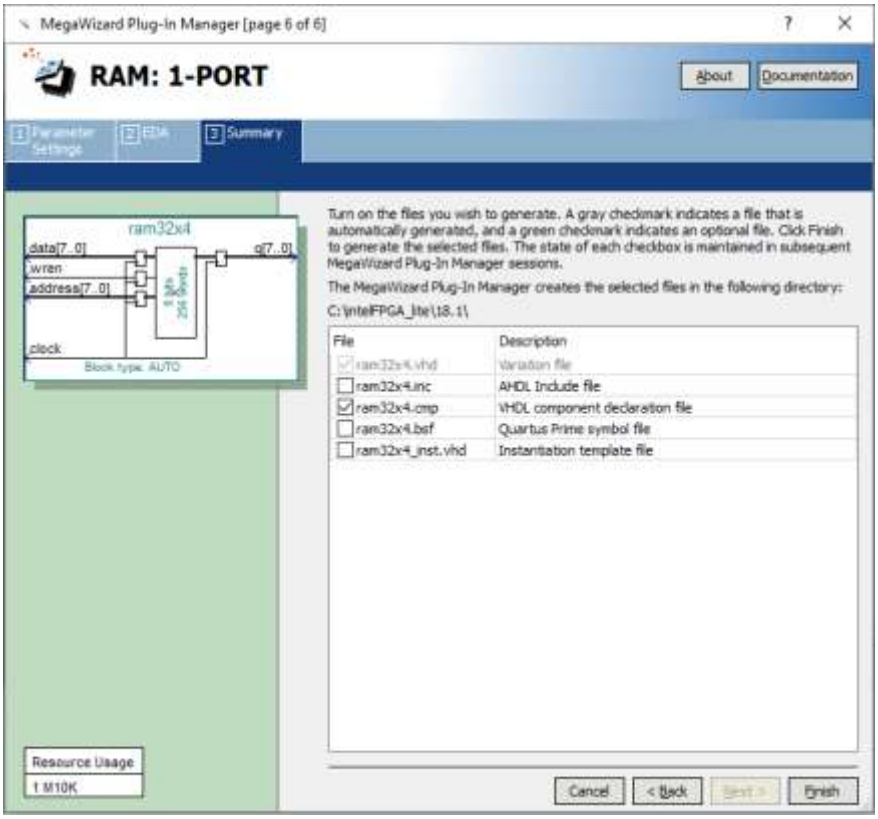
Memory block yang berisi kalkulator Tambah

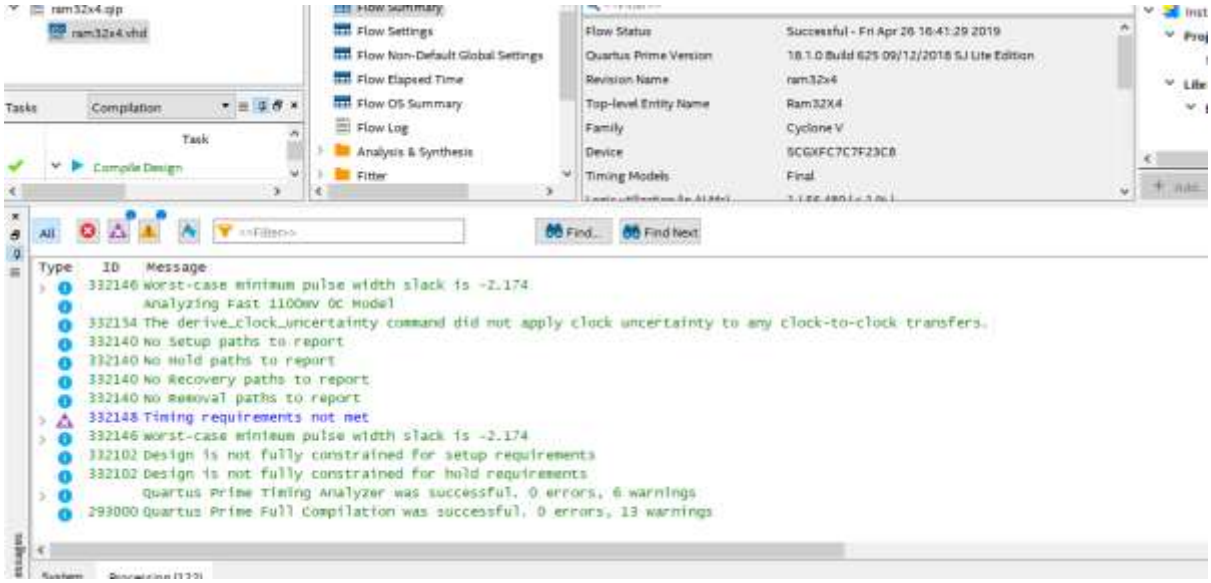




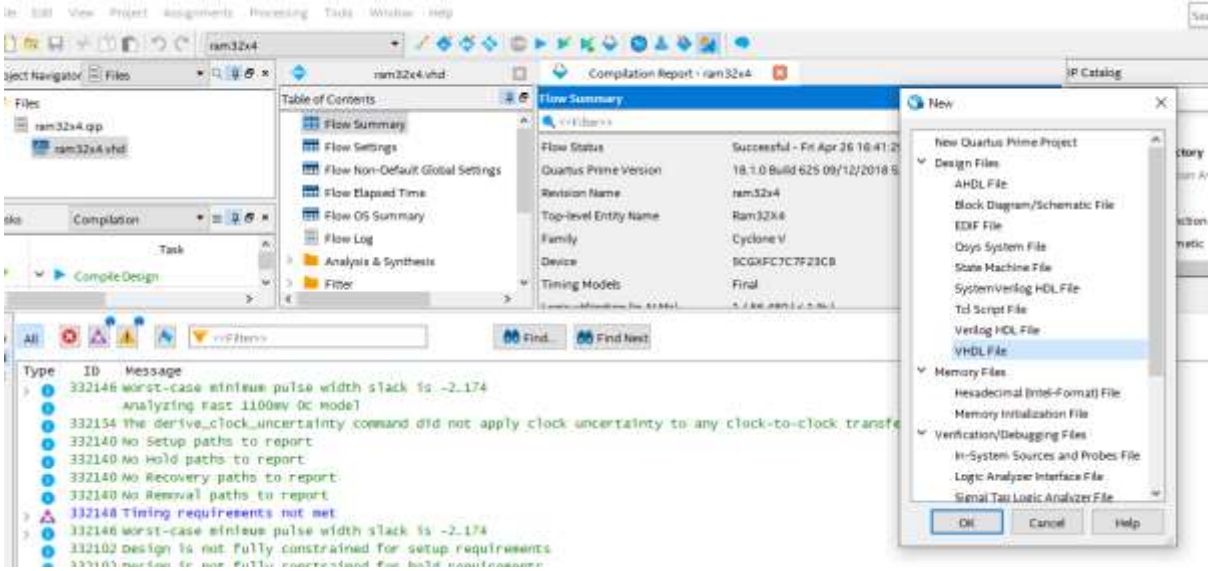

MegaWizard Plug-In Manager [page 1 of 6]
RAM: 1-PORT
About
Documentation
1 Parameter Settings
2 EDA
3 Summary
Widths/Blk Type/Clks
Regs/Clken/Byte Enable/Adrs
Read During Write Option
Mem Init
ram32x4
data[7..0]
wren
address[7..0]
clock
q[7..0]
Block type: AUTO
Currently selected device family:
Match project/default
How wide should the 'q' output bus be?
8
bits
How many 8-bit words of memory?
256
words
Note: You could enter arbitrary values for width and depth
What should the memory block type be?
Auto
MLAB
M10K
M-RAM
LCs
Options...
Set the maximum block depth to
Auto
words
What clocking method would you like to use?
Single clock
Dual clock: use separate 'input' and 'output' clocks
Resource Usage
1 M10K
Cancel
< Back
Next >
Finish

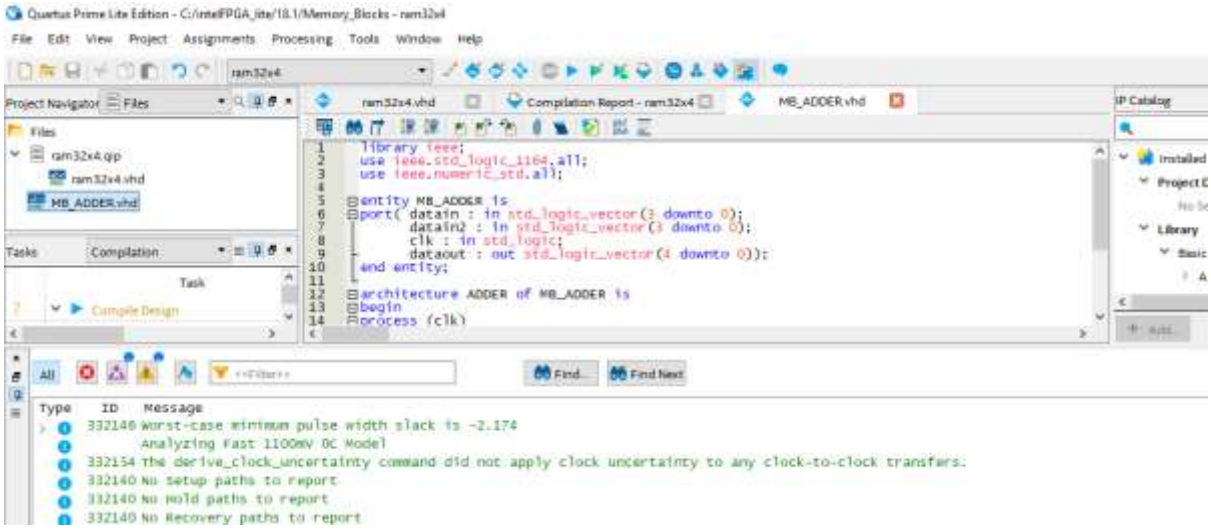

MegaWizard Plug-In Manager [page 6 of 6]
RAM: 1-PORT
About
Documentation
1 Parameter Settings
2 EDA
3 Summary
ram32x4
data[7..0]
wren
address[7..0]
clock
q[7..0]
Block type: AUTO
Turn on the files you wish to generate. A gray checkmark indicates a file that is automatically generated, and a green checkmark indicates an optional file. Click Finish to generate the selected files. The state of each checkbox is maintained in subsequent MegaWizard Plug-In Manager sessions.
The MegaWizard Plug-In Manager creates the selected files in the following directory:
C:\intelFPGA_lite\18.1\
File
Description
ram32x4.vhd
Variation file
ram32x4.inc
AHDL Include file
ram32x4.cmp
VHDL component declaration file
ram32x4.bsf
Quartus Prime symbol file
ram32x4_inst.vhd
Instantiation template file
Resource Usage
1 M10K
Cancel
< Back
Next >
Finish

HASIL Compile ram32x4:

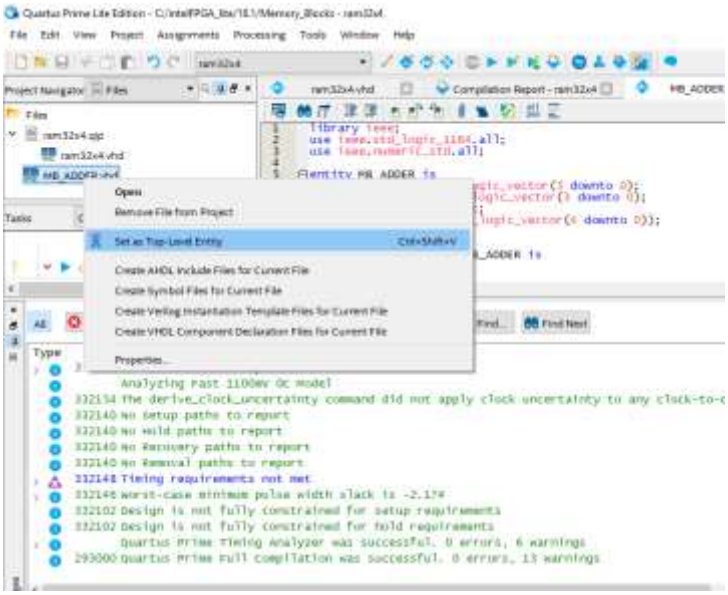


Lalu menambahkan file vhdl untuk MemoryBlock_Adder:

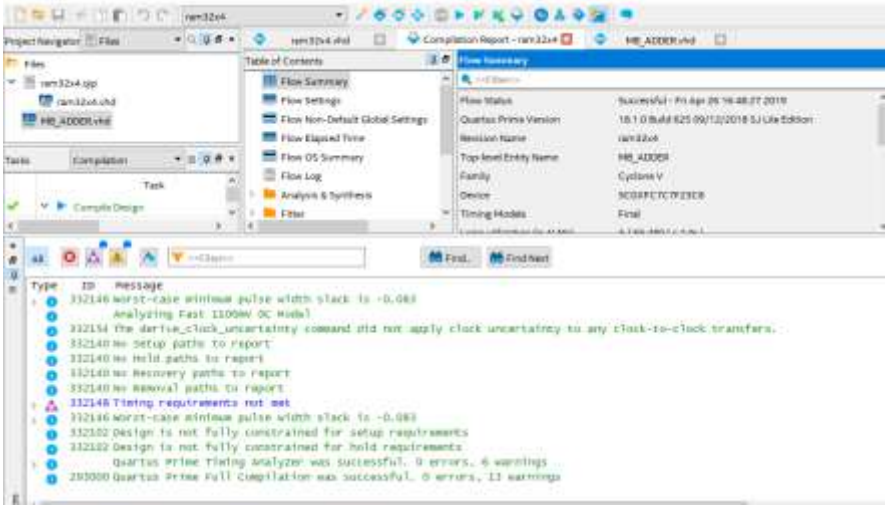




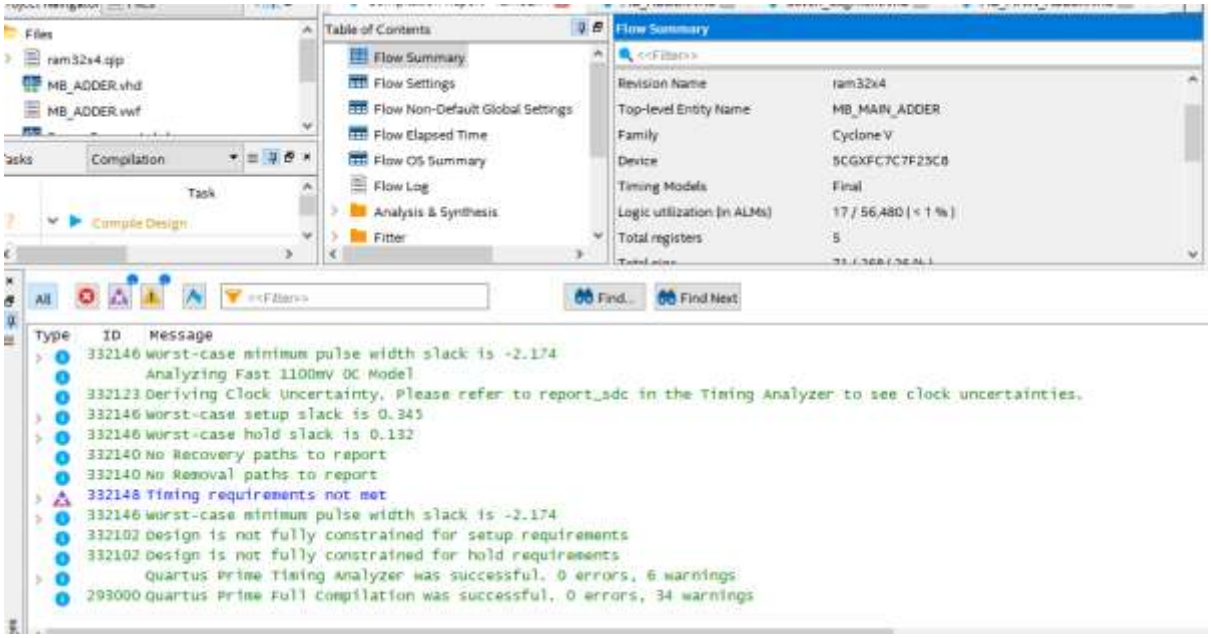
Lalu Compile File tersebut sebagai Top-Level Entity



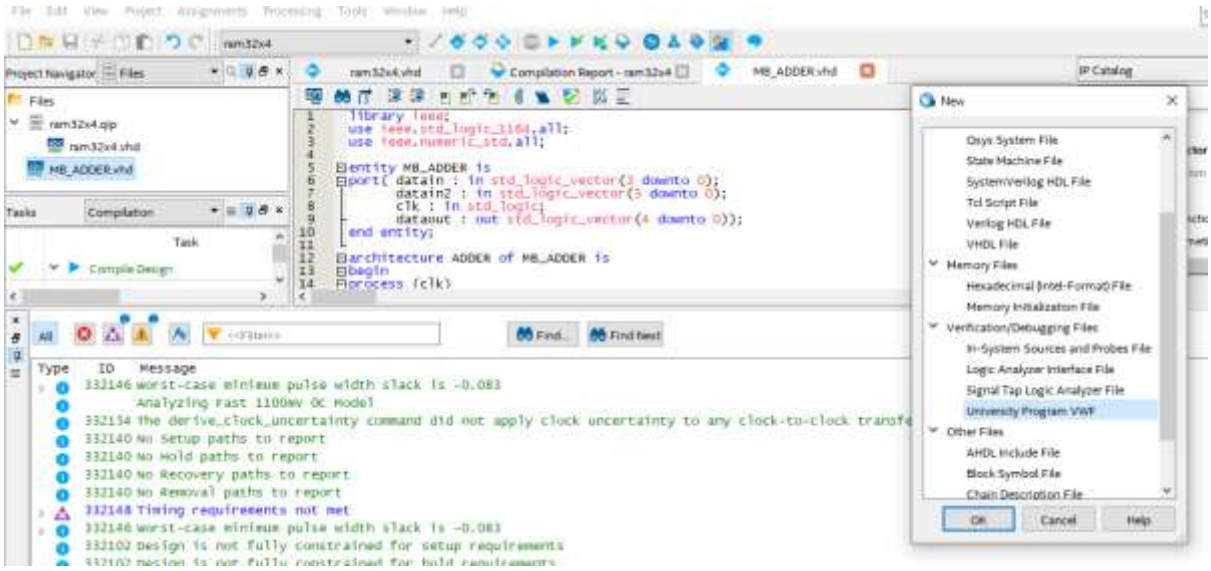
HASIL compile MB_Adder sebagai top-level entity:

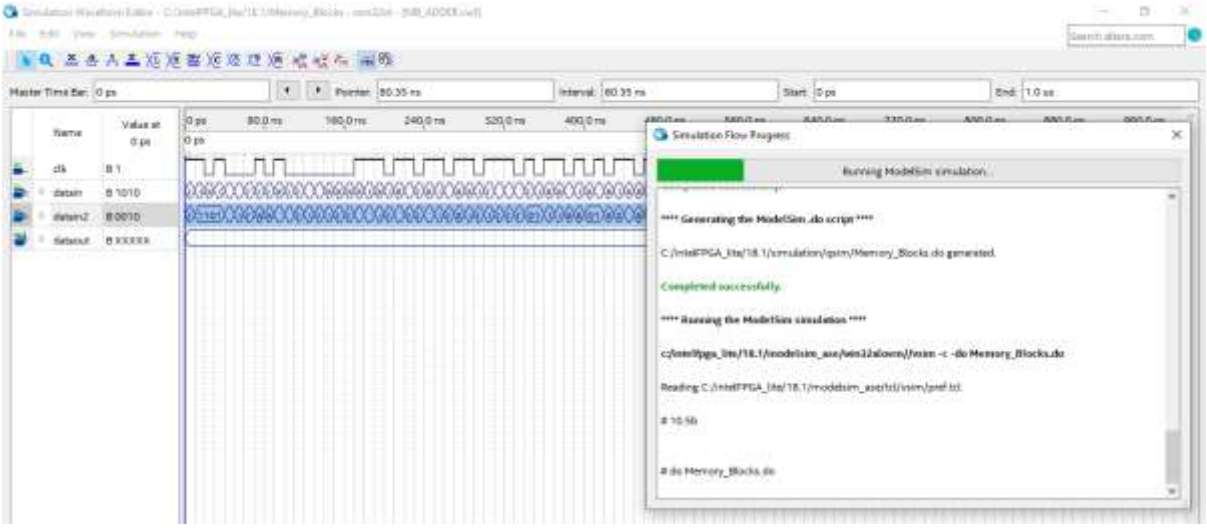


Dan MB_MAIN_ADDER:

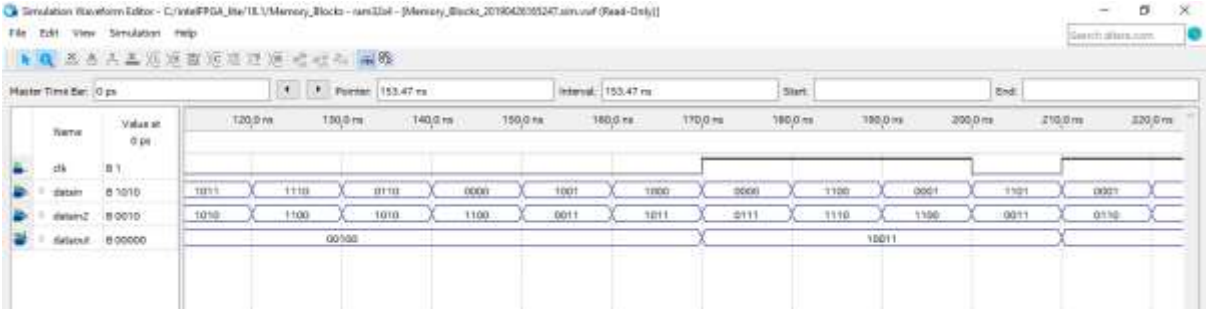


Membuat Wave Untuk Memory Block Adder:

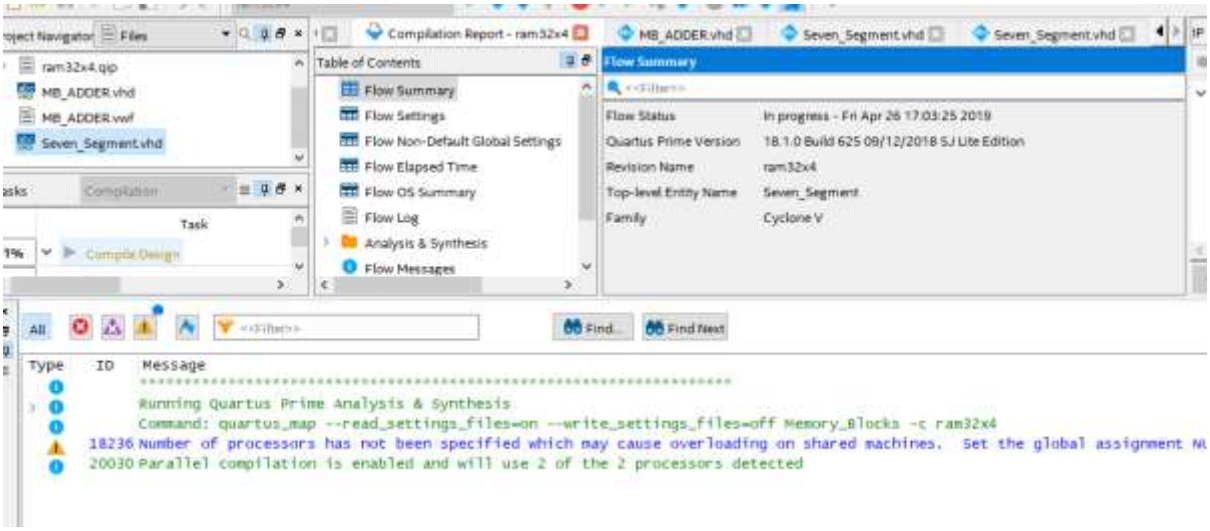




Input Pada wave menggunakan Randomize, Hasil simulasinya:

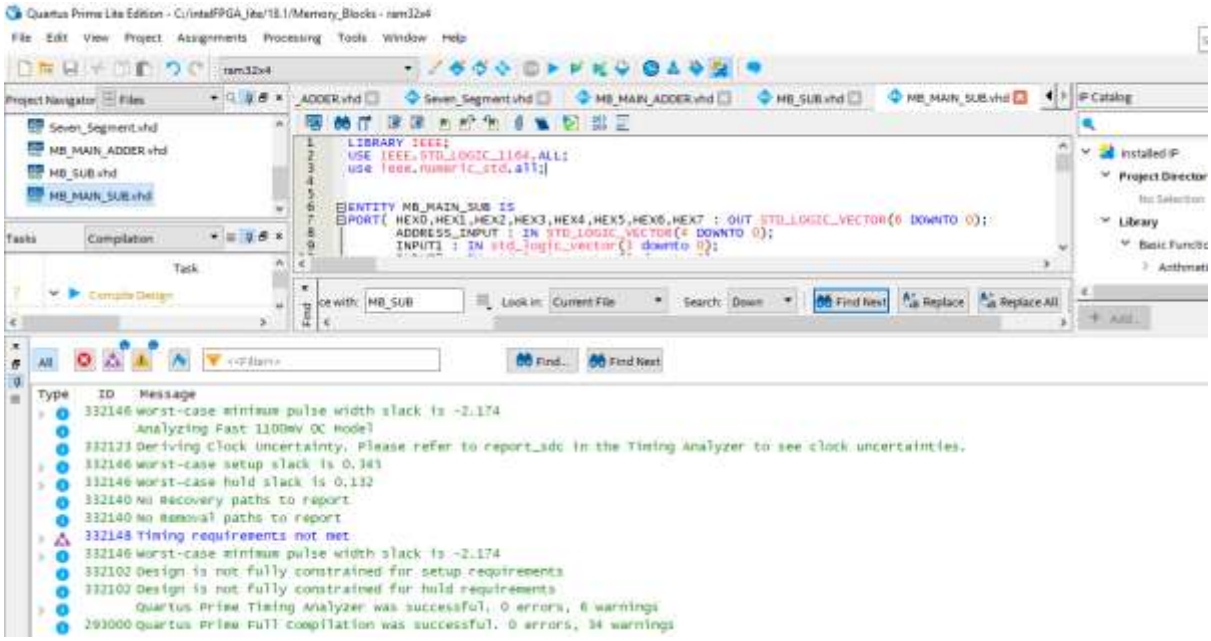


Menambahkan Seven Segment VHD lalu compile

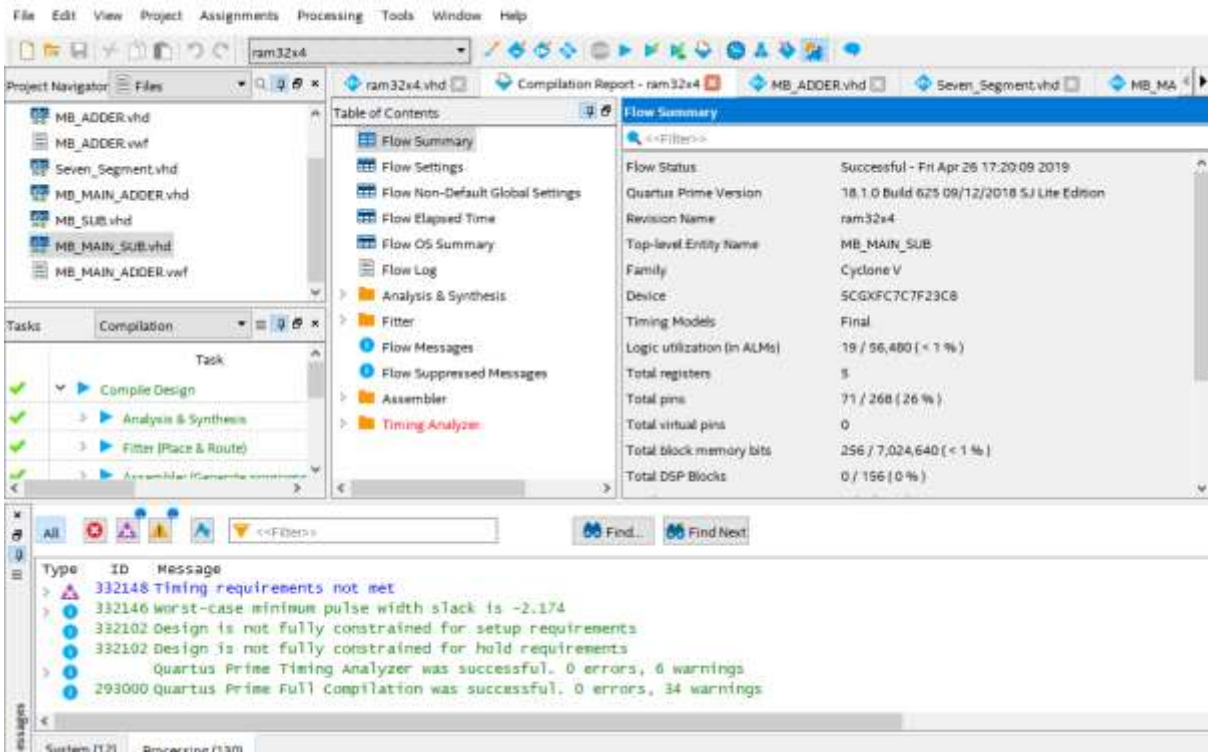


Memory block yang berisi kalkulator Kurang

Menambahkan MB_SUB dan MB_MAIN_SUB:



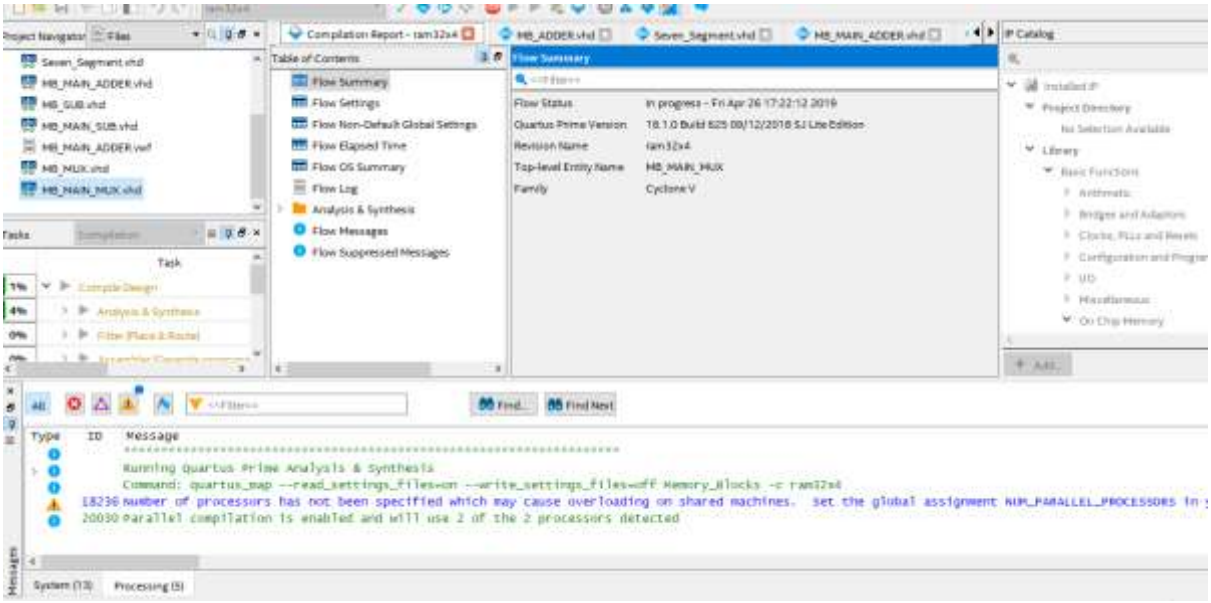
HASIL COMPILE:

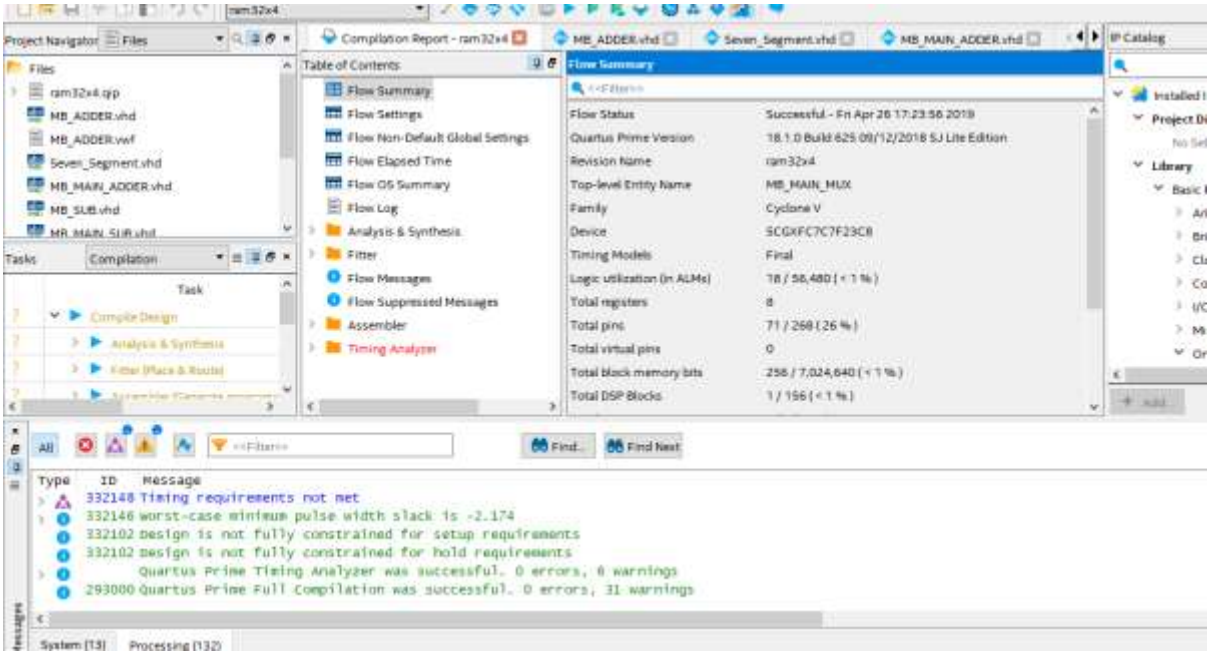


HASIL SUMULASI SUBSTRACTOR

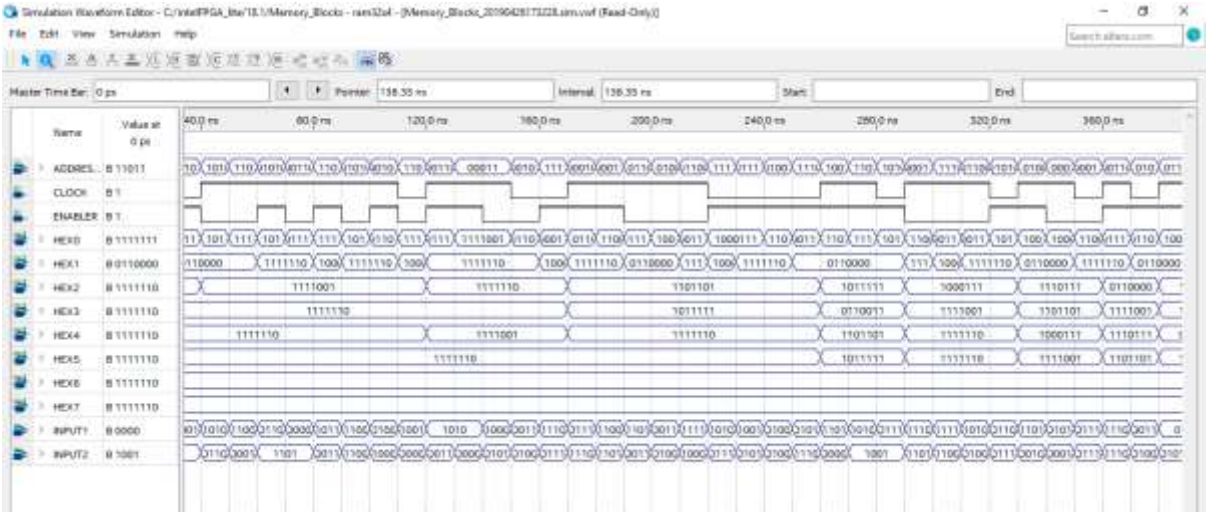
Memory block yang berisi kalkulator Kali

HASIL COMPILE:



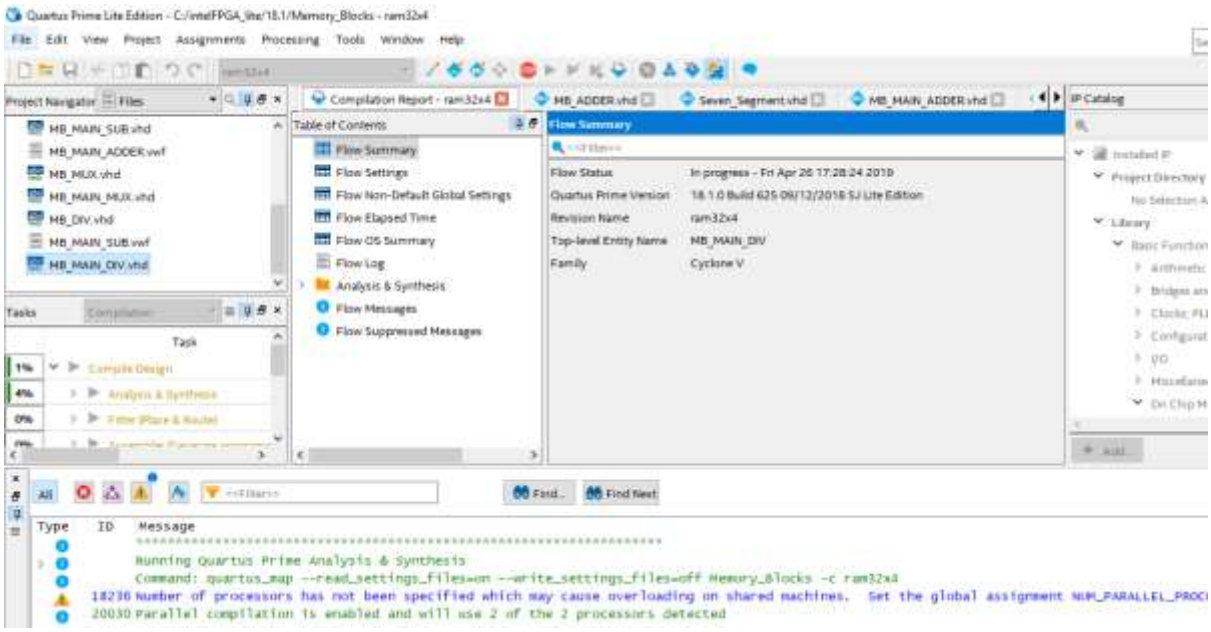

Flow Summary
Flow Status Successful - Fri Apr 26 17:23:56 2019
Quartus Prime Version 18.1.0 Build 625 09/12/2018 SJ Lite Edition
Revision Name ram32x4
Top-level Entity Name MB_MAIN_MUX
Family Cyclone V
Device 5CGXFC7C7F23C8
Timing Models Final
Logic utilization (in ALMs) 18 / 56,480 (< 1 %)
Total registers 8
Total pins 71 / 268 (26 %)
Total virtual pins 0
Total block memory bits 256 / 7,024,640 (< 1 %)
Total DSP Blocks 1 / 156 (< 1 %)
Type ID Message
332148 Timing requirements not met
332146 Worst-case minimum pulse width slack is -2.174
332102 Design is not fully constrained for setup requirements
332102 Design is not fully constrained for hold requirements
Quartus Prime Timing Analyzer was successful. 0 errors, 6 warnings
293000 Quartus Prime Full Compilation was successful. 0 errors, 31 warnings

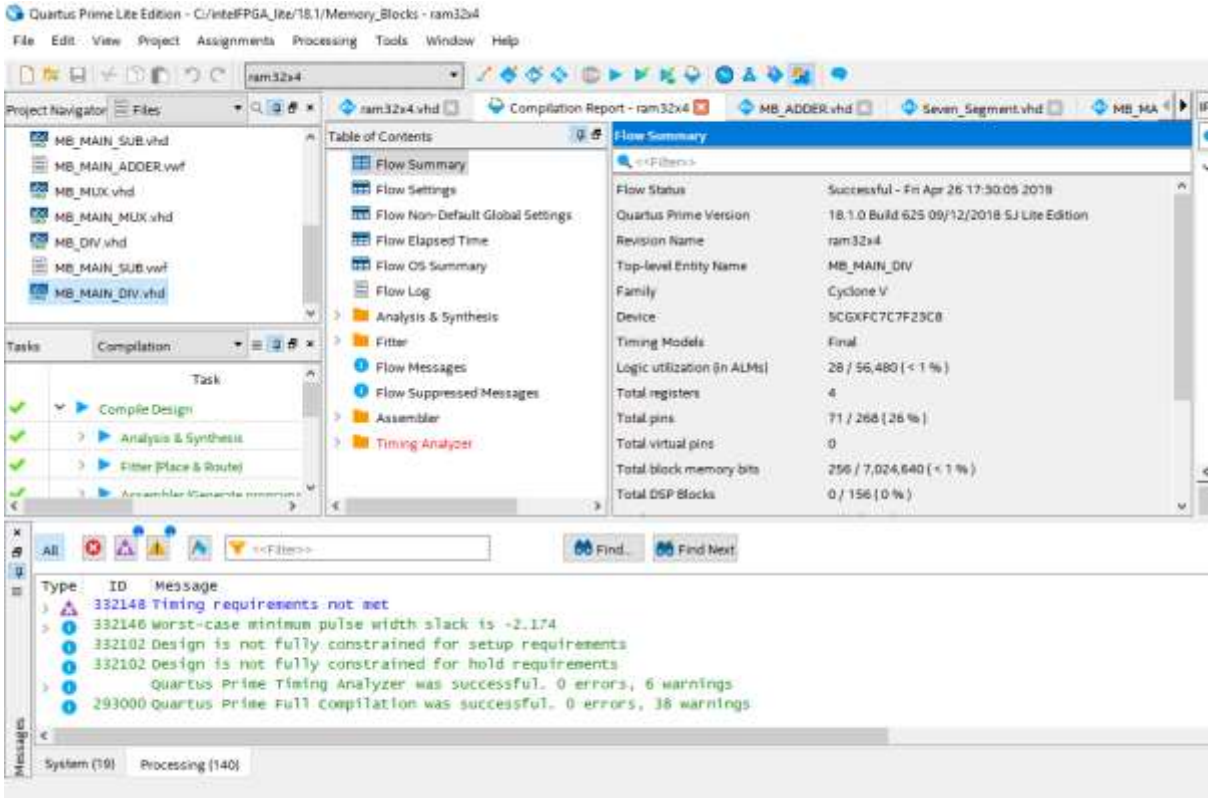
SIMULASI



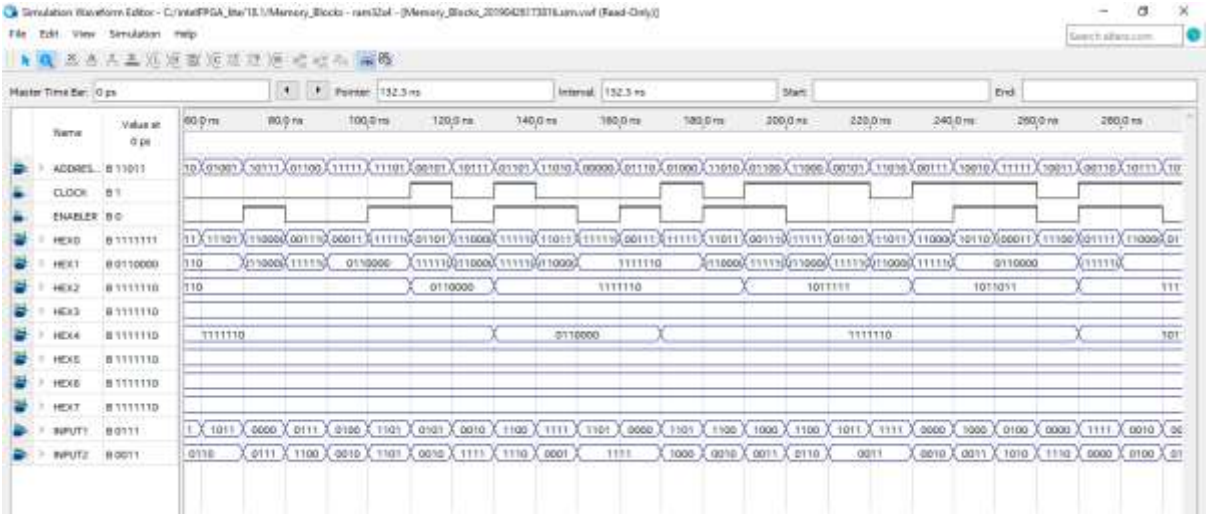
Memory block yang berisi kalkulator Bagi

COMPILE:



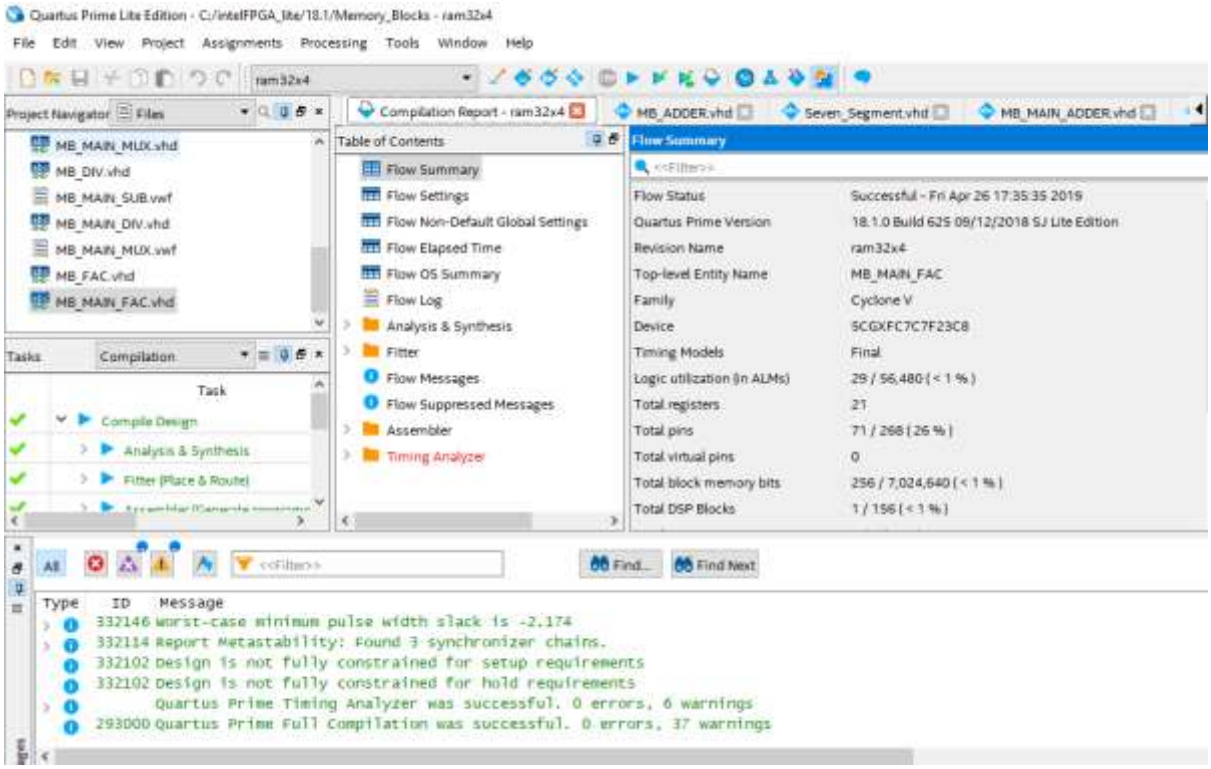


SIMULASI:


Simulation Waveform Editor
File Edit View Simulation Help
Master Time Bar:
Pointer:
Interval:
Start:
End:
Name
Value at 0 ps
ADDRESS
CLOCK
ENABLER
HEX0
HEX1
HEX2
HEX3
HEX4
HEX5
HEX6
HEX7
INPUT1
INPUT2

Memory block yang berisi kalkulator faktorial

Compile Factorial:



SIMULATION FACTIROAL: