MYD-CZU3EG/4EV/5EV PIN MAP

Version.	V/1 1	2021	03 04

MYIR			MYD-CZU3	BEG	/4EV/5EV PIN MA	AΡ			Version: V1.1 2021.03.04
nction ound	SoC Pin Name	Bank Ball			Net Name VCC_IN_COM	Ball	Bank	SoC Pin Name	Function SOM POWER
)	MGTHTXP3_224 MGTHTXN3_224	Bank 224 N4 Bank 224 N3	MGTHTXP3_224 MGTHTXN3_224	3 4 5 6	VCC_IN_COM VCC_IN_COM			DC 3.3V DC 3.3V DC 3.3V	SOM POWER SOM POWER
ind	MGTHRXP3 224	Bank 224 P2	MGTHRXP3 224	7 8 9 10	GND MGTHTXP2 224	R4	Bank 224	Ground MGTHTXP2 224	
nd	MGTHRXN3_224 MGTHTXP1_224	Bank 224 P1 Bank 224 U4	GND 1	13 14	MGTHTXN2_224 GND MGTHRXP2_224		Bank 224 Bank 224	MGTHTXN2_224 Ground MGTHRXP2 224	
d	MGTHTXN1_224	Bank 224 U3	MGTHTXN1_224 1 GND 1	17 18	MGTHRXN2_224		Bank 224	MGTHRXN2_224 Ground	
	MGTHRXP1_224 MGTHRXN1 224	Bank 224 V2 Bank 224 V1	MGTHRXP1_224 2 MGTHRXN1 224 2	21 22 23 24	MGTHTXP0_224 MGTHTXN0 224		Bank 224 Bank 224	MGTHTXP0_224 MGTHTXN0_224	
nd	MGTREFCLKØP 224	Bank 224 Y6	GND 2 MGTREFCLK0P 224 2	25 26	GND MGTHRXPØ 224 MGTHRXNØ 224		Bank 224	Ground MGTHRXP0 224	
nd	MGTREFCLKØN 224	Bank 224 Y5	GND 3	31 32	GND		Bank 224	MGTHRXN0 224 Ground	
TOU_N12_VRP_65 _RB_TX_Disable	IO_T0U_N12_VRP_65 IO_T2U_N12_65	Bank 65 W9 Bank 65 P9	IO_T2U_N12_65 3	35 36	IO L4P_T0U_N6_DBC_AD7P_SMBALERT_6: IO_L4N_T0U_N7_DBC_AD7N_65 IO_L15P_T2L_N4_AD11P_65	T8	Bank 65 Bank 65	IO_L4P_T0U_N6_DBC_AD7P_SMBALERT_65 IO_L4N_T0U_N7_DBC_AD7N_65 IO_L15P_T2L_N4_AD11P_65	
RT_TX_Disable	IO T3U N12 65 IO_T1U_N12_65 VCCO 65	Bank 65 K5 Bank 65 H2 Bank 65	IO_T1U_N12_65 3	39 40	IO_L15N_T2L_N5_AD11N_65	N7 N6	Bank 65 Bank 65	IO L15P T2L N4 AD11P 65 IO_L15N_T2L_N5_AD11N_65 Ground	
K 65 POWER DC 1.8V	IO_L13P_T2L_N0_GC_QBC_65 IO_L13N_T2L_N1_GC_QBC_65	Bank 65 L7 Bank 65 L6	IO L13P T2L NØ GC QBC 65 4	41 42 43 44 45 46	IO_L6P_T0U_N10_AD6P_65 IO_L6N_T0U_N11_AD6N_65		Bank 65 Bank 65	IO_L6P_T0U_N10_AD6P_65 IO L6N T0U N11 AD6N 65	
	IO L7P T1L N0 QBC AD13P 65 IO_L7N_T1L_N1_QBC_AD13N_65	Bank 65 L1	IO L7P T1L N0 QBC AD13P 6 4	47 48	IO L16P T2U N6 QBC AD3P 65 IO_L16N_T2U_N7_QBC_AD3N_65	P7	Bank 65 Bank 65	IO L16P T2U N6 QBC AD3P 65 IO L16N T2U N7 QBC AD3N 65	
und	TO 114P T21 N2 GC 65	Bank 65 M6	GND 5	51 52	GND IO L2P TØL N2 65		Bank 65	Ground IO L2P TOL N2 65	
	IO_L14N_T2L_N3_GC_65 IO L1P T0L N0 DBC 65	Bank 65 L5 Bank 65 W8	IO_L14N_T2L_N3_GC_65 5 IO L1P T0L N0 DBC 65 5	53 54 55 56 57 58	IO_L2N_T0L_N3_65 IO L12P T1U N10 GC 64	V9	Bank 65 Bank 64	IO_L2N_T0L_N3_65 IO L12P T1U N10 GC 64	
und	IO_L1N_T0L_N1_DBC_65	Bank 65 Y8	IO_L1N_T0L_N1_DBC_65		IO_L12N_T1U_N11_GC_64 GND	AF5	Bank 64	IO_L12N_T1U_N11_GC_64 Ground	SFP_LT_TX_
	IO_L24P_T3U_N10_64 IO_L24N_T3U_N11_64	Bank 64 AF1 Bank 64 AG1	IO_L24P_T3U_N10_64 6 IO_L24N_T3U_N11_64 6	63 64	IO_L21P_T3L_N4_AD8P_65 IO_L21N_T3L_N5_AD8N_65	H7	Bank 65 Bank 65	IO_L21P_T3L_N4_AD8P_65 IO_L21N_T3L_N5_AD8N_65	SDA
	IO L18P T2U N10 AD2P 65 IO_L18N_T2U_N11_AD2N_65	Bank 65 M8 Bank 65 L8	IO_L18N_T2U_N11_AD2N_65 6	67 68 69 70	IO L22P T3U N6 DBC AD0P 64 IO_L22N_T3U_N7_DBC_AD0N_64	AE2 AF2	Bank 64 Bank 64	IO L22P T3U N6 DBC AD0P 64 IO_L22N_T3U_N7_DBC_AD0N_64	
POWER DC 1.2V-1.5V	VCC_PSBATT IO_L23P_T3U_N8_64 IO_L23N_T3U_N9_64	Bank 64 AH2 Bank 64 AH1		71 72 73 74	GND IO_L10P_T1U_N6_QBC_AD4P_64 IO_L10N_T1U_N7_QBC_AD4N_64		Bank 64 Bank 64	Ground IO_L10P_T1U_N6_QBC_AD4P_64 IO_L10N_T1U_N7_QBC_AD4N_64	HDMI HDMI
02	IO L22P T3U N6 DBC AD0P 65	Bank 65 K8	IO L22P T3U N6 DBC AD0P 6 7	75 76 77 78	IO L14P T2L N2 GC 64	AC4	Bank 64 Bank 64	IO L14P T2L N2 GC 64	HDMI
und 0 IN	IO_L22N_T3U_N7_DBC_AD0N_65 IO L20P T3L N2 AD1P 64	Bank 65 K7	GND 8	81 82 83 84	IO_L14N_T2L_N3_GC_64 GND IO L16P T2U N6 OBC AD3P 64		Bank 64	IO_L14N_T2L_N3_GC_64 Ground IO L16P T2U N6 QBC AD3P 64	
0_1N	IO_L20N_T3L_N3_AD1N_64 IO_L12N_T1U_N10_GC_65	Bank 64 AH3 Bank 65 L3	10 L20P 13L N2 AD1P 64 8 10 L20N T3L N3 AD1N 64 8 10 L12P T1U N10 GC 65 8	85 86 87 88	IO L16P 12U N6 QBC AD3P 64 IO L16N T2U N7 QBC AD3N 64 IO L6P T0U N10 AD6P 64	AD1	Bank 64	IO_L16P_12U_N6_QBC_AD3P_64 IO_L16N_T2U_N7_QBC_AD3N_64 IO_L6P_T0U_N10_AD6P_64	HDMI
und	IO_L12N_T1U_N11_GC_65	Bank 65 L3	IO_L12N_T1U_N11_GC_65 8	89 90 91 92	IO_L6N_T9U_N11_AD6N_64 VCCO_64		Bank 64	IO_L6N_T0U_N11_AD6N_64 VCCO_64	HDMI BANK 64 POWER
	IO_L3P_T0L_N4_AD15P_65 IO_L3N_T0L_N5_AD15N_65	Bank 65 U8 Bank 65 V8	IO_L3P_T0L_N4_AD15P_65 9 IO_L3N_T0L_N5_AD15N_65 9	93 94 95 96	IO_T0U_N12_VRP_64 IO_T1U_N12_64	AH6	Bank 64 Bank 64	IO_T0U_N12_VRP_64 IO_T1U_N12_64	IMGH IMGH
	IO L9P T1L N4 AD12P 65 IO_L9N_T1L_N5_AD12N_65	Bank 65 K2 Bank 65 J2	IO L9P T1L N4 AD12P 65 9 IO L9N T1L N5 AD12N 65 9	97 98 99 100	IO T2U N12 64 IO_T3U_N12_64	AB5	Bank 64 Bank 64	IO T2U N12 64 IO_T3U_N12_64	HDMI
und D2	TO 113P T21 NO GC OBC 64	Bank 64 AD5	GND 16	01 102 03 104	GND IO L15P T2L N4 AD11P 64	AB4	Bank 64	Ground IO L15P T2L N4 AD11P 64	
02	IO_L13N_T2L_N1_GC_QBC_64 IO L11P T1U N8 GC 65	Bank 64 AD4 Bank 65 K4	IO_L13N_T2L_N1_GC_QBC_64 10 IO L11P T1U N8 GC 65 10	95 106 97 108	IO_L15N_T2L_N5_AD11N_64 IO L5P T0U N8 AD14P 65	R7	Bank 64 Bank 65	IO_L15N_T2L_N5_AD11N_64 IO L5P T0U N8 AD14P 65	HDMI
und	IO_L11N_T1U_N9_GC_65	Bank 65 K3	IO_L11N_T1U_N9_GC_65 10 GND 11	11 112	IO_L5N_T0U_N9_AD14N_65 GND	T7	Bank 65	IO_L5N_T0U_N9_AD14N_65 Ground	
3_IN ID2 ID2	IO_L19P_T3L_N0_DBC_AD9P_64 IO_L19N_T3L_N1_DBC_AD9N_64	Bank 64 AG4 Bank 64 AH4	IO_L19P_T3L_N0_DBC_AD9P_6 11 IO_L19N_T3L_N1_DBC_AD9N_6 11	13 114	IO L10P_T1U_N6_QBC_AD4P_65 IO_L10N_T1U_N7_QBC_AD4N_65 TO_L11P_T1U_N8_GC_64	H3	Bank 65 Bank 65	IO_L10P_T1U_N6_QBC_AD4P_65 IO_L10N_T1U_N7_QBC_AD4N_65	
D2 D2 und	IO L21P T3L N4 AD8P 64 IO_L21N_T3L_N5_AD8N_64	Bank 64 AE3 Bank 64 AF3	IO_L21N_T3L_N5_AD8N_64 11	19 120	IO_L11N_T1U_N9_GC_64	AF7 AF6	Bank 64 Bank 64	IO L11P T1U N8 GC 64 IO_L11N_T1U_N9_GC_64 Ground	
und D1 D1	IO_L19P_T3L_N0_DBC_AD9P_65	Bank 65 35 Bank 65 34	GND 12 IO_L19P_T3L_N0_DBC_AD9P_6 12 IO_L19N_T3L_N1_DBC_AD9N_6 12	23 124	IO_LSP_T0U_N8_AD14P_64 IO_LSN_T0U_N9_AD14N_64		Bank 64 Bank 64	IO_L5P_T0U_N8_AD14P_64 IO_L5N_T0U_N9_AD14N_64	
D1 D1	IO L19N T3L N1 DBC AD9N 65 IO_L17P_T2U_N8_AD10P_65 IO_L17N_T2U_N9_AD10N_65	Bank 65 N9 Bank 65 N8	IO_L17P_T2U_N8_AD10P_65 12	27 128 29 138	IO L3P_TOL_N4_AD15P_64 IO_L3N_TOL_N5_AD15N_64	AB8	Bank 64 Bank 64	IO LSN 160 NS ADIAN 64 IO_L3P_T6L_N4_AD15P_64 IO_L3N_T6L_N5_AD15N_64	HDMI
und 01	IO L23P T3U N8 I2C SCLK 65	Bank 65 K9	GND 13 IO_L23P_T3U_N8_I2C_SCLK_6 13	31 132	GND IO L4P T9U N6 DBC AD7P 64		Bank 64	Ground IO L4P TØU N6 DBC AD7P 64	
01	IO L23N T3U N9 65 IO_L8P_T1L_N2_AD5P_65	Bank 65 39 Bank 65 31	IO L23N T3U N9 65 13 IO_L8P_T1L_N2_AD5P_65 13		IO L4N TOU N7 DBC AD7N 64 IO_L7P_T1L_NO_QBC_AD13P_64	AE7	Bank 64 Bank 64	IO L4N TOU N7 DBC AD7N 64 IO_L7P_T1L_N0_QBC_AD13P_64	HDMI
und	IO_L8N_T1L_N3_AD5N_65	Bank 65 H1	IO_L8N_T1L_N3_AD5N_65 13	39 148 41 142	IO_L7N_T1L_N1_QBC_AD13N_64	AH9		IO_L7N_T1L_N1_QBC_AD13N_64 Ground	HDMI
D1 D1	IO_L20P_T3L_N2_AD1P_65 IO L20N T3L N3 AD1N 65	Bank 65 J6 Bank 65 H6	IO_L20P_T3L_N2_AD1P_65 14	43 144	IO_L24P_T3U_N10_PERSTN1_I2C_SDA_6: IO L24N T3U N11 PERSTN0 65		Bank 65 Bank 65	IO_L24P_T3U_N10_PERSTN1_I2C_SDA_65 IO L24N T3U N11 PERSTN0 65	
4_IN D2	IO_L18P_T2U_N10_AD2P_64 IO_L18N_T2U_N11_AD2N_64	Bank 64 AB1 Bank 64 AC1	IO_L18P_T2U_N10_AD2P_64 14	47 148 49 150	IO_L8P_T1L_N2_AD5P_64 IO_L8N_T1L_N3_AD5N_64	AF8	Bank 64	IO_L8P_T1L_N2_AD5P_64 IO_L8N_T1L_N3_AD5N_64	HDMI
und 5_IN	IO_L17P_T2U_N8_AD10P_64	Bank 64 AB2	GND 15 IO_L17P_T2U_N8_AD10P_64 15	51 152 53 154	GND IO_L2P_T0L_N2_64		Bank 64	Ground IO_L2P_T0L_N2_64	
D TP INTn D_TP_RESET	IO L17N T2U N9 AD10N 64 IO_L9P_T1L_N4_AD12P_64	Bank 64 AC2 Bank 64 AH8	IO L9P T1L N4 AD12P 64 15	55 156 57 158	IO L2N TOL N3 64 IO_L1P_TOL_NO_DBC_64	AC9	Bank 64 Bank 64	IO L2N TOL N3 64 IO_L1P_TOL_NO_DBC_64	HD
II_RESET/LCD_PWR_EN	IO_L9N_T1L_N5_AD12N_64	Bank 64 AH7	IO_L9N_T1L_N5_AD12N_64 15	59 160	IO_L1N_T0L_N1_DBC_64	AD9	Bank 64	IO_L1N_TOL_N1_DBC_64	LC
nction	SoC Pin Name	Bank Ball		33	Net Name	Ball	Bank	SoC Pin Name	F
_TX	IO TOU N12 VRP 66 IO_T2U_N12_66	Bank 66 G4 Bank 66 E7	IO_T2U_N12_66	3 4	VCC_IN_COM			DC 3.3V DC 3.3V	SOM POWER SOM POWER
_RX	IO_T1U_N12_66 IO_T3U_N12_66	Bank 66 D2 Bank 66 C7	IO_T1U_N12_66 IO_T3U_N12_66		USER_CLKIN_P USER_CLKIN_N			Ground USER_CLKIN_P	
und	IO L8P T1L N2 AD5P 66	Bank 66 A2 Bank 66 A1	GND IO L8P T1L N2 AD5P 66 1 IO_L8N_T1L_N3_AD5N_66 1	11 12				USER CLKIN N Ground	S15338 refence S15338
	IO L8N_T1L_N3_AD5N_66 IO L9P_T1L_N4_AD12P_66 IO L9N_T1L_N5_AD12N_66	Bank 66 B3 Bank 66 A3	10 L9P_T1L_N5_AD3N_66 1 10 L9P_T1L_N5_AD12N_66 1	15 16 17 18	USER_CLKOUT_N			USER_CLKOUT_N Ground	S15338
und	IO L5P T0U N8 AD14P 66	Bank 66 E4	IO_L5P_T0U_N8_AD14P_66 2	19 20	IO L13P T2L NØ GC QBC 66 IO_L13N_T2L_N1_GC_QBC_66	D7	Bank 66 Bank 66	IO L13P T2L NØ GC QBC 66 IO_L13N_T2L_N1_GC_QBC_66	
	IO_L5N_TOU_N9_AD14N_66 IO_L4P_TOU_N6_DBC_AD7P_66	Bank 66 E3 Bank 66 G3	IO L5N T0U N9 AD14N 66 2	23 24	IO_L10P_T1U_N6_QBC_AD4P_66 IO_L10N_T1U_N7_QBC_AD4N_66	B4	Bank 66	IO L10P T1U N6 QBC AD4P 66 IO L10N T1U N7 QBC AD4N 66	
und	IO_L4N_T0U_N7_DBC_AD7N_66	Bank 66 F3	TO LAN TRU NY DRC ADYN 66	27 28 29 30	GND IO L2P TØL N2 66	E1	Bank 66	Ground IO L2P T0L N2 66	
	IO_L14P_T2L_N2_GC_66 IO_L14N_T2L_N3_GC_66	Bank 66 E5 Bank 66 D5	IO_L14P_T2L_N2_GC_66 IO_L14N_T2L_N3_GC_66	29 30 31 32 33 34	IO L2N T0L N3 66 IO L3P T0L N4 AD15P 66	D1	Bank 66	IO_L2N_T0L_N3_66 IO_L3P_T0L_N4_AD15P_66	
	IO_L12P_T1U_N10_GC_66 IO_L12N_T1U_N11_GC_66	Bank 66 C3 Bank 66 C2	IO_L12P_T1U_N10_GC_66 IO_L12N_T1U_N11_GC_66	35 36 37 38	IO_L3N_T0L_N5_AD15N_66 GND		Bank 66	IO_L3N_T0L_N5_AD15N_66 Ground	
und	IO_L6P_T0U_N10_AD6P_66	Bank 66 G5	IO_L6P_T0U_N10_AD6P_66 4	39 40 41 42	IO L19P T3L NØ DBC AD9P 66 IO_L19N_T3L_N1_DBC_AD9N_66	A5	Bank 66 Bank 66	IO L19P T3L NØ DBC AD9P 66 IO_L19N_T3L_N1_DBC_AD9N_66	
	IO_L6N_T0U_N11_AD6N_66 IO_L7P_T1L_N0_QBC_AD13P_66	Bank 66 F5 Bank 66 C1	IO L7P T1L N0 QBC AD13P 6 4	43 44 45 46	IO_L1P_T0L_N0_DBC_66 IO L1N T0L N1 DBC 66		Bank 66 Bank 66	IO_L1P_T0L_N0_DBC_66 IO_L1N_T0L_N1_DBC_66	
und	IO_L7N_T1L_N1_QBC_AD13N_66	Bank 66 B1	GND 4	47 48 49 <mark>50</mark>	IO L20P T3L N2 AD1P 66		Bank 66	Ground IO L20P T3L N2 AD1P 66	
	IO_L23P_T3U_N8_66 IO_L23N_T3U_N9_66	Bank 66 A9 Bank 66 A8	IO_L23P_T3U_N8_66 IO_L23N_T3U_N9_66	51 52 53 54	IO_L20N_T3L_N3_AD1N_66 IO_L11P_T1U_N8_GC_66	D4	Bank 66 Bank 66	IO_L20N_T3L_N3_AD1N_66 IO_L11P_T1U_N8_GC_66	
	IO_L15P_T2L_N4_AD11P_66 IO_L15N_T2L_N5_AD11N_66	Bank 66 G6 Bank 66 F6	IO_L15P_T2L_N4_AD11P_66 IO_L15N_T2L_N5_AD11N_66	55 56 57 58		-	Bank 66	IO_L11N_T1U_N9_GC_66 Ground	
und	IO L24P_T3U_N10_66 IO L24N_T3U_N11_66	Bank 66 C9 Bank 66 B9	IO_L24P_T3U_N10_66 6	59 60 61 62	IO L21P T3L N4 AD8P 66 IO L21N T3L N5 AD8N 66 IO L22P T3U N6 DBC AD0P 66	A6	Bank 66 Bank 66 Bank 66	IO L21P T3L N4 AD8P 66 IO L21N T3L N5 AD8N 66	
	IO_L24N_T3U_N11_66 IO_L18P_T2U_N10_AD2P_66 IO_L18N_T2U_N11_AD2N_66	Bank 66 B9 Bank 66 E9 Bank 66 D9	IO_L24N_T3U_N11_66 6 10_L18P_T2U_N10_AD2P_66 10_L18N_T2U_N11_AD2N_66 6	63 64 65 66 67 68	IO_L22N_T3U_N7_DBC_AD0N_66		Bank 66 Bank 66	IO L22P_T3U_N6_DBC_AD0P_66 IO_L22N_T3U_N7_DBC_AD0N_66 Ground	
und Data plus	USB_PHY_DP	00 09		59 <mark>70</mark>	IO L17P T2U N8 AD10P 66 IO_L17N_T2U_N9_AD10N_66	F8 E8	Bank 66 Bank 66	IO L17P T2U N8 AD10P 66 IO L17N T2U N9 AD10N 66	
Data minus IO POWER DC 1.8V	USB_PHY_DM		USB_PHY_DM 7 VCC_PSMIO_COM 7	73 74 75 76	IO_L16P_T2U_N6_QBC_AD3P_66 IO_L16N_T2U_N7_QBC_AD3N_66	G8	Bank 66 Bank 66	IO L16P T2U N6 QBC AD3P 66 IO L16N T2U N7 QBC AD3N 66	
OTG ID VBUS	USB_PHY_ID USB_PHY_VBUS		USB_PHY_ID 7 USB_PHY_VBUS 7	77 <mark>78</mark> 79 80	VCCO_66 ETH MD1 P	Ė		VCCO_66 ETH MD1 P	BANK 66 POWER Ethernet Data 1 F
Active high VBUS control output	VBUS_SW_EN PS_MI027	Bank 501 J15	VBUS_SW_EN 8 PS_MIO27 8	81 82 83 84	ETH_MD1_N GND			ETH_MD1_N Ground	Ethernet Data 1 M
HP_DET	PS_MI028 PS_MI036	Bank 501 K15 Bank 501 K17	PS_MI028 8 PS_MI036 8	85 86 87 88	ETH_MD2_P ETH_MD2_N			ETH_MD2_P ETH_MD2_N	Ethernet Data 2 N
E_PERST	PS_MI032 PS_MI031	Bank 501 316 Bank 501 H16	PS MI032 8 PS_MI031 9	99 90 91 92	GND ETH_MD3_P			Ground ETH_MD3_P	Ethernet Data 3 F
	PS_MI033 PS_MI037	Bank 501 L16 Bank 501 J17	PS_MI037 9	95 96				ETH_MD3_N Ground	
DE LUANT TYP	PS MIO30 PS MIO29	Bank 501 F16 Bank 501 G16	PS MI029 9	99 100	ETH MD4 P ETH MD4 N			ETH MD4 P	
UART_TXD UART_RXD	DEBUG_TXD DEBUG_RXD SD1_D3	Bank 501 H17 Bank 501 L17 Bank 501 M18	DEBUG_RXD 16		GND ETH_LED_LINK ETH LED ACT			Ground ETH_LED_LINK ETH_LED_ACT	
	SD1 CD	Bank 501 M18 Bank 501 K20 Bank 501 J20	SD1 CD 16	97 108	ETH_LED_ACT PS_LPD_EN PS_FPD_EN		Bank 501 Bank 501	PS LPD EN PS FPD EN	PS low-power domain
Card Detection		Bank 501 J20	SD1_D1 11	11 112	PS_FPD_EN PL_PD_EN PS_VCCO_EN		Bank 501 Bank 501	PS_FPD_EN PL_PD_EN PS_VCCO_EN	PL power domain
Card Detection Write Protected Data 1	SD1_WP SD1_D1 SD1_CMD			15 116	PS_VCCO_EN PL_VCCO_EN PL_VCU_EN	717	Bank 501	PS_VCCO_EN PL_VCCO_EN PL_VCU EN	PL P
Card Detection White Protected Data 1 Command Data 2	SD1_D1 SD1_CMD SD1_D2	Bank 501 M19 Bank 501 J21	SD1_D2 11	17 110				SYS_RESET_IN	SYSTE
O Card Detection Write Protected D Data 1 Command D Data 2 D Data 0 Clock	SD1_D1 SD1_CMD SD1_D2 SD1_D0 SD1_CLK	Bank 501 M19 Bank 501 J21 Bank 501 L20 Bank 501 L21	SD1_D2 11 SD1_D0 11 SD1_CLK 11	17 118 19 120	SYS_RESET_IN		Bank 503 Bank 503	SYS_KESET_IN	configuration his
O Card Detection Data 1 Command Data 2 Data 2 Data 2 Data 6 Clock Test Node Select Test Data Output	SD1_D1 SD1_CMD SD1_D2 SD1_D2 SD1_CLK PS_JTAG_TMS PS_JTAG_TD0	Bank 501 M19 Bank 501 J21 Bank 501 L20 Bank 501 L21 Bank 503 N21 Bank 503 T21	SDI_D2 11 SDI_D2 11 SDI_D6 11 SDI_CLK 11 PS_JTAG_TMS 12 PS_JTAG_TD0 12	17 118 19 120 21 122 23 124 25 126	SYS_RESET_IN PS_PROG_B PS_MODE0		Bank 503 Bank 503	PS_PROG_B PS_MODE0	configuration bloc
O Card Detection Data 1 Data 1 Data 2 Data 2 Data 3 Clock Jest Node Select Jest Node Select Jest Data Juput	SD1_D1 SD1_CMD SD1_D2 SD1_D0 SD1_CLK PSTTAG_TMS	Bank 501 M19 Bank 501 J21 Bank 501 L20 Bank 501 L21 Bank 503 N21	SDI_D2 11 SDI_D8 11 SDI_CLK 11 PS_JTAG_TMS 12 PS_JTAG_TD0 12 PS_JTAG_TD1 12 PS_JTAG_TD 12 PS_JTAG_TCK 12	25 126 27 128	SYS_RESET_IN PS_PROG_B PS_MODE0 PS_MODE1 PS_MODE2			PS_PR0G_B PS_MODE1 PS_MODE1 PS_MODE2	configuration bloc
Card betection Weiste Protected Data 1 Command Data 2 Data 2 Data 2 Clock Command Clock Command Clock Command Test Clock Command Test Command	S01_D1 S01_CM0 S01_CM0 S01_D2 S01_D0 S01_D0 S01_CLK PS_JTAG_TMS PS_JTAG_TD0 PS_JTAG_TD1 PS_JTAG_TC1 PS_JTAG_TC1 PS_JTAG_TC1 PS_JTAG_TC1 PS_JTAG_TC1 PS_JTAG_TC1 PS_JTAG_TC1 PS_JTAG_TC1	Bank 501 M19 Bank 501 J21 Bank 501 L21 Bank 503 L21 Bank 503 M21 Bank 503 R18 Bank 503 R18 Bank 505 E25	SDI_D2 1 1 1 1 1 1 1 1 1	25 126 27 128 29 130 31 132	SYS_RESET_IN PS_PROG_B PS_MODE0 PS_MODE1 PS_MODE2 GNOD PS_MGTRTXP1_505	R17	Bank 503 Bank 505	PS_PROG_B PS_MODE0 PS_MODE1 PS_MODE2 Ground PS_MITENTALTS_585	configuration bloc
Card betection Weiste Protected Data 1 Data 2 Data 2 Data 2 Clock Tiest Note Select	SDI_DI SDI_CMD SDI_DZ SDI_DB SDI_CLK PSJTAG_TMS PS_JTAG_TDD PS_JTAG_TDI PS_JTAG_TCK	Bank 501 M19 Bank 501 J21 Bank 501 L20 Bank 501 L21 Bank 503 N21 Bank 503 R18 Bank 503 R18 Bank 503 R19	SDL D2 JSDL D9	25 126 27 128 29 130 31 132 33 134 35 136	SYS_RESET_IN PS_PROG_B PS_MODE0 PS_MODE1 PS_MODE1 PS_MODE2 GND PS_MGTRIXP1_505 PS_MGTRIXV1_505	D23 D24	Bank 503	PS_PROG_B PS_MODE0 PS_MODE1 PS_MODE2 Ground	configuration bloc 11 11 11 11
O Card Detection Data 1 Data 1 Command O Command D Otac 8 D Otac 8 D Clock G Test Node Select G Test Node Select G Test Clock	SOL_D1 SOL_D40 SOL_D2 SOL_D2 SOL_D3 SOL_CLK SOL_CLK PS_TMAG_TMS PS_TMAG_TMD PS_TMAG_TD0 PS_TMAG_TOT PS_TMAG_TOT PS_TMAG_TOT PS_TMAG_TOT PS_MITTERVB_SOS	Bank 501 M19 Bank 501 121 Bank 501 L20 Bank 501 L21 Bank 503 N21 Bank 503 R18 Bank 503 R18 Bank 503 R19 Bank 503 R19 Bank 505 E25 Bank 505 E26	SOL D2 SOL D8 SOL L08 SOL L08 PS_3TAG_TMS_12 PS_3TAG_TMS_12 PS_3TAG_TMS_12 PS_3TAG_TMS_12 PS_3TAG_TMS_12 PS_3TAG_TMS_12 PS_3TAG_TMS_12 PS_MCTRYDMS_SSS_12	25 126 27 128 29 130 31 132 33 134 35 136 37 138 39 140	SYS, RESET, IM PS PROG, B PS PROG B PS MODE B PS MODE I PS MODE C SAND PS MOTERVAL J P	D23 D24	Bank 503 Bank 505 Bank 505	PS_PROCE PS_MODER PS_MODER PS_MODER PS_MODER PS_MODER PS_MOTRTVN1_SOS PS_MOTRTVN1_SOS PS_MOTRTVN1_SOS PS_MOTRTVN1_SOS PS_MOTRTVN1_SOS PS_MOTRTVN1_SOS PS_MOTRTVN1_SOS PS_MOTRTVN1_SOS	configuration bloc 11 17 17 17 17 18 19 19 19 19 19 19 19 19 19 19 19 19 19
D Data 3 Card Detection Unite Protected Dotta 1. Dotta 1. D Data 2 D Data 2 D Data 2 D Clock T Fest Mode Select T Fest Data Output T Fest Data Output T Fest Clock E E United Data 0 3.0 3.0 3.0 3.0 3.0	SOL_D1 SOL_CMD SOL_D2 SOL_D2 SOL_D2 SOL_D3 SOL_D4 SOL_D4 PS_TAG_TBG PS_TAG_TB	Bank 501 M19 Bank 501 120 Bank 501 120 Bank 501 L21 Bank 503 N21 Bank 503 721 Bank 503 R18 Bank 503 R19 Bank 505 E25 Bank 505 E26 Bank 505 C25	SSI_ 02 SSI_ 04 SSI_ 05 SSI_ 06 SSI_ 06 SSI_ 07 SSI_ 0	25 126 27 128 29 130 31 132 33 134 35 136 37 138 39 140	SYS, RESET, IM PS PROG, B PS PROG B PS MODE B PS MODE I PS MODE C SAND PS MOTERVAL J P	D23 D24 A25 A26	Bank 503 Bank 505 Bank 505 Bank 505	PS_PRIG_B PS_MODEL PS_MODEL PS_MODEL PS_MODEL Ground PS_MOTELS FS_MOTETXIL_SBS PS_MOTETXIL_SBS PS_MOTETXIL_SBS PS_MOTETXIL_SBS	configuration bloc 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
O Card Detection Unite Protected Data 1 Command Command Cottal C	SOL_D1 SOL_D4 SOL_D4 SOL_D5 SOL_D5 SOL_D5 SOL_D6 SOL_D6 SOL_D6 SOL_D6 SOL_D6 SOL_D7 SO	Bank 591 M19 Bank 591 J21 Bank 591 J21 Bank 591 L21 Bank 591 L22 Bank 593 T21 Bank 593 R19 Bank 593 R19 Bank 595 E26 Bank 595 C25 Bank 595 C25 Bank 595 D27 Bank 595 D28	SOI D2 SOI D3 SOI D4 SOI D6 SOI D7 SO	25 126 27 128 29 130 31 132 33 134 35 136 37 138 39 140 41 142 43 144 45 146 47 148	SYS_RESET_IN SYS_PROG_B BYS_PROG_B BYS_PROG_B BYS_PROG_B BYS_PROG_B BYS_PROG_B BYS_PROG_B BYS_PROG_B BYS_PROG_B BYS_PROG_B BYS_B BYS	D23 D24 A25 A26 B23 B24	Bank 505 Bank 505 Bank 505 Bank 505 Bank 505 Bank 505	PS_PROCE PS_MODE PS_MODE PS_MODE PS_MODE PS_MOTREYS_USS PS_MOTREYS	configuration bloc To see the see that the
O Card Detection Unite Protected Dota 1 Command Dota 2 Dota 3 First Node Select G Test Node Select G Test Node Select G Test Ota Data Input G Test Ota Data Input G Test Ota Select G Test Ota	SOL_D1 SOL_D40 SOL_D40 SOL_D40 SOL_D40 SOL_D40 SOL_C4K PS_TA6_TB0 PS_TA6_TB0 PS_TA6_TB0 PS_TA6_TB1	Bank 591 M19 Bank 591 J21 Bank 591 J21 Bank 591 L22 Bank 593 L22 Bank 593 T21 Bank 593 R19 Bank 593 R19 Bank 595 E25 Bank 595 E26 Bank 595 C26 Bank 595 C26	SOI_ D2 SOI_ D6 SOI_ D6 SOI_ D6 SOI_ D6 SOI_ D6 SOI_ D6 SOI_ D7 SOI_ D6 P5_ JTAC_ T70	25 126 27 128 29 130 31 132 33 134 35 136 37 138 39 140 41 142 43 144 45 146 47 148 49 150 53 154	SYS_RESE_T IN SYS_PROG_8 B SS_PROG_8 B SS_	D23 D24 A25 A26 B23 B24 B27 B28	Bank 505 Bank 505 Bank 505 Bank 505 Bank 505 Bank 505	PS_PROCE PS_MOTENTS_ PS_MOTENT	configuration bloc To recommend the configuration bloc PS MCTRR PS MCTRR PS MCTRR PS P

