

Lab 4: Pipelined MIPS Simulator

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Objective:

The objective of lab 4 was to extend the pipelined MIPS simulator from previous labs. This lab should be able to detect data hazards and handle them properly. This lab included two key parts pipeline stalls and forwarding.

Implementation:

This lab required implementing a way to detect data hazards. This was included in the ID stage to decide whether data hazards would be occurring soon. If they were detected stalls or forwards could be used. As shown in the lab document there are a few situations that data hazards could occur. These four possible data hazards are included and set off the data hazard flag if present. In the first part stalls were simply used as a way to wait out the impending data hazards. This led the pipelining being not very efficient. To correct this deficiency forwarding could be used. This allowed values that are ready to be used to be forwarded to the EX stage of an instruction awaiting that value. Using these forwards reduces the stalls needed and therefore produces a more efficient pipeline.

Conclusion and Results:

This lab successfully created a more efficient pipeline than was present in the previous lab. The previous iteration would have simply ignored data hazards while the new

product accounts for and ensures that data hazards will not be present. Therefore, this a successful and very necessary addition to the MIPS pipelined simulator.

Screenshots:

(no forwarding)

```
MU-MIPS SIM:> run 4
Running simulator for 4 cycles...
```

```
MU-MIPS SIM:> show
Current PC: 4194320
IF_ID.IR: 612696065
IF_ID.PC: 4194316
ID_EX.IR: 604241940
ID_EX.A: 0
ID_EX.B: 0
ID_EX.imm: 20
EX_MEM.IR: 1006833665
EX_MEM.A: 0
EX_MEM.B: 0
EX_MEM.ALUOutput: 268500992
MEM_WB.IR: 604110858
MEM_WB.ALUOutput: 10
MEM_WB.LMD: 0
MU-MIPS SIM:> run 2
Running simulator for 2 cycles...
```

```
Stalling..
Stalling..
MU-MIPS SIM:> show
Current PC: 4194320
IF_ID.IR: 612696065
IF_ID.PC: 4194316
ID_EX.IR: 0
ID_EX.A: 0
ID_EX.B: 0
ID_EX.imm: 20
EX_MEM.IR: 0
EX_MEM.A: 0
EX_MEM.B: 0
EX_MEM.ALUOutput: 20
MEM_WB.IR: 604241940
MEM_WB.ALUOutput: 20
MEM_WB.LMD: 0
MU-MIPS SIM:> sim
Simulation Started...
```

```

MU-MIPS SIM:> mdump
0x10010000
0x10010030
-----
Memory content [0x10010000..0x10010030] :
-----
[Address in Hex (Dec) ] [Value]
0x10010000 (268500992) : 0x00000015
0x10010004 (268500996) : 0x00000000
0x10010008 (268501000) : 0x00000000
0x1001000c (268501004) : 0x00000000
0x10010010 (268501008) : 0x00000000
0x10010014 (268501012) : 0x00000000
0x10010018 (268501016) : 0x00000000
0x1001001c (268501020) : 0x00000000
0x10010020 (268501024) : 0x00000000
0x10010024 (268501028) : 0x00000000
0x10010028 (268501032) : 0x00000000
0x1001002c (268501036) : 0x00000000
0x10010030 (268501040) : 0x00000000

MU-MIPS SIM:> q
*****
Exiting MU-MIPS! Good Bye...
*****

```

(forwarding on)

```

MU-MIPS SIM:> forward 1
Forwarding ON
MU-MIPS SIM:> run 4
Running simulator for 4 cycles...

MU-MIPS SIM:> show
Current PC: 4194320
IF_ID.IR: 612696065
IF_ID.PC: 4194316
ID_EX.IR: 604241940
ID_EX.A: 0
ID_EX.B: 0
ID_EX.imm: 20
EX_MEM.IR: 1006833665
EX_MEM.A: 0
EX_MEM.B: 0
EX_MEM.ALUOutput: 268500992
MEM_WB.IR: 604110858
MEM_WB.ALUOutput: 10
MEM_WB.LMD: 0
MU-MIPS SIM:> run 2
Running simulator for 2 cycles...

MU-MIPS SIM:> show
Current PC: 4194328
IF_ID.IR: 1007026192
IF_ID.PC: 4194324
ID_EX.IR: 2892300288
ID_EX.A: 268500992
ID_EX.B: 21
ID_EX.imm: 0
EX_MEM.IR: 612696065
EX_MEM.A: 20
EX_MEM.B: 0
EX_MEM.ALUOutput: 21
MEM_WB.IR: 604241940
MEM_WB.ALUOutput: 20
MEM_WB.LMD: 0
MU-MIPS SIM:> rdump
*****

```

MU-MIPS SIM:> rdump

Dumping Register Content

Instructions Executed : 0
Cycles Executed : 27
PC : 0x00400064

[Register] [Value]

[R0]	: 0x00000000
[R1]	: 0x00000000
[R2]	: 0x0000000a
[R3]	: 0x10010000
[R4]	: 0x00000014
[R5]	: 0x00000015
[R6]	: 0x00100000
[R7]	: 0x00000000
[R8]	: 0x00000000
[R9]	: 0x00000000
[R10]	: 0x00000007
[R11]	: 0x00000015
[R12]	: 0x00000002
[R13]	: 0x00000015
[R14]	: 0x00000015
[R15]	: 0x00000015
[R16]	: 0x0000002a
[R17]	: 0x00000000
[R18]	: 0x0000002a
[R19]	: 0x0000002a
[R20]	: 0x0000002a
[R21]	: 0x00000000
[R22]	: 0x00000000
[R23]	: 0x00000000
[R24]	: 0x00000000
[R25]	: 0x00000000
[R26]	: 0x00000000
[R27]	: 0x00000000
[R28]	: 0x00000000
[R29]	: 0x00000000
[R30]	: 0x00000000
[R31]	: 0x00000000

[HI] : 0x00000000
[LO] : 0x00000000

MU-MIPS SIM:> mdump

0x10010000

0x10010030

Memory content [0x10010000..0x10010030] :

[Address in Hex (Dec)]	[Value]
0x10010000 (268500992) :	0x00000015
0x10010004 (268500996) :	0x00000000
0x10010008 (268501000) :	0x00000000
0x1001000c (268501004) :	0x00000000
0x10010010 (268501008) :	0x00000000
0x10010014 (268501012) :	0x00000000
0x10010018 (268501016) :	0x00000000
0x1001001c (268501020) :	0x00000000
0x10010020 (268501024) :	0x00000000
0x10010024 (268501028) :	0x00000000
0x10010028 (268501032) :	0x00000000
0x1001002c (268501036) :	0x00000000
0x10010030 (268501040) :	0x00000000