Lab 5: Pipelined MIPS Simulator

ECE 4270

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Objective:

The objective of lab 5 was to expand the pipelining MIPS simulator from lab 4 to include control hazards as well as support branch and jump instructions. This also included implementing flushes.

Implementation:

This lab required that control hazards be detected within the MIPS simulator. Within the control hazard there are two different types. Those who require branching and those who do not. CheckControlHazard is the function where the detection occurs. It calls CheckBranch to see which of the two cases are happening.

This lab also included implementing the branch and jump instructions. These instructions were simply modified versions of the instructions as they were created in lab 1. These instructions are all found in the instructions.c file.

Conclusion and Results:

This lab included the testHazards.in file to test the MIPS pipelined processor and when running I believe it successfully handles the control hazards and uses

flushes as necessary. Screenshots show the rdump of the completed program as well as a few random sports throughout the execution.

```
MU-MIPS SIM:> sim
Simulation Started...

FLUSHING... [1]
FLUSHING... [2]
FLUSHING... [3]
FLUSHING... [4]
FLUSHING... [5]
FLUSHING... [6]
FLUSHING... [7]
FLUSHING... [8]
FLUSHING... [9]
FLUSHING... [10]
FLUSHING... [11]
FLUSHING... [12]
FLUSHING... [13]
FLUSHING... [14]
Simulation Finished.

MU-MIPS SIM:> rdump
-------------------------------------
Dumping Register Content
-------------------------------------
# Instructions Executed : 0
# Cycles Executed       : 148
PC      : 0x00400100
-------------------------------------
[Register]      [Value]
-------------------------------------
[R0]    : 0x00000000
[R1]    : 0x00000000
[R2]    : 0x0000000a
[R3]    : 0x00040000
[R4]    : 0xfffffff9
[R5]    : 0x00000008
[R6]    : 0x10010000
[R7]    : 0x00100001
[R8]    : 0x00008000
[R9]    : 0x00000004
[R10]   : 0x00000001
[R11]   : 0x00000001
[R12]   : 0x0000000a
[R13]   : 0x0000000a
[R14]   : 0x0000000a
[R15]   : 0x0000000a
[R16]   : 0x0000000a
[R17]   : 0x0000000a
[R18]   : 0x0000000a
[R19]   : 0x0000000a
[R20]   : 0x0000000a
[R21]   : 0x0000000a
[R22]   : 0x00007ffe
[R23]   : 0x00007fff
[R24]   : 0xfffc0000
[R25]   : 0x0000000a
[R26]   : 0x0000000a
[R27]   : 0x00000000
[R28]   : 0x00000000
[R29]   : 0x00000000
[R30]   : 0x00400090
[R31]   : 0x004000c4
-------------------------------------
[HI]    : 0x00000004
[LO]    : 0x00007fff
-------------------------------------
```

```
MU-MIPS SIM:> run 32
Running simulator for 32 cycles...

FLUSHING... [1]
MU-MIPS SIM:> show
Current PC: 4194360
IF_ID.IR: 4534306
IF_ID.PC: 4194356
ID_EX.IR: 0
ID_EX.A: 0
ID_EX.B: 1
ID_EX.imm: 10432
EX_MEM.IR: 338112
EX_MEM.A: 0
EX_MEM.B: 1
EX_MEM.ALUOutput: 8
MEM_WB.IR: 0
MEM_WB.ALUOutput: 268501000
MEM_WB.LMD: 1
MU-MIPS SIM:> rdump
------------------------------------
Dumping Register Content
------------------------------------
# Instructions Executed : 0
# Cycles Executed       : 32
PC      : 0x00400038
------------------------------------
[Register]      [Value]
------------------------------------
[R0]    : 0x00000000
[R1]    : 0x00000000
[R2]    : 0x10010008
[R3]    : 0x10010008
[R4]    : 0x00000001
[R5]    : 0x00000001
[R6]    : 0x00000000
[R7]    : 0x00000000
[R8]    : 0x00000000
[R9]    : 0x00000000
[R10]   : 0x00000000
[R11]   : 0x00000000
[R12]   : 0x00000000
[R13]   : 0x00000000
[R14]   : 0x00000000
[R15]   : 0x00000000
[R16]   : 0x00000000
[R17]   : 0x00000000
[R18]   : 0x00000000
[R19]   : 0x00000000
[R20]   : 0x00000000
[R21]   : 0x00000000
[R22]   : 0x00000000
[R23]   : 0x00000000
[R24]   : 0x00000000
[R25]   : 0x00000000
[R26]   : 0x00000000
[R27]   : 0x00000000
[R28]   : 0x00000000
[R29]   : 0x00000000
[R30]   : 0x00000000
[R31]   : 0x00000000
------------------------------------
[HI]    : 0x00000000
[LO]    : 0x00000000
------------------------------------
MU-MIPS SIM:>
```

```
MU-MIPS SIM:> run 64
Running simulator for 64 cycles...

FLUSHING... [2]
FLUSHING... [3]
FLUSHING... [4]
FLUSHING... [5]
FLUSHING... [6]
FLUSHING... [7]
MU-MIPS SIM:> show
Current PC: 4194428
IF_ID.IR: 605093898
IF_ID.PC: 4194428
ID_EX.IR: 0
ID_EX.A: 0
ID_EX.B: 0
ID_EX.imm: 0
EX_MEM.IR: 474021875
EX_MEM.A: 32767
EX_MEM.B: 0
EX_MEM.ALUOutput: 10
MEM_WB.IR: 605028362
MEM_WB.ALUOutput: 10
MEM_WB.LMD: 0
MU-MIPS SIM:> rdump
------------------------------------
Dumping Register Content
------------------------------------
# Instructions Executed : 0
# Cycles Executed       : 96
PC      : 0x0040007c
------------------------------------
[Register]      [Value]
------------------------------------
[R0]    : 0x00000000
[R1]    : 0x00000000
[R2]    : 0x00007fff
[R3]    : 0x00040000
[R4]    : 0xfffffff9
[R5]    : 0x00000008
[R6]    : 0x10010000
[R7]    : 0x00100001
[R8]    : 0x00008000
[R9]    : 0x00000004
[R10]   : 0x00000001
[R11]   : 0x00000001
[R12]   : 0x0000000a
[R13]   : 0x0000000a
[R14]   : 0x0000000a
[R15]   : 0x0000000a
[R16]   : 0x0000000a
[R17]   : 0x00000000
[R18]   : 0x00000000
[R19]   : 0x00000000
[R20]   : 0x00000000
[R21]   : 0x00000000
[R22]   : 0x00000000
[R23]   : 0x00000000
[R24]   : 0x00000000
[R25]   : 0x00000000
[R26]   : 0x00000000
[R27]   : 0x00000000
[R28]   : 0x00000000
[R29]   : 0x00000000
[R30]   : 0x00000000
[R31]   : 0x00000000
------------------------------------
[HI]    : 0x00000004
[LO]    : 0xfffc0000
------------------------------------
```