

Divyanshu Jain

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Industry Experience

NXP Semiconductors

System Design Engineer

Irvine

2016–present

- Designed, simulated, coded, tested and verified parts of NXP's first UWB chip targetting secure indoor localization.
- Tested and verified reader demodulation design of the latest NFC chip using system Verilog.
- Created modem design verification infrastructure using python, MATLAB and bash.

Broadcom Corp.

System Design Engineer

Irvine

2013–2016

- Developed part of ultra low power Bluetooth and ZigBee receiver. Algorithmic and systemic approaches were employed to achieve the objective.
- Designed a template for converting C++ algorithms to RTL using HLS tools like FORTE.
- Verified frequency synchronization algorithms for Broadcom's NFC chips. Also, hacked other competitor's NFC chips to compare and understand the performance of their receiver's algorithm
- Wrote template code for converting Simulink designs to C++ using Real Time Workshop.
- Created scalable infrastructure in python, MATLAB to perform functional verification, bitmatching and code coverage to validate the design.

Mojix Inc.

Member of Technical Staff

Los Angeles

2008–2013

- Developed firmware and hardware for Mojix RFID Interrogators (implement real time protocol standardized by EPC to query and manage tag population).
- Wrote microcontroller (ARM Cortex-M3) code in C for Mojix low power signal distributors and regenerators.
- Implemented a conductive testing procedure to characterize performance of RFID Readers via BER curves by generating random tag signal mixed with Gaussian noise at different Eb/No values.
- Member of the team involved in designing and implementing a proprietary protocol to transmit protocol commands and receive sensor data, tag data over a wired link passing through multiple devices in a massive distributed network.
- Coded and developed a part of the python - Tk based GUI to control, test and setup parameters of our RFID system.

Qualcomm Inc.

Interim Engineering Intern

San Diego

2008–2008

- Wrote a high level design document for carrier frequency offset estimation.
- Visualized the LTE modem system timeline using GTK wave analyzer.

Technical skills

Languages: C/C++, Assembly, Verilog, Python, Java, Tcl

Platform: Linux, Windows

Concepts: Signal Processing, Filters, Probability, Artificial Intelligence, Algorithms

Dev Tools: MATLAB, Simulink, Verdi, FORTE, IDEs

Software: Office, Version Control Systems

Hardware: Pattern and Waveform Generators, Oscilloscopes, Spectrum Analyzers

Education

University of California

Masters in Electrical Engineering, GPA 3.7/4.0

Los Angeles, California

2006–2007

Madhav Institute of Technology and Science

Bachelors in Electrical Engineering, Aggregate 80.2/100.0

Gwalior, India

2002–2006

Masters thesis

Title: *Optimization techniques for Implementing Real Time MIMO channel estimation on a DSP (TI-C64x)*

- Simulated minimum number of channel coefficient bits required to be within permissible error bounds.
- Optimized hand written assembly code via novel techniques:
 - Leveraged input data properties. (Used simulated number of bits for division algorithm selection)
 - Equalized load across different functional units of the processor. (by using suboptimal instructions)
 - Eliminated cross path stalling by manual scheduling.

Awards

Academic Distinction

Bhojwani scholarship for securing highest marks in junior year.

M.I.T.S. Gwalior, India

June 2005

Patents

- Dong-U Lee, Divyanshu Jain, 2016. *Feedback-based adaptive load modulation (ALM) for a near field communication (NFC) device*, U.S. Patent **US9590701 B2** filed July 27, 2015, and issued Mar 7, 2017.
- Manolis Frantzeskakis, Dong-U Lee, Divyanshu Jain, Jianhua Gan, Shengyang Xu, 2016. *Carrier synchronization appropriate for alm nfc data transmission* U.S. Patent **US20160241384 A1** filed October 20, 2015, and issued August 18, 2016.