Divyanshu Jain |

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Industry Experience

Broadcom Inc. **Irvine**
System Design Engineer *2013–present*

- Developed part of ultra low power Bluetooth and ZigBee receiver. Algorithmic and systemic approaches were employed to achieve the objective.
- Designed a template for converting C++ algorithms to RTL using HLS tools like FORTE.
- Verified frequency synchronization algorithms for Broadcom's NFC chips. Also, hacked other competitor's NFC chips to compare and understand the performance of their receiver's algorithms.

Mojix Inc. **Los Angeles**
Member of Technical Staff *2008–2013*

- Developed firmware and hardware for Mojix RFID Interrogators (implement real time protocol standardized by EPC to query and manage tag population).
- Wrote microcontroller (ARM Cortex-M3) code in C for Mojix low power signal distributors and regenerators.
- Implemented a conductive testing procedure to characterize performance of RFID Readers via BER curves by generating random tag signal mixed with Gaussian noise at different Eb/No values.
- Member of the team involved in designing and implementing a proprietary protocol to transmit protocol commands and receive sensor data, tag data over a wired link passing through multiple devices in a massive distributed network.
- Coded and developed a part of the python - Tk based GUI to control, test and setup parameters of our RFID system.

Qualcomm Inc. **San Diego**
Interim Engineering Intern *2008–2008*

- Wrote a high level design document for carrier frequency offset estimation for the LTE project and assembly coded the critical sections to optimize processor cycle usage.
- Plotted the system timeline using GTK wave analyzer showing interaction between functions (channel estimation, frequency estimation, IFFT) and the respective time taken in each routine.

Technical skills

Languages: C/C++, Assembly, Python, Java, Verilog, Tcl

Platform: Linux, Windows

Concepts: Signal Processing, Filters, Probability, Artificial Intelligence, Algorithms

Dev Tools: MATLAB, Simulink, Verdi, FORTE, IDEs

Software: Office, Version Control Systems

Hardware: Pattern and Waveform Generators, Oscilloscopes, Spectrum Analyzers

Education

University of California **Los Angeles, California**
Masters in Electrical Engineering, GPA 3.7/4.0 *2006–2007*

Madhav Institute of Technology and Science **Gwalior, India**
Bachelors in Electrical Engineering, Aggregate 80.2/100.0 *2002–2006*

Masters thesis

Title: *Optimization techniques for Implementing Real Time MIMO channel estimation on a DSP (TI-C64x)*

- Simulated minimum number of channel coefficient bits required to be within permissible error bounds.
- Optimized hand written assembly code via novel techniques:
  - Leveraged input data properties. (Used simulated number of bits for division algorithm selection)
  - Equalized load across different functional units of the processor. (by using suboptimal instructions)
  - Eliminated cross path stalling by manual scheduling.

Awards

Academic Distinction **M.I.T.S. Gwalior, India**
Bhojwani scholarship for securing highest marks in junior year. *June 2005*