FPD-Link PCB guidelines for the TRAVEO™ T2G family CYT4D series MCUs

Associated part number

- CYT4D Series

About this document

Scope and purpose

AN226037 provides PCB layout guidelines for the flat panel display link interface (FPD-Link) for TRAVEO™ T2G Family CYT4D Series MCUs.

Intended audience

This document is intentded for anyone using TRAVEO™ T2G family CYT4D series.

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1 Introudction

TRAVEO™ T2G Family CYT4D Series MCUs have an FPD-Link used to connect high-performance video displays. FPD-Link is a high-speed interface using low-voltage differential signaling (LVDS).

The FPD-Link graphics display port of CYT4D Series MCUs has the following characteristics:

- High speed: Data rates up to 350 Mbps per lane
- Low voltage swing: Approximately 350 mV
- Five differential signals: TxCLK± and TxDOUT[0:3]±

Due to these characteristics, the PCB for FPD-Link cannot be treated as a simple group of traces. This application note provides guidelines for the layout of the FPD-Link PCB for CYT4D Series devices.

2 Recommended PCB specifications

The following best practices are recommended for routing the LVDS signals used in an FPD-Link interface:

- Use balanced transmission lines with a characteristic impedance of 100 Ω ±10%.
- Avoid vias by using the programmable inversion and output signal selection[1] abilities of the FPD-Link Controller.
- Ensure that the PCB design conforms to the parameters listed in Table 1.

Table 1 PCB layout trace space, width, and length

S_{DP}	Space between differential pair signals (CLK+[2] and CLK–[3] or DIF+[4] and DIF–[5])	Minimum Pair spacing[6]	Figure 1, Figure 2, Figure 3
S_{DD}	Space between differential signals and GND, differential CLK± and differential DIF±, or differential DIF± and other differential DIF±	Minimum Pair spacing x 2	Figure 1, Figure 2, Figure 3
S_{DC}	Space between differential signals and logic signals	Minimum Pair spacing x 4	Figure 2
W_{PCB}	Width of trace	Trace width[6]	Figure 1, Figure 2, Figure 3
L_{DP}	Length difference between the true (+) and complement (–) signals of a differential pair (CLK+ and CLK–, or DIF+ and DIF–)[7]	Maximum 5 mm	Figure 4
L_{DD}	Length difference between any two differential signals (CLK± and DIF± or DIF± and any other DIF±)[7]	Maximum 5 mm	Figure 4

1 CYT4D Series MCUs can select the output signal for FPD-Link. See the Architecture Technical Reference Manual (TRM) for more details.
2 CLK+ is the true/positive (+) signal of the differential clock.
3 CLK– is the complement/negative (–) signal of the differential clock.
4 DIF+ is the true/positive (+) signal of a differential data line.
5 DIF– is the complement/negative (–) signal of a differential data line.
6 This value is determined by the specifications of the layer thicknesses and dielectric materials used by the board manufacturer. To ensure proper differential impedance in manufacturing, it is recommended to include a test transmission line on a coupon adjacent to each board, and verify the transmission line impedance as part of the test process of the bare board.
7 For microstrip transmission lines in FR-4 with a dielectric constant of 4.7.

3 PCB design considerations

3.1 Layer layout

Balanced transmission lines for the FPD-Link signals may be implemented as any of the following types:[8]

- Edge-coupled microstrip[9], [10]
- Edge-coupled stripline
- Broadside-coupled stripline

This application note shows edge-coupled microstrip in the examples.

If the PCB has four or more layers, use the structure shown in Figure 1. This places the balanced microstrip traces on one side of the board, and the noisy logic traces on the opposite side of the board.[11]

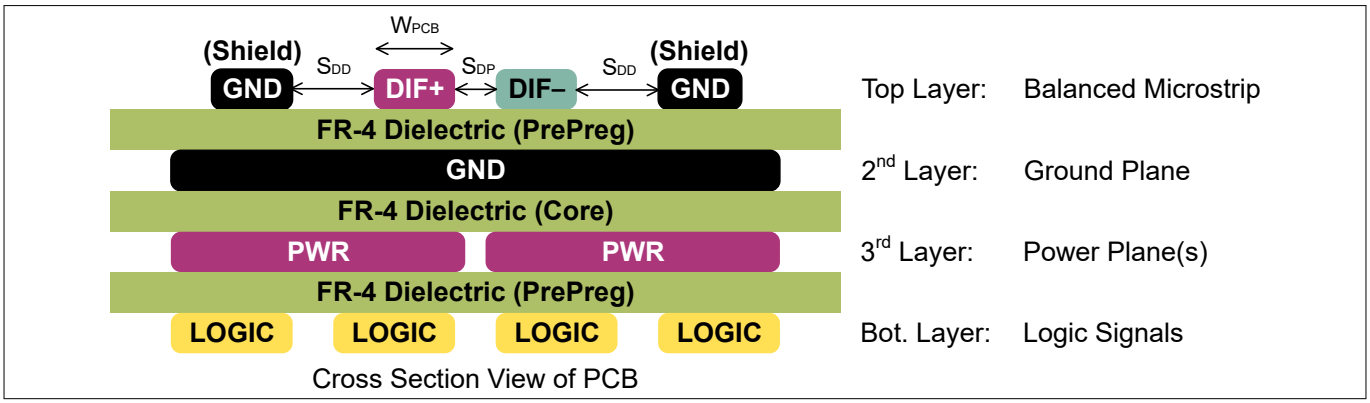

Figure 1 Layout guidelines for 4-layer PCBs

If the PCB has only two layers, or requires both logic and balanced microstrip traces on the same layer, do the following.

- Type-I: Use a GND trace between any logic trace and the nearest trace of any balanced transmission line to act as a shield.
- Type-II: Use at least four times the space between the traces of a balanced microstrip transmission line as the space between any logic trace, and either trace of that balanced transmission line (see Equation 1).

Equation 1

$$S_{DC} = 4 \times S_{DP}$$

Figure 2 shows examples of Type-I and Type-II recommended layouts.

8 While any of these transmission line constructs can be used, do not mix the types; that is, do not use balanced microstrip for some signals and balanced stripline for others. The signals propagate at different rates on these transmission lines, which makes it difficult to maintain matched delays.

9 Most design equations for microstrip and balanced microstrip do not consider the dielectric impact of the soldermask layer. When selecting a new board manufacturer, a test board allowing evaluation of multiple different spacings is recommended to determine the target values for the board design.

10 Do not use gold-plated traces as a replacement for soldermask. The nickel diffusion-barrier layer has ferromagnetic properties that distort high-speed signals.

11 LVDS signals are ground-referenced. When implementing balanced microstrip transmission lines, it is preferred to couple the lines to a ground plane instead of a power plane. When coupled to a power plane, noise on that supply is coupled as common-mode noise to the signals on the transmission lines.

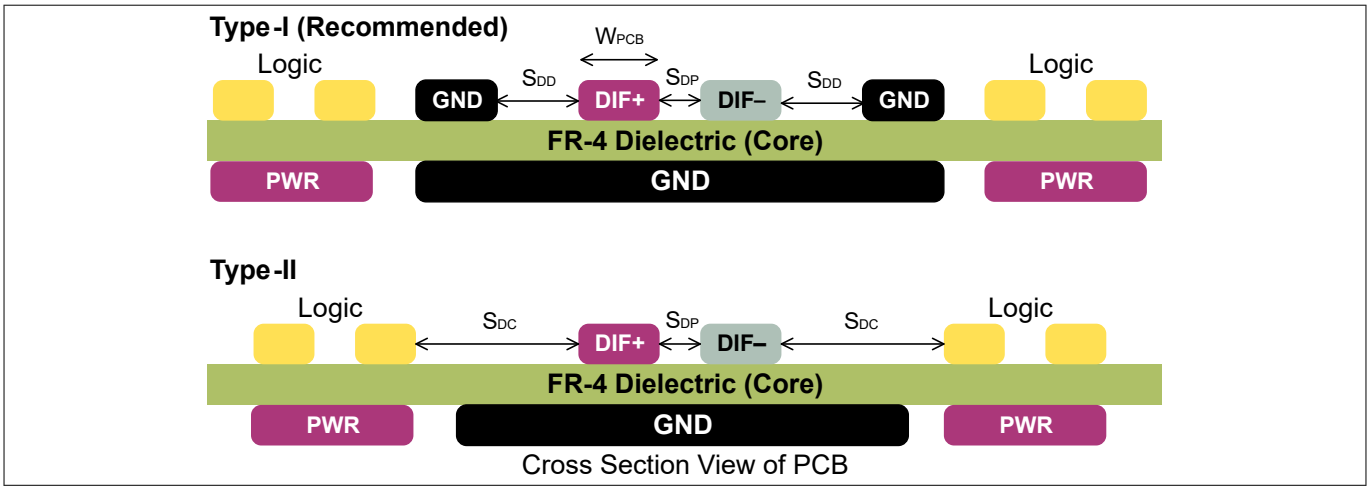

Figure 2 Recommended layouts

3.2 Balanced transmission lines spacing

When two or more balanced transmission lines are present in the same layer, do the following:

- Type-I: Use a ground (GND) trace between each balanced transmission line to act as a shield.
- Type-II: Use twice the space between the traces of a balanced microstrip transmission line and other balanced transmission lines (see Equation 2).

Equation 2

$$S_{DD} = 2 \times S_{DP}$$

Figure 3 shows two examples of balanced transmission lines spacing.

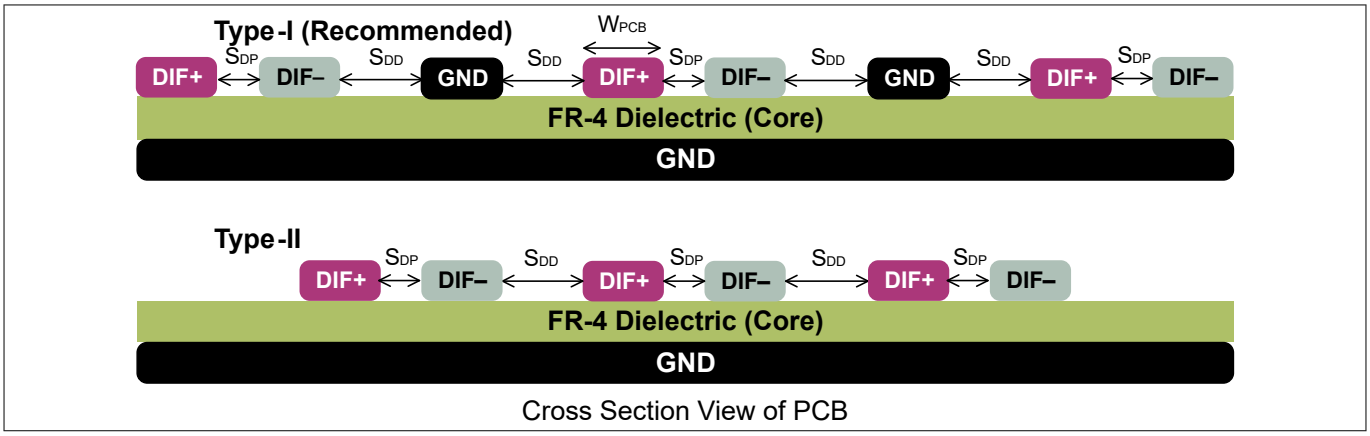

Figure 3 Balanced transmission lines spacing

3.3 Physical length/Delay matching

The physical length of the traces, which form each balanced transmission line and the level of matching, determine most of the signal integrity and timing margin of the interface. Length must be matched between the true and complement traces that form each balanced transmission line (L_{DP}) and between different balanced transmission lines (L_{DD}). The matching of physical length is used to limit the conversion of a differential signal into common-mode, and the differences in delay of each transmission line between the source and destination. Figure 4 shows three differential pairs routed between the sending device (CYT4D) and a connector, and how routing can introduce differences in physical length.

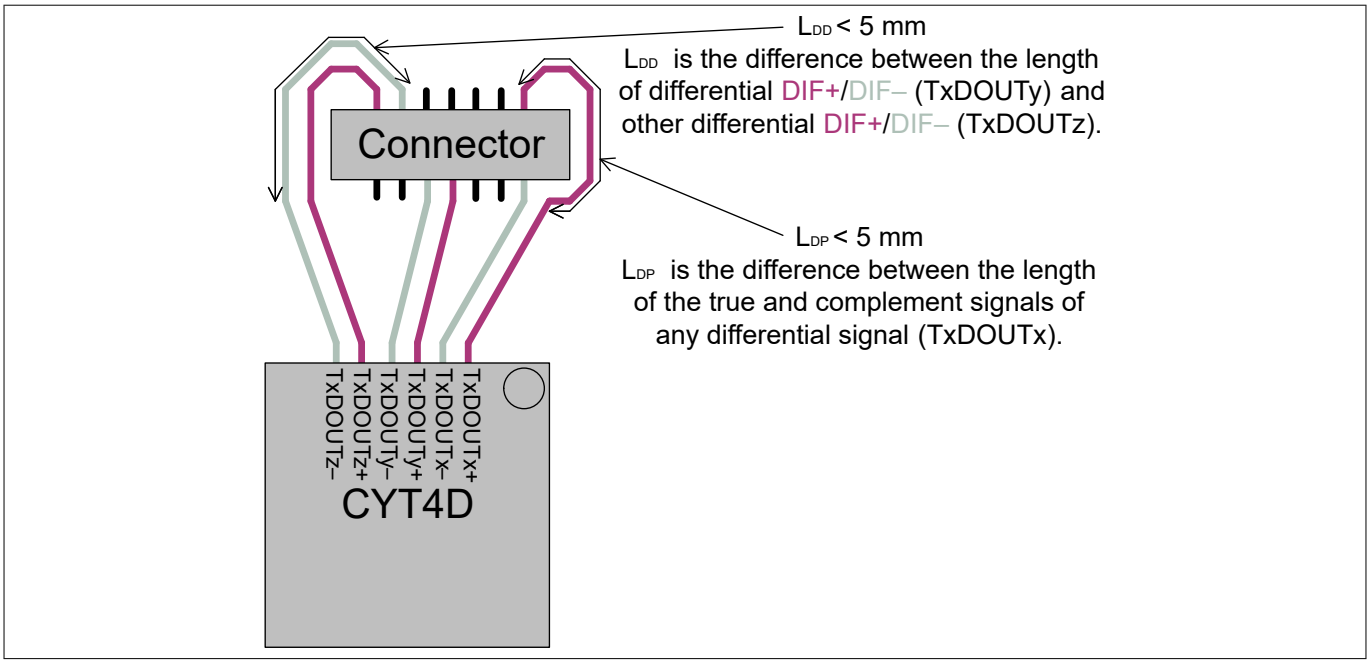

Figure 4 Physical length

Of the three balanced transmission lines shown in Figure 4, the TxDOUTy± signal has the best matching of trace length within the balanced pair ($L_{D\ P}$). Though there is a mismatch in the trace length of the TxDOUTz± signal, a difference of less than 5 mm is acceptable. However, for the TxDOUTy± signal, there is a significant difference in trace length between the TxDOUTx+ and TxDOUTx– signals, and this should be avoided.

When routed as a balanced microstrip on FR4, each millimeter of length equates to approximately 10 ps of delay[12], and every millimeter of length difference between traces equates to a time offset of 10 ps. When there is a difference in length between the true and complement traces of a balanced transmission line, the electromagnetic field between these two traces becomes unbalanced, and some of the energy in the signal is converted to common-mode. This conversion should be avoided wherever possible for the following reasons:

- Common-mode energy radiates as EMI
- Common-mode noise couples as crosstalk to nearby signals
- Imbalance causes a reduction in differential signal integrity

As noted in Table 1, it is recommended to limit the mismatch between true and complement signals within a balanced pair (L_{DP}) to no more than 5 mm or 50 ps. This limitation is based on the rise or fall time of the signals on these transmission lines (typically 400 ps), and remains the same regardless of the signaling rate.

While there appears to be a significant signal length mismatch ($L_{D\ D}$) between the TxDOUTy± and TxDOUTz± signals, the routing to one connector only shows a part of the transmission line. There is often a second connector at the other end of the cable, so the exit-routing of that connector may be used to compensate for the entry-routing to a local connector. When measuring L_{DD}, the total mismatch in length is between the pins of the sending device (CYT4D) and the pins of the receiving device (normally a display), and not just with the local connector.

The recommendation in Table 1 for L_{DD} is also 5 mm (50 ps), but this is for an operation at the 50-MHz clock rate of the FPD-Link interface. The L_{DD} mismatch causes an increase in the transmit pulse position offset (TPPOS) by offsetting the clock and data signals. With a TxCLK± of 50 MHz, each data line carries 350 Mbps of video; the unit interval (UI) of this data is 2.85 ns. At this signaling rate, a 50-ps offset is less than 0.02 UI, and reduces the link timing margin by less than 2%. At slower signaling rates, larger L_{DD} offsets are usually acceptable if the interface meets the setup and hold requirements at the display end of the FPD-Link interface.

12 For microstrip transmission lines in FR-4 with a dielectric constant of 4.7.

3.4 Trace routing limitations

Do not use 90-degree bends when routing traces; instead, use 45-degree angles or curves because sharp bends have additional capacitance between the traces, which causes a change in the transmission line impedance. Figure 5 shows trace routing recommendations.

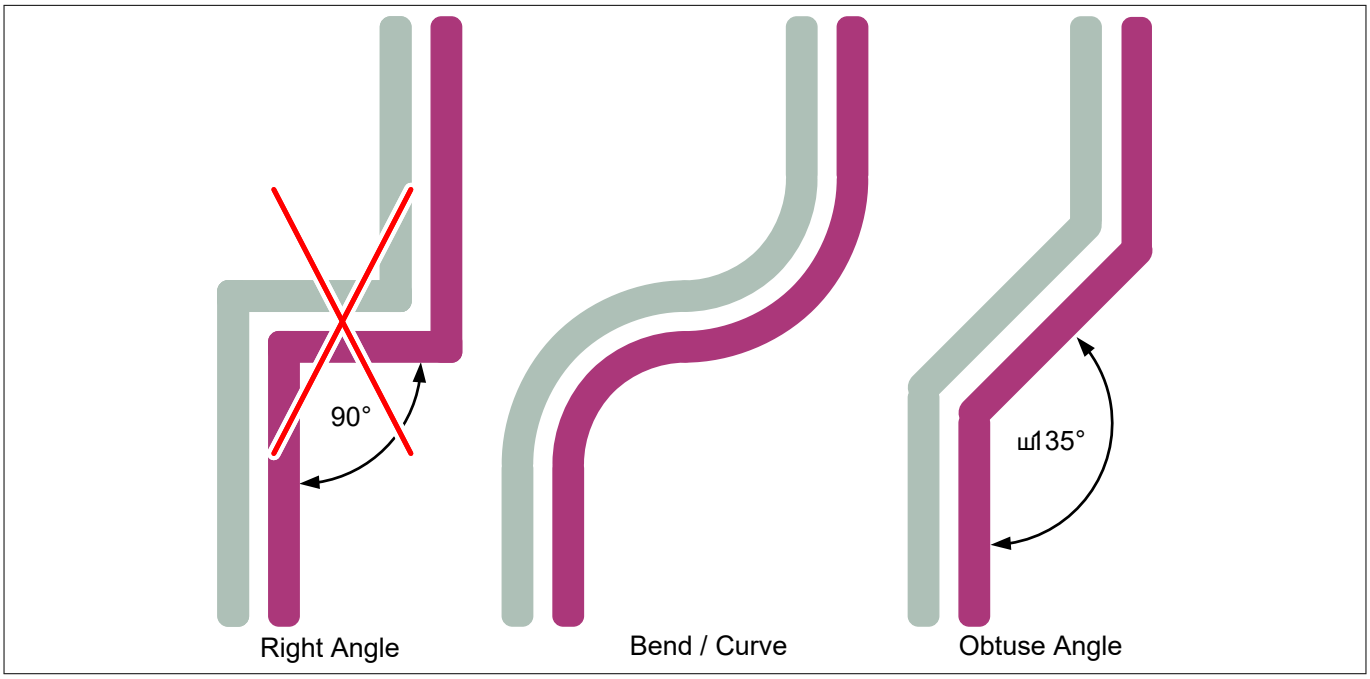

Figure 5 Trace routing recommendations

3.5 Layout of power and ground

Power and ground traces should be as short and wide as reasonably possible. Power for the FPD-Link should be isolated from other power domains of the regulator. Place bypass capacitors near power and ground pins. Figure 6 shows a layout of power and ground.

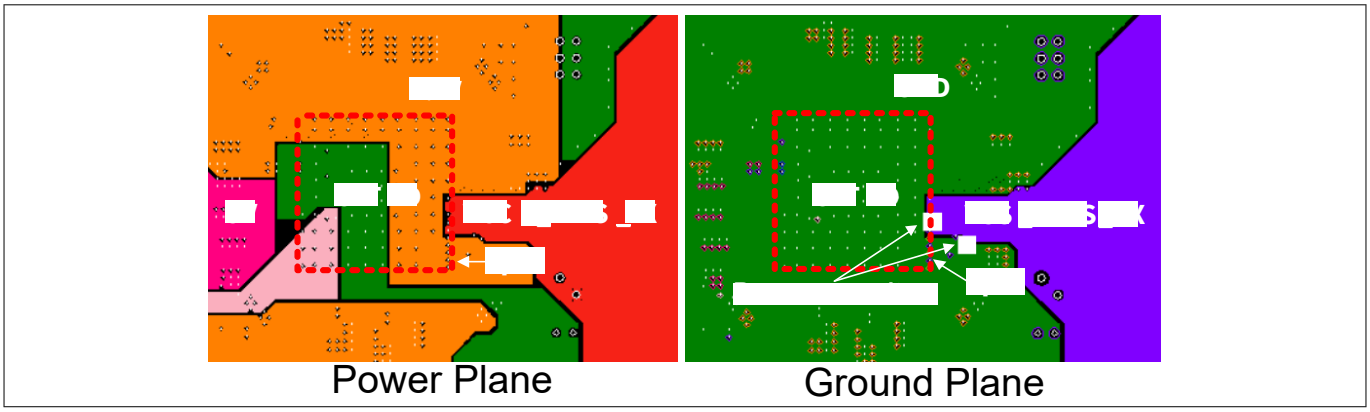

Figure 6 Layout of power and ground

3.6 Distance between IC and connector

Theoretically, the distance between the driver and receiver on a transmission line should have limited impact on the signaling. In reality, the longer and more complex the routing between these points, the larger is the imbalance introduced into the signals and the more difficult it becomes to maintain a matched delay for all five

balanced pairs. When possible, place the IC as close as possible to the FPD-Link connector. Figure 7 shows the recommended routing between the IC and connector.

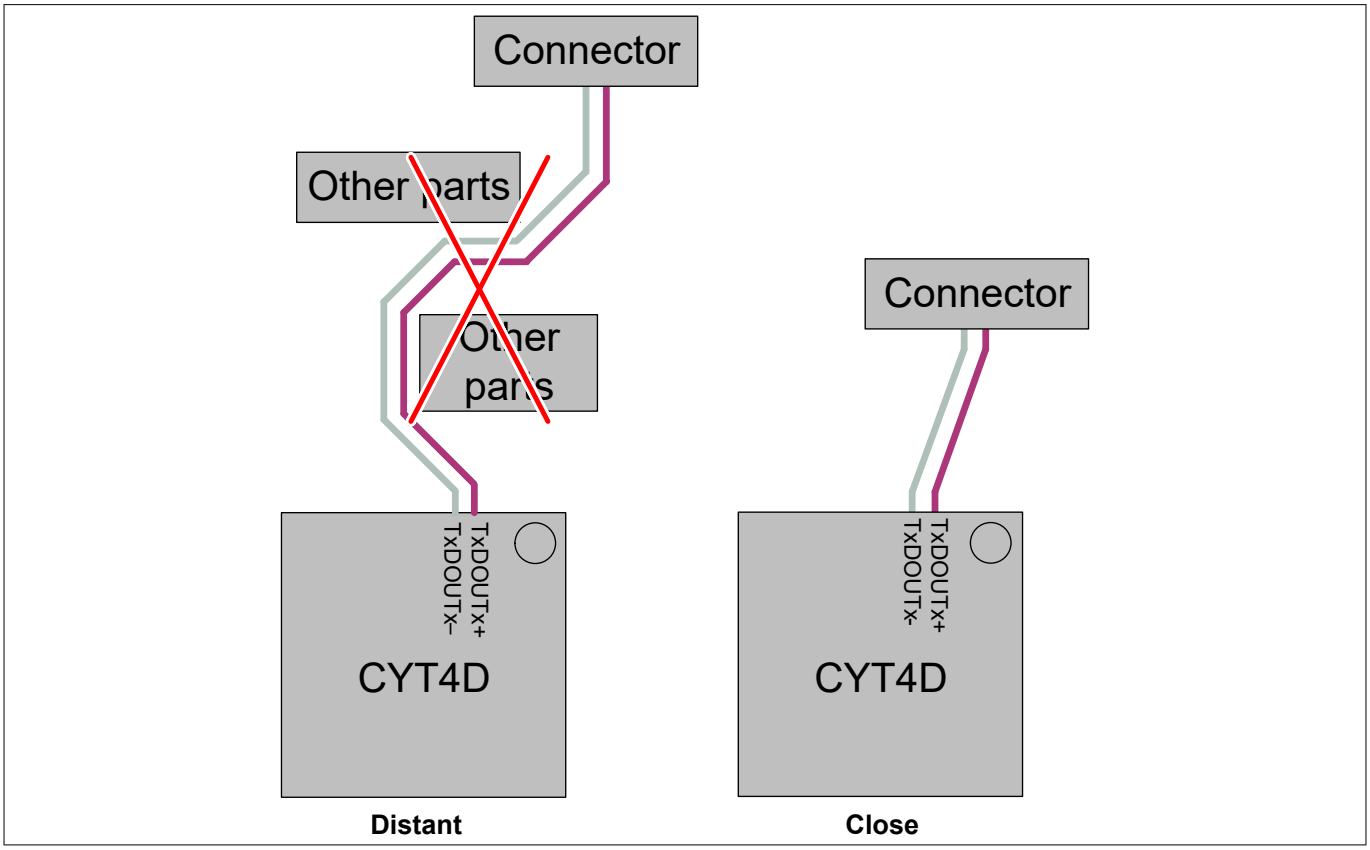

Figure 7 Distance between IC and connector

3.7 Signal assignment to the connector

When assigning signals to the pins of the connecter, consider the following:

- Make sure that the connectors have a low skew with matched impedance.
- Select connectors with the same lead lengths for a lower skew and crosstalk.
- Route the true and complement signals of the same differential pair to adjacent pins of the connector.
- If possible, place ground pins between differential pairs.
- PreEnd pins of the connectors should preferably be grounded and must not be used for high-speed signals.
- Terminate all unused pins of the connector to ground.

Figure 8 shows two examples of signal assignments of the connector. While the signal assignment on the upper diagram does introduce a mismatch in signal length between the true and complement signals of the differential pair (L_{DP}), if the pin spacing between rows of the connector is small (< 3 mm), this should remain below the 5-mm target. Signal assignment in the lower diagram introduces a small difference in length between differential signals (L_{DD}). This can be compensated by adjusting the lengths of the signals at the other end of the cable exiting from the opposite side of the connector.

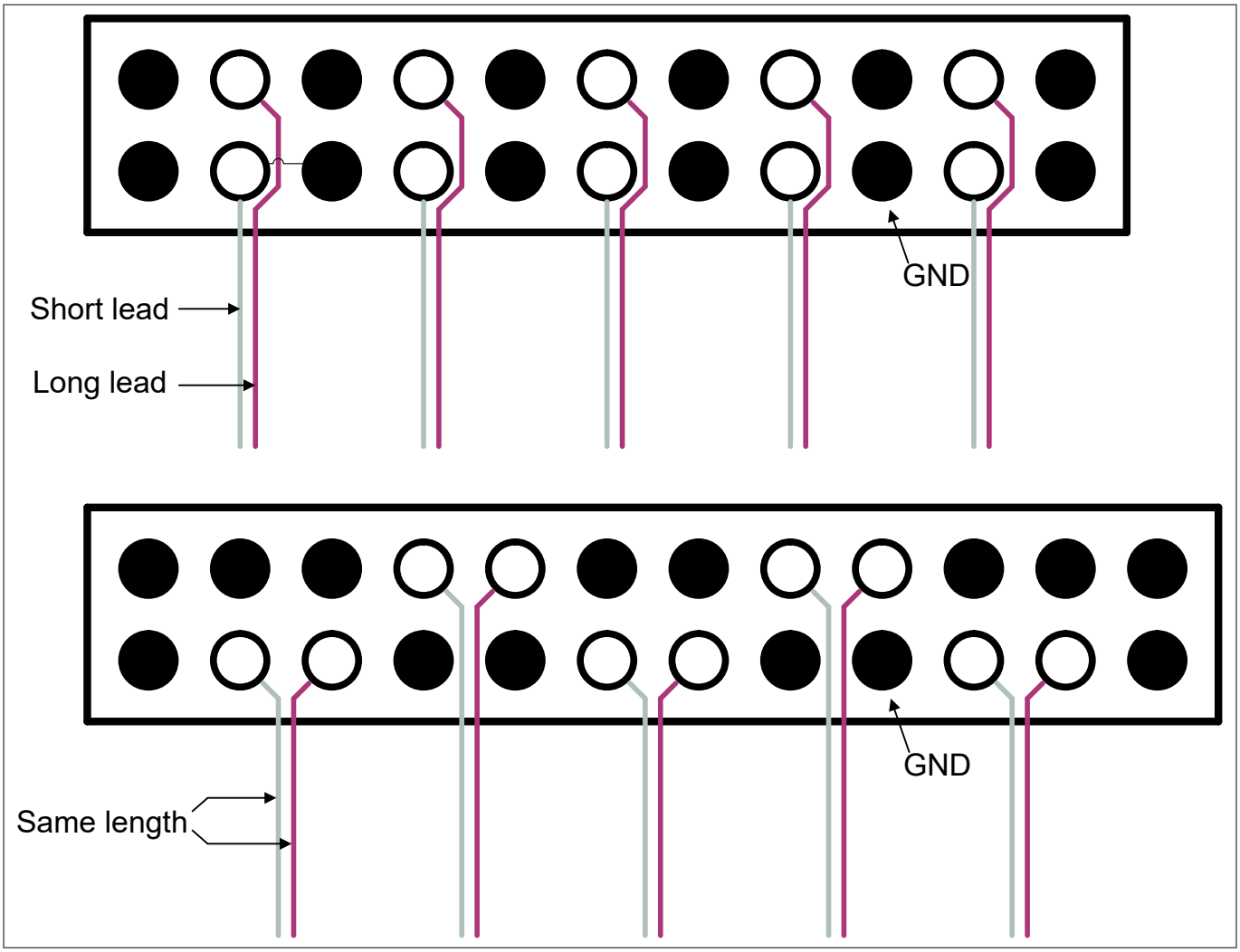

Figure 8 Signal assignment to the connector

4 References

The following are the TRAVEO™ T2G family series datasheets and Technical Reference Manuals. Contact Technical Support to obtain these documents.

- Device datasheet
  - CYT4DN Datasheet 32-Bit Arm® Cortex®-M7 Microcontroller TRAVEO™ T2G Family
- Cluster 2D Family
  - TRAVEO™ T2G Automotive Cluster 2D Family Architecture Technical Reference Manual (TRM)
  - TRAVEO™ T2G Automotive Cluster 2D Registers Technical Reference Manual (TRM)

Revision history

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*A	2023-11-12	Template update; no content update

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Do you have a question about any aspect of this document?

Email: erratum@infineon.com

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