

# LCD controller setup in TRAVEO™ T2G family

## About this document

### Scope and purpose

This application note explains how to set up the LCD controller in TRAVEO™ T2G family CYT2CL series MCU.

### Intended audience

This document is intended for anyone who uses the TRAVEO™ T2G family MCUs with LCD controller.

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## Introduction

# 1 Introduction

This application note describes the LCD controller configuration for TRAVEO™ T2G family CYT2CL series MCUs. This LCD controller allows the MCU to drive super twisted nematic (STN) and twisted nematic (TN) segment LCDs directly.

To understand the functionality described and terminology used in this application note, see the “LCD controller” chapter in the [architecture technical reference manual \(TRM\)](#).

## 1.1 Features

The LCD controller has the following features:

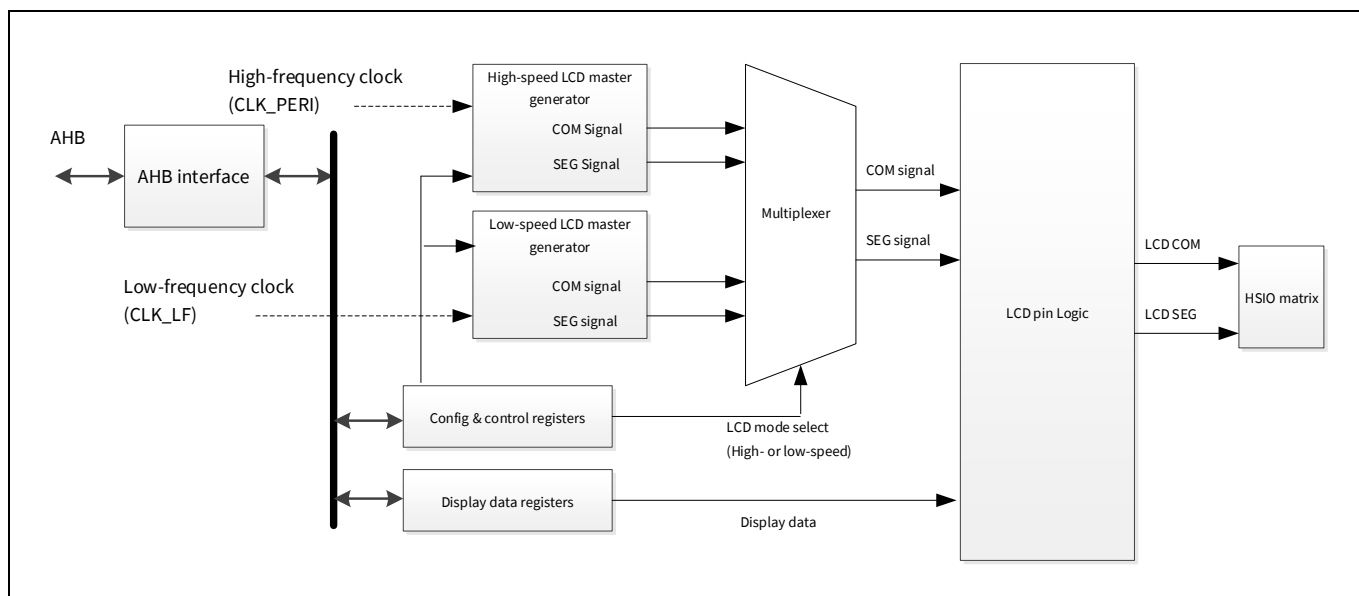
- Supports up to 32 segments (SEG) and four commons (COM)
- Supports Type A (standard) and Type B (low-power) drive waveforms
- Enables configuring any GPIO pin as a common or segment
- Supports three drive methods:
  - PWM at 1/2 bias
  - PWM at 1/3 bias
  - Digital correlation
- Operates in Active, Sleep, and DeepSleep power modes
- Enables digital contrast control

## LCD controller overview

## 2 LCD controller overview

### 2.1 Operation overview

**Figure 1** shows a simplified block diagram of the LCD controller in CYT2CL series MCUs.



**Figure 1 LCD controller block diagram**

The LCD controller block contains two generators: a high-speed clock source (based on CLK\_PERI) and a low-speed clock source (based on CLK\_LF). These are called high-speed and low-speed LCD master generators respectively. Both the generators support PWM and digital correlation drive modes.

The multiplexer selects one of these two generator outputs to drive the LCD controller as configured by firmware. The LCD pin logic block routes the COM and SEG outputs from the generators to the corresponding I/O matrices. Any GPIO pin can be used as either COM or SEG. This configurable pin assignment for COM or SEG is implemented in the GPIO and I/O matrix. See the “I/O system” chapter in the [architecture TRM](#).

The two generators share the same configuration registers. These memory-mapped I/O registers are connected to the system interconnect bus using an AHB interface.

The LCD controller works in three device power modes: Active, Sleep, and DeepSleep. High-speed operation is supported in Active and Sleep modes. Low-speed operation is supported in Active, Sleep, and DeepSleep modes. The LCD controller is not powered in Hibernate mode.

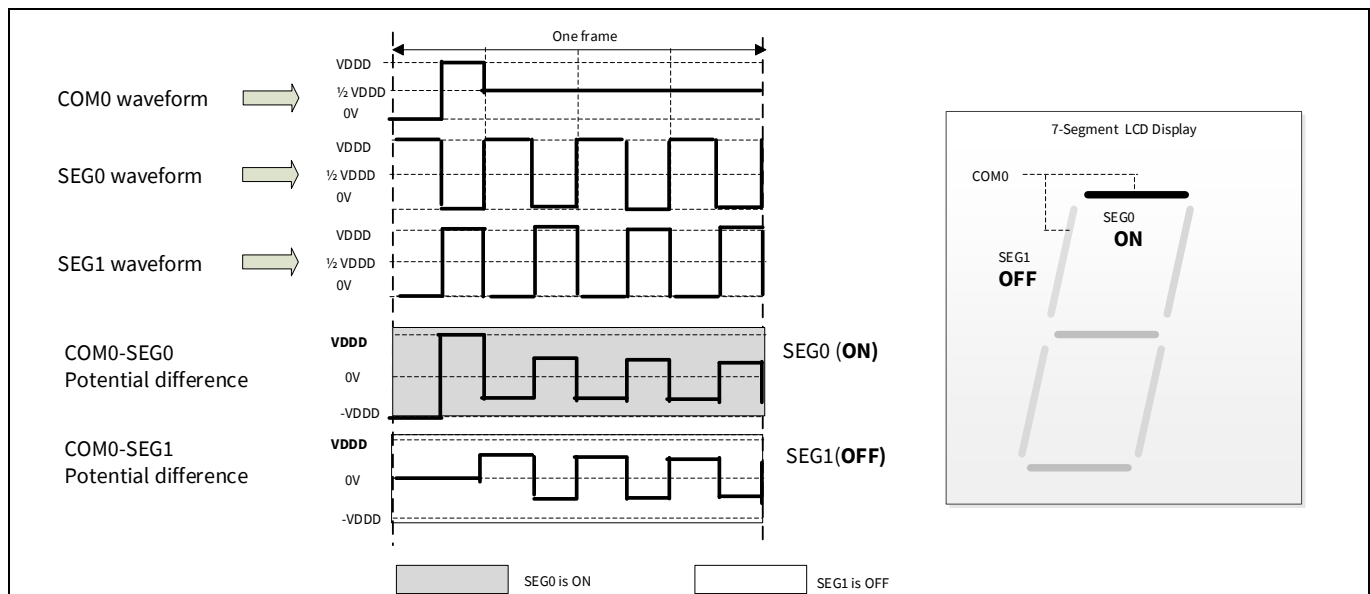
Note: DeepSleep operation is supported only with internal clocks (IMO/ILO).

## LCD controller overview

### 2.2 Segmented LCD panel

A segmented LCD panel has the liquid crystal material between two sets of electrodes and various polarization and reflector layers. The two electrodes of an individual segment are called commons (COM) and segment electrodes (SEG). From an electrical perspective, an LCD segment can be considered as a capacitive load. These COM and SEG electrodes can be considered as the rows and columns in a matrix of segments.

**Figure 2** shows the relationship between COM0 and SEG0/1 in the 7-segment LCD display.



**Figure 2** 7-segment display by combining COM0 and SEG0/1 waveform

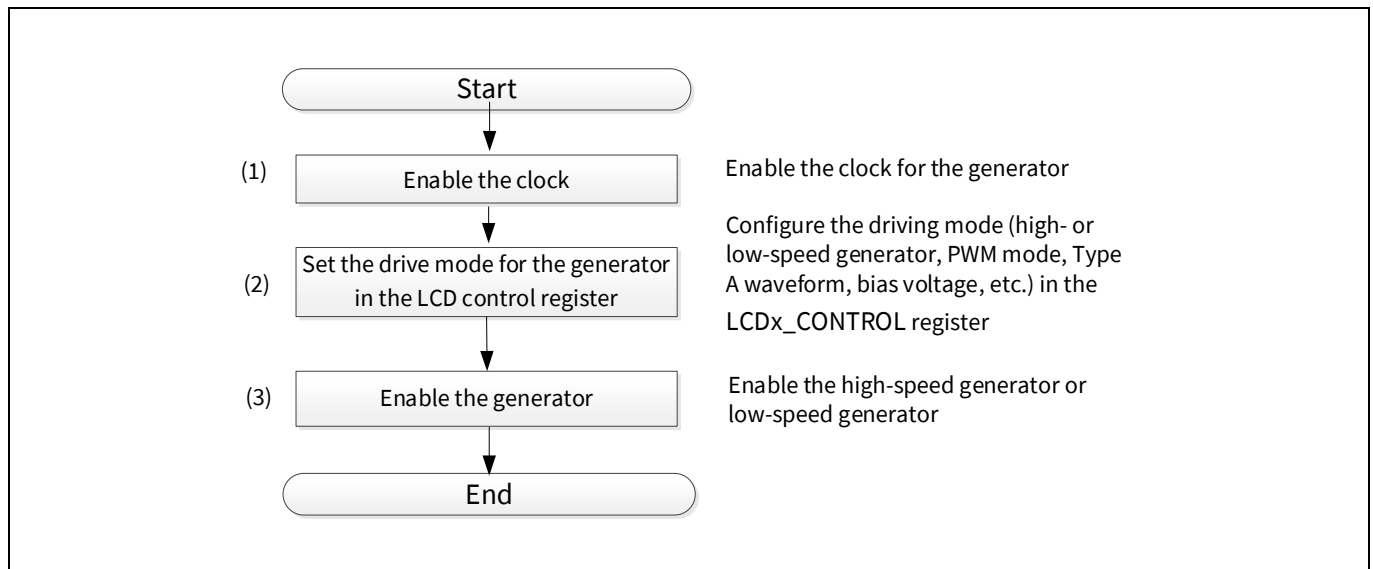
In this example, the 7-segment LCD display, COM0, and SEG0/1 are connected as shown in **Figure 2**, and drive in PWM mode at 1/2 bias with type A waveforms. This configuration addresses the COM signal once per frame and sets the voltage in three steps. The SEG signal is output continuously. When the potential difference between COM0 and SEG0 is reached to  $V_{DD}$  in the same phase, SEG0 is turned ON. If the potential difference between COM0 and SEG1 does not reach  $V_{DD}$  in the same phase, SEG1 is turn OFF. In this way, 7 segments can be displayed by combining the COM and SEG waveforms.

## LCD controller overview

## 2.3 Initial configuration

This section describes the initialization of the generator to operate the LCD controller.

**Figure 3** shows an example flow to initialize the generator.



**Figure 3 Example flow for generator initialization**

The LCD controller and output ports remain in the default state when the controller is disabled or in the reset state. The procedure to start the generator is as follows:

1. Enable clock (CLK\_PERI or CLK\_LF).
2. Configure the LCDx\_CONTROL register before enabling the generator.
3. Enable the high-speed generator or low-speed generator.

In addition, do the following to switch generators:

1. Disable the high-speed or low-speed generator without changing any configuration in the LCDx\_CONTROL register.
2. To disable the low-speed generator, wait for LCDx\_CONTROL.LS\_EN\_STAT to be cleared by hardware before next step. The low-speed generator clock must be present.
3. Configure the clock.
4. Change the LCDx\_CONTROL register to switch the generator.

## Use case

### 3 Use case

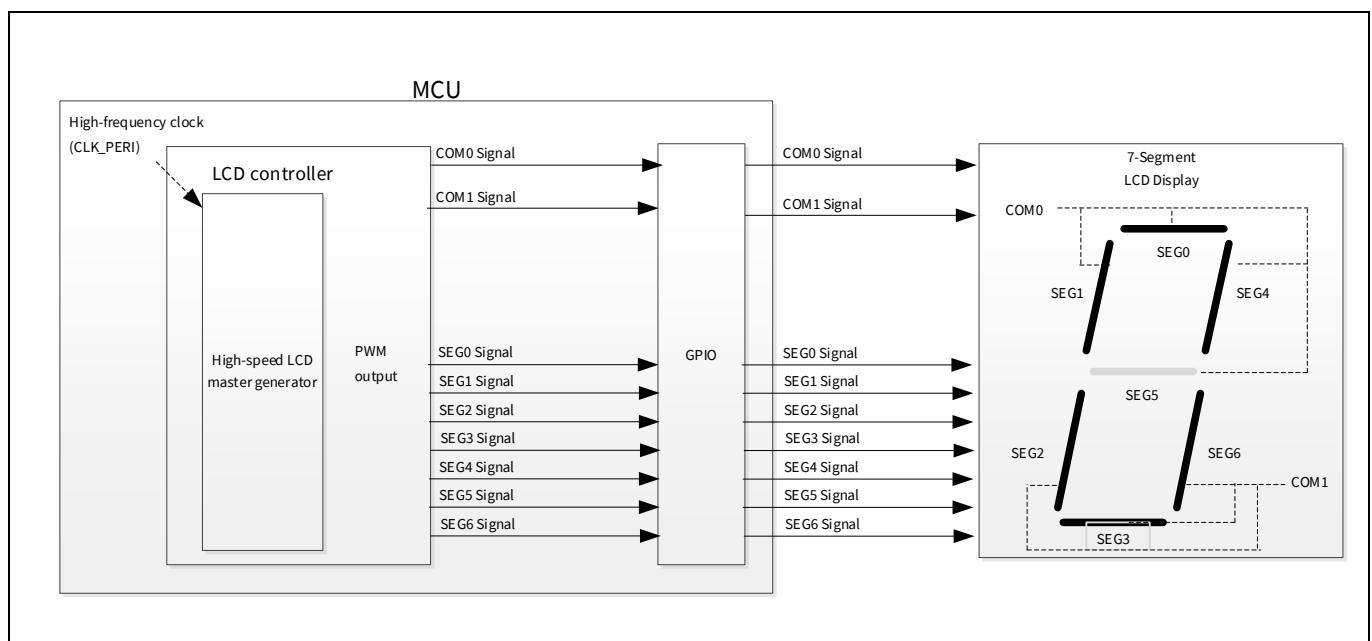
#### 3.1 LCD controller use case

This use case shows an example of using an LCD controller to display numbers on a 7-segment LCD. This use case is implemented based on the following settings.

- 7 segments (SEG0-6) and two commons (COM0/1) and display "0"
- High speed generator
- Type A drive waveform
- PWM drive mode at 1/2 bias

First, enable the generator. The generator uses the high-speed LCD master generator (see 2.3). The generator outputs PWM waveform signals to each COM and SEG based on the PMW mode setting. Each COM, and SEG of 7 segments are connected as shown in [Figure 4](#).

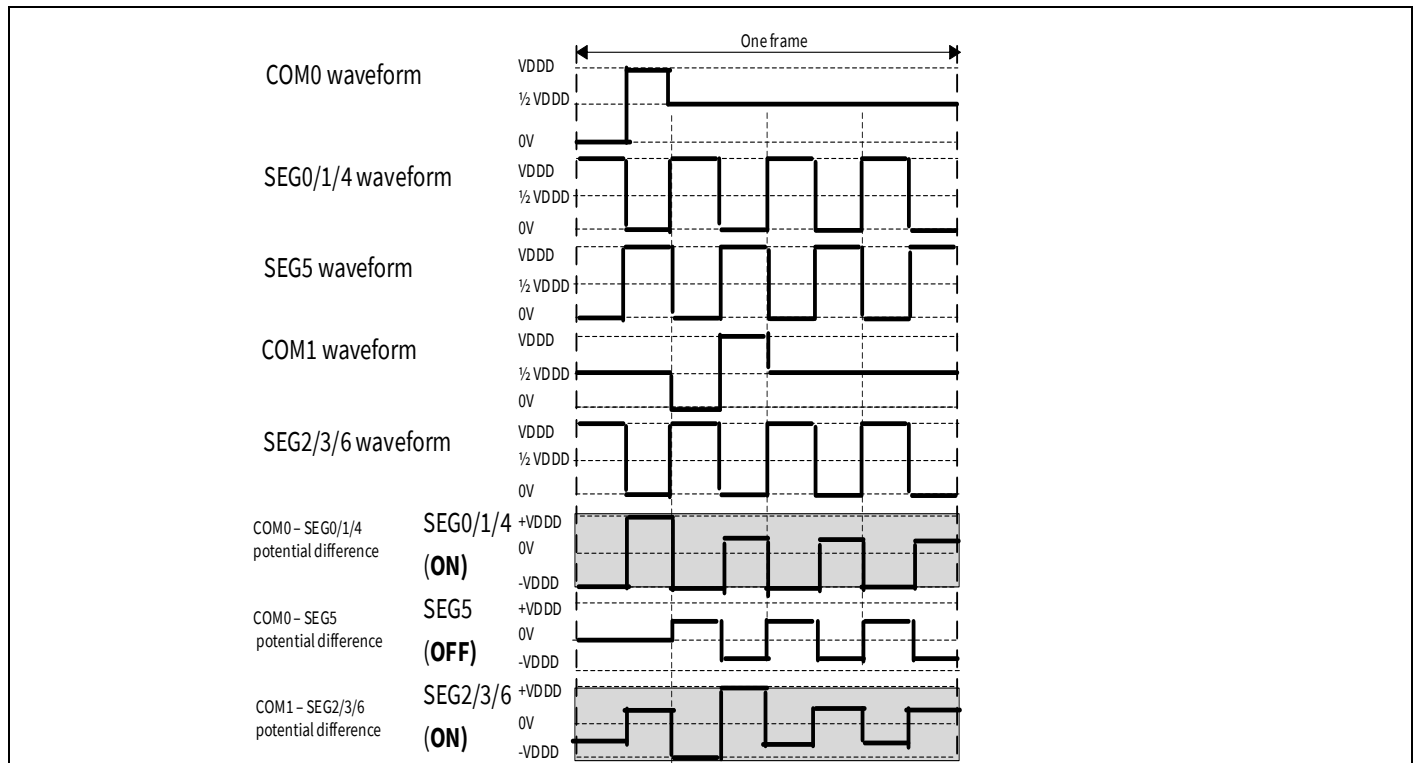
For example, this 7-segment SEG0 display is turned ON or OFF from the potential difference of the same phase of the PWM waveform signals in COM0 and SEG0 (see [Figure 2](#)).



**Figure 4** LCD controller use case block diagram

[Figure 5](#) shows simplified the relationship between COM0/1, and SEG0-6 for displaying number '0' on a 7-segment LCD.

## Use case



**Figure 5 Relationship between COM0/1 and SEG0-6 turn on display**

In this description, SEG refers to each display part such as SEG0, SEG1, etc. The segment shows whole COM and SEG.

First, to display '0', turn ON SEG0, SEG1, SEG2, SEG3, SEG4, and SEG6 in shown [Figure 4](#). SEG0, SEG1, and SEG4 have the same set of configurations. SEG2, SEG3, and SEG6 are connected to COM1. The combination is as shown in [Figure 4](#).

These segments SEG0, SEG1, SEG2, SEG3, SEG4, SEG6 have reached VDD in the potential difference waveform. Therefore, SEG0, SEG1, SEG2, SEG3, SEG4, SEG6 are turned ON.

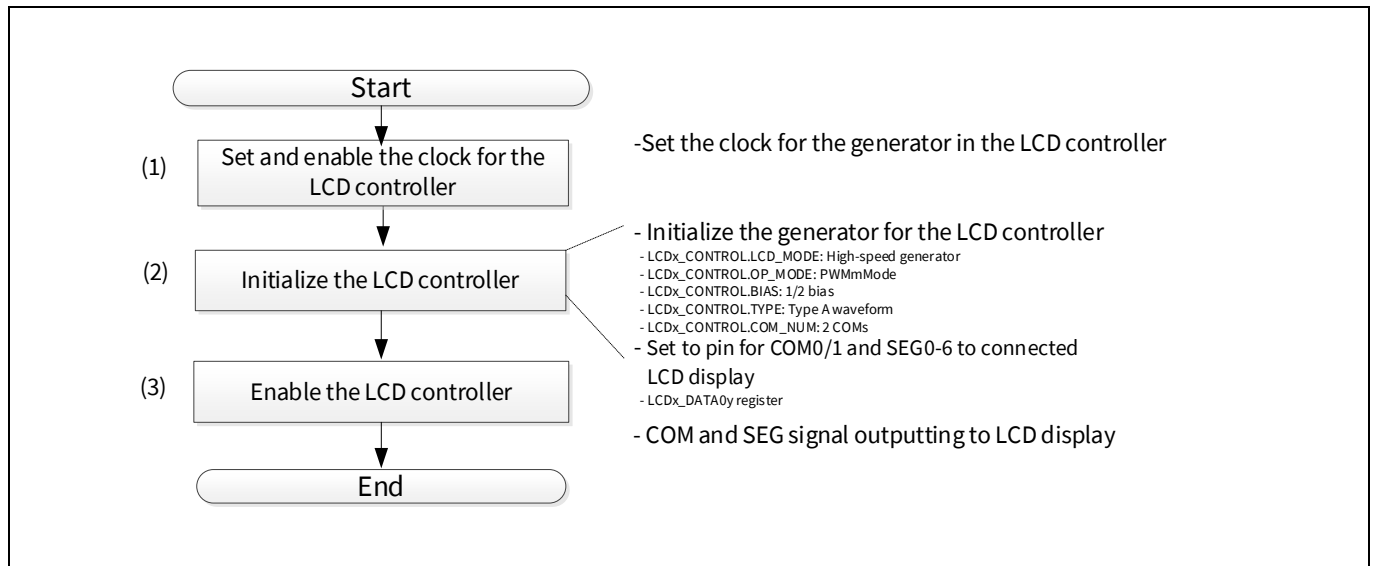
In addition, turn OFF SEG5. SEG5 is connected to COM0.

SEG5 has not reached VDD in the potential difference waveform. Therefore, it is turned OFF.

COM0/1 and SEG0-6 waveforms in the figure are output by configuring the PWM mode as 1/2 bias and setting the Type A waveform with the LCDx\_CONTROL register.

[Figure 6](#) shows a flowchart of this use case.

## Use case



**Figure 6 LCD controller use case flowchart**

1. Set the clock for the high-speed generator from the CLK\_PERI source and enable the clock.
2. Initialize the LCD controller. Set the basic drive mode as shown in [Figure 6](#), and then set the pins to assign COM0/1 and SEG0-6 in the register.
3. Enable the generator in LCD controller operation. These COM and SEG signals are output to the LCD display.



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**Glossary****4 Glossary****Table 1 Glossary**

| <b>Terms</b> | <b>Description</b>   |
|--------------|--|
| COM/SEG      | COM and SEG are two electrodes to drive an LCD display. The COM repeats the same common waveform. The SEG is set based on user specifications for display. |
| CPU          | Central processing unit  |
| CPUSS        | CPU subsystem  |
| LCD          | Liquid crystal display. See the “LCD controller” chapter of the <a href="#">architecture TRM</a> for details.  |
| MCU          | Microcontroller unit   |
| PWM          | Pulse width modulation   |

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## Related documents

### 5 Related documents

The following are the TRAVEO™ T2G family series datasheets and technical reference manuals. Contact [Technical Support](#) to obtain these documents.

- Device datasheet
  - CYT2CL datasheet 32-bit Arm® Cortex®-M4F microcontroller TRAVEO™ T2G family (Doc No. 002- 32508)
- Architecture technical reference manual (TRM)
  - TRAVEO™ T2G automotive cluster entry family architecture technical reference manual (TRM) (Doc No. 002-33175)
- Registers technical reference manual (TRM)
  - TRAVEO™ T2G automotive cluster entry registers technical reference manual (TRM) (Doc No. 002-33404)

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## Revision history

### Revision history

| Document version | Date of release | Description of changes |
|------------------|-----------------|------------------------|
| **               | 2021-12-13      | New application note.  |

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