# Comparison of TRAVEO™ T1G and TRAVEO™ T2G

## About this document

### Scope and purpose

AN218629 compares MCUs of the TRAVEO™ T1G family with MCUs of the TRAVEO™ T2G Family CYT2/CYT3/CYT4 series.

### Associated Part Family

TRAVEO™ T1G Family, TRAVEO™ T2G Family

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# 1 Introduction

This application note compares TRAVEO™ T1G Family MCUs with TRAVEO™ T2G Family MCUs. Both TRAVEO™ T1G and TRAVEO™ T2G families are manufactured in 40-nm CMOS technology with embedded flash.

Several global system configurations are different between these two product families. While several resources have been enhanced, downward compatibility is maintained.

This application note consists of two main sections: one for automotive body segment, and the other for automotive cluster segment. The Body Entry/High Products section compares body products, while the Cluster Products section compares cluster products. The product lineup is listed in Table 1.

**Table 1 MCU List for Comparison**

| Products | TRAVEO™ T1G Family | TRAVEO™ T2G Family |
|---|---|---|
| Body Entry/High Products | S6J3428, S6J3429, and S6J342A Series | CYT2B7, CYT2B9, and CYT4BF Series |
| Cluster Products | S6J3200 Series | CYT4DN and CYT2C9 Series |

# 2 Body Entry/High Products

## 2.1 TRAVEO™ T2G Family MCU Features

**Table 2 Features of TRAVEO™ T2G Family MCUs**

| Function | CYT2B7 Series | CYT2B9 Series | CYT4BF Series |
|---|---|---|---|
| Flash Memory (Code Flash) | Up to 1088 KB | 2112 KB | 8256 KB |
| Flash Memory (Work Flash) | Up to 96 KB | 128 KB | 512 KB |
| SRAM0 | Up to 64 KB | 128 KB | 512 KB |
| SRAM1 | Up to 64 KB | 128 KB | 512 KB |
| CXPI | Not Supported | Supported | Not Supported |
| FlexRay | Not Supported | Not Supported | Supported |
| Secure Digital High Capacity (SDHC) Host Controller | Not Supported | Not Supported | Supported |
| Serial Memory Interface | Not Supported | Not Supported | Supported |
| Ethernet | Not Supported | Not Supported | Supported |

## 2.2 Product Overview

TRAVEO™ T2G Family is a family of 32-bit MCUs based on the high-performance Arm® Cortex®-M series of CPUs, as Figure 1 shows, intended for automotive body-control applications.

The Cortex-M4 processor is the main CPU designed for a short interrupt response time, high code density, and high 32-bit throughput while maintaining a strict cost and power consumption budget. A secondary Cortex-M0+ based CPU can implement security, safety, and protection features. Note that the CYT4BF series uses two Cortex-M7 processors for primary processing.

Figure 1 through Figure 3 show the major architecture components of the CYT2B7 series, CYT2B9 series, and CYT4BF series. There are four major subsystems: CPU subsystem, system resources, peripheral blocks, and I/O subsystem.

## 2 Body Entry/High Products

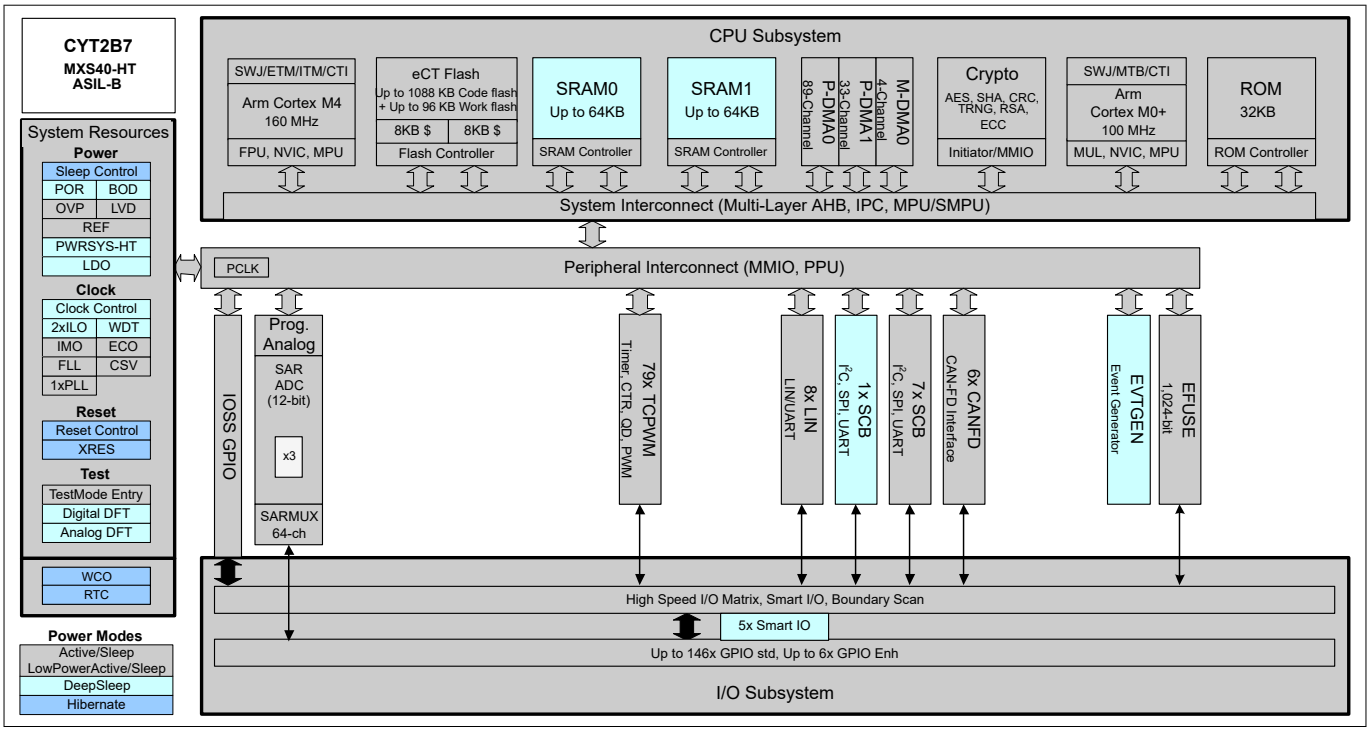


**Figure 1 Block Diagram (CYT2B7 Series)**

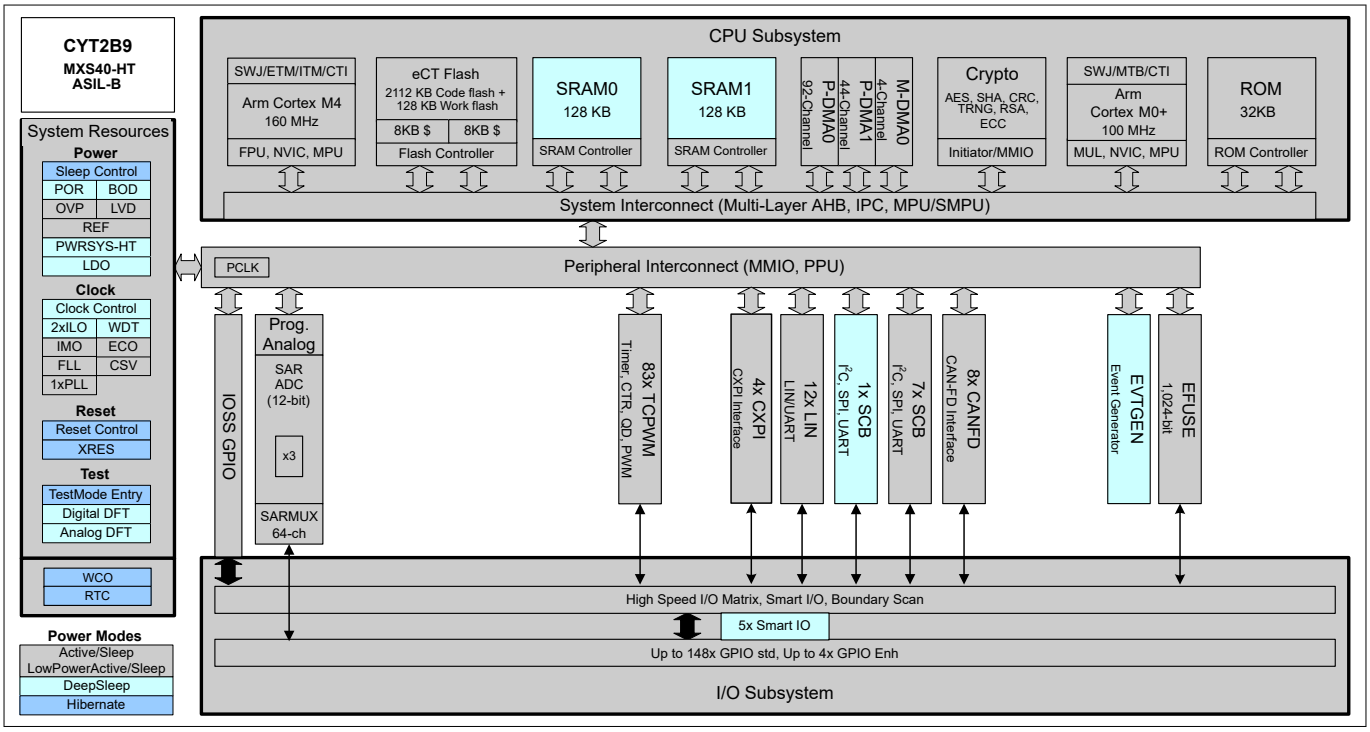


**Figure 2 Block Diagram (CYT2B9 Series)**

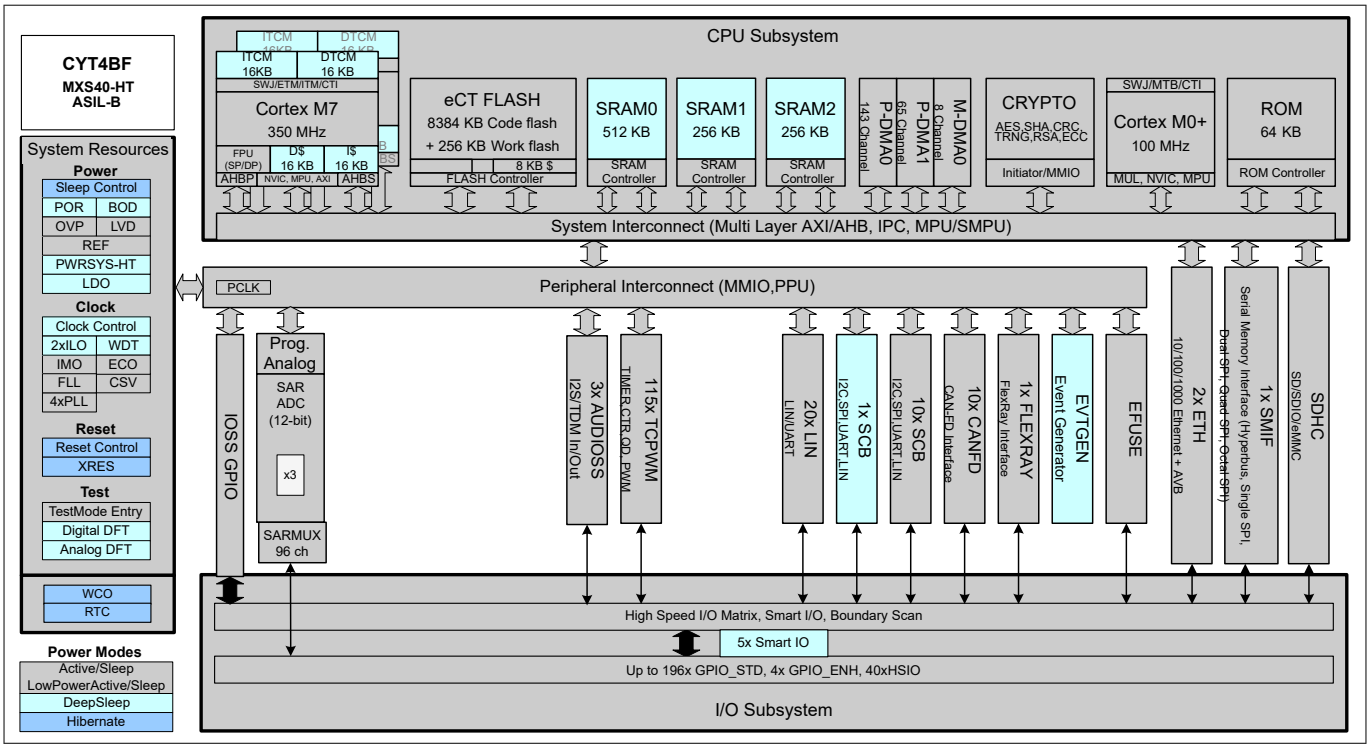


**Figure 3 Block Diagram (CYT4BF Series)**

## 2.3 On-chip System Features

### 2.3.1 CPU

Both TRAVEO™ T1G and TRAVEO™ T2G Family are based on 32-bit Arm Cortex processors.

TRAVEO™ T1G Family has a single Cortex-R5 processor, while TRAVEO™ T2G Family is a dual-CPU with Cortex-M4 and Cortex-M0+ processors. In TRAVEO™ T2G, two CPUs are configured as the CPU subsystem; Cortex-M4 or Cortex-M7 processor is the main CPU and Cortex-M0+ processor is the secondary CPU that can implement security, safety, and protection features. Note that as the CPU core changes, MCU features change according to the core specification.

**Table 3 Differences in CPU**

| Item | TRAVEO™ T1G Family | TRAVEO™ T2G Family | | | Remarks |
|---|---|---|---|---|---|
| | | Main CPU | | Secondary CPU | |
| | | CYT2B7/B9 Series | CYT4BF Series | | |
| CPU Core | Cortex-R5F | Cortex-M4 | Cortex-M7 (x2) | Cortex-M0+ | |
| Operation Frequency | Up to 132 MHz | Up to 160 MHz | Up to 350 MHz | Up to 100 MHz | Product specifications |
| FPU | Single/Double precision | Single precision | Single/Double precision | None | |
| MPU | 16 regions | 8 regions | 16 regions | 8 regions | 1) |

**(table continues...)**

1 TRAVEO™ T2G family has SMPU as memory protection in addition to the CPU's internal MPU. Refer to Protection.

**Table 3 (continued) Differences in CPU**

| Item | TRAVEO™ T1G Family | TRAVEO™ T2G Family | | | Remarks |
|---|---|---|---|---|---|
| | | Main CPU | | Secondary CPU | |
| | | CYT2B7/B9 Series | CYT4BF Series | | |
| Cache Memory | I-cache 16 KB / D-cache 16 KB | None | I-cache 16 KB / D-cache 16 KB | None | |
| TCM Interface | Supported<br>Implemented TCRAM | Not supported | Supported (ITCM, DTCM) | Not supported | |
| Support for Interrupt Controller | Vector Interrupt Controller (VIC) | Nested Vector Interrupt Controller (NVIC) | | | |

## 2.3.2 Memory Design

Table 4 lists the Code Flash features. The main differences are in program size, Read-While-Write operation, and redundancy.

**Table 4 Differences in Code Flash**

| Code Flash | S6J3428/9/A Series | CYT2B7/B9, CYT4BF Series |
|---|---|---|
| ECC | SEC/DED | SEC/DED |
| Sector Size | 32 KB, 8 KB | 32 KB, 8 KB |
| Program Size | 32 bits, 64 bits, 256 bits | 64 bits, 256 bits, 4096 bits |
| Program and Erase Cycles/Retention | 1000/20 years | 1000/20 years |
| Read-While-Write Operation | Not supported | Supported |

Table 5 lists the Work Flash features. The main differences are in the sector size, program and erase cycles, Read-While-Write operation, and redundancy. When compared to TRAVEO, TRAVEO™ T2G families support smaller sector size and higher program and erase cycles.

**Table 5 Differences in Work Flash**

| Work Flash | S6J3428/9/A Series | CYT2B7/B9, CYT4BF Series |
|---|---|---|
| ECC | SEC/DED | SEC/DED |
| Sector Size | 4 KB | 2 KB, 128 B |
| Program Size | 32 bits | 32 bits |
| Program and Erase Cycles/Retention | 1000/20 years<br>10000/10 years<br>100000/5 years | 125000/20 years<br>250000/10 years |
| Read-While-Write Operation | Not supported | Supported |

Table 6 lists the SRAM features. The main difference is the data retention in low power mode. TRAVEO™ T2G Family supports data retention in DeepSleep mode.

**Table 6 Differences in SRAM**

| SRAM | S6J3428/9/A Series | CYT2B7/B9, CYT4BF Series |
|---|---|---|
| ECC | SEC/DED | SEC/DED |
| Data Retention in Low Power Mode | Not supported<br>(TCRAM and SRAM are not retained in Shutdown mode. Backup RAM is retained in Shutdown mode) | Supported<br>(SRAM is retained in DeepSleep mode) |

### 2.3.3 Debug

TRAVEO™ T1G and TRAVEO™ T2G families support JTAG and SWD Debug Interface. Table 7 shows the main differences in debugging.

**Table 7 Differences in Debugging**

| Item | S6J3428/9/A Series | CYT2B7/B9, CYT4BF Series |
|---|---|---|
| Debug interface | JTAG<br>SWD | JTAG<br>SWD |

### 2.3.4 Mode Setting

TRAVEO™ T2G Family does not support the serial programming mode; therefore, there is no mode pin in TRAVEO™ T2G Family. When the debugger is connected to JTAG, TRAVEO™ T2G Family transitions to Debug mode and enables programming to flash.

**Table 8 Differences in Mode Setting**

| Item | S6J3428/9/A Series | CYT2B7/B9, CYT4BF Series |
|---|---|---|
| Normal Mode | Setting by mode pin<br>• User Mode | Debugger is not connected (SWD or JTAG)<br>• Boot mode/user mode/trusted mode<br>• Life cycle stage (Secure) |
| Board mode | Setting by mode pin<br>• Serial programming mode<br>• Parallel programming mode | Debugger is connected (SWD or JTAG)<br>• Debug mode<br>• Life cycle stage (Normal_Provisioned /Secure/ Secure_With_Debug/RMA/Corrupted) |

### 2.3.5 Power Supply and Monitoring

The power supply of TRAVEO™ T2G Family is the same as that of TRAVEO™ T1G Family, but signal names of power supply are different. Also, the type of power monitoring mode has been enhanced in TRAVEO™ T2G Family.

#### 2.3.5.1 Power Supply

Table 9 lists the power supply and differences in functionality.

**Table 9 Power Supply**

| Power Supply | | S6J3428/9/A Series | | CYT2B7/B9, CYT4BF Series | |
|---|---|---|---|---|---|
| External | Digital | $V_{CC}$ | 2.7 to 5.5 V | $V_{DDD}$ | 2.7 to 5.5 V |
| | I/O | | | $V_{DD\ IO\_1/2}$ | 2.7 to 5.5 V |
| | | | | $V_{DD\ IO\_3/4}$ | 2.7 to 3.6 V (only for CYT4BF series) |
| | Analog | AVCC0/1 | 2.7 to 5.5 V | $V_{DD\ A}$ | 2.7 to 5.5 V |
| Internal | | C | 1.2 V | $V_{CCD}$ | 1.1 V<br>$V_{CCD}$ of CYT4BF can be also external power supply (typical 1.15 V when $V_{CCD}$ is external power supply) |

### 2.3.5.2 Monitoring

Table 10 lists the differences in voltage between TRAVEO™ T1G and TRAVEO™ T2G families.

**Table 10 Voltage Monitoring**

| Monitoring | S6J3428/9/A Series | CYT2B7/B9, CYT4BF Series |
|---|---|---|
| Voltage Monitoring | • Power-on reset (POR)<br>• LVD | • POR<br>• LVD<br>• Brownout detection (BOD)<br>• Overvoltage detection (OVD)<br>• Overcurrent detection (OCD) |

## 2.3.6 Reset Factor

Note that all resets in TRAVEO™ T2G Family are asynchronous resets. This difference is because the reset factor is optimized according to the TRAVEO™ T2G system. If you need the RAM retention Reset, see the Architecture Technical Reference Manual (TRM). Table 11 lists the main differences in Reset Factor.

**Table 11 Differences in Reset Factors**

| Reset Sources | S6J3428/9/A Series | CY2B7/B9, CYT4BF Series | Remarks |
|---|---|---|---|
| POR | Yes | Yes | |
| BOD Reset | • External LVD Reset<br>• Internal LVD Reset<br>• RAM retention LVD Reset | • External voltage BOD Reset[2)]<br>• Internal voltage BOD Reset[3)]<br>• Analog input voltage BOD Reset[3), 4)] | |

**(table continues...)**

2 Programmable Trip point (2 points)
3 Fixed Trip point
4 Reset or Fault report can be selected

**Table 11 (continued) Differences in Reset Factors**

| Reset Sources | S6J3428/9/A Series | CY2B7/B9, CYT4BF Series | Remarks |
|---|---|---|---|
| OVD Reset | No | • External voltage OVD Reset[3)]<br>• Internal voltage OVD Reset[4)]<br>• Analog input voltage OVD Reset[3),4)] | |
| OCD Reset | No | Internal voltage OCD Reset[4)] | |
| External Reset | RSTX pin | XRES_L pin | |
| Clock Stop Wait Timeout Reset | Yes | No, does not support synchronous reset | |
| Illegal Mode Detection Reset | Yes | No, does not have MD pin | |
| Profile Error Reset | Yes | No, does not support Profile setting | |
| Watchdog Timer (WDT) Reset | • Hardware WDT Reset<br>• Software WDT Reset | • WDT Reset<br>• Multi-Counter WDT Reset | See Watchdog Timer |
| Internal System (Software) Reset | • Software Reset<br>• Software trigger hard Reset | • Software Reset | |
| Fault Detection Reset | No | Yes: via Fault report | |
| Clock Supervision (CSV) Reset | • Main Clock CSV Reset<br>• Sub Clock CSV Reset<br>• PLL Clock CSV Reset<br>• SSCG Clock CSV Reset<br>• Fast CR CSV Reset<br>• Slow CR CSV Reset | • CLK_REF CSV Reset<br>• ILO0 CSV Reset<br>• CLK_HF CSV Reset<br>• CLK_LF CSV Reset | |
| Wakeup Reset | Yes (Power Domain Reset) | Yes (Hibernate Wake up Reset) | |
| Debugger Reset | • TRSTX<br>• Software Reset | • NTRST<br>• Software Reset | |

### 2.3.7 Clock System

Compared to TRAVEO™ T1G Family clock system, TRAVEO™ T2G Family (only CYT4B Series) has Spread Spectrum Clock Generator functions. In TRAVEO™ T2G Family, frequency-locked loop (FLL) featuring fast startup and low power is implemented. Table 12 lists the main differences in clock system.

See the datasheet for the AC characteristics of each clock.

3 Fixed Trip point
4 Reset or Fault report can be selected

**Table 12 Differences in Clock System**

| Clock System | | TRAVEO™ T1G Family(S6J3428/9/A Series) | TRAVEO™ T2G Family(CYT2B Series) | TRAVEO™ T2G Family(CYT4B Series) |
|---|---|---|---|---|
| Internal Clock Source | | Fast CR: 4 MHz<br>(Using source clock after reset)<br>Slow CR: 100 kHz | IMO: 8 MHz<br>(Using source clock after reset)<br>ILO0/1: 32 kHz | |
| External Clock Source | | Main clock: 3.6 to 16 MHz<br>Sub clock: 32.768 kHz | ECO: 3.988 to 33.33 MHz<br>WCO: 32.768 kHz<br>EXT_CLK[5] : 0.25 to 100 MHz | |
| High-Speed Clock Generation | PLL | PLL x1<br>Input: 3.6 to 17.6 MHz<br>Output: 200 to 320 MHz<br>SSCG PLL x1<br>Input: 3.6 to 32MHz<br>Output:200 up to 320 MHz | PLL x1<br>Input: 3.988 to 33.34 MHz<br>Output: 11 to 160 MHz<br>SSCG not supported | PLL without SSCG x2<br>Input: 3.988 to 33.34 MHz<br>Output: 11 to 200 MHz<br>PLL with SSCG x2<br>Input: 3.988 to 33.34 MHz<br>Output: 25 to 400 MHz |
| | FLL | Not implemented | FLL x1<br>Input: 0.25 to 80 MHz<br>Output: 24 to 100 MHz | FLL x1<br>Input: 0.25 to 80 MHz<br>Output: 24 to 100 MHz |
| Clock Gear | | Supported | Not implemented | |
| Clock Supervision | | Main clock<br>Sub clock<br>PLL clock<br>SSCG clock<br>Slow CR<br>Fast CR | CLK_REF (IMO or ECO or EXT_CLK)<br>CLK_HF (PLL and FLL)<br>ILO0<br>CLK_LF (ILO1 or WCO) | |

## 2.3.8 Watchdog Timer

Table 13 lists the watchdog timer (hardware) features. The main differences are counter clock, maximum timeout, and the behavior during low-power mode and debugging.

**Table 13 Differences in Watchdog Timer (Hardware)**

| Watchdog Timer (Hardware) | S6J3428/9/A Series | CY2B7/B9, CYT4BF Series |
|---|---|---|
| Trigger | Reset | Reset |
| Counter Clock | • Fast internal clock: 4 MHz<br>• Slow internal clock: 100 kHz | • Internal low speed oscillator: 32 kHz |
| Counter | 32 bits | 32 bits |

**(table continues...)**

5 It can be sourced from a designated I/O pin

**Table 13 (continued) Differences in Watchdog Timer (Hardware)**

| Watchdog Timer (Hardware) | S6J3428/9/A Series | CY2B7/B9, CYT4BF Series |
|---|---|---|
| Maximum Timeout | 12 hours | 38.33 hours |
| Window Function | Supported | Supported |
| Warning Interrupt | Supported | Supported |
| Timeout Expiration Action | Reset or nonmaskable interrupt (NMI) | Reset |
| Behavior During Low-Power Mode | Stop | Register can select stop or run |
| Behavior During Debugging | Stop at debugging state | Register can select stop or run |

Table 14 lists the multi-counter watchdog timer (software) features. The main differences are counter clock, counter, maximum timeout, and the behavior during debugging.

**Table 14 Differences in Multi-Counter Watchdog Timer (Software)**

| Multi-counter Watchdog Timer (Software) | S6J3428/9/A Series | CY2B7/B9, CYT4BF Series |
|---|---|---|
| Trigger | User program | User program |
| Counter Clock | • Fast internal clock: 4 MHz<br>• Slow internal clock: 100 kHz<br>• Main clock: 4 to 16 MHz<br>• Sub clock: 32 kHz | • Internal low-speed oscillator: 32 kHz<br>• Watch crystal oscillator: 32 kHz |
| Counter | 32 bits | 2 * 16-bit, 32 bits only for interrupt |
| Maximum Timeout | 36.4 hours | 2.11 seconds |
| Window Function | Supported | Supported |
| Warning Interrupt | Supported | Supported |
| Timeout Expiration Action | Reset or NMI | Reset or Fault |
| Behavior During Low-Power Mode | Register can select stop or run. | Register can select stop or run. |
| Behavior During Debugging | Stop at debugging state | Register can select stop or run. |

## 2.3.9 Low-Power Mode

Table 15 lists the low-power modes. TRAVEO™ T2G Family supports almost all low-power modes with DeepSleep mode.

**Table 15 Differences of Low-Power Modes**

| Low Power Mode | S6J3428/9/A Series | CY2B7/B9, CYT4BF Series |
|---|---|---|
| Sleep<br>• CPU: Halt<br>• Peripheral: Active<br>• SRAM retention | Supported: Sleep<br>• TCRAM/SRAM/Backup RAM retention | Supported: Sleep<br>• SRAM retention |

**(table continues...)**

**Table 15 (continued) Differences of Low-Power Modes**

| Low Power Mode | S6J3428/9/A Series | CY2B7/B9, CYT4BF Series |
|---|---|---|
| Timer<br>• CPU: Halt<br>• Peripheral: Halt except RTC, GPIO<br>• SRAM retention | Supported: Timer<br>• TCRAM/SRAM/Backup RAM retention | Supported: DeepSleep<br>• Peripheral: OFF except RTC, Event generator, GPIO<br>• SRAM retention |
| Stop<br>• CPU: Halt<br>• Peripheral: Halt except GPIO<br>• SRAM retention | Supported: Stop<br>• TCRAM/SRAM/Backup RAM retention | Supported: DeepSleep<br>• Peripheral: OFF except RTC, Event generator, GPIO<br>• SRAM retention |
| Partial wakeup (Shutdown)<br>• CPU: OFF<br>• Peripheral: OFF except RTC, ADC, GPIO<br>• Partial RAM retention | Supported: Partial wakeup<br>• ADC is triggered by RTC<br>• Backup RAM retention | Supported: DeepSleep<br>• Peripheral: OFF except RTC, Event generator, GPIO<br>• ADC and LIN are triggered by Event generator<br>• SRAM retention (Full/Partial) |
| Timer (Shutdown)<br>• CPU: OFF<br>• Peripheral: OFF except RTC, GPIO<br>• Partial RAM retention | Supported: Timer (Shutdown)<br>• Backup RAM retention | Supported: DeepSleep<br>• Peripheral: OFF except RTC, Event generator, GPIO<br>• SRAM retention (Full/Partial) |
| Stop (Shutdown)<br>• CPU: OFF<br>• Peripheral: OFF except GPIO<br>• Partial RAM retention | Supported: Stop (Shutdown)<br>• Backup RAM retention | Supported: DeepSleep<br>• SRAM retention (Full/Partial) |

### 2.3.10 Interrupt Structure

The interrupt structure of TRAVEO™ T1G and TRAVEO™ T2G families differ based on the CPU. TRAVEO™ T1G Family (Cortex-R5) interrupt controller used vector interrupt controller (VIC), while TRAVEO™ T2G Family (Cortex-M4//M7/M0+) uses nested vector interrupt controller (NVIC). Table 16 lists the main differences in interrupt structure.

TRAVEO™ T1G Family controls system interrupts such as enable/disable, levels, and level masks with an external interrupt controller. Each CPU of TRAVEO™ T2G Family has eight interrupt inputs, and controls interrupts within the CPU, thereby performing high-speed interrupt processing.

TRAVEO™ T2G Family uses up to 1023 system interrupts assigned to eight groups. All interrupts within a group has the same priority. Four of the 1023 system interrupts can be assigned as NMI.

TRAVEO™ T2G Family implements wakeup interrupt controller (WIC), which enables interrupt detection for CPU wakeup in DeepSleep power mode.

**Table 16 Differences of Interrupt Structure**

| Item | S6J3428/9/A Series | CY2B7/B9, CYT4BF Series | | Remarks |
|---|---|---|---|---|
| CPU core | Cortex-R5F | Cortex-M4/M7 | Cortex-M0+ | |
| Supported Interrupt Controller in CPU | VIC | NVIC | | |
| Number of IRQ inputs of CPU | 1 | 8 | 8 | |
| Number of NMI Inputs of CPU | 1 | 1 | 1 | |
| Priority Level | Interrupt: 32 levels<br>NMI: 16 levels | Interrupt: 8 levels NMI: None | Interrupt: 4 levels NMI: None | |
| Number of System Interrupts | Up to 512 | Up to 1023 | | 6) |
| Vector Address | Assigned for each system interrupt | Assigned for each IRQ input.<br>Multiple system interrupts share a CPU interrupt handler as provided by the VTOR table. | | |
| WIC | Not Supported | Supported | | |

## 2.3.11 Data Transfer

For data transfer, TRAVEO™ T2G Family has two types of DMA with different purposes: Peripheral DMA (P-DMA) and Memory DMA (M-DMA). Table 17 lists the main differences in data transfer.

P-DMA focuses on achieving low latency for a large number of channels. P-DMA has a single data transfer engine that is shared by all channels.

M-DMA focuses on achieving high memory bandwidth for a small number of channels. M-DMA has a dedicated data transfer engine for each channel.

The DMA transfer specification of TRAVEO™ T1G Family is set by the register. In TRAVEO™ T2G Family, transfer is specified by the descriptor in SRAM. P/M-DMA of TRAVEO™ T2G Family can perform transfer chaining with descriptor setting.

**Table 17 Differences of Data Transfer**

| Item | S6J3428/9/A Series | CY2B7/B9, CYT4BF Series | | Remarks |
|---|---|---|---|---|
| Function Name | DMAC | P-DMA | M-DMA | |
| Data Transfer Specifics | Register | Descriptor in memory | | |
| Data Size | 8-/16-/32-/64-bit | 8-/16-/32-bit | | |

**(table continues...)**

6 System Interrupts are interrupts generated from peripheral functions and external inputs. For the list of system interrupts supported by the device variants, see the following documents:

- TRAVEO™ T1G Family: Hardware Manual by the device variants.
- TRAVEO™ T2G Family: Architecture Technical Reference Manual by the device variants.

**Table 17 (continued) Differences of Data Transfer**

| Item | S6J3428/9/A Series | CY2B7/B9, CYT4BF Series | | Remarks |
|---|---|---|---|---|
| Transfer Mode | • Single<br>• Block<br>• Burst | • Single<br>• 1D/2D<br>• CRC transfer<br>• Descriptor chaining | • Single<br>• 1D/2D<br>• Memory copy<br>• Scatter<br>• Descriptor chaining | |
| Activation Trigger | • Hardware<br>• Software | • Hardware<br>• Software<br>• Transfer completion trigger output | • Software<br>• Transfer completion trigger output | |
| Channel Arbitration Schemes | • Fixed<br>• Dynamic<br>• Round robin | • Fixed four levels<br>• Round-robin in the same priority group | | |
| Interrupt Generation | • Transfer Completion<br>• Error occurrence | • Transfer completion<br>• Error occurrence | | |
| Protection Schemes | Dedicated MPU<br>• Access range<br>• User/Privilege<br>• Read/Write | SMPU and PPU<br>• Access range<br>• User/Privileged<br>• Read/Write<br>• Secure/Non-secure<br>• Protection Contexts | | See Protection. |

## 2.3.12 TPU

TRAVEO™ T1G Family has a dedicated timer for timing protection (TPU). However, TRAVEO™ T2G Family does not have a dedicated timer. TRAVEO™ T2G Family uses a TCPWM timer for timing protection.

The TCPWM timer is a general-purpose timer that can generate interrupts for overflow, underflow, and compare matches. This interrupt can be implemented as NMI, which can provide the TPU function. Figure 4 shows the configuration of the TPU and Figure 5 shows an example of the operation.

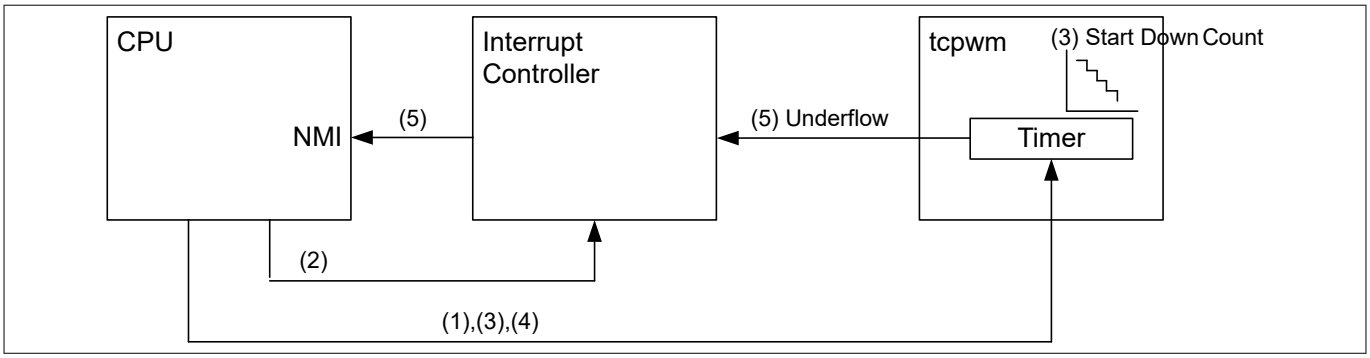


**Figure 4 Timing Protection Implementation Example**

1. Configure the TCPWM initial values (for example, using DownCount mode), and set the upper limit of the measurement time as the initial time.
2. Set the TCPWM interrupt to NMI.
3. Software starts the timer at the start point of the measurement process.
4. Software stops the timer at the end point of the measurement process.
5. If the counter under-flowed before the software stops the timer, the Underflow interrupt of the TCPWM is notified as an NMI to the CPU via the interrupt controller.

*Note: The interrupt controller can notify the system interrupt as NMI, including the TCPWM interrupt.*

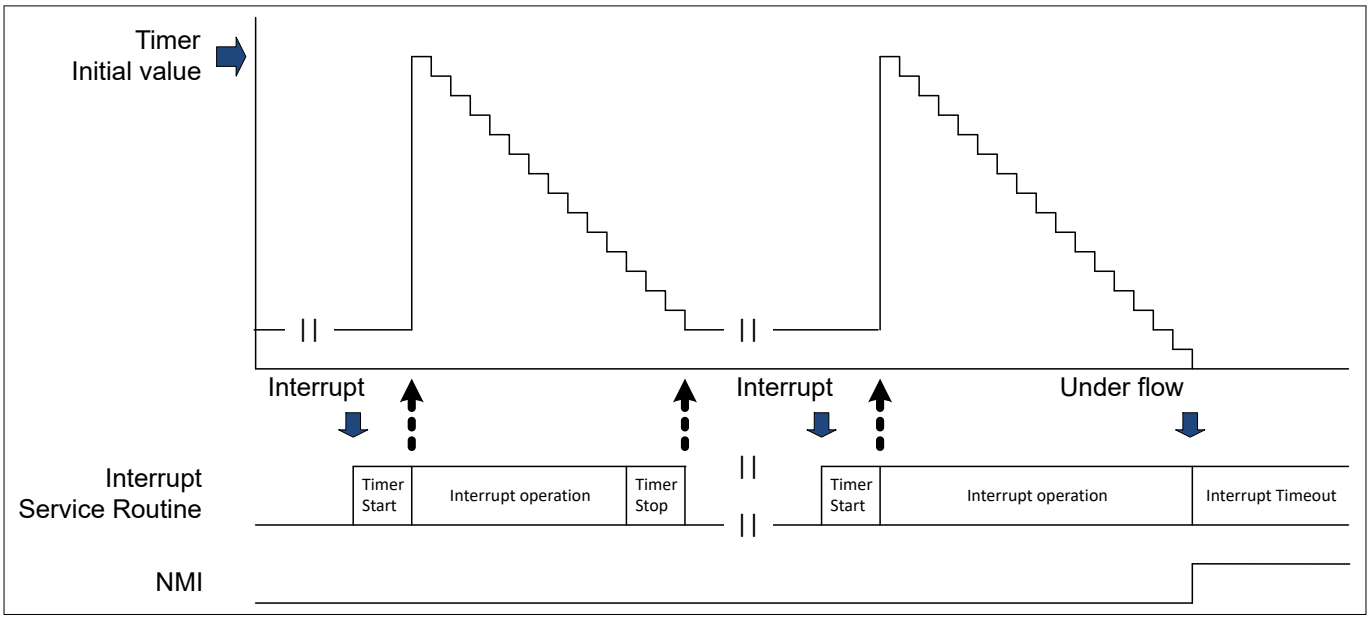


**Figure 5 Timing Protection Example (Monitoring of the Interrupt Service Routine Operation Time)**

## 2.3.13 Fault Report

Fault report is a new feature of TRAVEO™ T2G Family. Figure 6 shows a block diagram of the Fault structure.

The centralization of faults by Fault report structures for a system-wide consistent handling of faults simplifies software development.

Fault report captures up to 96[7)] failures such as MPU/SMPU/PPU protection violations, SRAM controller ECC errors, peripheral-specific errors, and so on. When Fault report captures a fault, it generates a notification signal

such as fault interrupt, trigger output, external pin output, and fault reset request. Each of these output signals can be enabled or disabled.

The fault interrupt can be mapped to the CPU NMI as a system interrupt. In addition, Fault report provides the fault source and additional fault-specific information.

For more details, see the TRAVEO™ T2G Architecture Technical Reference Manual (TRM).

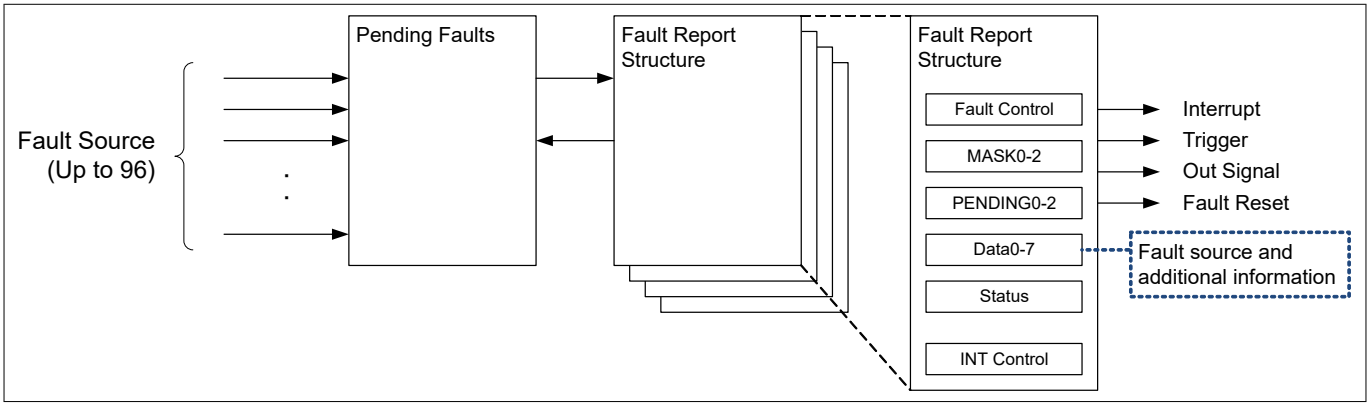


**Figure 6 Fault Structure**

## 2.3.14 Protection

The Protection function of TRAVEO™ T1G Family consists of the CPU's Memory Protection Unit (MPU), DMA's MPU, and Peripheral Protection Unit (PPU). TRAVEO™ T2G Family consists of MPU, Shared Memory Protection Unit (SMPU), and PPU. Table 18 lists the main differences in Protection Units.

In TRAVEO™ T2G Family, memory protection is provided by MPU and SMPU. MPU is implemented as part of the CPU and bus infrastructure. P-DMA, M-DMA, and encrypted components do not have MPU. Instead, they inherit the access control attributes of programmed bus transfer.

SMPU is shared by all masters; PPU is a protection unit for peripheral registers.

TRAVEO™ T2G Family supports a new protection attribute (Secure/Non-secure), and protection contexts. Protection contexts can change the access restriction without changing the setting of the protection unit.

For more details, see the Technical Reference Manual.

**Table 18 Differences in Protection Configuration and Access Attribute**

| Item | S6J3428/9/A Series | CY2B7/B9, CYT4BF Series | Remarks |
|---|---|---|---|
| MPU implemented in the CPU | Cortex-R5: 16 Regions<br>Access Attribute:<br>• Access Range<br>• Privileged/Unprivileged<br>• Read/Write<br>• Execute (Code or Data) | | |

**(table continues...)**

[7] For the list of system interrupts supported by the device variants, see the Technical Reference Manual.

**Table 18 (continued) Differences in Protection Configuration and Access Attribute**

| Item | S6J3428/9/A Series | CY2B7/B9, CYT4BF Series | Remarks |
|---|---|---|---|
| MPU implemented in the bus infrastructure | Not supported | 16 Regions<br>Access Attribute:<br>• Access Range<br>• Privileged/Unprivileged<br>• Read/Write<br>• Execute (Code or Data) | For external master such as debugger |
| SMPU | Not supported | 16 Regions<br>Access Attribute:<br>• Access Range<br>• Privileged/Unprivileged<br>• Read/Write<br>• Execute (Code or Data)<br>• Secure/Non-secure<br>• Protection Contexts | |
| PPU | Access Attribute:<br>• USER/Privilege<br>• Read/Write | Access Attribute:<br>• Access Range<br>• Privileged/Unprivileged<br>• Read/Write<br>• Execute (Code or Data)<br>• Secure/Non-secure<br>• Protection Contexts | |
| MPU16-AHB | Access Attribute:<br>• Access range<br>• USER/Privilege<br>• Read/Write | Not supported.<br>DMA access protection is provided by SMPU and PPU. | |

### 2.3.15 Boot Process

The boot process of both TRAVEO™ T1G and TRAVEO™ T2G families is executed after reset and before the application program starts. The boot process is executed by the Cortex-R5 processor in TRAVEO™ T1G Family, and is executed by the secure master (Cortex-M0+ processor) in TRAVEO™ T2G Family.

The boot process in TRAVEO™ T1G Family mainly executes based on the operation mode and the security setting that the debugger connection authenticates, secure boot processing, and hardware watchdog timer according to the flash marker.

In TRAVEO™ T2G Family, the boot process consists of ROM boot and flash boot. The ROM boot process determines the Protection State and validates the flash boot process. The flash boot process configures the protection unit such as SMPU and PPU, and verify the application program code in the flash memory. In addition, activates the boot loader.

For more details, see the Technical Reference Manual.

### 2.3.16 Security

Table 19 lists the security features. TRAVEO™ T2G Family supports lifecycle stages, device protection states, and Hardware Security Module (HSM).

**Table 19 Differences of Security**

| Security | S6J3428/9/A Series | CY2B7/B9, CYT4BF Series |
|---|---|---|
| Lifecycle stages<br>Device protection states | Not supported | Supported<br>• Lifecycle stages<br>• Protection states |
| Flash protection | Supported | Supported |
| Debugger security | Supported | Supported |
| Hardware-based encryption | Supported<br>Secure Hardware Extension (SHE) | Supported<br>Enhanced Secure Hardware Extension (eSHE) and HSM support are enabled by third-party firmware. |

## 2.4 Peripherals

### 2.4.1 Timer

The Timer function of TRAVEO™ T1G Family consists of a Base timer, Reload timer, Free-run timer, Input Capture, Output compare, and Quadrature Position/Revolution Counter (QPRC).

TRAVEO™ T2G Family implements TCPWM with integrated multiple timer functions. The TCPWM has seven operation modes. All TCPWM channels can be operated by selecting one of the seven modes. Table 20 lists the corresponding modes of each function.

**Table 20 TCPWM Channel Modes**

| Function Name | S6J3428/9/A Series | CY2B7/B9, CYT4BF Series |
|---|---|---|
| Timer Mode | Base timer: Reload Timer mode<br>Free-run Timer<br>Reload Timer | TCPWM: Timer mode |
| Capture Mode | Input Capture<br>Base timer: PWC Timer mode | TCPWM: Capture mode |
| Quadrature Decoder | QPRC | TCPWM: QUAD mode |
| PWM Mode | Output compare<br>Base timer: PWM Timer mode<br>Base timer: PPG Timer mode | TCPWM: PWM mode |
| PWM with Dead Time | Not supported | TCPWM: PWM_DT mode |
| Pseudo-Random PWM | Not supported | TCPWM: PWM_PR mode |
| Shift Register | Not supported | TCPWM: SR mode |

### 2.4.1.1 Base Timer: Reload Timer Mode

The Base Trimer Reload mode in TRAVEO™ T1G Family is a timer that counts down from a set value. When the timer value reaches '0', the timer stops or starts counting down from the set value again. Also, an event can be generated if the timer value is '0'. In TRAVEO™ T2G Family, the same operation is possible using TCPWM Timer mode. Table 21 lists the main differences in Base Timer Reload Timer modes between TRAVEO™ T1G and TRAVEO™ T2G families.

**Table 21 Differences in Base Timer: Reload Timer Mode**

| Counter | S6J3428/9/A Series | CY2B7/B9, CYT4BF Series |
|---|---|---|
| Timer Function | Base Timer: Reload Timer mode | TCPWM: Timer mode |
| Counter Width | 16 bits or 32 bits (uses two 16-bit timer) | 16 bits or 32 bits |
| Count Mode | Down | Up, Down, Up-down1/2 |
| Operation Clock | Internal clock: 12 types:<br>/1, /2, /4, /8, /16, /32, /64, /128, /256, /512, /1024 or /2048 | Internal clock: 8 types:<br>/1, /2, /4, /8, /16, /32, /64 or /128 |
| | External clock:<br>Rising-edge, falling-edge, or both-edge | Not supported[8)] |
| Operation mode | One shot mode:<br>Stop event is underflow | One shot mode:<br>Stop event depends on count mode. (underflow, overflow or both) |
| | Reload mode | Reload mode |
| Gate function | Supported | Supported |
| Activation | Software | Software: via Trigger Multiplexer |
| | External trigger | External trigger |
| | External Timer Match Starting | Not supported |
| Event Generation | Underflow | TC event:<br>TC event depends on count mode. (underflow, overflow or both) |
| | Timer Activation trigger | Not Supported |
| | Not supported | Compare match event |
| Debug Mode | Supported | Supported |

### 2.4.1.2 32-bit Free-run Timer

The Free-run timer in TRAVEO™ T1G Family counts up or up-down within a set value. In TRAVEO™ T2G Family, the same operation is possible using TCPWM Timer mode. However, in TRAVEO™ T2G Family there is no interrupt mask count function. Table 22 lists the main differences in Free-run Timer.

8 The external clock cannot be used as the timer's count clock. However, when the count event is used in the rising edge (supported falling and both edge) detection mode, the timer will count with count event detection. In this case, the count event can be used as the external clock.

**Table 22 Differences in 32-bit Free-run Timer**

| Counter | S6J3428/9/A Series | CY2B7/B9, CYT4BF Series |
|---|---|---|
| Timer function | 32-bit Free-run Timer | TCPWM: Timer mode |
| Counter width | 32 bits | 16 bits or 32 bits |
| Count mode | Up, Up-down | Up, Down, Up-down1/2 |
| Operation clock | Internal clock: 9 types:<br>/1, /2, /4, /8, /16, /32, /64, /128 or /256 | Internal clock: 8 types:<br>/1, /2, /4, /8, /16, /32, /64 or /128 |
| | External clock:<br>Both-edge | Not supported[8] |
| Operation mode | Not Supported | One shot mode:<br>Stop event depends on the count mode (underflow, overflow, or both) |
| | Reload mode | Reload mode |
| Buffer function | Supported | Supported |
| Activation | Software | Software: via Trigger Multiplexer |
| | Not supported | External trigger |
| Event Generation | Compare clear<br>Zero Detection | TC event:<br>TC event depends on count mode (underflow, overflow, or both) |
| | Not supported | Compare match event |
| | Interrupt mask count Function | Not Supported |
| Debug Mode | Supported | Supported |

### 2.4.1.3 32-bit Reload Timer

The 32-bit Reload mode in TRAVEO™ T1G Family is a timer that counts down from a set value. In TRAVEO™ T2G Family, the same operation is possible using TCPWM Timer mode. Table 23 lists the main differences in 32-bit Reload Timer.

**Table 23 Differences of 32-bit Reload Timer**

| Counter | S6J3428/9/A Series | CY2B7/B9, CYT4BF Series |
|---|---|---|
| Timer Function | 32-bit Reload Timer | TCPWM: Timer mode |
| Counter Width | 32 bits | 16 bits or 32 bits |
| Count Mode | Down | Up, Down, Up-down1/2 |
| Operation Clock | Internal clock: 6 types:<br>/1, /2, /4, /8, /16 or /32 | Internal clock: 8 types:<br>/1, /2, /4, /8, /16, /32, /64 or /128 |

**(table continues...)**

8 The external clock cannot be used as the timer's count clock. However, when the count event is used in the rising edge (supported falling and both edge) detection mode, the timer will count with count event detection. In this case, the count event can be used as the external clock.

**Table 23 (continued) Differences of 32-bit Reload Timer**

| Counter | S6J3428/9/A Series | CY2B7/B9, CYT4BF Series |
|---|---|---|
| | External clock:<br>Rising-edge, falling-edge, or both edges | Not supported[8] |
| Operation Mode | One shot mode:<br>Stop event is underflow | One shot mode:<br>Stop event depends on count mode (underflow, overflow, or both) |
| | Reload mode | Reload mode |
| Gate Function | Supported | Supported |
| Activation | Software | Software: via Trigger Multiplexer |
| | External trigger | External trigger |
| Event Generation | Underflow | TC event:<br>TC event depends on count mode (underflow, overflow, or both) |
| | Not supported | Compare match event |
| Simultaneous Soft Start | Supported | Supported: via Trigger Multiplexer |
| Debug Mode | Supported | Supported |

### 2.4.1.4 32-bit Input Capture

The 32-bit input capture function in TRAVEO™ T1G Family measures the input pulse width and external clock cycle based on the value of the 32-bit free-run timer. In TRAVEO™ T2G Family, the same operation is possible using the TCPWM capture mode.

In TRAVEO™ T1G Family, the Input capture function is a linkage function with the free-run timer, but TRAVEO™ T2G Family has an independent timer for each TCPWM channel. Therefore, TRAVEO™ T2G Family does not need a different timer for the Input Capture function. Table 24 lists the main differences in 32-bit Input Capture.

**Table 24 Differences in 32-bit Input Capture**

| Counter | S6J3428/9/A Series | CY2B7/B9, CYT4BF Series |
|---|---|---|
| Timer Function | 32-bit Input Capture | TCPWM: Capture mode |
| Counter Width | 32 bits | 16 bits or 32 bits |
| Count Mode | Follow Free-run Timer | Up, Down, Up-down1/2 |
| Operation Mode | Follow Free-run Timer | One shot mode:<br>Stop event depends on count mode. (underflow, overflow or both) |
| | | Reload mode |

**(table continues...)**

8 The external clock cannot be used as the timer's count clock. However, when the count event is used in the rising edge (supported falling and both edge) detection mode, the timer will count with count event detection. In this case, the count event can be used as the external clock.

**Table 24 (continued) Differences in 32-bit Input Capture**

| Counter | S6J3428/9/A Series | CY2B7/B9, CYT4BF Series |
|---|---|---|
| Clock Pre-scaling | Follow Free-run Timer | Internal clock: 8 types:<br>/1, /2, /4, /8, /16, /32, /64 or /128 |
| Capture Event | Rising-edge, falling-edge, or both-edge | Supported: via Trigger Multiplexer |
| Buffer Function | Not supported | Double buffer<br>Counter value is copied to the capture register and capture register is copied to the capture buffer register when a Capture event is detected. |
| Event Generation | Capture event detection | Counter value is captured. |

### 2.4.1.5 Base Timer: PWC Timer Mode

Base Timer: PWC Timer mode in TRAVEO™ T1G Family measures the time and cycle between any input pulse events by using a counter.

TRAVEO™ T2G Family does not have the same operation mode. However, the TCPWM capture mode can measure via software the time between two events using two buffers. Figure 7 shows an example of the operation.

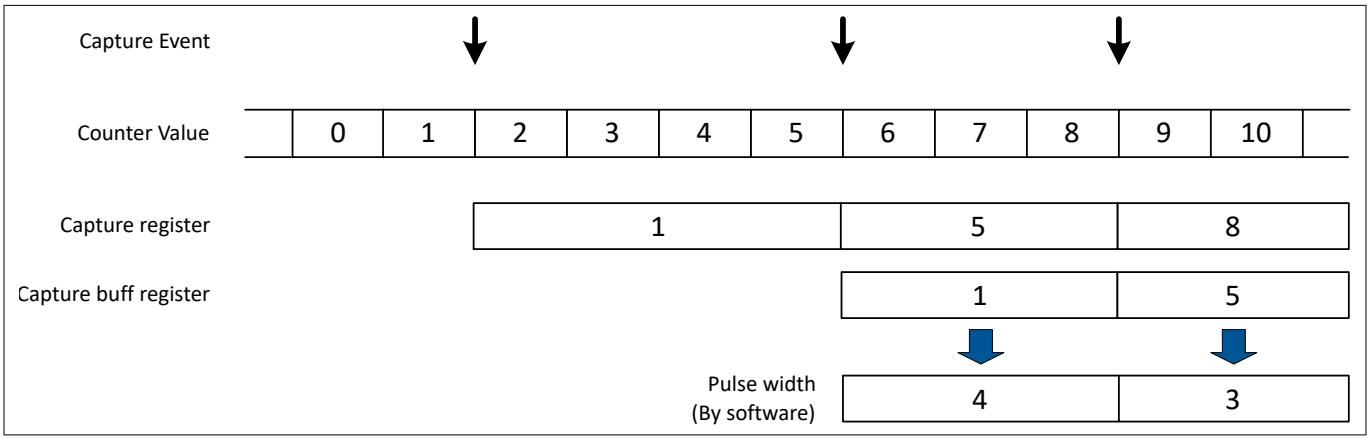


**Figure 7 Example for Pulse Width Count Measurements**

### 2.4.1.6 QPRC

The Quadrature decoder is used to measure the position of position encoder. Both TRAVEO™ T1G and TRAVEO™ T2G families implement Quadrature Decoder.

Both support x 1, x 2, x 4 count modes. However, Revolution counter operation mode is not supported in TRAVEO™ T2G Family. Table 25 lists the main differences in QPRC.

**Table 25 Differences in QPRC**

| Counter | S6J3428/9/A Series | CY2B7/B9, CYT4BF Series |
|---|---|---|
| Timer function | QPRC | TCPWM: QUAD mode |
| Counter width | Two 16 bits (Position counter, Revolution counter) | 16 bits or 32 bits |

**(table continues...)**

**Table 25 (continued) Differences in QPRC**

| Counter | S6J3428/9/A Series | CY2B7/B9, CYT4BF Series |
|---|---|---|
| Position counter Operation mode | Up/Down count mode | Up/Down Rotary mode |
| | Not Supported | x 1 encoding |
| | Phase difference count mode x2 mode<br>Count edge: phi_B | x 2 encoding<br>Count edge: phi_A |
| | Phase difference count mode x4 mode | x 4 encoding |
| | Count mode with direction | Not Supported |
| Revolution counter Operation mode | RC_mode1 | Not supported |
| | RC_mode2 | |
| | RC_mode3 | |
| Event Generation | Count inversion | Not Supported |
| | Zero index | tc event with Reload/Index event |
| | Overflow | Supported<br>QUAD_RANGE1_CMP, QUAD_RANGE1_CAPT |
| | Under flow | Supported<br>QUAD_RANGE1_CMP, QUAD_RANGE1_CAPT |
| | PC and RC match | Not Supported |
| | PC match | Supported:<br>QUAD_RANGE0_CMP<br>QUAD_RANGE1_CMP |
| | PC match and RC match | Not Supported |
| | Out range | Not Supported |
| Capture | Not Supported | Supported: QUAD_RANGE1_CAPT |
| Debug Mode | Not Supported | Supported |

### 2.4.1.7 32-bit Output Compare

The 32-bit output compare in TRAVEO™ T1G Family generates the PWM waveform with 32-bit Free-run timer. In addition, events can be generated at compare match. In TRAVEO™ T2G Family, the same operation is possible using TCPWM PWM mode. Table 26 lists the main differences in 32-bit Reload Timer.

**Table 26 Differences in 32-bit Output Compare**

| Counter | S6J3428/9/A Series | CY2B7/B9, CYT4BF Series |
|---|---|---|
| Timer function | 32-bit Output compare | TCPWM: PWM mode |
| Counter width | 32 bits | 16 bits or 32 bits |
| Count mode | Up, Up-down | Up, Down, Up-down1/2 |
| Operation clock | 9 types Internal Clock<br>• /1, /2, /4, /8, /16, /32, /64, /128 or /256 | Internal clock: 8 types<br>• /1, /2, /4, /8, /16, /32, /64 or /128 |

**(table continues...)**

**Table 26 (continued) Differences in 32-bit Output Compare**

| Counter | S6J3428/9/A Series | CY2B7/B9, CYT4BF Series |
|---|---|---|
| | External clock<br>• Both-edge | Not supported[8] |
| Buffer function | Supported | Supported |
| Compare registers per channel | Two | Two |
| Output pins per channel | Two<br>• OUT0 for compare register 0<br>• OUT1 for compare register 1 | Two<br>• LINE_OUT is an output<br>• LINE_COMPL_OUT is a complementary output |
| One shot mode | Not Supported | One shot mode:<br>• Stop event depends on count mode. (underflow, overflow or both) |
| Signal output | Invert mode | Supported |
| | Set/Reset mode | Supported |
| Activation | Software | Software: via Trigger Multiplexer |
| | Not supported | External trigger |
| | Compare match | Supported |
| | Not Supported | TC event:<br>• TC event depends on count mode. (underflow, overflow or both) |
| Kill modes | Not supported | Supported |
| Debug Mode | Supported | Supported |

### 2.4.1.8 Base Timer: PWM Timer Mode

Base Trimer PWM mode in TRAVEO™ T1G Family can output waveforms of the set cycle either singly or continuously upon the detection of a trigger. In this mode, cycle and duty are set to generate PWM waveform.

In TRAVEO™ T2G Family, the same operation is possible using TCPWM PWM mode. Table 27 lists the main differences in Base Timer PWM Mode.

**Table 27 Differences in Base Timer: PWM Timer Mode**

| Counter | S6J3428/9/A Series | CY2B7/B9, CYT4BF Series |
|---|---|---|
| Timer Function | Base Timer: PWM mode | TCPWM: PWM mode |
| Counter Width | 16 bits | 16 bits or 32 bits |
| Count Mode | Down | Up, Down, Up-down1/2 |

**(table continues...)**

8 The external clock cannot be used as the timer's count clock. However, when the count event is used in the rising edge (supported falling and both edge) detection mode, the timer will count with count event detection. In this case, the count event can be used as the external clock.

**Table 27 (continued) Differences in Base Timer: PWM Timer Mode**

| Counter | S6J3428/9/A Series | CY2B7/B9, CYT4BF Series |
|---|---|---|
| Operation Clock | Internal clock: 12 types<br>/1, /2, /4, /8, /16, /32, /64, /128, /256, /512, /1024 or /2048 | Internal clock: 8 types<br>/1, /2, /4, /8, /16, /32, /64 or /128 |
| | External clock:<br>Rising-edge, falling-edge, or both-edge | Not supported[8] |
| Operation Mode | One shot mode:<br>Stop event is underflow | One shot mode:<br>Stop event depends on count mode. (underflow, overflow or both) |
| | Continuous mode | Reload mode |
| Start Delay | Supported | Not Supported[9] |
| Buffer Function | Supported | Supported |
| Activation | Software | Software: via Trigger Multiplexer |
| | External trigger | External trigger |
| | External Timer Match Starting | Not supported |
| Signal Output | 1: Inverted output when cycle and duty match | 2: Inverted output when compare match<br>LINE_OUT and LINE_COMPL_OUT |
| | Right-aligned PWM | Left-aligned, Right-aligned,<br>Center-aligned, Asymmetric PWM |
| | Output polarity control | Supported |
| Trigger Output | A/D convertor activation | Supported |
| Event Generation | Underflow | TC event:<br>TC event depends on count mode. (underflow, overflow or both) |
| | Duty match | Supported: compare match |
| | Start Trigger Detection | Not Supported |
| Debug Mode | Supported | Supported |

### 2.4.1.9 Base Timer: PPG Timer Mode

The Base Trimer PPG mode in TRAVEO™ T1G Family can output single or continuous waveforms with the configured cycle either when a trigger is detected. In this mode, 'L' width and 'H' width are set to generate the PPG waveform.

In TRAVEO™ T2G Family, the same operation is possible using TCPWM mode. Table 28 lists the main differences in Base Timer: PPG Timer Mode.

8 The external clock cannot be used as the timer's count clock. However, when the count event is used in the rising edge (supported falling and both edge) detection mode, the timer will count with count event detection. In this case, the count event can be used as the external clock.

9 Counters can be pre-loaded with values reflecting the desired phase shift and then started synchronously. Note that during the initial (start delay) period, some counters can already generate the PWM output, depending on the duty cycle.

**Table 28 Differences in Base Timer: PPG Timer Mode**

| Counter | S6J3428/9/A Series | CY2B7/B9, CYT4BF Series |
|---|---|---|
| Timer Function | Base Timer: PPG mode | TCPWM: PWM mode |
| Counter Width | 16 bits | 16 bits or 32 bits |
| Count Mode | Down | Up, Down, Up-down1/2 |
| Operation Clock | Internal clock: 12 types<br>/1, /2, /4, /8, /16, /32, /64, /128, /256, /512, /1024 or /2048 | Internal clock: 8 types:<br>/1, /2, /4, /8, /16, /32, /64 or /128 |
| | External clock:<br>Rising-edge, falling-edge, or both-edge | Not supported[8)] |
| Operation mode | One shot mode:<br>Stop event is underflow | One shot mode:<br>Stop event depends on count mode. (underflow, overflow or both) |
| | Continuous mode | Reload mode |
| Activation | Software | Software: via Trigger Multiplexer |
| | External trigger | External trigger |
| Signal Output | 1<br>Inverted output when cycle and duty match | 2<br>• Inverted output when compare match<br>• LINE_OUT and LINE_COMPL_OUT |
| Event Generation | Underflow | TC event:<br>TC event depends on count mode. (underflow, overflow or both) |
| | Start Trigger Detection | Not Supported |
| Debug Mode | Supported | Supported |

### 2.4.1.10 TCPWM: PWM_DT Mode

This mode adds Dead time to the PMW output waveform. This function is not supported in TRAVEO™ T1G Family. Figure 8 shows an example of the operation. The PWM_DT functionality is the same as the PWM functionality except for the following differences:

- PWM_DT supports dead time insertion; PWM does not support dead time insertion.
- PWM_DT does not support clock pre-scaling; PWM supports clock pre-scaling.

For more details, see the Technical Reference Manual.

8 The external clock cannot be used as the timer's count clock. However, when the count event is used in the rising edge (supported falling and both edge) detection mode, the timer will count with count event detection. In this case, the count event can be used as the external clock.

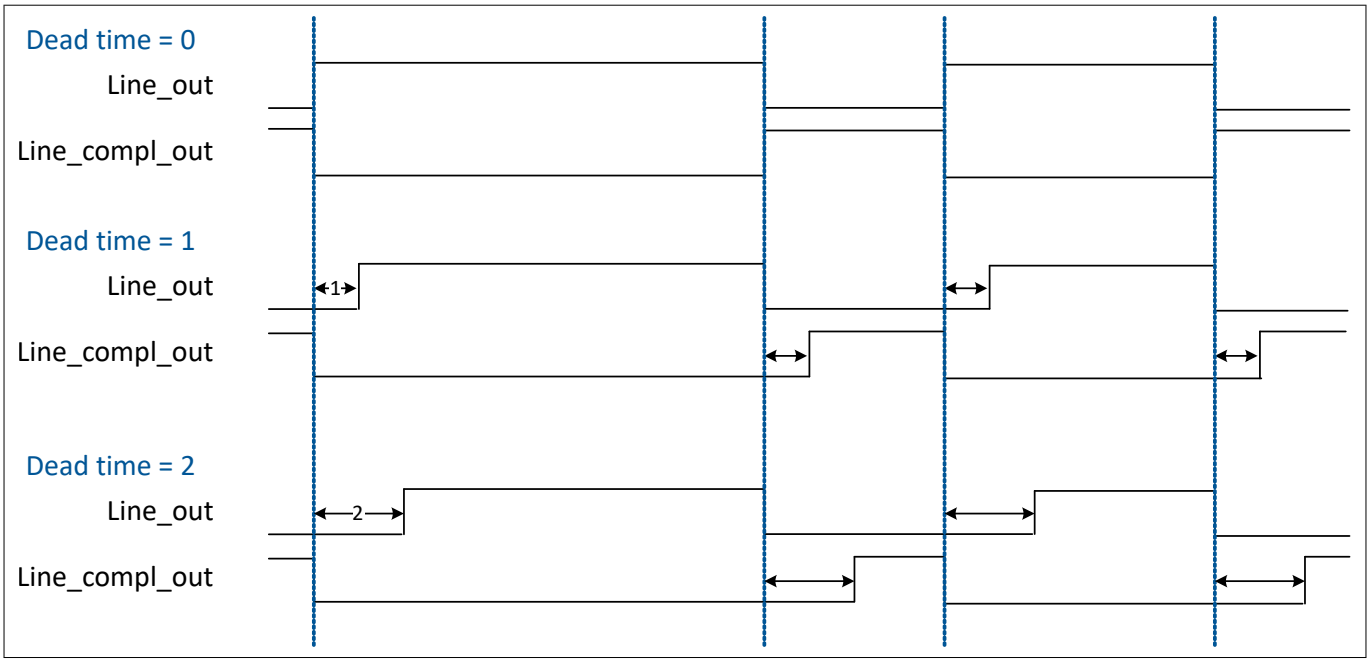


**Figure 8 Dead Time Timing**

### 2.4.1.11 TCPWM: PWM_PR Mode

This functionality changes the counter value using the linear feedback shift register (LFSR). This results in a pseudo random number sequence; the generated signal has frequency/noise characteristics different from a regular PWM signal. This function is not supported in TRAVEO™ T1G Family. Figure 9 shows an example of the operation.

For more details, see the Technical Reference Manual.

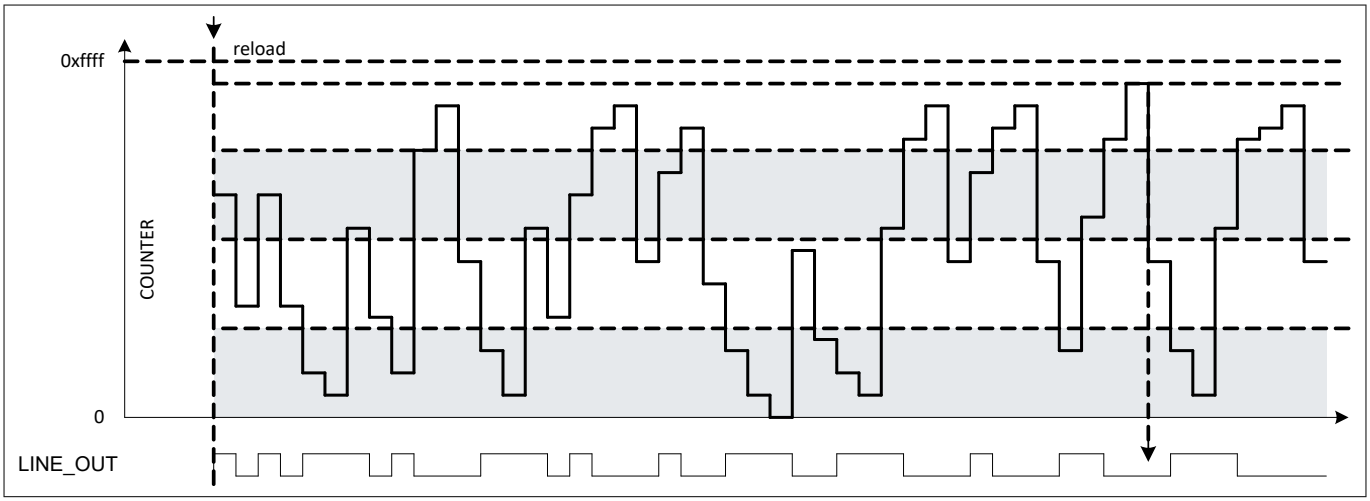


**Figure 9 PWM_PR Output**

### 2.4.1.12 TCPWM: SR Mode

This functionality shifts the counter value to the right. This implements a signal delay function from the trigger input to the line output, which can be used for functions such as detecting frequency shift keying (FSK) signals. This function is not supported in TRAVEO™ T1G Family. Figure 10 shows an example of the operation. For more details, see the TRM.

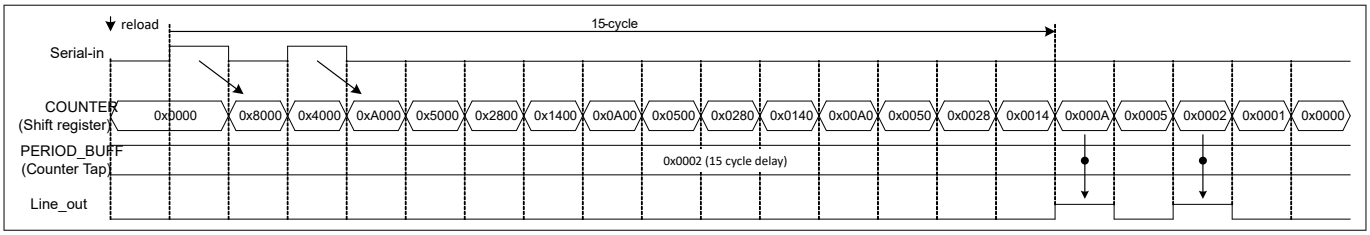


**Figure 10 SR Mode Operation**

PWM line output is generated from an XOR combination of enabled counter taps (bit position) defined by PERIOD_BUFF.

## 2.4.2 Serial Communication Block

The serial communication function realized by MFS on TRAVEO™ T1G Family is realized by SCB in TRAVEO™ T2G Family. In TRAVEO™ T2G Family, the LIN function is realized by a dedicated module.

**Table 29 Differences in Serial Communication Block**

| Item | S6J3428/9/A Series | CY2B7/B9, CYT4BF Series | |
|---|---|---|---|
| Function name | Multi-Function Serial (MFS) | Serial communication Block (SCB) | LIN |
| Supported function | • UART<br>• CSIO (SPI Supported)<br>• I2C<br>• LIN (v2.1) | • UART<br>• SPI<br>• I2C | LIN (v 2.2A) |

### 2.4.2.1 UART

TRAVEO™ T2G Family SCB (UART) data transmission and reception are always executed in FIFO mode. In TRAVEO™ T2G Family, eight out of nine SCB blocks support full UART, and one SCB does not support UART mode. Table 30 lists the main differences.

**Table 30 Differences in UART**

| Item | S6J3428/9/A Series | CY2B7/B9, CYT4BF Series |
|---|---|---|
| Data | Transmission and reception FIFOs (64 bytes each) (when FIFOs are used) | Transmission/reception FIFO (32/256/512 bytes each) (FIFO mode only) |
| Serial Input | Oversampling is performed 3 times by the bus clock. The reception value is determined by majority decision. | • Use clk_scb<br>• Use input clock (clk_scb) as “oversampling multiple” of interface clock |
| Transfer Format | Asynchronous | Asynchronous |
| Baud Rate | Dedicated baud rate generator (15-bit reload counter configuration) | CTRL.OVS register supported<br>• Baud rate= clk_scb / (OVS + 1) *OVS=7-15 |
| | The external clock input can be adjusted by the reload counter. | Not supported |

**(table continues...)**

**Table 30 (continued) Differences in UART**

| Item | S6J3428/9/A Series | CY2B7/B9, CYT4BF Series |
|---|---|---|
| Data Length | 5 to 9 bits (for normal mode), or 7 to 8 bits (for multi-processor mode) | 4 to 16 bits (Standard/Multi-processor mode) |
| Signaling Method | NRZ | NRZ |
| | Inverted NRZ | Not supported |
| Start Bit Detection | Synchronized to falling edges of the start bit (for NRZ method) | Synchronized with the start bit falling edge (NRZ system) |
| | Synchronized to rising edges of the start bit (for inverted NRZ method) | Not supported |
| Reception Error Detection | Framing error | Framing error |
| | Overrun error | Not supported |
| | Parity error<br>(Normal mode only) | Parity support<br>(Odd parity and even parity) |
| Hardware Flow Control | Transmission/reception auto control by CTS and RTS | Transmission/reception auto control by CTS and RTS |
| Interrupt Request | Reception interrupt | Reception interrupt<br>(Frame error, Parity error) |
| | Reception FIFO interrupt | Reception FIFO interrupt<br>(RX FIFO is full, RX FIFO is not empty, RX FIFO overflow, RX FIFO underflow) |
| | Transmission interrupt | Transmission interrupt (TX done) |
| | Transmission FIFO interrupt | Transmission FIFO interrupt<br>(TX FIFO is not full, TX FIFO is empty<br>TX FIFO overflow, TX FIFO underflow) |
| | DMA transfer is supported for both transmission and reception | Not supported |
| | Status interrupt | Not supported |
| Master/Slave-Type Communication Function (Multi-Processor Mode) | 1 (master) -to-n (slave) communication is supported.<br>(Both master and slave systems are supported.) | 1 (Master)-to-n (slave)<br>communication is supported<br>(Both master and slave systems are supported) |
| FIFO option | Transmission and reception FIFOs are provided | Transmission and reception FIFOs are supported |
| | Transmission FIFO and reception FIFO can be selected | Not supported |
| | Transmission data can be retransmitted | Not supported |
| | The timing of the reception FIFO interrupt can be changed by software | The timing of the reception FIFO interrupt can be changed by software |
| | Independent FIFO reset is supported | Independent FIFO reset is supported |

### 2.4.2.2 I²C

TRAVEO™ T2G Family SCB (I²C) data transmission and reception are always executed in FIFO mode. In TRAVEO™ T2G Family, eight out of nine SCB blocks support full I²C and one SCB supports only I²C slave mode. Table 31 lists the main differences.

**Table 31 Differences in I²C**

| Item | S6J3428/9/A Series | CY2B7/B9, CYT4BF Series |
|---|---|---|
| Data Buffer | Full duplex-double buffer (FIFO is unused). | Single memory buffer.<br>(EZ I²C /Command-RESP). |
| | Transmission/reception FIFO (16 bytes each) (when FIFO is used). | Transmission/reception FIFO (32/256/512 bytes each) (FIFO mode only). |
| Serial Input | For serial clock and data input, noise from 2 to up to 38 bus clocks is filtered out. | Filtering glitches up to 50 ns. |
| Transfer Mode | Synchronization | Synchronization |
| Baud Rate | Dedicated baud rate generator provided (comprising 15-bit reload counter). | • Slow mode (50 kbps)<br>• Standard mode (100 kbps)<br>• Fast mode (400 kbps)<br>• Fast mode plus (1000 kbps) |
| Data Length | 8 bits | 8 bits |
| Signaling Method | NRZ | NRZ |
| Interrupt Request | Reception interrupt | Reception interrupt.<br>(I²C STOP detection at the end of each transfer, I²C STOP detection at the end of a read transfer). |
| | Transmission interrupt | Transmission interrupt.<br>(I²C STOP detection at the end of each transfer, I²C STOP detection at the end of a write transfer). |
| | Status interrupt<br>(INT interrupt, stop condition interrupt, repeated start detection interrupt, serial timer interrupt). | Status interrupt.<br>(I²C master lost arbitration, I²C master received NACK, I²C master received ACK, I²C bus error, I²C slave lost arbitration, I²C slave received NACK, I²C slave received ACK, I²C slave received STOP, I²C slave received START, I²C slave address matched, I²C bus error). |
| | Transmission FIFO interrupt (A transmission FIFO overrun error occurs when the transmission FIFO is not higher than the interrupt trigger level or when the transmission FIFO is empty). | Transmission FIFO interrupt (TX FIFO is not full, TX FIFO is empty, TX FIFO overflow, TX FIFO underflow). |
| | Reception FIFO interrupt (reception FIFO under run) | Reception FIFO interrupt (RX FIFO is full, RX FIFO is not empty, RX FIFO overflow, RX FIFO underflow). |

**(table continues...)**

**Table 31 (continued) Differences in I²C**

| Item | S6J3428/9/A Series | CY2B7/B9, CYT4BF Series |
|---|---|---|
| | A DMA transfer support function is provided for both transmission and reception. | Not supported |
| | Not supported | Wake up request on address match |
| FIFO | • Transmission and reception FIFOs are provided (64 bytes for the transmission FIFO and 64 bytes for the reception FIFO).<br>• The transmission FIFO and reception FIFO can be selected.<br>• Transmission data can be retransmitted.<br>• The reception FIFO interrupt timing can be changed by software.<br>• Independent FIFO reset is supported. | • Transmission/reception FIFO (32/256/512 bytes).<br>• The transmission FIFO and reception FIFO can be selected.<br>• Transmission data can be retransmitted.<br>• The reception FIFO interrupt timing can be changed by software. |
| Clock Stretching | Supported | Supported |
| I²C Mode | Supported<br>• Master<br>• Slave<br>• Multi-master | Supported<br>• Master<br>• Slave<br>• Multi-master |

### 2.4.2.3 SPI

TRAVEO™ T2G Family SCB (SPI) data transmission and reception are always executed in FIFO mode. In TRAVEO™ T2G Family, eight out of nine SCB blocks support full SPI, and one SCB supports only SPI slave mode. Table 32 lists the main differences.

**Table 32 Differences in SPI**

| Item | S6J3428/9/A Series | CY2B7/B9, CYT4BF Series |
|---|---|---|
| Data Buffer | Transmission and reception FIFOs (64 bytes each) (when FIFO is used) | Transmission/reception FIFO (32/256/512 bytes each) (FIFO mode only) |
| Transfer Format | Clock synchronization (no start/stop bits) | Clock synchronization (no start/stop bits) |
| | Master/slave functions | Master/slave functions |
| | Supports SPI (supports both master and slave) | Supports SPI (supports both master and slave) |
| Baud Rate | A dedicated baud rate generator is provided (configured from a 15-bit reload counter, during master operation).<br>Maximum 8 Mbps | • CTRL.OVS register supported<br>• Baud rate= clk_scb / (OVS + 1) *OVS=3-15, Maximum 12 Mbps |
| | External clock input is enabled (during slave operation) | Supports externally clocked slave operation |

**(table continues...)**

**Table 32 (continued) Differences in SPI**

| Item | S6J3428/9/A Series | CY2B7/B9, CYT4BF Series |
|---|---|---|
| Data Length | 5 to 16, 20, 24, and 32 bits | Data frame size programmable from 4 bits to 32 bits |
| Interrupt Request | Reception interrupt<br>• Reception completion<br>• Overrun error<br>• Reception block transfer error | Not supported |
| | Reception FIFO interrupt<br>• Reception FIFO under run | Reception FIFO interrupt<br>• RX FIFO is full<br>• RX FIFO is not empty<br>• RX FIFO overflow<br>• RX FIFO underflow |
| | Transmission interrupt<br>• Transmission data empty<br>• Transmission bus idle<br>• Chip error interrupt<br>• Transmission block transfer error | Transmission interrupt<br>• SPI master transfer done<br>• SPI Bus Error<br>• SPI slave deselected after any EZSPI transfer occurred<br>• SPI slave deselected after a write EZSPI transfer occurred |
| | Transmission FIFO interrupt<br>• When the transmission FIFO is not higher than the interrupt trigger level<br>• When the transmission FIFO is empty, transmission FIFO overrun | Transmission FIFO interrupt<br>• TX FIFO is not full<br>• TX FIFO is empty<br>• TX FIFO overflow<br>• TX FIFO underflow |
| | DMA Transfer support function is provided for both transmission and reception | Not supported |
| | Status interrupt<br>• Serial timer interrupt | Status interrupt<br>• Wake up request on slave select<br>• SPI STOP detection at the end of each transfer<br>• SPI STOP detection at the end of a write transfer<br>• SPI STOP detection at the end of a read transfer |
| Serial Chip Select | • Four-channel control (independent control, rounding control)<br>• The setup/hold/deselect times can be made variable<br>• The active level can be selected for each channel | • Supports up to four slave select lines |

**(table continues...)**

**Table 32 (continued) Differences in SPI**

| Item | S6J3428/9/A Series | CY2B7/B9, CYT4BF Series |
|---|---|---|
| Synchronous Mode | Master or slave function | Master or slave function |
| FIFO Option | • Incorporates transmission and reception FIFOs (64 bytes for transmission FIFO, 64 bytes for reception FIFO)<br>• The transmission and reception FIFOs can be selected<br>• Transmission data can be retransmitted<br>• The timing of the reception FIFO interrupt can be changed by software<br>• Independent FIFO reset is supported | • Transmission/reception FIFO equipped (transmission FIFO: 32/256/512 bytes, reception FIFO: 32/256/512 bytes)<br>• Reception FIFO interrupt timing can be modified by software<br>• FIFO reset is supported independently |

### 2.4.2.4 LIN

The TRAVEO™ T2G Family LIN block supports autonomous forwarding of LIN frames. Table 33 lists the main differences.

**Table 33 Differences in LIN**

| Item | S6J3428/9/A Series | CY2B7/B9, CYT4BF Series |
|---|---|---|
| Serial Input | Over sampling is performed by the bus clock 3 times. The reception value is determined by the rule of majority. | 3 times oversample (noise filter) at sample point. |
| Transfer Mode | Asynchronous | Asynchronous |
| Baud Rate | • Dedicated baud rate generator is provided (consisting of a 15-bit reload counter).<br>• The external clock can be adjusted by the reload counter.<br>• Auto baud rate adjustment with Sync Field reception. | • Set for each channel.<br>• baud rate adjustment by receiving Sync Field by application. |
| Data Length | 8 bits | 8 bits |
| Signaling Method | NRZ | NRZ |
| Start Bit Detection | Synchronized with falling edges of the start bit | Synchronized with falling edges of the start bit |

**(table continues...)**

**Table 33 (continued) Differences in LIN**

| Item | S6J3428/9/A Series | CY2B7/B9, CYT4BF Series |
|---|---|---|
| Error Detection | • Framing error<br>• Overrun error<br>• Transmitter bit error<br>• Receive synchronization error<br>• Receiver PID error<br>• Receiver frame error<br>• Response checksum error<br>• Timeout detection | • Transmitter bit error<br>• Receive synchronization error<br>• Receiver frame error<br>• Receiver PID parity error<br>• Response checksum error<br>• Receiver noise detection |
| Interrupt Request | Reception interrupt<br>• Reception completion<br>• Reception block transfer error | Reception interrupt<br>• RX break wakeup done<br>• RX header sync done<br>• RX header done<br>• RX response done |
| | Reception FIFO interrupt<br>• Reception FIFO underrun | Not supported |
| | Transmission interrupt<br>• TX data empty<br>• TX bus idle<br>• TX block transfer error | Transmission interrupt<br>• TX header done<br>• TX response done<br>• TX wakeup done |
| | Status interrupts<br>• LIN Break Field detection<br>• Serial timer interrupt | Status interrupts<br>• Receiver noise detection<br>• Time out detection |
| | Interrupt request to ICU<br>• LIN Sync Field detection: LSYN | Not supported |
| | Transmission FIFO interrupt<br>• When the transmission FIFO is within the interrupt threshold<br>• When the transmission FIFO is empty<br>• Transmission FIFO overrun | Not supported |
| | DMA transfer is supported for both transmission and reception. | Not supported |

**(table continues...)**

**Table 33 (continued) Differences in LIN**

| Item | S6J3428/9/A Series | CY2B7/B9, CYT4BF Series |
|---|---|---|
| LIN Bus Option | • Support for LIN Protocol Revision 2.1<br>• Master device operation (auto and manual mode)<br>• Slave device operation (only manual mode)<br>• Auto header transmission<br>• Auto response transmission<br>• Auto response reception<br>• Detection of the start/stop edge of the LIN sync field connected to an input capture<br>• LIN break field generation (manual mode)<br>• LIN break delimiter generation (manual mode)<br>• LIN break field detection (manual mode) | • LIN protocol support in hardware according to ISO 17987 standard<br>• Master device operation (auto mode)<br>• Slave device operation (auto mode)<br>• Auto header transmission<br>• Auto response transmission<br>• Auto response reception |
| Wakeup Pulse | • Reception not supported<br>• Transmission not supported | • Reception supported<br>• Transmission supported |
| LIN Transceiver Control | • Not supported | • Supported |
| UART protocol | • Not supported | • Supported |

## 2.4.3 CAN FD

Table 34 lists the CAN FD features. TRAVEO™ T2G Family shares the message RAM and Timestamp function for global channel control. TRAVEO™ T2G Family supports the receive FIFO top pointer for DMA transfer.

**Table 34 Differences in CAN FD**

| CAN FD | S6J3428/9/A Series | CY2B7/B9, CYT4BF Series |
|---|---|---|
| Classical CAN | Supported | Supported |
| CAN FD | Supported | Supported |
| TTCAN | Not supported | Supported |

**(table continues...)**

**Table 34 (continued) Differences in CAN FD**

| CAN FD | S6J3428/9/A Series | CY2B7/B9, CYT4BF Series |
|---|---|---|
| Message Buffer[10] | • 64 (Extended ID]) + 128 (Standard ID]) Rx filters<br>• 2 * 64 MSG Rx FIFO + 64 MSG dedicated Rx buffers<br>• 32 MSG dedicated Tx buffers<br>• 32 event Tx FIFO | • 64 (Extended ID]) + 128 (Standard ID]) Rx filters<br>• 2 * 64 MSG Rx FIFO + 64 MSG dedicated Rx buffers<br>• 32 MSG dedicated Tx buffers<br>• 32 event Tx FIFO |
| Message Handler | 1 | 1 |
| Message RAM Access | Direct access | Direct access |
| Message RAM | Dedicated type | Shared type |
| Message RAM with ECC | Supported | Supported |
| Timestamp Function | Supported | Supported<br>• Shared Timestamp counter |
| Receive FIFO Top Pointer | Not supported | Supported |

## 2.4.4 I/O Interface

Table 35 lists the I/O interface features. The main differences are the input threshold selection, output drive strength selection, noise filter, and Smart IO.

**Table 35 Differences in I/O Interface**

| I/O Interface | S6J3428/9/A Series | CY2B7/B9, CYT4BF Series |
|---|---|---|
| Input Threshold Selection<br>• CMOS (0307)<br>• Automotive (0508)<br>• TTL | Supported except TTL | Supported |
| Output Drive Strength Selection | Supported<br>• 1 mA<br>• 2 mA<br>• 3 mA only for I2C<br>• 5 mA | Supported<br>• 0.5 mA<br>• 1 mA<br>• 2 mA<br>• 5 mA<br>• 6 mA only for GPIO (IOL)<br>• 10 mA only for HSIO_STD (Only for CYT4BF) |

**(table continues...)**

10 For TRAVEO™ T1G and TRAVEO™ T2G the listed numbers indicate the maximum addressable message buffers; utilization depends on available MRAM size.

**Table 35 (continued) Differences in I/O Interface**

| I/O Interface | S6J3428/9/A Series | CY2B7/B9, CYT4BF Series |
|---|---|---|
| Pull-up/Pull-down | Supported<br>• 50 kΩ (typ) | Supported<br>• 50 kΩ (typ) |
| High-Z State | Supported | Supported |
| Port Status Hold During Low-Power Mode | Supported | Supported |
| Noise Filter | Supported per port pin<br>• Max 100 ns | Supported per port group<br>• Max 50 ns |
| Smart IO | Not supported | Supported |

## 2.4.5 ADC

Table 36 lists the ADC features. The main differences are the result data format, averaging, and pre-conditioning.

**Table 36 Differences in ADC**

| ADC | S6J3428/9/A Series | CY2B7/B9, CYT4BF Series |
|---|---|---|
| 12-bit Resolution | Supported | Supported |
| Logical Channel | Supported | Supported |
| Software Trigger | Supported | Supported |
| Hardware Trigger | Supported | Supported |
| Idle Trigger (Continuous) | Supported<br>• Idle trigger | Supported<br>• Continuous |
| Result Data per Each Channel | Supported<br>• Single buffer | Supported<br>• Double buffer |
| Result Data Format | • Unsigned (fixed)<br>• Right alignment (fixed)<br>• 8-bit/10-bit/12-bit | • Sign/unsigned<br>• Left/right alignment<br>• Max 16-bit (Sign/zero extension), Programmable right shift |
| Programmable Sample Time per Each Channel | Supported<br>• Select one from four 16-bit register<br>• ≥ 7 cycles | Supported<br>• 12-bit registers per each channel<br>• ≥ 11 cycles |
| Comparison Time | ≥ 16 cycles (16-bit register) | 15 cycles (Fixed) |
| Range Detection | Supported<br>• Select one from eight thresholds (above/below) register per each channel<br>• Inside/Outside | Supported<br>• Thresholds (above/below) registers per each channel<br>• Inside/Outside/Above/Below |

**(table continues...)**

**Table 36 (continued) Differences in ADC**

| ADC | S6J3428/9/A Series | CY2B7/B9, CYT4BF Series |
|---|---|---|
| Pulse Detection | Supported<br>• 8-bit Positive counter<br>• 5-bit Negative counter | Supported<br>• 8-bit Positive counter<br>• 5-bit Negative counter |
| Averaging | Not supported | Supported |
| Group Scan | Supported | Supported |
| Preemption Types when Group Interrupted | Supported<br>• Resume<br>• Restart<br>• Stop | Supported<br>• ABORT_RESUME<br>• ABORT_RESTART<br>• ABORT_CANCEL<br>• FINISH_RESUME |
| Priority | Supported<br>• 16 priorities per channel | Supported<br>• 8 priorities per group |
| Interrupt | Supported<br>• Per channel/group conversion done<br>• Per channel range detect<br>• Per channel pulse detect<br>• Group interrupted | Supported<br>• Per channel range detect<br>• Per channel pulse detect<br>• Per channel/group overflow<br>• Group/channel done<br>• Group cancelled |
| DMA Request | Supported | Supported |
| Calibration | Supported<br>• Analog calibration | Supported<br>• Analog calibration<br>• Alternate calibration<br>• Coherent calibration update |
| Pre-conditioning | Not supported | Supported<br>• Off<br>• VREFL<br>• VREFH<br>• Diagnostic reference voltage |
| Diagnostic Reference Voltage | Supported<br>• AVRL<br>• AVRH | Supported<br>• 10 voltage levels from VREFL to VREFH |
| Power Down Mode | Supported | Supported |
| Debug Mode | Supported | Supported |
| Software Abort | Supported<br>• Forced stop | Supported<br>• IP disable |

### 2.4.6 RTC

Table 37 lists the RTC features. The main differences are the source clock, interrupts, and the counters of half-second/month/year.

**Table 37 Differences of RTC**

| RTC | S6J3428/9/A Series | CY2B7/B9, CYT4BF Series |
|---|---|---|
| Source Clock | Main clock oscillator (4 MHz)<br>Sub clock oscillator (32 kHz)<br>Internal low speed oscillator (100 kHz) | Watch Crystal oscillator (32 kHz)<br>Internal low speed oscillator (32 kHz) |
| Half-second Counter | Supported | Not supported<br>• Event Generator can count less than a second |
| Second Counter | Supported | Supported |
| Minute Counter | Supported | Supported |
| Hour Counter | Supported | Supported |
| Day Counter | Supported | Supported |
| Month Counter | Not supported | Supported |
| Year Counter | Not supported | Supported |
| Automatic Leap Year Correction | Not supported | Supported |
| Interrupt | Each counter (Day/Hour/Minute/Second/ Half-second) | Two independent alarms (Month + Day + Hour + Minute + Second) |
| Calibration | Supported<br>• Automatic calibration by main clock | Supported<br>• Calibration by waveform output and software |

### 2.4.7 CRC

In TRAVEO™ T1G Family, CRC was implemented in a dedicated CRYPT and DMA module.

**Table 38 Differences in CRC**

| Item | S6J3428/9/A Series | CY2B7/B9, CYT4BF Series |
|---|---|---|
| Method | Supported CRC module<br>• CCITT CRC16 (polynomial = “0x1021”)<br>• IEEE-802.3 CRC32 (polynomial = “0x04C11DB7”) | Supported CRYPT module and DMA module<br>• CCITT CRC16 (polynomial = “0x1021”)<br>• IEEE-802.3 CRC32 (polynomial = “0x04C11DB7”) |

### 2.4.8 CXPI

TRAVEO™ T2G Family has a CXPI module only in CYT2B9 series MCUs.

CXPI supports the following:

- CXPI protocol support in hardware according to ISO/WD 20794-4

- Master node
  - Autonomous request field and response transfer processing
- Network access method
  - Event-triggered method
  - Polling method
- Carrier sense multiple access and collision resolution (CSMA/CR)
- Data signal encoding/decoding format
  - Non-return to zero (NRZ) mode
  - Pulse width modulation (PWM) mode
- Wake pulse generation
- Clock detection
- 8-bit checksum for normal frame and 16-bit checksum for long frame
- 400x bit time oversampling
- Error detection
- Timeout detection
- Message buffers for the following:
  - Protected identifier (PID) field
  - Frame information (FI) field
  - 16x depth transmission and reception FIFO buffer
  - Checksum field
- Test modes include hardware error injection

### 2.4.9 FlexRay

TRAVEO™ T2G Family has a FlexRay module only in CYT4BF Series MCUs.

FlexRay provides the following functionalities:

- Conformance with FlexRay protocol specification v2.1
- Data rates of up to 10 Mbps on each channel
- Up to 128 message buffers configurable
- 8 KB Message RAM for storage. This can be 128 message buffers with max. 48-bytes data section or up to 30 message buffers with 254-byte data section.
- Configuration of message buffers with different payload lengths possible
- One configurable Receive FIFO
- Each message buffer can be configured as Receive buffer, as Transmit buffer, or as part of the Receive FIFO
- Host access to message buffers via Input and Output Buffer
- Input Buffer: Holds message to be transferred to the Message RAM
- Output Buffer: Holds message read from the Message RAM
- Filtering for slot counter, cycle counter, and channel
- Maskable module interrupts
- Network Management supported

FlexRay consists of the following major six sub-blocks implementing these interfaces:

- FlexRay protocol specification 2.1, and supports up to a 10 Mbps data rate
- CIF MMIO registers
- DMA control

- Synchronization trigger generator
- Decoder acts between the AHB interface and other functional blocks
- AHB slave interface drives the host requests to this FlexRay module

The following interfaces are supported:

- 32-bit AHB-lite interface to the Host processor. Only word (32-bit) transactions are supported. Half-word (16-bit) and byte (8-bit) transactions return bus error responses.
- FlexRay physical layer interface
- Interrupts to the Host processor.
- Trigger interface (DMA and External synchronization)

### 2.4.10 SDHC Host Controller

TRAVEO™ T2G Family has a SDHC Host Controller module only in CYT4BF Series MCUs.

The SDHC Interface provides the following functionalities:

- Standard compliance:
  - SD 6.0 / SDIO 4.10 / eMMC 5.1
    - SD SDR50: 50 MB/s (4-bits data @ 100 MHz)
    - eMMC 52 MHz DDR: 104 MB/s (8 bits data @ 52 MHz DDR)
- - HCI 4.2 (Host Controller Interface) spec shared by SD and eMMC
- AHB master interface
  - With ADMA3
    - Supports data prefetch for back to back WRITE operations
- Single ported RAM for packet storage
  - Automatic packing/unpacking of data to fit buffer width
- AHB slave interface for configuration/control/status

### 2.4.11 Serial Memory Interface

TRAVEO™ T2G Family has a Serial Memory Interface (SMIF) only in CYT4BF Series MCUs.

SMIF provides an SPI master interface to serial memory devices that support a single, dual, or quad SPI protocol. SMIF provides the following functionality:

- HyperBus protocol
- SPI mode 0: clock polarity (CPOL) and clock phase (CPHA) are both ‘0’.
- Support for single, dual and quad SPI protocols.
- Support for dual-quad SPI mode: the use of two quad SPI memory devices to increase data bandwidth for SPI read and write transfers.
- Support for single data rate (SDR) and dual data rate (DDR) transfers.
- Support for up to four external memory devices. Support for device capacities in the range of [64 KB, 4 GB] in power of 2 multiples.
- Execute-in-place (XIP) and memory-mapped input/output (MMIO) operation modes.
  - XIP operation mode supports both SPI read and write transfers.
- Support of a 4-KB XIP read cache.
- XIP operation mode supports on-the-fly encryption for write data and on-the-fly decryption for read data.
- SPI interface logic supports stalling of SPI transfers to address back pressure on FIFOs.
- SPI interface logic supports an asynchronous SPI transmit and receive interface clock.

- SPI interface logic supports multiple interface receive clocks.
- SPI interface logic supports flexible external memory devices data signal connections.

### 2.4.12 Ethernet

TRAVEO™ T2G Family has an Ethernet module only in CYT4BF Series MCUs.

Ethernet provides an interface to an external PHY to get Ethernet functionality. Ethernet provides the following functionality:

- 10, 100, and 1000 Mbps full-duplex operation
- RGMII, RMII, and GMII interfaces supported
- AXI Interface (64-bit)
- Support for up four Tx and 1 Rx Priority queues
- Support for 802.1AS and 1588 precision clock synchronization protocol
- Support for 1588 one-step clock for Tx Sync frames
- Optional IEEE 1588 timestamp unit
- Support for 802.3az EEE
- Support for 802.1Qbb priority-based flow control
- Receive and transmit IP, TCP, and UDP checksum offload
- Automatic pad and CRC generation on transmitted frames
- MDIO interface for PHY management
- Supports 802.1Qav traffic shaping on two highest-priority transmit queues
- Supports strict priority, DWRR, or Enhanced Transmission Selection (ETS - 802.1Qaz) on transmit queues

## 2.5 Development Tools and Flash Programming Tools

TRAVEO™ T1G and TRAVEO™ T2G families supports Green Hills Software (GHS) and IAR tools. In addition to these tools, TRAVEO™ T2G Family also supports the tools from other vendors such as iSystem, Lauterbach, and Segger.

Table 39 lists the main differences between development tools and Flash programming.

**Table 39 Development Tools and Flash Programming Tools**

| Tools | S6J3428/9/A Series | | CY2B7/B9, CYT4BF Series | |
|---|---|---|---|---|
| | **Emulators/Probes** | **Software/Compiler** | **Emulators/Probes** | **Software/Compiler** |
| Development Tool | GHS Probe | GHS Multi (v2015.1.6 or later) | GHS Probe (5.4.4) | GHS Multi V7 (Version 7.1.4) |
| | IAR I-JET | EWARM (v7.30.4 or later) | IAR I-JET | EWARM (8.11) |
| | – | – | iSystem i-TAG Family | – |
| | | | Lauterbach TRACE 32-ICE | |
| Flash Programming Tool | GHS Probe | GHS Multi (v2015.1.6 or later) | GHS Probe (5.4.4) | GHS Multi V7 (Version 7.1.4) |

**(table continues...)**

**Table 39 (continued) Development Tools and Flash Programming Tools**

| Tools | S6J3428/9/A Series | | CY2B7/B9, CYT4BF Series | |
|---|---|---|---|---|
| | **Emulators/Probes** | **Software/Compiler** | **Emulators/Probes** | **Software/Compiler** |
| | IAR I-JET | EWARM (v7.30.4 or later) | IAR I-JET | EWARM (8.11) |
| | Serial Interface Cable (with serial programming mode) | Flash programmer | Cypress MiniProg3 | Cypress Programmer (CYP) |
| | Minato | – | Segger J-Link | J-Flash |
| | BPM Micro | | Segger Flasher Arm (for mass-production) | J-Flash |
| | DTS INSIGHT | | | |

## 2.6 MCAL Support

Table 40 lists MCAL features. The main differences are AUTOSAR revision, compiler, and OCU module.

**Table 40 Differences in MCAL Support**

| MCAL | TRAVEO™ T1G Family | TRAVEO™ T2G Family |
|---|---|---|
| AUTOSAR Revision | 4.0.3 | 4.2.2 |
| Compiler | GHS MULTI V2015.1.6 | GHS MULTI V2017.1.4 |
| MCU module | Supported | Supported |
| WDG module | Supported | Supported |
| GPT module | Supported | Supported |
| FLS module | Supported | Supported |
| SPI module | Supported | Supported |
| LIN module | Supported | Supported |
| CAN module | Supported | Supported |
| ICU module | Supported | Supported |
| PWM module | Supported | Supported |
| ADC module | Supported | Supported |
| DIO module | Supported | Supported |
| PORT module | Supported | Supported |
| OCU module | Not supported | Supported |

# 3 Cluster Products

## 3.1 Target Products and TRAVEO™ T2G Family MCU Features

**Table 41 Target Products**

| MCU Family | MCU Series |
|---|---|
| TRAVEO™ T1G Family | S6J3200 series |
| TRAVEO™ T2G Family | CYT4DN series, CYT2C9 series |

**Table 42 Comparison of TRAVEO™ T1G and TRAVEO™ T2G Family MCUs**

| Function | TRAVEO™ T1G Family | TRAVEO™ T2G Family | |
|---|---|---|---|
| | S6J3200 Series | CYT4DN Series | CYT2C9 Series |
| Flash Memory (Code Flash) | 2112 KB | 6336 KB | 2112 KB |
| Flash Memory (Work Flash) | 112 KB | 128 KB | 128 KB |
| SRAM0 | 256 KB | 256 KB | 256 KB |
| SRAM1 | – | 256 KB | – |
| SRAM2 | – | 128 KB | – |
| CXPI | Not Supported | Supported | Supported |
| Graphics Interface | Video output<br>• DRGB x2<br>• RSDS x1<br>• LVDS (FDP-Link) x1<br>Video input<br>• RGB/YUV/ITU656 x1<br>Graphics Engine<br>• 2D graphics engine (2.5D effects)<br>• 3D graphics engine | Video output<br>• DRGB x2<br>• LVDS (FDP-Link) x2<br>Video input<br>• RGB/YUV/ITU656 x1<br>• MIPI CSI-2 x1<br>Graphics Engine<br>• 2D graphics engine (2.5D effects) | Not Supported |
| Audio | $I^2S$ x2<br>Not Supported TDM<br>PCMPWM x2<br>Sound Generator x1, Sound Waveform Generator x1<br>Mixer x5<br>Audio DAC x1 | $I^2S$ x4<br>TDM x4<br>PCMPWM x2<br>Sound Generator x1<br>Mixer x2<br>Audio DAC x1 | $I^2S$ x2<br>TDM x2<br>PCMPWM x1<br>Sound Generator x5<br>Mixer x1<br>Not Supported Audio DAC |
| Serial Memory Interface | Supported (HSSPI, HyperBus) | Supported | Not Supported |
| Ethernet | Supported | Supported | Not Supported |
| LCD Controller | Supported | Not Supported | Supported |

## 3.2 Product Overview

Figure 11 show the major architecture components of the CYT4DN series.

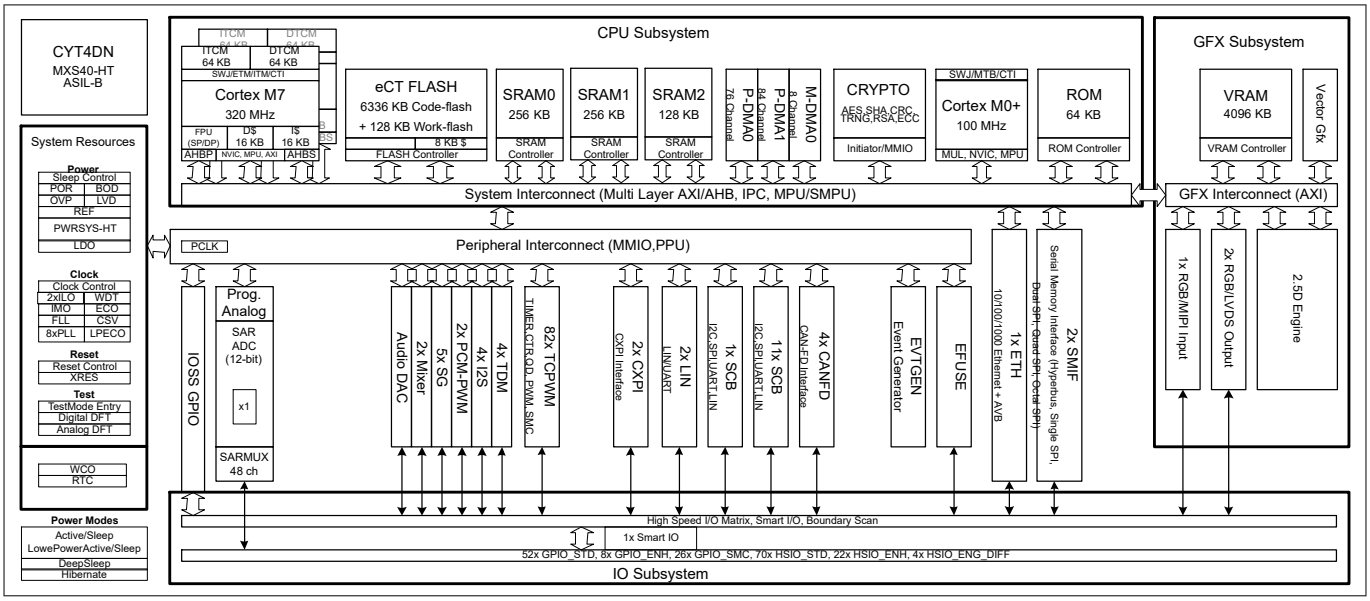


**Figure 11 Block Diagram (CYT4DN Series)**

## 3.3 On-chip System Features

### 3.3.1 CPU

TRAVEO™ T1G Family has a single Cortex-R5 processor, while TRAVEO™ T2G Family is a dual-processing CPU (two Cortex-M7s and a Cortex-M0+ processor). In TRAVEO™ T2G Family, dual-processing CPUs are configured as the CPU subsystem; two Cortex-M7 processors are the main CPU and Cortex-M0+ processor is the secondary CPU that can implement security, safety, and protection features. Note that as the CPU core changes, MCU features change according to the core specification.

**Table 43 Differences in CPU**

| Item | TRAVEO™ T1G Family (S6J3280 Series) | TRAVEO™ T2G Family (CYT4DN Series) | | Remarks |
|---|---|---|---|---|
| | | Main CPU | Secondary CPU | |
| CPU Core | Cortex-R5F | Cortex-M7 (x2) | Cortex-M0+ | |
| Operation Frequency | Up to 240 MHz | Up to 320 MHz | Up to 100 MHz | Product specifications |
| FPU | Single/Double precision | Single/Double precision | None | |
| MPU | 16 regions | 16 regions | 8 regions | *11)* |
| Cache Memory | I-cache 16 KB/D-cache 16 KB | I-cache 16 KB/D-cache 16 KB | None | |
| TCM Interface | Supported<br>Implemented TCRAM | Supported | Not supported | |

**(table continues...)**

11 TRAVEO™ T2G has SMPU as memory protection in addition to the CPU's internal MPU. Refer to Protection.

**Table 43 (continued) Differences in CPU**

| Item | TRAVEO™ T1G Family (S6J3280 Series) | TRAVEO™ T2G Family (CYT4DN Series) | | Remarks |
|---|---|---|---|---|
| | | Main CPU | Secondary CPU | |
| Support for Interrupt Controller | Vector Interrupt Controller (VIC),<br>Software nested interrupt | Nested Vector Interrupt Controller (NVIC) | | |

### 3.3.2 Memory Design

Table 44 lists the Code Flash features. The main differences are in program size, Read-While-Write operation, and redundancy.

**Table 44 Differences in Code Flash**

| Code Flash | S6J3280 Series | CYT4DN Series |
|---|---|---|
| ECC | SEC/DED | SEC/DED |
| Sector Size | 64 KB, 8 KB | 32 KB, 8 KB |
| Program Size | 8 bits, 16 bits, 32 bits, 64 bits | 64 bits, 256 bits, 4096 bits |
| Program and Erase Cycles/ Retention | 1000/20 years | 1000/20 years |
| Read-While-Write Operation | Not supported | Supported |

Table 45 lists the Work Flash features. The main differences are in the sector size, program and erase cycles, Read-While-Write operation, and redundancy. Comparing with TRAVEO, TRAVEO™ T2G families supports smaller sector size and higher program and erase cycles.

**Table 45 Differences in Work Flash**

| Work Flash | S6J3280 Series | CYT4DN Series |
|---|---|---|
| ECC | SEC/DED | SEC/DED |
| Sector Size | 4 KB | 2 KB, 128 B |
| Program Size | 32 bits | 32 bits |
| Program and Erase Cycles/ Retention | 1000/20 years<br>10000/10 years<br>100000/5 years | 125000/20 years<br>250000/10 years |
| Read-While-Write Operation | Not supported | Supported |

Table 46 lists the SRAM features. The main difference is the data retention in low power mode. TRAVEO™ T2G Family supports data retention in DeepSleep mode.

**Table 46 Differences in SRAM**

| SRAM | S6J3280 Series | CYT4DN Series |
|---|---|---|
| ECC | SEC/DED | SEC/DED |

**(table continues...)**

**Table 46 (continued) Differences in SRAM**

| SRAM | S6J3280 Series | CYT4DN Series |
|---|---|---|
| Data Retention in Low Power Mode | Not supported<br>(TCRAM and SRAM are not retained in Shutdown mode. Backup RAM is retained in Shutdown mode) | Supported<br>(SRAM is retained in DeepSleep mode) |

### 3.3.3 Debug

TRAVEO™ T1G and TRAVEO™ T2G families support JTAG and SWD Debug Interface. Table 47 shows the main differences in debugging.

**Table 47 Differences in Debugging**

| Item | S6J3280 Series | CYT4DN Series |
|---|---|---|
| Debug interface | JTAG | JTAG<br>SWD |

### 3.3.4 Mode Setting

This section is as same as the Body Entry/High Products. See section 2.3.4 Mode Setting.

### 3.3.5 Power Supply and Monitoring

The power supply of TRAVEO™ T2G Family is the same as that of TRAVEO™ T1G Family, but signal names of power supply are different. Also, the type of power monitoring mode has been enhanced in TRAVEO™ T2G Family.

#### 3.3.5.1 Power Supply

Table 48 lists the power supply and differences in functionality.

**Table 48 Power Supply**

| Power Supply | | S6J3280 Series | | CYT4DN Series | |
|---|---|---|---|---|---|
| External | Digital | $V_{CC5}$ | 4.5 to 5.5 V | $V_{DDD}$ | 2.7 to 5.5 V |
| | | $V_{CC12}$ | 1.1 to 1.3 V | $V_{CCD}$ | 1.09 to 1.21 V |
| | I/O | $V_{CC53}$ | 3.0 to 3.6 V/4.5 to 5.5 V | $V_{DDIO\_GPIO}$ | 2.7 to 5.5 V |
| | | $DV_{CC}$ | 4.5 to 5.5 V | $V_{DDIO\_SMC}$ | 2.7 to 5.5 V |
| | | $V_{CC3}$ | 3.0 to 3.6 V | $V_{DDIO\_HSIO}$ , $V_{DDIO\_SMIF\_HV}$ | 3.0 to 3.6 V |
| | | - | - | $V_{DDIO\_SMIF}$ | 1.7 to 2.0 V |
| | Analog | $AV_{CC3\_DAC}$ | | $V_{DDHA\_FPD0}$ , $V_{DDHA\_FPD1}$ | 3.0 to 3.6 V |
| | | $V_{CC3\_LVDS\_Tx}$ | | $V_{DDA\_FPD0}$ , $V_{DDA\_FPD1}$ | 1.09 to 1.21 V |

**(table continues...)**

**Table 48 (continued) Power Supply**

| Power Supply | | S6J3280 Series | | CYT4DN Series | |
|---|---|---|---|---|---|
| | | $V_{CC3\_LVDS\_PLL}$ | | $V_{DDPLL\_FPD0}$ , $V_{DDPLL\_FPD1}$ | 1.09 to 1.21 V |
| | | - | - | $V_{DDA\_MIPI}$ | 1.09 to 1.21 V |
| | | $AV_{CC5}$ | $AV_{CC5}$ | $V_{DDA\_ADC}$ | 2.7 to 5.5 V |

### 3.3.5.2 Monitoring

This section is as same as the Body Entry/High Products. See section 2.3.5.2 Monitoring .

## 3.3.6 Reset Factor

This section is as same as the Body Entry/High Products. See section 2.3.6 Reset Factor.

## 3.3.7 Clock System

Compared to the TRAVEO™ T1G Family clock system, TRAVEO™ T2G Family has Spread Spectrum Clock Generator (SSCG). TRAVEO™ T2G Family does not have Clock Gear functions. In TRAVEO™ T2G Family, frequency-locked loop (FLL) featuring fast startup and low power is implemented. LPECO that operates in DeepSleep and Hibernate mode is added. Table 49 lists the main differences in the clock system.

See the datasheet for the AC characteristics of each clock.

**Table 49 Differences in Clock System**

| Clock System | | S6J3200 Series | CYT4DN Series | CYT2C9 Series |
|---|---|---|---|---|
| Internal Clock Source | | Fast CR: 4 MHz(Using source clock after reset)<br>Slow CR: 100 kHz | IMO: 8 MHz(Using source clock after reset)<br>ILO0/1: 32 kHz | IMO: 8 MHz(Using source clock after reset)<br>ILO0/1: 32 kHz |
| External Clock Source | | Main clock: 3.6 to 16 MHz<br>Sub clock: 32.768 kHz | ECO: 3.988 to 33.33 MHz<br>WCO: 32.768 kHz<br>LPECO: 4 to 8MHz<br>EXT_CLK[12] : 0.25 to 100 MHz | ECO: 3.988 to 33.33 MHz<br>WCO: 32.768 kHz<br>LPECO: 4 to 8MHz<br>EXT_CLK[12] : 0.25 to 100 MHz |
| High-Speed Clock Generation | PLL | PLL x4<br>Input: 3.6 to 32 MHz<br>Output: max. 400 MHz (PLL1)<br>SSCG PLL x4<br>Input: 3.6 to 32 MHz<br>Output: max. 400 MHz (SSCG3) | PLL without SSCG x3<br>Input: 3.988 to 33.34 MHz<br>Output: max. 200 MHz<br>PLL with SSCG x5<br>Input: 3.988 to 33.34 MHz<br>Output: max. 400 MHz | PLL without SSCG x2<br>Input: 3.988 to 33.34 MHz<br>Output: max. 200 MHz<br>PLL with SSCG x1<br>Input: 3.988 to 33.34 MHz<br>Output: max. 400 MHz |

**(table continues...)**

12 It can be sourced from a designated I/O pin.

**Table 49 (continued) Differences in Clock System**

| Clock System | | S6J3200 Series | CYT4DN Series | CYT2C9 Series |
|---|---|---|---|---|
| | FLL | Not implemented | FLL x1<br>Input: 0.25 to 80 MHz<br>Output: 24 to 100 MHz | FLL x1<br>Input: 0.25 to 80 MHz<br>Output: 24 to 100 MHz |
| Clock Gear | | Supported | Not implemented | Not implemented |
| Clock Supervision | | Main clock<br>Sub clock<br>PLL clock<br>SSCG clock<br>Slow CR<br>Fast CR | CLK_REF (IMO or ECO or EXT_CLK)<br>CLK_HF (PLL and FLL)<br>ILO0<br>CLK_LF (ILO1 or WCO) | CLK_REF (IMO or ECO or EXT_CLK)<br>CLK_HF (PLL and FLL)<br>ILO0<br>CLK_LF (ILO1 or WCO) |

### 3.3.8 Watchdog Timer

The watchdog timer (hardware) features are same as the features listed in Table 13.

Table 50 lists the multi-counter watchdog timer (software) features. The main differences are counter clock, counter, maximum timeout, and the behavior during debugging.

**Table 50 Differences in Multi-Counter Watchdog Timer (Software)**

| Multi-counter Watchdog Timer (Software) | S6J3280 Series | CYT4DN Series |
|---|---|---|
| Trigger | User program | User program |
| Counter Clock | • Fast internal clock: 4 MHz<br>• Slow internal clock: 100 kHz<br>• Main clock: 4 to 16 MHz<br>• Sub clock: 32 kHz | • Internal low-speed oscillator: 32 kHz<br>• Watch crystal oscillator: 32 kHz<br>• ECO via Prescaler and Low Power External Clock Oscillator (LPECO) via Prescaler can also be used for MCWDT. |
| Counter | 32 bits | 2 * 16-bit, 32 bits only for interrupt |
| Maximum Timeout | 36.4 hours | 2.11 seconds |
| Window Function | Supported | Supported |
| Warning Interrupt | Supported | Supported |
| Timeout Expiration Action | Reset or NMI | Reset or Fault |
| Behavior During Low-Power Mode | Can select stop/run by register | Can select stop/run by register |
| Behavior During Debugging | Stop at debugging state | Can select stop/run by register |

### 3.3.9 Low Power Mode

This section is as same as the Body Entry/High Products. See section 2.3.9 Lower Power Mode.

### 3.3.10 Interrupt Structure

This section is as same as the Body Entry/High Products. See section 2.3.10 Interrupt Structure.

### 3.3.11 Data Transfer

This section is as same as the Body Entry/High Products. See section 2.3.11 Data Transfer .

### 3.3.12 TPU

This section is as same as the Body Entry/High Products. See section 2.3.12 TPU.

### 3.3.13 Fault Report

This section is as same as the Body Entry/High Products. See section 2.3.13 Fault Report.

### 3.3.14 Protection

The Protection function of TRAVEO™ T1G Family consists of the CPU's Memory Protection Unit (MPU), DMA's MPU, and Peripheral Protection Unit (PPU). TRAVEO™ T2G Family consists of MPU, Shared Memory Protection Unit (SMPU), and PPU. Table 51 lists the main differences in Protection Units.

In TRAVEO™ T2G Family, memory protection is provided by MPU and SMPU. MPU is implemented as part of the CPU and bus infrastructure. P-DMA, M-DMA, and encrypted components do not have MPU. Instead, they inherit the access control attributes of programmed bus transfer.

SMPU is shared by all masters; PPU is a protection unit for peripheral registers.

TRAVEO™ T2G Family supports a new protection attribute (Secure/Non-secure), and protection contexts. Protection contexts can change the access restriction without changing the setting of the protection unit.

For more details, see the Technical Reference Manual.

**Table 51 Differences in Protection Configuration and Access Attribute**

| Item | S6J3280 Series | CYT4DN Series | Remarks |
|---|---|---|---|
| MPU implemented in the CPU | Cortex-R5: 16 Regions<br>Access Attribute:<br>• Access Range<br>• Privileged/Unprivileged<br>• Read/Write<br>• Execute (Code or Data) | Cortex- M0+: 8 Regions<br>Cortex-M7: 16 Regions<br>Access Attribute:<br>• Access Range<br>• Privileged/Unprivileged<br>• Read/Write<br>• Execute (Code or Data) | |
| MPU implemented in the bus infrastructure | Not supported | 16 Regions<br>Access Attribute:<br>• Access Range<br>• Privileged/Unprivileged<br>• Read/Write<br>• Execute (Code or Data) | For external master such as debugger |

**(table continues...)**

**Table 51 (continued) Differences in Protection Configuration and Access Attribute**

| Item | S6J3280 Series | CYT4DN Series | Remarks |
|---|---|---|---|
| SMPU | Not supported | 16 Regions<br>Access Attribute:<br>• Access Range<br>• Privileged/Unprivileged<br>• Read/Write<br>• Execute (Code or Data)<br>• Secure/Non-secure<br>• Protection Contexts | |
| PPU | Access Attribute:<br>• USER/Privilege<br>• Read/Write | Access Attribute:<br>• Access Range<br>• Privileged/Unprivileged<br>• Read/Write<br>• Execute (Code or Data)<br>• Secure/Non-secure<br>• Protection Contexts | |
| MPU16-AHB | Access Attribute:<br>• Access range<br>• USER/Privilege<br>• Read/Write | Not supported.<br>DMA access protection is provided by SMPU and PPU. | |

### 3.3.15 Boot Process

This section is as same as the Body Entry/High Products. See section 2.3.15 Boot Process .

### 3.3.16 Security

This section is as same as the Body Entry/High Products. See section 2.3.16 Security .

## 3.4 Peripherals

### 3.4.1 Timer

This section is as same as the Body Entry/High Products. See section 2.4.1 Timer.

### 3.4.2 Serial Communication Block

#### 3.4.2.1 UART

This section is as same as the Body Entry/High Products. See section 2.4.2.1 UART .

#### 3.4.2.2 $I^2C$

This section is as same as the Body Entry/High Products. See section 2.4.2.2 $I^2C$ .

### 3.4.2.3 SPI

This section is as same as the Body Entry/High Products. See section 2.4.2.3 SPI .

### 3.4.2.4 LIN

This section is as same as the Body Entry/High Products. See section 2.4.2.4 LIN .

### 3.4.3 CAN FD

This section is as same as the Body Entry/High Products. See section 2.4.3 CAN FD.

### 3.4.4 I/O Interface

Table 52 lists the I/O interface features. The main differences are the input threshold selection, output drive strength selection, noise filter, and Smart IO.

**Table 52 Differences in I/O Interface**

| I/O Interface | S6J3280 Series | CYT4DN Series |
|---|---|---|
| Input Threshold Selection<br>• CMOS (0307)<br>• Automotive (0508)<br>• TTL | Supported except TTL | Supported |
| Output Drive Strength Selection | Supported<br>• 1 mA<br>• 2 mA<br>• 3 mA only for I2C<br>• 5 mA<br>• 6 mA only for MediaLB<br>• 10 mA / 20 mA only for 3 V I/O<br>• 30 mA only for SMC | Supported<br>• 0.1 mA only for HSIO_ENH<br>• 0.5 mA<br>• 1 mA<br>• 2 mA<br>• 3 mA only for HSIO_ENH<br>• 5 mA<br>• 6 mA only for GPIO (IOL)<br>• 10 mA only for HSIO_STD<br>• 30 mA only for GPIO_SMC |
| Pull-up / Pull-down | Supported<br>• 50 kΩ (typ) | Supported<br>• 50 kΩ (typ) |
| High-Z State | Supported | Supported |
| Port Status Hold during Low-Power Mode | Supported | Supported |
| Noise Filter | Supported per port pin<br>• Max 100 ns | Supported per port group<br>• Max 50 ns |
| Smart IO | Not supported | Supported |

### 3.4.5 ADC

This section is as same as the Body Entry/High Products. See section 2.4.5 ADC.

### 3.4.6 RTC

Table 53 lists the RTC features. The main differences are the source clock, interrupts, and the counters of half-second/month/year.

**Table 53 Differences of RTC**

| RTC | S6J3280 series | CYT4DN Series |
|---|---|---|
| Source Clock | Main clock oscillator (4 MHz)<br>Sub clock oscillator (32 kHz)<br>Internal low speed oscillator (100 kHz) | Watch Crystal oscillator (32 kHz)<br>Internal low speed oscillator (32 kHz)<br>Low Power External Clock oscillator |
| Half-second Counter | Supported | Not supported<br>• Event Generator can count less than a second. |
| Second Counter | Supported | Supported |
| Minute Counter | Supported | Supported |
| Hour Counter | Supported | Supported |
| Day Counter | Supported | Supported |
| Month Counter | Not supported | Supported |
| Year Counter | Not supported | Supported |
| Automatic Leap Year Correction | Not supported | Supported |
| Interrupt | Each counter (Day/Hour/Minute/Second/Half-second) | Two independent alarms (Month + Day + Hour + Minute + Second) |
| Calibration | Supported<br>• Automatic calibration by main clock | Supported<br>• Calibration by waveform output and software |

### 3.4.7 CRC

This section is as same as the Body Entry/High Products. See section 2.4.7 CRC.

### 3.4.8 CXPI

TRAVEO™ T2G Family has a CXPI module in CYT4DN and CYT2C9 series MCUs.

CXPI supports the following:

- CXPI protocol support in hardware according to ISO/WD 20794-4
- Master node
  - Autonomous request field and response transfer processing
- Network access method
  - Event-triggered method
  - Polling method
- Carrier sense multiple access and collision resolution (CSMA/CR)

- Data signal encoding/decoding format
  - Non-return to zero (NRZ) mode
  - Pulse width modulation (PWM) mode
- Wake pulse generation
- Clock detection
- 8-bit checksum for normal frame and 16-bit checksum for long frame
- 400x bit time oversampling
- Error detection
- Timeout detection
- Message buffers for the following:
  - Protected identifier (PID) field
  - Frame information (FI) field
  - 16x depth transmission and reception FIFO buffer
  - Checksum field
- Test modes include hardware error injection

### 3.4.9 Serial Memory Interface

TRAVEO™ T2G Family has SMIF only in CYT4DN Series MCUs.

SMIF provides an SPI master interface to serial memory devices that support a single, dual, or quad SPI protocol. SMIF provides the following functionalities:

- HyperBus protocol
- SPI mode 0: clock polarity (CPOL) and clock phase (CPHA) are both ‘0’.
- Support for single, dual, and quad SPI protocols.
- Support for dual-quad SPI mode: use of two quad SPI memory devices to increase data bandwidth for SPI read and write transfers.
- Support for single data rate (SDR) and dual data rate (DDR) transfers.
- Support for up to four external memory devices. Support for device capacities in the range of [64 KB, 4 GB] in power of 2 multiples.
- Execute-in-place (XIP) and memory-mapped input/output (MMIO) operation modes.
  - XIP operation mode supports both SPI read and write transfers.
- Support of a 4-KB XIP read cache in AHB-Lite Bus.
- XIP operation mode supports on-the-fly encryption for write data and on-the-fly decryption for read data.
- SPI interface logic supports stalling of SPI transfers to address back pressure on FIFOs.
- SPI interface logic supports an asynchronous SPI transmit and receive interface clock.
- SPI interface logic supports multiple interface receive clocks.
- SPI interface logic supports flexible external memory devices data signal connections.
- Supports Data Learning Pattern (DLP) function.

### 3.4.10 Ethernet

TRAVEO™ T2G Family has an Ethernet module only in CYT4DN Series MCUs.

Ethernet provides an interface to an external PHY to get Ethernet functionality. Ethernet provides the following functionalities:

- 10, 100, and 1000 Mbps full-duplex operation

- RGMII, RMII, and GMII interfaces supported
- AXI Interface (64-bit)
- Support for up four Tx and 1 Rx Priority queues
- Support for 802.1AS and 1588 precision clock synchronization protocol
- Support for 1588 one-step clock for Tx Sync frames
- Optional IEEE 1588 timestamp unit
- Support for 802.3az EEE
- Support for 802.1Qbb priority-based flow control
- Receive and transmit IP, TCP, and UDP checksum offload
- Automatic pad and CRC generation on transmitted frames
- MDIO interface for PHY management
- Supports 802.1Qav traffic shaping on two highest-priority transmit queues
- Supports strict priority, DWRR, or Enhanced Transmission Selection (ETS - 802.1Qaz) on transmit queues

### 3.4.11 Graphics Interface

Table 54 lists the Graphics interface features. TRAVEO™ T1G Family comes with highly-efficient 2D/3D graphics engines. TRAVEO™ T2G Family supports a 2D graphics engine. Both TRAVEO™ T1G and TRAVEO™ T2G families have features with advanced feature-sets for memory saving, safety, and high image quality to help manufacturers take advantage of the lower overall system costs.

**Table 54 Differences in Graphics Interface**

| Item | S6J3280 Series | CYT4DN Series |
|---|---|---|
| RSDS output | 1 unit available | Not available |
| LVDS (FPD-Link) output | 1 unit available | 2 units available single (max display size: 1920 x 720) or 1 unit available dual (max display size is 2880 x 1080) |
| DRGB output | 2 units available | 2 units available |
| ITU656, YUV, RGB video input | 1 unit available | 1 unit available |
| MIPI CSI-2 video input | Not available | 1 unit available |
| MediaLB | 1 unit available | Not available |
| Ethernet AVB | 1 unit available | 1 unit available |
| Graphics Engine | 2D graphics engine (2.5D effects)<br>3D graphics engine | 2D graphics engine (2.5D effects) |
| VRAM | 2048 KB | 4096 KB |

### 3.4.12 Audio Interface

Table 55 lists the Audio interface features. Both TRAVEO™ T1G and TRAVEO™ T2G families support Sound Processing.

**Table 55 Differences in Audio Interface**

| Item | TRAVEO™ T1G Family (S6J3200 Series) | TRAVEO™ T2G Family (CYT4DN Series) |
|---|---|---|
| PCMPWM | 1 unit available | 2 units available |
| TDM | Not Supported | 4 time-division multiplexing (TDM) Interface available |
| SG | 1 unit available | 1 unit available |
| SWFG | 1 unit available | Not available |
| Mixer | 2 units available | 2 units available |
| Audio DAC | Stereo 1ch available | Stereo 1ch available |
| $I^2S$ | 2 units available | 4 units available |

### 3.4.13 LCD Controller

TRAVEO™ T1G Family S6J3200 Series and TRAVEO™ T2G Family CYT2C9 Series have an LCD controller. Table 56 lists the differences in LCD Controller.

**Table 56 Differences in LCD Controller**

| Item | S6J3200 Series | CYT2C9 Series |
|---|---|---|
| Segments | Up to 32 segments (SEG) | Up to 32 segments (SEG) |
| Commons | 4 commons (COM) | 4 commons (COM) |
| Configurable Pin Assignment | Not Supported | Any GPIO pin can be configured as either COM or SEG. |
| Power Efficient Waveform | Not Supported | Type A (standard) and Type B (low-power) |
| Duty Drive | Duty Selection: 1/2, 1/3, and 1/4<br>Bias Selection: 1/2 and 1/3 | Duty Selection: 1/2, 1/3, and 1/4<br>Bias Selection: 1/2, 1/3, and Digital correlation |
| Static Drive | Supported | Not Supported |
| Device Power Modes | RUN/PSS timer | Active/Sleep/DeepSleep |
| Digital Contrast Control | Not Available | Available |

## 3.5 Development Tools and Flash Programming Tools

This section is as same as the Body Entry/High Products. See section 2.5 Development Tools and Flash Programming Tools.

## 3.6 MCAL Support

This section is as same as the Body Entry/High Products. See section 2.6 MCAL Support.

# 4 Related Documents

Body Entry/High Products:

TRAVEO™ T1G Family series datasheets and hardware manuals:

- https://www.cypress.com/node/502741 S6J3400 Series Datasheet
- S6J3 40 0 Series Hardware Manual
- TRAVEO™ T1G Family Hardware Manual Platform Part for S6J3400 Series

TRAVEO™ T2G Family series datasheets and technical reference manuals:

- Device datasheet (Contact Technical Support)
  - CYT2B7 Datasheet 32-Bit Arm® Cortex®-M4F Microcontroller TRAVEO™ II Family
  - CYT2B9 Datasheet 32-Bit Arm® Cortex®-M4F Microcontroller TRAVEO™ II Family
  - CYT4BF Datasheet 32-Bit Arm® Cortex®-M7 Microcontroller TRAVEO™ II Family
  - CYT3BB/4BB Datasheet 32-Bit Arm® Cortex®-M7 Microcontroller TRAVEO™ II Family
- Body Controller Entry Family (Contact Technical Support)
  - TRAVEO™ II Automotive Body Controller Entry Family Architecture Technical Reference Manual (TRM)
  - TRAVEO™ II Automotive Body Controller Entry Registers Technical Reference Manual (TRM) for CYT2B7
  - TRAVEO™ II Automotive Body Controller Entry Registers Technical Reference Manual (TRM) for CYT2B9
- Body Controller High Family (Contact Technical Support)
  - TRAVEO™ II Automotive Body Controller High Family Architecture Technical Reference Manual (TRM) for CYT4BF
  - TRAVEO™ II Automotive Body Controller High Registers Technical Reference Manual (TRM) for CYT3BB/4BB

Cluster Products:

TRAVEO™ T1G Family series datasheets and hardware manuals:

- S6J3200 Series Datasheet
- S6J3200 Series Hardware Manual
- TRAVEO™ T1G Family Hardware Manual Platform Part for S6J3200 Series

TRAVEO™ T2G Family series datasheets and technical reference manuals:

- Device datasheet (Contact Technical Support)
  - CYT4DN Datasheet 32-Bit Arm® Cortex®-M7 Microcontroller TRAVEO™ II Family
- Cluster 2D Family (Contact Technical Support)
  - TRAVEO™ II Automotive Cluster Family Architecture Technical Reference Manual (TRM)
  - TRAVEO™ II Automotive Cluster Registers Technical Reference Manual (TRM)

***Attention**:*

# Revision history

| Document version | Date of release | Description of changes |
|---|---|---|
| ** | 2017-12-19 | New application note. |
| *A | 2019-02-20 | Added items shown below:<br>Figure 2 and Figure 3 of the Section “2.1. Block Diagram”,<br>Section “2.1 Features Specific Functions of TRAVEO™ T2G Family MCUs”,<br>Section “4.8 CXPI” and Part Numbers of CYT2B9 Series MCU,<br>Section “4.9 FlexRay”, “4.10 Secure Digital Host Controller”, “4.11 Serial Memory Interface”, “4.12 Ethernet” and Part Numbers of CYT4BF Series MCU |
| *B | 2019-08-08 | Added Cluster Products Specifications. |
| *C | 2020-03-23 | Added items shown below:<br>TRAVEO™ T2G Family Cluster Products of the “Table 1. MCU List for Comparison”.<br>Expanded Target Products for Cluster Entry series following tables at “3. Cluster Products”:<br>Table 41. Target Products,<br>Table 42. Comparison of TRAVEO™ T1G and TRAVEO™ T2G Family MCUs, and<br>Table 48. Differences in Clock System. |
| *D | 2021-03-18 | Updated to Infineon template. |
| *E | 2023-11-10 | Updated template; no content update. |

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