

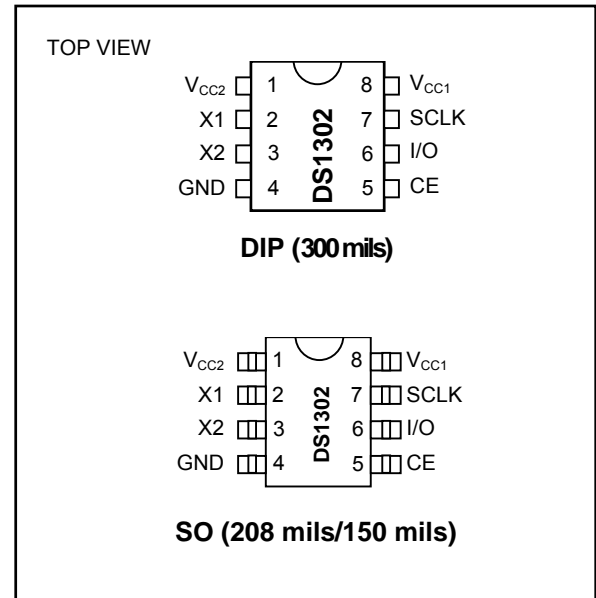
DS1302 Trickle-Charge Timekeeping Chip

www.maxim-ic.com

FEATURES

- Real-Time Clock Counts Seconds, Minutes, Hours, Date of the Month, Month, Day of the Week, and Year with Leap-Year Compensation Valid Up to 2100
- 31 x 8 Battery-Backed General-Purpose RAM
- Serial I/O for Minimum Pin Count
- 2.0V to 5.5V Full Operation
- Uses Less than 300nA at 2.0V
- Single-Byte or Multiple-Byte (Burst Mode) Data Transfer for Read or Write of Clock or RAM Data
- 8-Pin DIP or Optional 8-Pin SO for Surface Mount
- Simple 3-Wire Interface
- TTL-Compatible ($V_{CC} = 5V$)
- Optional Industrial Temperature Range: $-40^{\circ}C$ to $+85^{\circ}C$
- DS1202 Compatible
- Underwriters Laboratories (UL®) Recognized

PIN CONFIGURATIONS



ORDERING INFORMATION

| PART | TEMP RANGE | PIN-PACKAGE | TOP MARK* |
|-----------|----------------------------------|-------------------|-----------|
| DS1302+ | $0^{\circ}C$ to $+70^{\circ}C$ | 8 PDIP (300 mils) | DS1302 |
| DS1302N+ | $-40^{\circ}C$ to $+85^{\circ}C$ | 8 PDIP (300 mils) | DS1302 |
| DS1302S+ | $0^{\circ}C$ to $+70^{\circ}C$ | 8 SO (208 mils) | DS1302S |
| DS1302SN+ | $-40^{\circ}C$ to $+85^{\circ}C$ | 8 SO (208 mils) | DS1302S |
| DS1302Z+ | $0^{\circ}C$ to $+70^{\circ}C$ | 8 SO (150 mils) | DS1302Z |
| DS1302ZN+ | $-40^{\circ}C$ to $+85^{\circ}C$ | 8 SO (150 mils) | DS1302ZN |

+Denotes a lead-free/RoHS-compliant package.

*An N anywhere on the top mark indicates an industrial temperature grade device. A + anywhere on the top mark indicates a lead-free device.

UL is a registered trademark of Underwriters Laboratories, Inc.

DETAILED DESCRIPTION

The DS1302 trickle-charge timekeeping chip contains a real-time clock/calendar and 31 bytes of static RAM. It communicates with a microprocessor via a simple serial interface. The real-time clock/calendar provides seconds, minutes, hours, day, date, month, and year information. The end of the month date is automatically adjusted for months with fewer than 31 days, including corrections for leap year. The clock operates in either the 24-hour or 12-hour format with an AM/PM indicator.

Interfacing the DS1302 with a microprocessor is simplified by using synchronous serial communication. Only three wires are required to communicate with the clock/RAM: CE, I/O (data line), and SCLK (serial clock). Data can be transferred to and from the clock/RAM 1 byte at a time or in a burst of up to 31 bytes. The DS1302 is designed to operate on very low power and retain data and clock information on less than 1 μ W.

The DS1302 is the successor to the DS1202. In addition to the basic timekeeping functions of the DS1202, the DS1302 has the additional features of dual power pins for primary and backup power supplies, programmable trickle charger for V_{CC1} , and seven additional bytes of scratchpad memory.

OPERATION

Figure 1 shows the main elements of the serial timekeeper: shift register, control logic, oscillator, real-time clock, and RAM.

TYPICAL OPERATING CIRCUIT

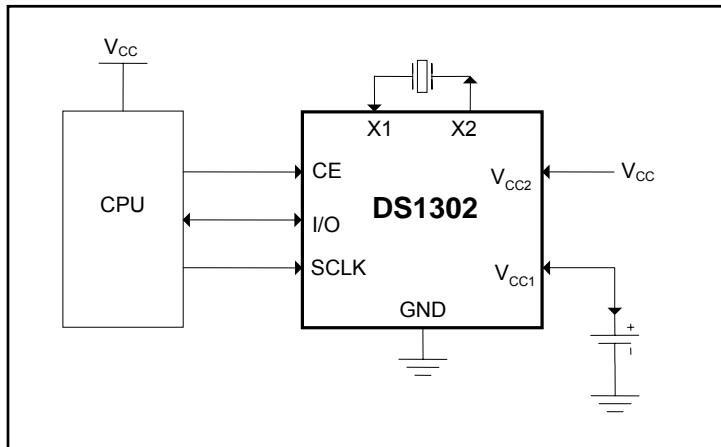
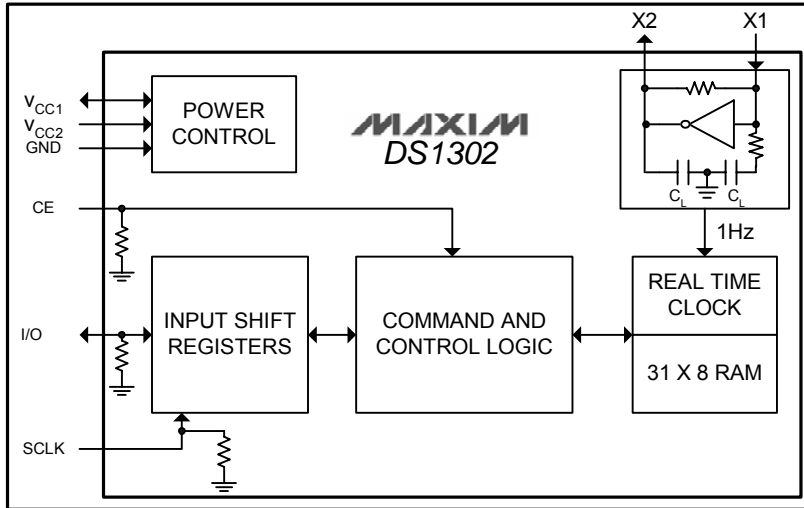
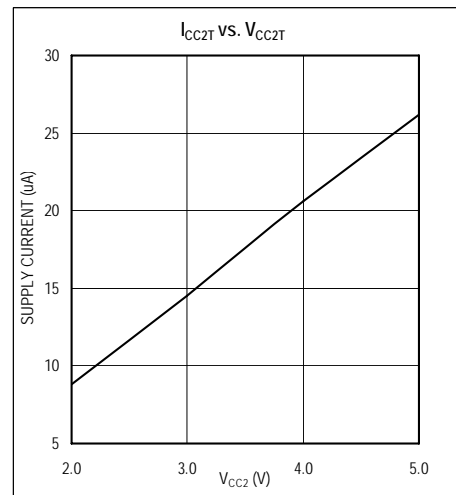
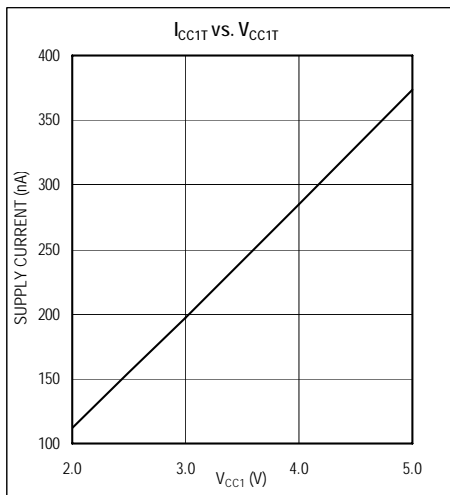


Figure 1. Block Diagram**TYPICAL OPERATING CHARACTERISTICS**

($V_{CC} = 3.3V$, $T_A = +25^\circ C$, unless otherwise noted.)



PIN DESCRIPTION

| PIN | NAME | FUNCTION |
|-----|------------------|---|
| 1 | V _{CC2} | Primary Power-Supply Pin in Dual Supply Configuration. V _{CC1} is connected to a backup source to maintain the time and date in the absence of primary power. The DS1302 operates from the larger of V _{CC1} or V _{CC2} . When V _{CC2} is greater than V _{CC1} + 0.2V, V _{CC2} powers the DS1302. When V _{CC2} is less than V _{CC1} , V _{CC1} powers the DS1302. |
| 2 | X1 | Connections for Standard 32.768kHz Quartz Crystal. The internal oscillator is designed for operation with a crystal having a specified load capacitance of 6pF. For more information on crystal selection and crystal layout considerations, refer to <i>Application Note 58: Crystal Considerations for Dallas Real-Time Clocks</i> . The DS1302 can also be driven by an external 32.768kHz oscillator. In this configuration, the X1 pin is connected to the external oscillator signal and the X2 pin is floated. |
| 3 | X2 | |
| 4 | GND | Ground |
| 5 | CE | Input. CE signal must be asserted high during a read or a write. This pin has an internal 40kΩ (typ) pulldown resistor to ground. Note: Previous data sheet revisions referred to CE as $\overline{\text{RST}}$. The functionality of the pin has not changed. |
| 6 | I/O | Input/Push-Pull Output. The I/O pin is the bidirectional data pin for the 3-wire interface. This pin has an internal 40kΩ (typ) pulldown resistor to ground. |
| 7 | SCLK | Input. SCLK is used to synchronize data movement on the serial interface. This pin has an internal 40kΩ (typ) pulldown resistor to ground. |
| 8 | V _{CC1} | Low-Power Operation in Single Supply and Battery-Operated Systems and Low-Power Battery Backup. In systems using the trickle charger, the rechargeable energy source is connected to this pin. UL recognized to ensure against reverse charging current when used with a lithium battery. Go to www.maxim-ic.com/TechSupport/QA/ntrl.htm . |

OSCILLATOR CIRCUIT

The DS1302 uses an external 32.768kHz crystal. The oscillator circuit does not require any external resistors or capacitors to operate. Table 1 specifies several crystal parameters for the external crystal. Figure 1 shows a functional schematic of the oscillator circuit. If using a crystal with the specified characteristics, the startup time is usually less than one second.

CLOCK ACCURACY

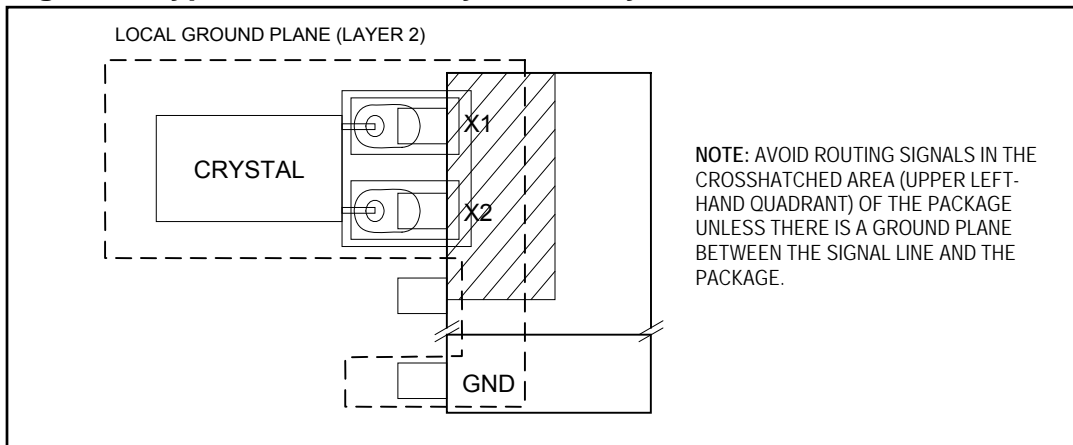
The accuracy of the clock is dependent upon the accuracy of the crystal and the accuracy of the match between the capacitive load of the oscillator circuit and the capacitive load for which the crystal was trimmed. Additional error will be added by crystal frequency drift caused by temperature shifts. External circuit noise coupled into the oscillator circuit may result in the clock running fast. Figure 2 shows a typical PC board layout for isolating the crystal and oscillator from noise. Refer to *Application Note 58: Crystal Considerations for Dallas Real-Time Clocks* for detailed information.

Table 1. Crystal Specifications*

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS |
|-------------------|--------|-----|--------|-----|-----------|
| Nominal Frequency | f_0 | | 32.768 | | kHz |
| Series Resistance | ESR | | | 45 | $k\Omega$ |
| Load Capacitance | C_L | | 6 | | pF |

*The crystal, traces, and crystal input pins should be isolated from RF generating signals. Refer to Application Note 58: Crystal Considerations for Dallas Real-Time Clocks for additional specifications.

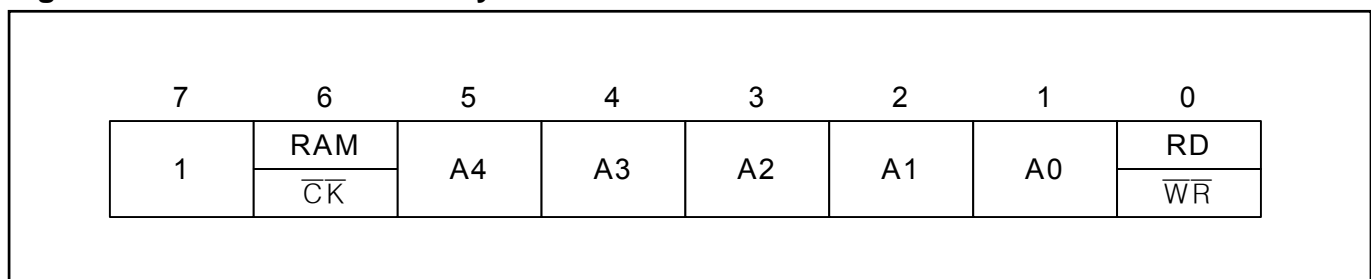
Figure 2. Typical PC Board Layout for Crystal



COMMAND BYTE

Figure 3 shows the command byte. A command byte initiates each data transfer. The MSB (bit 7) must be a logic 1. If it is 0, writes to the DS1302 will be disabled. Bit 6 specifies clock/calendar data if logic 0 or RAM data if logic 1. Bits 1 to 5 specify the designated registers to be input or output, and the LSB (bit 0) specifies a write operation (input) if logic 0 or read operation (output) if logic 1. The command byte is always input starting with the LSB (bit 0).

Figure 3. Address/Command Byte



CE AND CLOCK CONTROL

Driving the CE input high initiates all data transfers. The CE input serves two functions. First, CE turns on the control logic that allows access to the shift register for the address/command sequence. Second, the CE signal provides a method of terminating either single-byte or multiple-byte CE data transfer.

A clock cycle is a sequence of a rising edge followed by a falling edge. For data inputs, data must be valid during the rising edge of the clock and data bits are output on the falling edge of clock. If the CE input is low, all data transfer terminates and the I/O pin goes to a high-impedance state. Figure 4 shows data transfer. At power-up, CE must be a logic 0 until $V_{CC} > 2.0V$. Also, SCLK must be at a logic 0 when CE is driven to a logic 1 state.

DATA INPUT

Following the eight SCLK cycles that input a write command byte, a data byte is input on the rising edge of the next eight SCLK cycles. Additional SCLK cycles are ignored should they inadvertently occur. Data is input starting with bit 0.

DATA OUTPUT

Following the eight SCLK cycles that input a read command byte, a data byte is output on the falling edge of the next eight SCLK cycles. Note that the first data bit to be transmitted occurs on the first falling edge after the last bit of the command byte is written. Additional SCLK cycles retransmit the data bytes should they inadvertently occur so long as CE remains high. This operation permits continuous burst mode read capability. Also, the I/O pin is tri-stated upon each rising edge of SCLK. Data is output starting with bit 0.

BURST MODE

Burst mode can be specified for either the clock/calendar or the RAM registers by addressing location 31 decimal (address/command bits 1 through 5 = logic 1). As before, bit 6 specifies clock or RAM and bit 0 specifies read or write. There is no data storage capacity at locations 9 through 31 in the Clock/Calendar Registers or location 31 in the RAM registers. Reads or writes in burst mode start with bit 0 of address 0.

When writing to the clock registers in the burst mode, the first eight registers must be written in order for the data to be transferred. However, when writing to RAM in burst mode it is not necessary to write all 31 bytes for the data to transfer. Each byte that is written to will be transferred to RAM regardless of whether all 31 bytes are written or not.

CLOCK/CALENDAR

The time and calendar information is obtained by reading the appropriate register bytes. Table 3 illustrates the RTC registers. The time and calendar are set or initialized by writing the appropriate register bytes. The contents of the time and calendar registers are in the binary-coded decimal (BCD) format.

The day-of-week register increments at midnight. Values that correspond to the day of week are user-defined but must be sequential (i.e., if 1 equals Sunday, then 2 equals Monday, and so on.). Illogical time and date entries result in undefined operation.

When reading or writing the time and date registers, secondary (user) buffers are used to prevent errors when the internal registers update. When reading the time and date registers, the user buffers are synchronized to the internal registers the rising edge of CE.

The countdown chain is reset whenever the seconds register is written. Write transfers occur on the falling edge of CE. To avoid rollover issues, once the countdown chain is reset, the remaining time and date registers must be written within 1 second.

The DS1302 can be run in either 12-hour or 24-hour mode. Bit 7 of the hours register is defined as the 12- or 24-hour mode-select bit. When high, the 12-hour mode is selected. In the 12-hour mode, bit 5 is the \overline{AM}/PM bit with logic high being PM. In the 24-hour mode, bit 5 is the second 10-hour bit (20–23 hours). The hours data must be re-initialized whenever the 12/24 bit is changed.

CLOCK HALT FLAG

Bit 7 of the seconds register is defined as the clock halt (CH) flag. When this bit is set to logic 1, the clock oscillator is stopped and the DS1302 is placed into a low-power standby mode with a current drain of less than 100nA. When this bit is written to logic 0, the clock will start. The initial power-on state is not defined.

WRITE-PROTECT BIT

Bit 7 of the control register is the write-protect bit. The first seven bits (bits 0 to 6) are forced to 0 and always read 0 when read. Before any write operation to the clock or RAM, bit 7 must be 0. When high, the write-protect bit prevents a write operation to any other register. The initial power-on state is not defined. Therefore, the WP bit should be cleared before attempting to write to the device.

TRICKLE-CHARGE REGISTER

This register controls the trickle-charge characteristics of the DS1302. The simplified schematic of Figure 5 shows the basic components of the trickle charger. The trickle-charge select (TCS) bits (bits 4 to 7) control the selection of the trickle charger. To prevent accidental enabling, only a pattern of 1010 enables the trickle charger. All other patterns will disable the trickle charger. The DS1302 powers up with the trickle charger disabled. The diode select (DS) bits (bits 2 and 3) select whether one diode or two diodes are connected between V_{CC2} and V_{CC1} . If DS is 01, one diode is selected or if DS is 10, two diodes are selected. If DS is 00 or 11, the trickle charger is disabled independently of TCS. The RS bits (bits 0 and 1) select the resistor that is connected between V_{CC2} and V_{CC1} . The resistor and diodes are selected by the RS and DS bits as shown in Table 2.

Table 2. Trickle Charger Resistor and Diode Select

| TCS BIT 7 | TCS BIT 6 | TCS BIT 5 | TCS BIT 4 | DS BIT 3 | DS BIT 2 | RS BIT 1 | RS BIT 0 | FUNCTION |
|--------------|--------------|--------------|--------------|-------------|-------------|-------------|-------------|------------------------|
| X | X | X | X | X | X | 0 | 0 | Disabled |
| X | X | X | X | 0 | 0 | X | X | Disabled |
| X | X | X | X | 1 | 1 | X | X | Disabled |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 Diode, 2k Ω |
| 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 Diode, 4k Ω |
| 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 Diode, 8k Ω |
| 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 2 Diodes, 2k Ω |
| 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 2 Diodes, 4k Ω |
| 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 2 Diodes, 8k Ω |
| 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | Initial power-on state |

Diode and resistor selection is determined by the user according to the maximum current desired for battery or super cap charging. The maximum charging current can be calculated as illustrated in the following example. Assume that a system power supply of 5V is applied to V_{CC2} and a super cap is connected to V_{CC1} . Also assume that the trickle charger has been enabled with one diode and resistor R1 between V_{CC2} and V_{CC1} . The maximum current I_{MAX} would therefore be calculated as follows:

$$I_{MAX} = (5.0V - \text{diode drop}) / R1 \approx (5.0V - 0.7V) / 2k\Omega \approx 2.2mA$$

As the super cap charges, the voltage drop between V_{CC2} and V_{CC1} decreases and therefore the charge current decreases.

CLOCK/CALENDAR BURST MODE

The clock/calendar command byte specifies burst mode operation. In this mode, the first eight clock/calendar registers can be consecutively read or written (see Table 3) starting with bit 0 of address 0.

If the write-protect bit is set high when a write clock/calendar burst mode is specified, no data transfer will occur to any of the eight clock/calendar registers (this includes the control register). The trickle charger is not accessible in burst mode.

At the beginning of a clock burst read, the current time is transferred to a second set of registers. The time information is read from these secondary registers, while the clock may continue to run. This eliminates the need to re-read the registers in case of an update of the main registers during a read.

RAM

The static RAM is 31 x 8 bytes addressed consecutively in the RAM address space.

RAM BURST MODE

The RAM command byte specifies burst mode operation. In this mode, the 31 RAM registers can be consecutively read or written (see Table 3) starting with bit 0 of address 0.

REGISTER SUMMARY

A register data format summary is shown in Table 3.

CRYSTAL SELECTION

A 32.768kHz crystal can be directly connected to the DS1302 via pins 2 and 3 (X1, X2). The crystal selected for use should have a specified load capacitance (C_L) of 6pF. For more information on crystal selection and crystal layout consideration, refer to *Application Note 58: Crystal Considerations for Dallas Real-Time Clocks*.

Figure 4. Data Transfer Summary

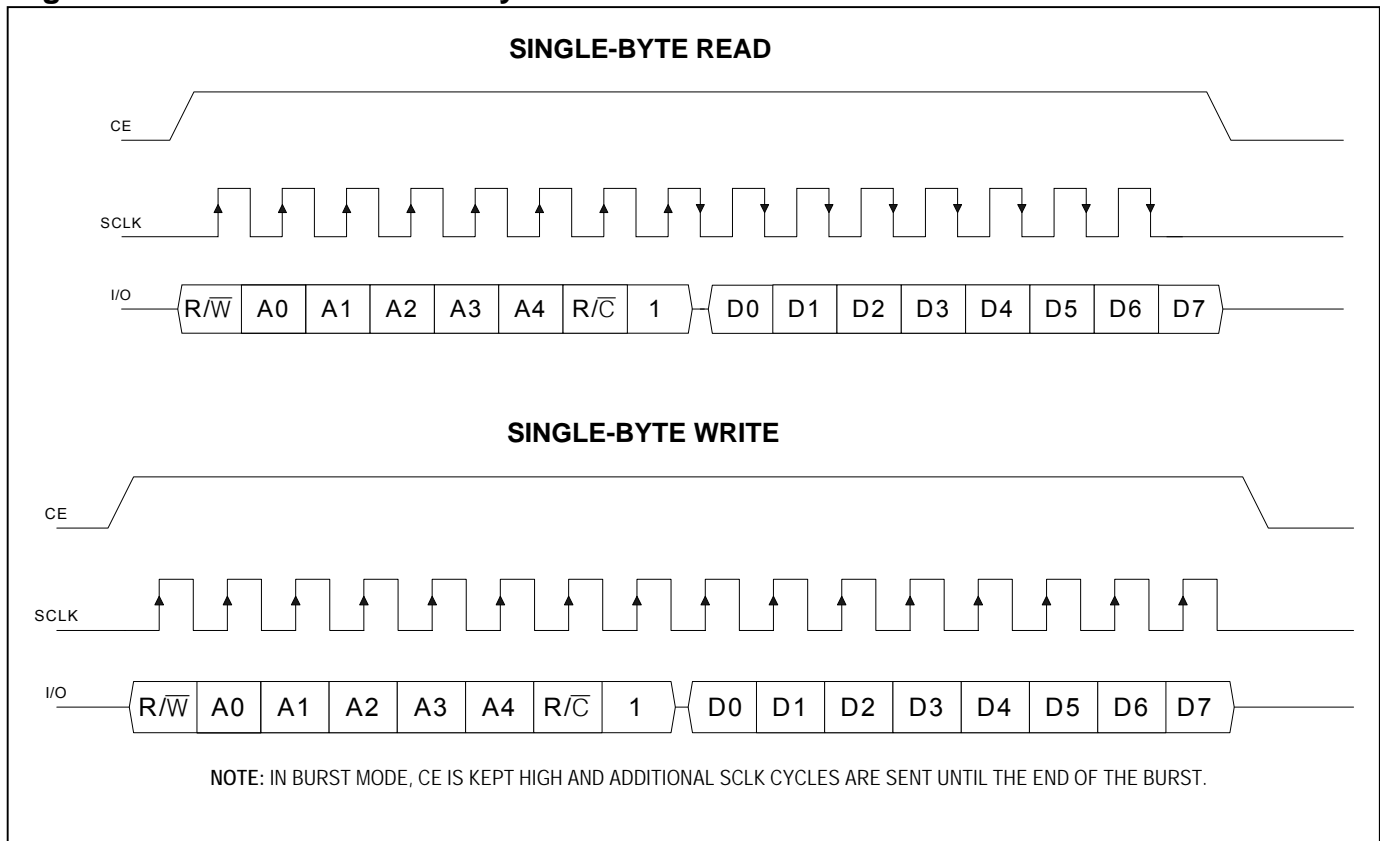


Table 3. Register Address/Definition**RTC**

| READ | WRITE | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 | RANGE |
|------|-------|---------|------------|-------------|-------------|---------|-------|-------|-------|-----------|
| 81h | 80h | CH | 10 Seconds | | | Seconds | | | | 00–59 |
| 83h | 82h | | 10 Minutes | | | Minutes | | | | 00–59 |
| 85h | 84h | 12/24 | 0 | 10 AM/PM | Hour | Hour | | | | 1–12/0–23 |
| 87h | 86h | 0 | 0 | 10 Date | | Date | | | | 1–31 |
| 89h | 88h | 0 | 0 | 0 | 10 Month | Month | | | | 1–12 |
| 8Bh | 8Ah | 0 | 0 | 0 | 0 | 0 | Day | | | 1–7 |
| 8Dh | 8Ch | 10 Year | | | | Year | | | | 00–99 |
| 8Fh | 8Eh | WP | 0 | 0 | 0 | 0 | 0 | 0 | 0 | — |
| 91h | 90h | TCS | TCS | TCS | TCS | DS | DS | RS | RS | — |

CLOCK BURST

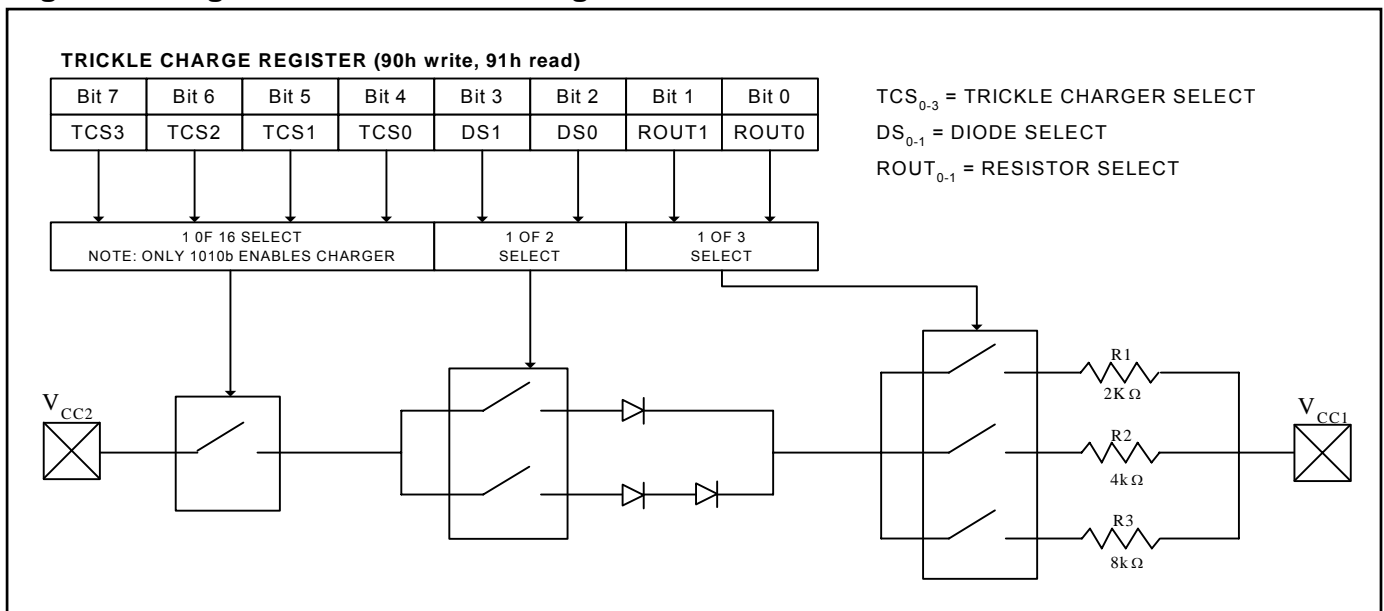
| | |
|-----|-----|
| BFh | BEh |
|-----|-----|

RAM

| | | | |
|-----|-----|--|--------|
| C1h | C0h | | 00–FFh |
| C3h | C2h | | 00–FFh |
| C5h | C4h | | 00–FFh |
| . | . | | . |
| . | . | | . |
| . | . | | . |
| FDh | FCh | | 00–FFh |

RAM BURST

| | |
|-----|-----|
| FFh | FEh |
|-----|-----|

Figure 5. Programmable Trickle Charger

ABSOLUTE MAXIMUM RATINGS

| | |
|--|-------------------------|
| Voltage Range on Any Pin Relative to Ground..... | -0.5V to +7.0V |
| Operating Temperature Range, Commercial..... | 0°C to +70°C |
| Operating Temperature Range, Industrial (IND)..... | -40°C to +85°C |
| Storage Temperature Range..... | -55°C to +125°C |
| Soldering Temperature (leads, 10 seconds)..... | 260°C |
| Soldering Temperature (surface mount)..... | See IPC/JEDEC J-STD-020 |

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

($T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$ or $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--------------------------------------|--------------------------|------------------------|------|-----|----------------|-------|
| Supply Voltage V_{CC1} , V_{CC2} | V_{CC1} , V_{CC2} | (Notes 2, 10) | 2.0 | 3.3 | 5.5 | V |
| Logic 1 Input | V_{IH} | (Note 2) | 2.0 | | $V_{CC} + 0.3$ | V |
| Logic 0 Input | V_{IL} | $V_{CC} = 2.0\text{V}$ | -0.3 | | +0.3 | V |
| | | $V_{CC} = 5\text{V}$ | -0.3 | | +0.8 | |

DC ELECTRICAL CHARACTERISTICS

($T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$ or $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|------------|-------------------------|-----|------|-------|---------------|
| Input Leakage | I_{LI} | (Notes 5, 13) | | 85 | 500 | μA |
| I/O Leakage | I_{LO} | (Notes 5, 13) | | 85 | 500 | μA |
| Logic 1 Output ($I_{OH} = -0.4\text{mA}$) | V_{OH} | $V_{CC} = 2.0\text{V}$ | 1.6 | | | V |
| Logic 1 Output ($I_{OH} = -1.0\text{mA}$) | | $V_{CC} = 5\text{V}$ | 2.4 | | | |
| Logic 0 Output ($I_{OL} = 1.5\text{mA}$) | V_{OL} | $V_{CC} = 2.0\text{V}$ | | | 0.4 | V |
| Logic 0 Output ($I_{OL} = 4.0\text{mA}$) | | $V_{CC} = 5\text{V}$ | | | 0.4 | |
| Active Supply Current (Oscillator Enabled) | I_{CC1A} | $V_{CC1} = 2.0\text{V}$ | | | 0.4 | mA |
| | | $V_{CC1} = 5\text{V}$ | | | 1.2 | |
| Timekeeping Current (Oscillator Enabled) | I_{CC1T} | $V_{CC1} = 2.0\text{V}$ | | 0.2 | 0.3 | μA |
| | | $V_{CC1} = 5\text{V}$ | | 0.45 | 1 | |
| Standby Current (Oscillator Disabled) | I_{CC1S} | $V_{CC1} = 2.0\text{V}$ | | 1 | 100 | nA |
| | | $V_{CC1} = 5\text{V}$ | | 1 | 100 | |
| | | IND | | 5 | 200 | |
| Active Supply Current (Oscillator Enabled) | I_{CC2A} | $V_{CC2} = 2.0\text{V}$ | | | 0.425 | mA |
| | | $V_{CC2} = 5\text{V}$ | | | 1.28 | |
| Timekeeping Current (Oscillator Enabled) | I_{CC2T} | $V_{CC2} = 2.0\text{V}$ | | | 25.3 | μA |
| | | $V_{CC2} = 5\text{V}$ | | | 81 | |
| Standby Current (Oscillator Disabled) | I_{CC2S} | $V_{CC2} = 2.0\text{V}$ | | | 25 | μA |
| | | $V_{CC2} = 5\text{V}$ | | | 80 | |
| Trickle-Charge Resistors | R1 | | | 2 | | k Ω |
| | R2 | | | 4 | | |
| | R3 | | | 8 | | |
| Trickle-Charge Diode Voltage Drop | V_{TD} | | | 0.7 | | V |

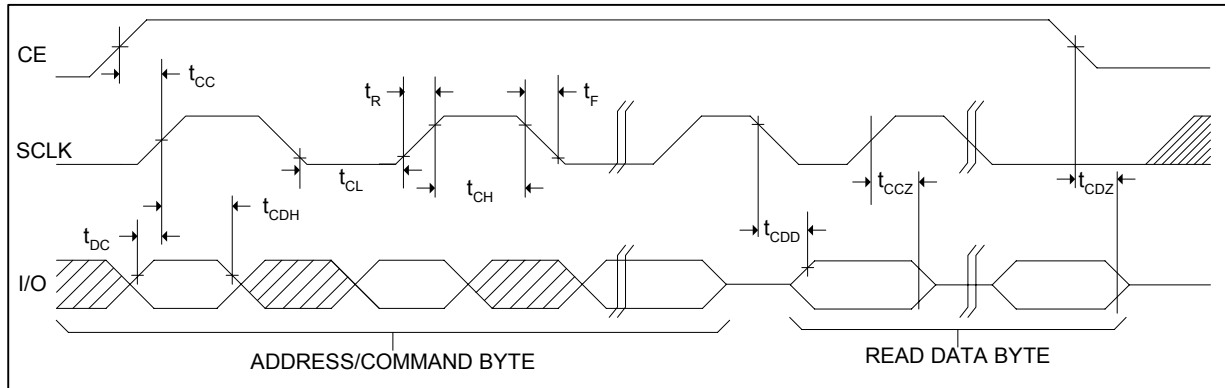
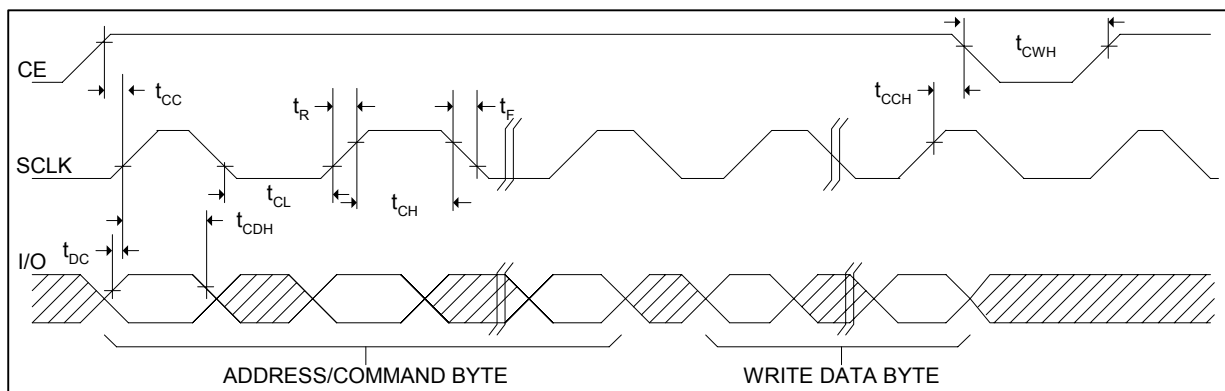
CAPACITANCE(T_A = +25°C)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS |
|-------------------|------------------|-----|-----|-----|-------|
| Input Capacitance | C _I | | 10 | | pF |
| I/O Capacitance | C _{I/O} | | 15 | | pF |

AC ELECTRICAL CHARACTERISTICS(T_A = 0°C to +70°C or T_A = -40°C to +85°C.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|----------------------------|---------------------------------|--|-----------------|-------------|------------------|-------|
| Data to CLK Setup | t _{DC} | V _{CC} = 2.0V V _{CC} = 5V | (Note 6) | 200 50 | | ns |
| CLK to Data Hold | t _{CDH} | V _{CC} = 2.0V V _{CC} = 5V | (Note 6) | 280 70 | | ns |
| CLK to Data Delay | t _{CDD} | V _{CC} = 2.0V V _{CC} = 5V | (Notes 6, 7, 8) | | 800 200 | ns |
| CLK Low Time | t _{CL} | V _{CC} = 2.0V V _{CC} = 5V | (Note 6) | 1000 250 | | ns |
| CLK High Time | t _{CH} | V _{CC} = 2.0V V _{CC} = 5V | (Note 6) | 1000 250 | | ns |
| CLK Frequency | t _{CLK} | V _{CC} = 2.0V V _{CC} = 5V | (Note 6) | | 0.5 2.0 DC | MHz |
| CLK Rise and Fall | t _R , t _F | V _{CC} = 2.0V V _{CC} = 5V | | | 2000 500 | ns |
| CE to CLK Setup | t _{CC} | V _{CC} = 2.0V V _{CC} = 5V | (Note 6) | 4 1 | | μs |
| CLK to CE Hold | t _{CCH} | V _{CC} = 2.0V V _{CC} = 5V | (Note 6) | 240 60 | | ns |
| CE Inactive Time | t _{CWH} | V _{CC} = 2.0V V _{CC} = 5V | (Note 6) | 4 1 | | μs |
| CE to I/O High Impedance | t _{CDZ} | V _{CC} = 2.0V V _{CC} = 5V | (Note 6) | | 280 70 | ns |
| SCLK to I/O High Impedance | t _{CCZ} | V _{CC} = 2.0V V _{CC} = 5V | (Note 6) | | 280 70 | ns |

Note 1: Limits at -40°C are guaranteed by design and are not production tested.**Note 2:** All voltages are referenced to ground.**Note 3:** I_{CC1T} and I_{CC2T} are specified with I/O open, CE and SCLK set to a logic 0.**Note 4:** I_{CC1A} and I_{CC2A} are specified with the I/O pin open, CE high, SCLK = 2MHz at V_{CC} = 5V; SCLK = 500kHz, V_{CC} = 2.0V.**Note 5:** CE, SCLK, and I/O all have 40kΩ pulldown resistors to ground.**Note 6:** Measured at V_{IH} = 2.0V or V_{IL} = 0.8V and 10ns maximum rise and fall time.**Note 7:** Measured at V_{OH} = 2.4V or V_{OL} = 0.4V.**Note 8:** Load capacitance = 50pF.**Note 9:** I_{CC1S} and I_{CC2S} are specified with CE, I/O, and SCLK open.**Note 10:** V_{CC} = V_{CC2}, when V_{CC2} > V_{CC1} + 0.2V; V_{CC} = V_{CC1}, when V_{CC1} > V_{CC2}.**Note 11:** V_{CC2} = 0V.**Note 12:** V_{CC1} = 0V.**Note 13:** Typical values are at +25°C.

Figure 6. Timing Diagram: Read Data Transfer**Figure 7. Timing Diagram: Write Data Transfer****CHIP INFORMATION**

TRANSISTOR COUNT: 11,500

THERMAL INFORMATION

| PACKAGE | THETA-JA (°C/W) | THETA-JC (°C/W) |
|-----------------|--------------------|--------------------|
| 8 DIP | 110 | 40 |
| 8 SO (150 mils) | 170 | 40 |

PACKAGE INFORMATIONFor the latest package outline information and land patterns, go to www.maxim-ic.com/packages.

| PACKAGE TYPE | PACKAGE CODE | DOCUMENT NO. |
|-----------------|--------------|-------------------------|
| 8 PDIP | — | 21-0043 |
| 8 SO (208 mils) | — | 21-0262 |
| 8 SO (150 mils) | — | 21-0041 |

REVISION HISTORY

| REVISION DATE | DESCRIPTION | PAGES CHANGED |
|------------------|---|------------------|
| 120208 | Removed the leaded parts and references to the 16-pin SO package. | 1, 4, 12 |
| | In the <i>Features</i> section, changed the 31 x 8 RAM feature to indicate that it is battery backed. | 1 |
| | Updated Figure 1 and removed original Figure 2 (oscillator circuit). | 3, 5 |
| | Added a new Table 2 for the trickle charger resistor and diode select. | 7 |
| | Replaced the timing diagrams (Figures 6 and 7). | 12 |
| | Added <i>Package Information</i> table. | 12 |