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Section: BCS-2D

Assignment NO: DLD LAB ASSIGNMENT 10

Submitted To Respected Maam: Anam

Lab 10

To Design and Implement Multiplexer & Demultiplexer

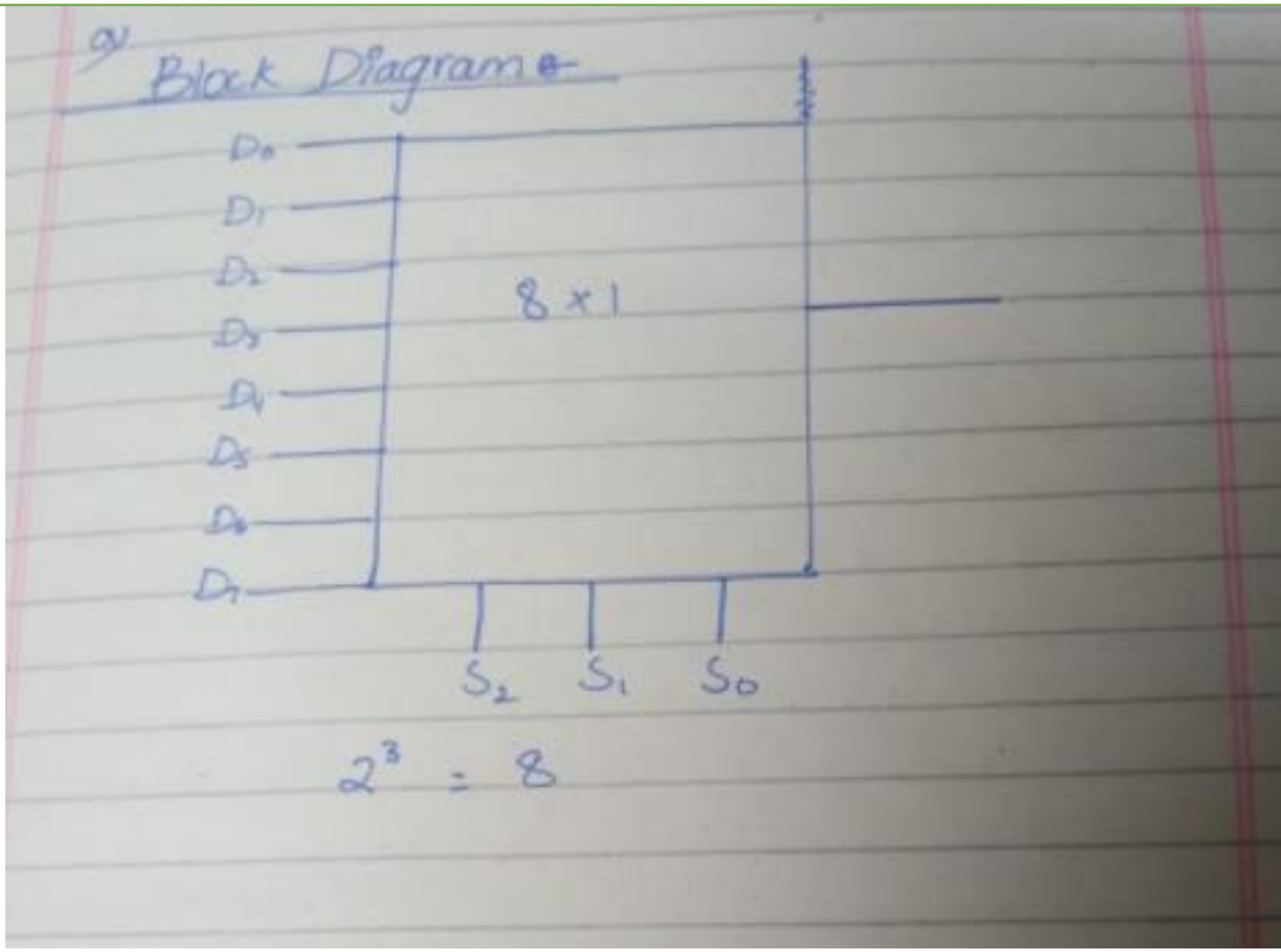
Note: For all the circuits in the tasks, your logic diagrams should be either hand drawn or from the software logicly. Keep them neat and legible. These circuits will be having many connections so, for simulations, make sure that you label the inputs and outputs clearly. Use Label tag in "logically". You can also edit the pictures of your outputs in "paint" easily.

Tasks

1. **Construct a logic circuit for 8 to 1 multiplexer with the help of truth table. Also write the Boolean expression for output(s). Simulate your circuit to verify the outputs.**

8 to 1 Mux

a) Block Diagram



b) Truth Table

b) Truth Table :-

S_2	S_1	S_0	Y
0	0	0	D_0
0	0	1	D_1
0	1	0	D_2
0	1	1	D_3
1	0	0	D_4
1	0	1	D_5
1	1	0	D_6
1	1	1	D_7

c)Boolean Expression

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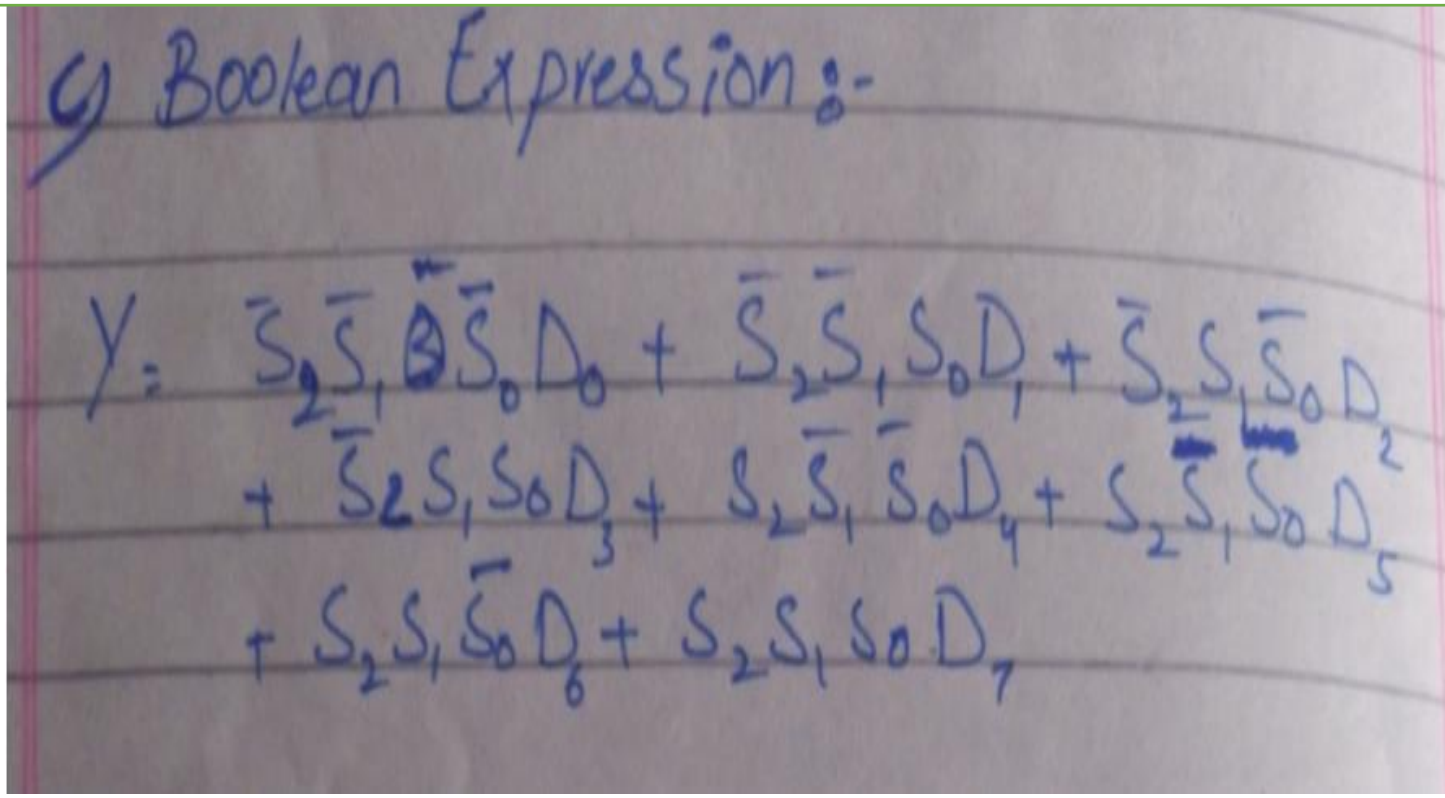
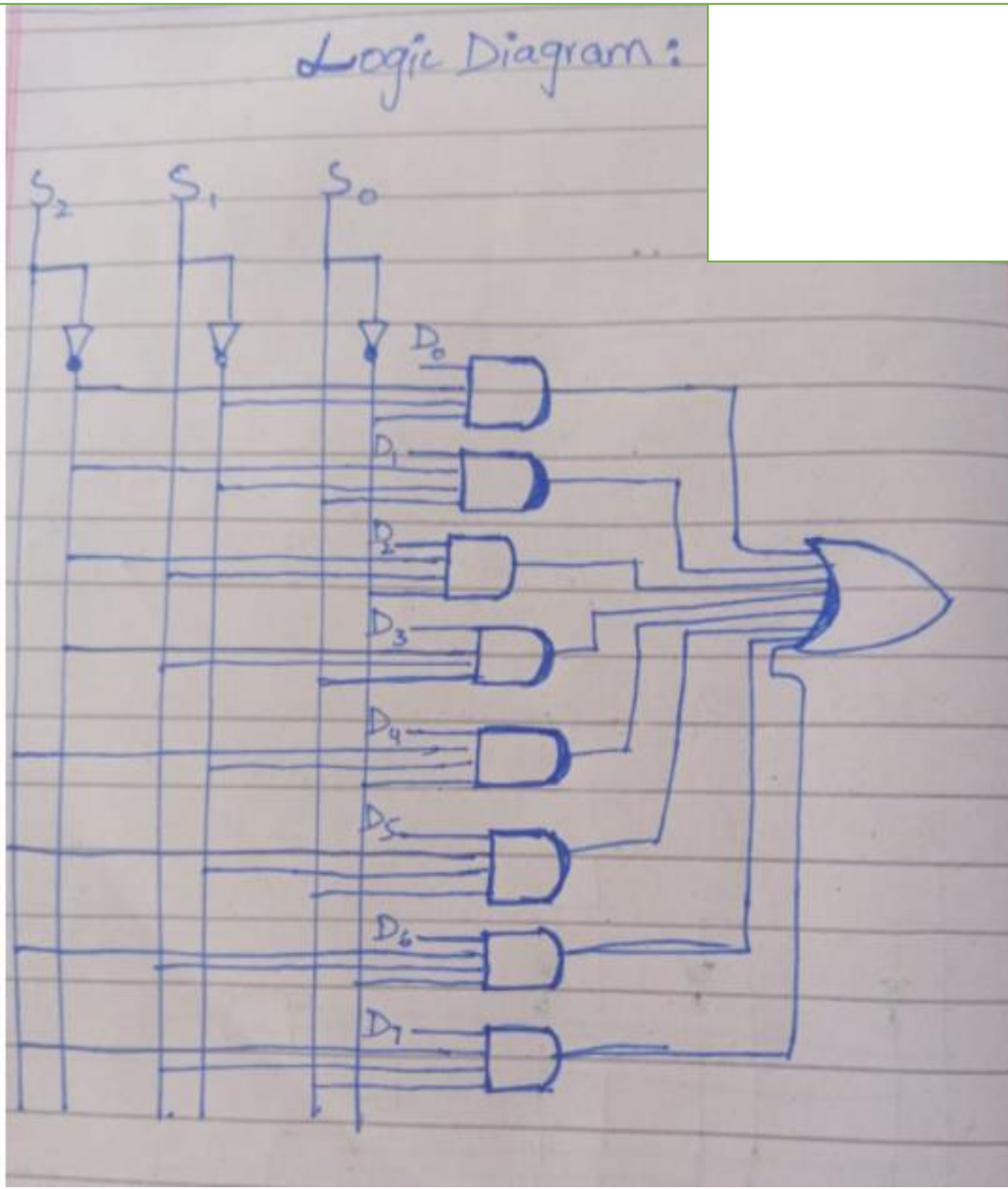


d) Logic Diagram (from logicaly or hand drawn)

Logic Diagram:



e)Software Simulation

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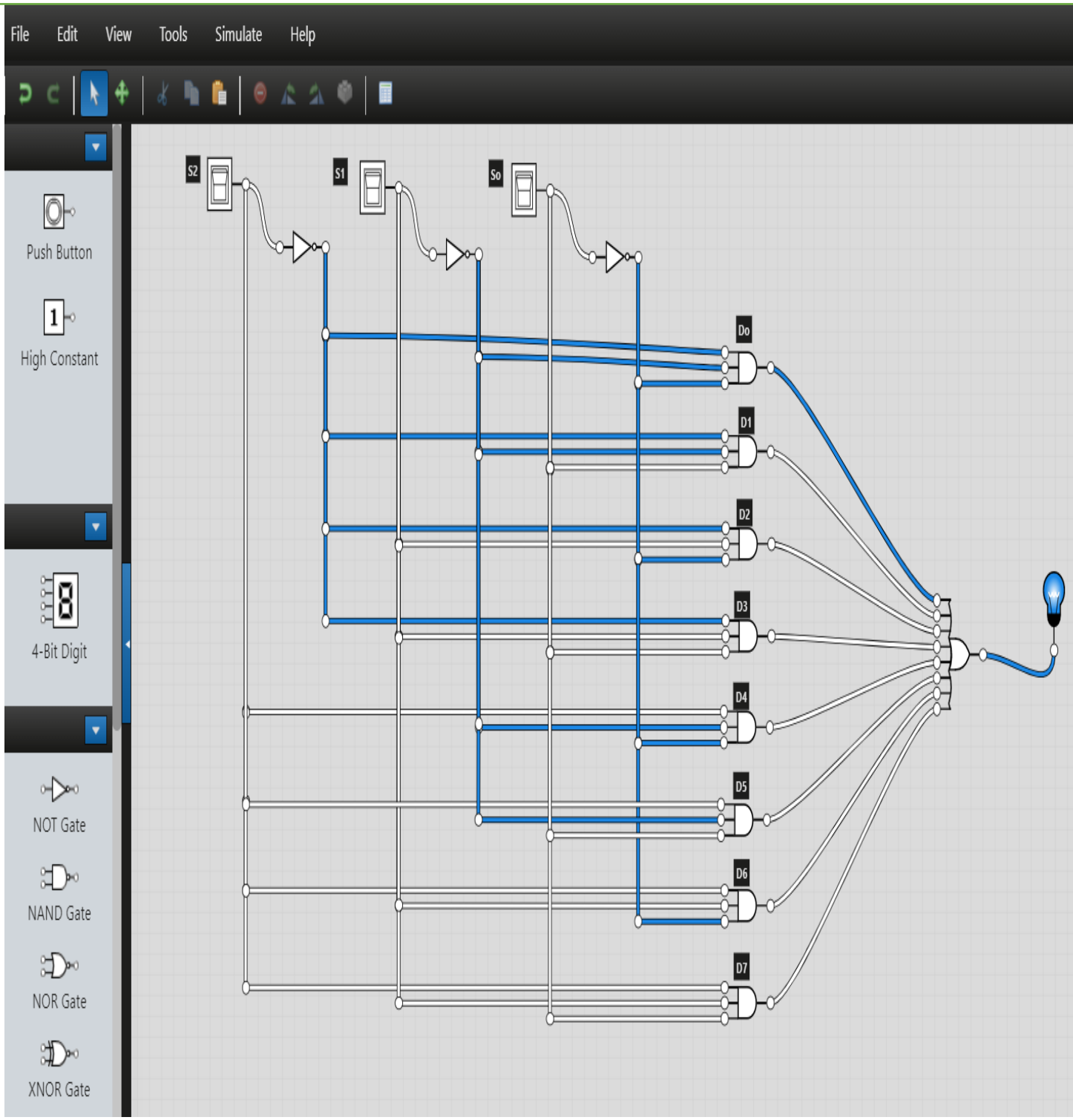
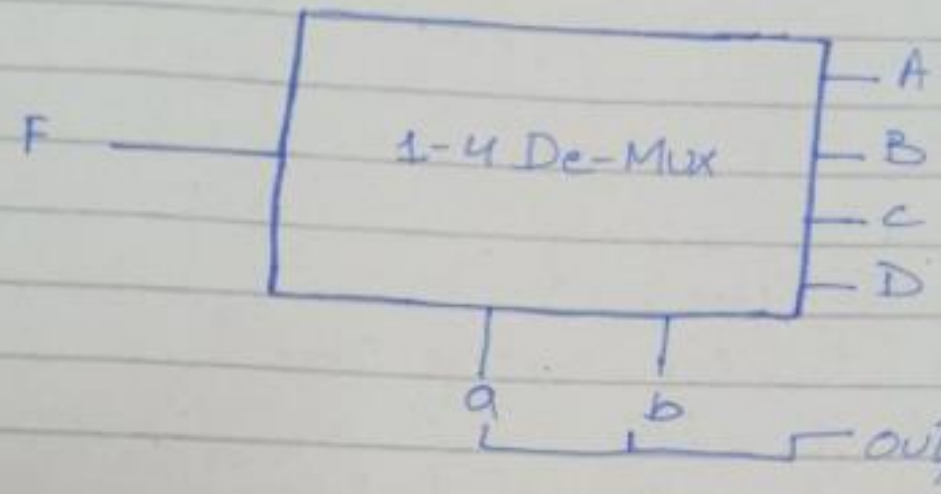


2. **Design a logic circuit for 1 to 4 line Demultiplexer. Also write the Boolean expression for output(s). Simulate your circuit to verify the outputs.**

a) Block Diagram, Truth Table, Boolean Expression

Block Diagram :-



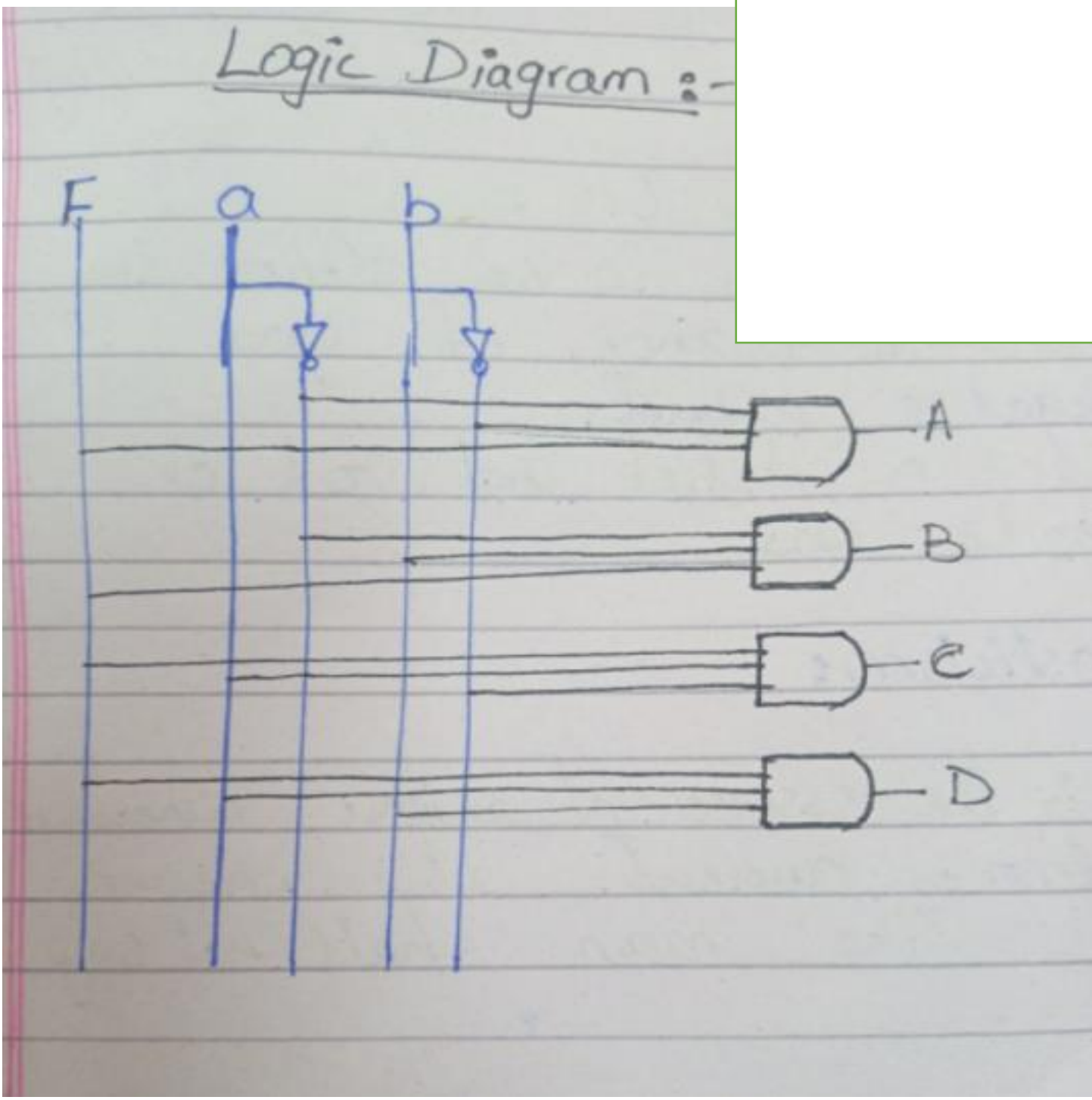
Truth Table :-

a	b	D-output selected
0	0	A
0	1	B
1	0	C
1	1	D

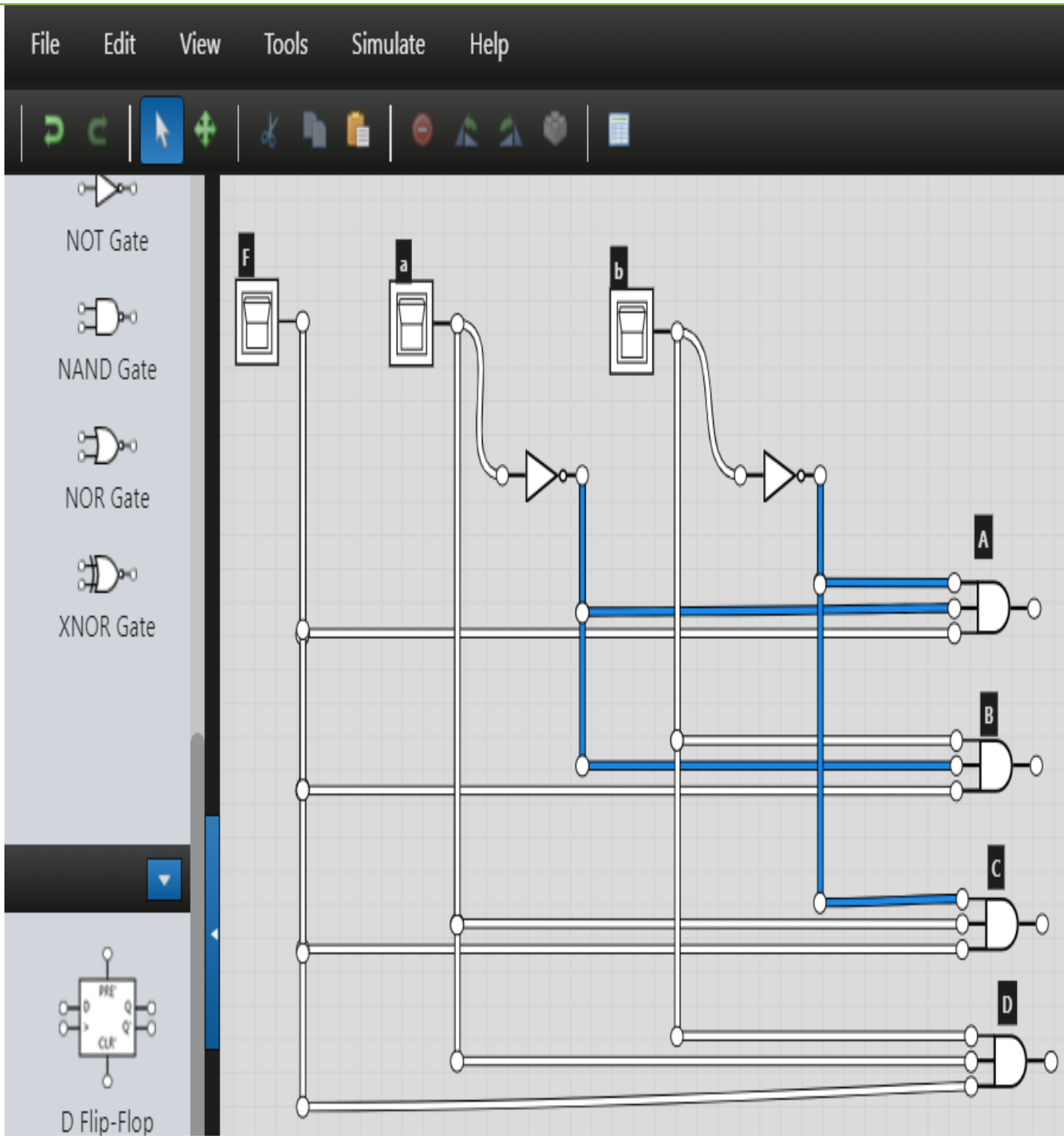
Boolean Expression :-

$$F = \bar{a}.\bar{b}A + \bar{a}.b.B + a.\bar{b}.C + a.b.D$$

b) Logic Diagram

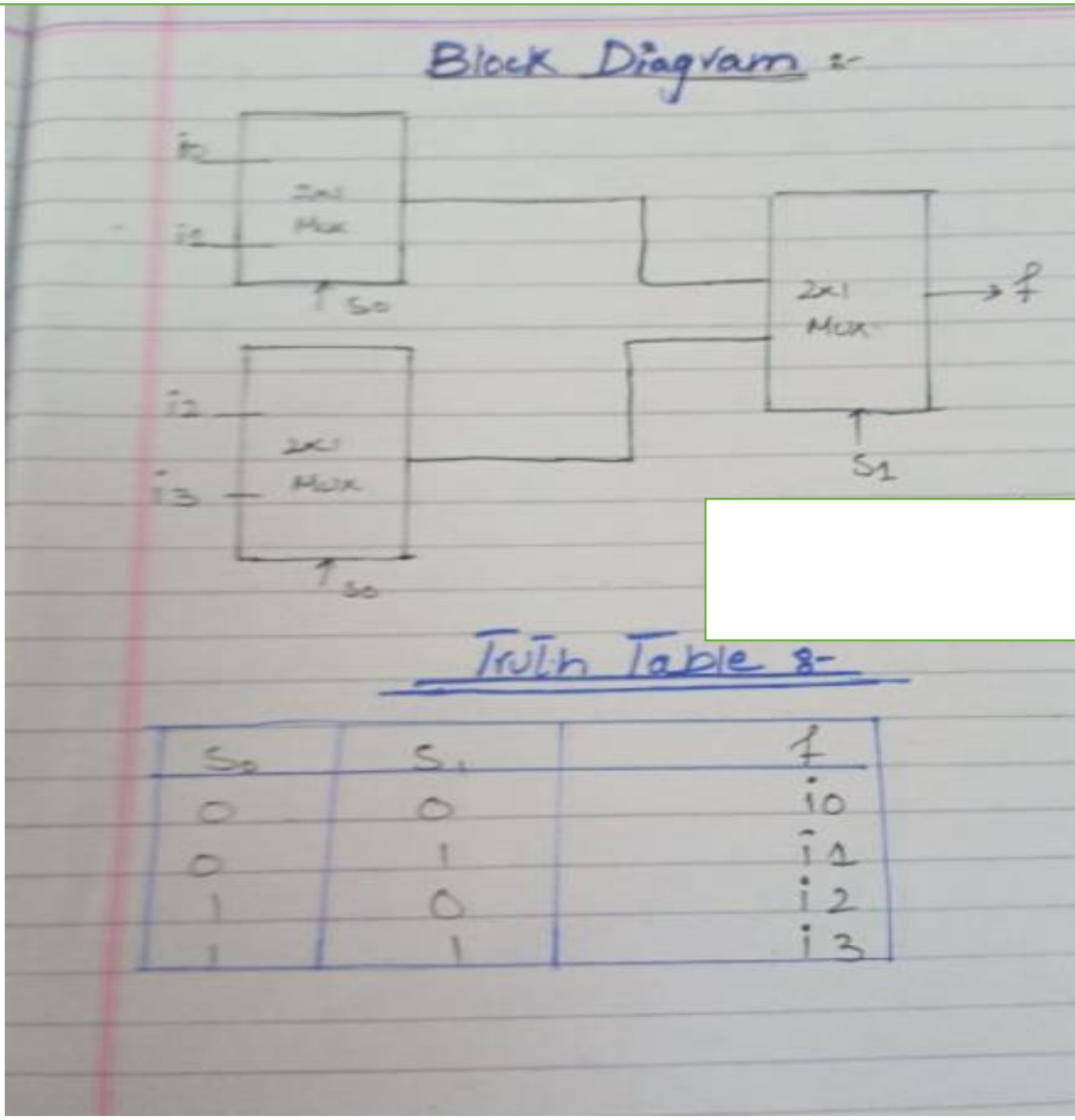


c) Software Simulation


File
Edit
View
Tools
Simulate
Help
NOT Gate
NAND Gate
NOR Gate
XNOR Gate
D Flip-Flop
F
a
b
A
B
C
D

3. **Design a circuit for 4 to 1 Multiplexer using 2 to 1 Multiplexer(s). You can take help from google or the link below. Just ignore the coding language discussed in the link.**
   https://bravelearn.com/design-of-4x2-multiplexer-using-2x1-mux-in-verilog/

a) Block Diagram, Truth Table



b) Logic Circuit (on the basis of 2 to 1 Muxes used/follow the block diagram to draw this circuit)

*You need to connect three **2 x1 Multiplexers** in order to make one **4x1 Multiplexer**.*

Logic Diagram:-