8-D1 PCI Express Reference Design

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Title				
Title Page				
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Title: Table of Contents

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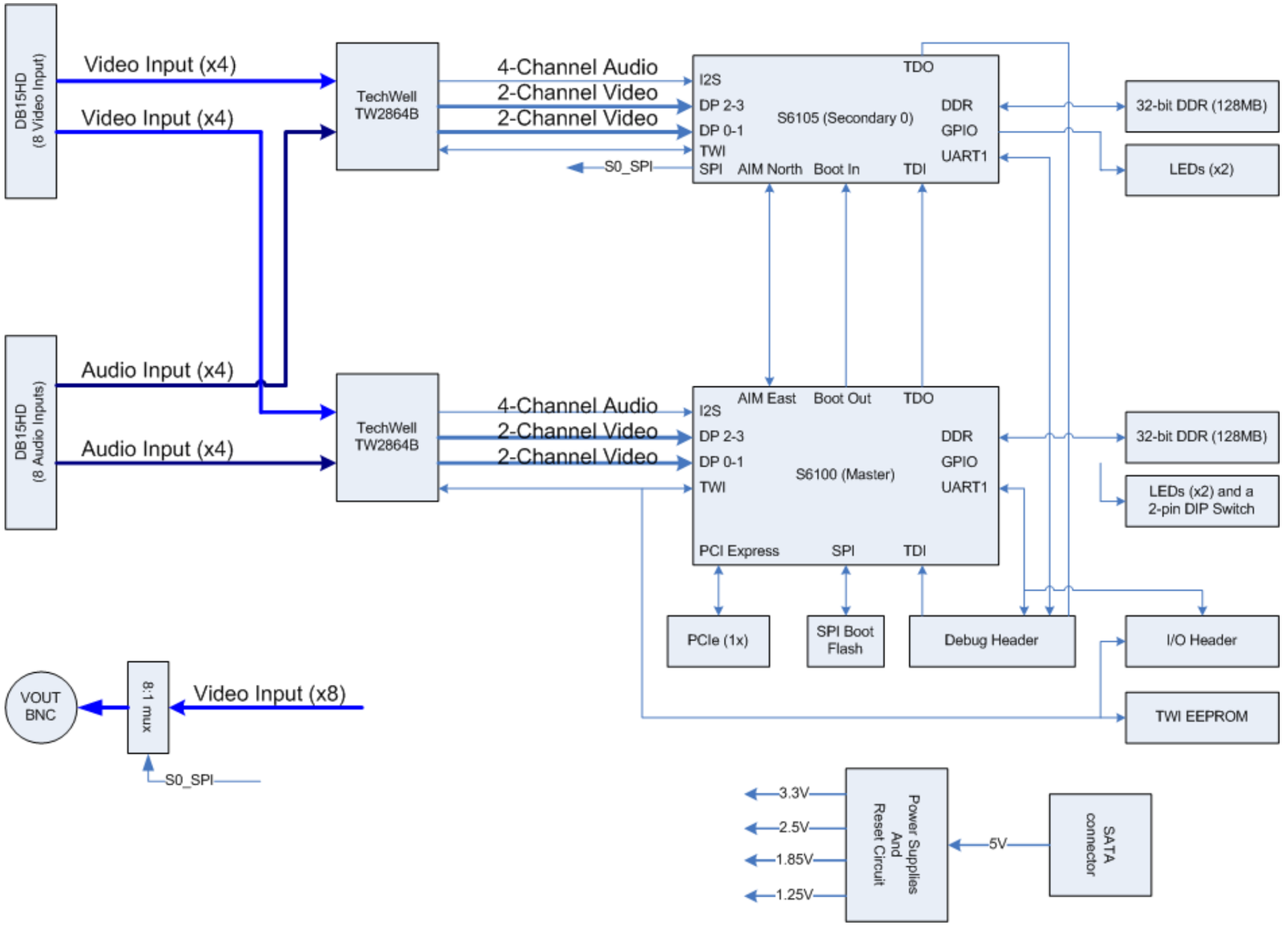

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Title: Block Diagram

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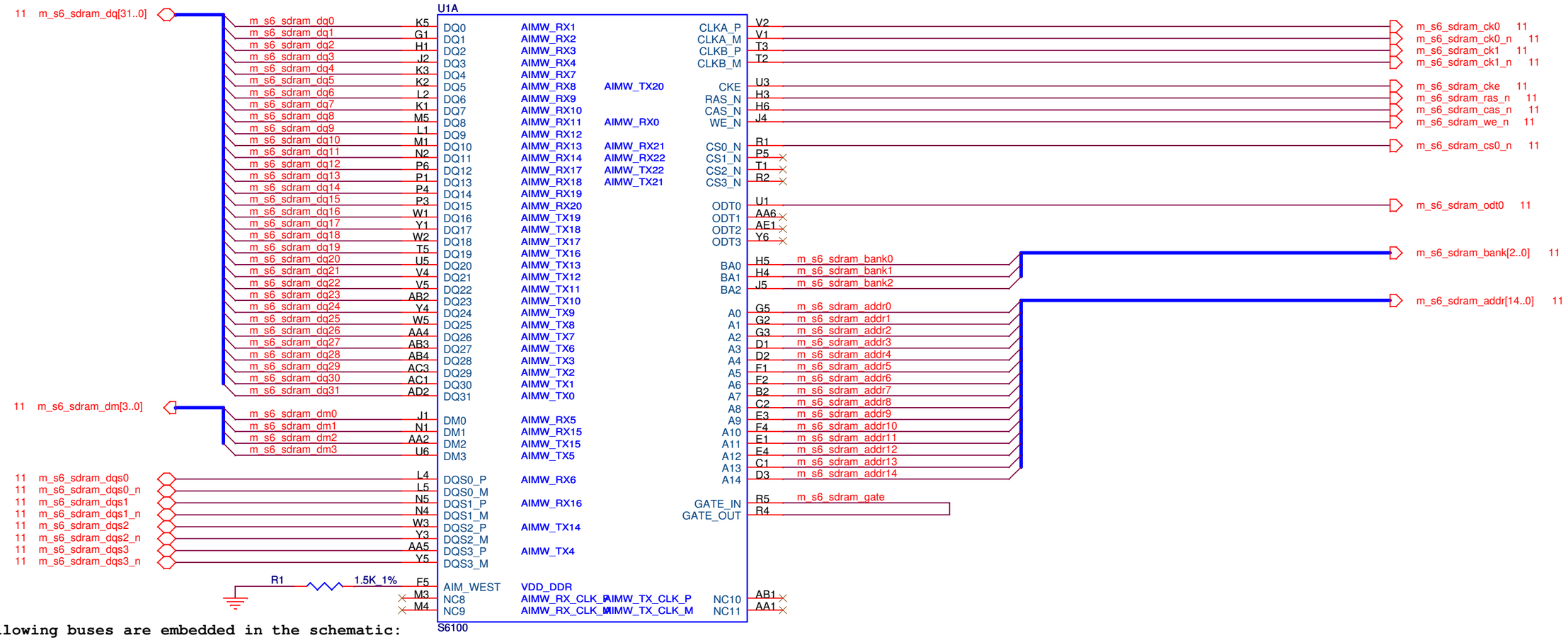

The following buses are embedded in the schematic:
M_S6_DDR_DATA
->contains all the sdram_dq, sdam_dm, sdram_dqs, and sdram_dqs_n signals
M_S6_DDR_CLK
->contains the sdram_ck and sdram_gate signals
M_S6_DDR_ADDR
->contains the sdram_cke, sdram_ras_n, sdram_cas_n, sdram_we_n, sdram_cs0_n, sdram_bank, and sdram_addr signals

The following differential pairs are embedded in the schematic:
M_S6_DDR_DQS0
M_S6_DDR_DQS1
M_S6_DDR_DQS2
M_S6_DDR_DQS3
M_S6_DDR_CK0
M_S6_DDR_CK1

ROUTING RULES (S6100 package legths should be taken into consideration when determining the trace lengths):
1) Differential pairs should be matched to within +/- 5ps (25mil) .
2) The DDR_ADDR bus and clocks should be matched to within +/- 75ps (375mil).
3) The DDR_DATA bus should be matched to within +/- 50ps (250mil).
4) The signals in a byte lane should be matched to within +/- 30ps (150mil) and be routed on the same layer.
5) The clocks and dqs signals should be matched to within +/- 100ps (500mil).
6) m_s6_sdram_gate signal should be as short as possible and accesible using a via.

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Title: Master S6 (DDR Interface)

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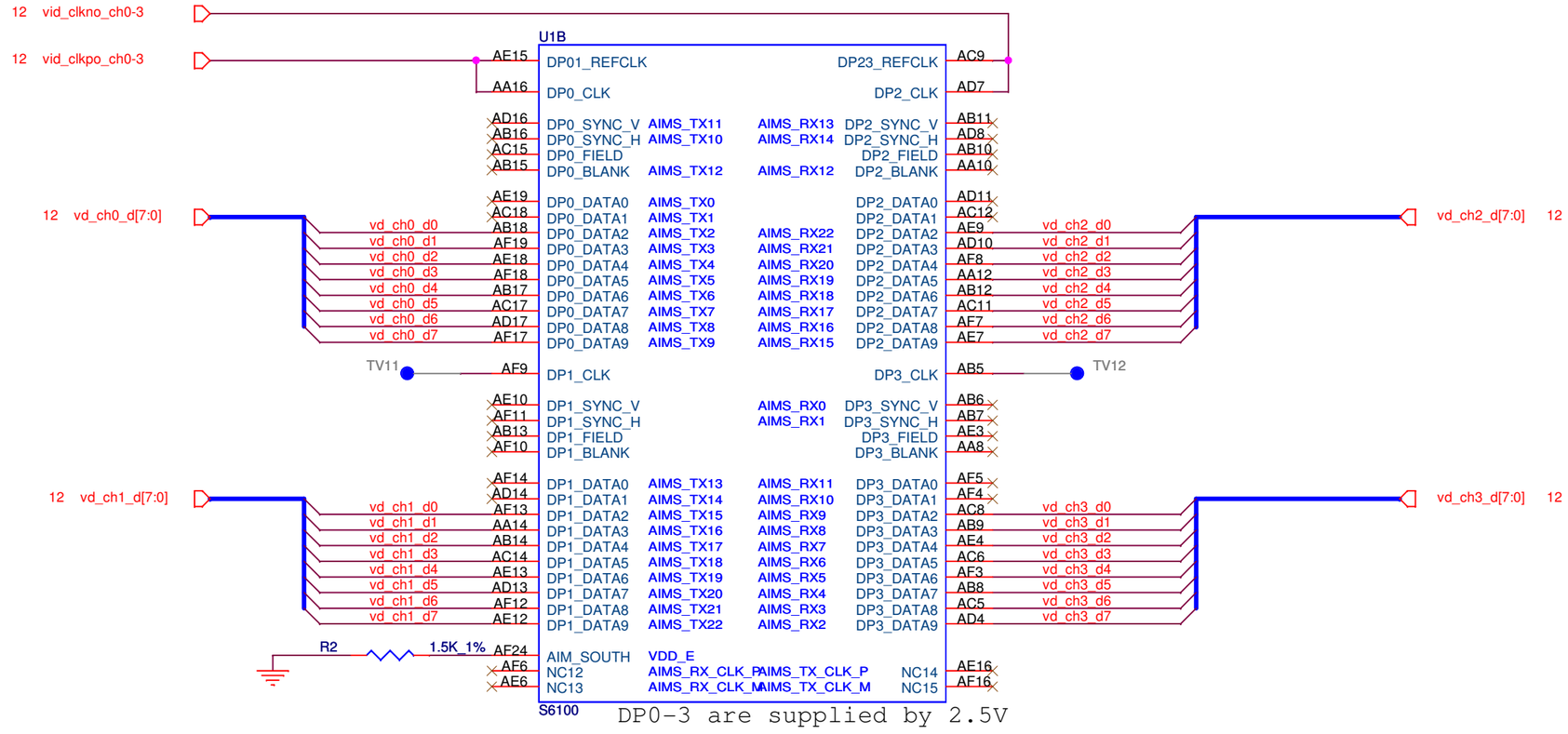

The following buses are embedded in the schematic:
VD_CH0
->contains all the vd_ch0 signals
VD_CH2
->contains all the vd_ch2 signals

ROUTING RULES (S6100 package legths should be taken into consideration when determining the trace lengths):
The VD_CH0, VD_CH2 buses, vid_clkpo_ch0-3, vid_clkno_ch0-3 should be matched to within +/- 250ps (1250mil).

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Master S6 (Data Port Interface)				
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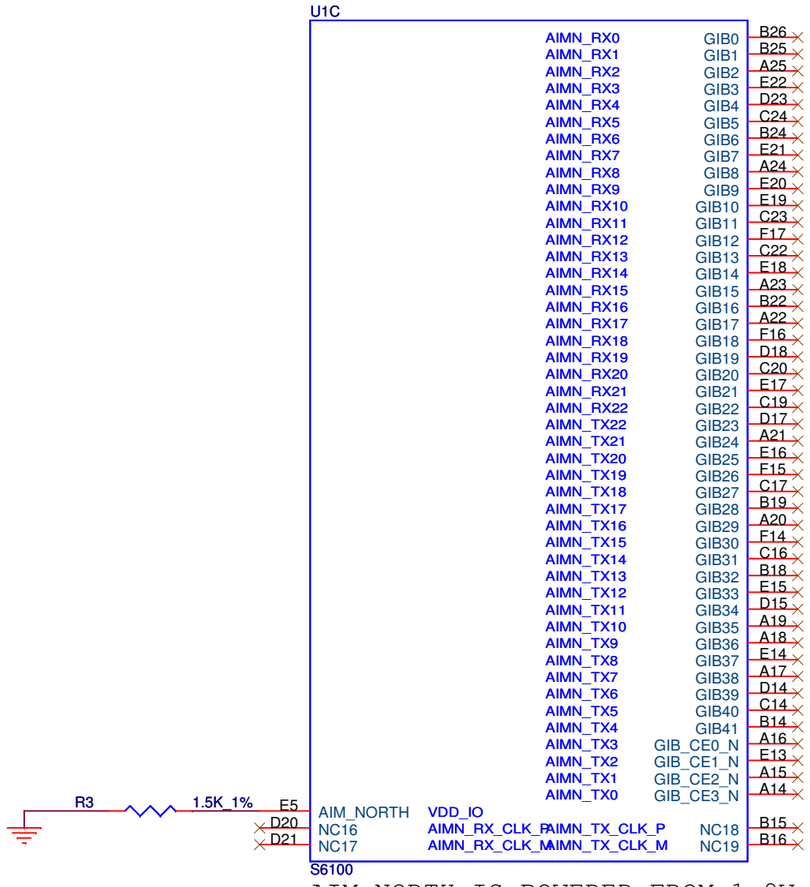

AIM NORTH IS POWERED FROM 1.8V

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Title: Master S6 (GIB Interface)

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ROUTING RULES (S6100 package legths should be taken into consideration when determining the trace lengths):

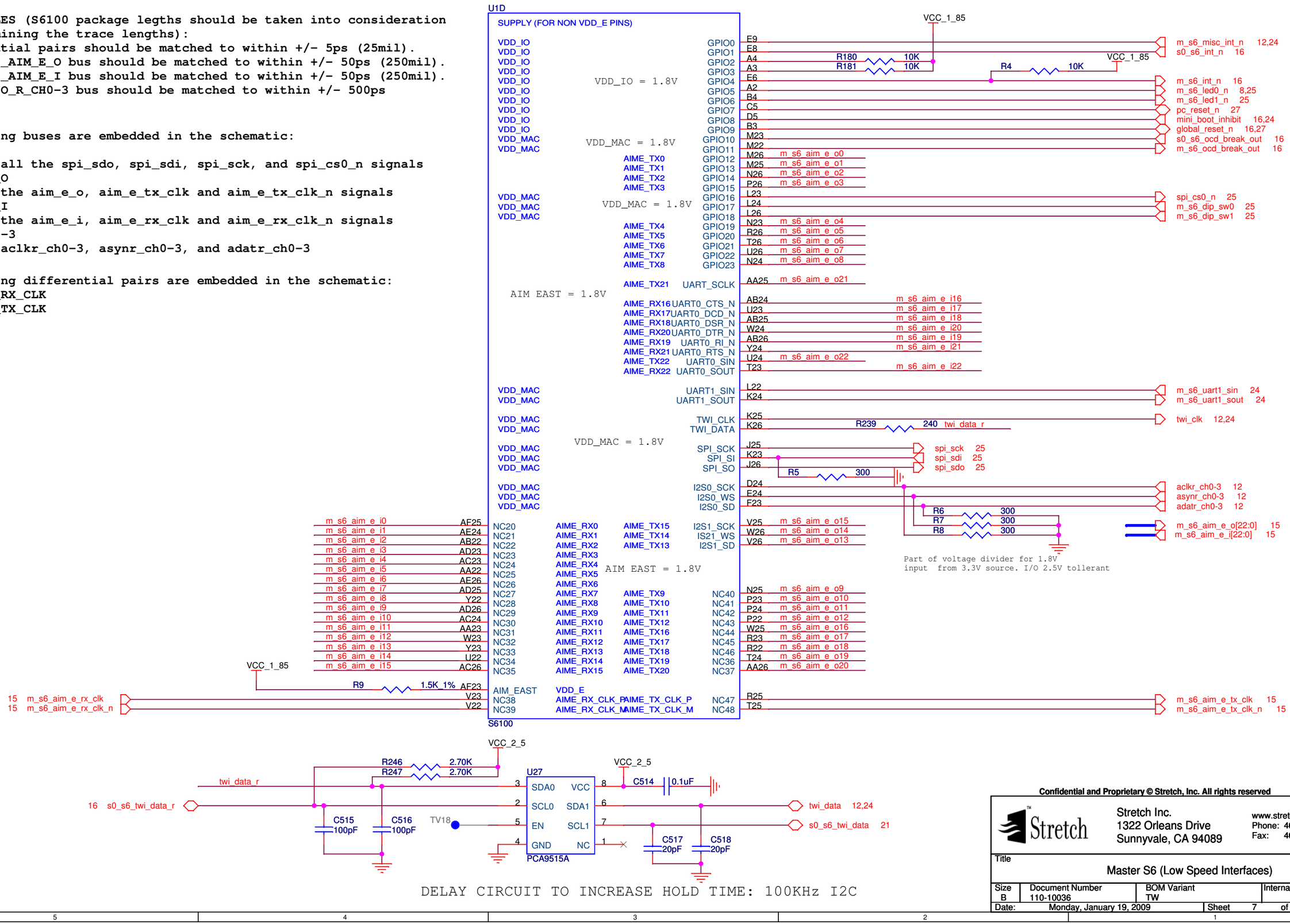
1) Differential pairs should be matched to within +/- 5ps (25mil).
2) The M_S6_AIM_E_O bus should be matched to within +/- 50ps (250mil).
3) The M_S6_AIM_E_I bus should be matched to within +/- 50ps (250mil).
4) The AUDIO_R_CH0-3 bus should be matched to within +/- 500ps (2500mil).

The following buses are embedded in the schematic:

SPI
->contains all the spi_sdo, spi_sdi, spi_sck, and spi_cs0_n signals
M_S6_AIM_E_O
->contains the aim_e_o, aim_e_tx_clk and aim_e_tx_clk_n signals
M_S6_AIM_E_I
->contains the aim_e_i, aim_e_rx_clk and aim_e_rx_clk_n signals
AUDIO_R_CH0-3
->contains aclkr_ch0-3, asynr_ch0-3, and adatr_ch0-3

The following differential pairs are embedded in the schematic:

M_S6_AIM_E_RX_CLK
M_S6_AIM_E_TX_CLK



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Master S6 (Low Speed Interfaces)				
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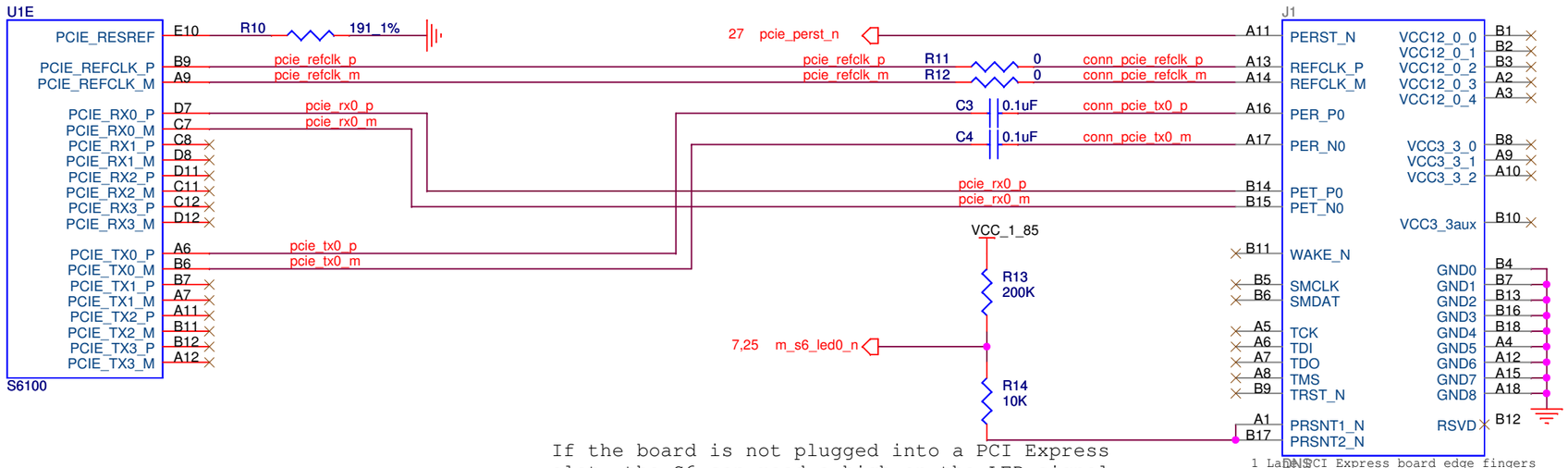
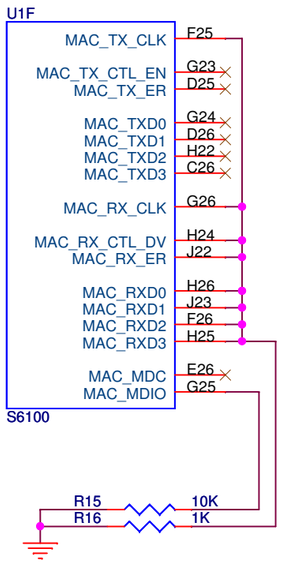
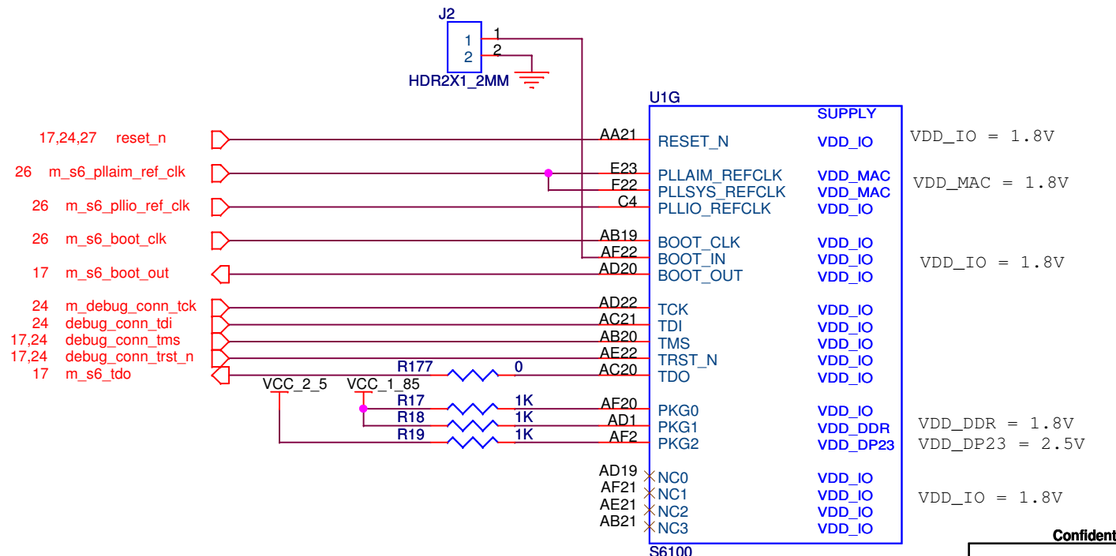


If the board is not plugged into a PCI Express slot, the S6 can read a high on the LED signal, otherwise, a low will be detected (PRSNT1_N is connected to ground on the system board).

The following differential pairs are embedded in the schematic: CONN_PCIE_TX, CONN_PCIE_RX, CONN_PCIE_REFCLK



ROUTING RULES (S6100 package lengths should be taken into consideration when determining the trace lengths):
1) The differential pairs should be routed to within 5mil.
2) The length from the PCI Express connector to the S6100 should be less than 3.5".
3) Extend the PCI fingers such that they can be used for probing signals (no soldermask).



The following buses are embedded in the schematic:
PCIE
->contains all the pcie signals

The following differential pairs are embedded in the schematic:
PCIE_REFCLK
PCIE_RX0
PCIE_TX0

ROUTING RULES (S6100 package legths should be taken into consideration when determining the trace lengths):
1) The differential pairs should be routed to within 5mil.
2) The length from the PCI Express connector to the S6100 should be less than 3.5".

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Title: Master S6 (PCI Express and Ethernet Interfaces)

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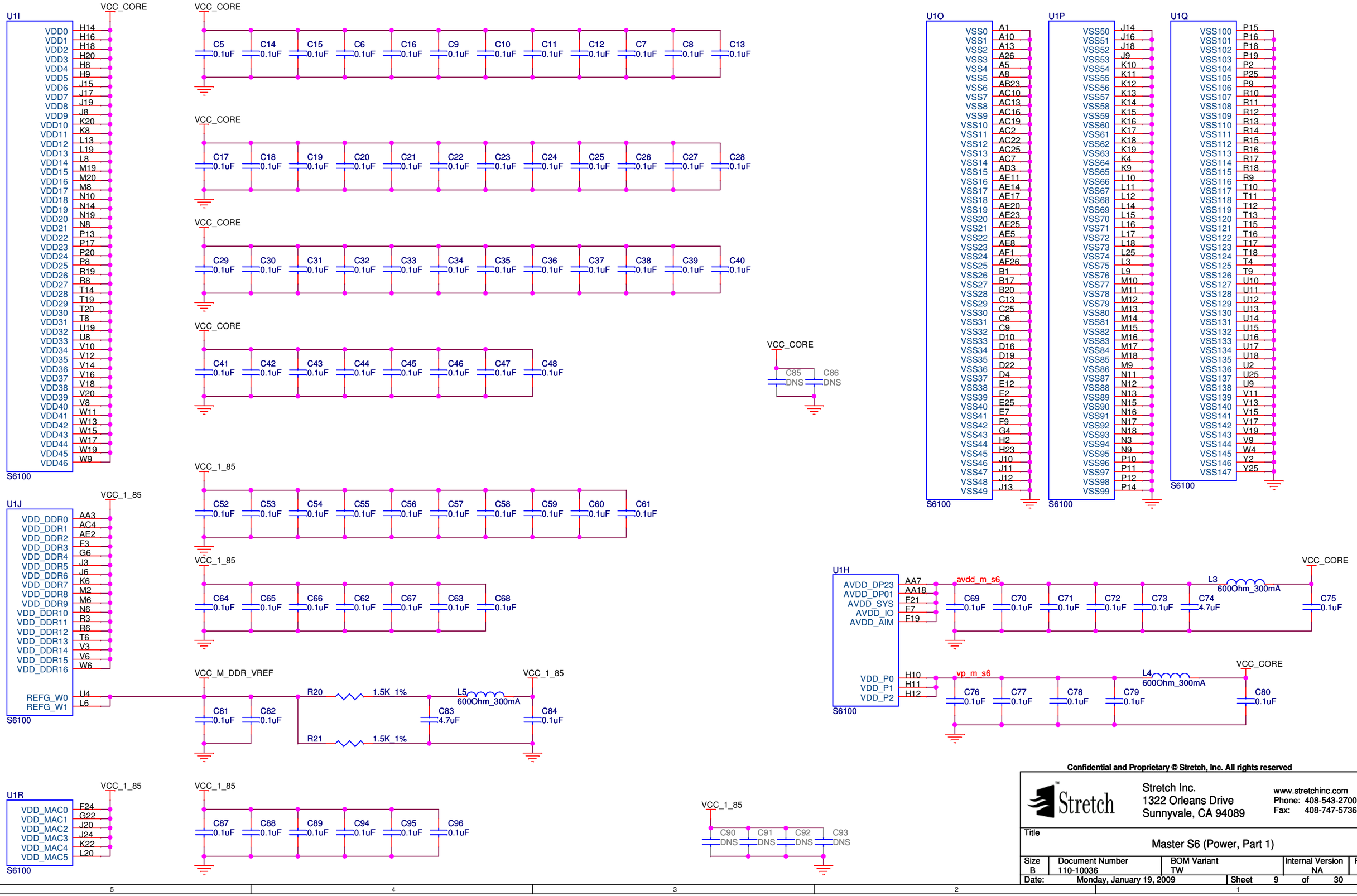

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Title: Master S6 (Power, Part 1)

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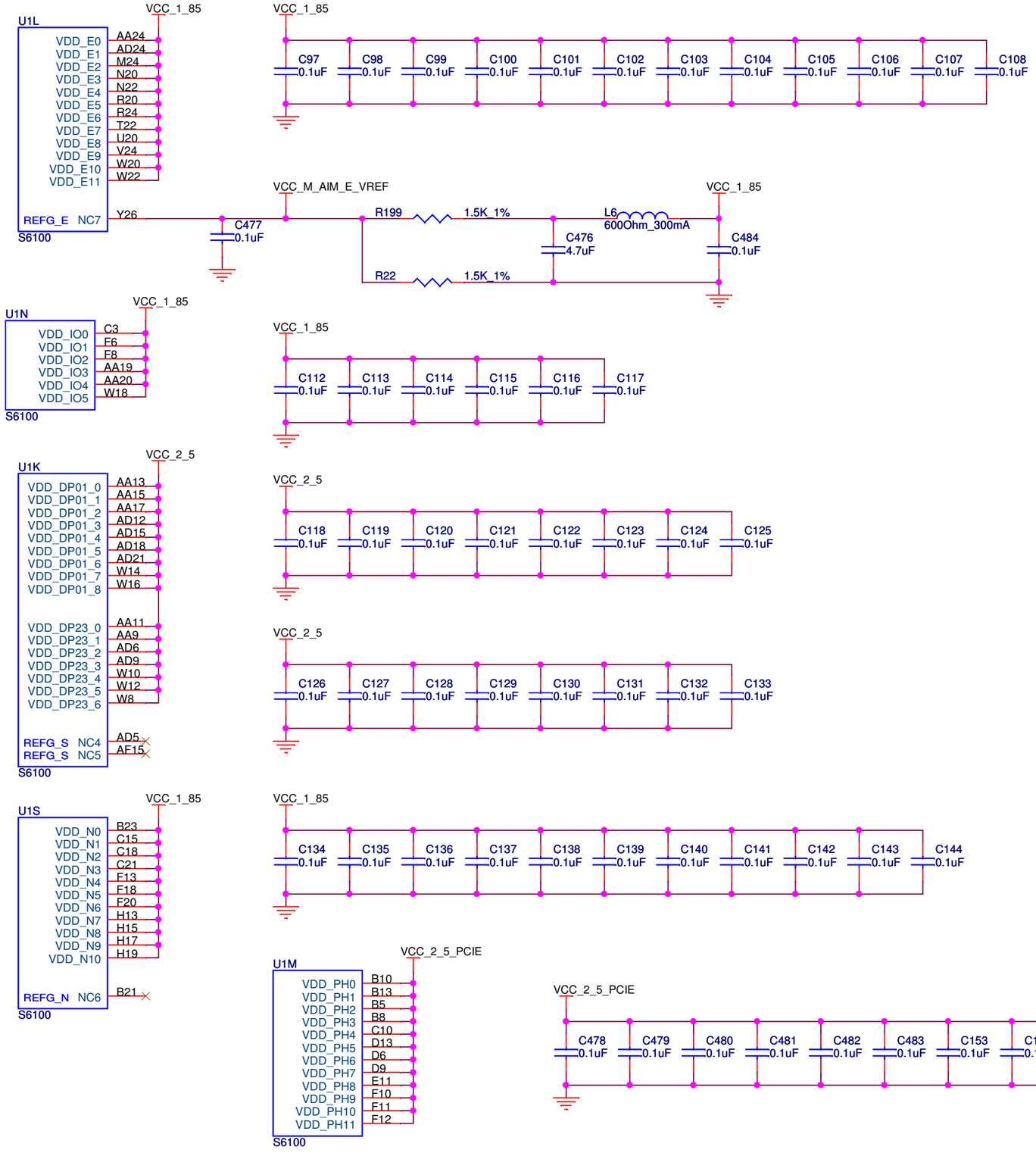

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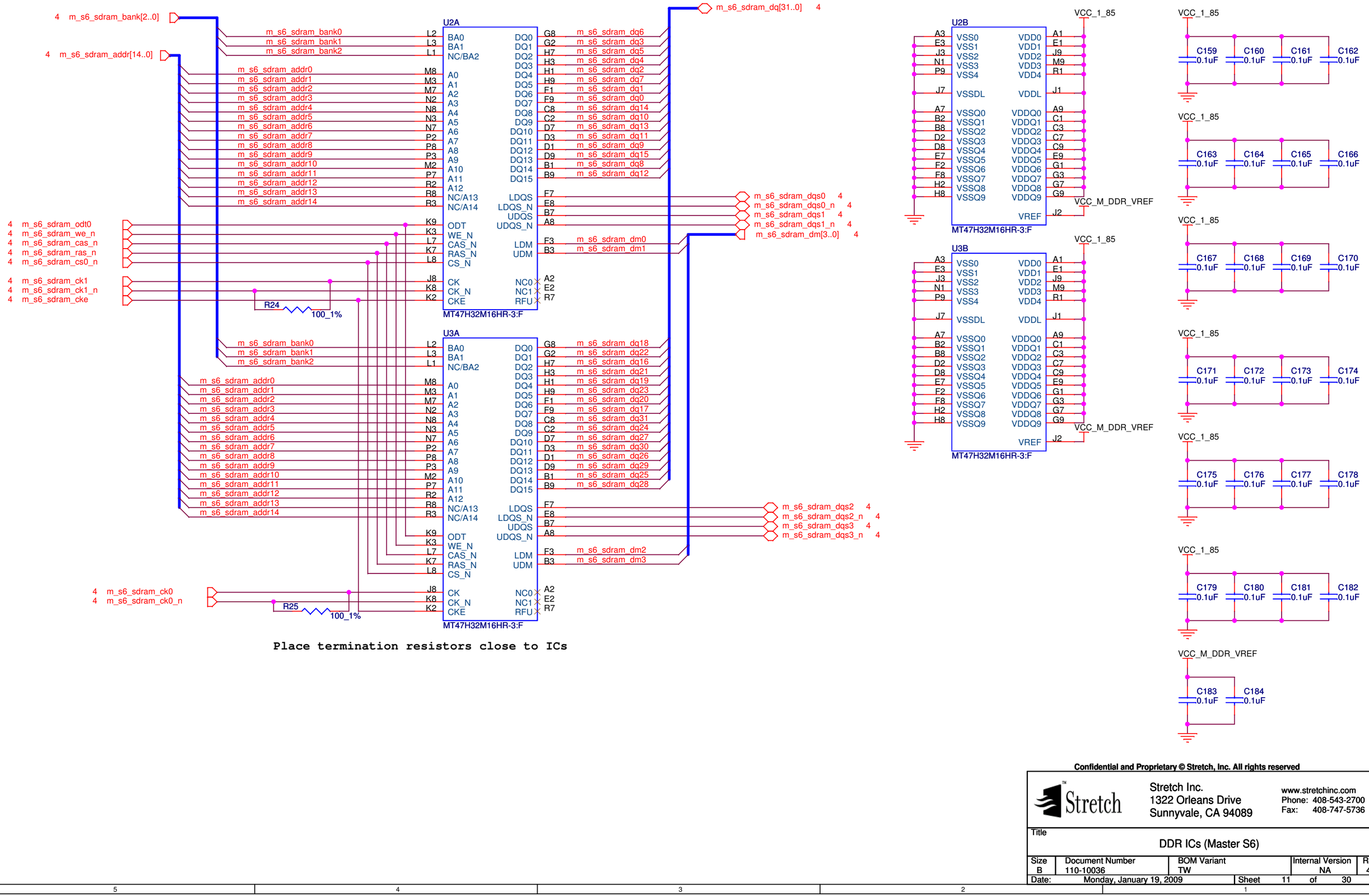

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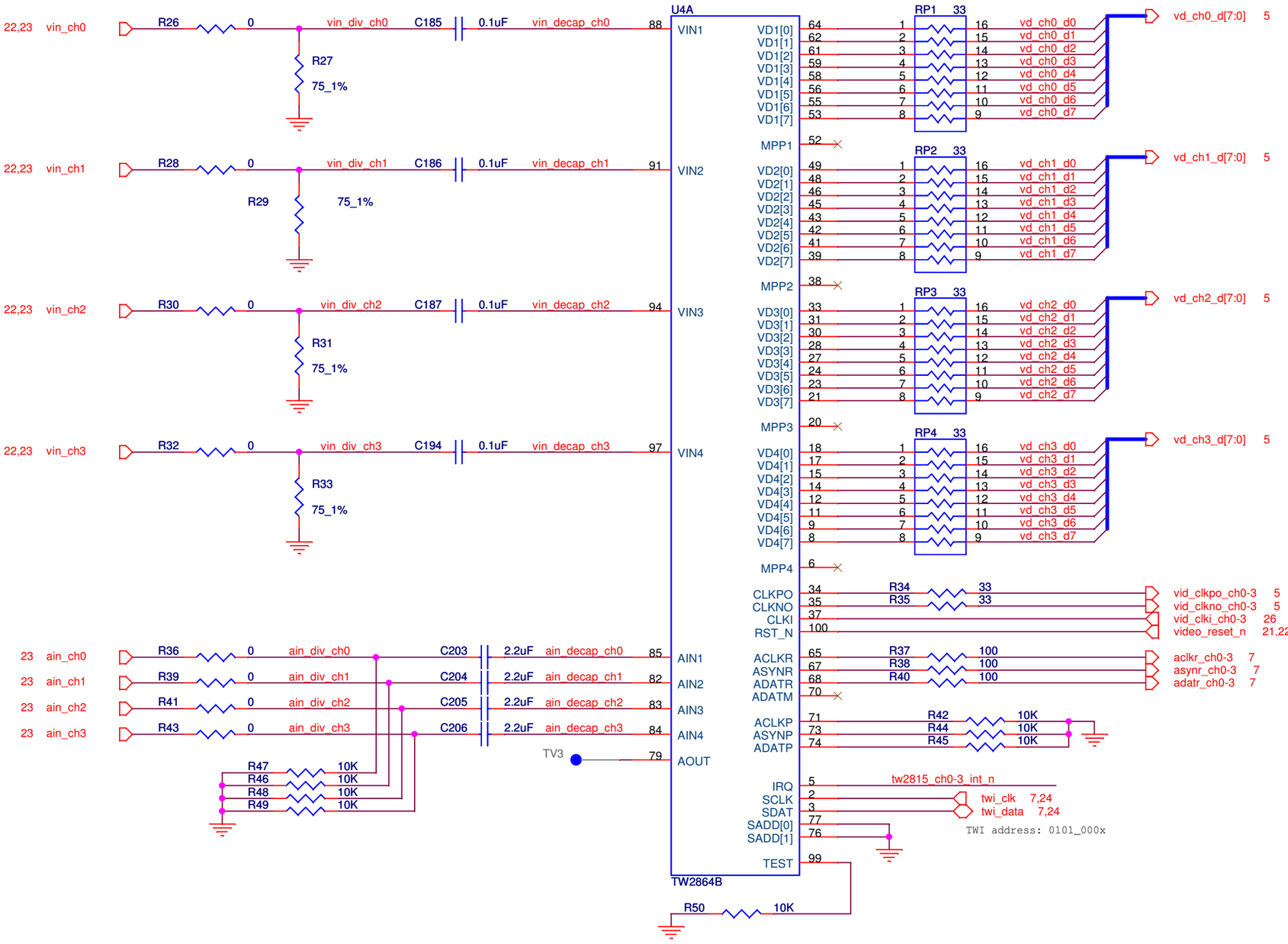

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Title: TW2864 (Master S6)

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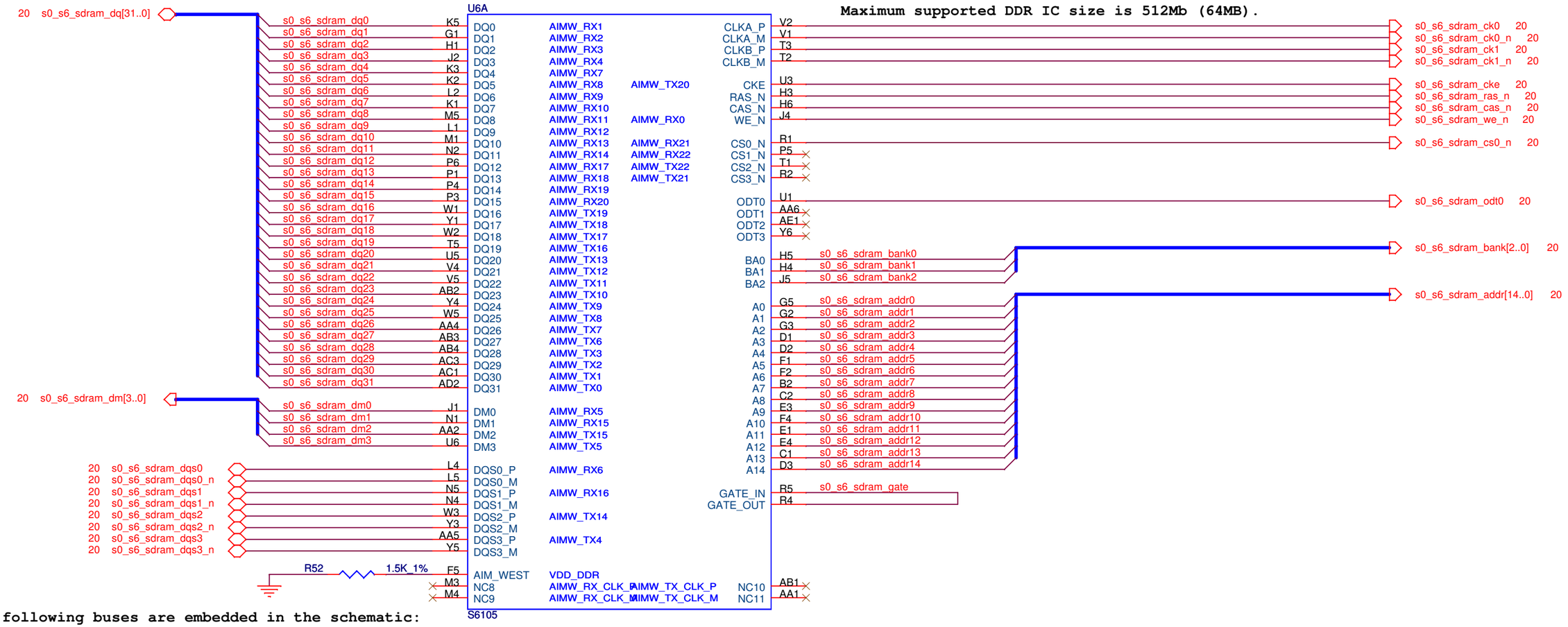

The following buses are embedded in the schematic:
S0_S6_DDR_DATA
->contains all the sdram_dq, sdam_dm, sdram_dqs, and sdram_dqs_n signals
S0_S6_DDR_CLK
->contains the sdram_ck and sdram_gate signals
S0_S6_DDR_ADDR
->contains the sdram_cke, sdram_ras_n, sdram_cas_n, sdram_we_n, sdram_cs0_n, sdram_bank, and sdram_addr signals

The following differential pairs are embedded in the schematic:
S0_S6_DDR_DQS0
S0_S6_DDR_DQS1
S0_S6_DDR_DQS2
S0_S6_DDR_DQS3
S0_S6_DDR_CK0
S0_S6_DDR_CK1

ROUTING RULES (S6100 package legths should be taken into consideration when determining the trace lengths):
1) Differential pairs should be matched to within +/- 5ps (25mil) .
2) The DDR_ADDR bus and clocks should be matched to within +/- 75ps (375mil).
3) The DDR_DATA bus should be matched to within +/- 50ps (250mil).
4) The signals in a byte lane should be matched to within +/- 30ps (150mil) and be routed on the same layer.
5) The clocks and dqs signals should be matched to within +/- 100ps (500mil).
6) s0_s6_sdram_gate signal should be as short as possible and accesible using a via.

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Secondary 0 S6 (DDR Interface)				
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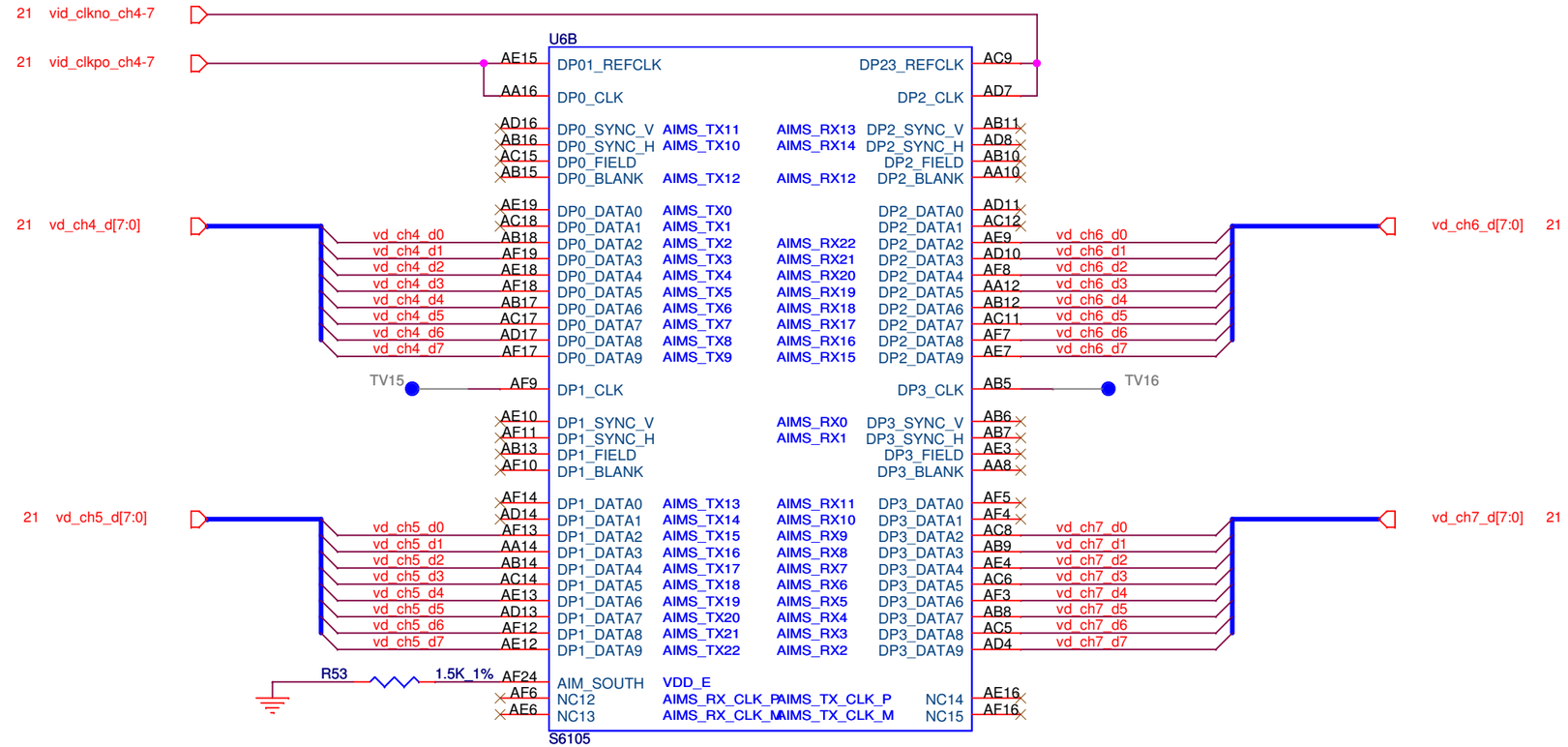

DP 0-3 ARE POWERED FROM 2.5V

The following buses are embedded in the schematic:
VD_CH4
->contains all the vd_ch4 signals
VD_CH6
->contains all the vd_ch6 signals

ROUTING RULES (S6100 package legths should be taken into consideration when determining the trace lengths):
The VD_CH4, VD_CH6 buses, vid_clkpo_ch4-7, and vid_clkno_ch4-7 should be matched to within +/- 250ps (1250mil).

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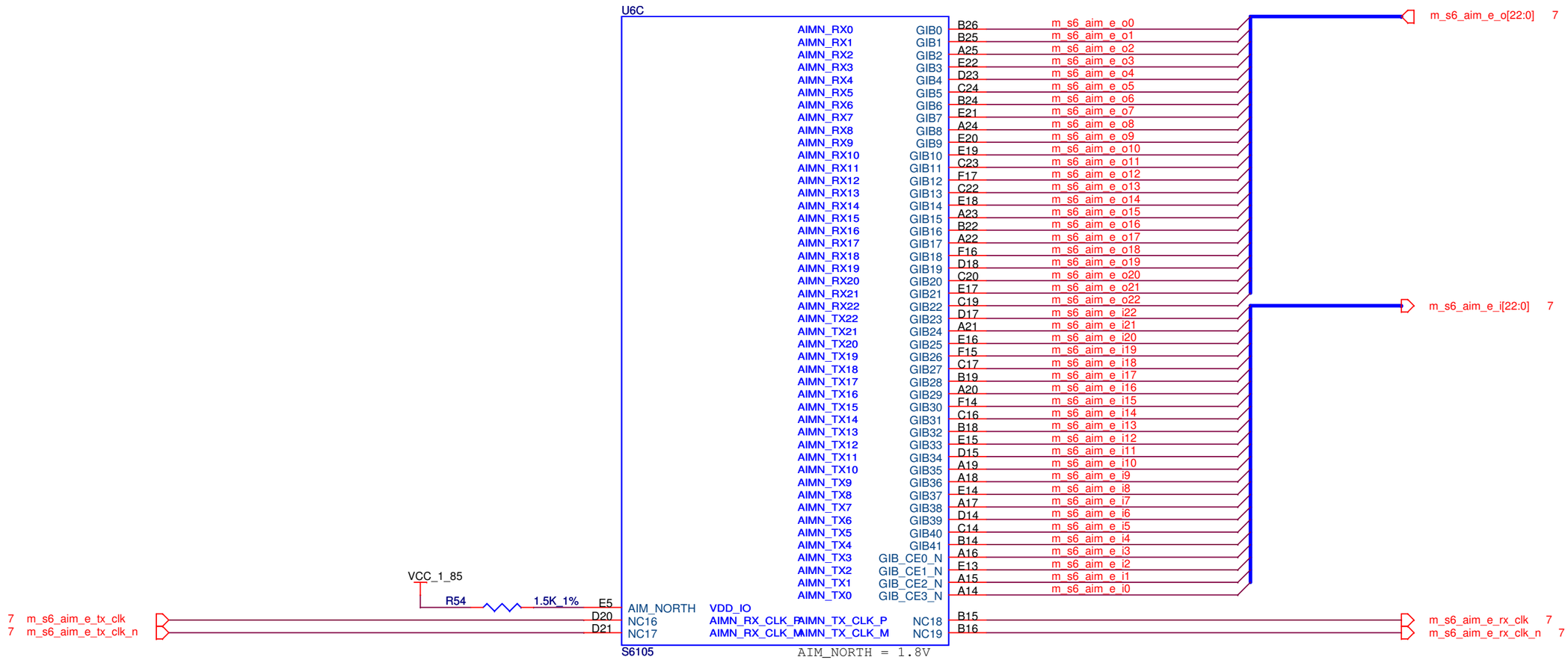

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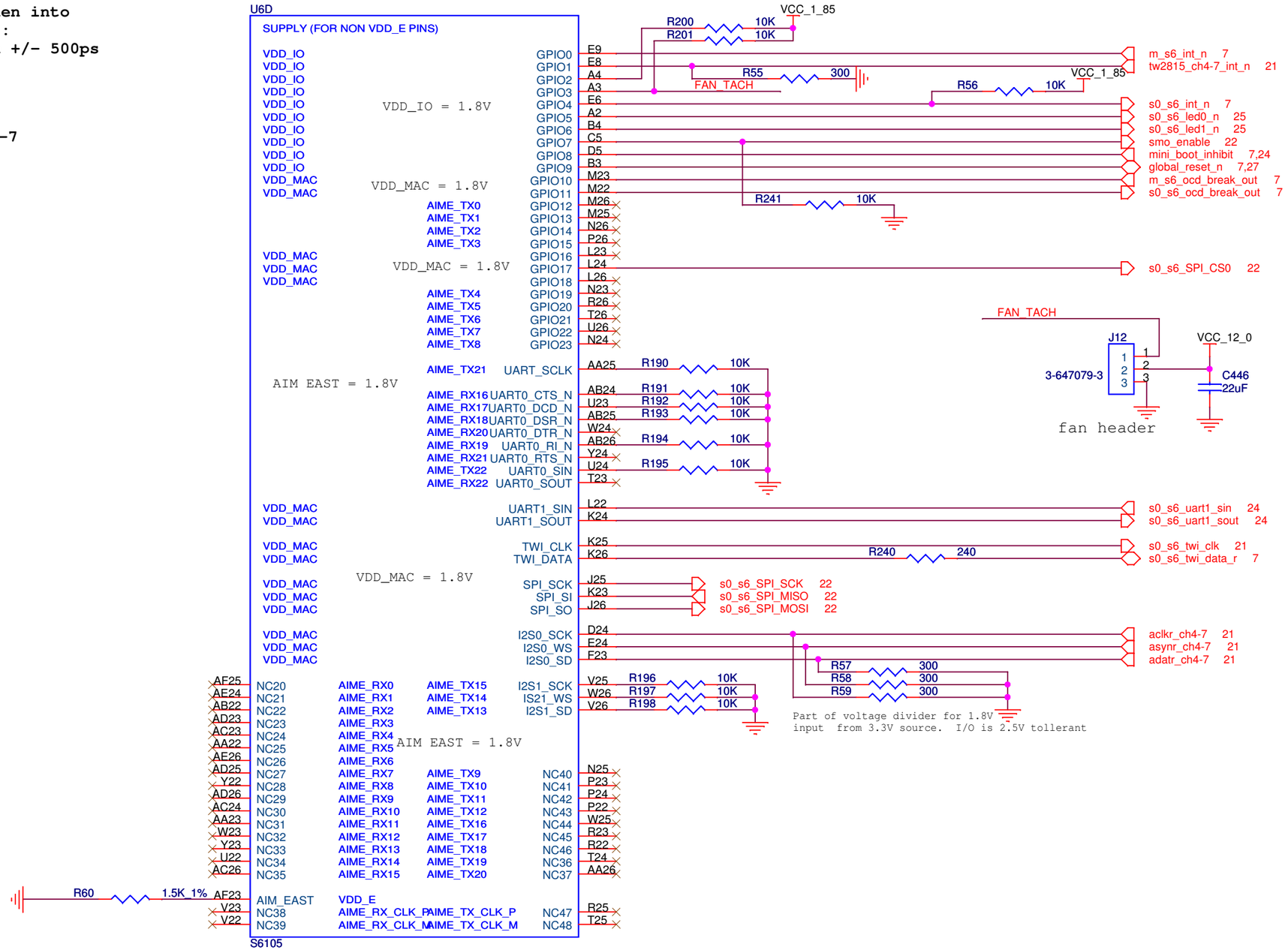
ROUTING RULES (S6100 package legths should be taken into consideration when determining the trace lengths):
The AUDIO_R_CH4-7 bus should be matched to within +/- 500ps (2500mil).

The following buses are embedded in the schematic:
AUDIO_R_CH4-7
->contains aclkr_ch4-7, asynr_ch4-7, and adatr_ch4-7



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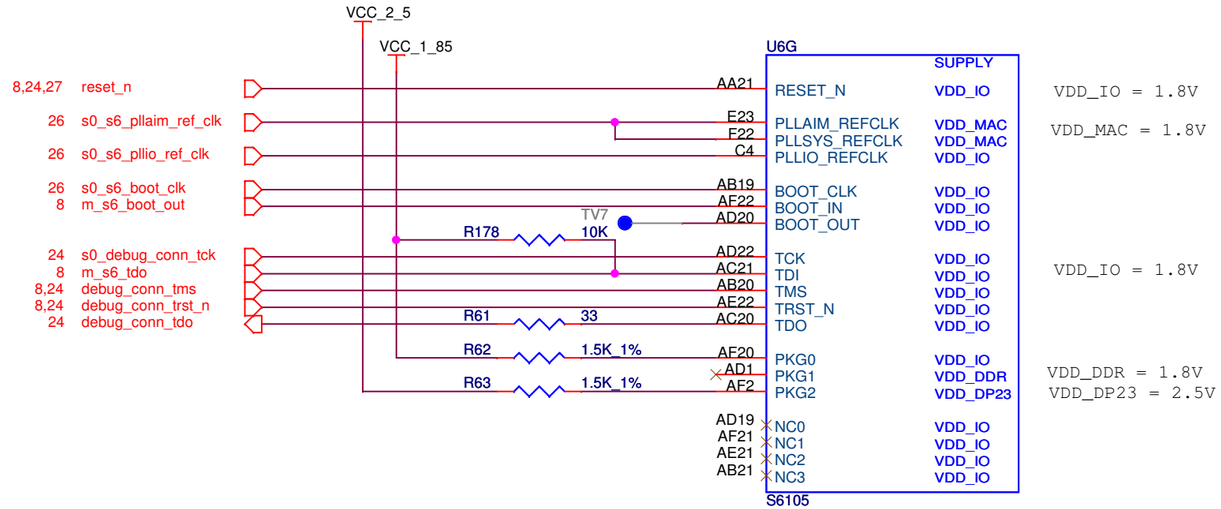

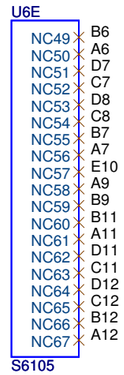

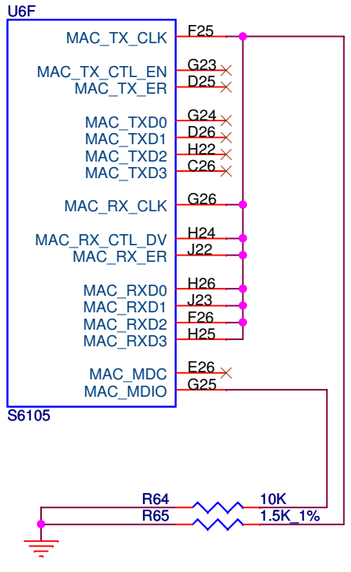

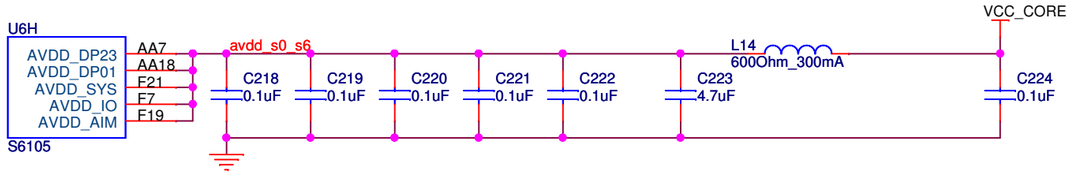

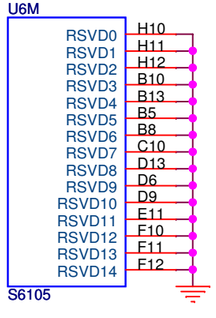

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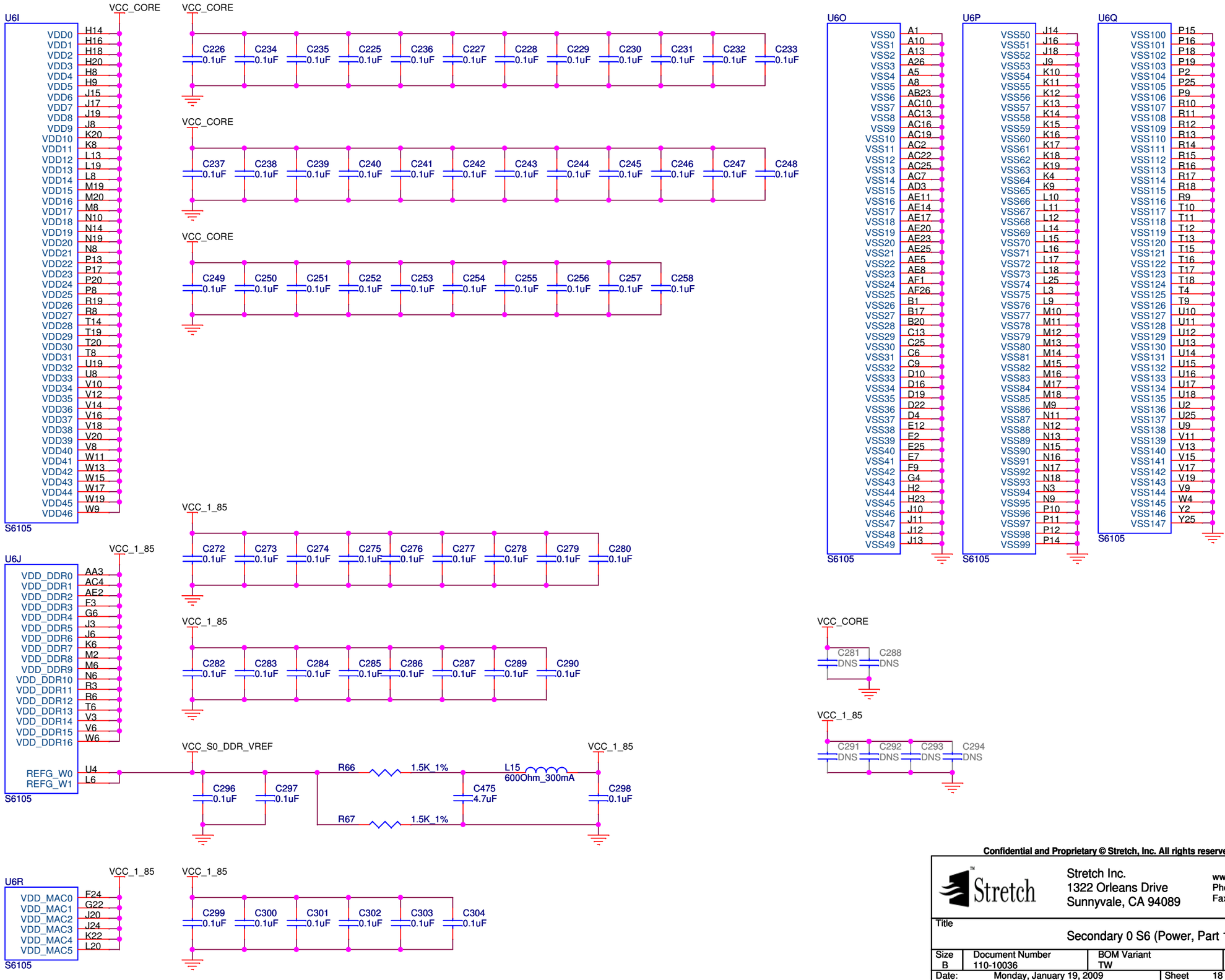

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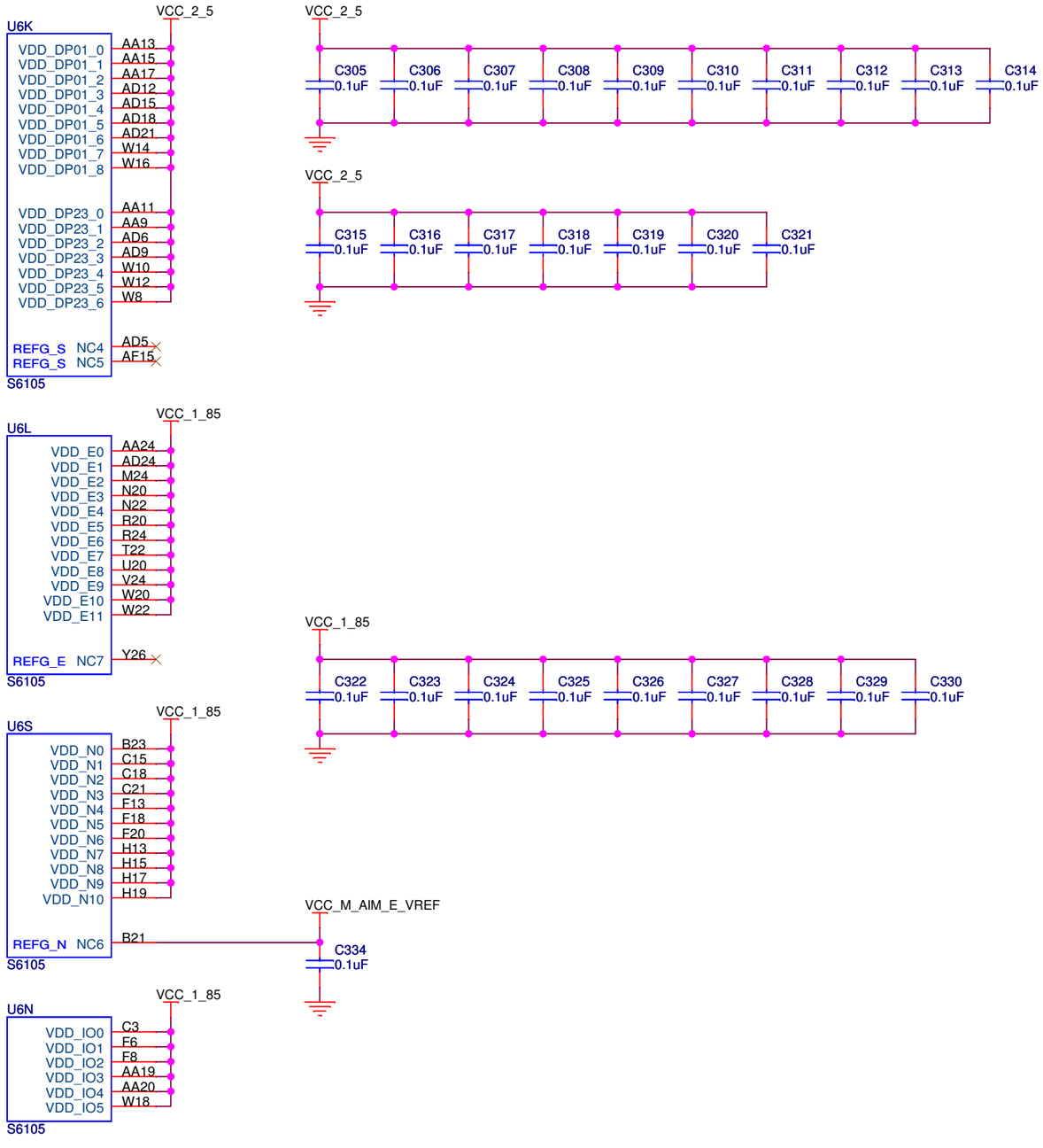

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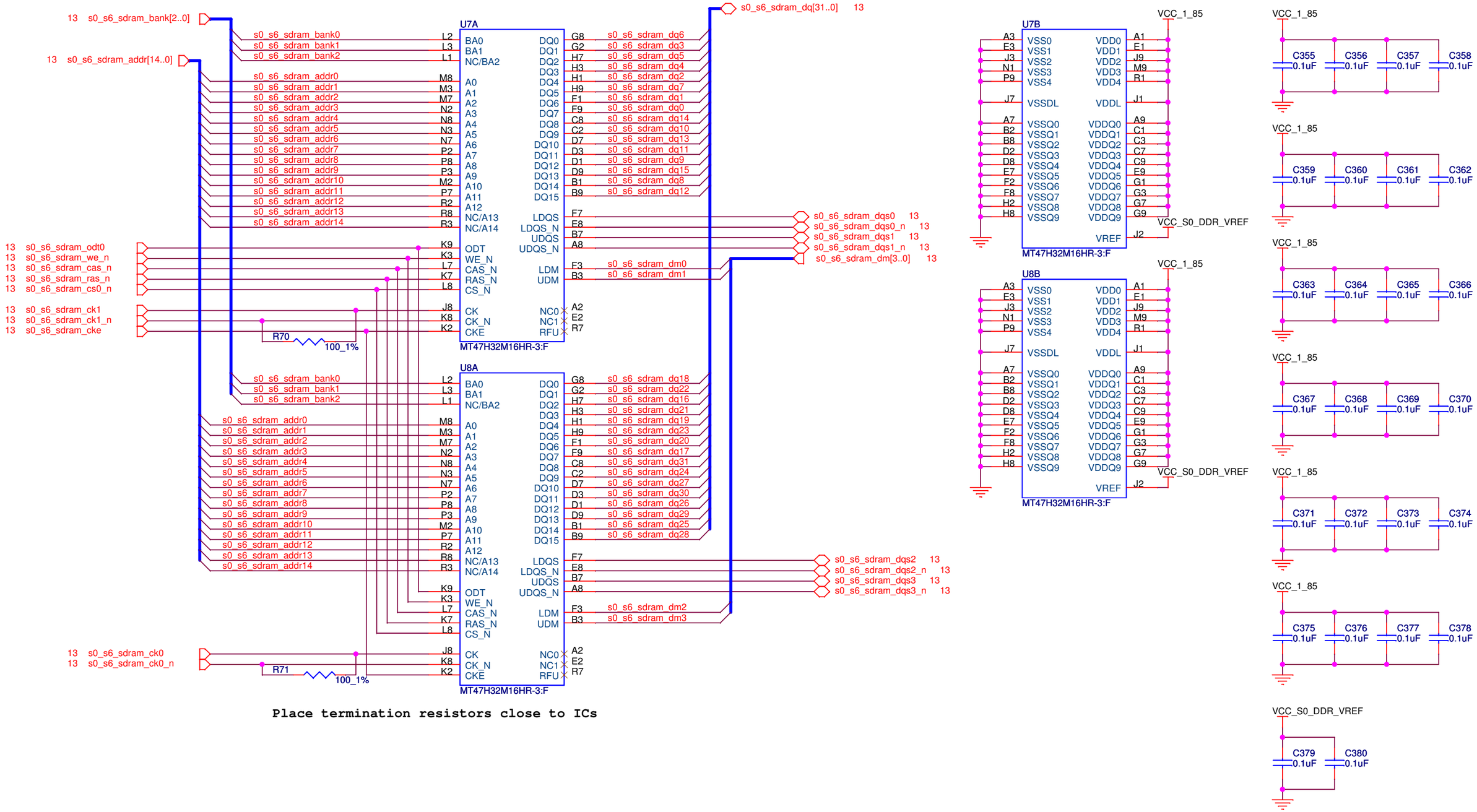

Place termination resistors close to ICs

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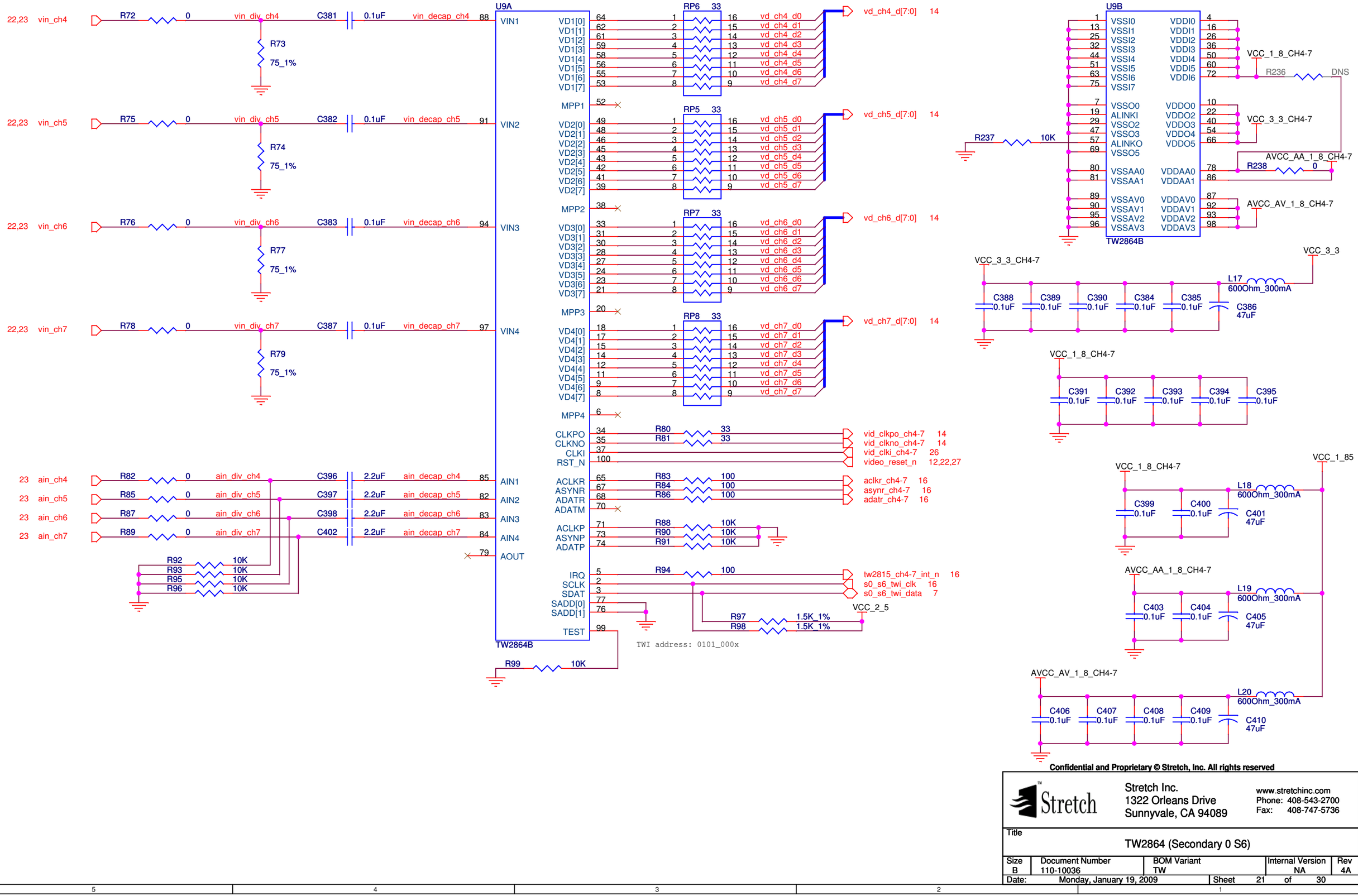
DDR ICs (Secondary 0 S6)				
Size: B	Document Number: 110-10036	BOM Variant: TW	Internal Version: NA	Rev: 4A
Date: Monday, January 19, 2009		Sheet 20 of 30		



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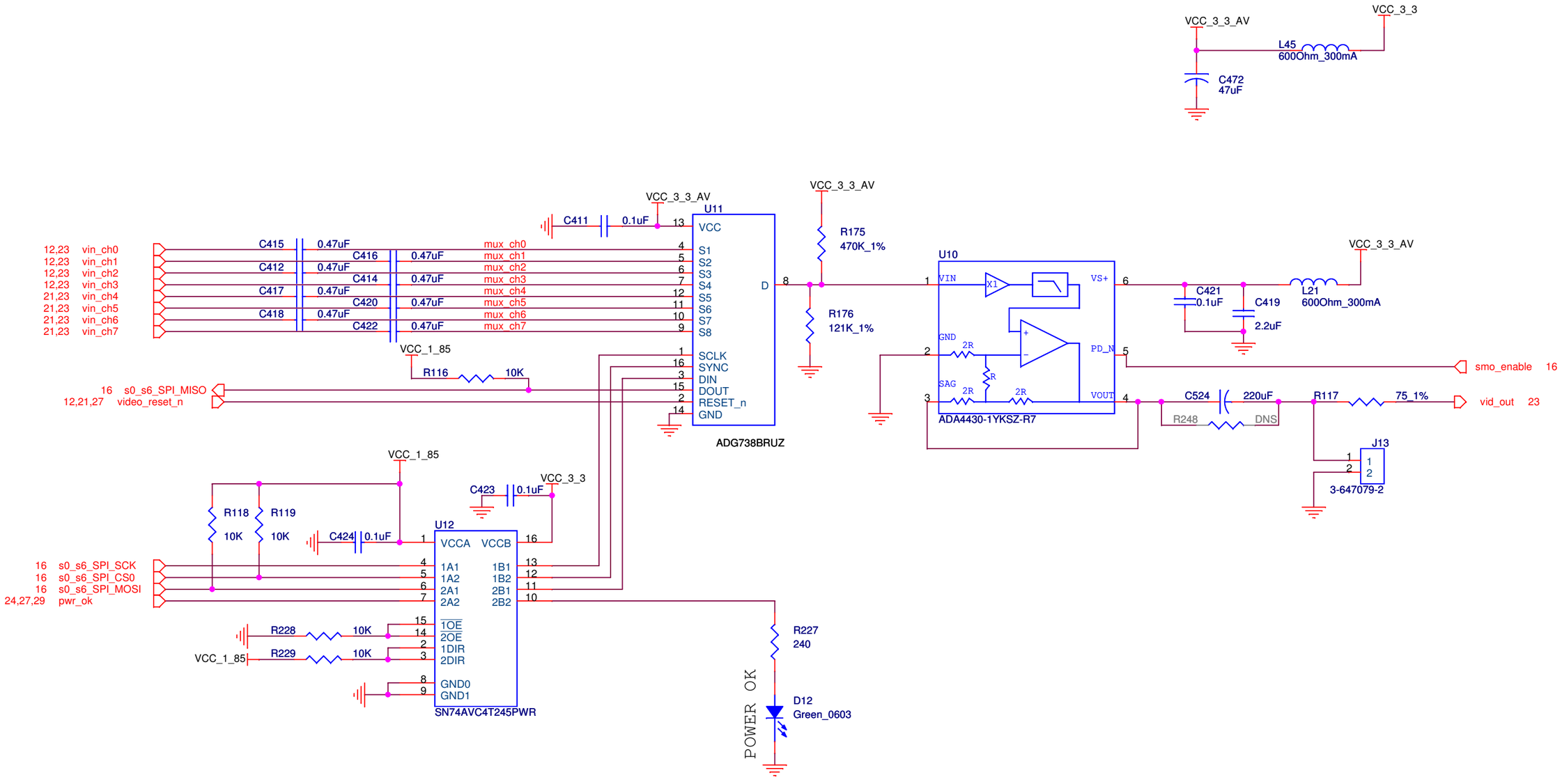
Title: TW2864 (Secondary 0 S6)

Size	Document Number	BOM Variant	Internal Version	Rev
B	110-10036	TW	NA	4A

Date: Monday, January 19, 2009 Sheet 21 of 30



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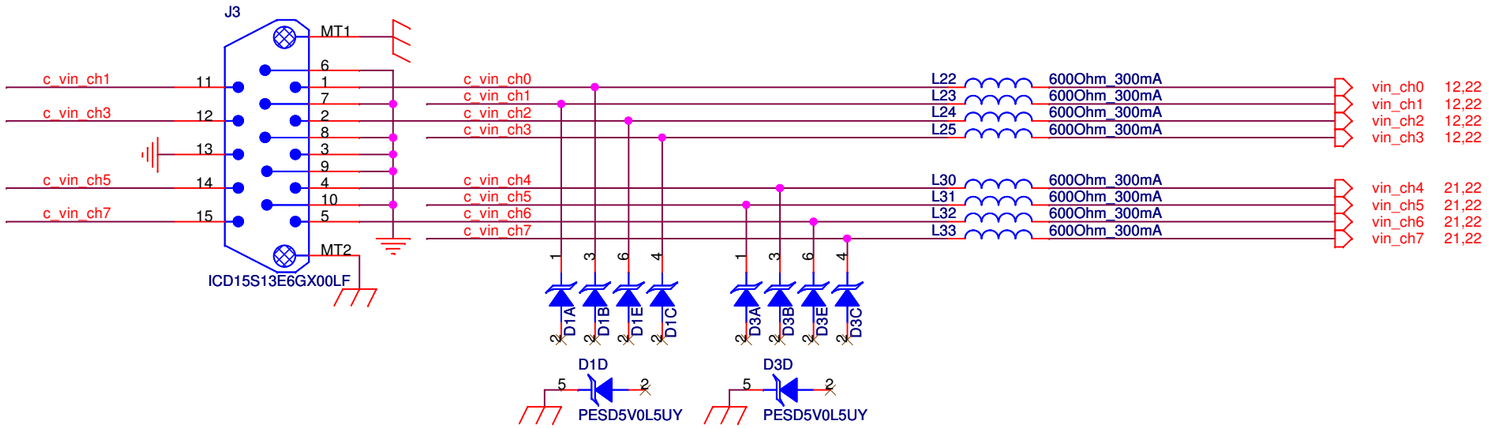
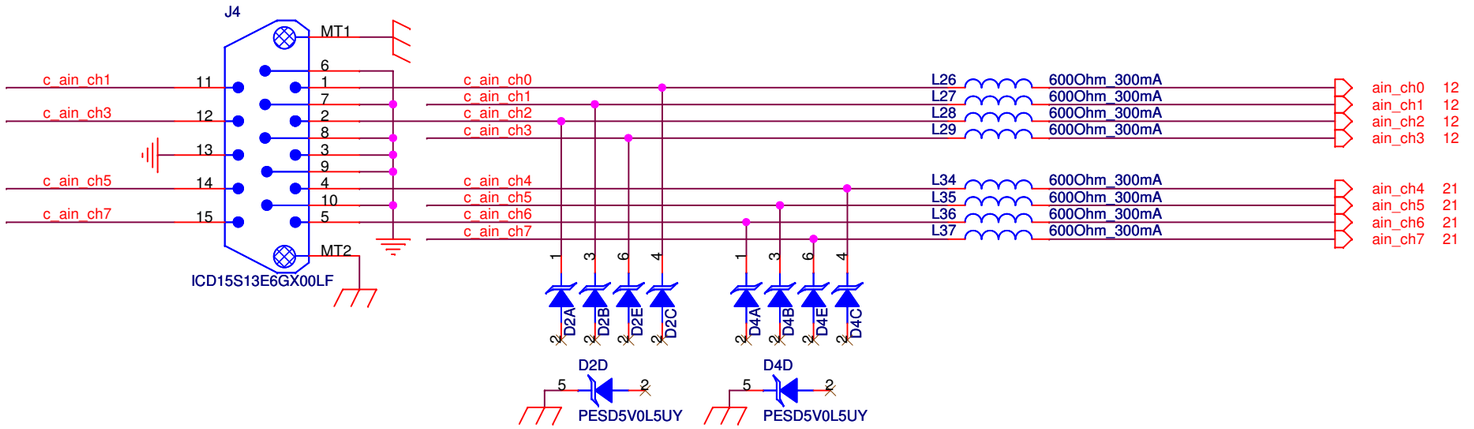
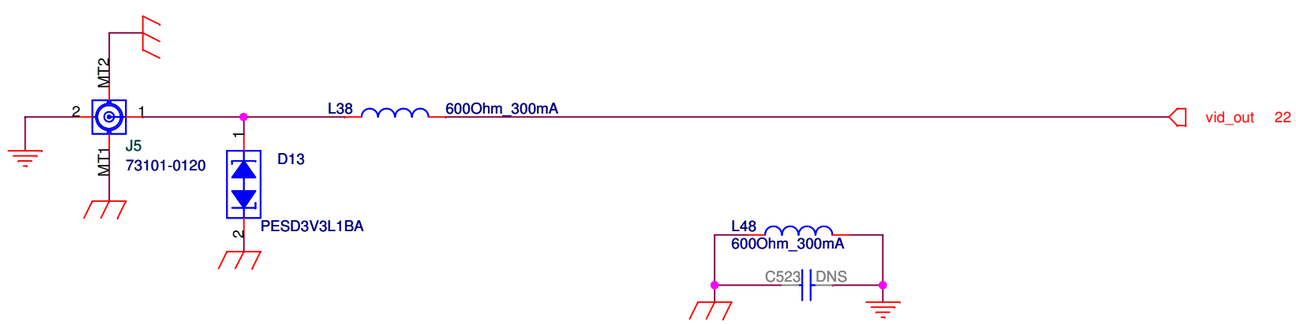
Title: Video Out

Size	Document Number	BOM Variant	Internal Version	Rev
B	110-10036	TW	NA	4A

Date: Monday, January 19, 2009 | Sheet 22 of 30







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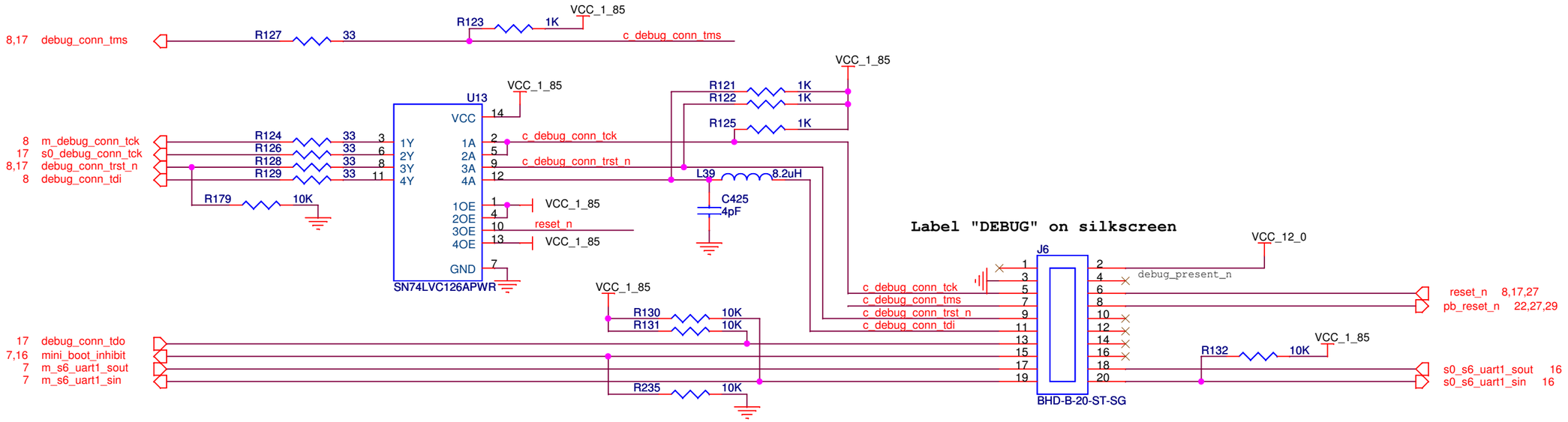
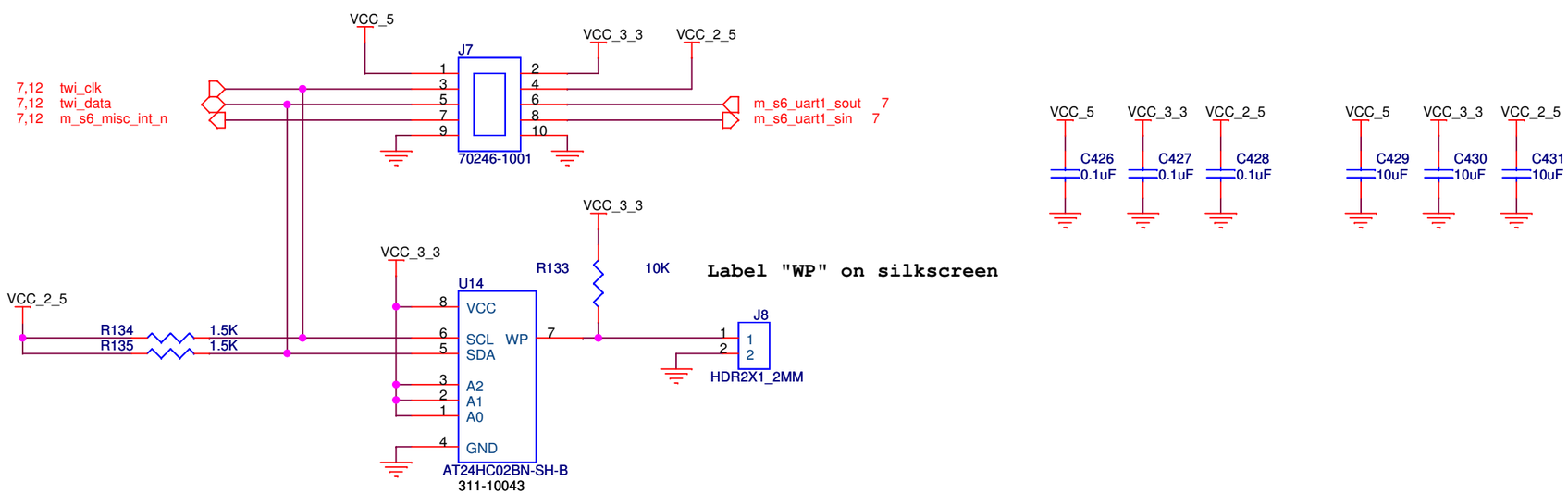
Title: Video and Audio Connectors

Size	Document Number	BOM Variant	Internal Version	Rev
B	110-10036	TW	NA	4A

Date: Monday, January 19, 2009 | Sheet 23 of 30





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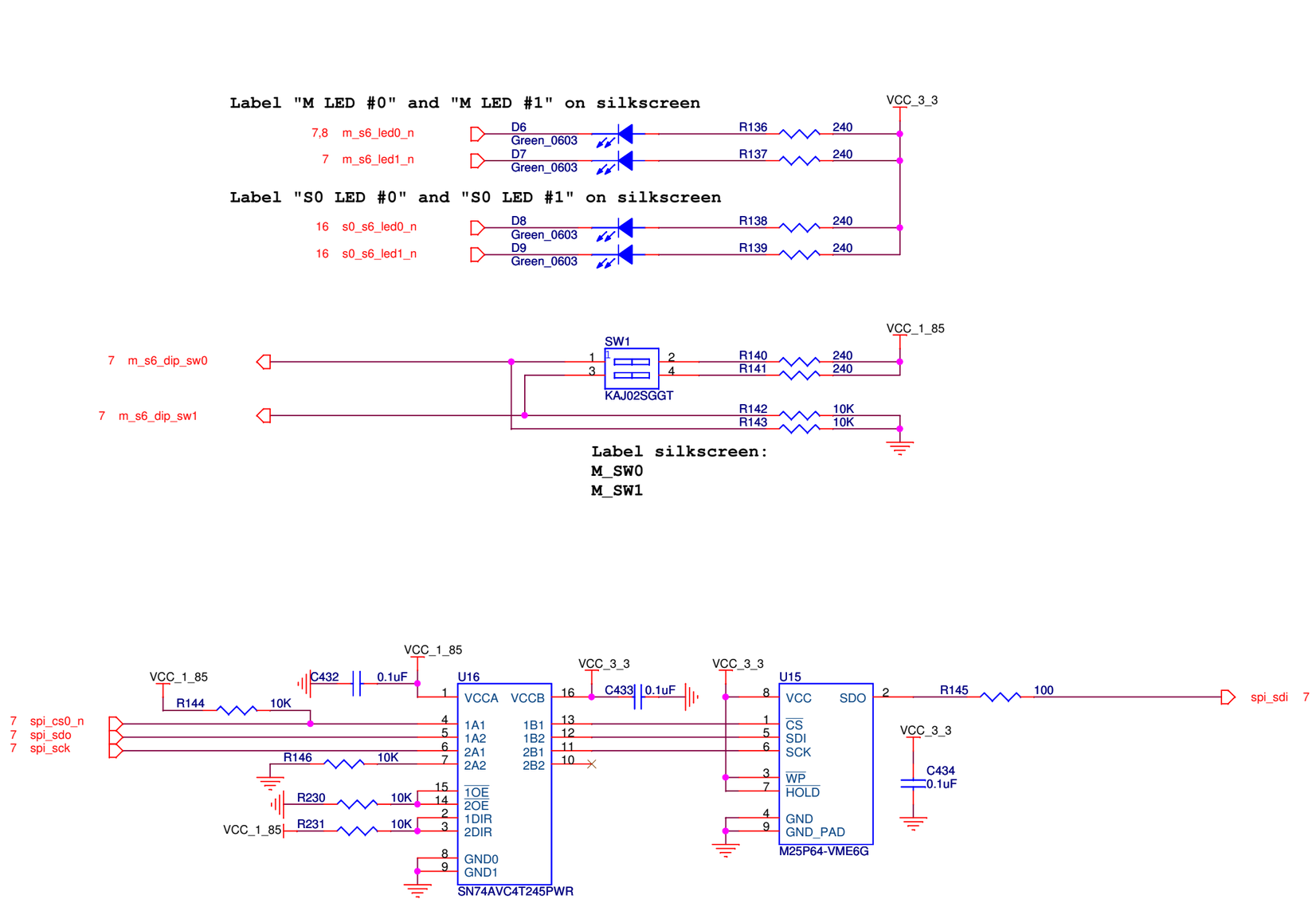
Title: TWI EEPROM, I/O, & Debug Connectors

Size	Document Number	BOM Variant	Internal Version	Rev
B	110-10036	TW	NA	4A

Date: Monday, January 19, 2009 Sheet 24 of 30



Test components are not populated in production system.

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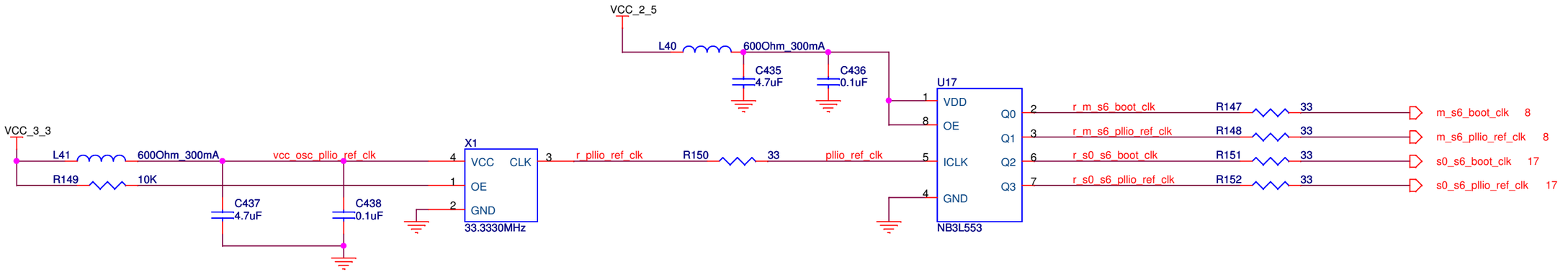
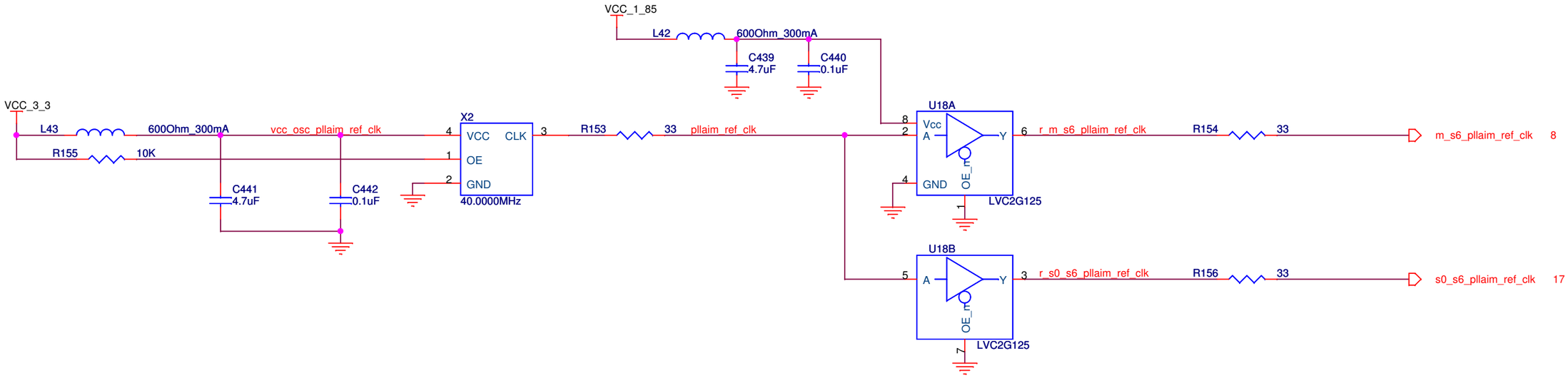
Title: Flash & Misc

Size	Document Number	BOM Variant	Internal Version	Rev
B	110-10036	TW	NA	4A

Date: Monday, January 19, 2009 | Sheet 25 of 30





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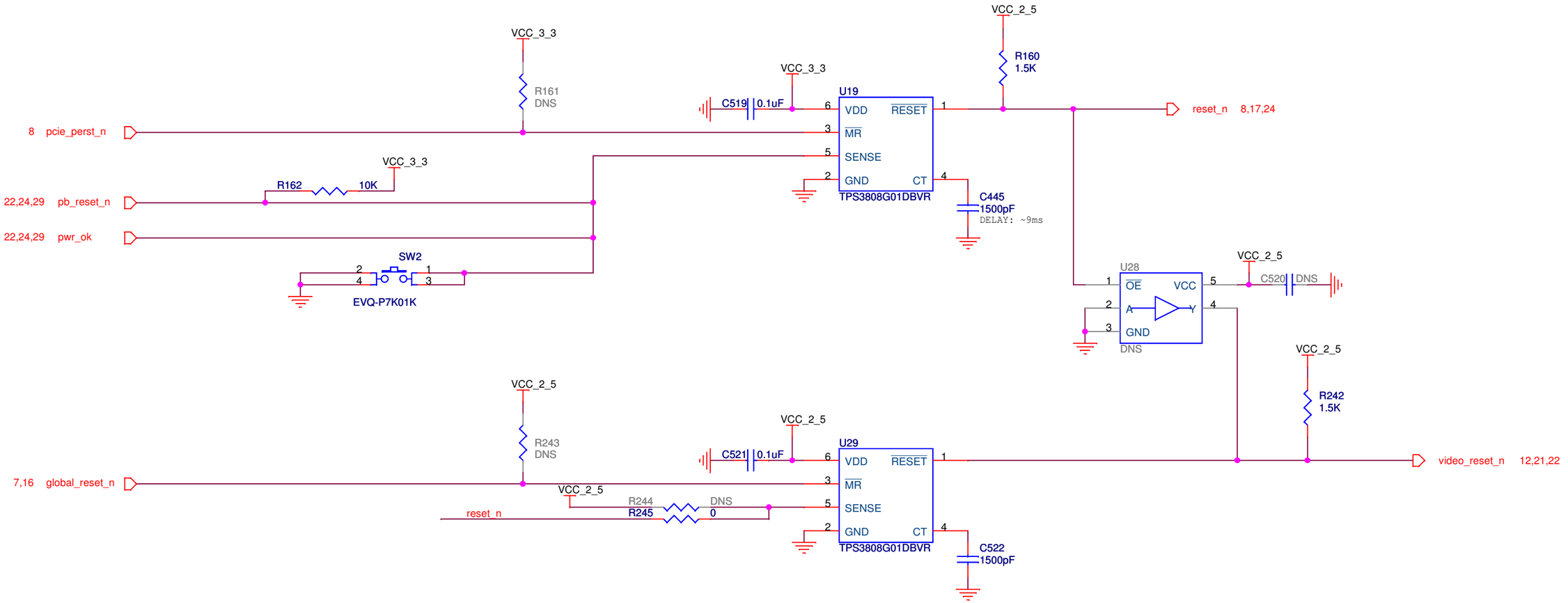
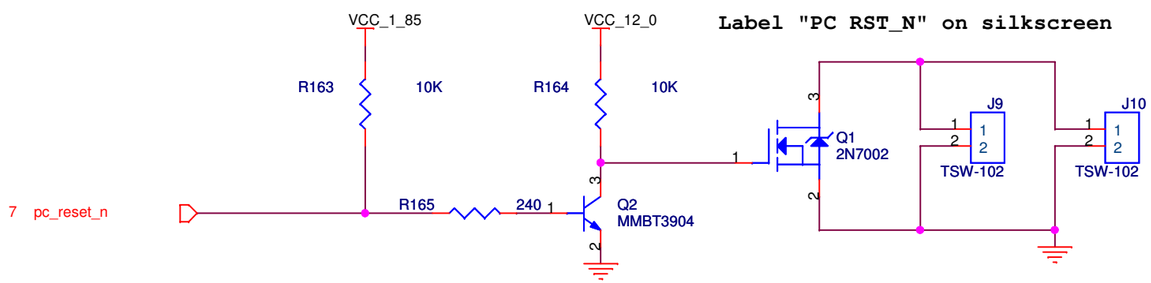
Title: Clocks

Size	Document Number	BOM Variant	Internal Version	Rev
B	110-10036	TW	NA	4A

Date: Monday, January 19, 2009 | Sheet 26 of 30





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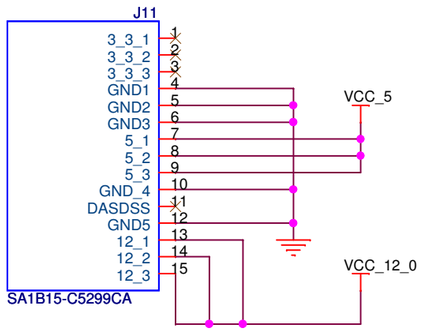
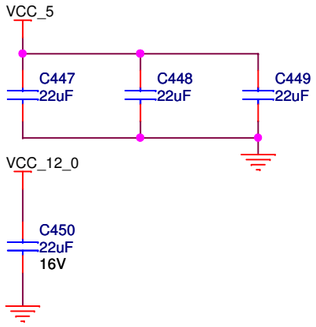
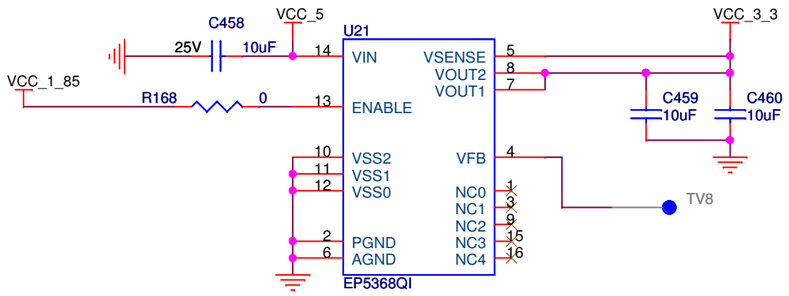
Title: Reset

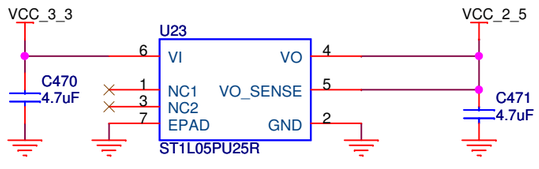
Size	Document Number	BOM Variant	Internal Version	Rev
B	110-10036	TW	NA	4A

Date: Monday, January 19, 2009 Sheet 27 of 30









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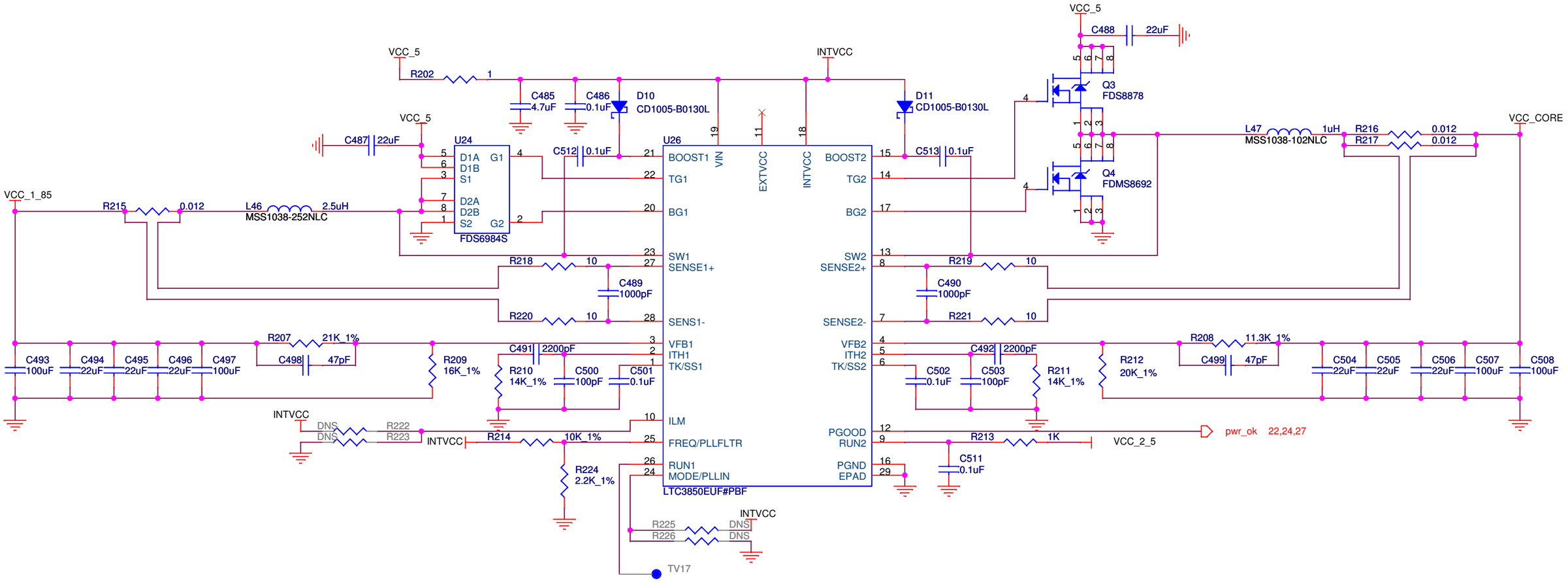
Title: System Power 1

Size	Document Number	BOM Variant	Internal Version	Rev
B	110-10036	TW	NA	4A

Date: Monday, January 19, 2009 | Sheet 28 of 30



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Title: System Power 2

Size	Document Number	BOM Variant	Internal Version	Rev
B	110-10036	TW	NA	4A

Date: Monday, January 19, 2009 Sheet 29 of 30

Revision History

Revision	Date	Description
3A	11/05/08	- Remove video output mux input bias and bias at the mux output - Add cascade header - Move FAN_TACH connection to GPIO3 and use GPIO7 to enable SMO
4A	1/09/09	- Changed SMO output buffer - Changed PC_RESET_N header type to 0.1"
	1/20/10	- Add NVP1104 Variant option

```
NET_PHYSICAL_TYPE:
POWER
-> Current carrying traces.
AVIDEO
-> Analog video signals
AAUDIO
-> Analog audio signals
100HM_DIFF
-> Differential signals (100 ohm).


NET_SPACING_TYPE:
WX1P5_GAP
-> 1.5x trace width spacing
WX2_GAP
-> 2.0x trace width spacing
WX2P5_GAP
-> 2.5x trace width spacing
WX3_GAP
-> 3.0x trace width spacing
WX5_GAP
-> 5.0x trace width spacing
AAUDIO
-> analog audio signal (3x trace width spacing)
AVIDEO
-> analog video signals (3.75x trace width spacing)
```

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Title				
Revision				
Size: B	Document Number: 110-10036	BOM Variant: TW	Internal Version: NA	Rev: 4A
Date: Tuesday, January 20, 2009		Sheet 30 of 30		