Stretch S6 D1 PCIe DVR

Data Sheet

Version 1.0

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Chapter 1 Introduction

Stretch PCI Express (PCIe) DVR boards are the most efficient, cost effective, and flexible way of accruing large amounts of video data, compressing it in a space-effective data format, and transferring that data to a network or data storage device.

The Stretch PCIe DVR board, associated software development kit, and reference design use four Stretch S6000 series processors to take in up to 16 channels of D1 data and compress them into H.264 or other high data density formats. The PCIe interface for this board is intended to output this data to a host PC for storage on a hard drive.

Figure 1-1 and Figure 2-1 on page 2-1 are block diagrams of the PCIe DVR design and its companion I/O board. These two boards make up the DVR system. The main PCIe DVR board contains all video input, processors, and PCIe logic, and the IO board holds an assortment of peripheral functions such as RS485 and alarm inputs and outputs.

1.1 Description

This document describes the hardware details of Stretch's PCI Express (PCIe) DVR board. The DVR board is a standard, one-half length, one-lane PCIe card. It can display and record 16 video channels and 16 audio channels. In addition, the board is designed to support 16 channels of alarm input–output and an RS485 interface for remote camera control. The DVR board features:

- Support for 1–16 D1 input video channels, each with audio
- One S6100 processor
- Three S6105 processors
- One output video channel (SMO) with two modes of operation
  - NXP SAA7121 video out encoder with on-screen display (OSD) and tiling
  - Selectable analog video channel input loop back for video out without OSD or tiling
- An I/O connector that supports up to 16 alarm inputs and outputs and RS485

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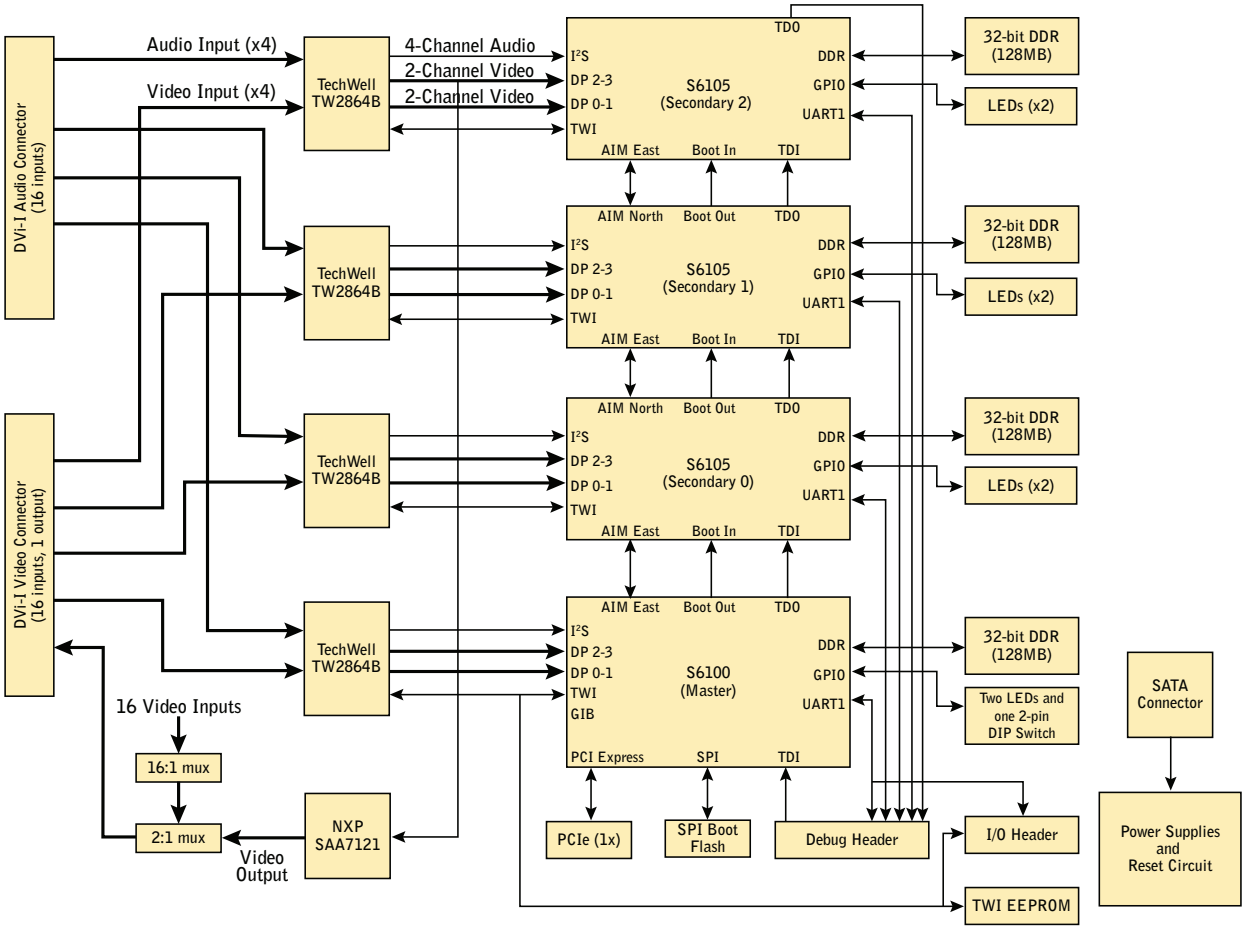
- Debug connector for UART and JTAG interfaces
- SATA power connector

Figure 1-1 PCIe DVR Board Block Diagram



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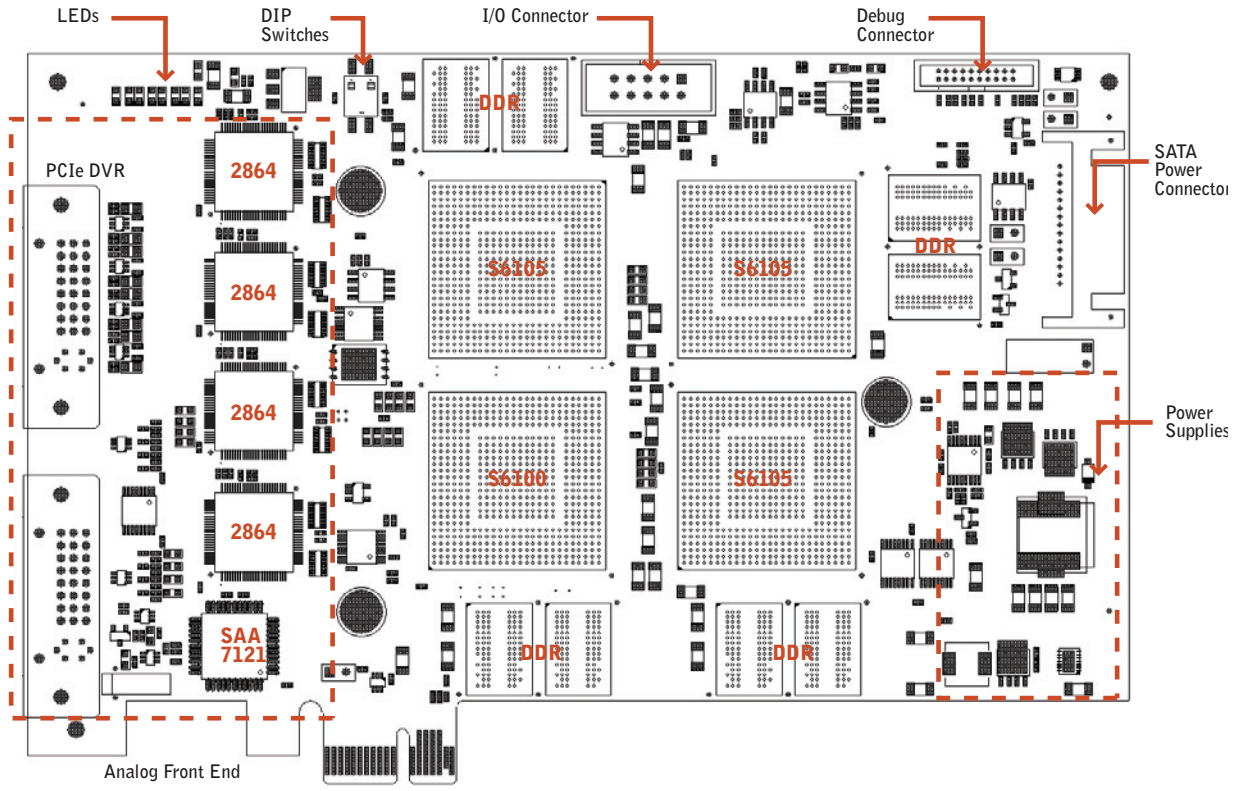
Chapter 2 Functional Descriptions

The PCIe DVR design includes the following:

- Analog front end (video and audio)
- PCI Express
- S6 processor complex
- Clocks
- Power and reset
- Miscellaneous

The following sections describe each of these features and the I/O board in more detail.

Figure 2-1 DVR Board Layout



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2.1 Analog Front End

The analog front end consists of audio and video decoders and CODECs.

2.1.1 Video Input

The analog video decoder and audio A/D used is the Techwell TW2864B. The TW2864 includes four high-quality NTSC/PAL/SECAM video decoders that convert analog composite video signal to digital component YCbCr data for security applications. The TW2864 contains four 10-bit ADC and proprietary clamp and gain controllers, and uses 4H comb filter for separating luminance and chrominance to reduce cross noise artifacts. The TW2864 adopts the image enhancement techniques such as IF compensation filter, CTI and programmable peaking. The TW2864 also includes an audio CODEC that has four audio analog-to-digital converters and one digital-to-analog converter. A built-in audio controller can generate digital outputs for recording and mixing, and accepts digital input for playback. The playback feature is not used in this design.

Four TW2864B ICs are used in this design. Each part takes four video inputs and converts them to a ITU-R BT.656 format 8-bit data stream. The TW2864B can operate the digital output ports in several modes. This design uses the time multiplex option. In this mode, the 8-bit data streams are clocked at a 54MHZ rate, and the CLKP and CLKN clocks operate at 27MHz.

For the 16 D1 PCIe DVR board, each TW2864B outputs two separate digital video ports. Each port has two multiplexed video channels that are demultiplexed by capturing them with the CLKNO and CLKPO clock outputs from the Techwell device. Each data port from the Techwell device is connected to two data ports on each S6. This is necessary to clock in each video channel of the multiplexed TW2864B data port. One video channel is clocked in with the CLKP and the other channel is clocked in with the CLKN clock.

The clock output on the TW2864B can be delayed to adjust the setup and hold times seen on the S6 (up to a maximum of 15ns with 1ns increments for multiplexed mode, and up to 30ns with 2ns increments for standard mode). This feature is controlled by the four S6 processors through the TWI and the application software.

The `DUAL_CH` register enables the dual ITU-R BT.656 time-multiplexed format and the `SEL_CH` register selects another channel output to be multiplexed with its own channel on each digital output port pins. Figure 2-2 illustrates the timing in the case of `CH1` and `CH2` time-multiplexed output through `CH1` video output port.

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Figure 2-2 Timing Diagram of Two-channel Time-multiplexed Format at 54MHz

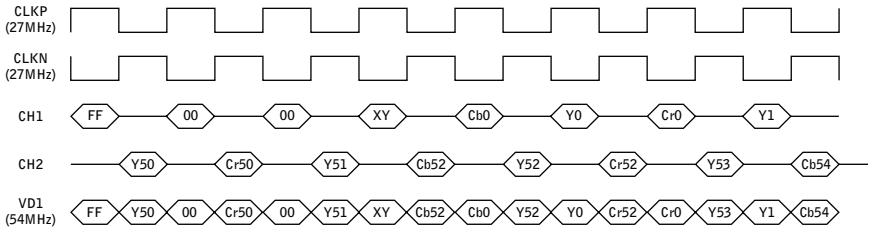
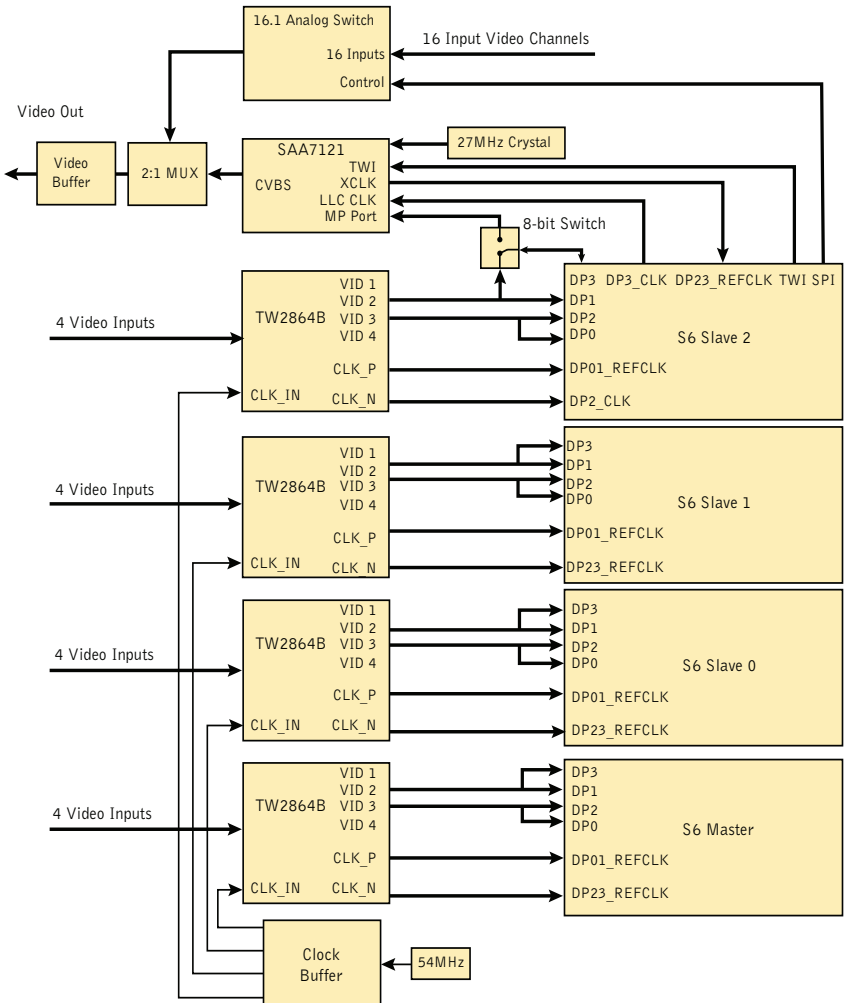


Figure 2-3 on page 2-3 illustrates the flow of data from the Techwell devices to the S6 processors.

Figure 2-3 16 D1 PCIe DVR Video Connections



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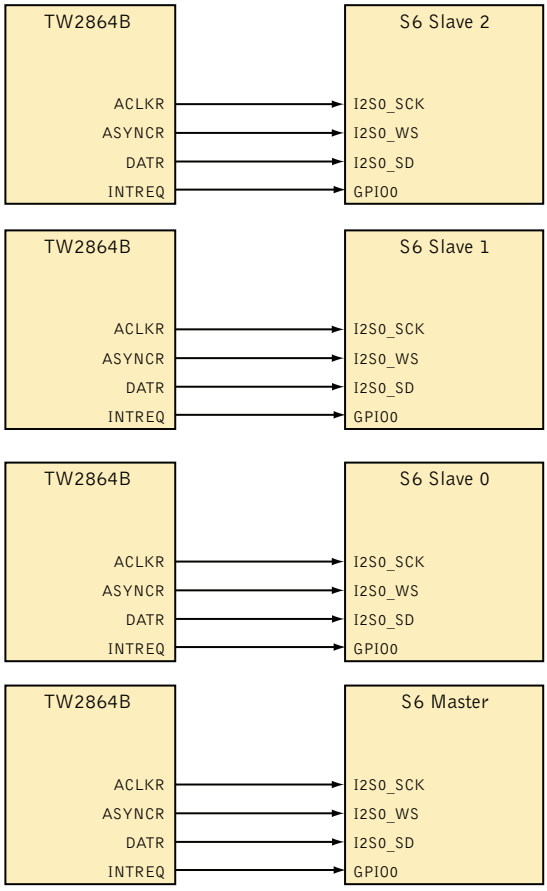
2.1.2 Audio Input

In the 16 D1 PCIe DVR board, each S6 receives audio data from its companion TW2864B. Using the I²S port, four audio channels per Techwell device are received and encoded. Figure 2-4 illustrates the audio connections on the 16 D1 S6 Processor Complex.

Figure 2-4 16 D1 PCIe DVR Audio Connections



To record audio data, the TW2864 provides the digital serial audio data through the ACLKR, ASYNR and ADATR pins. Sampling frequency comes from the 256xfs audio system clock setting. Even though the standard I²S and DSP format can have only two audio data on left and right channels, the TW2864 can provide an extended I²S and DSP format that can have 16-channel audio data through ADATR pin. The ASYNR signal is always fs frequency rate. One ASYNR period is always equal to 256 ACLKR clock lengths. Figure 2-5 on page 2-17 shows the digital serial audio data organization for multi-channel audio. Refer to the Techwell 2864 spec for more information.

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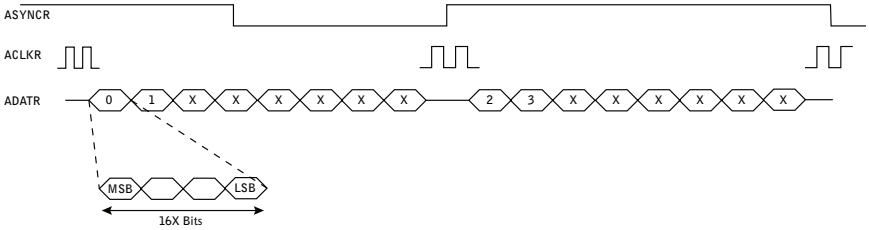
Figure 2-5 Digital Serial Auto Data Stream



2.1.3 Video Output

The video out function has two modes of operation. The first, and default mode, is a video input loopback through an output buffer. The 16 video inputs are connected to a 16-to-1 multiplexer that is controlled by the application. Any one of the inputs can be selected in either a rolling fashion where all 16 inputs are cycled through, or a single input can be selected to be the output source. This mode does not support tiling or OSD.

The second mode of operation uses the Slave 2 S6105's Data Port 3 as an output to drive the SAA7121 encoder by NXP. This mode has the extra features of video output tiling and OSD information. The SAA7121 is controlled by the TWI bus from the Slave 2 S6 chip. The host video application controls in which mode the video out (SMO) is operating. The Slave 2 processor handles all video out functions. This mode supports only 15 channels of video input.

2.2 PCI Express

The PCIe DVR board is a 1x link width, standard height (111.15mm maximum), half length (167.65mm maximum), card. This interface's physical implementation (decoupling, trace skew, and so on) follows the guidelines in the *PCI Express Card Electromechanical Specification, Revision 1.1, Chapter 4, Electrical Requirements.*

2.3 S6 Processor Complex

In this design there are four S6 family processors (one S6100 and three S6105s). Each S6 is connected to two DDR2 ICs to achieve a 32-bit data bus. The data signals are terminated by the on-die terminations (ODT) on the S6 and DDR2 ICs. The clock is differentially terminated. The short trace lengths involved mean that none of the signals has series termination resistors.

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The DDR layout is done using a 10mm x 14mm 84-pin FBGA, which allows the greatest flexibility for compatible parts.

The PCIe DVR board has each of the S6s connected serially using AIM as depicted in Figure 1-1 on page 1-2. Each processor handles four video channels and four audio channels. The master processor is also used for the PCIe interface and alarm I/O functions. The Slave 2 processor handles all video out functions. Each processor passes video data to the next processor on the AIM interfaces.

2.4 Master Processor Connectivity

Each processor's various interfaces is described in the following sections.

2.4.0.1 Master Processor

The master S6100 is also referred to as *Processing Element 0* (PE0). Its interfaces are:

- Multi-purpose AIM WEST/DDR is used for the DDR2 interface
- Multi-purpose AIM SOUTH/DP is used in data port mode. Data Ports 0 and 2 are connected to the companion Techwell Video Data Port 3. Data Ports 1 and 3 are connected to the companion Techwell Video Data Port 2.
- Multi-purpose AIM NORTH/GIB is not used
- Multi-purpose AIM EAST/GPIO miscellaneous functions is used in AIM mode and is connected to S6105 Slave 0's AIM EAST port
- PCIe is connected to the PCIe connector
- I^2S bus is connected to the Techwell digital audio bus
- SPI bus is connected to the Flash chip
- TWI bus is connected to the Techwell, IO connector, and EEPROM chips
- UART1 is connected to the Debug/JTAG connector
- Dedicated GPIO pins (refer to Table 2-3 on page 2-14)

2.4.0.2 Slave 0 Processor

The S6105 Slave 0 processor is also referred to as PE1.

- Multi-purpose AIM WEST/DDR is used for DDR2 interface
- Multi-purpose AIM SOUTH/DP is used in the data port mode. Data Ports 0 and 2 are connected to the companion Techwell Video Data Port 3. Data Ports 1 and 3 are connected to the companion Techwell Video Data Port 2.

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- Multi-purpose AIM NORTH/GIB is used in the AIM mode and is connected to Slave 1 S6105 AIM EAST
- Multi-purpose AIM EAST/GPIO, miscellaneous functions is used in the AIM mode and is connected to master S6100 AIM NORTH port
- PCIe is unused
- I²S bus is connected to the Techwell digital audio bus
- SPI bus is unused
- TWI bus is connected to the Techwell
- UART1 is connected to the Debug/JTAG connector.
- Dedicated GPIO pins (refer to Table 2-2 on page 2-10)

2.4.0.3 Slave 1 Processor

The S6105 Slave 1 processor is also referred to as PE2

- Multi-purpose AIM WEST/DDR is used for DDR2 interface
- Multi-purpose AIM SOUTH/DP is used in the Data Port mode. Data Ports 0 and 2 are connected to the companion Techwell Video Data Port 3. Data Ports 1 and 3 are connected to the companion Techwell Video Data Port 2
- Multi-purpose AIM NORTH/GIB is used in the AIM mode and is connected to Slave 2 S6105 AIM EAST
- Multi-purpose AIM EAST/GPIO, miscellaneous functions is used in the AIM mode and is connected to Slave 0 S6105 AIM NORTH port
- PCIe is unused
- I²S bus is connected to the Techwell digital audio bus
- SPI bus is unused
- TWI bus is connected to the Techwell
- UART1 is connected to the Debug/JTAG connector
- Dedicated GPIO pins (refer to Table 2-2 on page 2-10)

2.4.0.4 Slave 2 Processor

The S6105 Slave 2 processor is also referred to as PE3

- Multi-purpose AIM WEST/DDR is used for DDR2 interface
- Multi-purpose AIM SOUTH/DP is used in the Data Port mode. Data Ports 0 and 2 are connected to the companion Techwell Video Data Port 3. Data Ports 1 and 3 are connected to the companion Techwell Video Data Port 2.
- Multi-purpose AIM NORTH/GIB is unused

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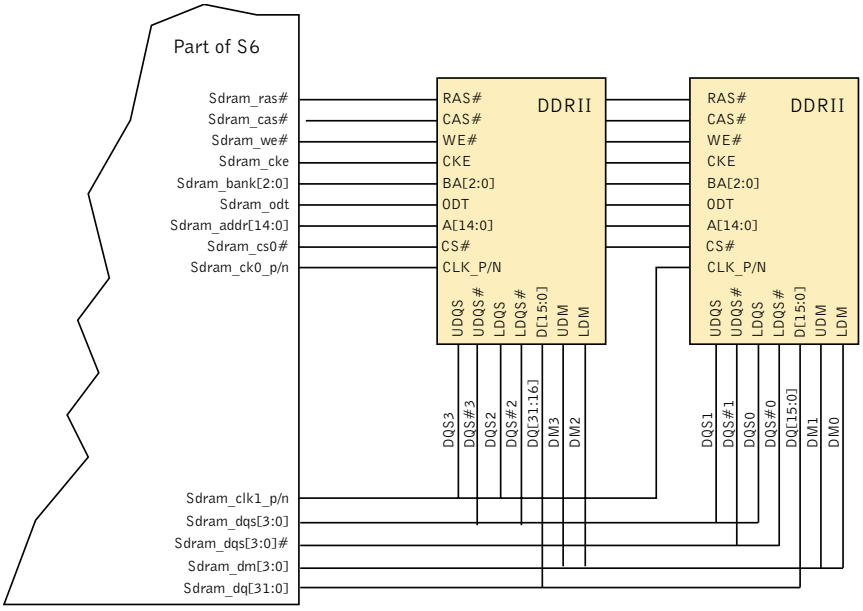
- Multi-purpose AIM EAST/GPIO, miscellaneous functions is used in the AIM mode and is connected to Slave 1 S6105 AIM EAST port
- PCIe is unused
- I²S bus is connected to the Techwell digital audio bus
- SPI bus is connected to the analog video input 16:1 mux
- TWI bus is connected to the Techwell and the NXP SAA7121 video out encoder
- UART1 is connected to the Debug/JTAG connector
- Dedicated GPIO pins (refer to Table 2-3 on page 2-14)

2.5 DDR

Data path termination is provided by the S610x and the DDR2 memory device's On-Die-Termination (ODT) functions. The clock is terminated as is appropriate for differential paired signals. The trace lengths between S610x and DDR2 are short, so no series termination is used. The DDR devices are connected directly to the S610x devices. All DDR signals are routed serially. The DDR physical spacing and control line connections are made such that several BGA packages and densities can be used. All processors have identical DDR implementations.

Figure 2-6 DDR2 Signal Diagram



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2.6 Clocks

The clocks are generated by surface mount oscillators with their outputs buffered and distributed to the different devices on the board. Table 2-1 defines the clocks required in the system. The `S6_PLLAIM_CLK` buffer also feeds the `S6_PLLSYS_CLK` pin of the S6 chips.

Table 2-1 Clock Frequencies

Name	Frequency	Stability	Max TIE Jitter
S6 boot_clk	33.333 MHz	50ppm	50ps
S6 pllio_ref_clk	33.333 MHz	50ppm	50ps
S6 pllsys_ref_clk	40 MHz	50ppm	50ps
S6 pllaim_ref_clk	40 MHz	50ppm	50ps
TW2864B CLKI	54 MHz	25ppm	-

Figure 2-7 Clock Distribution

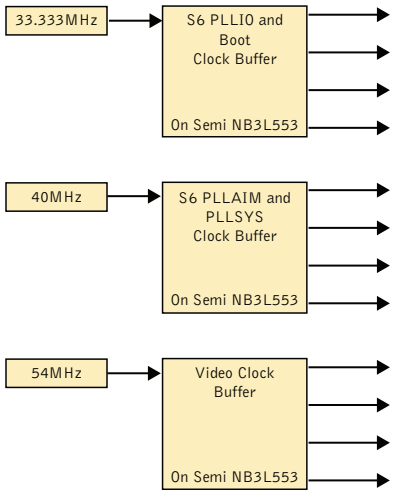

Figure 2-7 illustrates the clock distribution using 1-to-4 clock buffers.

The Data Port clock connections are described in Section 2.1, “Analog Front End”, on page 2-2.

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2.7 Power and Reset

The power for the DVR design is supplied from the SATA connector. Table 2-2 lists the different rails used in the design. The total power consumption for the design is approximately 25 watts, depending on software and data set.

2.7.1 DC Parameters

Table 2-2 lists the DC parameters for the DVR board.

Table 2-2 PCIe DVR DC Parameters

Name	Usage	Min	Typical	Max	Units
VCC12	Main power rail	23.8	23.8		Watts
VCC5	IO relay rail, reset circuit		1.0	3.0	Watts[1]
VCC3_3	TW2864B, Misc. circuits	1	1.0		Watts
VCC2_5	S6, Misc. circuits	.21	.21		Watts
VCC1_8	S6, DDR, TW2864B	7.2	7.2		Watts
VCC1_2	S6 core	13.2	13.2		Watts
Analog inputs	Audio and video inputs	.5	1.0	1.35	VDC

[1] If all 16 are active

2.7.2 Power Generation

The main power comes through the SATA connector. The SATA connector provides 12V, 5V, and 3.3V. The SATA connector was chosen because it is quickly replacing the older IDE connector as the general power connector inside a PC. The provision of 3.3V on this connector also means that the DVR does not need to generate this voltage onboard, saving money. The 12V rail is used to generate the 1.2V and the 1.8V rails. The 3.3V rail is used to generate 2.5V. The 5V rail is used to power some of the logic on the IO board, as well as some of the reset logic (Texas Instruments TL7702). The 3.3V supply for the video and audio circuits is a filtered version of the SATA's 3.3V. There is an option to use the 5V rail to drive the 3.3V that is used for the audio and video circuits. These components are not loaded and this is strictly provided as a fallback plan in case PCs with extremely noisy 3.3V rails are encountered.

The PCIe DVR board can be completely powered from a SATA disk drive connector. There is a provision for the use of an IDE-to-SATA converter for power. If this IDE-to-SATA converter is used, then there will be no 3.3V on the SATA connector that plugs into the DVR card, because there is no 3.3V on an IDE connector. There is a jumper, J13, which controls a load switch. When this

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jumper is installed, the load switch turns on and the 3.3V from the PCIe connector is used in place of the SATA's 3.3V source. No other power is used from the PCIe connector. Power must always be connected to the SATA connector. The 3.3V from the PCIe connector is not used otherwise.

2.7.3 Power Sequencing

The four power rails are sequenced in the following way. 1.8V comes up first. This in turn enables a load switch that turns on 3.3V. The 3.3V is then sent to an LDO that controls 2.5V. The 2.5V controls the enable for the 1.25V. Reset is released approximately 100ms after 1.25V is up.

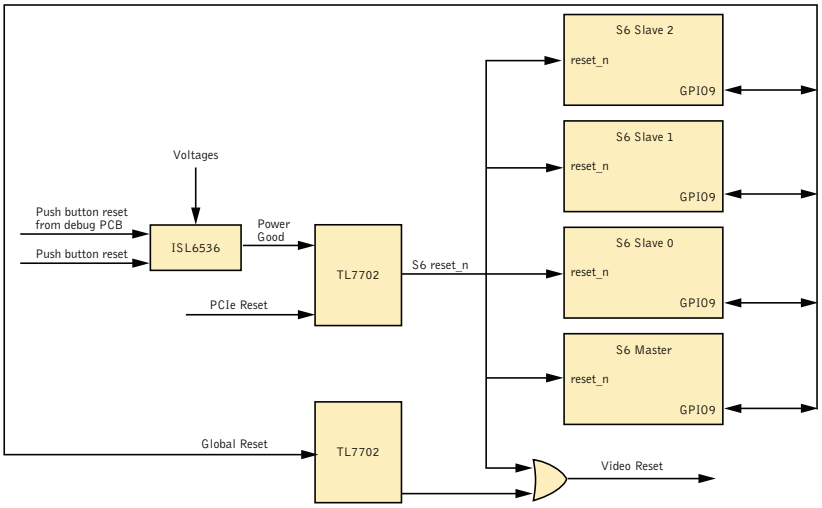
Graphically, the sequence is: 12V > 1.8V > 3.3V > 2.5V > 1.25V.

2.7.4 Reset Generation

An Intersil ISL6536 supervisor IC is used to monitor the power rails. The power good signal from the ISL6536 is connected to the sense input of a Texas Instruments TL7702, which generates a reset signal to the board components. The `global_reset_n` input/output from the S6s are connected together (open drain) and are used as a soft reset to each other and a secondary reset TL7702 IC. This soft reset does not assert the main `reset_n` signal on the S6s, but resets the video components in the system. Figure 2-8 on page 2-11 shows a block diagram of the reset circuit. A reset switch is located on the debug board along with the OCD and UART connectors.

A green LED is used to provide a visual power-on indication. There is also a red LED that is off in normal operation but turns on to indicate a power failure or main reset condition.

Figure 2-8 Board Reset



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2.8 Miscellaneous

The following sections describe the function of SPI and boot, TWI, GPIO, I/O board connectors, and debug connectors.

2.8.1 SPI

There are two SPI devices on the board. The first device is the SPI boot Flash, and is attached to the master S6. Details of this device are as follows:

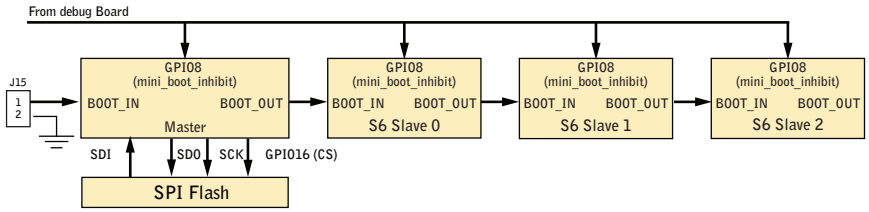
- M25P64 from STMicroelectronics
- 8MB Flash
- 8-pin VDFPN package (8mm x 6mm)

The second SPI device is the video input loop back multiplexer, and is connected to the Slave 2 S6105. The 16:1 multiplexer is actually two Analog Devices ADG738B 8:1 ICs with separate chip selects. GPIO 17 (SPI CS1) and GPIO 18 (SPI CS2) are used to select between two groups of eight video inputs.

2.8.2 Boot

Figure 2-9 on page 2-12 shows the boot chain and the Flash device on the DVR board. The `boot_inhibit` signal (GPIO 8) is connected to the debug board and can be used to stop the processors from loading code from the Flash device. A second method of inhibiting the boot sequence is to install jumper J15. If J15 is installed, some conservative default settings will be loaded instead and then waits for OCD (on-chip debugging) to take control. Jumper J15 should be installed only in the case of corrupted boot Flash data.

Figure 2-9 Boot Chain



The boot sequence for the Master S6 is summarized in Figure 2-10. Slave S6s have a similar sequence except that the Boot-in signal is controlled by the upstream S6. Instead of loading the application from Flash, the slaves are configured into AIM mode and wait for the master to give them instructions over the AIM bus.

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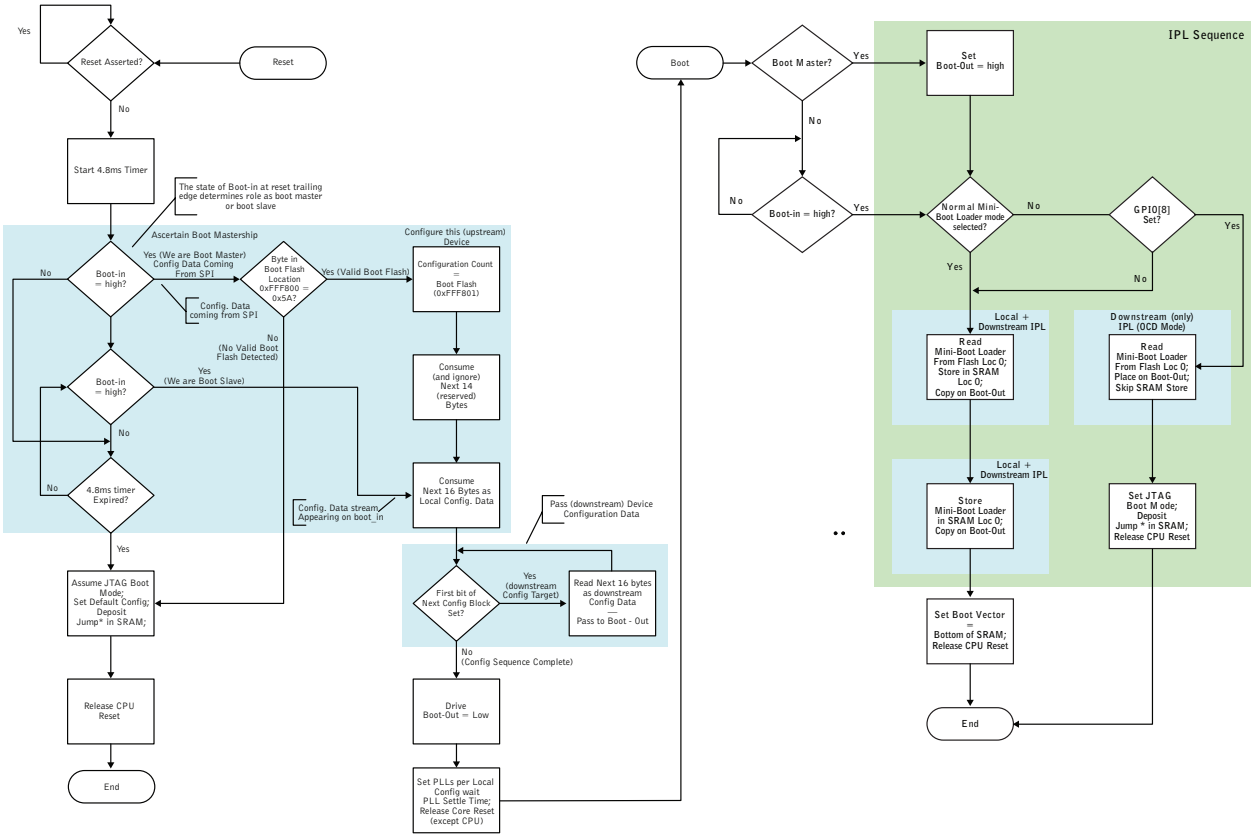
Figure 2-10 Boot Sequence



2.8.3 TWI

The Master S6 devices are as follows:

- Serial EEPROM used for manufacturing data (write protected)
  - AT24C02B-10TU-1.8 from Atmel
  - TWI address: `0x1010_0xxx` (selected through DIP a switch; `0x1010_011x` is the default)
- TW2864B
  - TWI address: `0x0101_000x`
- PCA9535 (TWI register, located on first I/O board)
  - TWI address: `0x0100_000x` (DIP switch selectable, default is `0x0100_000x`)
- PCA9535 (TWI register, located on second I/O board)
  - TWI address: `0x0100_001x` (DIP switch selectable, default is `0x0100_001x`)

The slave 0 devices are as follows:

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- TW2864B
  - TWI address 0x0101_000x

The slave 1 devices are as follows:

- TW2864B
  - TWI address 0x0101_000x

The slave 2 devices are as follows:

- TW2864B
  - TWI address 0x0101_000x
  - SAA7121 address 0x1000_100x

2.9 GPIO

Table 2-3 the GPIO pins and their functions for each processor.

Table 2-3 DVR GPIO Connections

	Function as Implemented per S610x			
Name	**S6 Master**	**S6 Slave 0**	**S6 Slave 1**	**S6 Slave 2**
GPIO0	TW2864B and I/O Board Interrupt (input)	S6 Master Interrupt (input)	S6 Master Interrupt (input)	S6 Master Interrupt (input)
GPIO1	S6 Slave 0 Interrupt (input)	TW2864B Interrupt (input)	S6 Slave 0 Interrupt (input)	S6 Slave 0 Interrupt (input)
GPIO2	S6 Slave 1 Interrupt (input)	S6 Slave 1 Interrupt (input)	TW2864B Interrupt (input)	S6 Slave 1 Interrupt (input)
GPIO3	S6 Slave 2 Interrupt (input)	S6 Slave 2 Interrupt (input)	S6 Slave 2 Interrupt (input)	TW2864B Interrupt (input)
GPIO4	S6 Master Interrupt (output)	S6 Slave 0 Interrupt (output)	S6 Slave 1 Interrupt (output)	S6 Slave 2 Interrupt (output)
GPIO5	LED	LED	LED	LED
GPIO6	LED	LED	LED	LED
GPIO7	PC reset (output)	nc	nc	nc
GPIO8	mini_boot_inhibit	mini_boot_inhibit	mini_boot_inhibit	mini_boot_inhibit
GPIO9	global_reset_n	global_reset_n	global_reset_n	global_reset_n
GPIO10	s2_ocd_break_out (input)	m_ocd_break_out (input)	s0_ocd_break_out (input)	s1_ocd_break_out (input)
GPIO11	m_ocd_break_out (output)	s0_ocd_break_out (output)	s1_ocd_break_out (output)	s2_ocd_break_out (output)
GPIO16	spi_cs0_n	nc	nc	VOUT_DIG_SEL

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Table 2-3 DVR GPIO Connections

	Function as Implemented per S610x			
Name	**S6 Master**	**S6 Slave 0**	**S6 Slave 1**	**S6 Slave 2**
GPIO17	DIP SW0	nc	nc	S2_S6_SPI_CS0
GPIO18	DIP SW1	nc	nc	S2_S6_SPI_CS1

2.9.1 PC Reset

The PC reset function is provided in case you want to have a way to control the PC's motherboard reset signal. GPIO 7 from the Master S6100 processor can drive an FET, and pull the PC's reset signal low. The reset connections are at J10 and J11. These connectors are in parallel. Either one can be used. Pin 2 must be used for ground. This ground must be the same as the motherboard ground. Pin 1 (+) is the reset signal.

2.9.2 DIP Switch

There is a DIP switch, SW1, that can be use to select how the code boots. TABLEREF describes the usage of this switch. When diagnostic mode is selected, a copy of the diagnostic is loaded into each processor and run as an independent test. The pass/fail results from the slave processors are then sent back to the Master S6 (PE0) and displayed through the Master UART1 port.

Table 2-4 DIP Switch SW1 Settings

SW1 Position 1	SW1 Position 0	Function
Off	Off	Run built-in diagnostics and perform PCIe loopback test (requires a special test board)
Off	On	Run built-in diagnostics without PCIe loopback
On	Off	Boot normally and run code from Flash memory
On	On	Boot normally and run code downloaded from PCIe bus

2.10 Layout

The layout guidelines are embedded in the schematic. In general, the PCB is 10 layer, 4/4 trace spacing PCB with 1oz. and .5oz layers

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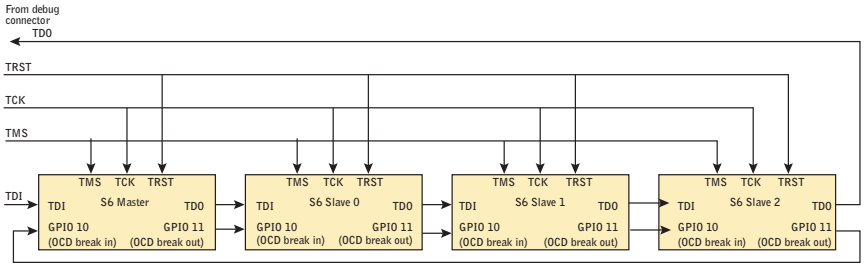
2.11 JTAG

For manufacturing and general debug purposes, a JTAG interface is available through the debug header. Figure 2-11 shows the JTAG chain.

Figure 2-11 OCD Chain



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2.12 DVR Connector Pin Outs

The following sections describe the DVR connector pin outs.

2.12.1 I/O Board Connector, J2

A 10-pin shrouded header is used to connect the DVR boards to an I/O board that provides alarms and RS-485/422 functionality. Table 2-5 lists the connector's pin-out.

Table 2-5 DVR I/O Board Connector Pin Out, J2

Pin #	Name	Function
1	VCC5	5V rail
2	VCC3_3	3.3V rail
3	twi_clk	TWI bus
4	VCC2_5	2.5V rail
5	twi_data	TWI bus
6	uart1_sout	RS-485/422
7	GPIO0	Interrupt
8	uart1_sin	RS-485/422
9	GND	Ground
10	GND	Ground

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2.12.2 Debug Connector, J1

The debug connector attaches the DVR board to Stretch's OCD debug board. Table 2-6 lists details of the connector.

Table 2-6 DVR Debug Board COnnector Pin Out, J1

Pin #	Name	Function
1	Reserved	No connect
2	VCC12_0	12V rail
3	GND	Ground
4	Presence detect	Unused
5	ocd_tck	OCD
6	Reset_n	Reset_n out to debug board
7	ocd_tms	OCD
8	Pb_reset_n	Reset_n input from debug board (push button)
9	ocd_trst_n	OCD
10	S2 uart1 sout	Slave #2 UART1 out
11	ocd_tdi	OCD
12	S2 uart1 sin	Slave #2 UART1 in
13	ocd_tdo	OCD
14	S1 uart1 sout	Slave #1 UART1 out
15	mini_boot_inhibit	OCD
16	S1 uart1 sin	Slave #1 UART1 in
17	M uart 1 sout	Master UART1 out
18	S0 uart1 sout	Slave #0 UART1 out
19	M uart1 sin	Master UART1 in
20	S0 uart1 sin	Slave #0 UART1 in

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2.13 SATA Connector, J17

Table 2-7 lists the SATA connections.

Table 2-7 SATA Connector, J17

Pin #	Name	Function
1	VCC33	3.3V Rail
2	VCC33	3.3V Rail
3	VCC33	3.3V Rail
4	GND	Ground
5	GND	Ground
6	GND	Ground
7	VCC5	5V Rail
8	VCC5	5V Rail
9	VCC5	5V Rail
10	GND	Ground
11	DAS/DSS	Unused
12	GND	Ground
13	VCC12	12V Rail
14	VCC12	12V Rail
15	VCC12	12V Rail

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2.14 DVR Jumpers

Table 2-8 lists the jumpers and their functions.

Table 2-8 DVR Jumpers

Jumper	Pin #	Description	Function
J13	1	1.8V	Load Switch Control J13 is used only when an IDE-to-SATA adapter is used. Place a 2-pin shunt at J13 to turn on the load switch that allows the PCI 3.3V source to be used.
	2	Load Switch En	
J15	1	Boot Inhibit	Boot Inhibit Place a 2-pin shunt at J15 to stop the DVR from booting from Flash. This is used for JTAG situations.
	2	Ground	
J3	1	Write Protect	Write Protect Left open, the upper half of the EEPROM is write protected. Place a shunt at J3 to enable writing to the upper half of the EEPROM.
	2	Ground	
J10, J11	1	Positive	PC Reset J10 and J11 are connected to each other in parallel. Connect J10 or J11 to the reset button or to the reset signal of the mother board.
	2	Negative Must be connected to ground	

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Chapter 3 I/O Board

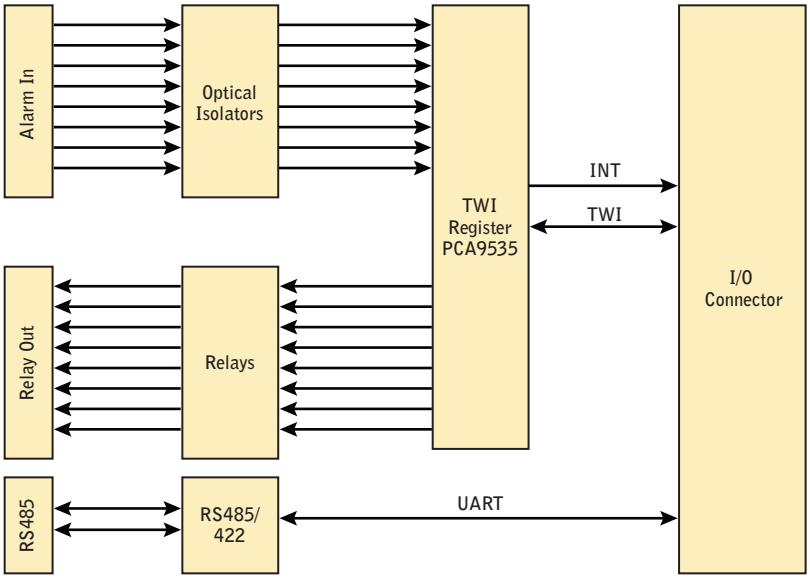
A separate I/O board provides alarm inputs and outputs as well as a half-duplex RS485/422 connection. The DVR system can support two of these I/O boards. It is not necessary to use the IO board if so desired. All the IO board interfaces are made available using an industry standard pluggable terminal block.

Figure 3-3 shows a block diagram of the I/O board. The master S6 UART1 port is connected to a RS-485/422 transceiver. This UART1 port is also shared with the Debug board for debug messages. So, if the UART is used for RS485, it will not display the normal boot text messages.

The I/O board features are:

- Half-duplex RS-485/422 port
- 8 alarm inputs (optically isolated)
- 8 alarm outputs (relays)
- PCA9535 TWI expander IC

Figure 3-1 I/O Board Block Diagram



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3.1 I/O Functional Overview

The following sections describe I/O functions on the DVR board.

3.1.1 Alarm Inputs

The alarm inputs can operate in two modes. In the default mode, the alarm inputs are active low. In this mode the inputs need to be grounded to create an alarm event and the opto-isolators are normally off. Place a jumper at J6 pins 1 and 2 to select this mode. This is also referred to as the *wet* mode.

The second mode is called the *dry* mode. In this mode the opto-isolators are normally on. To select this mode place a jumper at J6 pins 2 and 3. While in this mode the alarm inputs need to be driven high.

3.1.2 Alarm Outputs

When an alarm output is generated, a relay is closed and this pulls the alarm output low to ground. Table 3-4 on page 3-5 lists the electrical specifications for the alarm signals.

3.1.3 RS485

The RS485 is driven by the master S6 (PE0) UART 1 port. The RS485 transceiver is isolated through two Opto-Isolators. These Isolators impose a 19200KBs baud rate limitation. When the RS485 is used, the baud rate must be selected to match the slave to which it is talking, for example, a PTZ.

This UART 1 port is also used for general debug and boot messages through the debug connector. When this UART is used for RS485 functions, it will not be usable for other general messages. When booting, the UART 1 has a default baud rate of 38400KBs. Baud rates must be switched by software.

3.2 DIP Switches

There are two DIP switches on the I/O board, SW1 and SW2. SW1 controls the TWI address for the PCA9535 TWI expander IC and the AT25C01BN EEPROM. SW2 controls the RS485 termination.

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3.2.1 SW1

The TWI address's for the PCA9535 and the AT25C01BN are partially hard coded and partially selectable. SW1 is used to set the lower half of the address, the selectable part. The LSB is the read write bit and is controlled by software. When the address is changed by the use of SW1 both devices, PCA9535 and the AT24C01BN, are affected.

Table 3-1 SWI Address Settings

SW1 A1	SW1 A0	TWI Address PCA9535 0100_0[A1][A0] R/W		TWI Address AT24C01BN 1010_0[A1][A0] R/W	
0 (open)	0 (open)	0100_000x	40-41Hex	1010_000x	A0-A1Hex
0 (open)	1 (closed)	0100_001x	42-43Hex	1010_001x	A2-A3Hex
1 (closed)	0 (open)	0100_010x	44-45Hex	1010_010x	A4-A5Hex
1 (closed)	1 (closed)	0100_011x	46-47Hex	1010_011x	A6-A7Hex

If two IO boards are connected to one DVR board, then the SW1 settings must not be the same on both boards. This would cause a collision on the TWI bus. Set one I/O board for address 0100_000x and the other I/O board to address 0100_001x.

A PCA9535 TWI I/O expander is used to provide the signals required for the alarm input and output functions. This device provides 16 bits of GPIO, which are controlled through the TWI bus. If a pin is configured as an input, an interrupt can be enabled such that it is activated when the pin changes state. The interrupt pin of this device is connected to GPIO0 of the master S6.

Table 3-2 lists the PCA9535 IC connections.

Table 3-2 TWI I/O Expander Pin Out

Pin #	Name	Function
13	alarm_in0	Alarm input
14	alarm_in1	Alarm input
15	alarm_in2	Alarm input
16	alarm_in3	Alarm input
17	alarm_in4	Alarm input
18	alarm_in5	Alarm input
19	alarm_in6	Alarm input
20	alarm_in7	Alarm input
4	alarm_out0	Alarm output
5	alarm_out1	Alarm output

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Table 3-2 TWI I/O Expander Pin Out

Pin #	Name	Function
6	alarm_out2	Alarm output
7	alarm_out3	Alarm output
8	alarm_out4	Alarm output
9	alarm_out5	Alarm output
10	alarm_out6	Alarm output
11	alarm_out7	Alarm output

The pins on the PCA9535 are isolated from the alarm input signals by the use of opto-isolators. The alarm output signals are isolated using relays. This ensures that the on-board electronic circuits are protected from the external alarm voltages and currents.

The external alarms and RS-485/422 signals are connected to the board with industry standard connectors.

Table 3-3 I/O Board Alarm/Relay Connector Pin Out

Connector	Pin	Signal Name
J1	1	Relay 0 out
	2	Relay 1 out
	3	Relay 2 out
	4	Relay 3 out
	5	Relay 4 out
	6	Relay 5 out
	7	Relay 6 out
	8	Relay 7 out
	9	Ground
J5	1	Alarm in 0
	2	Alarm in 1
	3	Alarm in 2
	4	Alarm in 3
	5	Alarm in 4
	6	Alarm in 5
	7	Alarm in 6
	8	Alarm in 7
	9	Ground
J8	1	RS485 pos
	2	RS485 neg

Table 3-4 lists electrical characteristics for alarm I/O.

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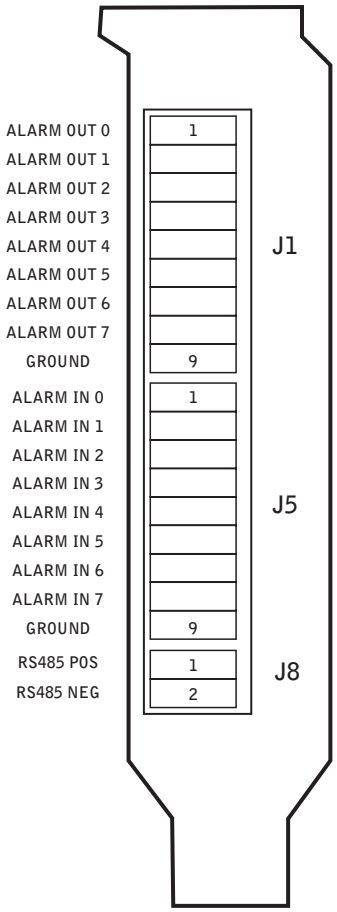
Table 3-4 DC Electrical Ratings – I/O

Absolute Maximum Ratings - Alarm I/O
All voltages referenced to GND. Alarm in trigger voltage is +7.5VDC.

Parameter	Symbol	Notes	Min	Typical	Max	Units
Alarm in trigger voltage	VIH	Dry mode	2.5	3.0	3.5	V
Alarm in current	IIH	Dry mode	2.5	3.0	3.5	MA
Alarm in current	IIL	Wet mode	3.2	3.0	3.7	MA
Alarm out		125VAC	-	-	.5	A
		24VDC	-	-	1.0	A
RS485 differential driver output	VOD		2.0	-	VCC(5V)	V
RS485 driver common-mode output voltage	VOC			VCC / 2	3.0	V

Figure 3-2 I/O Connector Pin Out Physical View



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3.2.2 SW2

SW2 is a four-position DIP switch. It is used to control the RS485 termination scheme. Use positions 1 and 2 together to get a Thevenin-equivalent, or dual-(split-) termination. Use position 4 alone to get the more common parallel differential termination.

Table 3-5 RS485 Termination

SW2 Position	Function	Default Setting
1	When closed, applies a 1K pull up resistor to the "POS" pin of the RS485 signal.	Closed
2	When closed, applies a 1K pull down resistor to the "NEG" pin of the RS485 signal.	Closed
3	Unused	Closed
4	When closed, applies a 120 ohm resistor across the "POS" and "NEG" pins of the RS485 pair. This is the most common setting.	Closed

3.3 Debug Board

The DVR system uses a debug board to provide a JTAG interface and a UART interface. The SDK uses a Catapult OCD module to download application code, diagnostics, and general software tool commands. The debug board has a DIP switch to select to which of the four processors' UART signals to connect. There is also a push button reset that will produce a power on reset scenario. The debug board contains the OCD connector used to connect to the Catapult, one UART port (connected through a DB-9), and the debug connector for the DVR board. Some signal level translation is performed on the debug board.

Debug board features:

- One UART channel that can connect to any of the S6 processors
- JTAG port for in-system debugging
- DIP switch for controlling boot operations
- DIP switch for UART selection

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3.4 Reference Documents

- PCI Express Card Electromechanical Specification, Revision 1.1
- Techwell 2864B specification.
- Stretch HMO user guide
- Maxim MAX13487

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