


16-D1 PCI Express Reference Design  
(Montserrat)

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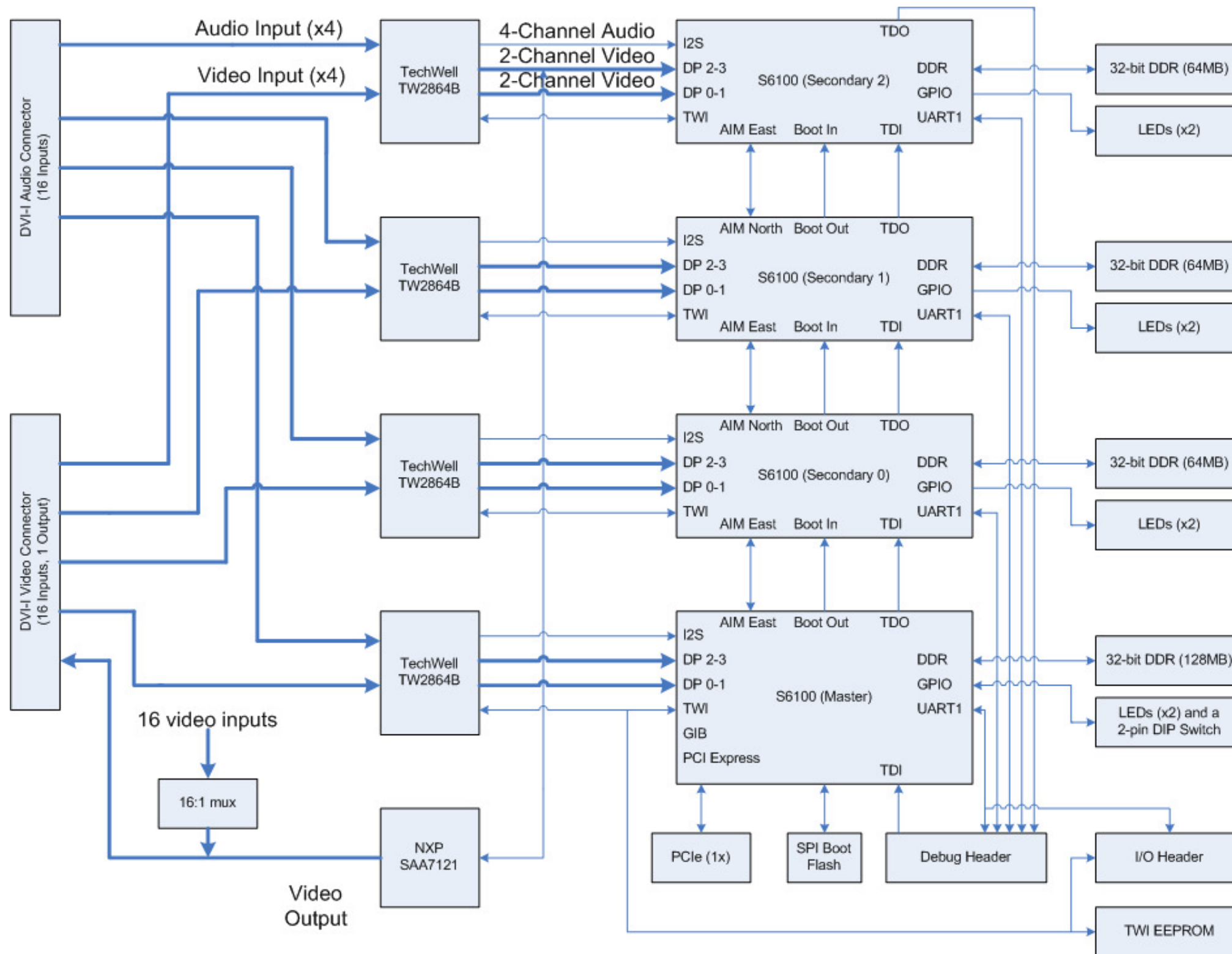
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Title				
Title Page				
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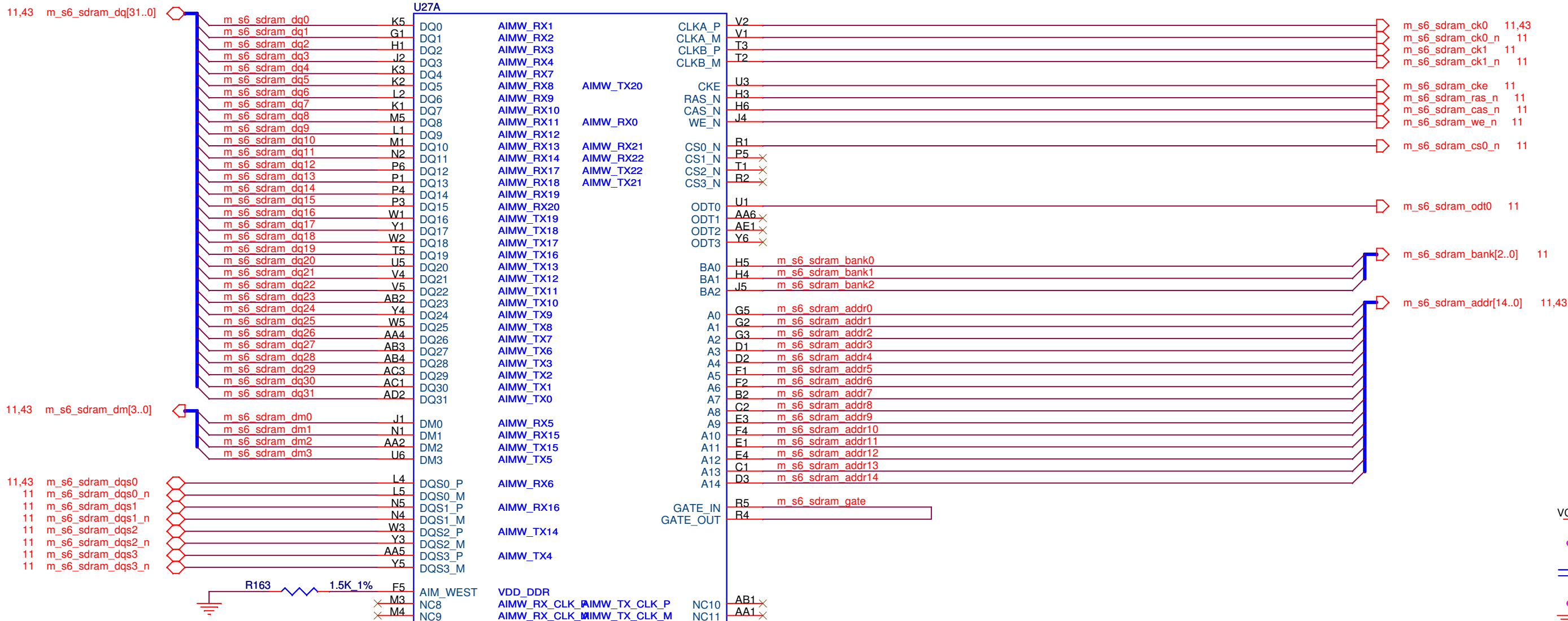
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Title				
Block Diagram				
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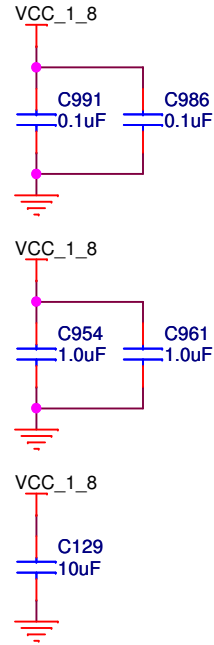
The following buses are embedded in the schematic:

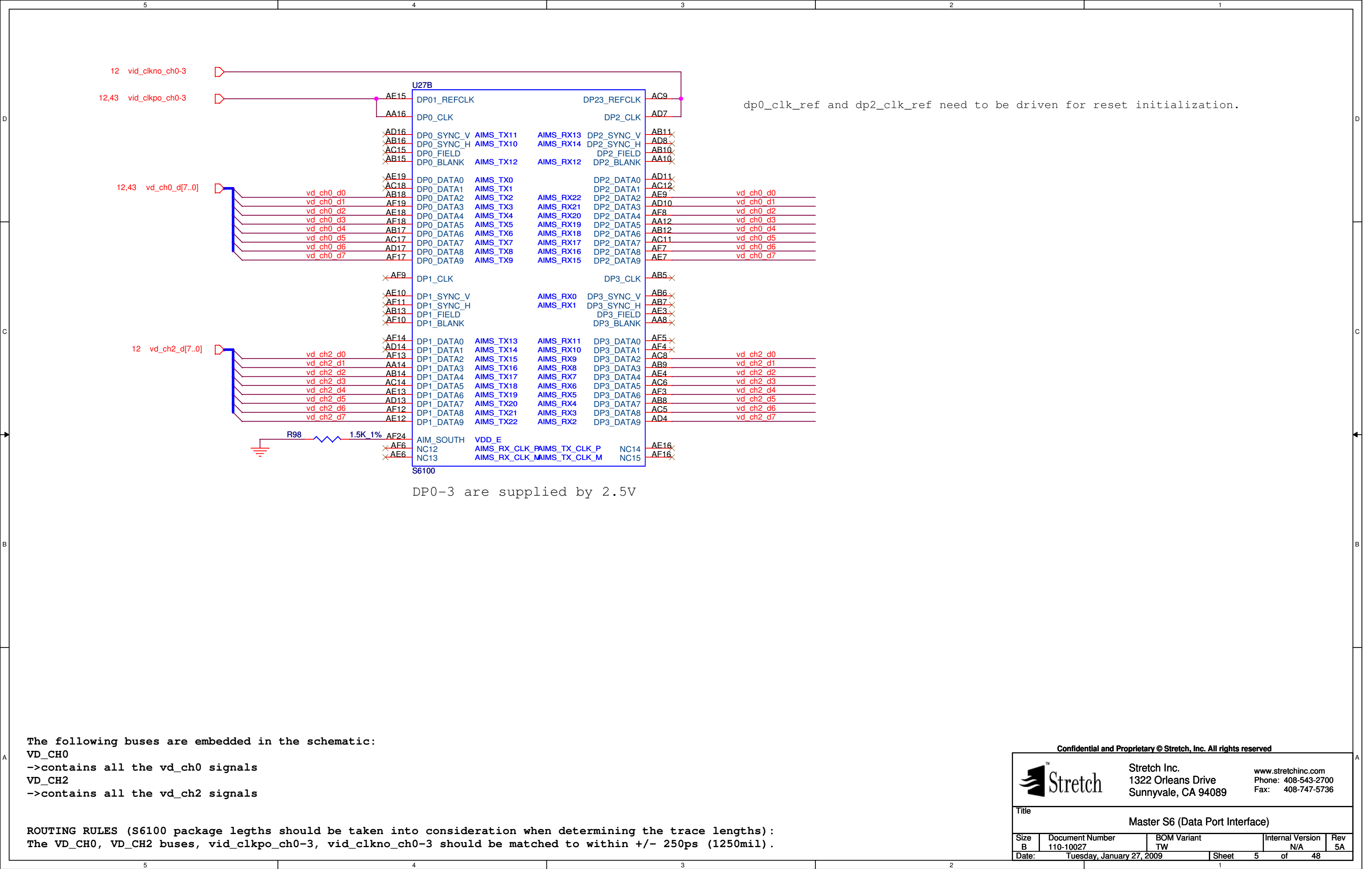
- M\_S6\_DDR\_DATA**  
->contains all the sdram\_dq, sdram\_dm, sdram\_dqs, and sdram\_dqs\_n signals
- M\_S6\_DDR\_CLK**  
->contains the sdram\_ck and sdram\_gate signals
- M\_S6\_DDR\_ADDR**  
->contains the sdram\_cke, sdram\_ras\_n, sdram\_cas\_n, sdram\_we\_n, sdram\_cs0\_n, sdram\_bank, and sdram\_addr signals

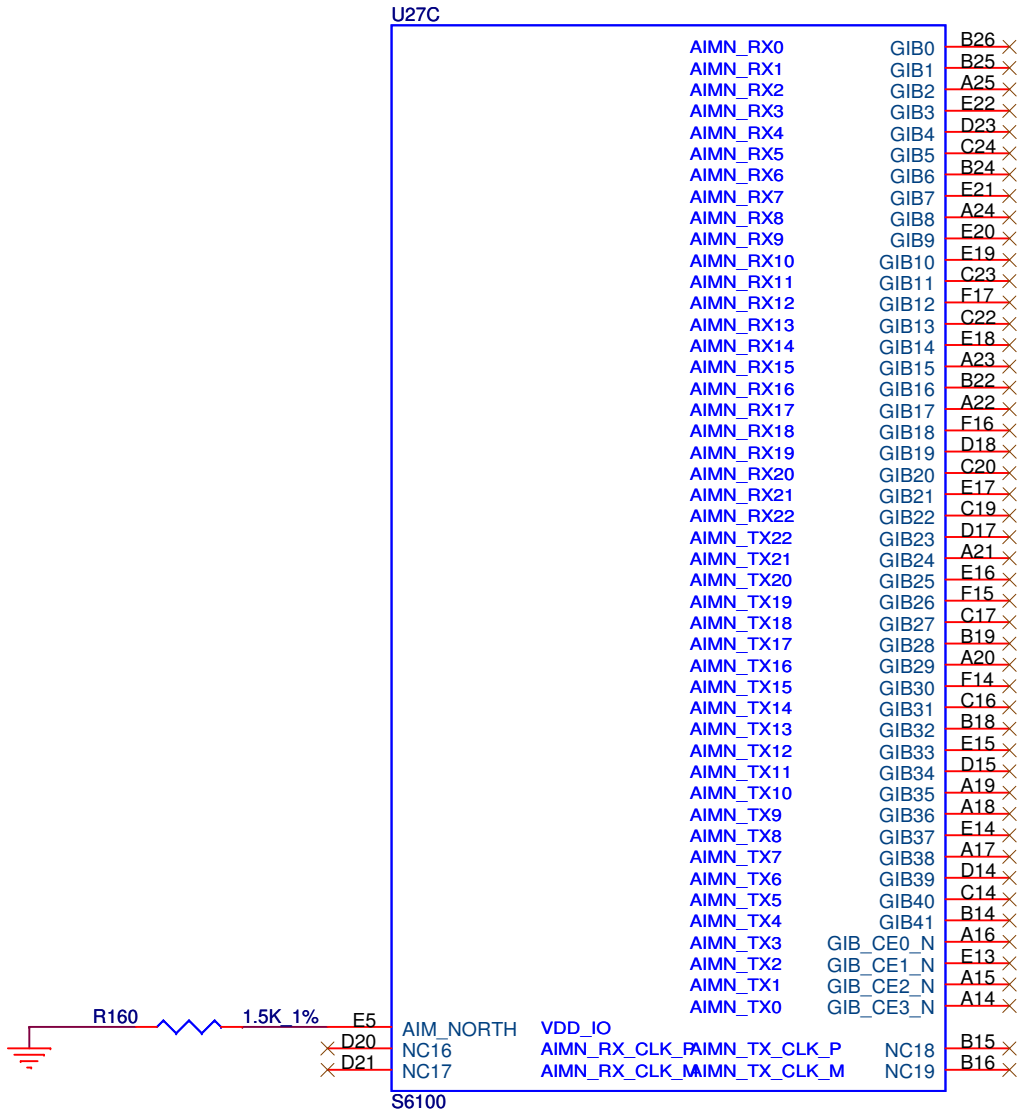
The following differential pairs are embedded in the schematic:

- M\_S6\_DDR\_DQS0
- M\_S6\_DDR\_DQS1
- M\_S6\_DDR\_DQS2
- M\_S6\_DDR\_DQS3
- M\_S6\_DDR\_CK0
- M\_S6\_DDR\_CK1

- ROUTING RULES (S6100 package legths should be taken into consideration when determining the trace lengths):
- 1) Differential pairs should be matched to within +/- 5ps (25mil) .
  - 2) The DDR\_ADDR bus and clocks should be matched to within +/- 75ps (375mil) .
  - 3) The DDR\_DATA bus should be matched to within +/- 50ps (250mil) .
  - 4) The signals in a byte lane should be matched to within +/- 30ps (150mil) and be routed on the same layer.
  - 5) The clocks and dqs signals should be matched to within +/- 100ps (500mil) .
  - 6) m\_s6\_sdram\_gate signal should be as short as possible and accesible using a via.







AIM NORTH IS POWERED FROM 1.8V

The following buses are embedded in the schematic:


GIB

->contains gib\_d[15:0], gib\_addr, gib\_wr\_n, gib\_rd\_n, and gib\_ce0\_n

ROUTING RULES (S6100 package legths should be taken into consideration when determining the trace lengths):

The GIB bus should be matched to within +/- 250ps (1250mil).

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Title

Master S6 (GIB Interface)

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ROUTING RULES (S6100 package legths should be taken into consideration when determining the trace lengths):

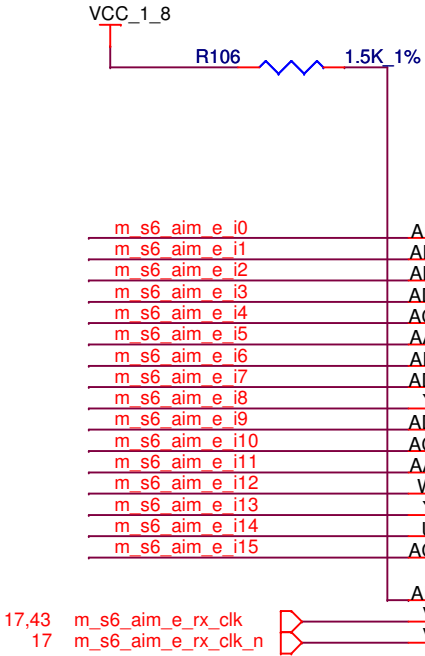
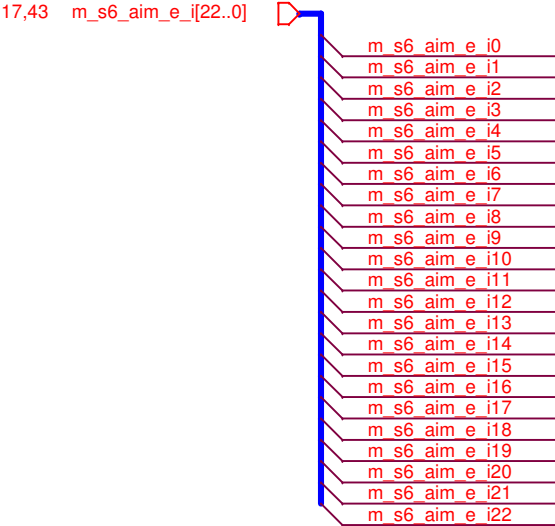
- 1) Differential pairs should be matched to within +/- 5ps (25mil).
- 2) The M\_S6\_AIM\_E\_O bus should be matched to within +/- 50ps (250mil).
- 3) The M\_S6\_AIM\_E\_I bus should be matched to within +/- 50ps (250mil).
- 4) The AUDIO\_R\_CH0-3 bus should be matched to within +/- 500ps (2500mil).

The following buses are embedded in the schematic:

- SPI  
->contains all the spi\_sdo, spi\_sdi, spi\_sck, and spi\_cs0\_n signals
- M\_S6\_AIM\_E\_O  
->contains the aim\_e\_o, aim\_e\_tx\_clk and aim\_e\_tx\_clk\_n signals
- M\_S6\_AIM\_E\_I  
->contains the aim\_e\_i, aim\_e\_rx\_clk and aim\_e\_rx\_clk\_n signals
- AUDIO\_R\_CH0-3  
->contains aclk\_r\_ch0-3, asynr\_ch0-3, and adatr\_ch0-3

The following differential pairs are embedded in the schematic:

- M\_S6\_AIM\_E\_RX\_CLK  
M\_S6\_AIM\_E\_TX\_CLK



U27D

SUPPLY (FOR NON VDD\_E PINS)

VDD\_IO = 1.8V  
VDD\_MAC = 2.5V  
VDD\_MAC = 2.5V

AIM EAST = 1.8V

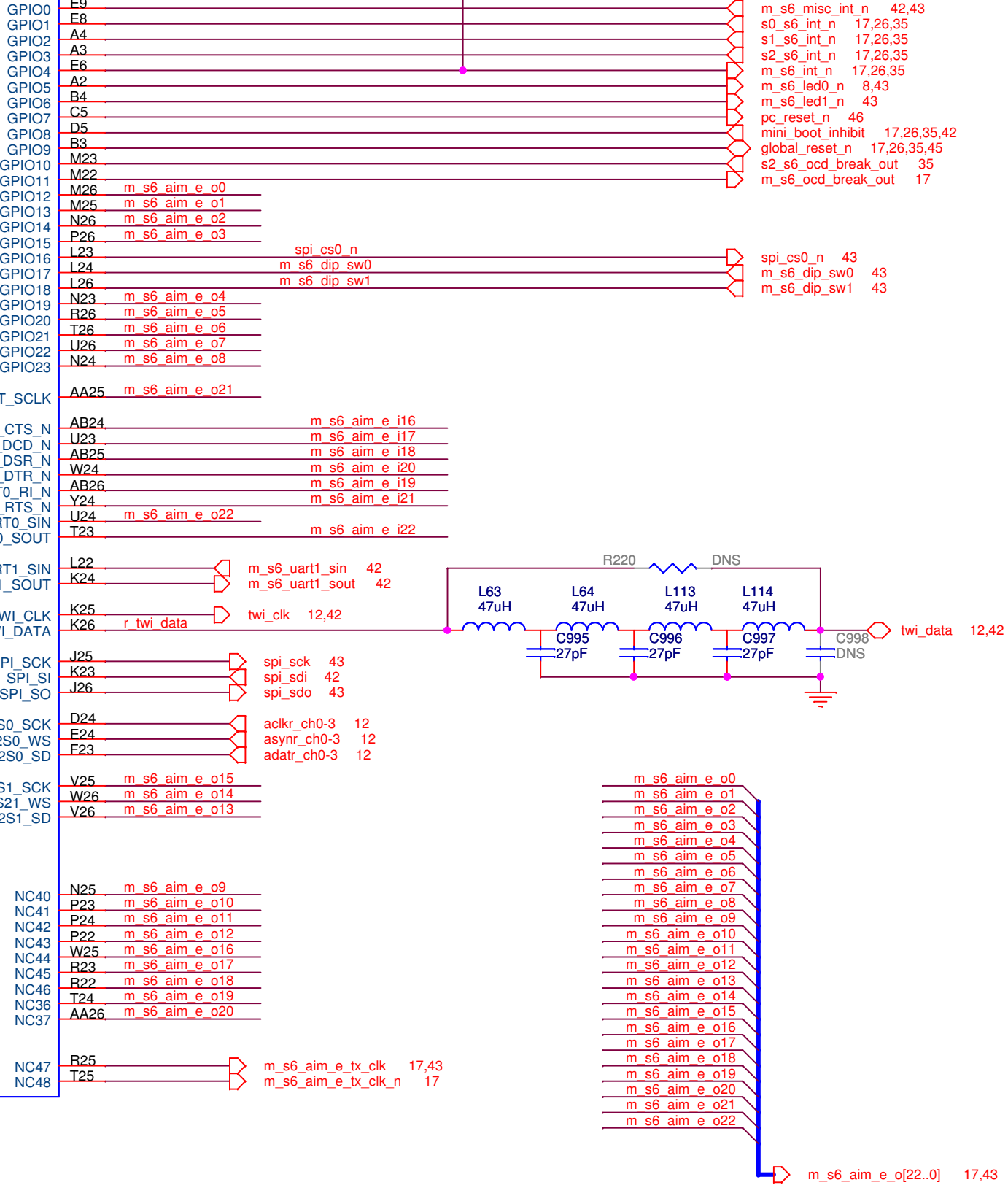
AIM EAST = 1.8V

VDD\_MAC = 2.5V

AIM EAST = 1.8V

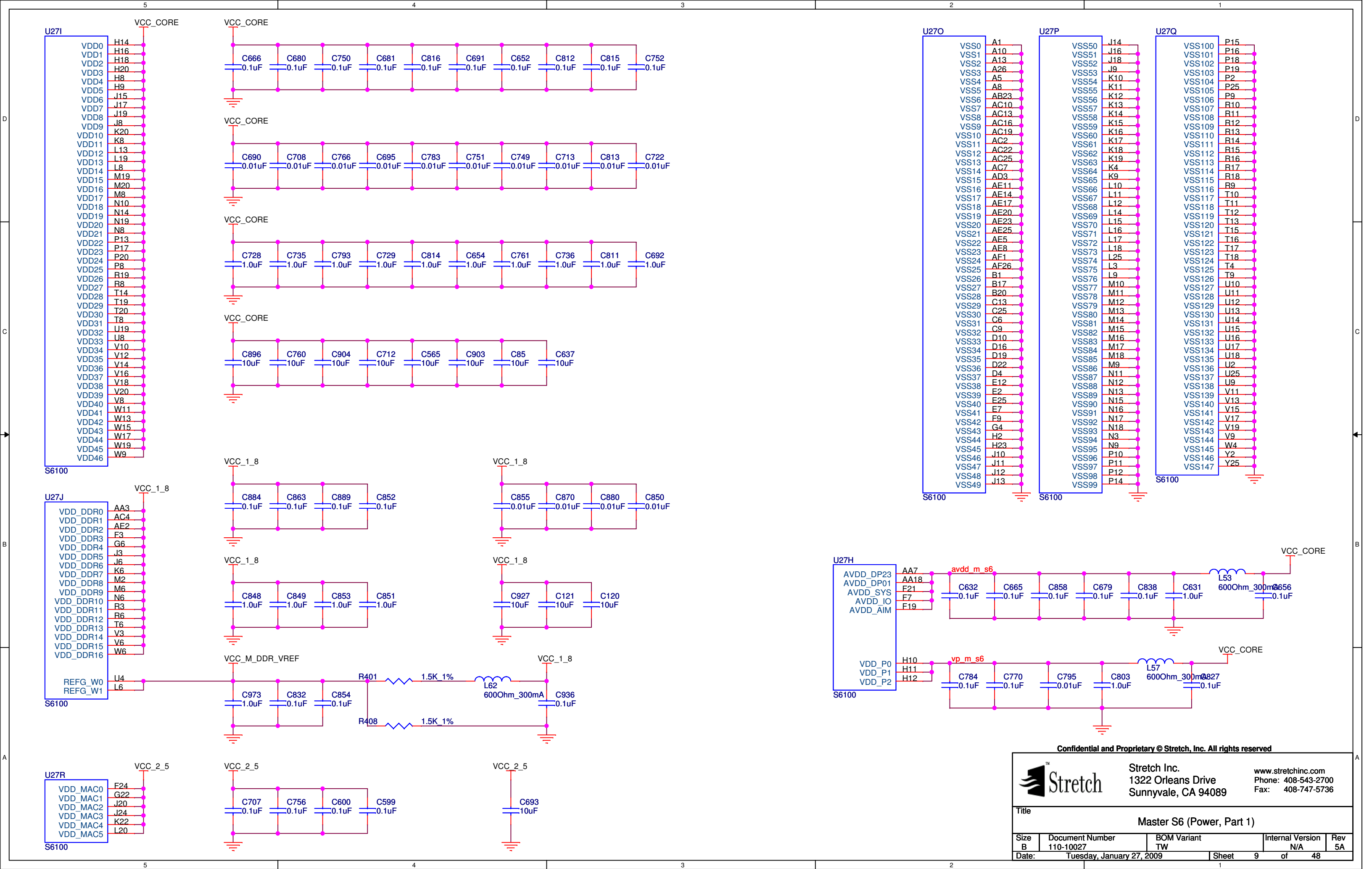
VDD\_E

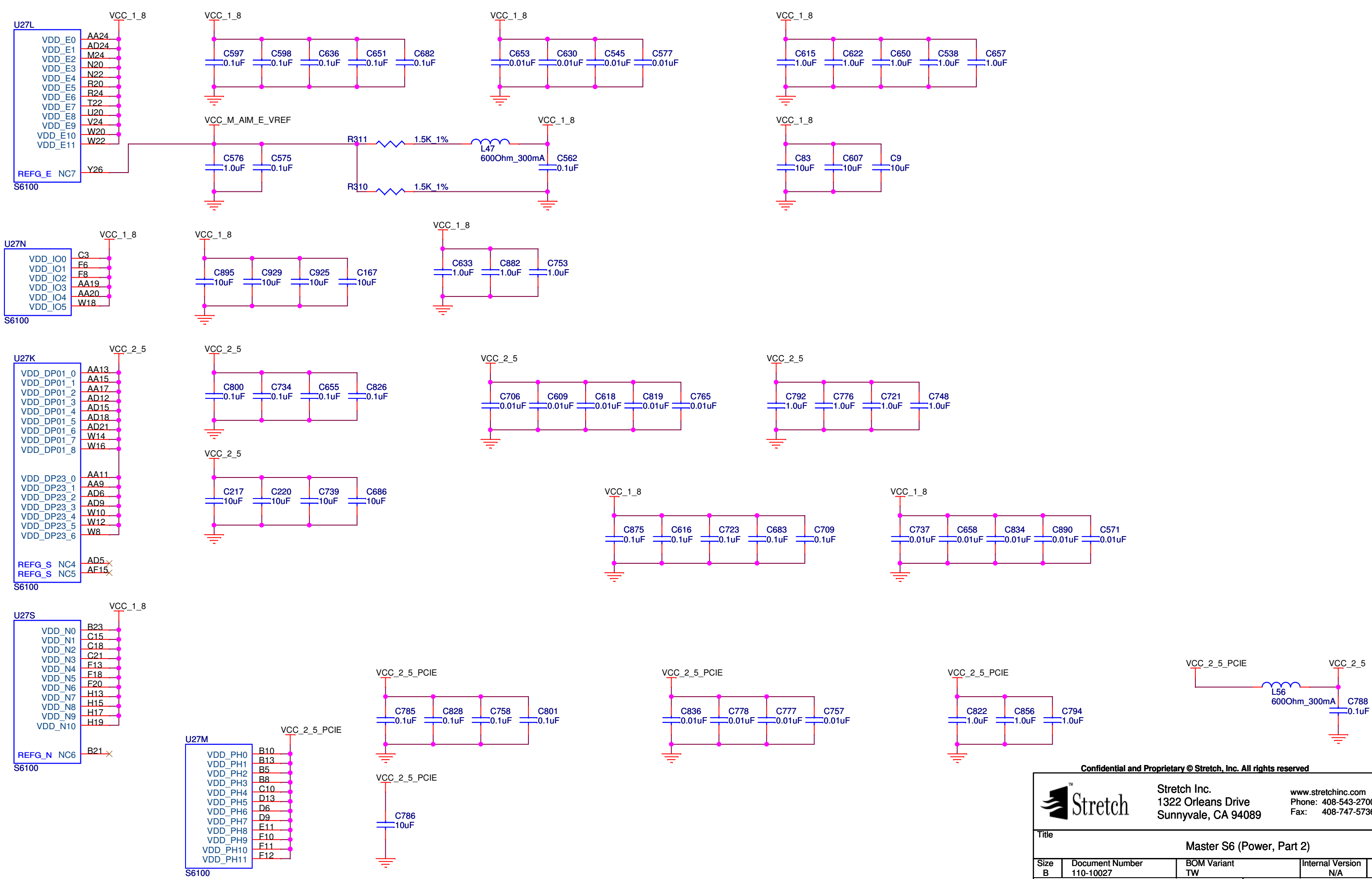
S6100

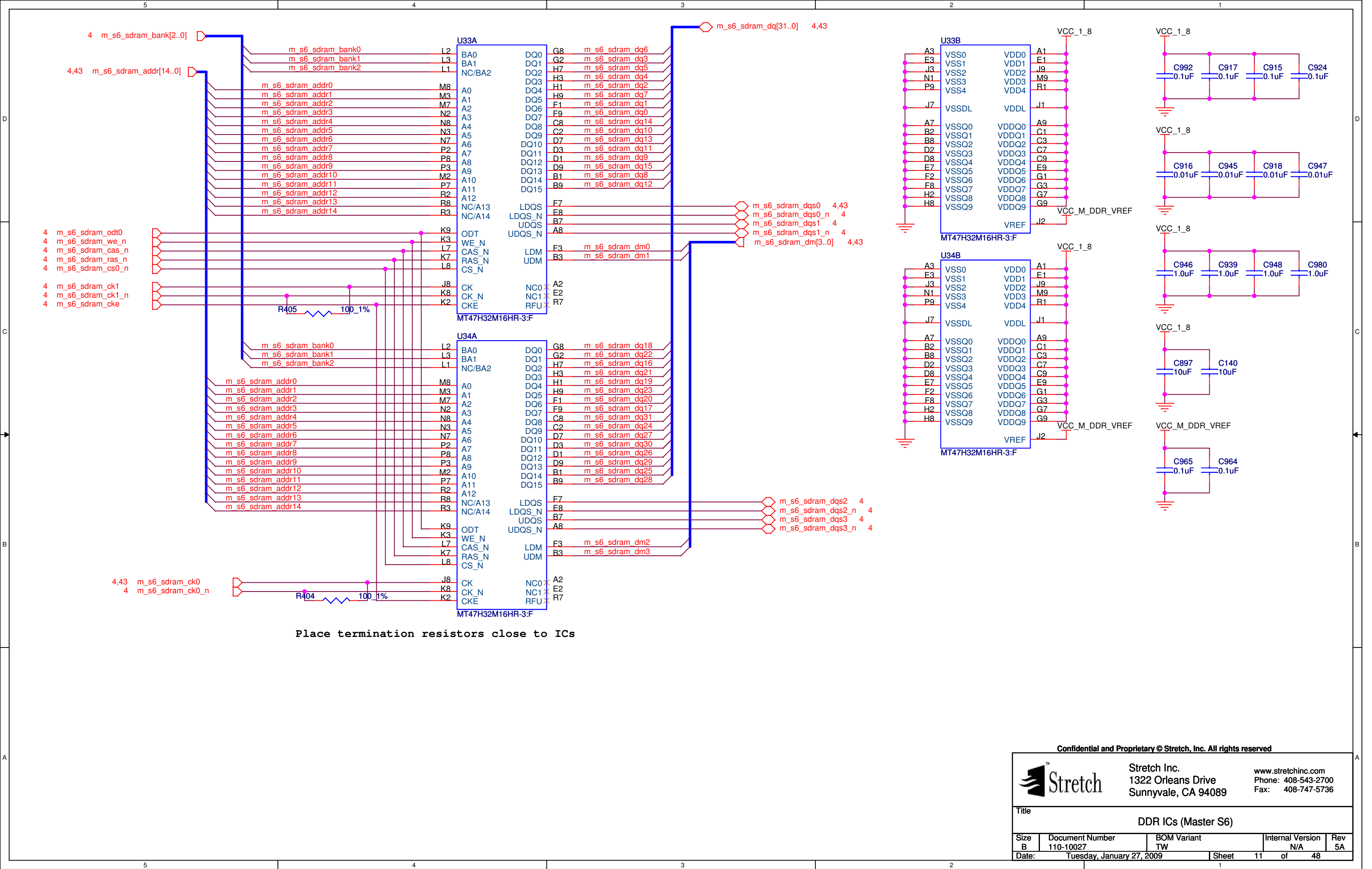


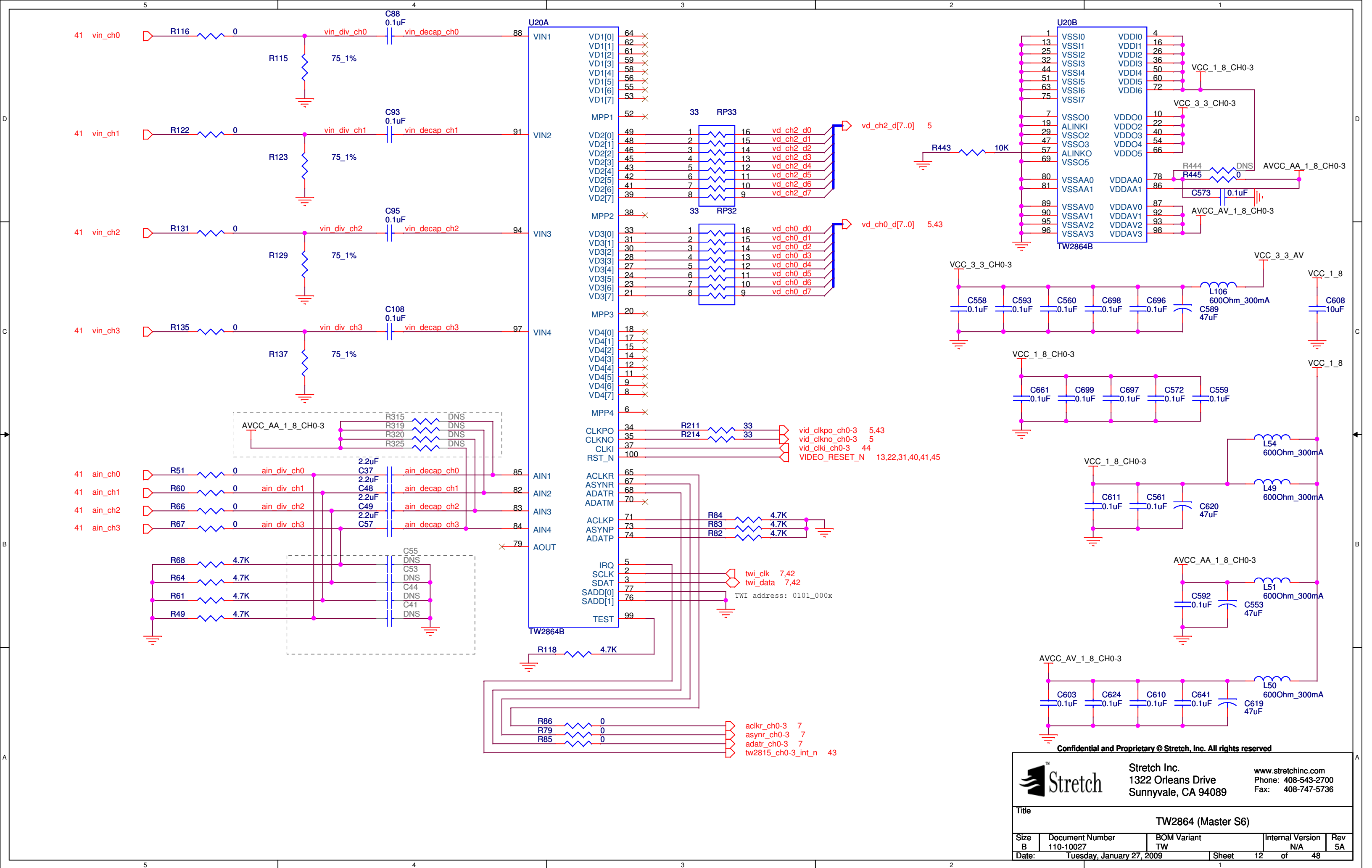




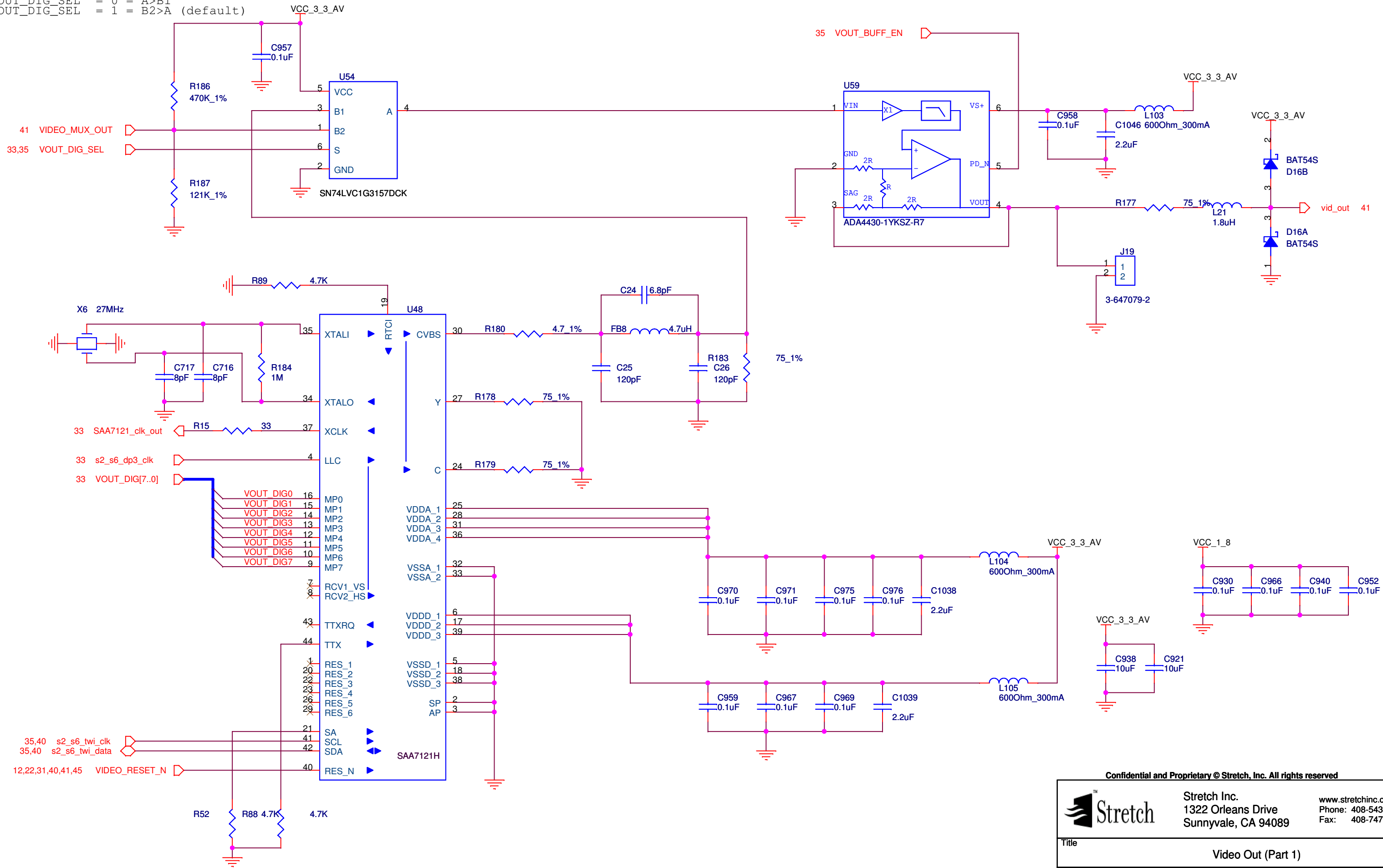




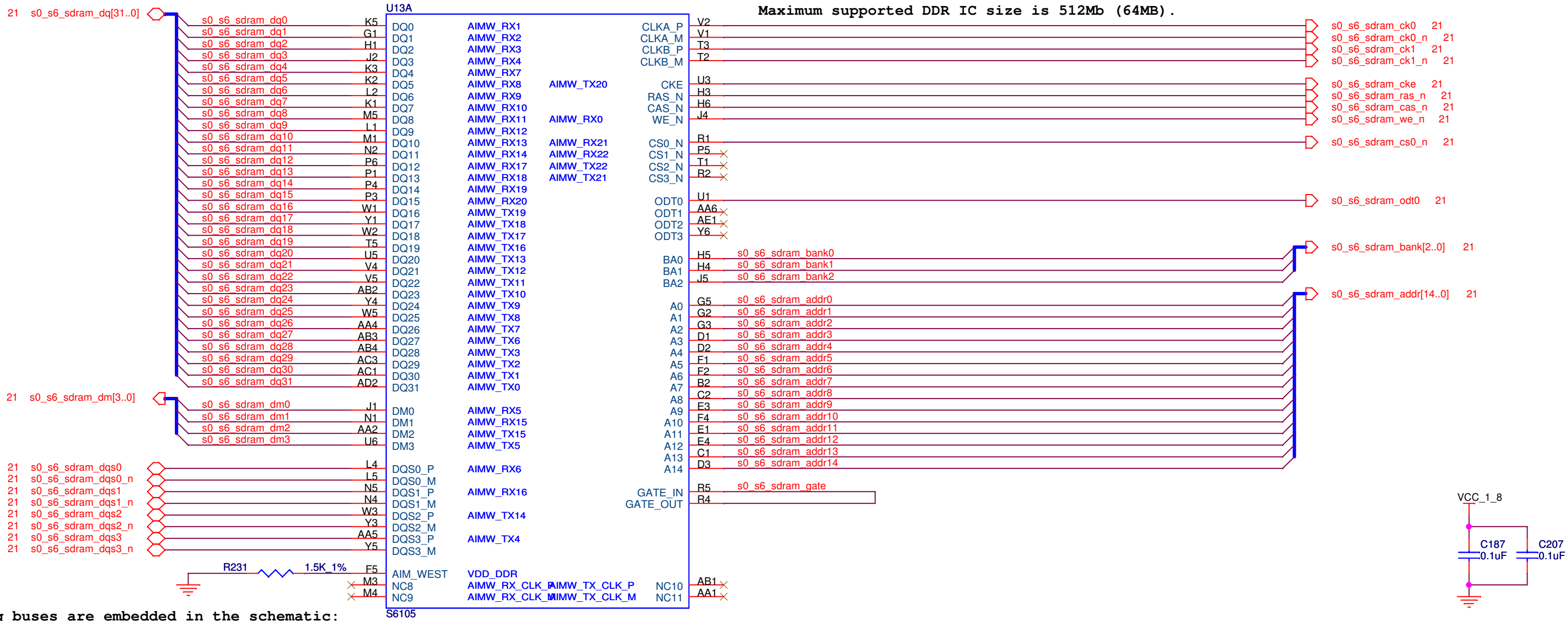




VOUT\_DIG\_SEL = 0 = A>B1  
VOUT\_DIG\_SEL = 1 = B2>A (default)







The following buses are embedded in the schematic:

S0\_S6\_DDR\_DATA

->contains all the sdram\_dq, sdram\_dm, sdram\_dqs, and sdram\_dqs\_n signals

S0\_S6\_DDR\_CLK

->contains the sdram\_ck and sdram\_gate signals

S0\_S6\_DDR\_ADDR

->contains the sdram\_cke, sdram\_ras\_n, sdram\_cas\_n, sdram\_we\_n, sdram\_cs0\_n, sdram\_bank, and sdram\_addr signals

The following differential pairs are embedded in the schematic:

S0\_S6\_DDR\_DQS0

S0\_S6\_DDR\_DQS1

S0\_S6\_DDR\_DQS2

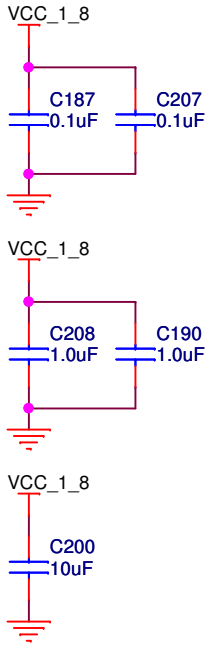
S0\_S6\_DDR\_DQS3

S0\_S6\_DDR\_CK0

S0\_S6\_DDR\_CK1

ROUTING RULES (S6100 package legths should be taken into consideration when determining the trace lengths):

- 1) Differential pairs should be matched to within +/- 5ps (25mil) .
- 2) The DDR\_ADDR bus and clocks should be matched to within +/- 75ps (375mil) .
- 3) The DDR\_DATA bus should be matched to within +/- 50ps (250mil) .
- 4) The signals in a byte lane should be matched to within +/- 30ps (150mil) and be routed on the same layer.
- 5) The clocks and dqs signals should be matched to within +/- 100ps (500mil) .
- 6) s0\_s6\_sdram\_gate signal should be as short as possible and accesible using a via.



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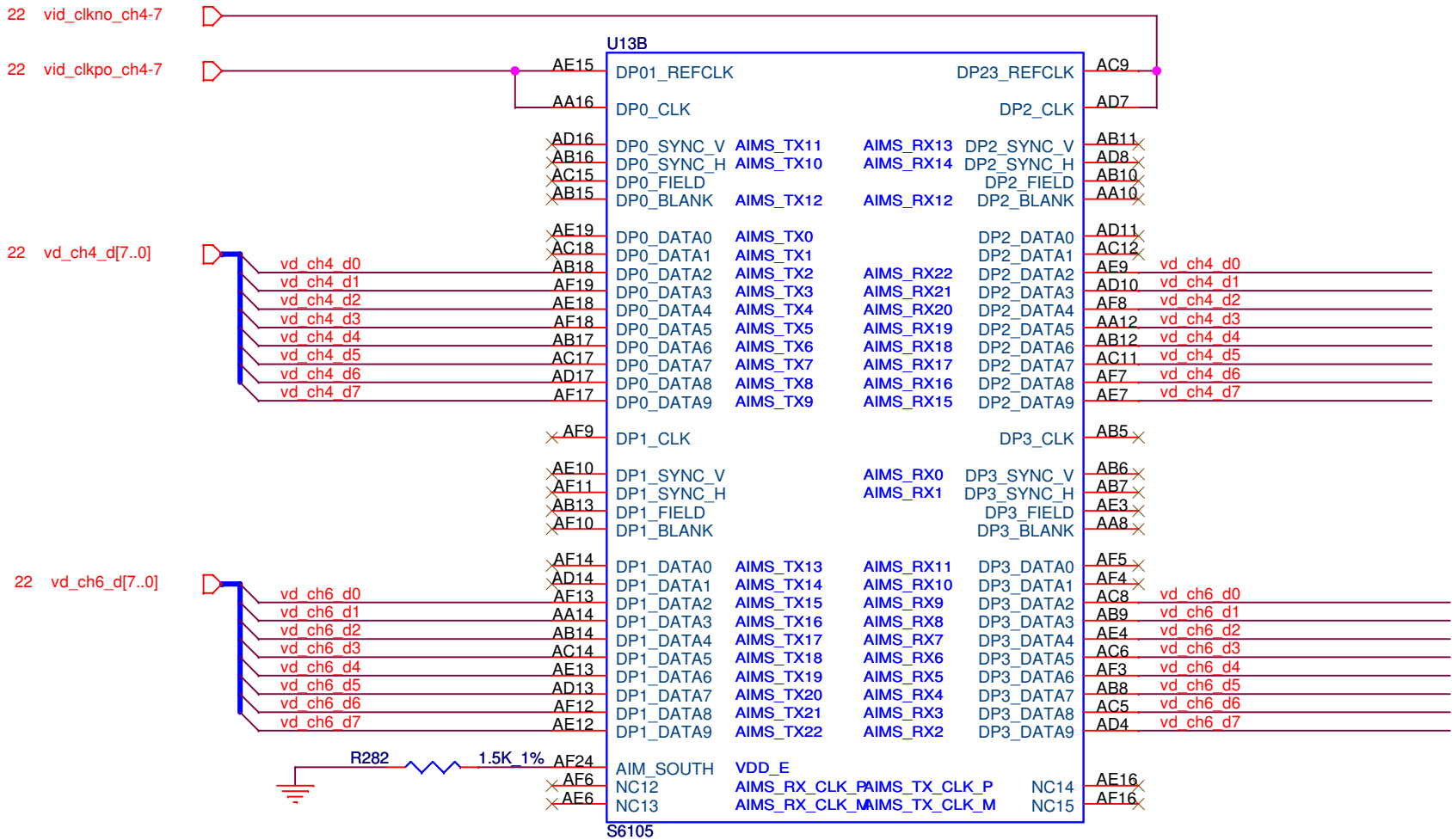


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Title				
Secondary 0 S6 (DDR Interface)				
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dp0\_clk\_ref and dp2\_clk\_ref need to be driven for reset initialization.

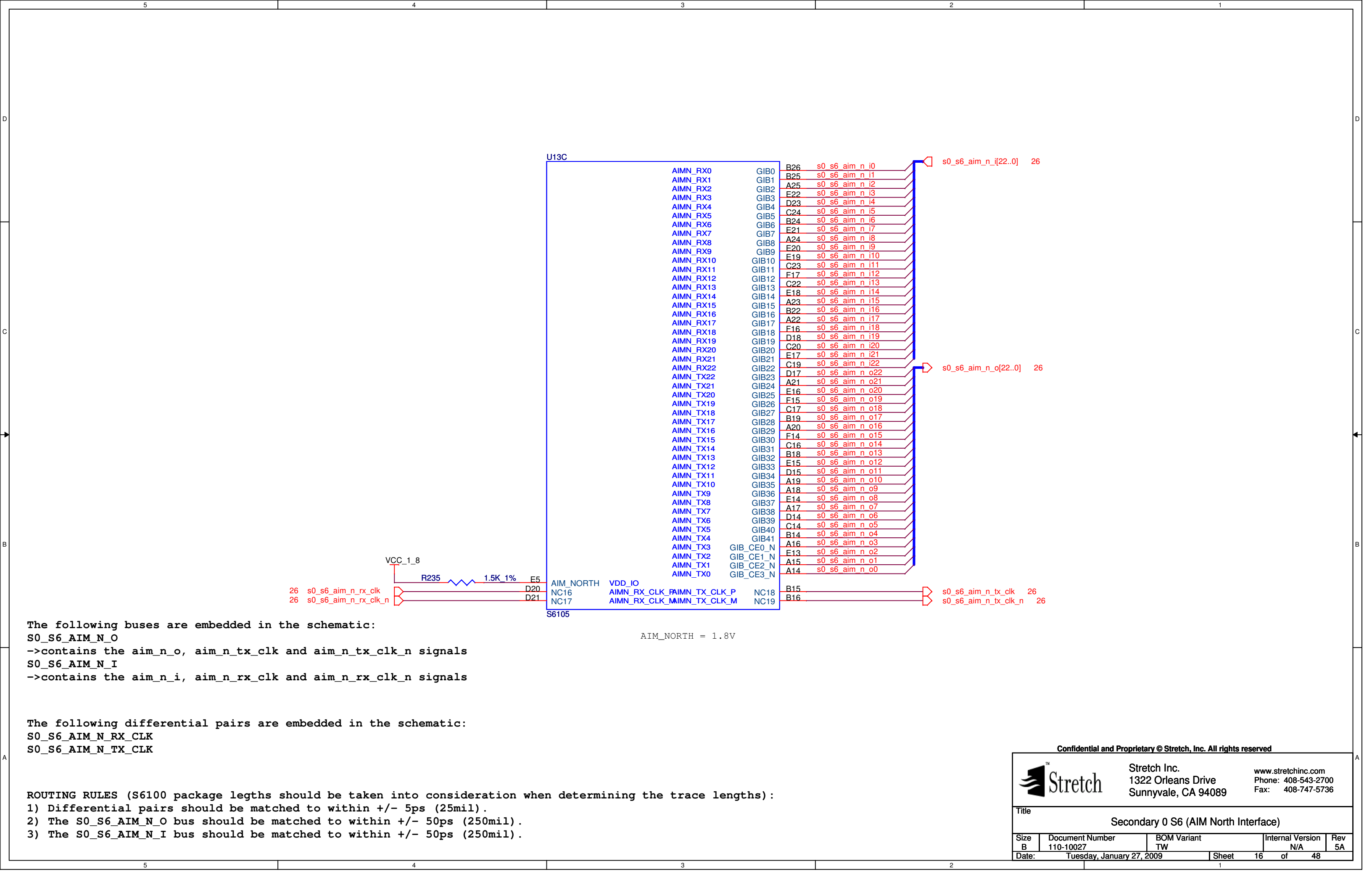


DP 0-3 ARE POWERED FROM 2.5V

The following buses are embedded in the schematic:

- VD\_CH4
- >contains all the vd\_ch4 signals
- VD\_CH6
- >contains all the vd\_ch6 signals

ROUTING RULES (S6100 package legth's should be taken into consideration when determining the trace lengths):  
The VD\_CH4, VD\_CH6 buses, vid\_clkpo\_ch4-7, and vid\_clkno\_ch4-7 should be matched to within +/- 250ps (1250mil).

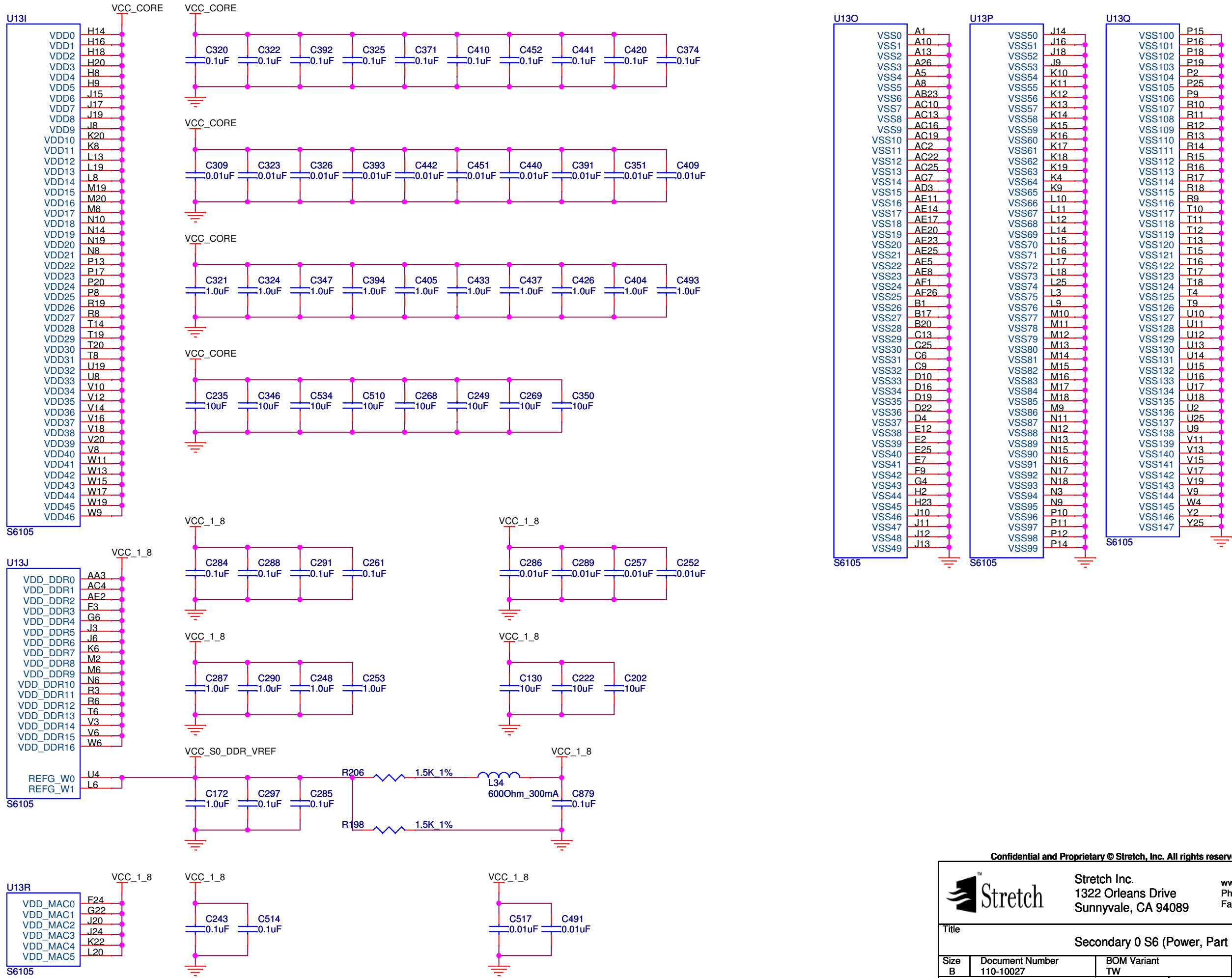


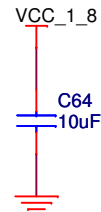
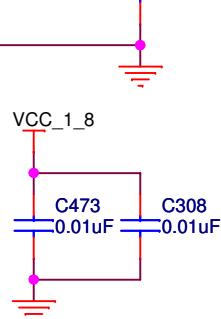
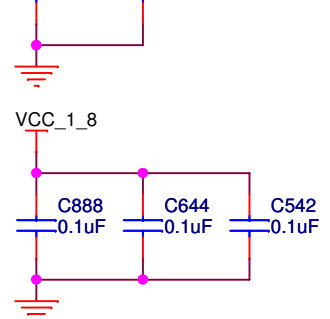
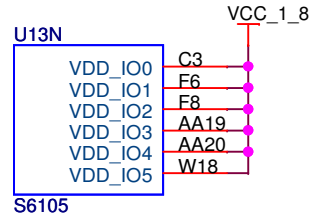
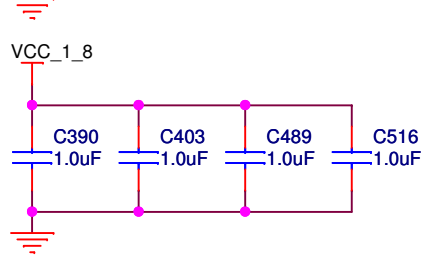
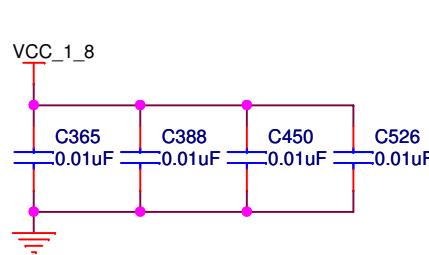
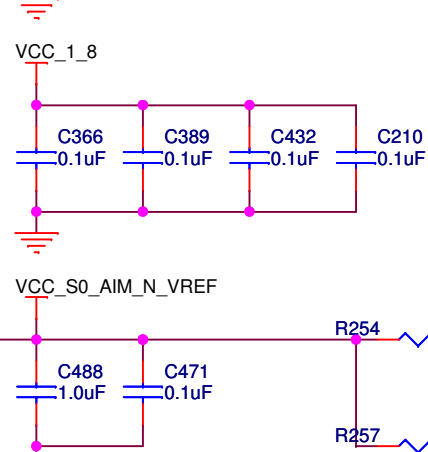
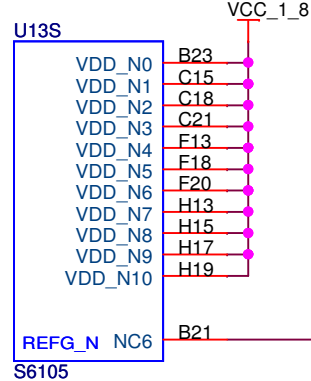
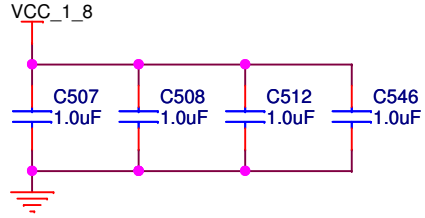
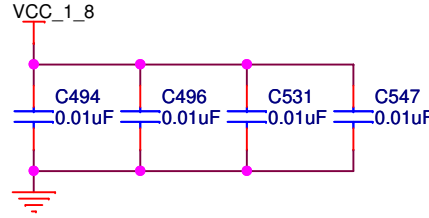
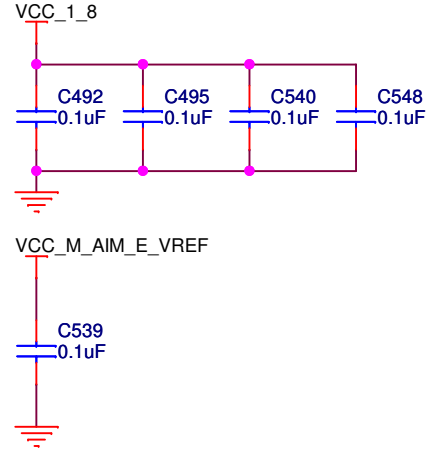
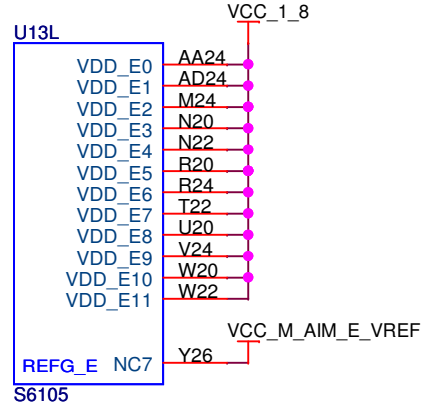
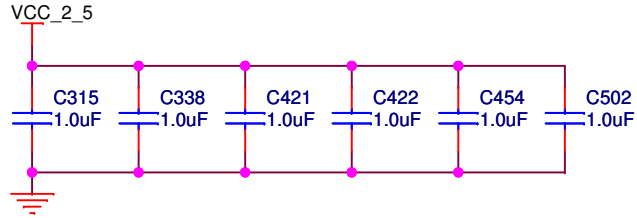
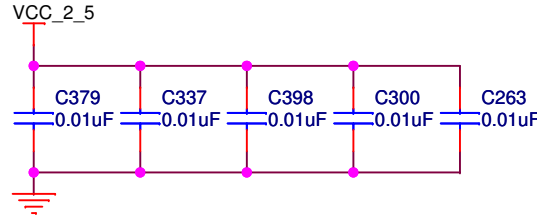
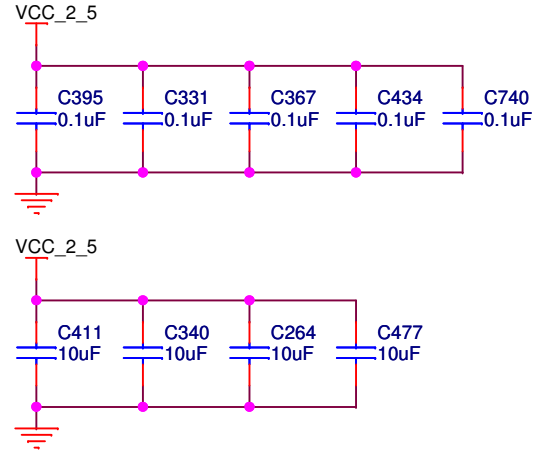
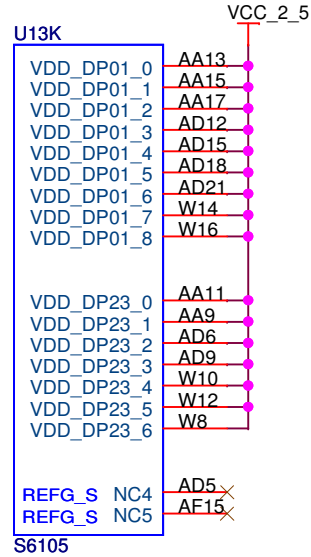
The following buses are embedded in the schematic:  
AUDIO\_R\_CH4-7  
->contains aclk\_r\_ch4-7, asynr\_ch4-7, and adatr\_ch4-7












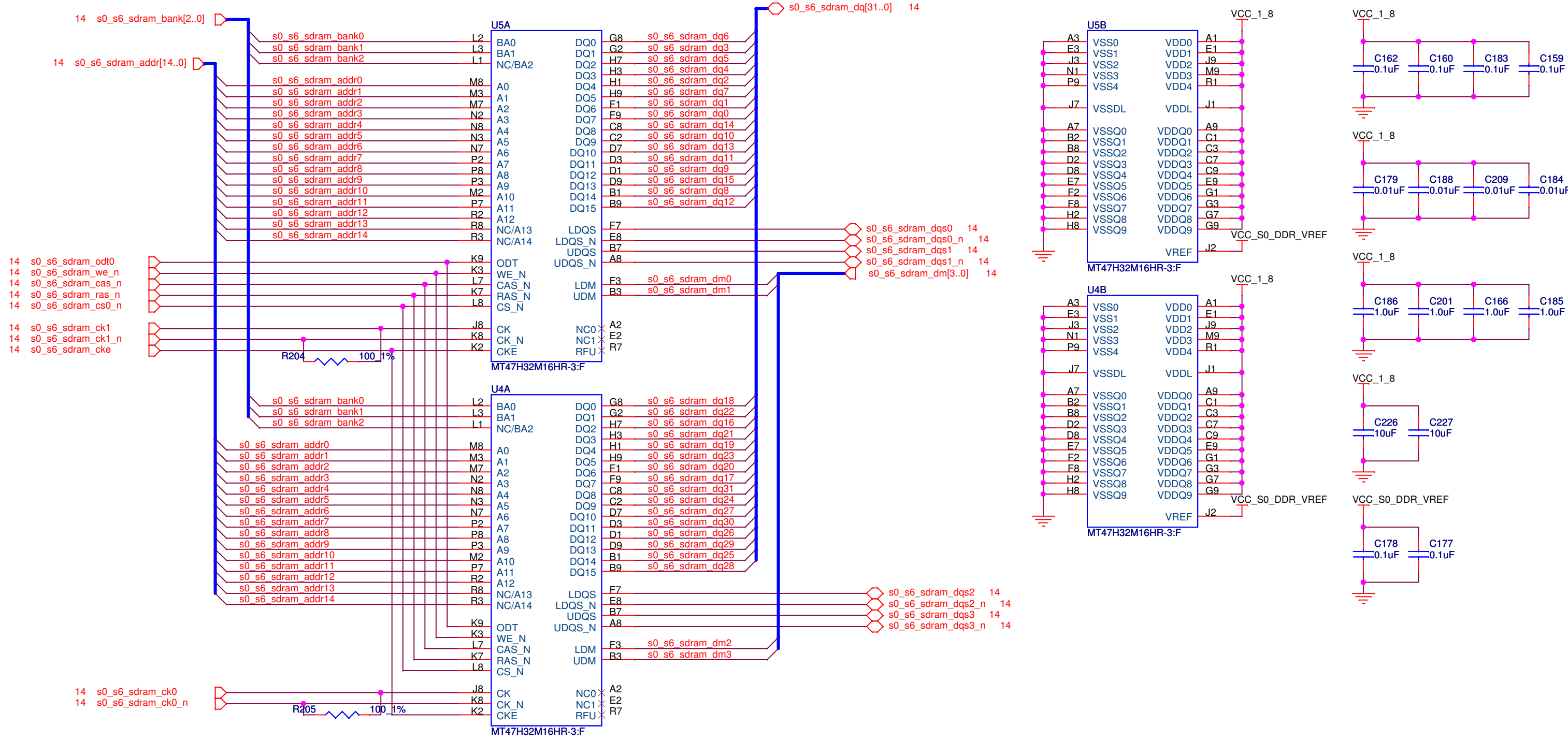
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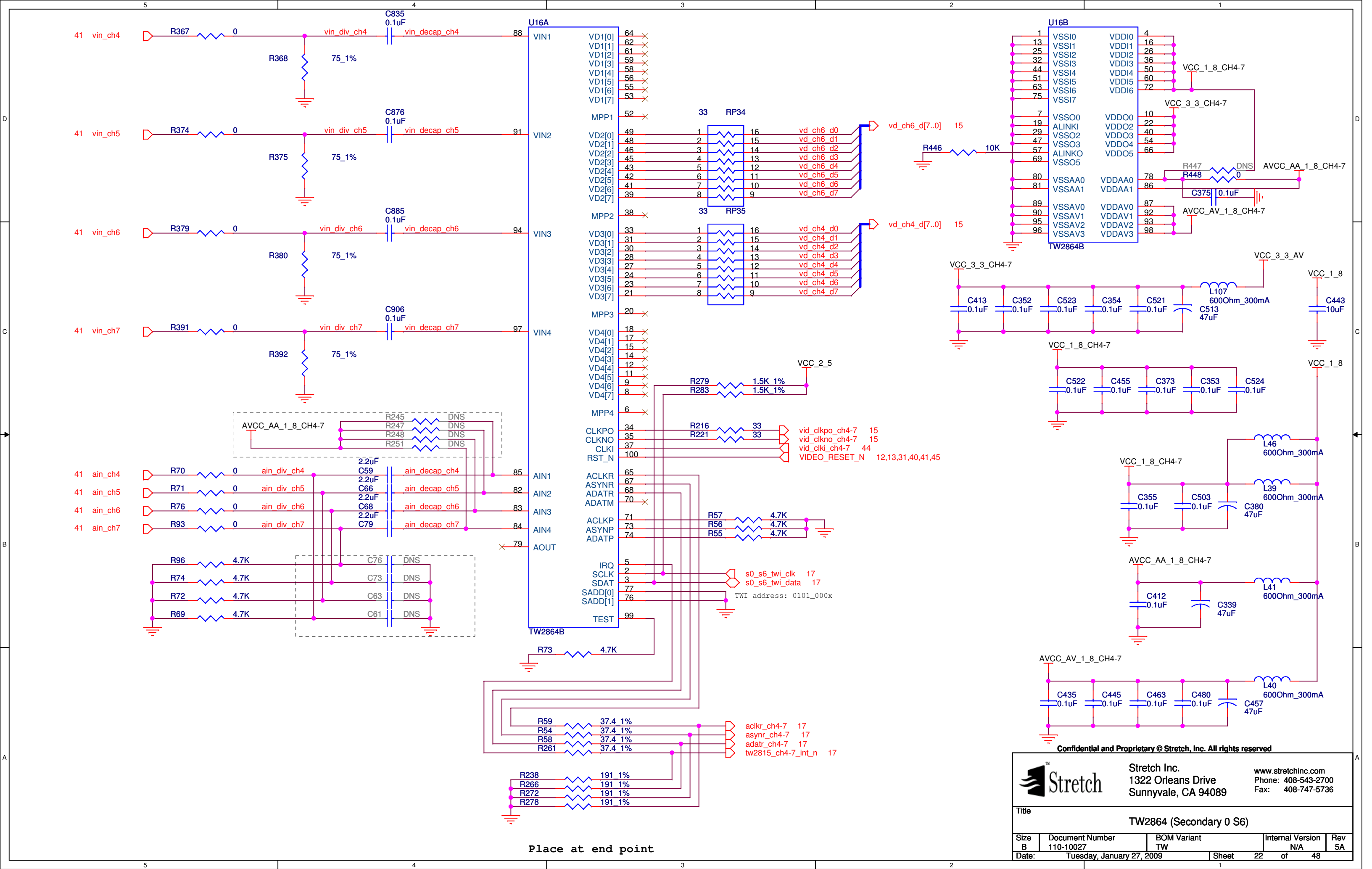
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Title  
Secondary 0 S6 (Power, Part 2)

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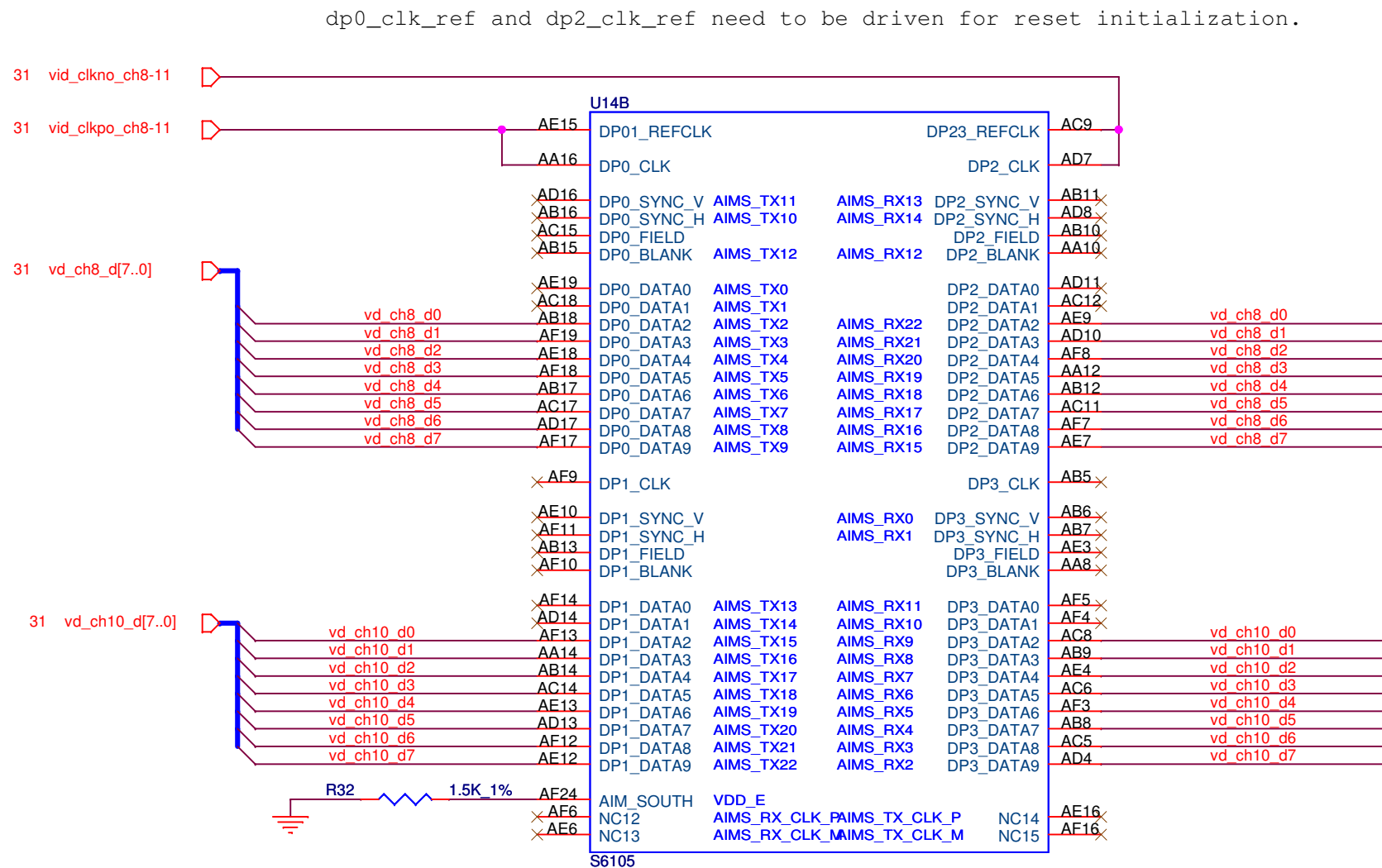


Place termination resistors close to ICs









DP0-3 ARE POWERED FROM 2.5V

The following buses are embedded in the schematic:

VD\_CH8

->contains all the vd\_ch8 signals

VD\_CH10

->contains all the vd\_ch10 signals

ROUTING RULES (S6100 package legth's should be taken into consideration when determining the trace lengths):

The VD\_CH8, VD\_CH10 buses, vid\_clkpo\_ch8-11, and vid\_clkno\_ch8-11 should be matched to within +/- 250ps (1250mil).

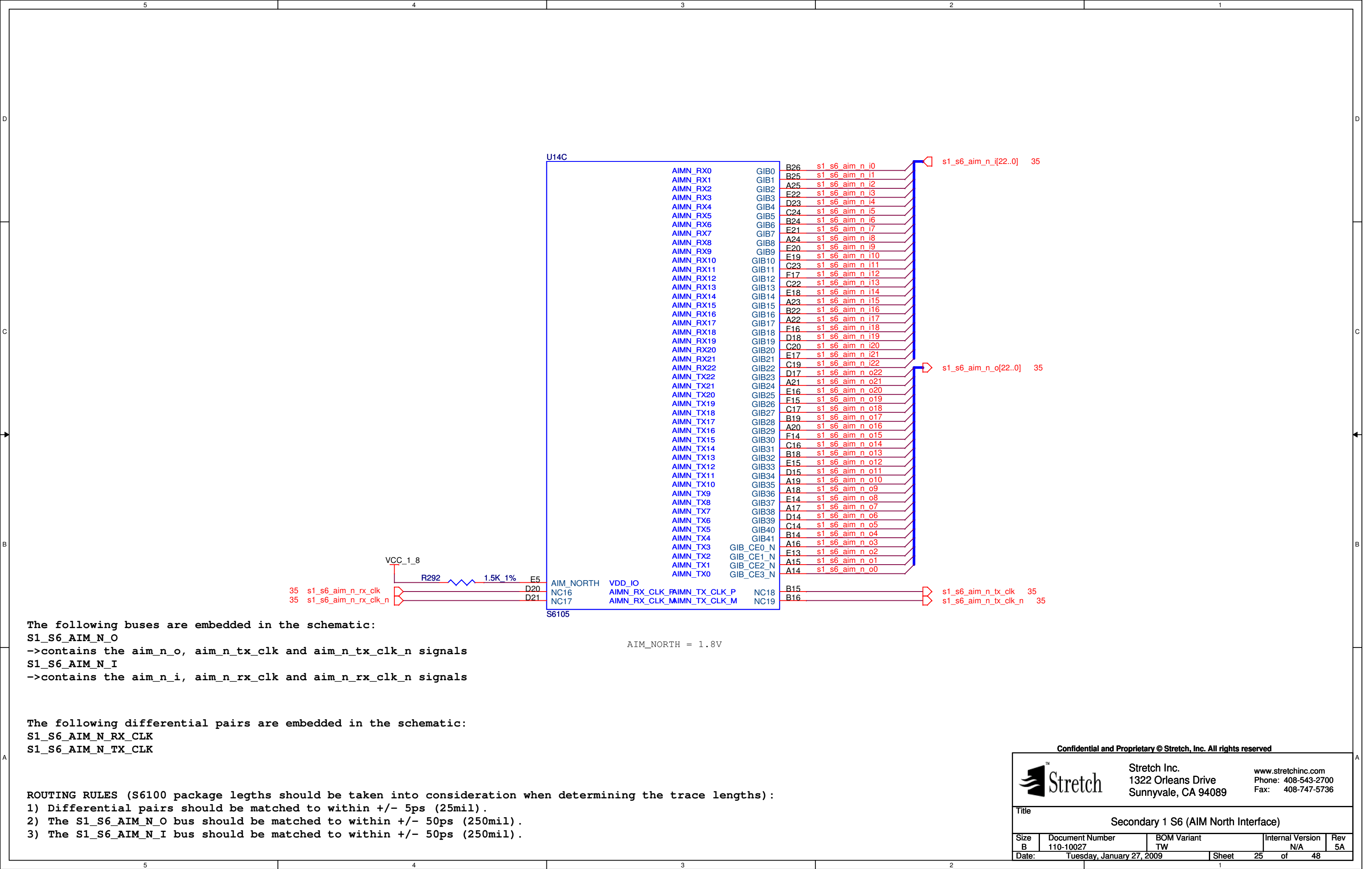
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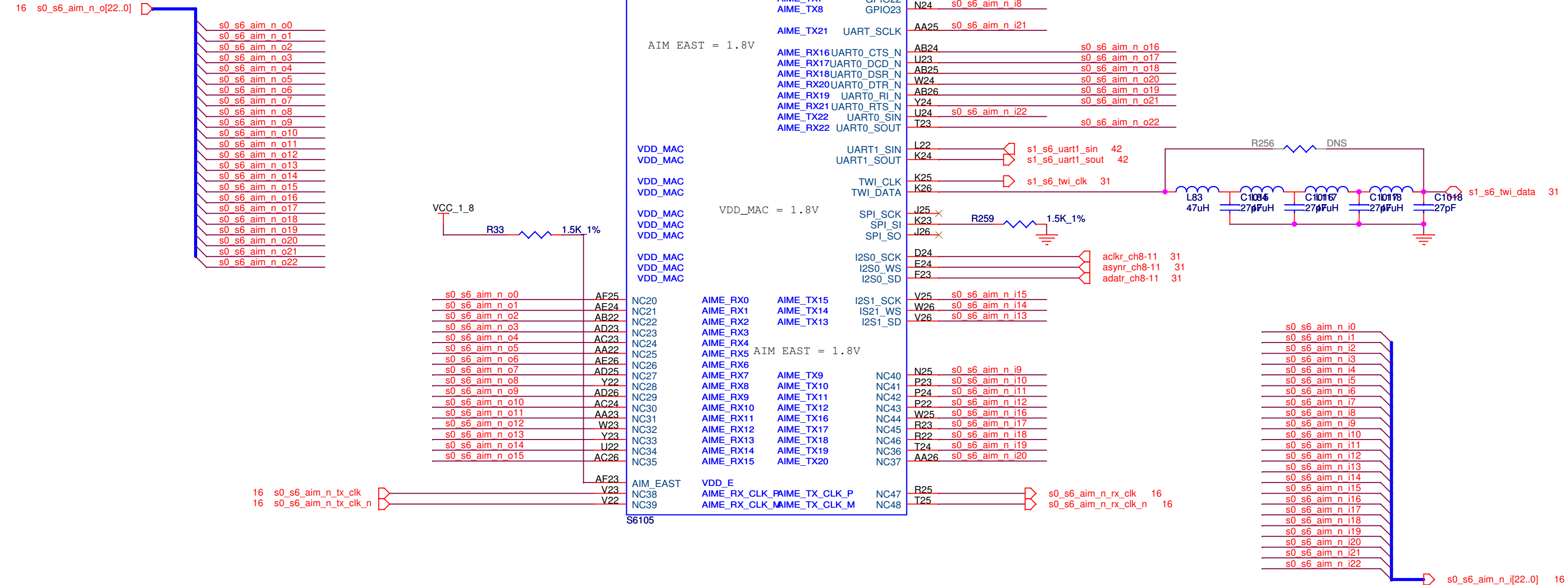
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Secondary 1 S6 (Data Port Interface)				
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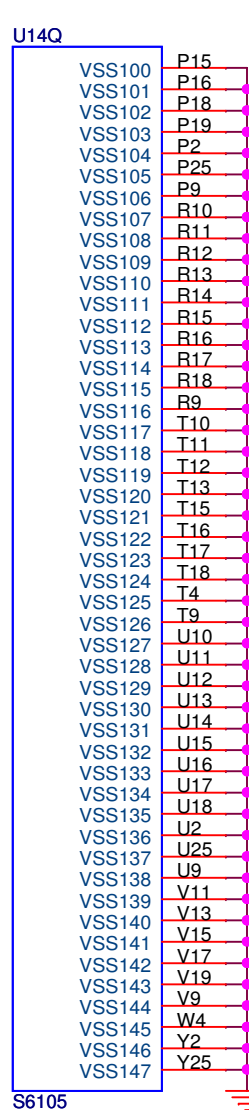
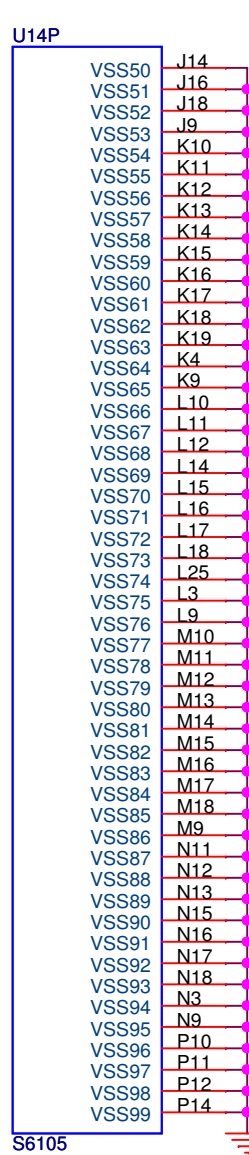
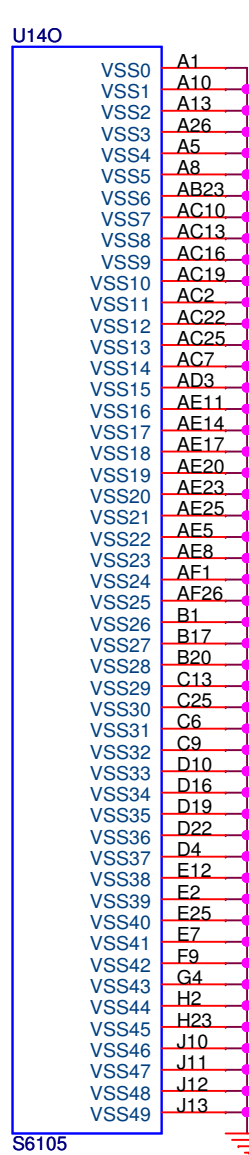
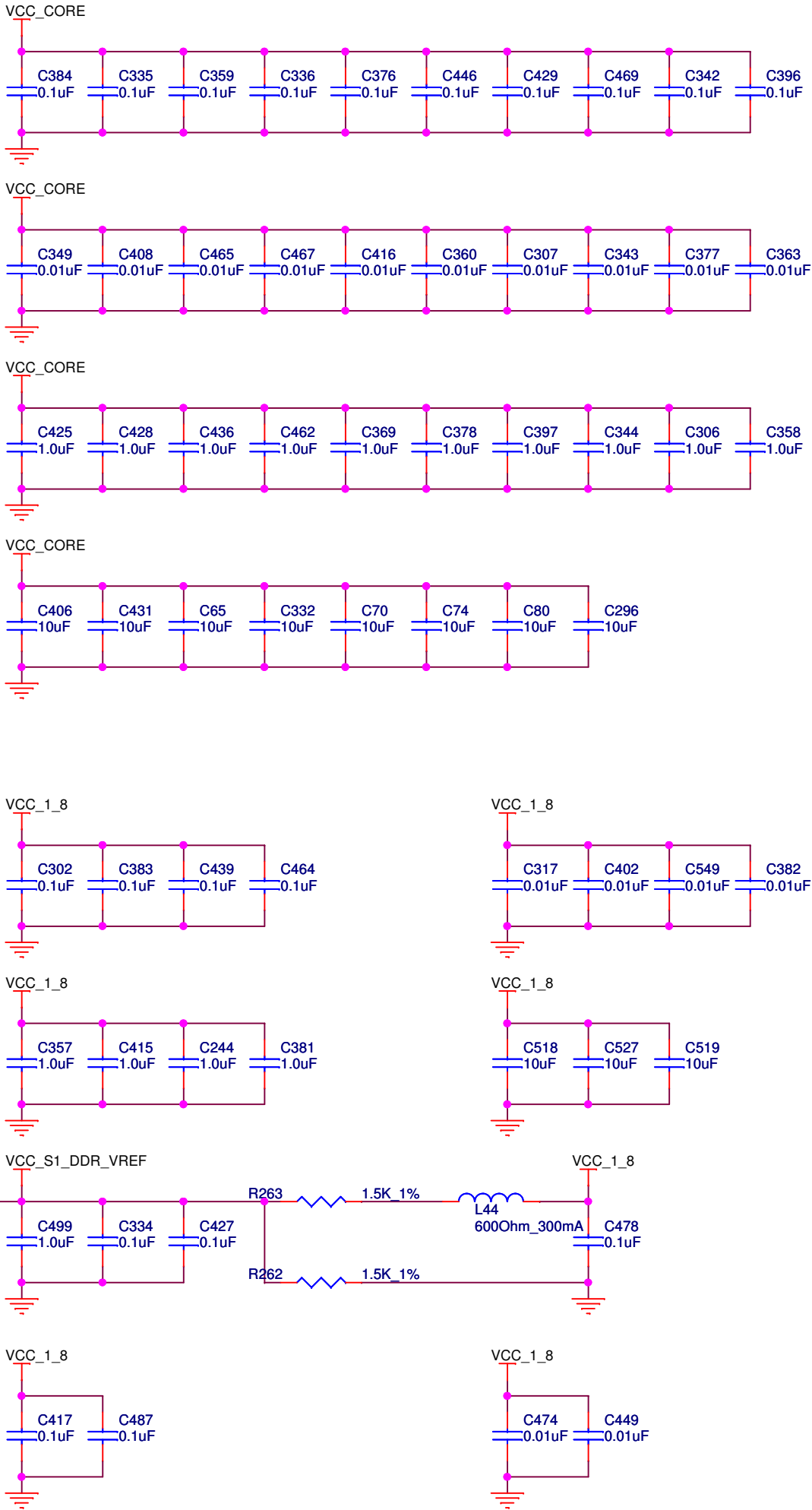
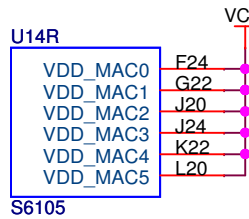
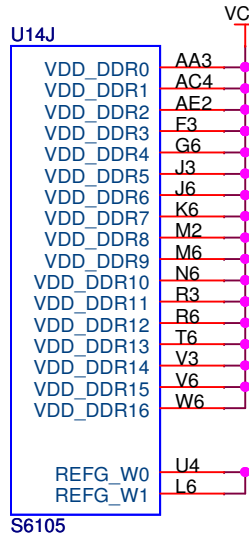
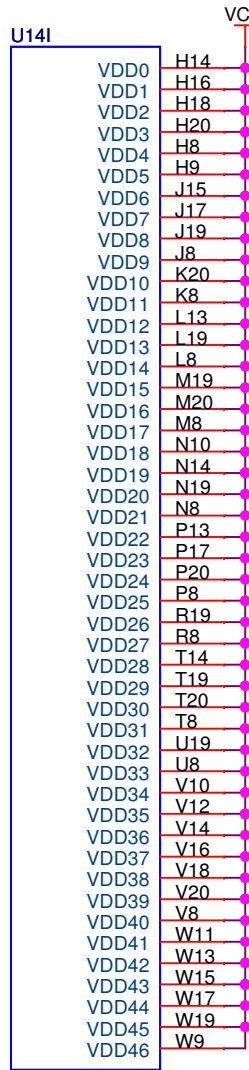


The following buses are embedded in the schematic:  
AUDIO\_R\_CH8-11  
->contains aclkr\_ch8-11, asynr\_ch8-11, and adatr\_ch8-11

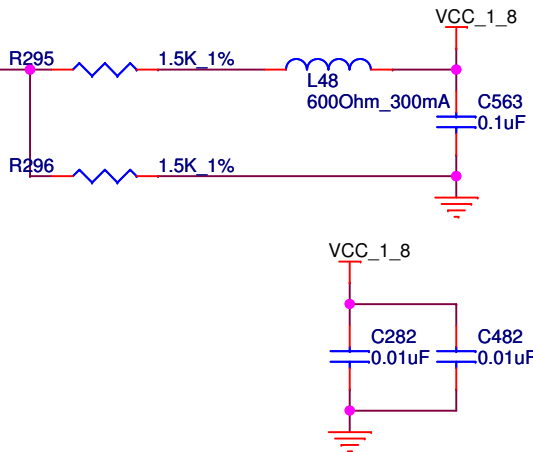
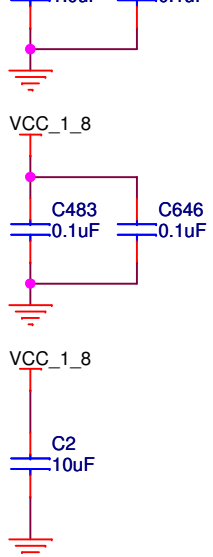
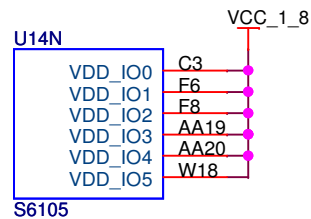
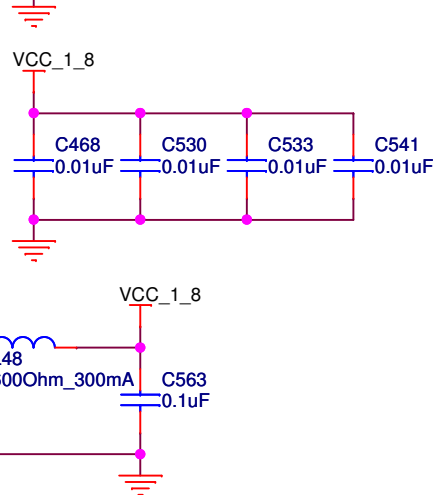
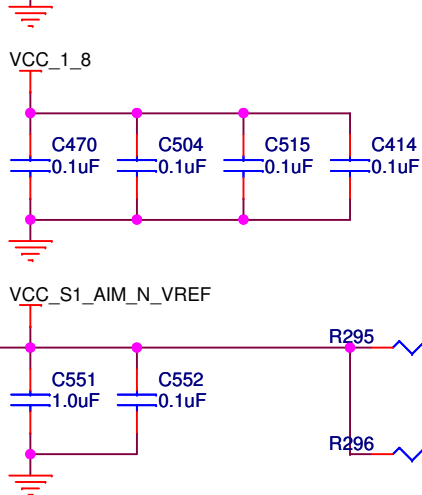
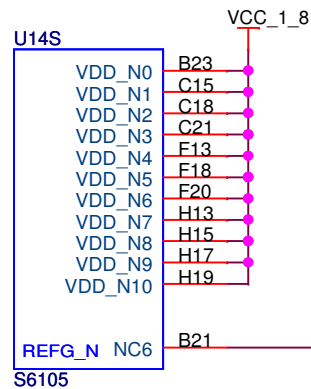
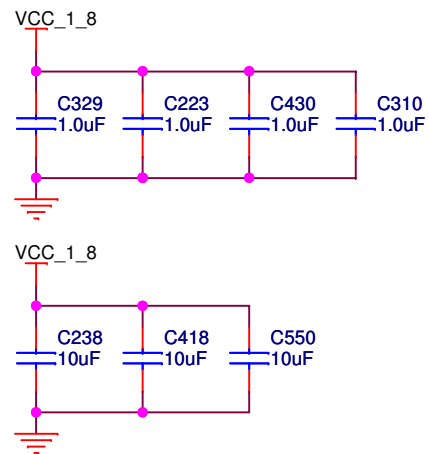
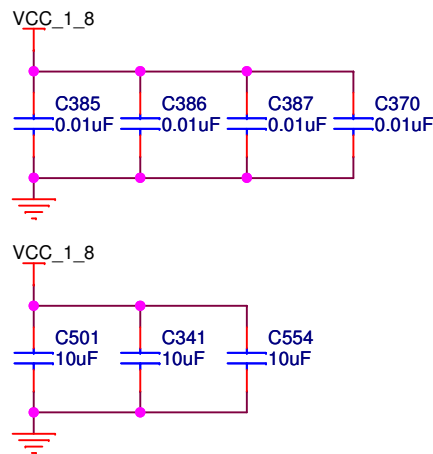
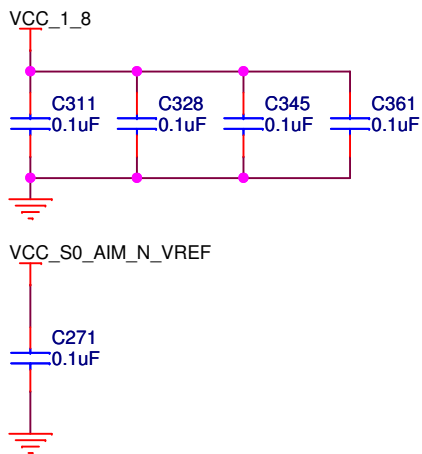
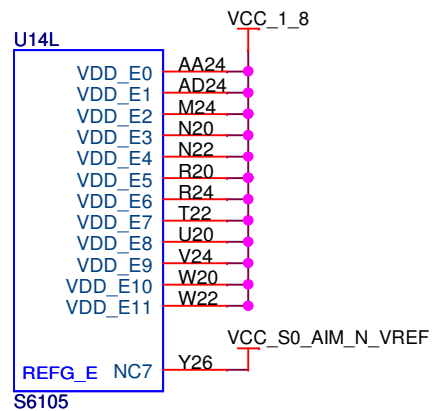
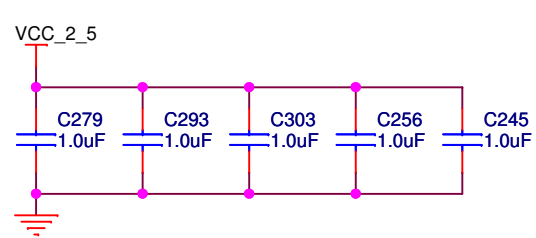
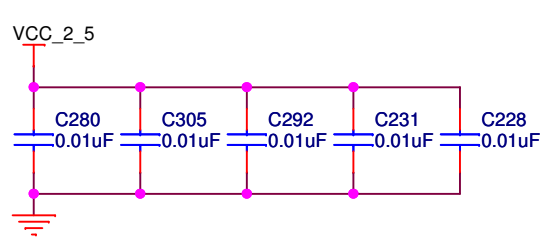
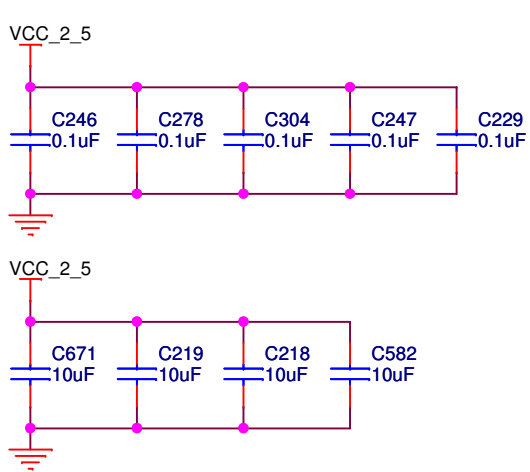
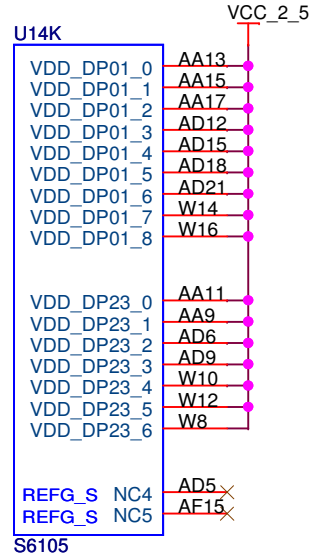
ROUTING RULES (S6100 package legth's should be taken into consideration when determining the trace lengths):  
The AUDIO\_R\_CH8-11 bus should be matched to within +/- 500ps (2500mil).






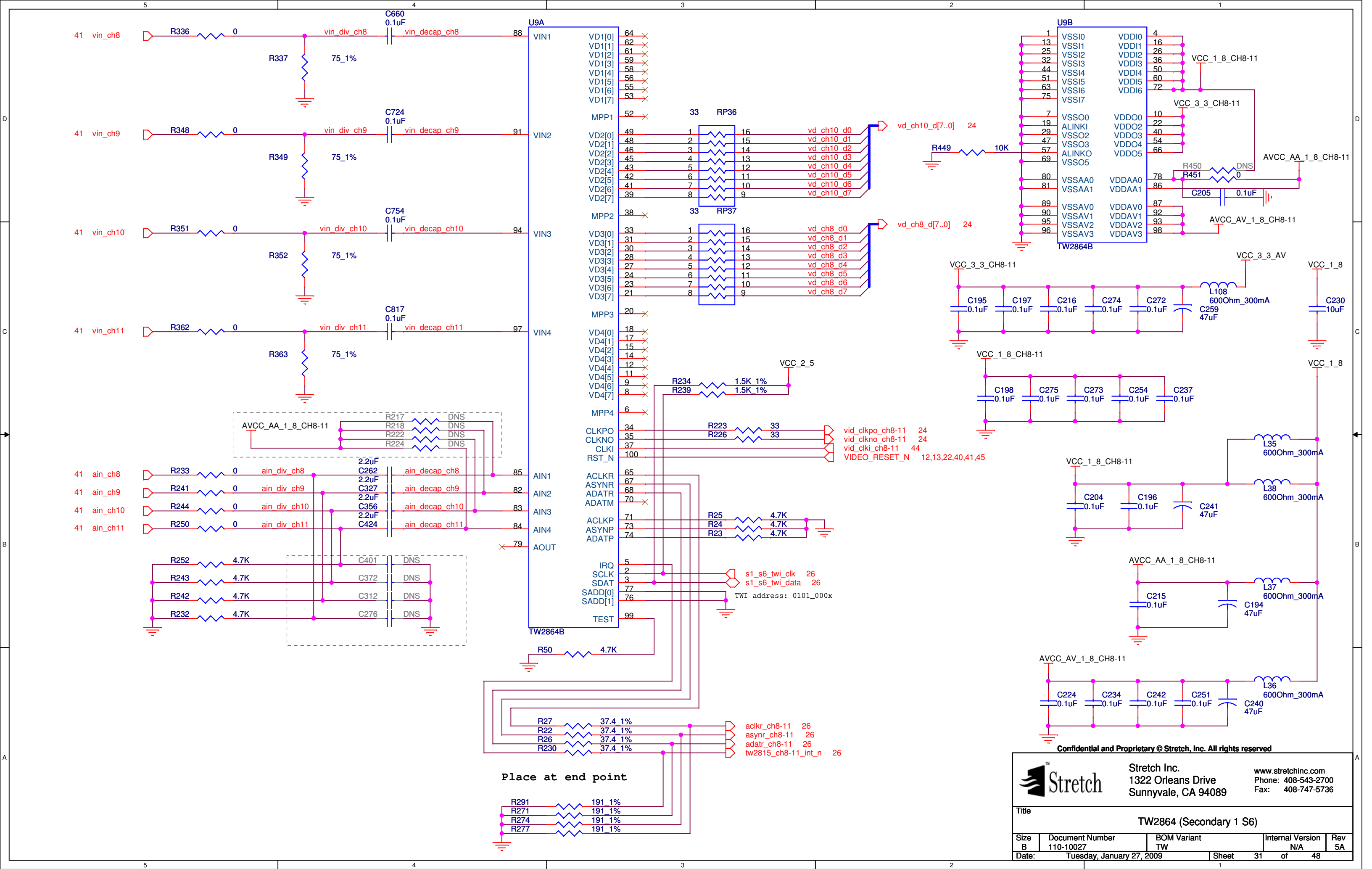






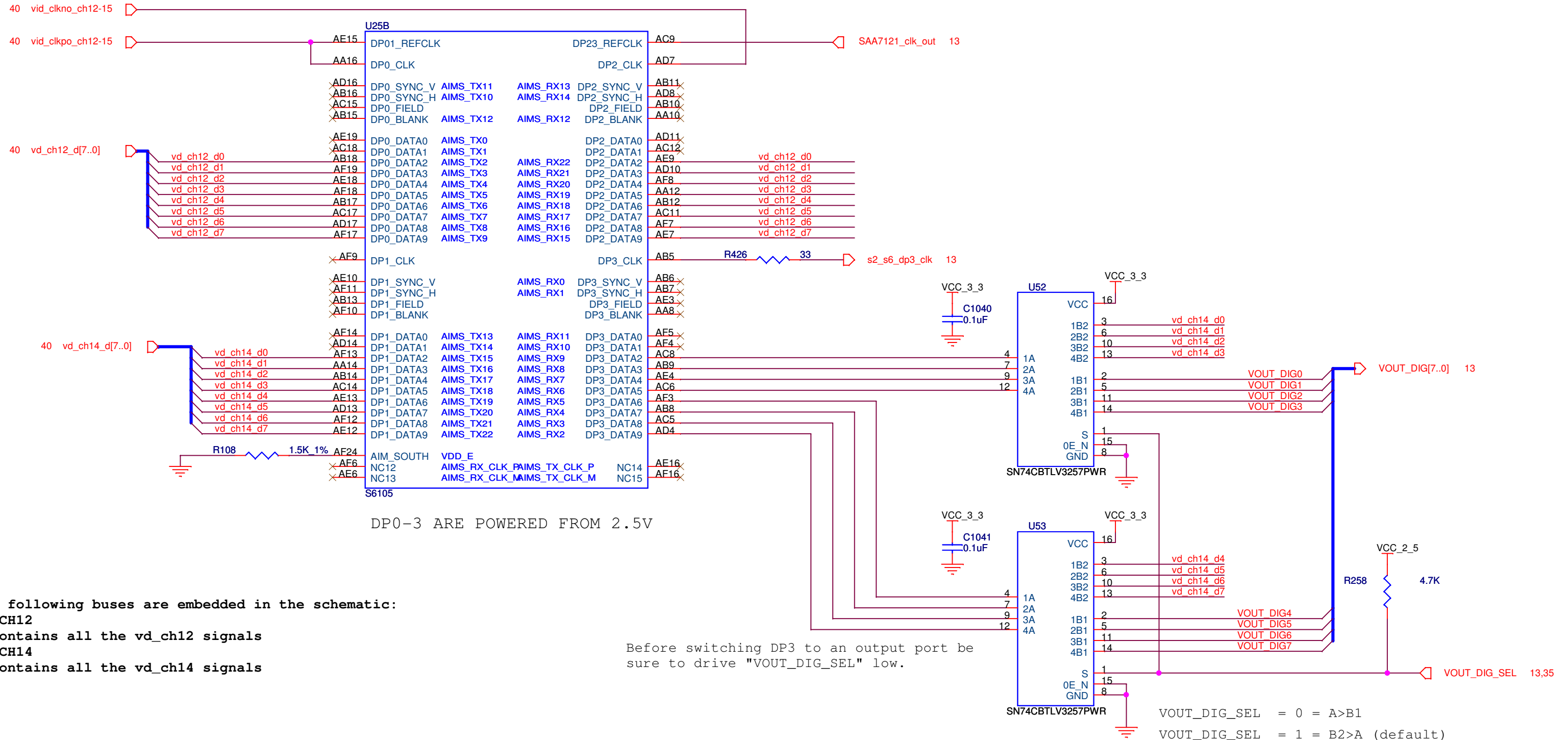
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Title Secondary 1 S6 (Power, Part 2)				
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dp0\_clk\_ref and dp2\_clk\_ref need to be driven for reset initialization.



The following buses are embedded in the schematic:

VD\_CH12

->contains all the vd\_ch12 signals

VD\_CH14

->contains all the vd\_ch14 signals

ROUTING RULES (S6100 package legths should be taken into consideration when determining the trace lengths):

The VD\_CH12, VD\_CH14, buses, vid\_clkpo\_ch12-15, and vid\_clkno\_ch12-15 should be matched to within +/- 250ps (1250mil).

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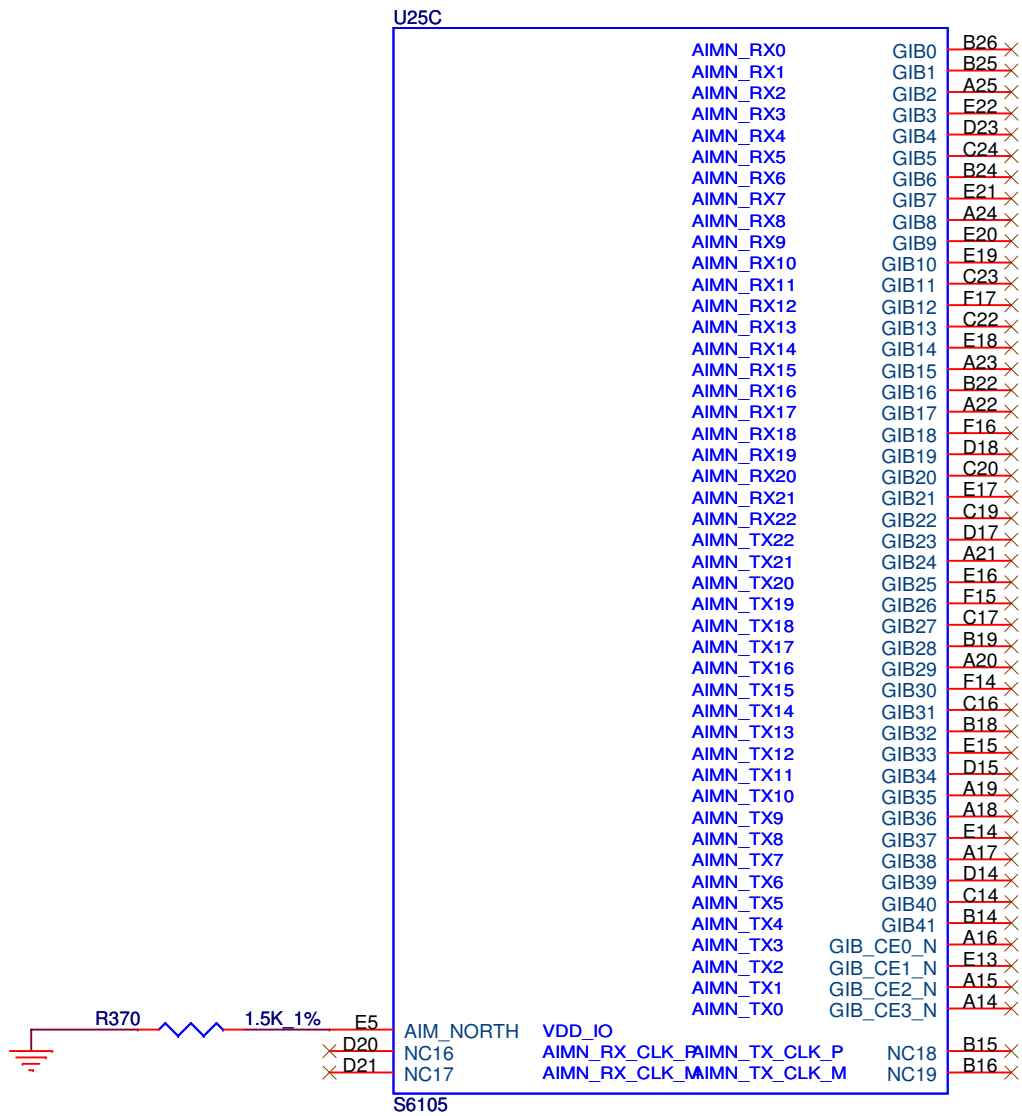


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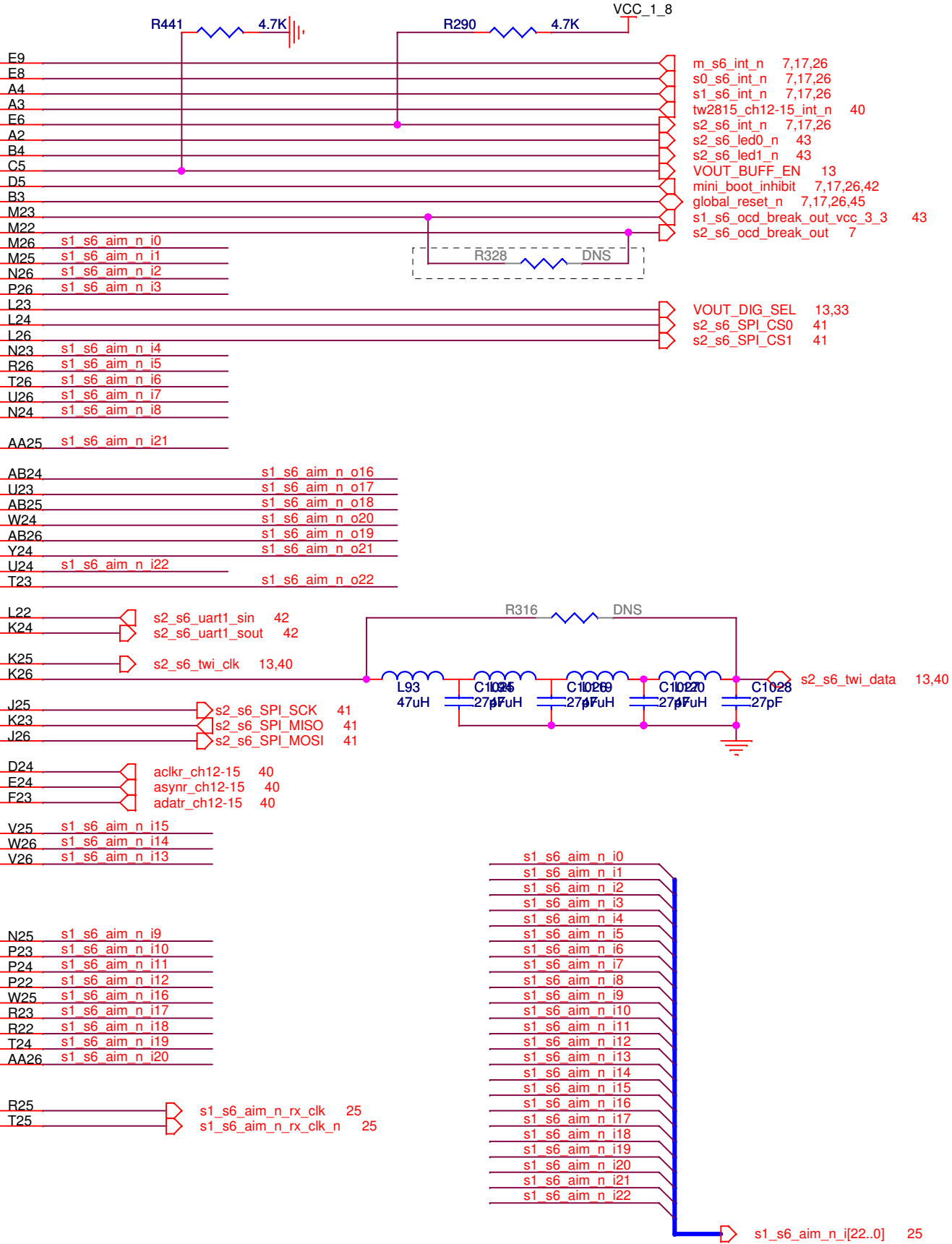
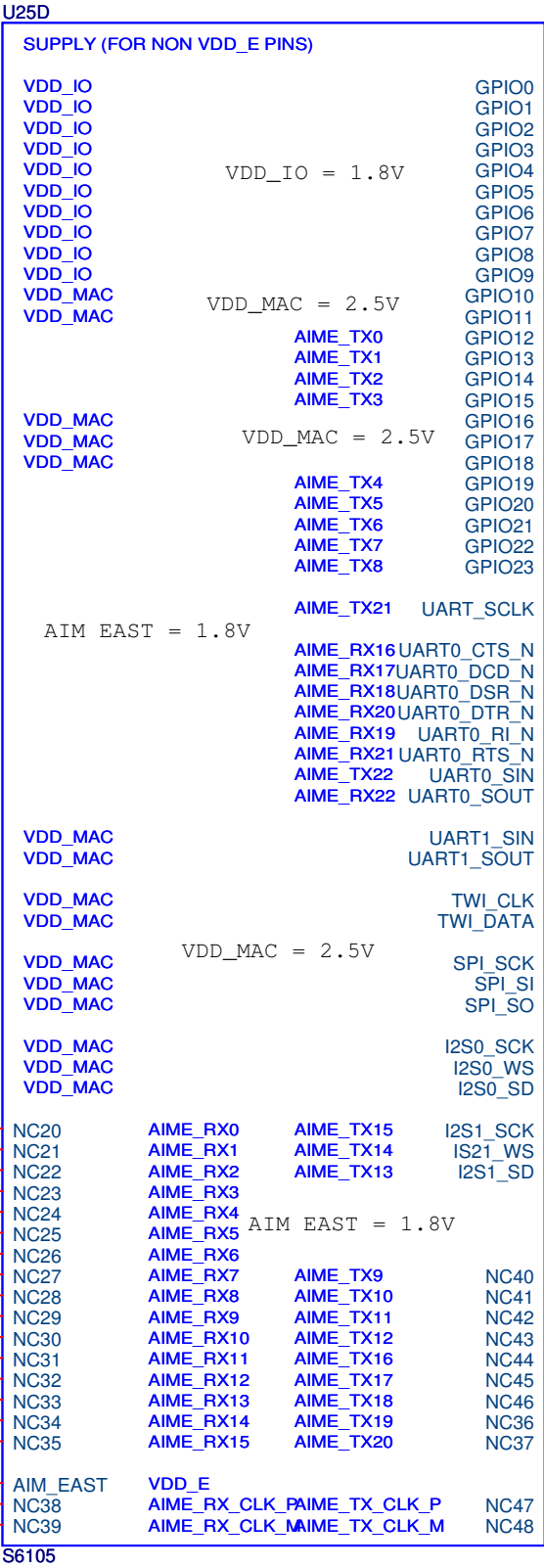
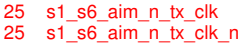
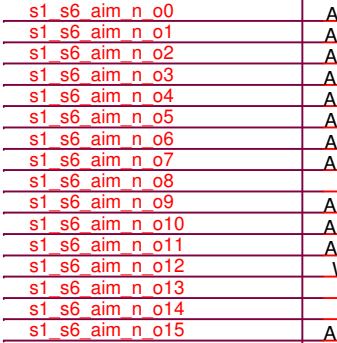
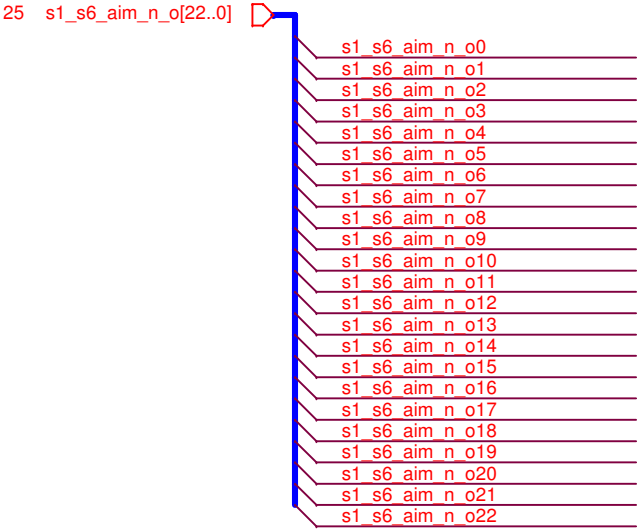
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Secondary 2 S6 (Data Port Interface)				
Size	Document Number	BOM Variant	Internal Version	Rev
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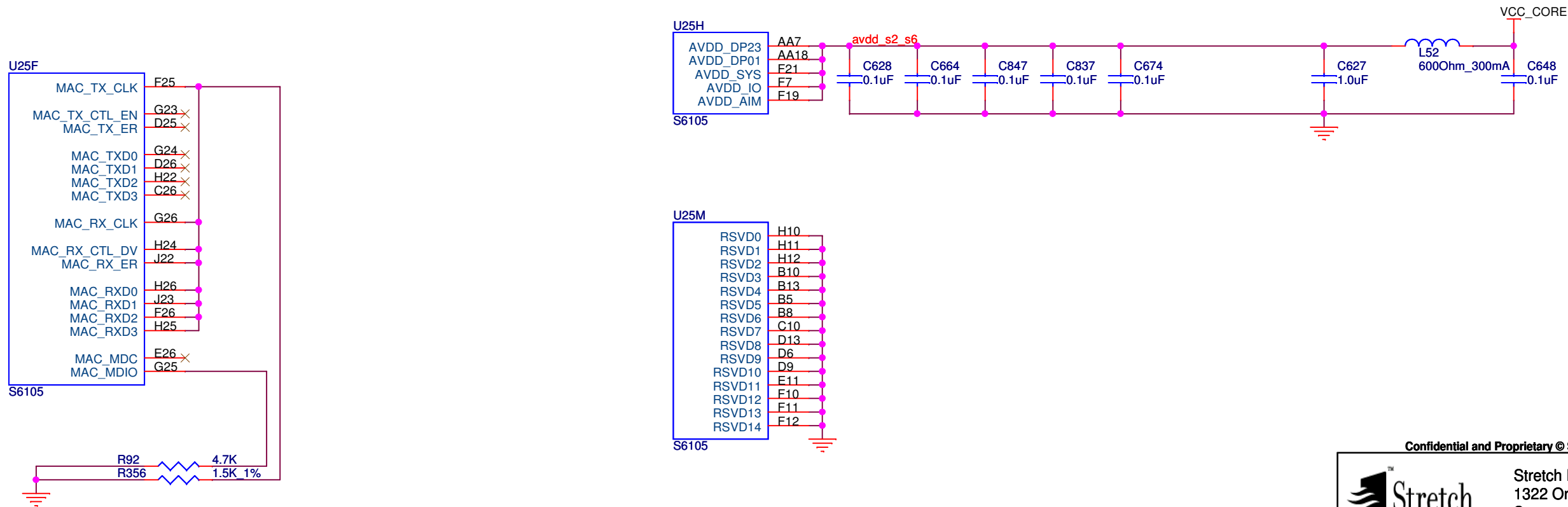
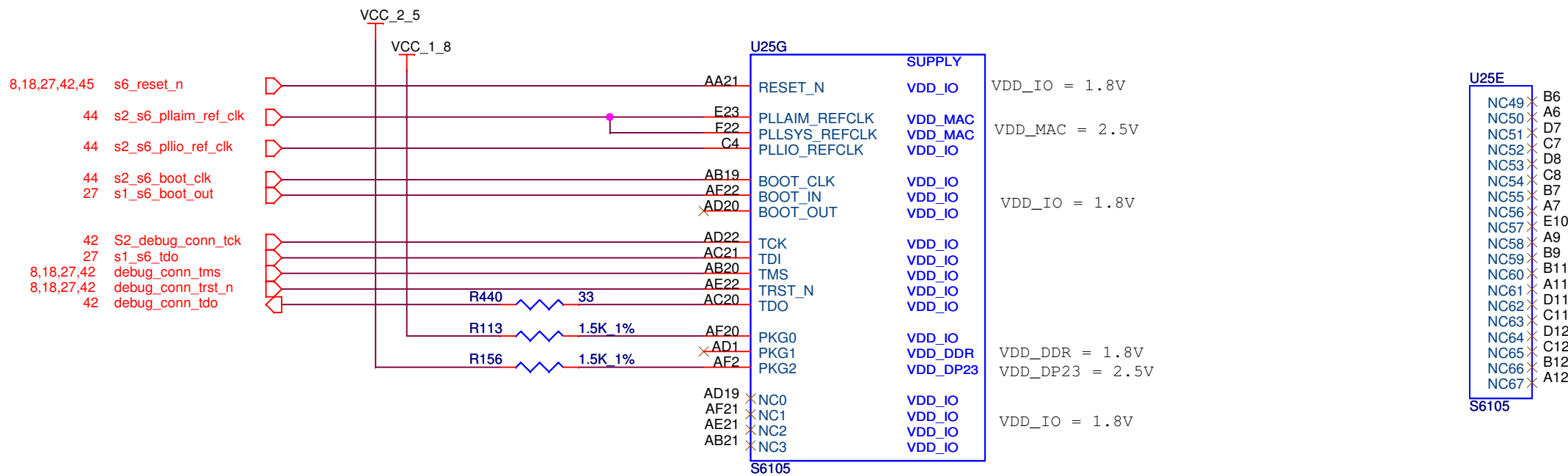


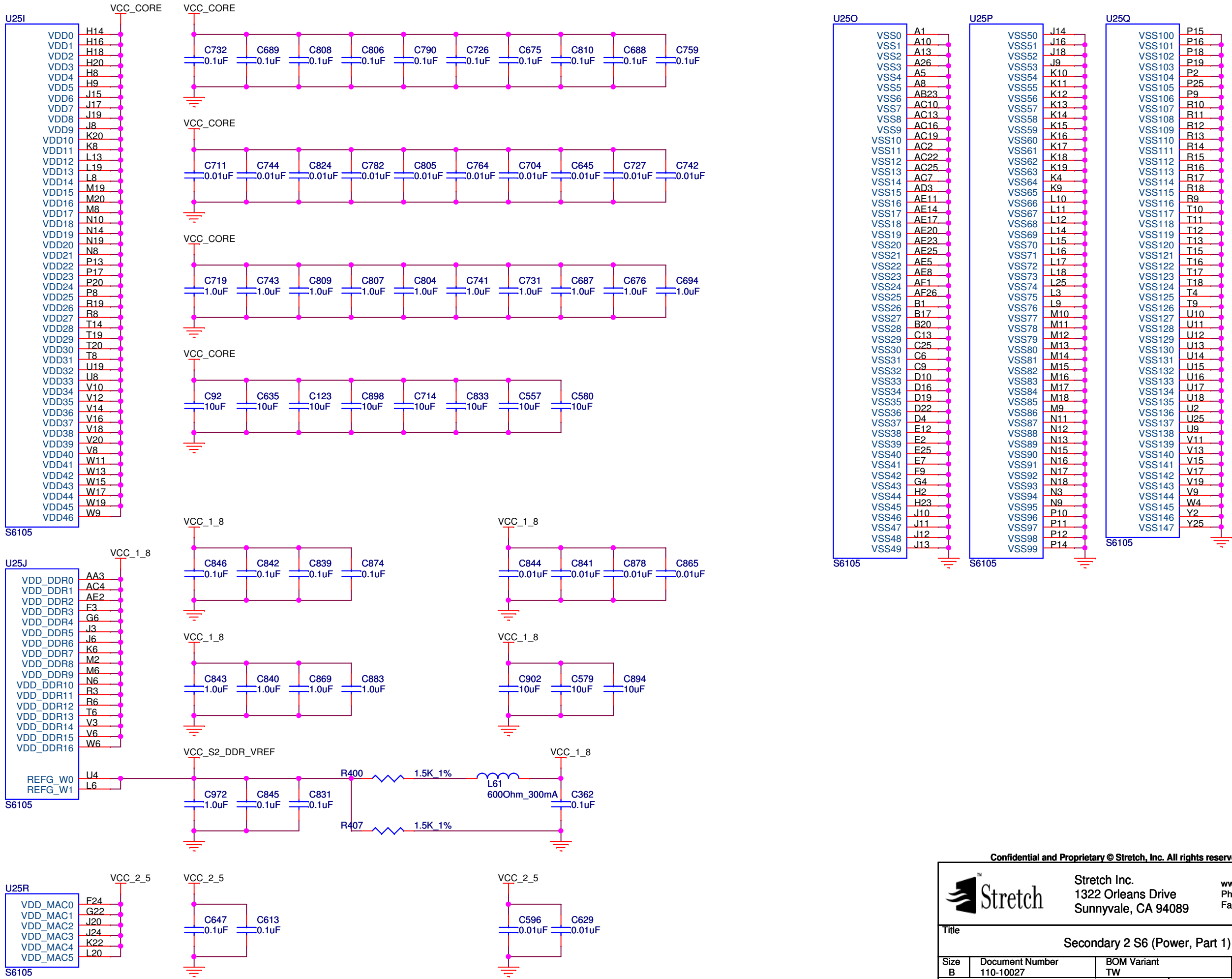


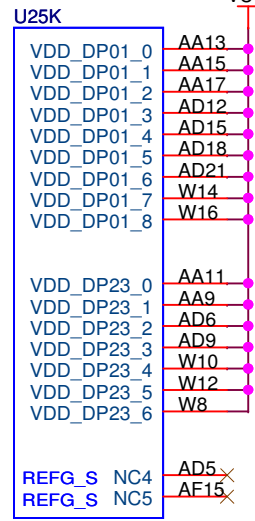
AIM NORTH IS POWERED FROM 2.5V

ROUTING RULES (S6100 package legths should be taken into consideration when determining the trace lengths):  
The AUDIO\_R\_CH12-15 bus should be matched to within +/- 500ps (2500mil).  
The following buses are embedded in the schematic:  
AUDIO\_R\_CH12-15  
->contains aclkr\_ch12-15, asynr\_ch12-15, and adatr\_ch12-15

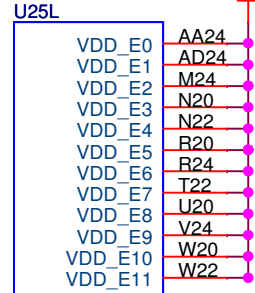




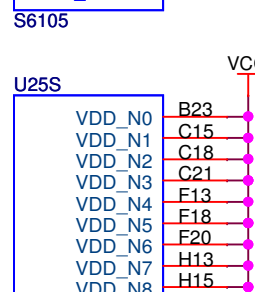




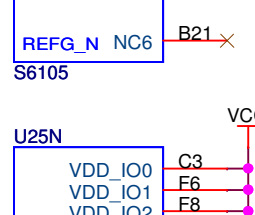
S6105



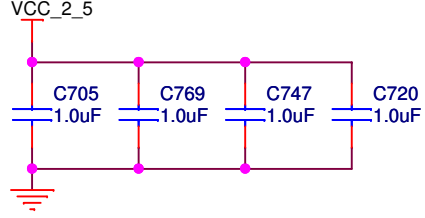
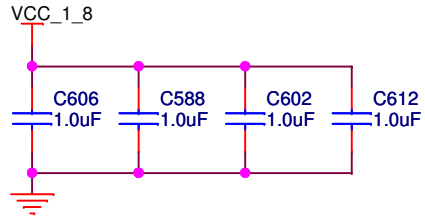
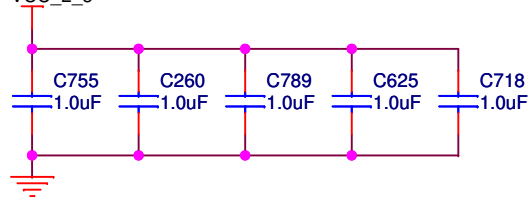
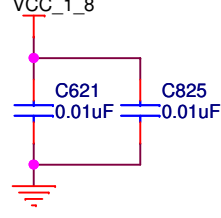
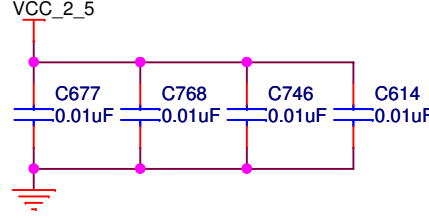
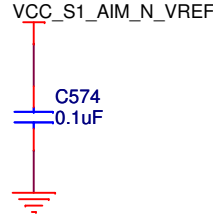
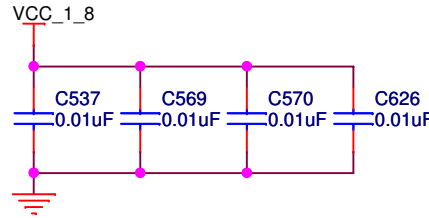
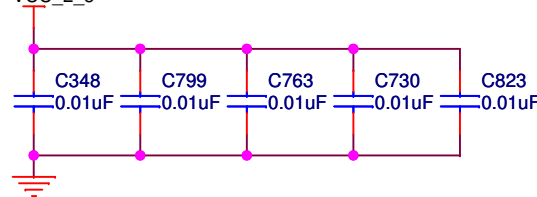
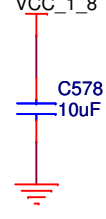
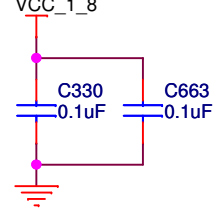
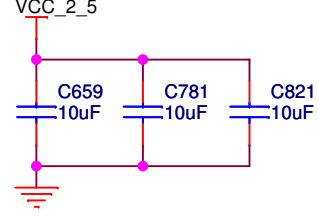
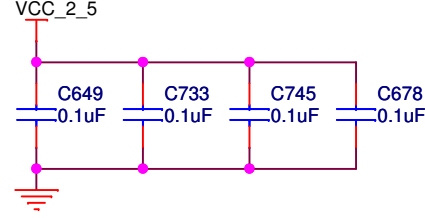
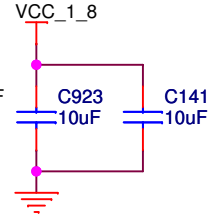
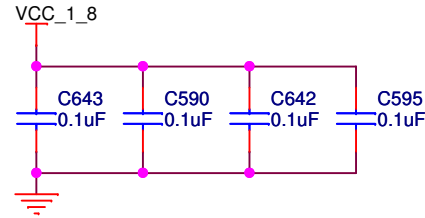
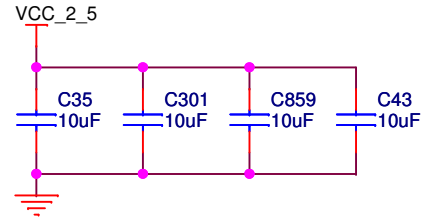
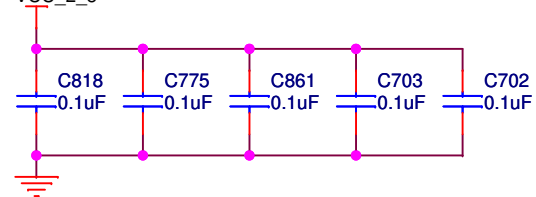
S6105



S6105



S6105



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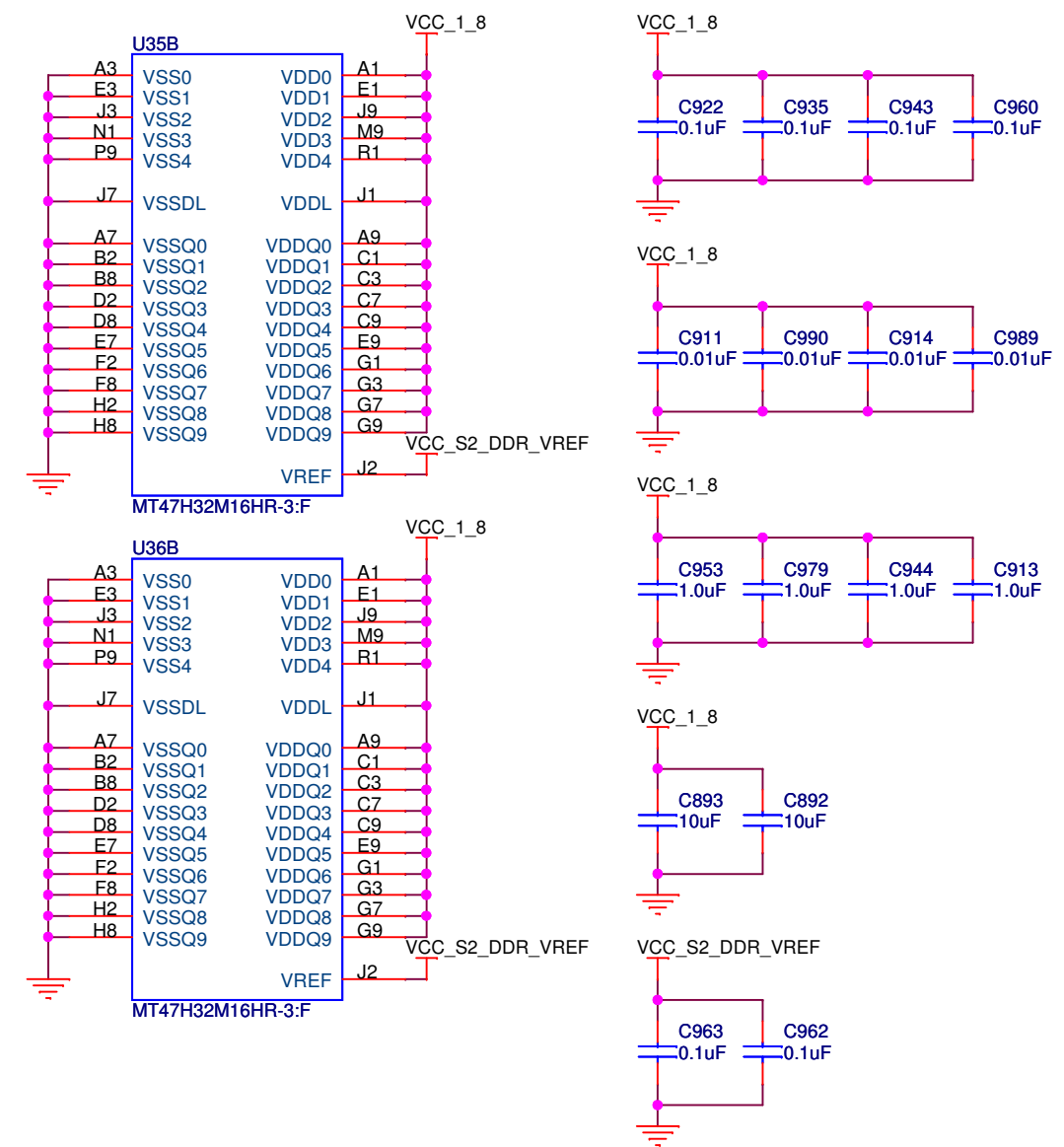
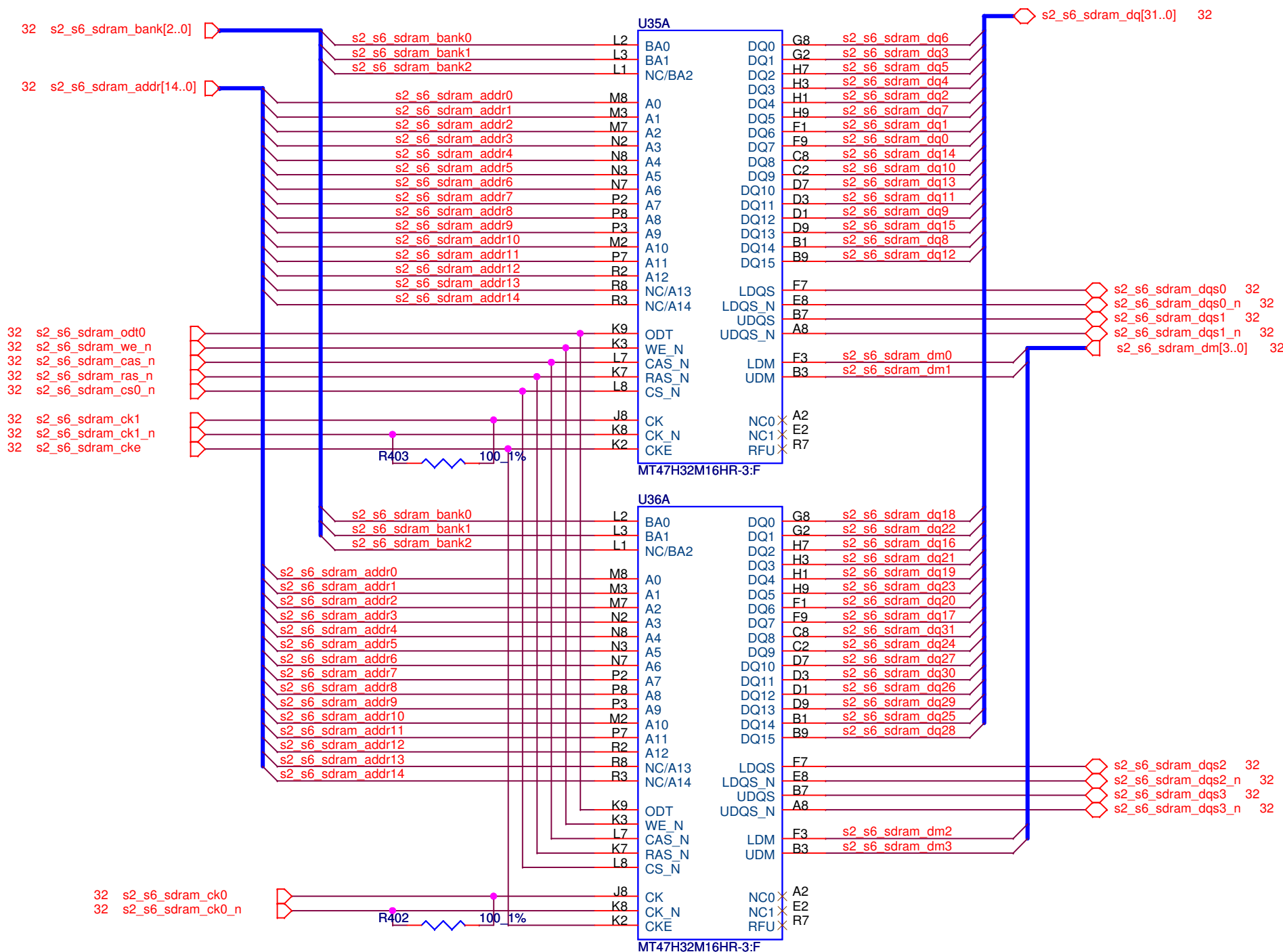


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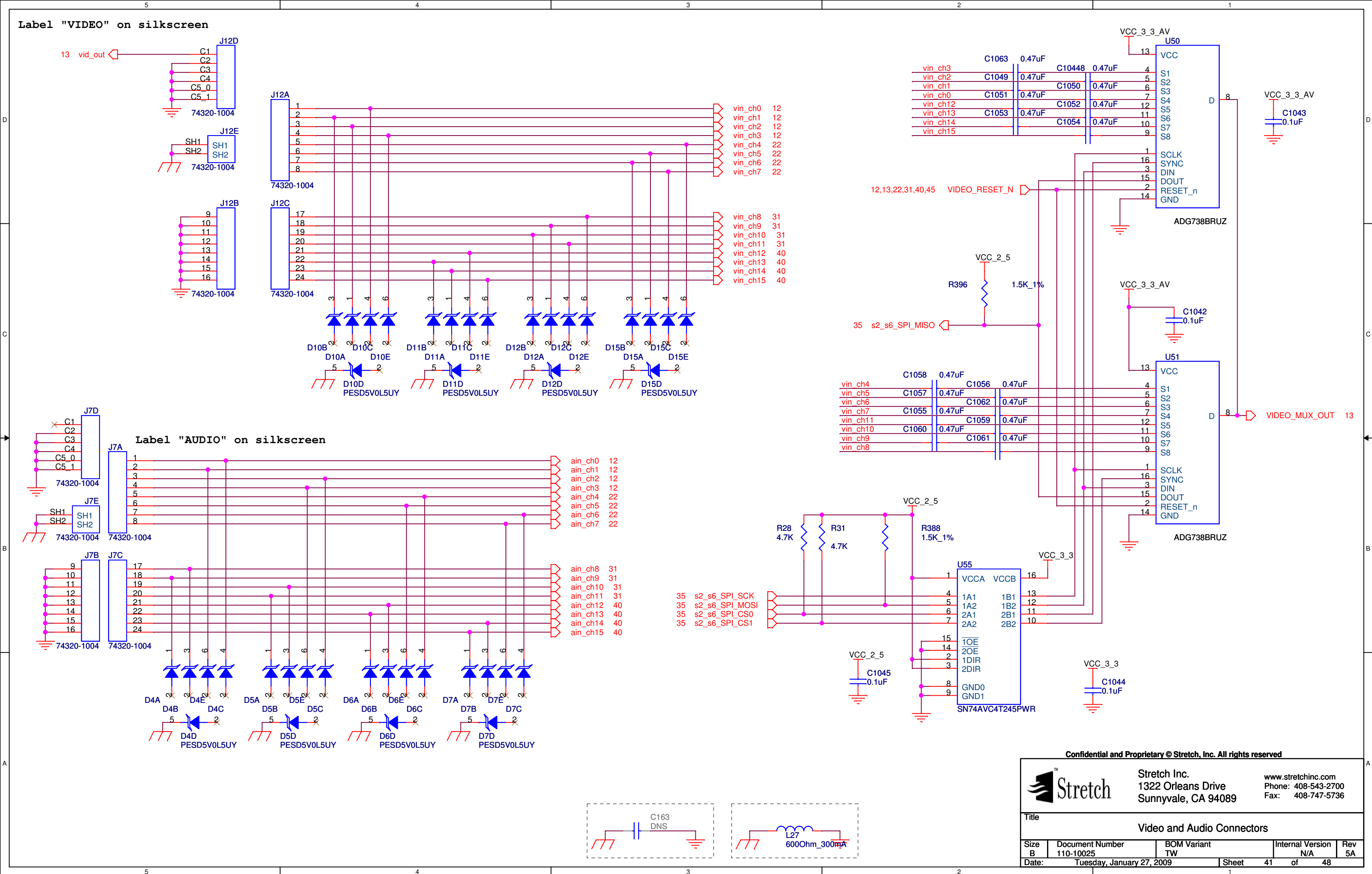
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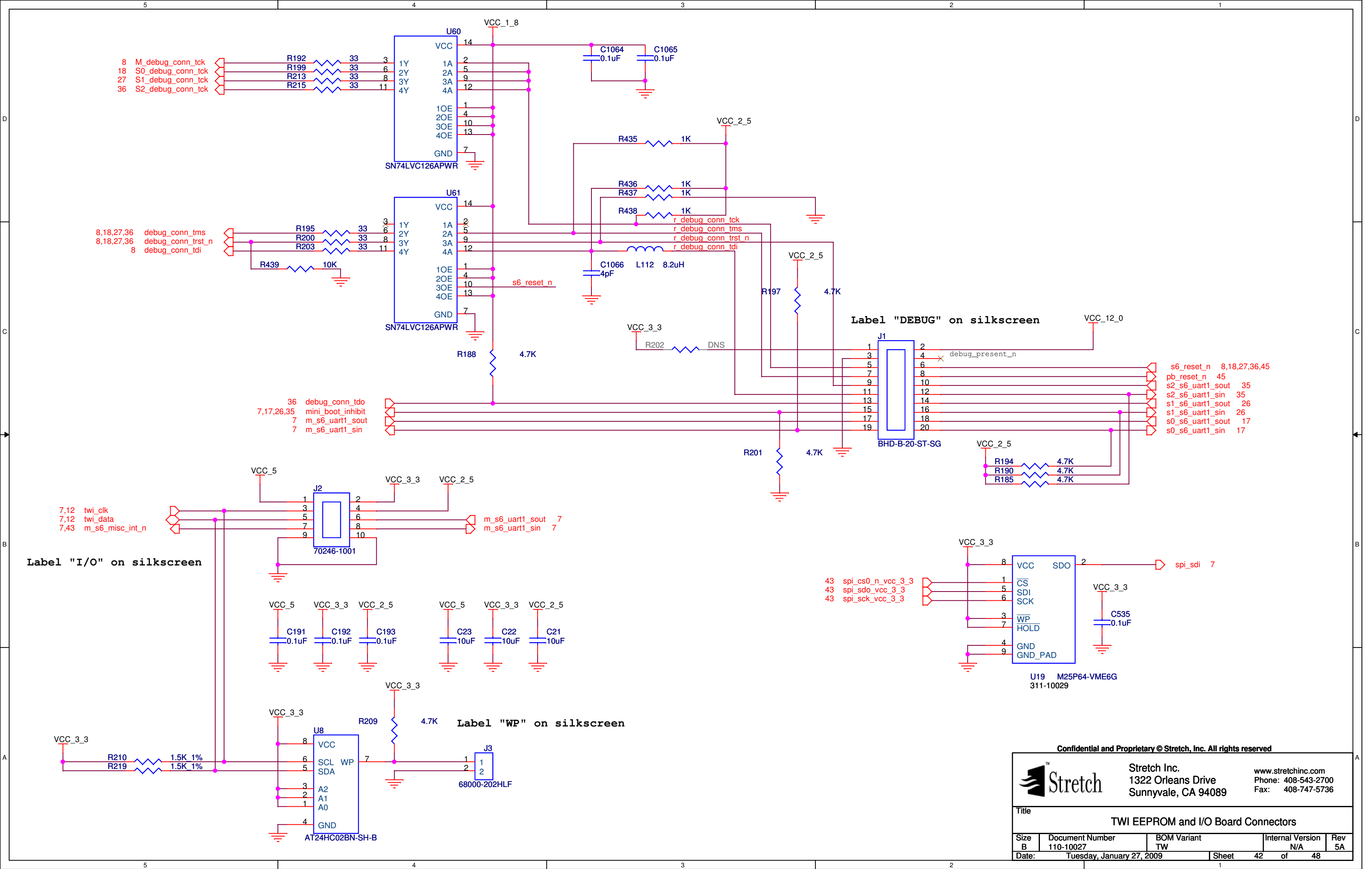
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Secondary 2 S6 (Power, Part 2)				
Size	Document Number	BOM Variant	Internal Version	Rev
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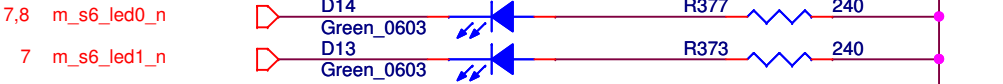




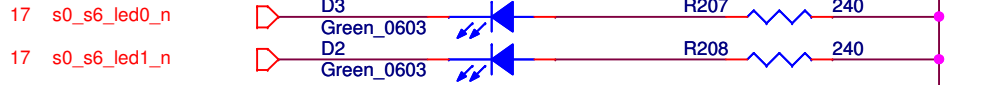




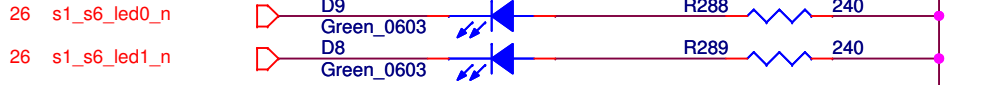
Label "M LED #0" and "M LED #1" on silkscreen



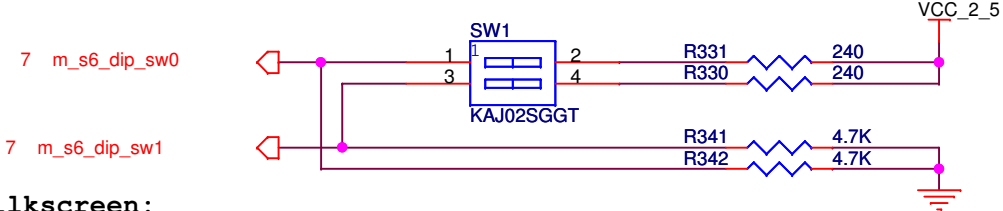
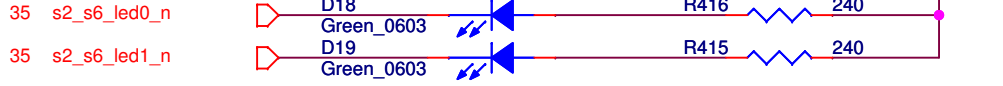
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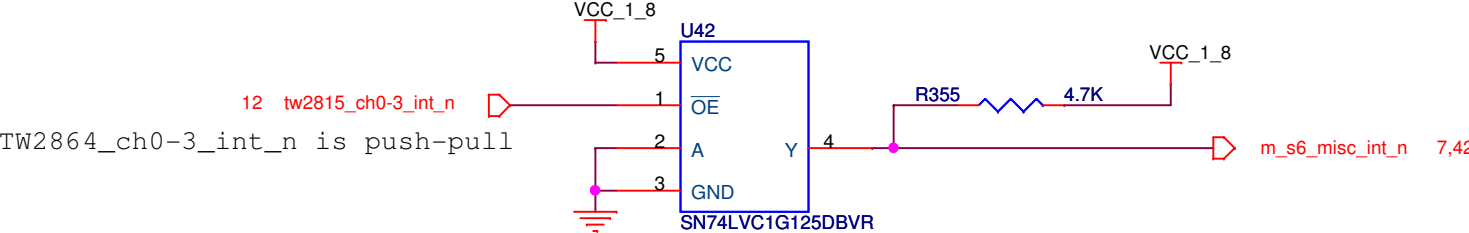
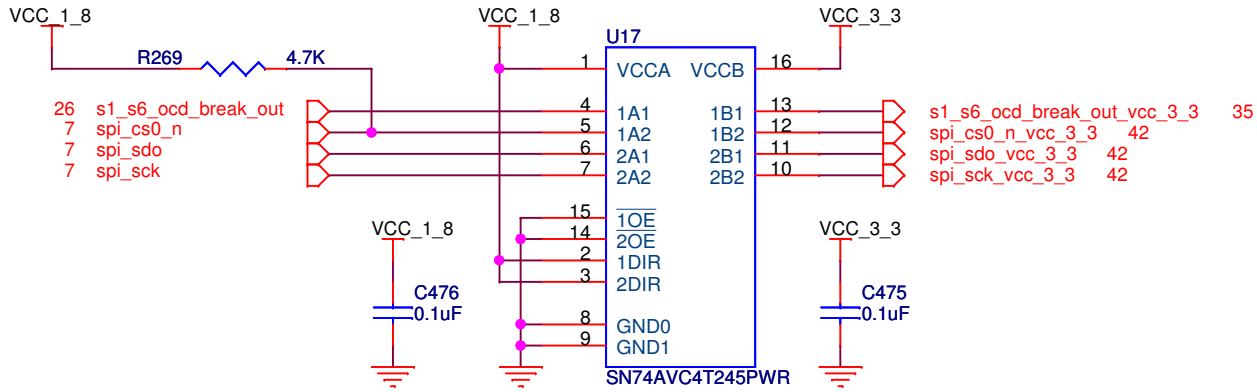
Label "S1 LED #0" and "S1 LED #1" on silkscreen



Label "S2 LED #0" and "S2 LED #1" on silkscreen



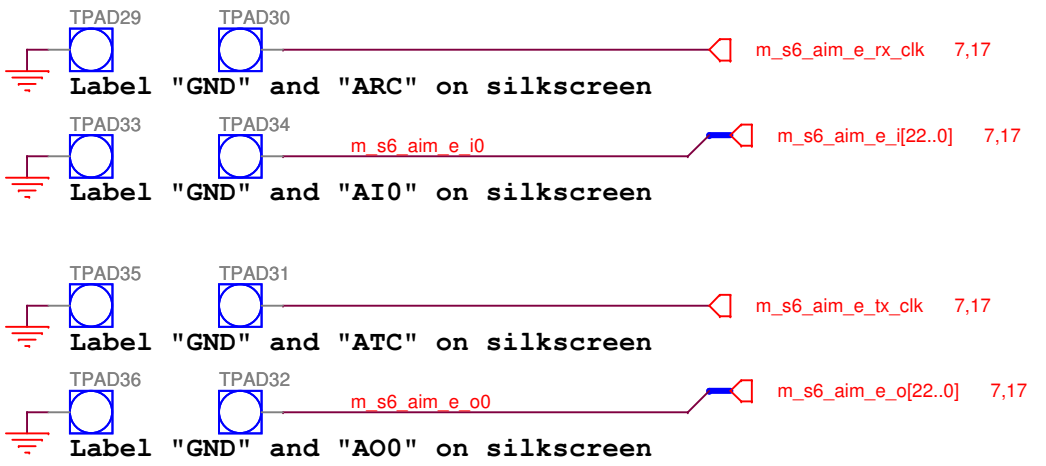
Label silkscreen:  
M\_SW0  
M\_SW1




Minimize stubs



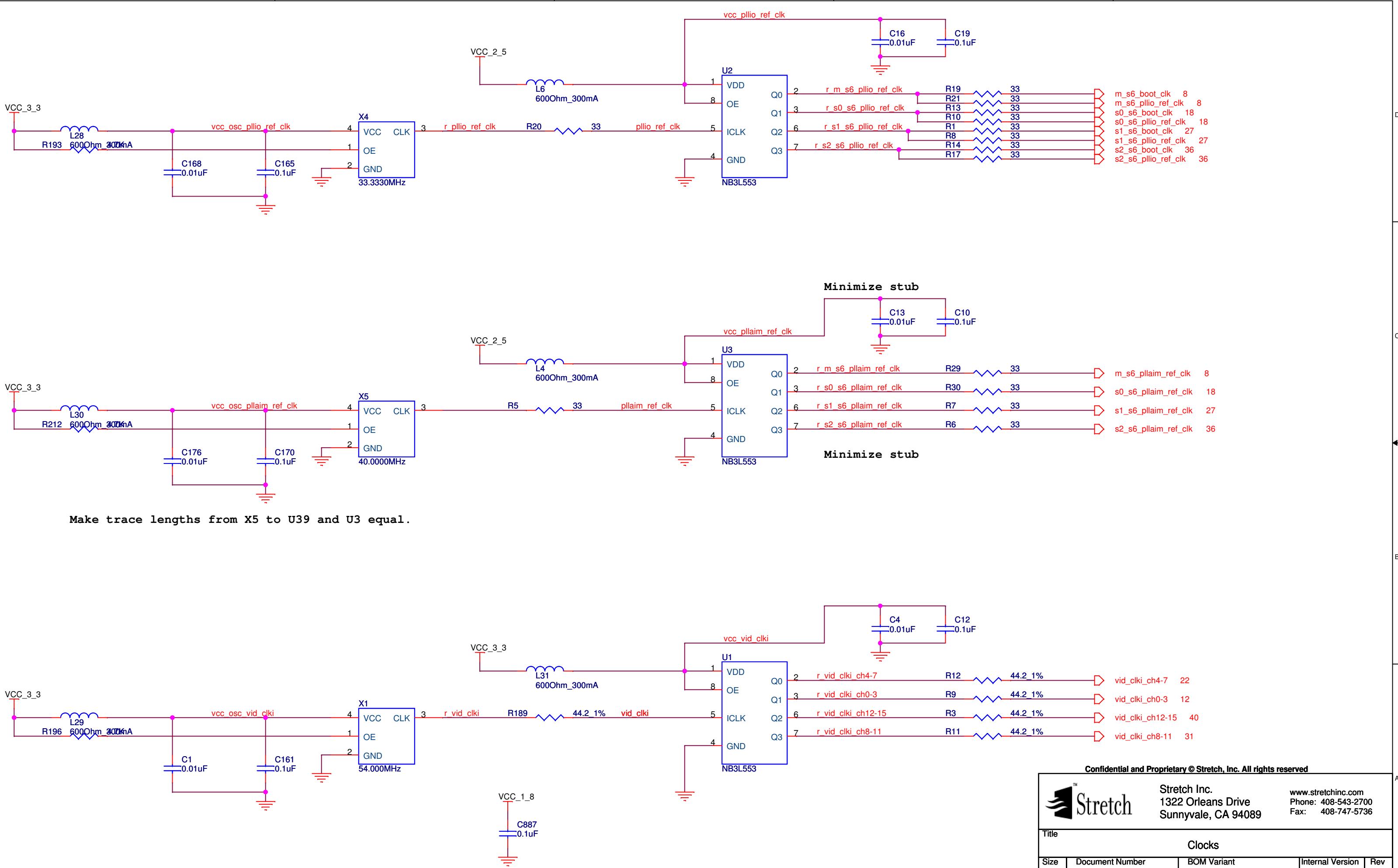
Minimize stubs



Test components are not populated in production system.


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Title Test Components and Signal Test Points				
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Make trace lengths from X5 to U39 and U3 equal.

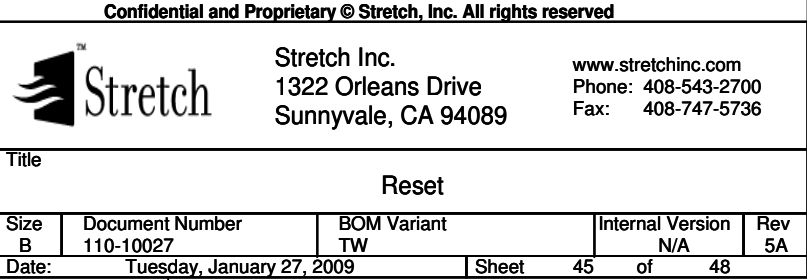
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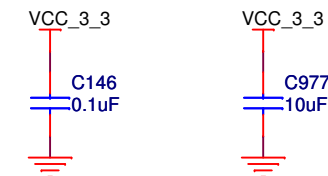
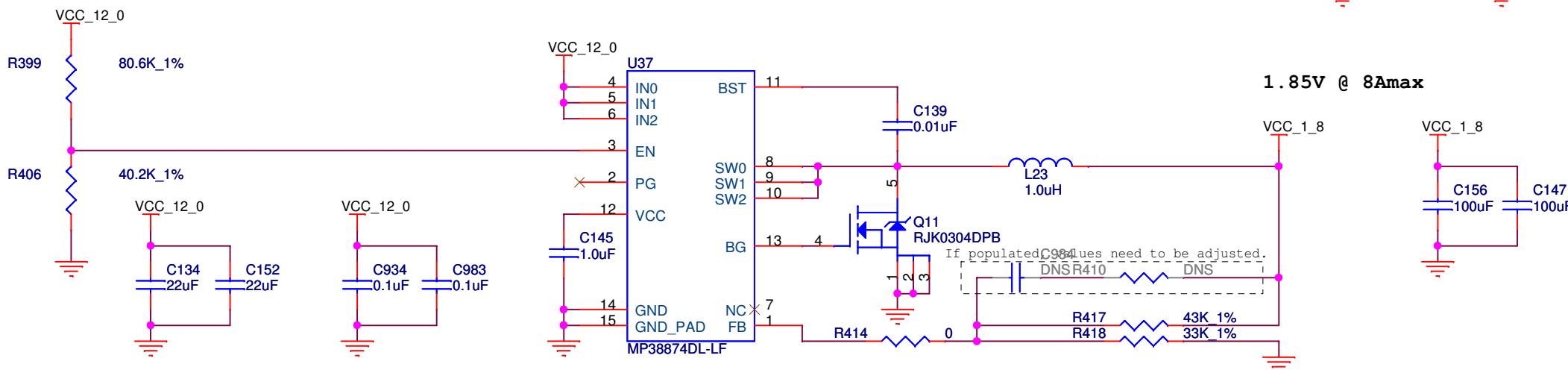
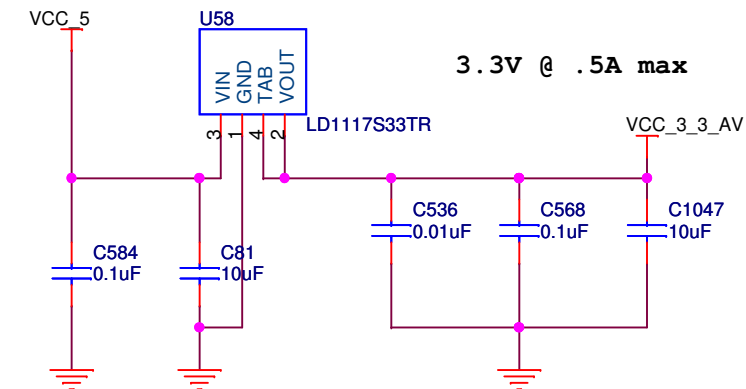
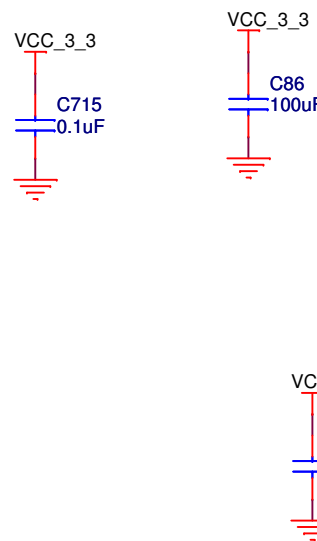
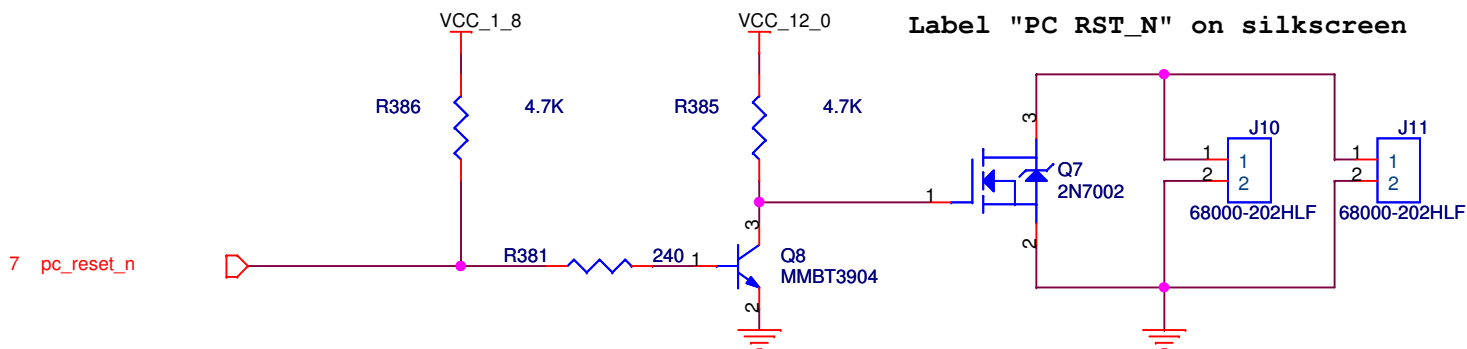
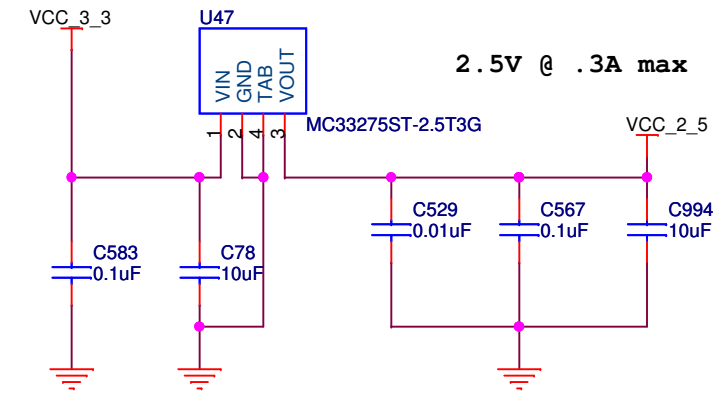
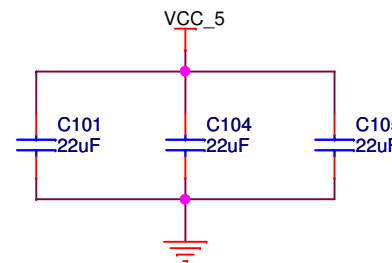
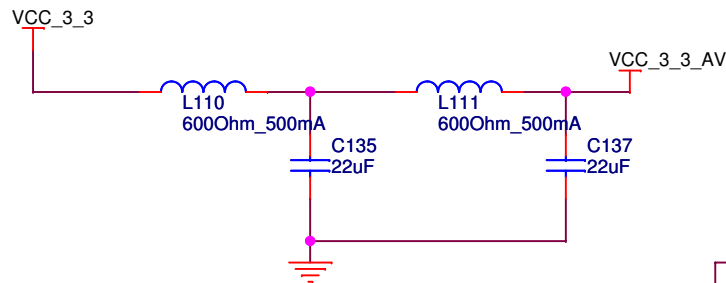
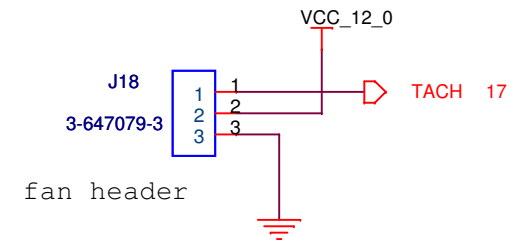
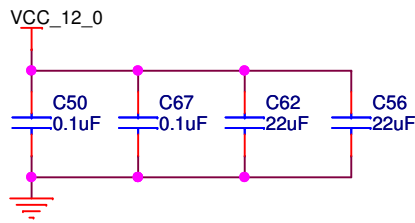
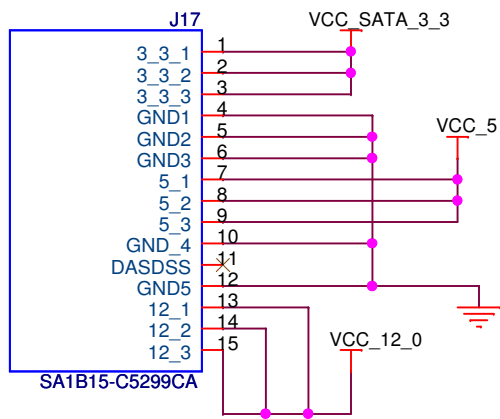


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Clocks				
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Title				
VCC_1_8 and VCC_1_5 Power Supplies				
Size B	Document Number 110-10027	BOM Variant TW	Internal Version N/A	Rev 5A
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