16-D1 PCI Express Reference Design

(Montserrat)

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Title				
Title Page				
Size: B	Document Number: 110-10027	BOM Variant: NVP	Internal Version: N/A	Rev: 5A
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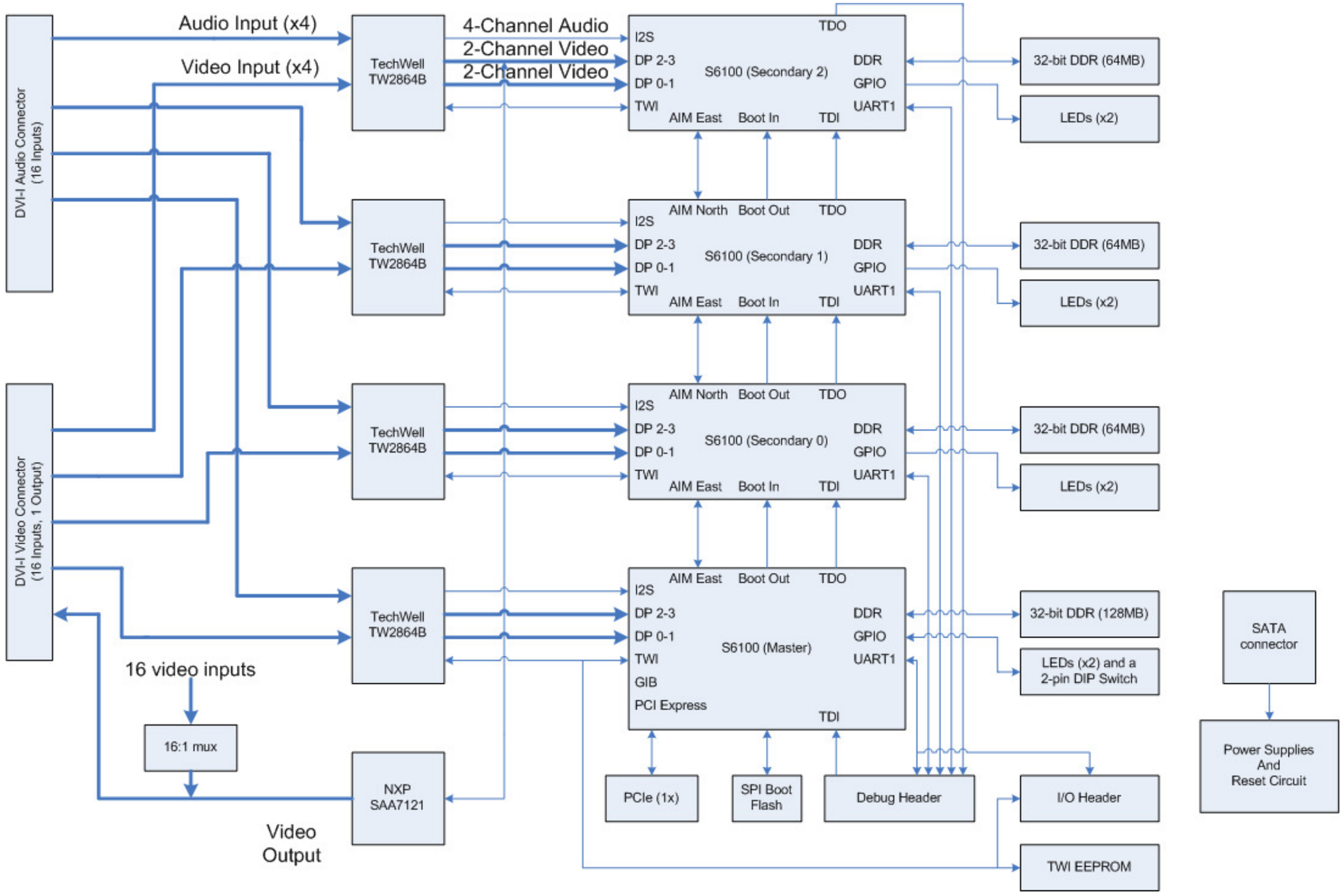

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Title: Block Diagram

Size	Document Number	BOM Variant	Internal Version	Rev
B	110-10027	NVP	N/A	5A

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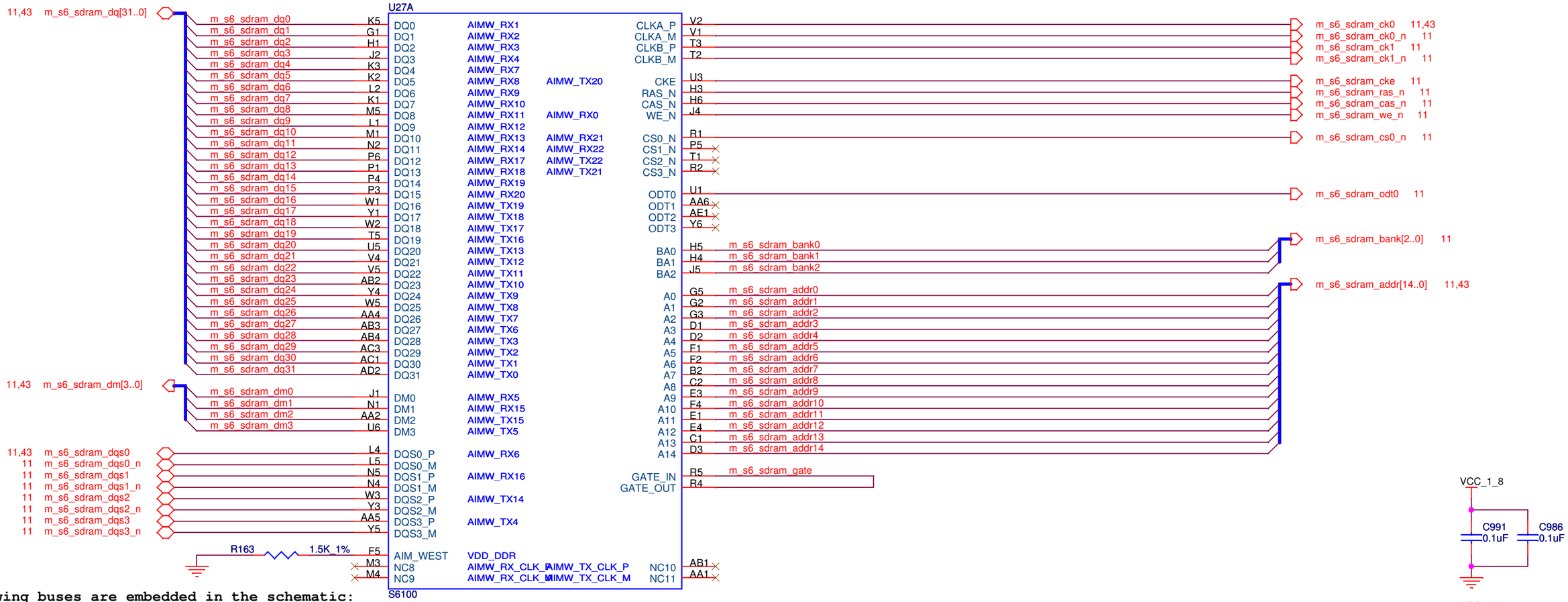

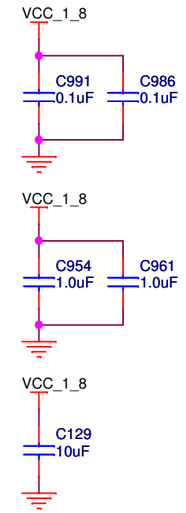

The following buses are embedded in the schematic:
M_S6_DDR_DATA
->contains all the sdram_dq, sdam_dm, sdram_dqs, and sdram_dqs_n signals
M_S6_DDR_CLK
->contains the sdram_ck and sdram_gate signals
M_S6_DDR_ADDR
->contains the sdram_cke, sdram_ras_n, sdram_cas_n, sdram_we_n, sdram_cs0_n,
sdram_bank, and sdram_addr signals

The following differential pairs are embedded in the schematic:
M_S6_DDR_DQS0
M_S6_DDR_DQS1
M_S6_DDR_DQS2
M_S6_DDR_DQS3
M_S6_DDR_CK0
M_S6_DDR_CK1

ROUTING RULES (S6100 package legths should be taken into consideration when determining the trace lengths):
1) Differential pairs should be matched to within +/- 5ps (25mil) .
2) The DDR_ADDR bus and clocks should be matched to within +/- 75ps (375mil).
3) The DDR_DATA bus should be matched to within +/- 50ps (250mil).
4) The signals in a byte lane should be matched to within +/- 30ps (150mil) and be routed on the same layer.
5) The clocks and dqs signals should be matched to within +/- 100ps (500mil).
6) m_s6_sdram_gate signal should be as short as possible and accesible using a via.

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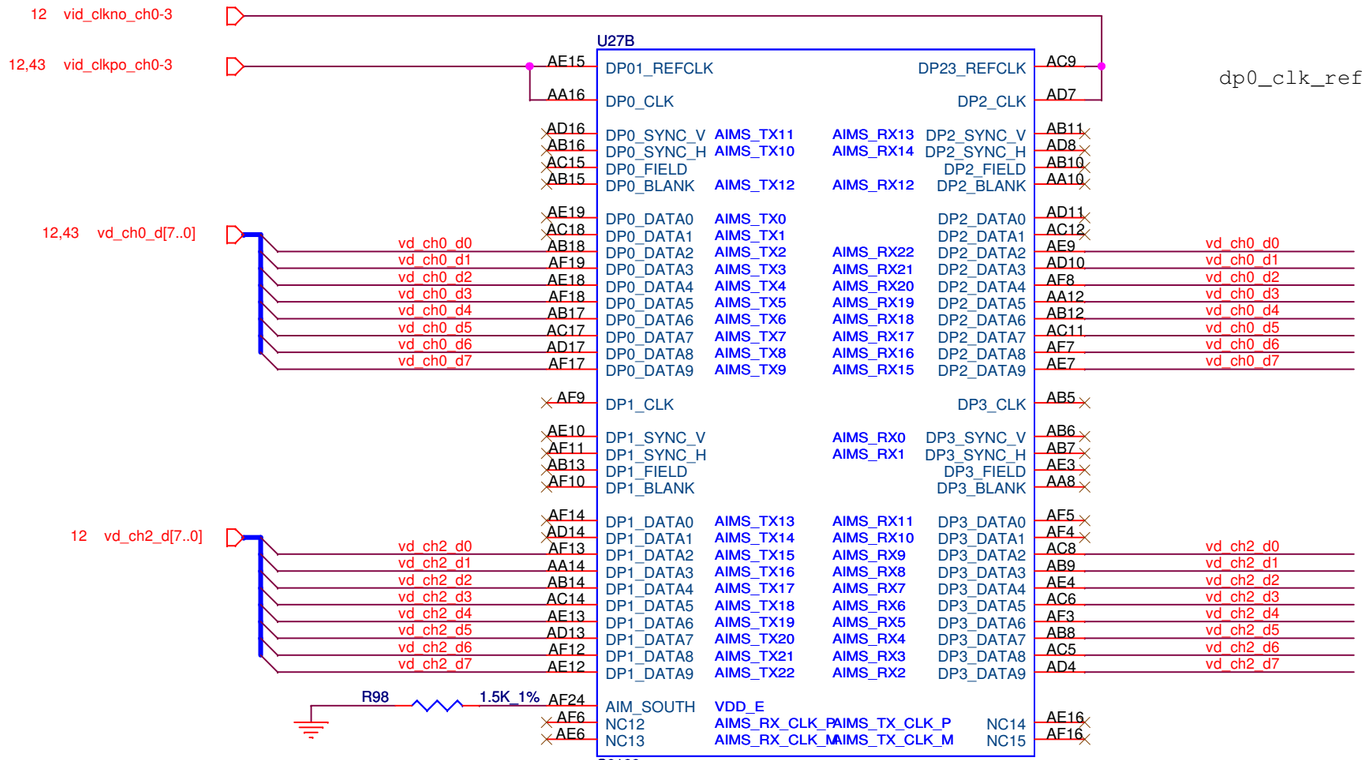
Title				
Master S6 (DDR Interface)				
Size B	Document Number 110-10027	BOM Variant NVP	Internal Version N/A	Rev 5A
Date: Tuesday, January 27, 2009	Sheet 4 of 48			



dp0_clk_ref and dp2_clk_ref need to be driven for reset initialization.

DP0-3 are supplied by 2.5V

The following buses are embedded in the schematic:
VD_CH0
->contains all the vd_ch0 signals
VD_CH2
->contains all the vd_ch2 signals

ROUTING RULES (S6100 package legths should be taken into consideration when determining the trace lengths):
The VD_CH0, VD_CH2 buses, vid_clkpo_ch0-3, vid_clkno_ch0-3 should be matched to within +/- 250ps (1250mil).

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Title				
Master S6 (Data Port Interface)				
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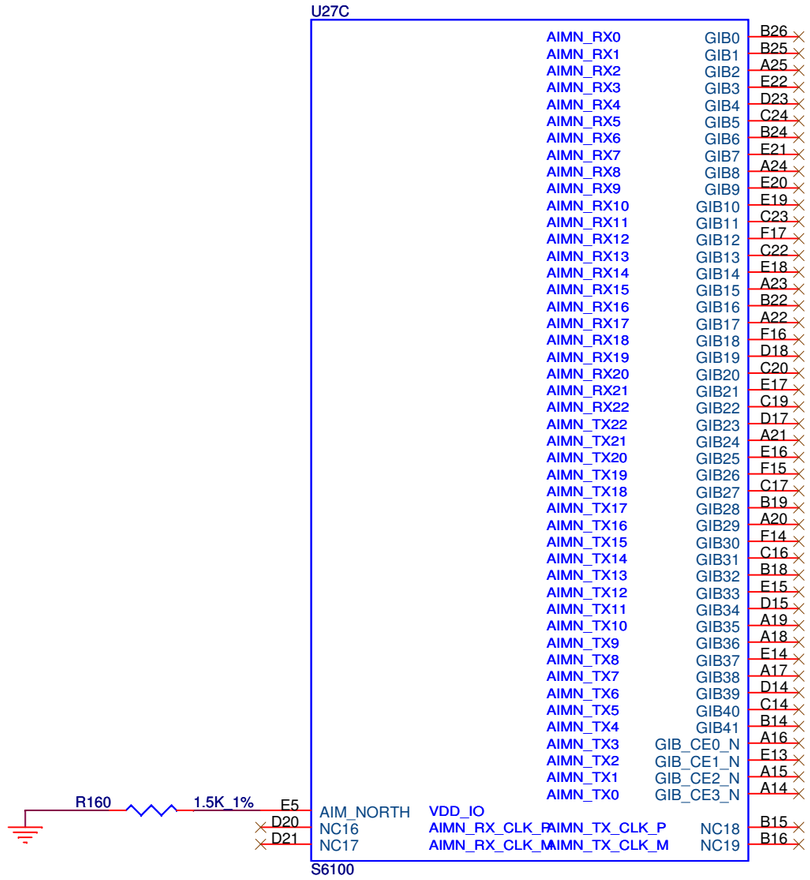
Date: Tuesday, January 27, 2009		Sheet 5 of 48		



AIM NORTH IS POWERED FROM 1.8V

The following buses are embedded in the schematic:
GIB
->contains gib_d[15:0], gib_addr, gib_wr_n, gib_rd_n, and gib_ce0_n

ROUTING RULES (S6100 package legths should be taken into consideration when determining the trace lengths):
The GIB bus should be matched to within +/- 250ps (1250mil).

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Master S6 (GIB Interface)				
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Date: Tuesday, January 27, 2009		Sheet 6 of 48		

ROUTING RULES (S6100 package legths should be taken into consideration when determining the trace lengths):

1) Differential pairs should be matched to within +/- 5ps (25mil).
2) The M_S6_AIM_E_O bus should be matched to within +/- 50ps (250mil).
3) The M_S6_AIM_E_I bus should be matched to within +/- 50ps (250mil).
4) The AUDIO_R_CH0-3 bus should be matched to within +/- 500ps (2500mil).

The following buses are embedded in the schematic:

SPI
->contains all the spi_sdo, spi_sdi, spi_sck, and spi_cs0_n signals
M_S6_AIM_E_O
->contains the aim_e_o, aim_e_tx_clk and aim_e_tx_clk_n signals
M_S6_AIM_E_I
->contains the aim_e_i, aim_e_rx_clk and aim_e_rx_clk_n signals
AUDIO_R_CH0-3
->contains aclkr_ch0-3, asynr_ch0-3, and adatr_ch0-3

The following differential pairs are embedded in the schematic:
M_S6_AIM_E_RX_CLK
M_S6_AIM_E_TX_CLK

U27D

SUPPLY (FOR NON VDD_E PINS)

VDD_IO = 1.8V
VDD_MAC = 2.5V
AIM EAST = 1.8V
VDD_MAC = 2.5V
VDD_MAC = 2.5V
AIM EAST = 1.8V

VDD_IO		GPIO0	E9						m_s6_misc_int_n 42,43
VDD_IO		GPIO1	E8						s0_s6_int_n 17,26,35
VDD_IO		GPIO2	A4						s1_s6_int_n 17,26,35
VDD_IO		GPIO3	A3						s2_s6_int_n 17,26,35
VDD_IO		GPIO4	E6						m_s6_int_n 17,26,35
VDD_IO		GPIO5	A2						m_s6_led0_n 8,43
VDD_IO		GPIO6	B4						m_s6_led1_n 43
VDD_IO		GPIO7	C5						pc_reset_n 46
VDD_IO		GPIO8	D5						mini_boot_inhibit 17,26,35,42
VDD_IO		GPIO9	B3						global_reset_n 17,26,35,45
VDD_MAC		GPIO10	M23						s2_s6_ocd_break_out 35
VDD_MAC		GPIO11	M22						m_s6_ocd_break_out 17
	AIME_TX0	GPIO12	M26	m_s6_aim_e_o0					
	AIME_TX1	GPIO13	M25	m_s6_aim_e_o1					
	AIME_TX2	GPIO14	N26	m_s6_aim_e_o2					
	AIME_TX3	GPIO15	P26	m_s6_aim_e_o3					
VDD_MAC		GPIO16	L23	spi_cs0_n					spi_cs0_n 43
VDD_MAC		GPIO17	L24	m_s6_dip_sw0					m_s6_dip_sw0 43
VDD_MAC		GPIO18	L26	m_s6_dip_sw1					m_s6_dip_sw1 43
	AIME_TX4	GPIO19	N23	m_s6_aim_e_o4					
	AIME_TX5	GPIO20	R26	m_s6_aim_e_o5					
	AIME_TX6	GPIO21	T26	m_s6_aim_e_o6					
	AIME_TX7	GPIO22	U26	m_s6_aim_e_o7					
	AIME_TX8	GPIO23	N24	m_s6_aim_e_o8					
	AIME_TX21	UART_SCLK	AA25	m_s6_aim_e_o21					
	AIME_RX16	UART0_CTS_N	AB24	m_s6_aim_e_i16					
	AIME_RX17	UART0_DCD_N	U23	m_s6_aim_e_i17					
	AIME_RX18	UART0_DSR_N	AB25	m_s6_aim_e_i18					
	AIME_RX20	UART0_DTR_N	W24	m_s6_aim_e_i20					
	AIME_RX19	UART0_RI_N	AB26	m_s6_aim_e_i19					
	AIME_RX21	UART0_RTS_N	Y24	m_s6_aim_e_i21					
	AIME_TX22	UART0_SIN	U24	m_s6_aim_e_o22					
	AIME_RX22	UART0_SOUT	T23	m_s6_aim_e_i22					
VDD_MAC		UART1_SIN	L22	m_s6_uart1_sin 42					
VDD_MAC		UART1_SOUT	K24	m_s6_uart1_sout 42					
VDD_MAC		TWI_CLK	K25	twi_clk 12,42					
VDD_MAC		TWI_DATA	K26	r_twi_data					
VDD_MAC		SPI_SCK	J25	spi_sck 43					
VDD_MAC		SPI_SI	K23	spi_sdi 42					
VDD_MAC		SPI_SO	J26	spi_sdo 43					
VDD_MAC		I2S0_SCK	D24	aclkr_ch0-3 12					
VDD_MAC		I2S0_WS	E24	asynr_ch0-3 12					
VDD_MAC		I2S0_SD	F23	adatr_ch0-3 12					
		I2S1_SCK	V25	m_s6_aim_e_o15					
		IS21_WS	W26	m_s6_aim_e_o14					
		I2S1_SD	V26	m_s6_aim_e_o13					
			N25	m_s6_aim_e_o9					
			P23	m_s6_aim_e_o10					
			P24	m_s6_aim_e_o11					
			P22	m_s6_aim_e_o12					
			W25	m_s6_aim_e_o16					
			R23	m_s6_aim_e_o17					
			R22	m_s6_aim_e_o18					
			T24	m_s6_aim_e_o19					
			AA26	m_s6_aim_e_o20					
AIM_EAST	VDD_E								
NC38	AIME_RX_CLK_P	AIME_TX_CLK_P	NC47	R25	m_s6_aim_e_tx_clk 17,43				
NC39	AIME_RX_CLK_M	AIME_TX_CLK_M	NC48	T25	m_s6_aim_e_tx_clk_n 17				
NC20	AIME_RX0	AIME_TX15							
NC21	AIME_RX1	AIME_TX14							
NC22	AIME_RX2	AIME_TX13							
NC23	AIME_RX3								
NC24	AIME_RX4								
NC25	AIME_RX5								
NC26	AIME_RX6								
NC27	AIME_RX7	AIME_TX9	NC40						
NC28	AIME_RX8	AIME_TX10	NC41						
NC29	AIME_RX9	AIME_TX11	NC42						
NC30	AIME_RX10	AIME_TX12	NC43						
NC31	AIME_RX11	AIME_TX16	NC44						
NC32	AIME_RX12	AIME_TX17	NC45						
NC33	AIME_RX13	AIME_TX18	NC46						
NC34	AIME_RX14	AIME_TX19	NC36						
NC35	AIME_RX15	AIME_TX20	NC37						

S6100

VCC_1_8 — R240 4.7K

R106 1.5K_1%

R220 DNS — L63 47uH, L64 47uH, L113 47uH, L114 47uH — C995 27pF, C996 27pF, C997 27pF, C998 DNS — twi_data 12,42

17,43 m_s6_aim_e_i[22..0]
m_s6_aim_e_i0
m_s6_aim_e_i1
m_s6_aim_e_i2
m_s6_aim_e_i3
m_s6_aim_e_i4
m_s6_aim_e_i5
m_s6_aim_e_i6
m_s6_aim_e_i7
m_s6_aim_e_i8
m_s6_aim_e_i9
m_s6_aim_e_i10
m_s6_aim_e_i11
m_s6_aim_e_i12
m_s6_aim_e_i13
m_s6_aim_e_i14
m_s6_aim_e_i15
m_s6_aim_e_i16
m_s6_aim_e_i17
m_s6_aim_e_i18
m_s6_aim_e_i19
m_s6_aim_e_i20
m_s6_aim_e_i21
m_s6_aim_e_i22

m_s6_aim_e_o0
m_s6_aim_e_o1
m_s6_aim_e_o2
m_s6_aim_e_o3
m_s6_aim_e_o4
m_s6_aim_e_o5
m_s6_aim_e_o6
m_s6_aim_e_o7
m_s6_aim_e_o8
m_s6_aim_e_o9
m_s6_aim_e_o10
m_s6_aim_e_o11
m_s6_aim_e_o12
m_s6_aim_e_o13
m_s6_aim_e_o14
m_s6_aim_e_o15
m_s6_aim_e_o16
m_s6_aim_e_o17
m_s6_aim_e_o18
m_s6_aim_e_o19
m_s6_aim_e_o20
m_s6_aim_e_o21
m_s6_aim_e_o22
m_s6_aim_e_o[22..0] 17,43

17,43 m_s6_aim_e_rx_clk
17 m_s6_aim_e_rx_clk_n

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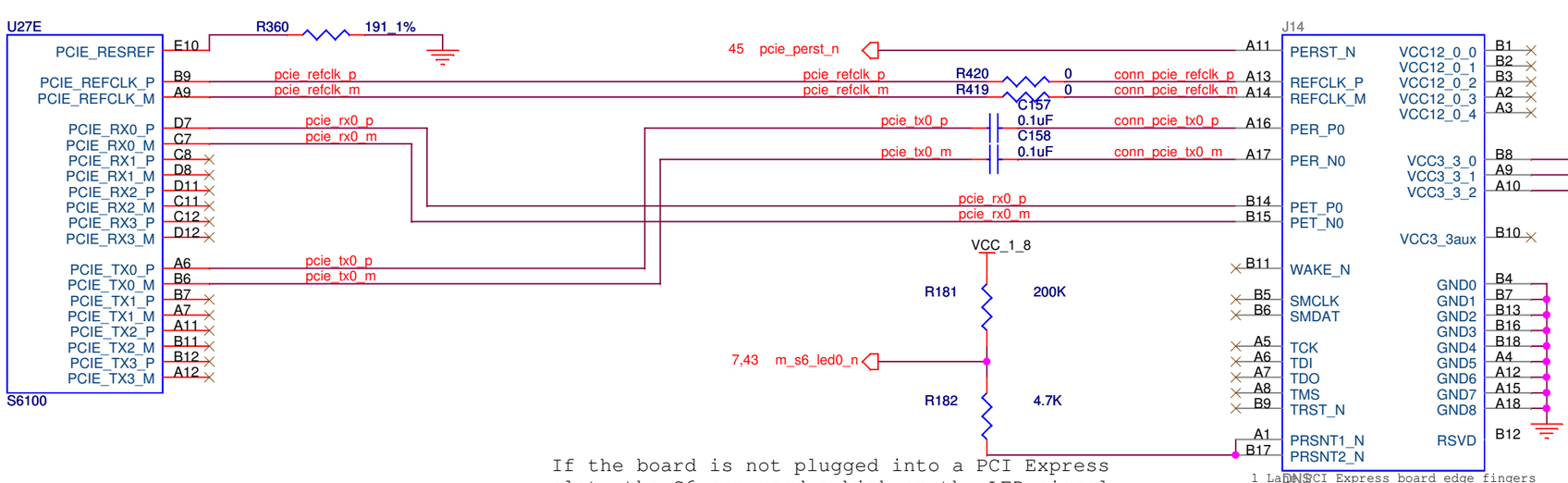
Title: Master S6 (Low Speed Interfaces)

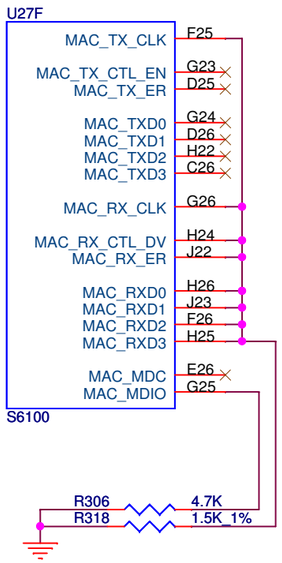
Size	Document Number	BOM Variant	Internal Version	Rev
B	110-10027	NVP	N/A	5A

Date: Tuesday, January 27, 2009 Sheet 7 of 48

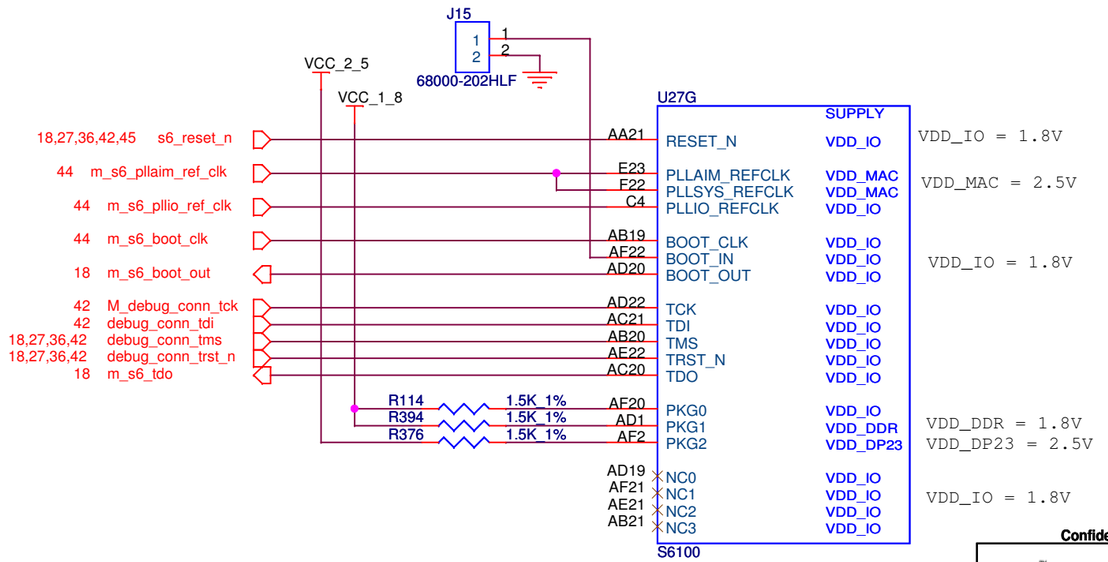


If the board is not plugged into a PCI Express slot, the S6 can read a high on the LED signal, otherwise, a low will be detected (PRSNT1_N is connected to ground on the system board).

The following differential pairs are embedded in the schematic:
CONN_PCIE_TX0
CONN_PCIE_REFCLK



ROUTING RULES (S6100 package legths should be taken into consideration when determining the trace lengths):
1) The differential pairs should be routed to within 5mil.
2) The length from the PCI Express connector to the S6100 should be less than 3.5".
3) Extend the PCI fingers such that they can be used for probing signals (no soldermask).



The following buses are embedded in the schematic:
PCIE
->contains all the pcie signals

The following differential pairs are embedded in the schematic:
PCIE_REFCLK
PCIE_RX0
PCIE_TX0

ROUTING RULES (S6100 package legths should be taken into consideration when determining the trace lengths):
1) The differential pairs should be routed to within 5mil.
2) The length from the PCI Express connector to the S6100 should be less than 3.5".

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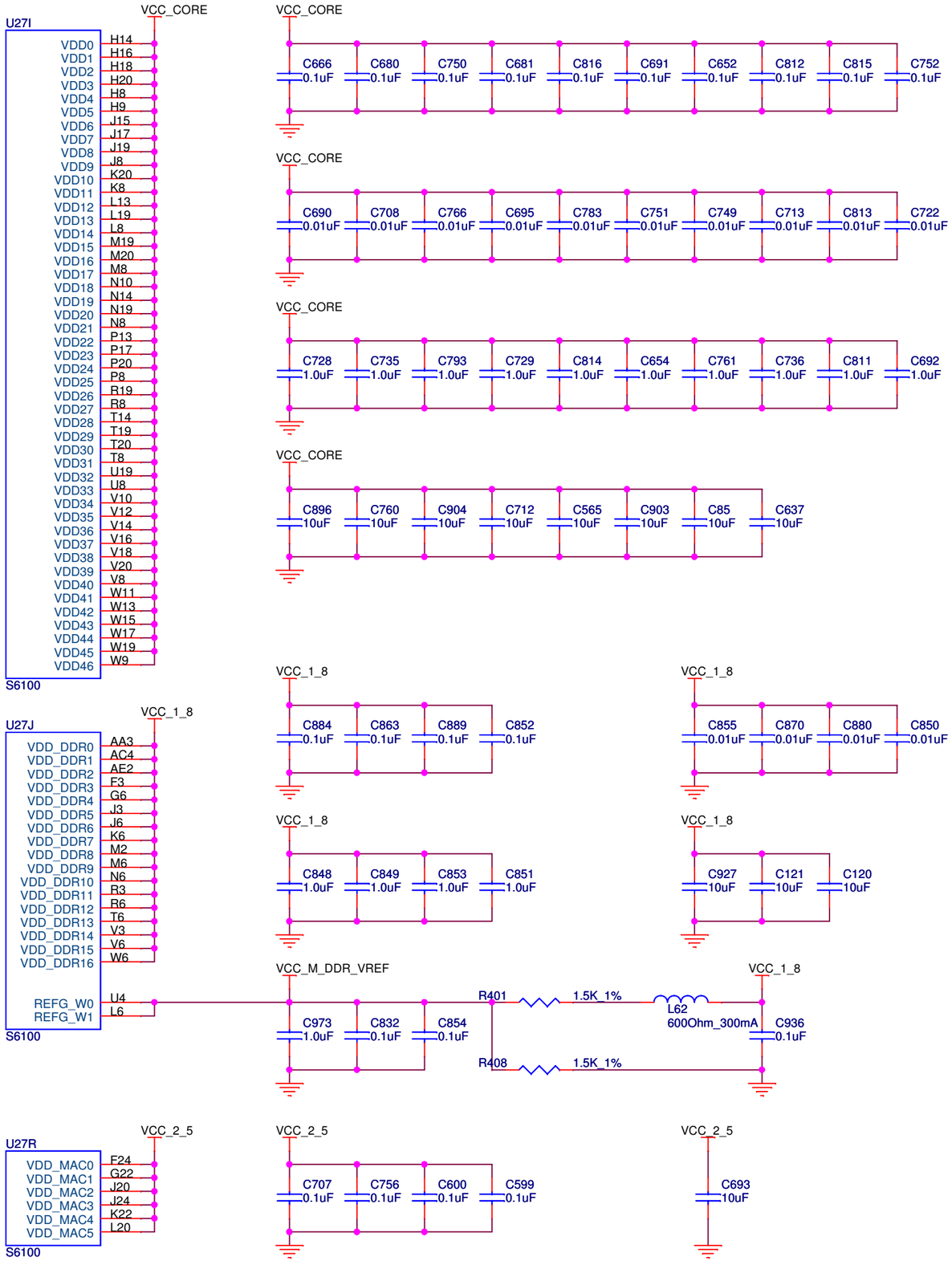
Title: Master S6 (PCI Express and Ethernet Interfaces)

Size	Document Number	BOM Variant	Internal Version	Rev
B	110-10027	NVP	N/A	5A

Date: Tuesday, January 27, 2009 Sheet 8 of 48



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Title: Master S6 (Power, Part 1)

Size	Document Number	BOM Variant	Internal Version	Rev
B	110-10027	NVP	N/A	5A

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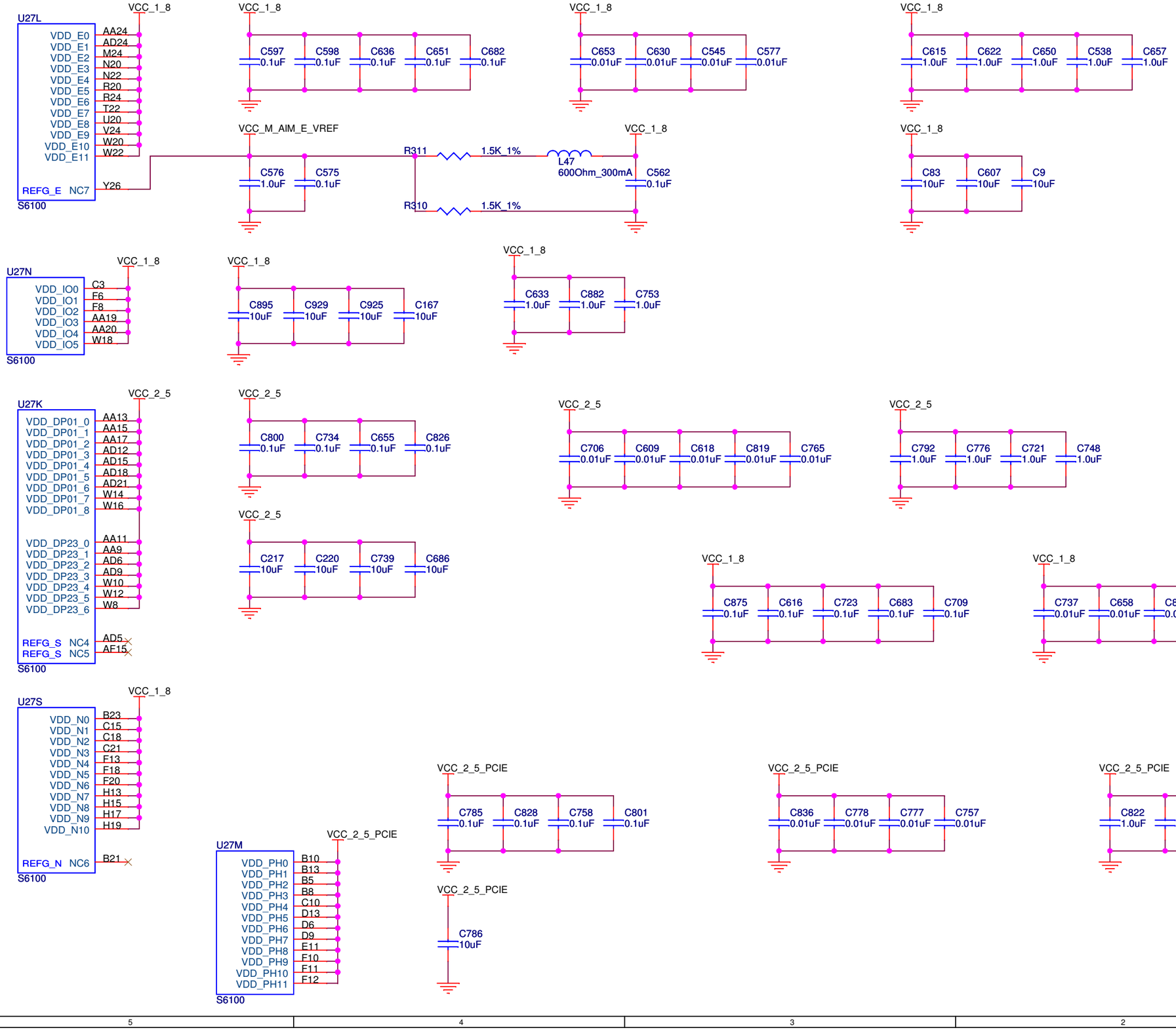

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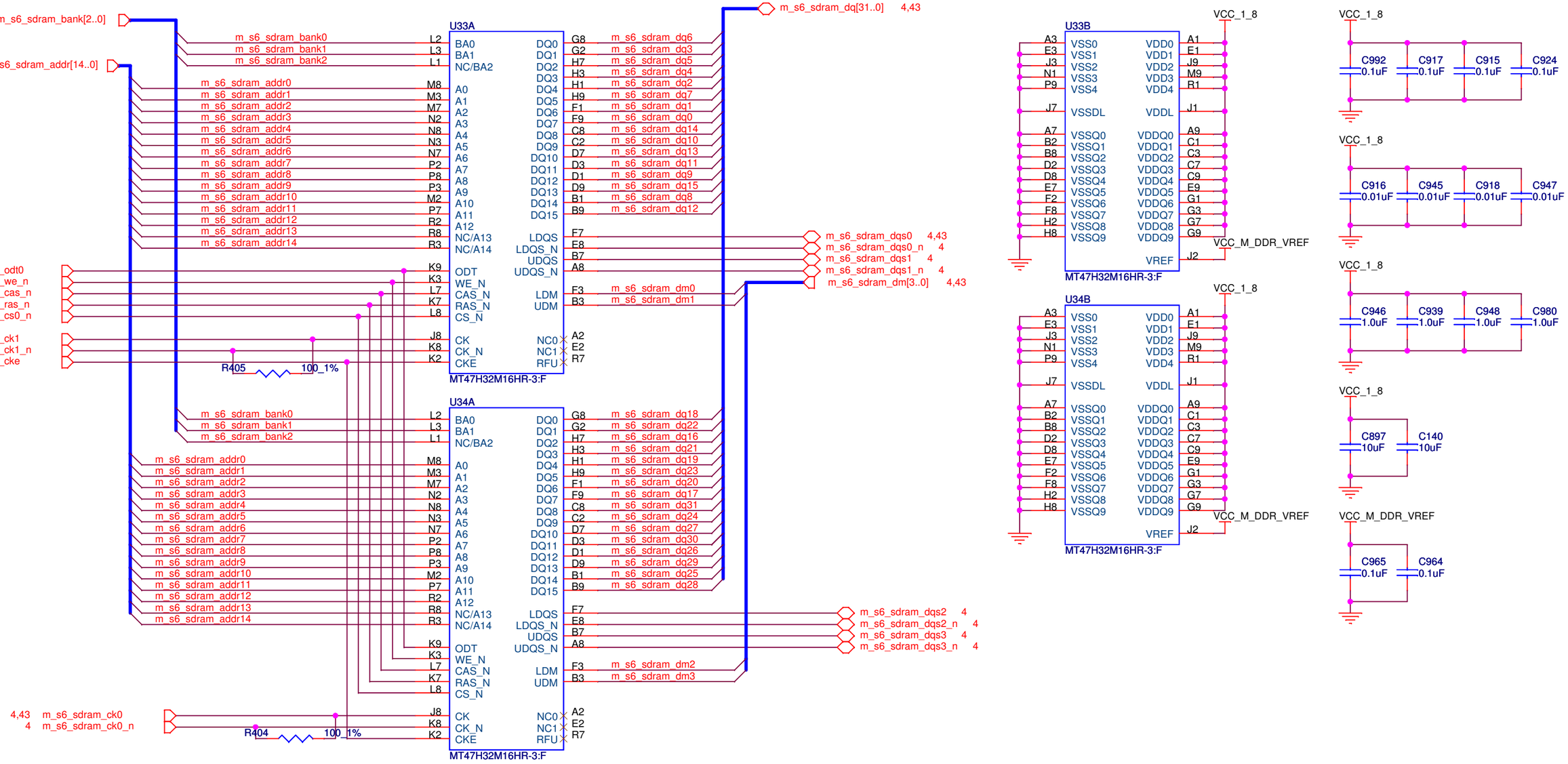
Title: Master S6 (Power, Part 2)

Size	Document Number	BOM Variant	Internal Version	Rev
B	110-10027	NVP	N/A	5A

Date: Tuesday, January 27, 2009 Sheet 10 of 48



Place termination resistors close to ICs

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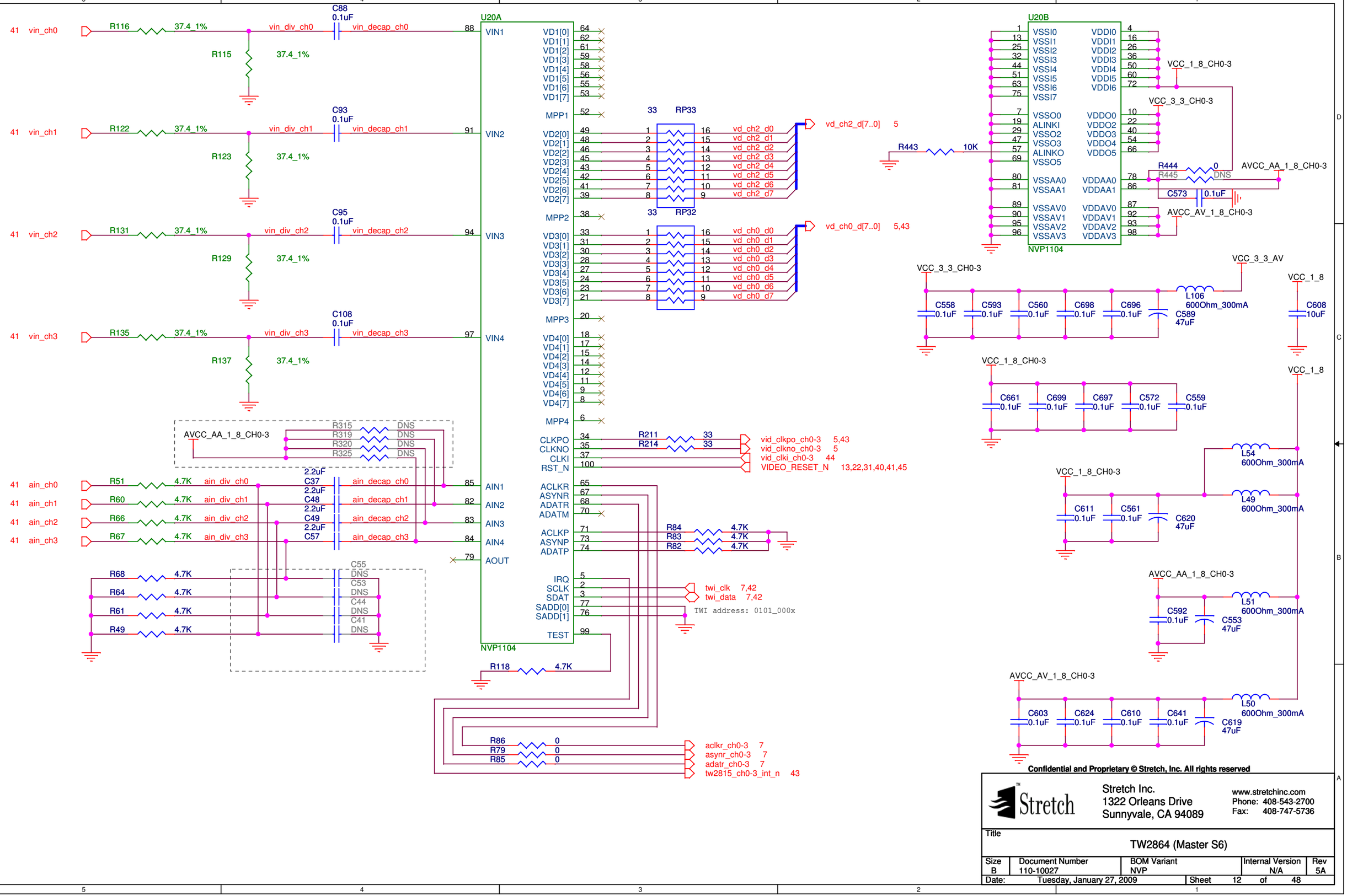
Title: DDR ICs (Master S6)

Size	Document Number	BOM Variant	Internal Version	Rev
B	110-10027	NVP	N/A	5A

Date: Tuesday, January 27, 2009 Sheet 11 of 48



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Title: TW2864 (Master S6)

Size	Document Number	BOM Variant	Internal Version	Rev
B	110-10027	NVP	N/A	5A

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VOUT_DIG_SEL = 0 = A>B1
VOUT_DIG_SEL = 1 = B2>A (default)

VCC_3_3_AV

C957 0.1uF

R186 470K_1%

R187 121K_1%

41 VIDEO_MUX_OUT

33,35 VOUT_DIG_SEL

U54

5 VCC
3 B1
1 B2
6 S
2 GND
4 A

SN74LVC1G3157DCK

35 VOUT_BUFF_EN

U59

1 VIN
2 GND
3 SAG
6 VS+
5 PD_N
4 VOUT

2R, R, 2R, 2R

ADA4430-1YKSZ-R7

C958 0.1uF

L103 C1046 600Ohm_300mA

2.2uF

VCC_3_3_AV

VCC_3_3_AV

BAT54S D16B

D16A BAT54S

R177 75_1% L21 1.8uH

vid_out 41

J19

1 2

3-647079-2

R89 4.7K

X6 27MHz

C717 8pF C716 8pF

R184 1M

U48

19 RTCI

35 XTALI
34 XTALO
37 XCLK
4 LLC
7 RCV1_VS
8 RCV2_HS
43 TTXRQ
44 TTX
1 RES_1
20 RES_2
22 RES_3
23 RES_4
26 RES_5
29 RES_6
21 SA
41 SCL
42 SDA
40 RES_N

30 CVBS
Y
C
27 R178 75_1%
24 R179 75_1%

C24 6.8pF

R180 4.7_1%

FB8 4.7uH

C25 120pF

R183 C26 120pF

75_1%

33 SAA7121_clk_out

R15 33

33 s2_s6_dp3_clk

33 VOUT_DIG[7..0]

VOUT_DIG0 16 MP0
VOUT_DIG1 15 MP1
VOUT_DIG2 14 MP2
VOUT_DIG3 13 MP3
VOUT_DIG4 12 MP4
VOUT_DIG5 11 MP5
VOUT_DIG6 10 MP6
VOUT_DIG7 9 MP7

VDDA_1 25
VDDA_2 28
VDDA_3 31
VDDA_4 36

VSSA_1 32
VSSA_2 33

VDDD_1 6
VDDD_2 17
VDDD_3 39

VSSD_1 5
VSSD_2 18
VSSD_3 38

SP 2
AP 3

SAA7121H

35,40 s2_s6_twi_clk
35,40 s2_s6_twi_data

12,22,31,40,41,45 VIDEO_RESET_N

R52 R88 4.7K 4.7K

C970 0.1uF C971 0.1uF C975 0.1uF C976 0.1uF C1038 2.2uF

C959 0.1uF C967 0.1uF C969 0.1uF C1039 2.2uF

L104 600Ohm_300mA

L105 600Ohm_300mA

VCC_3_3_AV

C938 10uF C921 10uF

VCC_1_8

C930 0.1uF C966 0.1uF C940 0.1uF C952 0.1uF

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Title: Video Out (Part 1)

Size	Document Number	BOM Variant	Internal Version	Rev
B	110-10027	NVP	N/A	5A

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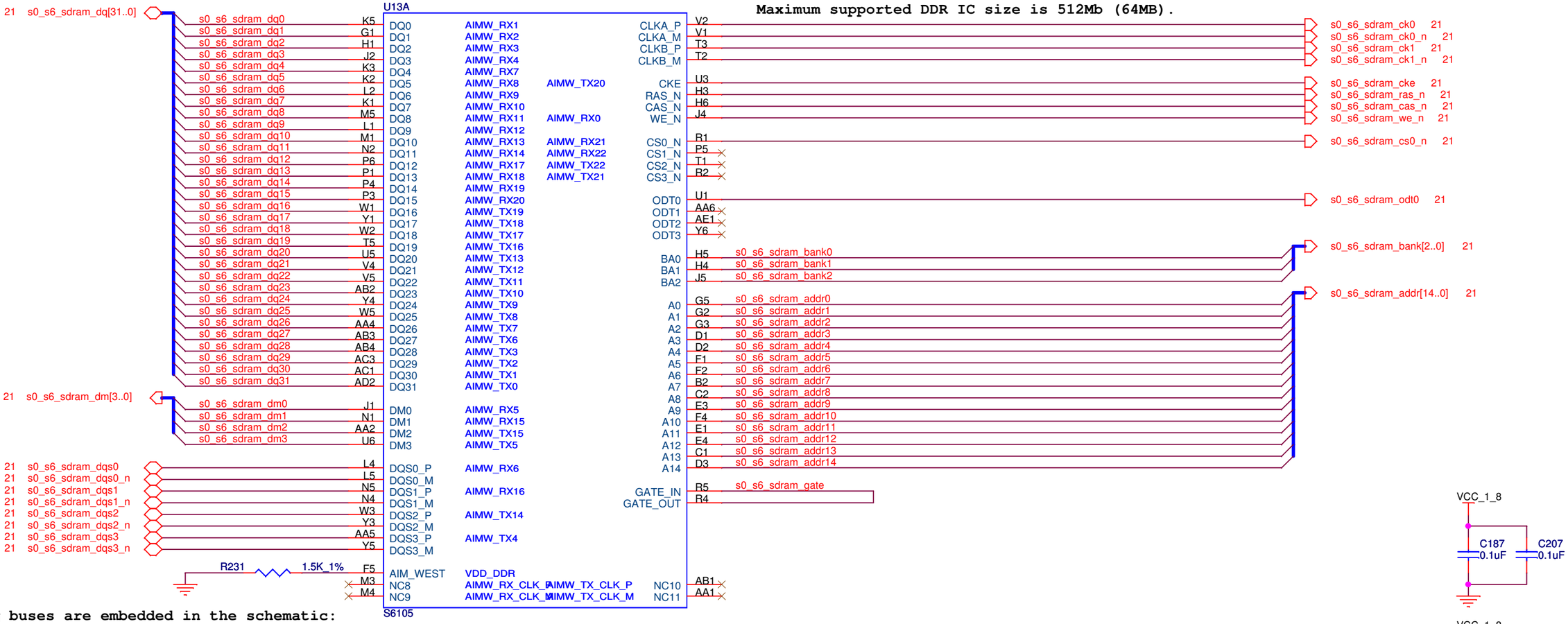

Maximum supported DDR IC size is 512Mb (64MB).

The following buses are embedded in the schematic:
S0_S6_DDR_DATA
->contains all the sdram_dq, sdam_dm, sdram_dqs, and sdram_dqs_n signals
S0_S6_DDR_CLK
->contains the sdram_ck and sdram_gate signals
S0_S6_DDR_ADDR
->contains the sdram_cke, sdram_ras_n, sdram_cas_n, sdram_we_n, sdram_cs0_n, sdram_bank, and sdram_addr signals

The following differential pairs are embedded in the schematic:
S0_S6_DDR_DQS0
S0_S6_DDR_DQS1
S0_S6_DDR_DQS2
S0_S6_DDR_DQS3
S0_S6_DDR_CK0
S0_S6_DDR_CK1

ROUTING RULES (S6100 package legths should be taken into consideration when determining the trace lengths):
1) Differential pairs should be matched to within +/- 5ps (25mil) .
2) The DDR_ADDR bus and clocks should be matched to within +/- 75ps (375mil).
3) The DDR_DATA bus should be matched to within +/- 50ps (250mil).
4) The signals in a byte lane should be matched to within +/- 30ps (150mil) and be routed on the same layer.
5) The clocks and dqs signals should be matched to within +/- 100ps (500mil).
6) s0_s6_sdram_gate signal should be as short as possible and accesible using a via.

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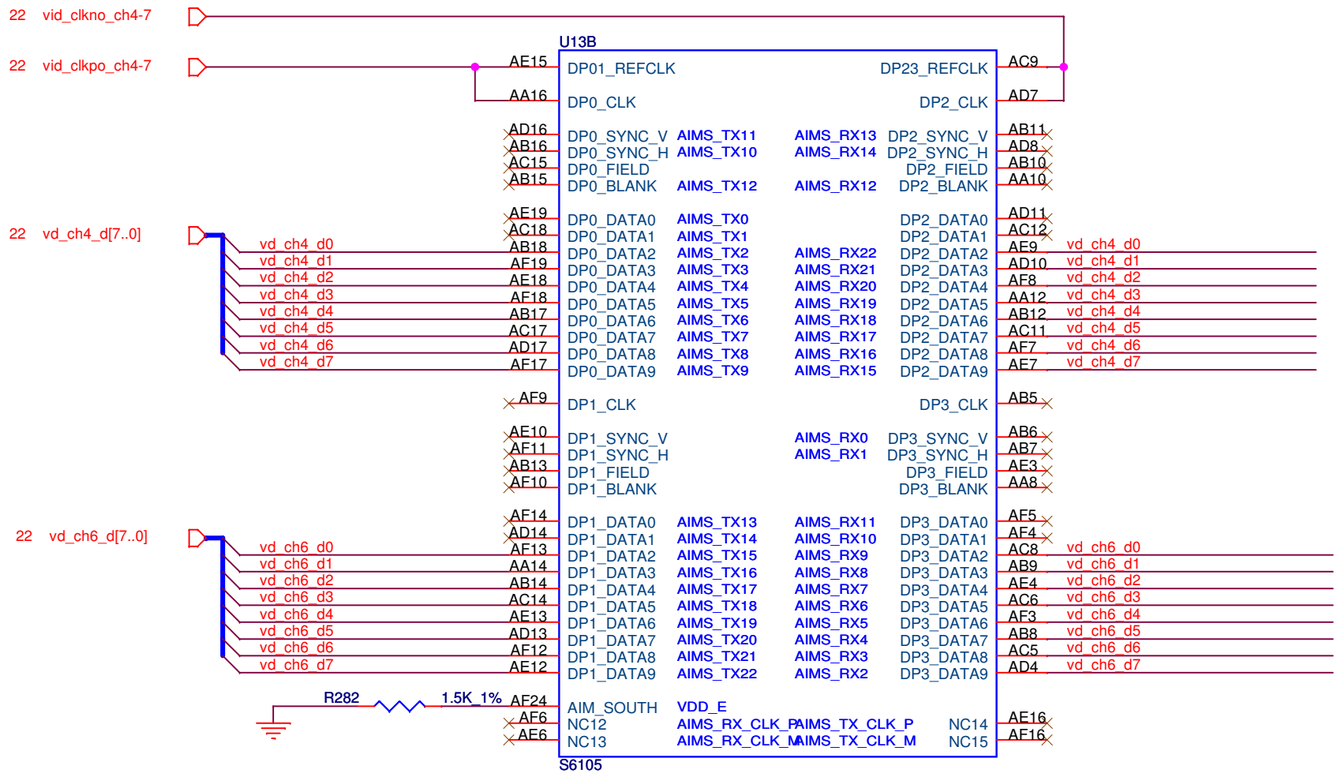
Title: Secondary 0 S6 (DDR Interface)

Size	Document Number	BOM Variant	Internal Version	Rev
B	110-10027	NVP	N/A	5A

Date: Tuesday, January 27, 2009 Sheet 14 of 48

dp0_clk_ref and dp2_clk_ref need to be driven for reset initialization.



DP 0-3 ARE POWERED FROM 2.5V

The following buses are embedded in the schematic:
VD_CH4
->contains all the vd_ch4 signals
VD_CH6
->contains all the vd_ch6 signals

ROUTING RULES (S6100 package legths should be taken into consideration when determining the trace lengths):
The VD_CH4, VD_CH6 buses, vid_clkpo_ch4-7, and vid_clkno_ch4-7 should be matched to within +/- 250ps (1250mil).

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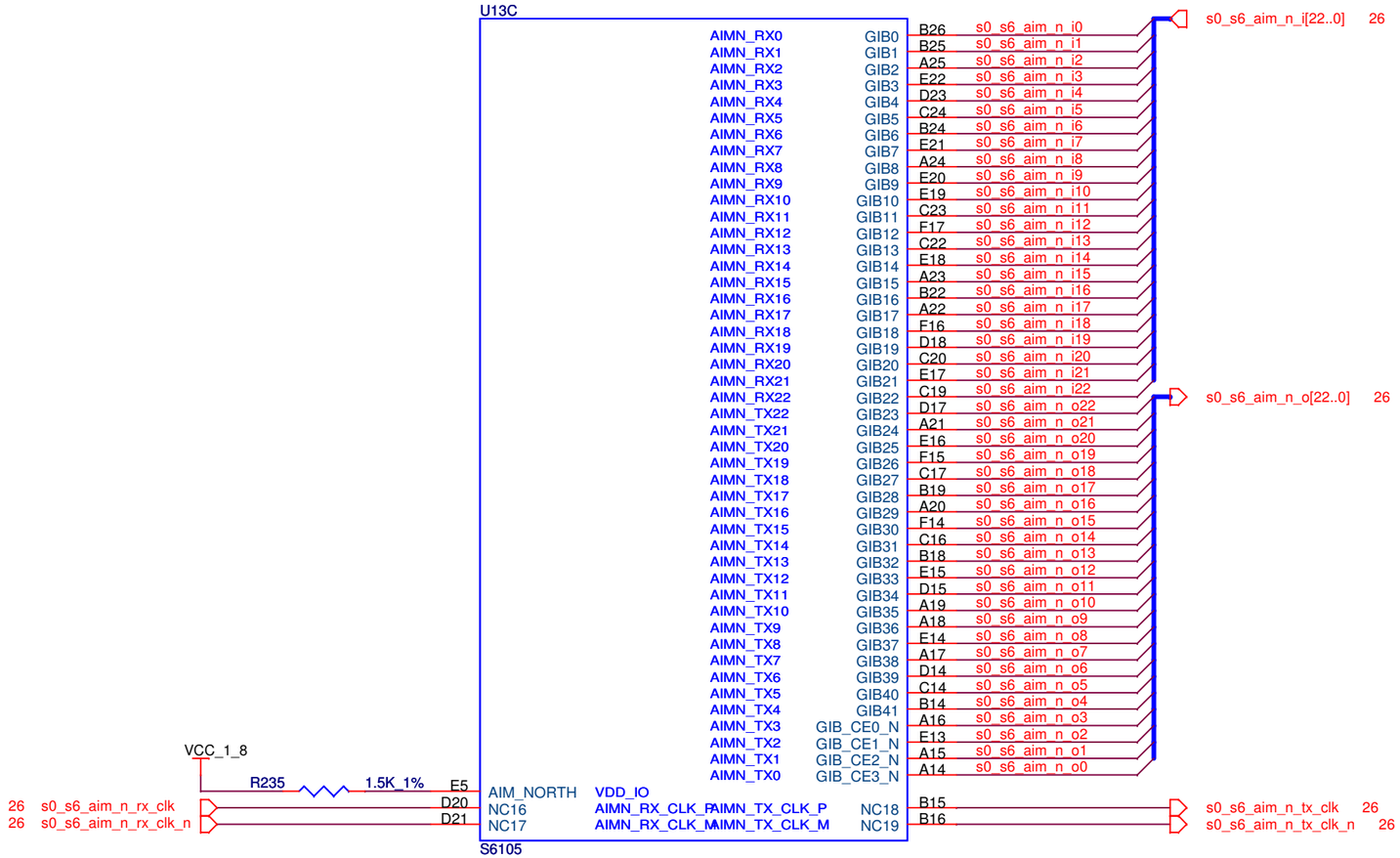
Title: Secondary 0 S6 (Data Port Interface)

Size	Document Number	BOM Variant	Internal Version	Rev
B	110-10027	NVP	N/A	5A

Date: Tuesday, January 27, 2009 Sheet 15 of 48



AIM_NORTH = 1.8V

The following buses are embedded in the schematic:
S0_S6_AIM_N_O
->contains the aim_n_o, aim_n_tx_clk and aim_n_tx_clk_n signals
S0_S6_AIM_N_I
->contains the aim_n_i, aim_n_rx_clk and aim_n_rx_clk_n signals

The following differential pairs are embedded in the schematic:
S0_S6_AIM_N_RX_CLK
S0_S6_AIM_N_TX_CLK

ROUTING RULES (S6100 package legths should be taken into consideration when determining the trace lengths):
1) Differential pairs should be matched to within +/- 5ps (25mil).
2) The S0_S6_AIM_N_O bus should be matched to within +/- 50ps (250mil).
3) The S0_S6_AIM_N_I bus should be matched to within +/- 50ps (250mil).

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Title: Secondary 0 S6 (AIM North Interface)

Size	Document Number	BOM Variant	Internal Version	Rev
B	110-10027	NVP	N/A	5A

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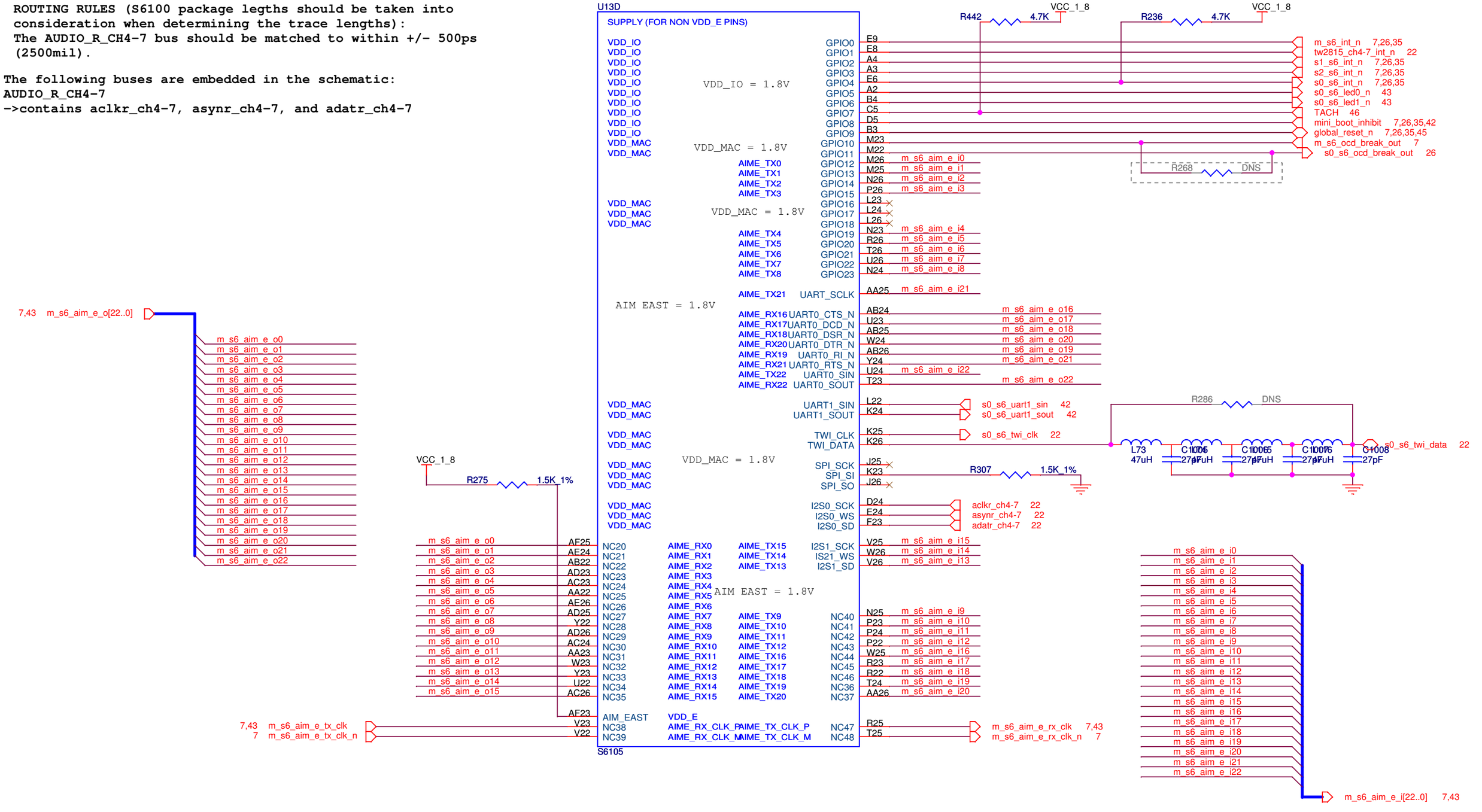
ROUTING RULES (S6100 package legths should be taken into consideration when determining the trace lengths):
The AUDIO_R_CH4-7 bus should be matched to within +/- 500ps (2500mil).

The following buses are embedded in the schematic:
AUDIO_R_CH4-7
->contains aclkr_ch4-7, asynr_ch4-7, and adatr_ch4-7



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Size	Document Number	BOM Variant	Internal Version	Rev
B	110-10027	NVP	N/A	5A

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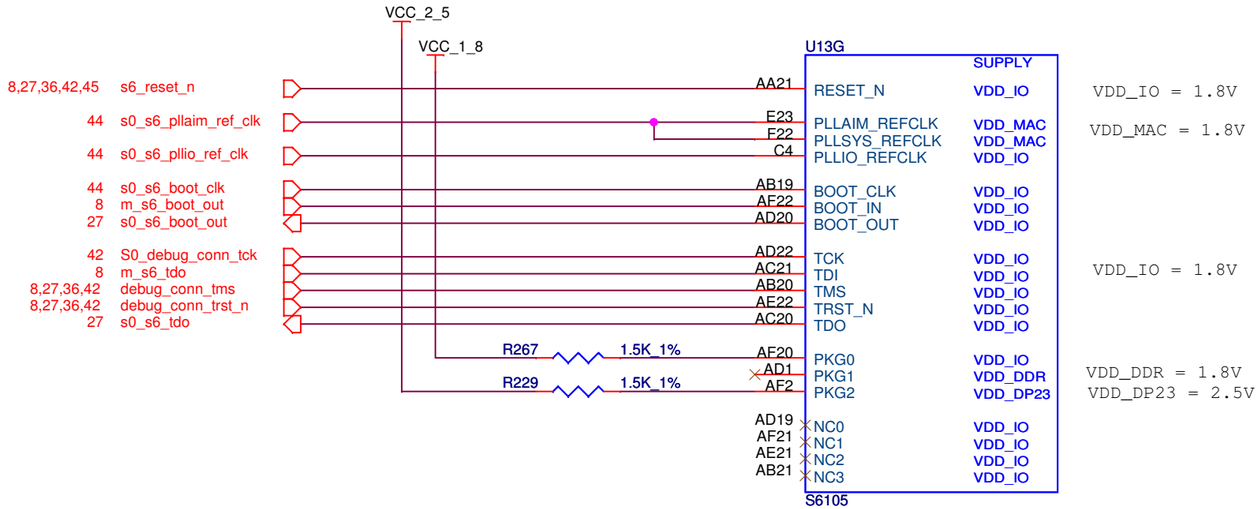

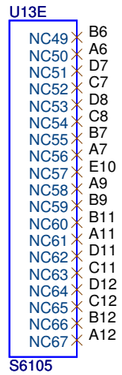

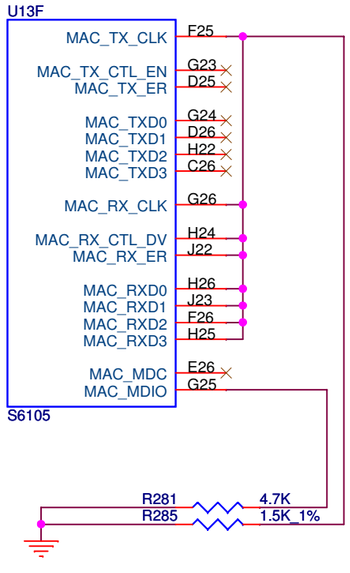

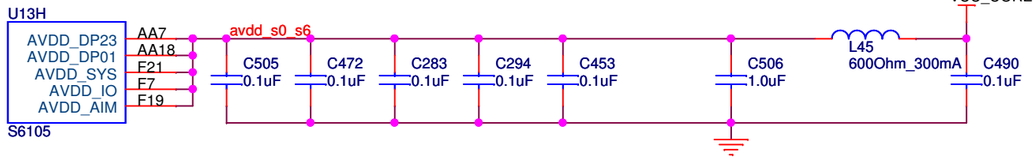

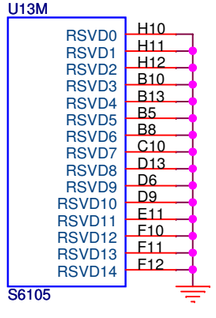

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Title: Secondary 0 S6 (Miscellaneous Interfaces)

Size	Document Number	BOM Variant	Internal Version	Rev
B	110-10027	NVP	N/A	5A

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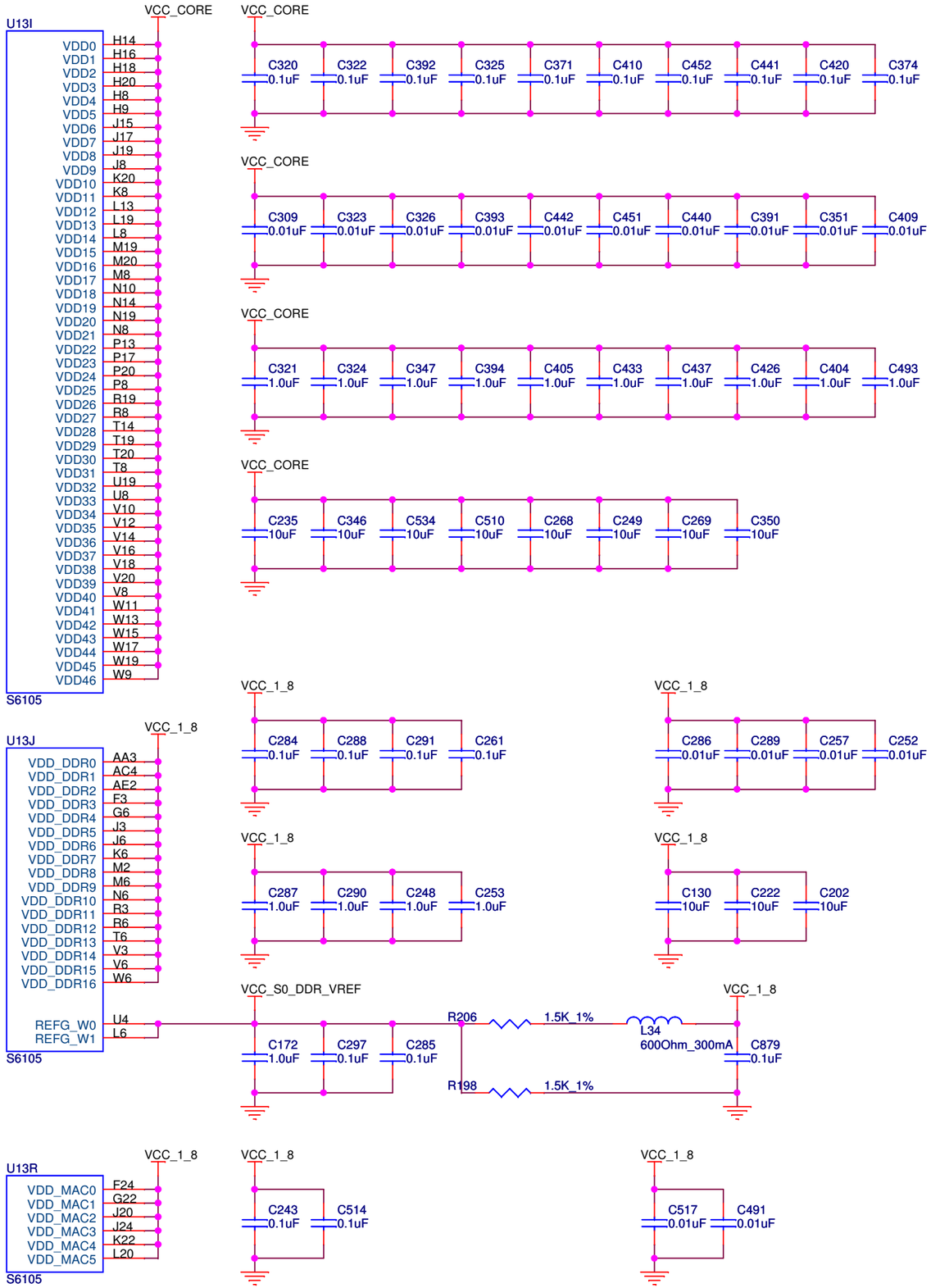

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Title: Secondary 0 S6 (Power, Part 1)

Size	Document Number	BOM Variant	Internal Version	Rev
B	110-10027	NVP	N/A	5A

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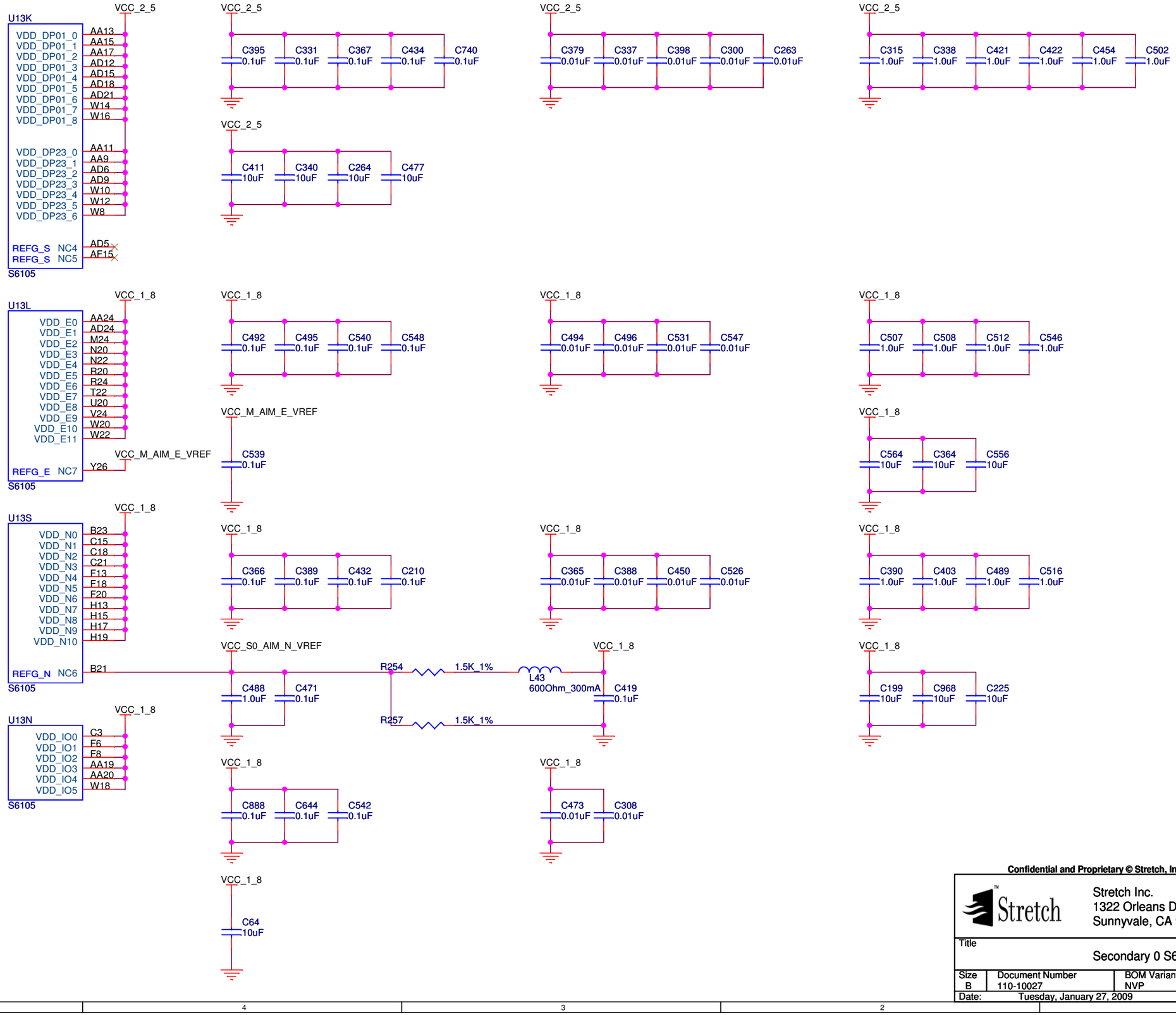

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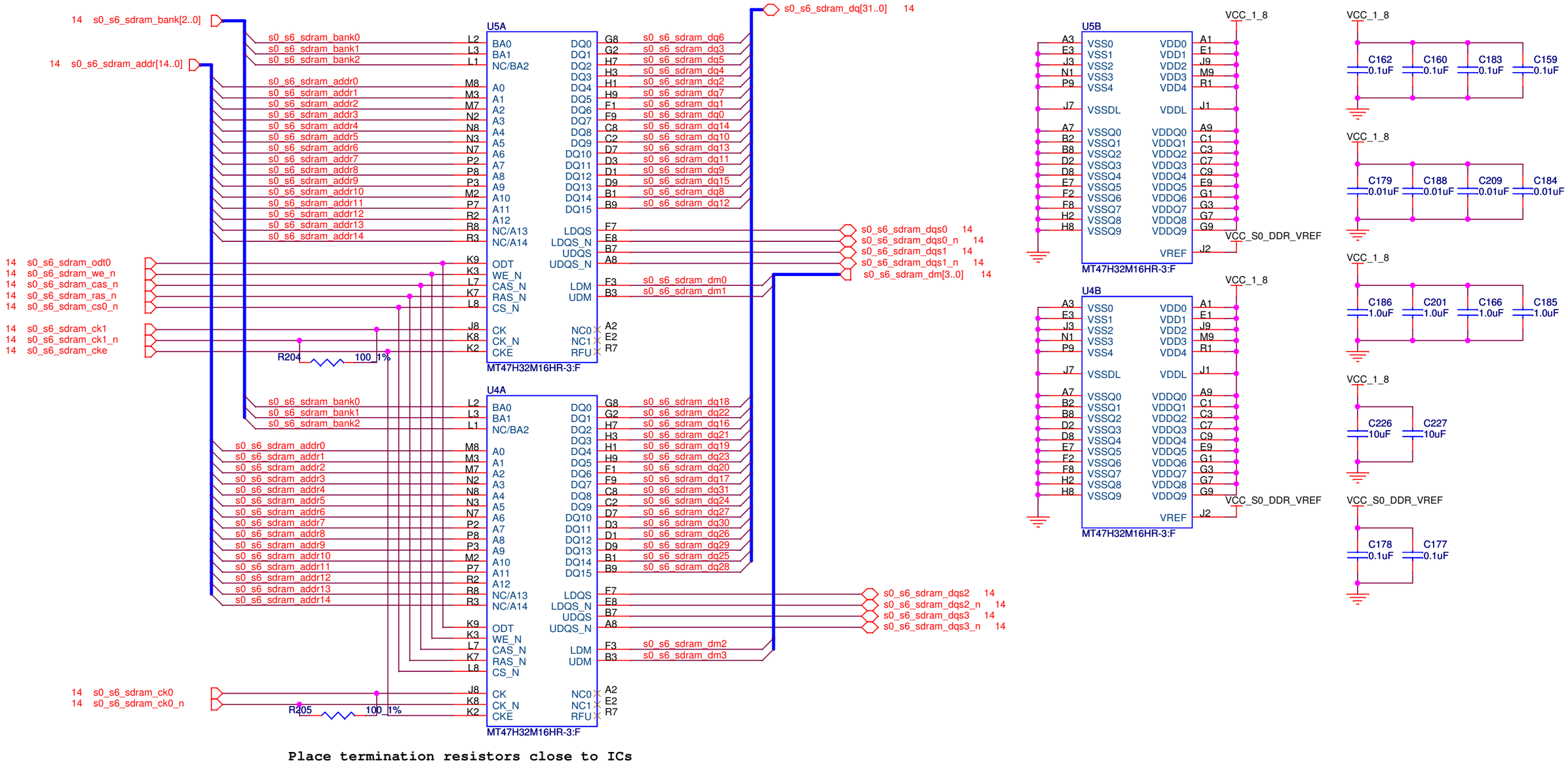
Title: Secondary 0 S6 (Power, Part 2)

Size	Document Number	BOM Variant	Internal Version	Rev
B	110-10027	NVP	N/A	5A

Date: Tuesday, January 27, 2009 Sheet 20 of 48



Place termination resistors close to ICs

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Title				
DDR ICs (Secondary 0 S6)				
Size: B	Document Number: 110-10027	BOM Variant: NVP	Internal Version: N/A	Rev: 5A
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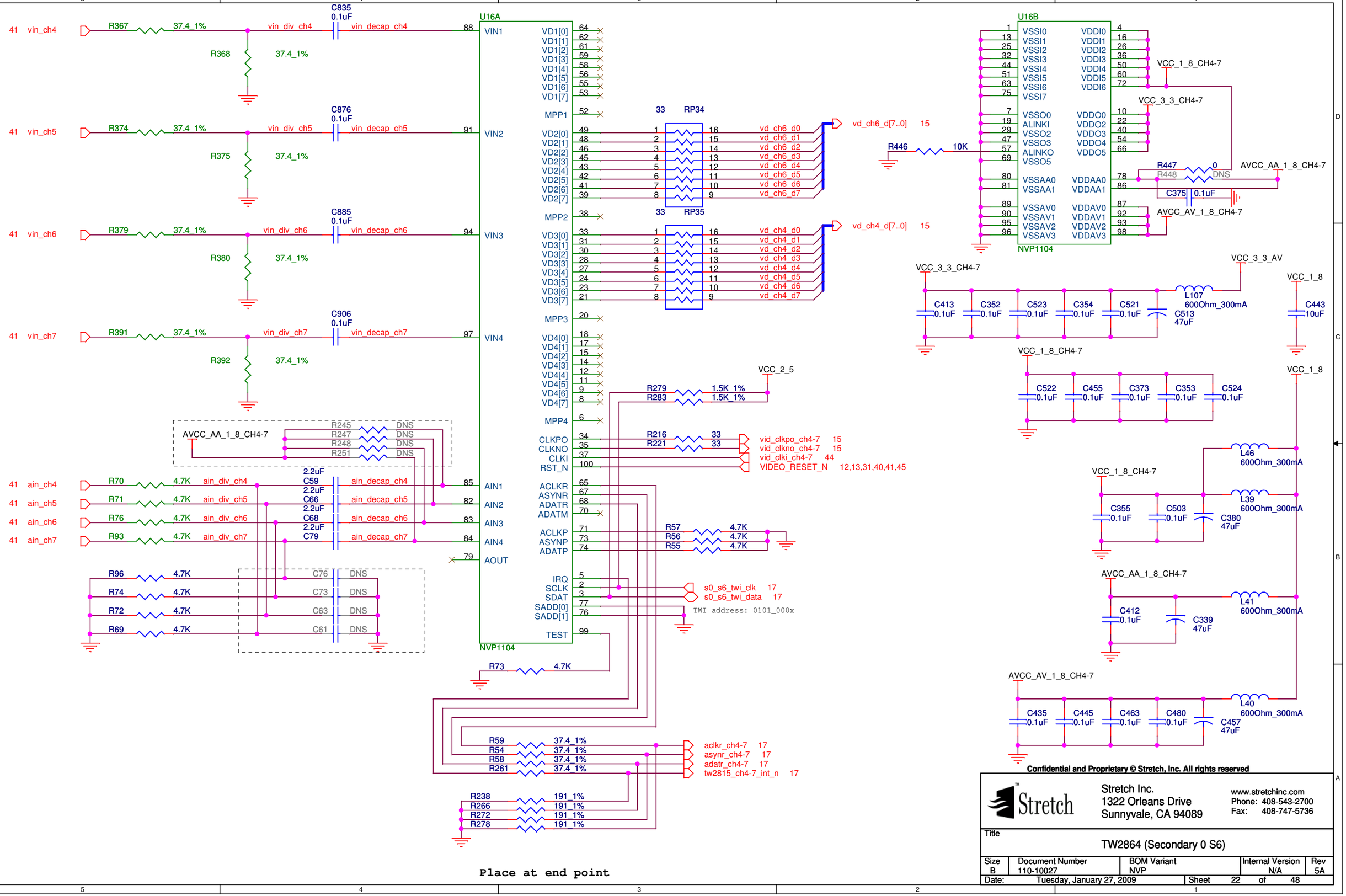

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Title: TW2864 (Secondary 0 S6)

Size	Document Number	BOM Variant	Internal Version	Rev
B	110-10027	NVP	N/A	5A

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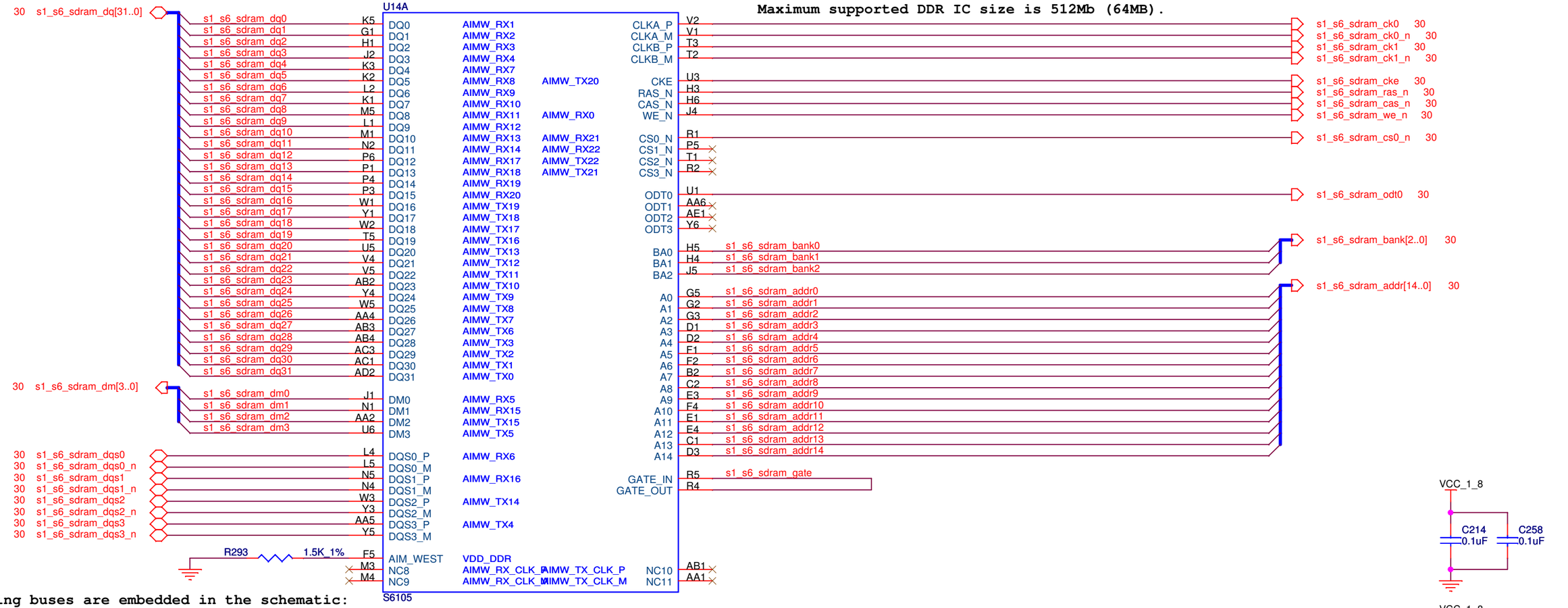

The following buses are embedded in the schematic:
S1_S6_DDR_DATA
->contains all the sdram_dq, sdam_dm, sdram_dqs, and sdram_dqs_n signals
S1_S6_DDR_CLK
->contains the sdram_ck and sdram_gate signals
S1_S6_DDR_ADDR
->contains the sdram_cke, sdram_ras_n, sdram_cas_n, sdram_we_n, sdram_cs0_n,
sdram_bank, and sdram_addr signals

The following differential pairs are embedded in the schematic:
S1_S6_DDR_DQS0
S1_S6_DDR_DQS1
S1_S6_DDR_DQS2
S1_S6_DDR_DQS3
S1_S6_DDR_CK0
S1_S6_DDR_CK1

ROUTING RULES (S6100 package legths should be taken into consideration when determining the trace lengths):
1) Differential pairs should be matched to within +/- 5ps (25mil) .
2) The DDR_ADDR bus and clocks should be matched to within +/- 75ps (375mil).
3) The DDR_DATA bus should be matched to within +/- 50ps (250mil).
4) The signals in a byte lane should be matched to within +/- 30ps (150mil) and be routed on the same layer.
5) The clocks and dqs signals should be matched to within +/- 100ps (500mil).
6) s1_s6_sdram_gate signal should be as short as possible and accesible using a via.

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Title				
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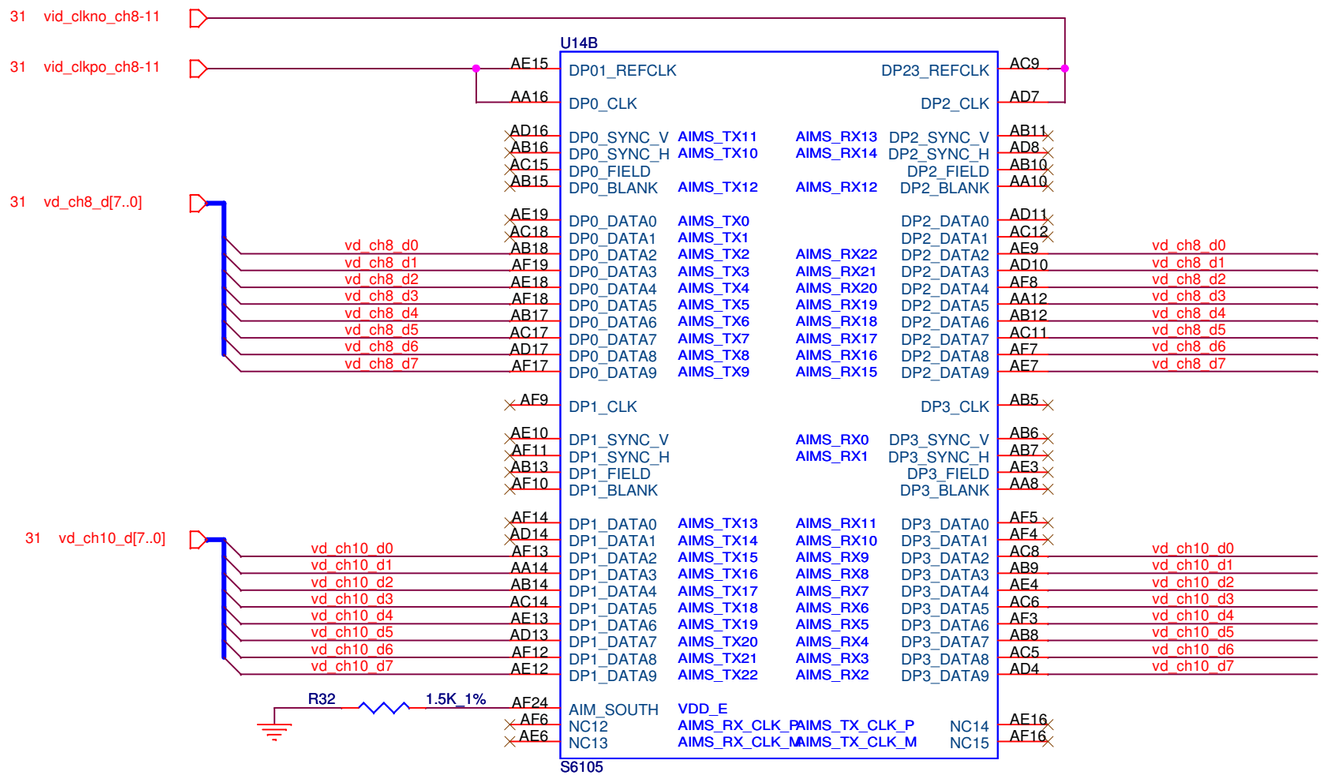
Size: B	Document Number: 110-10027	BOM Variant: NVP	Internal Version: N/A	Rev: 5A
Date: Tuesday, January 27, 2009	Sheet 23 of 48			

dp0_clk_ref and dp2_clk_ref need to be driven for reset initialization.



DP0-3 ARE POWERED FROM 2.5V

The following buses are embedded in the schematic:
VD_CH8
->contains all the vd_ch8 signals
VD_CH10
->contains all the vd_ch10 signals

ROUTING RULES (S6100 package legths should be taken into consideration when determining the trace lengths):
The VD_CH8, VD_CH10 buses, vid_clkpo_ch8-11, and vid_clkno_ch8-11 should be matched to within +/- 250ps (1250mil).

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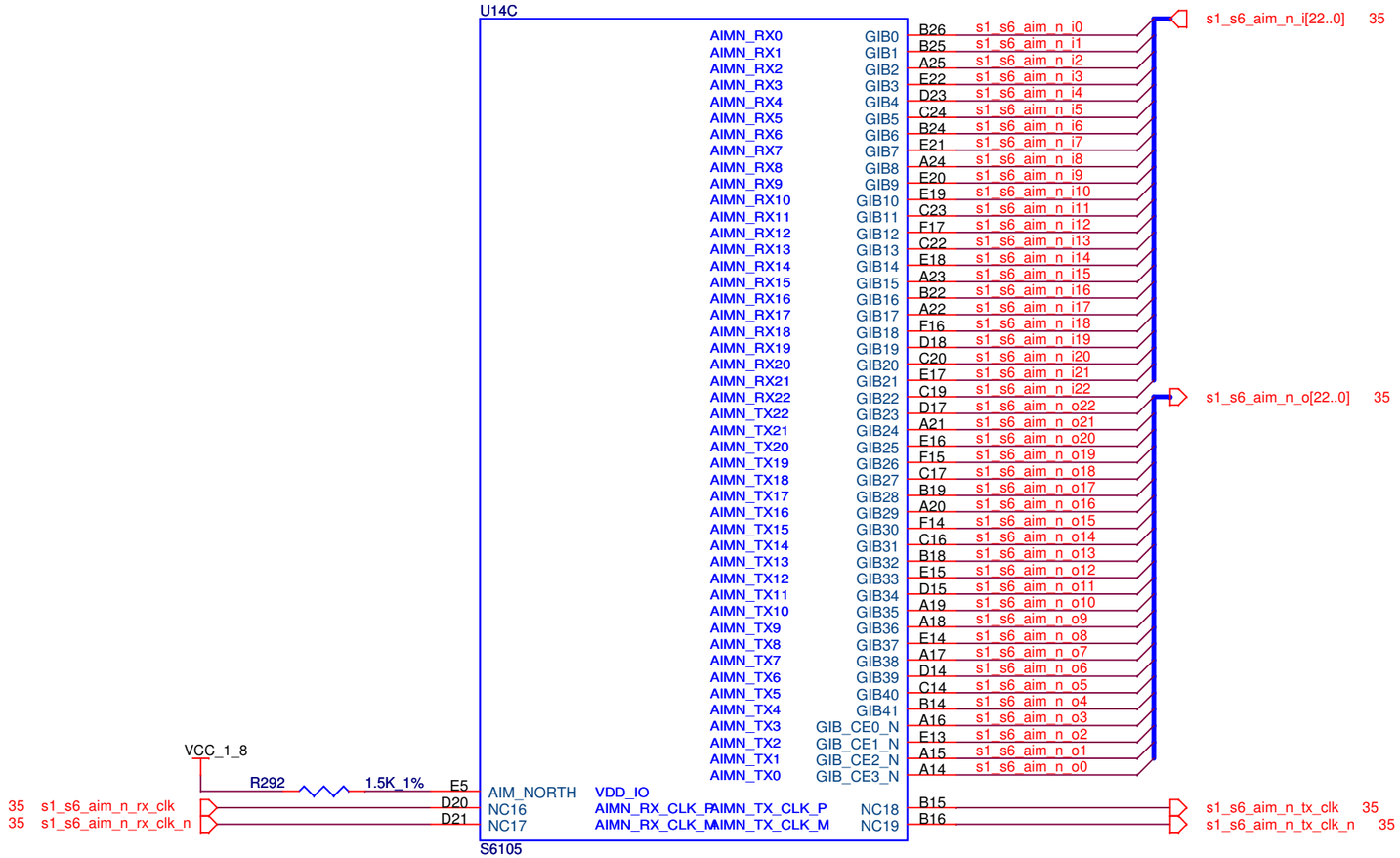
Title				
Secondary 1 S6 (Data Port Interface)				
Size: B	Document Number: 110-10027	BOM Variant: NVP	Internal Version: N/A	Rev: 5A
Date: Tuesday, January 27, 2009		Sheet 24 of 48		



AIM_NORTH = 1.8V

The following buses are embedded in the schematic:
S1_S6_AIM_N_O
->contains the aim_n_o, aim_n_tx_clk and aim_n_tx_clk_n signals
S1_S6_AIM_N_I
->contains the aim_n_i, aim_n_rx_clk and aim_n_rx_clk_n signals

The following differential pairs are embedded in the schematic:
S1_S6_AIM_N_RX_CLK
S1_S6_AIM_N_TX_CLK

ROUTING RULES (S6100 package legths should be taken into consideration when determining the trace lengths):
1) Differential pairs should be matched to within +/- 5ps (25mil).
2) The S1_S6_AIM_N_O bus should be matched to within +/- 50ps (250mil).
3) The S1_S6_AIM_N_I bus should be matched to within +/- 50ps (250mil).

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Title: Secondary 1 S6 (AIM North Interface)

Size	Document Number	BOM Variant	Internal Version	Rev
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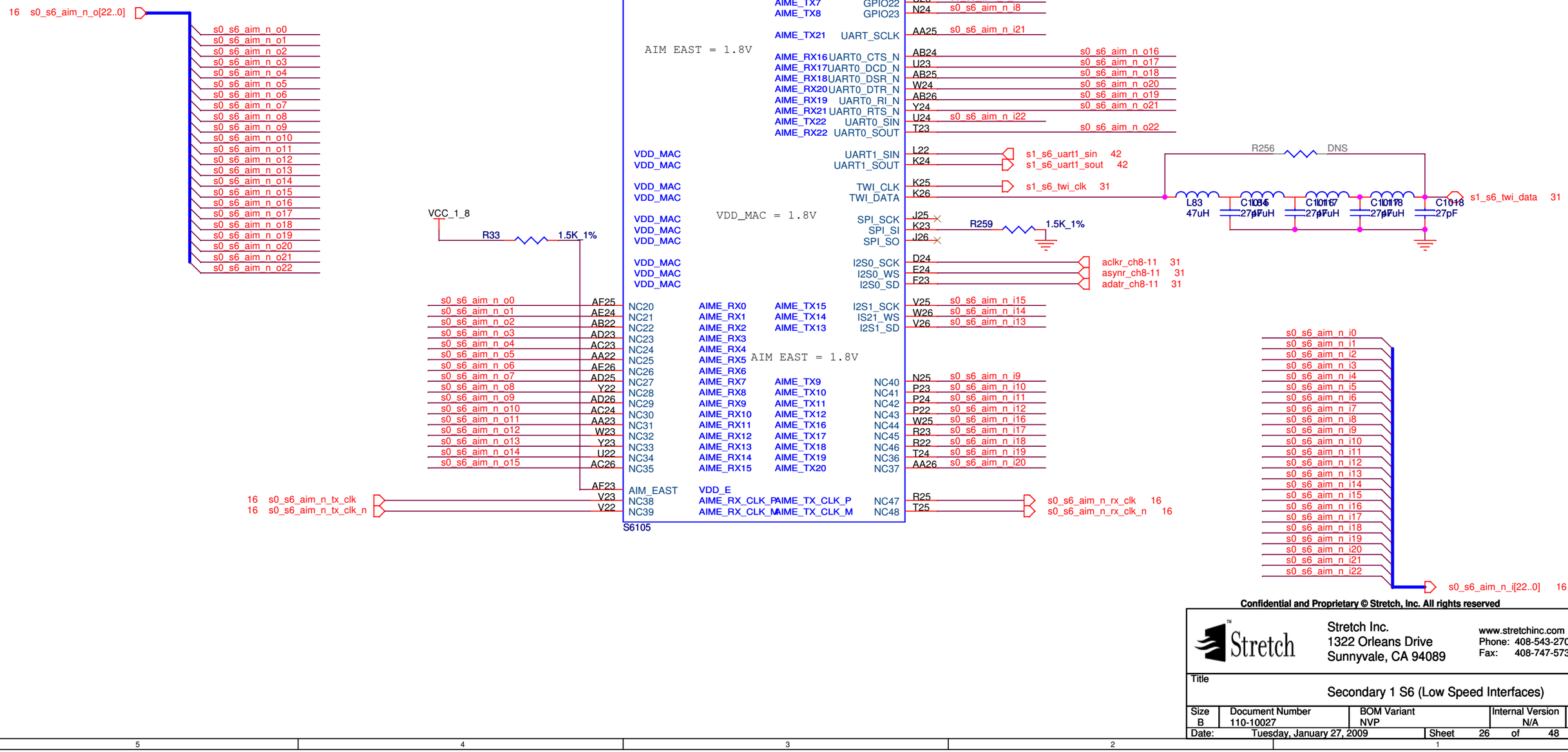
The following buses are embedded in the schematic:
AUDIO_R_CH8-11
->contains aclkr_ch8-11, asynr_ch8-11, and adatr_ch8-11

ROUTING RULES (S6100 package legths should be taken into consideration when determining the trace lengths):
The AUDIO_R_CH8-11 bus should be matched to within +/- 500ps (2500mil).



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Title: Secondary 1 S6 (Low Speed Interfaces)

Size	Document Number	BOM Variant	Internal Version	Rev
B	110-10027	NVP	N/A	5A

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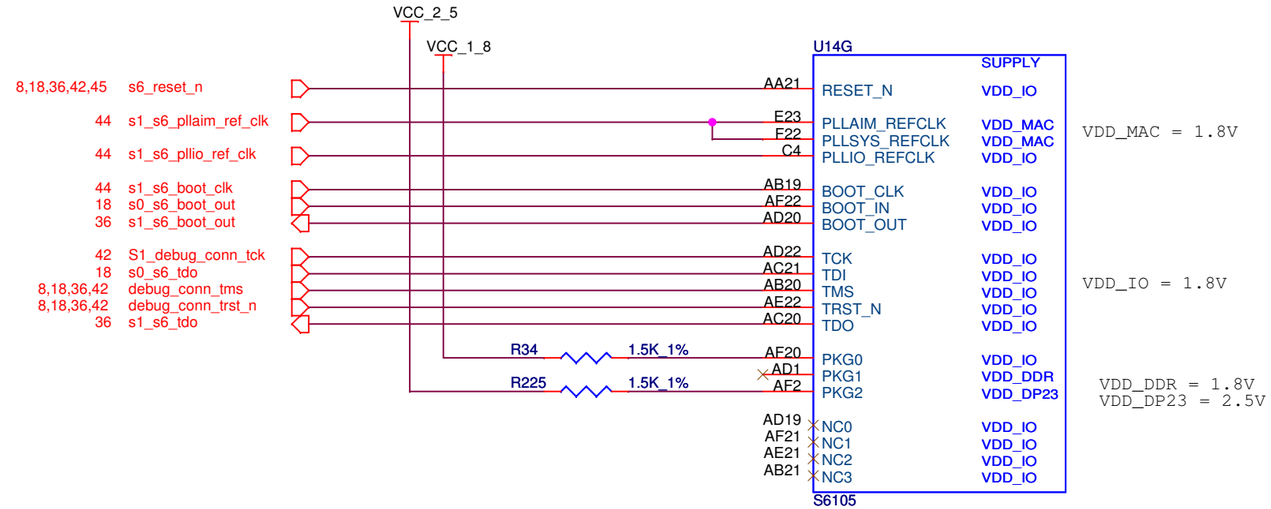

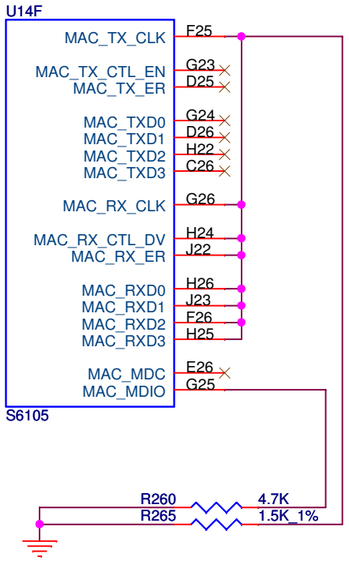

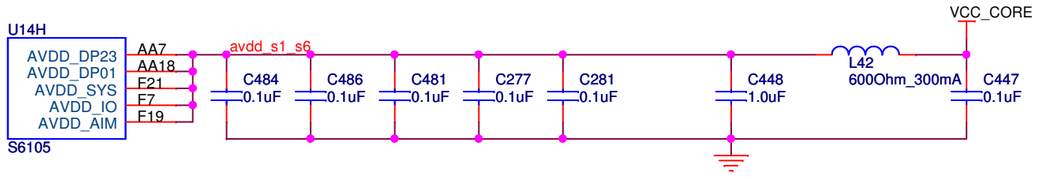

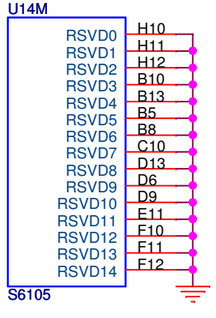

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Title: Secondary 1 S6 (Miscellaneous Interfaces)

Size	Document Number	BOM Variant	Internal Version	Rev
B	110-10027	NVP	N/A	5A

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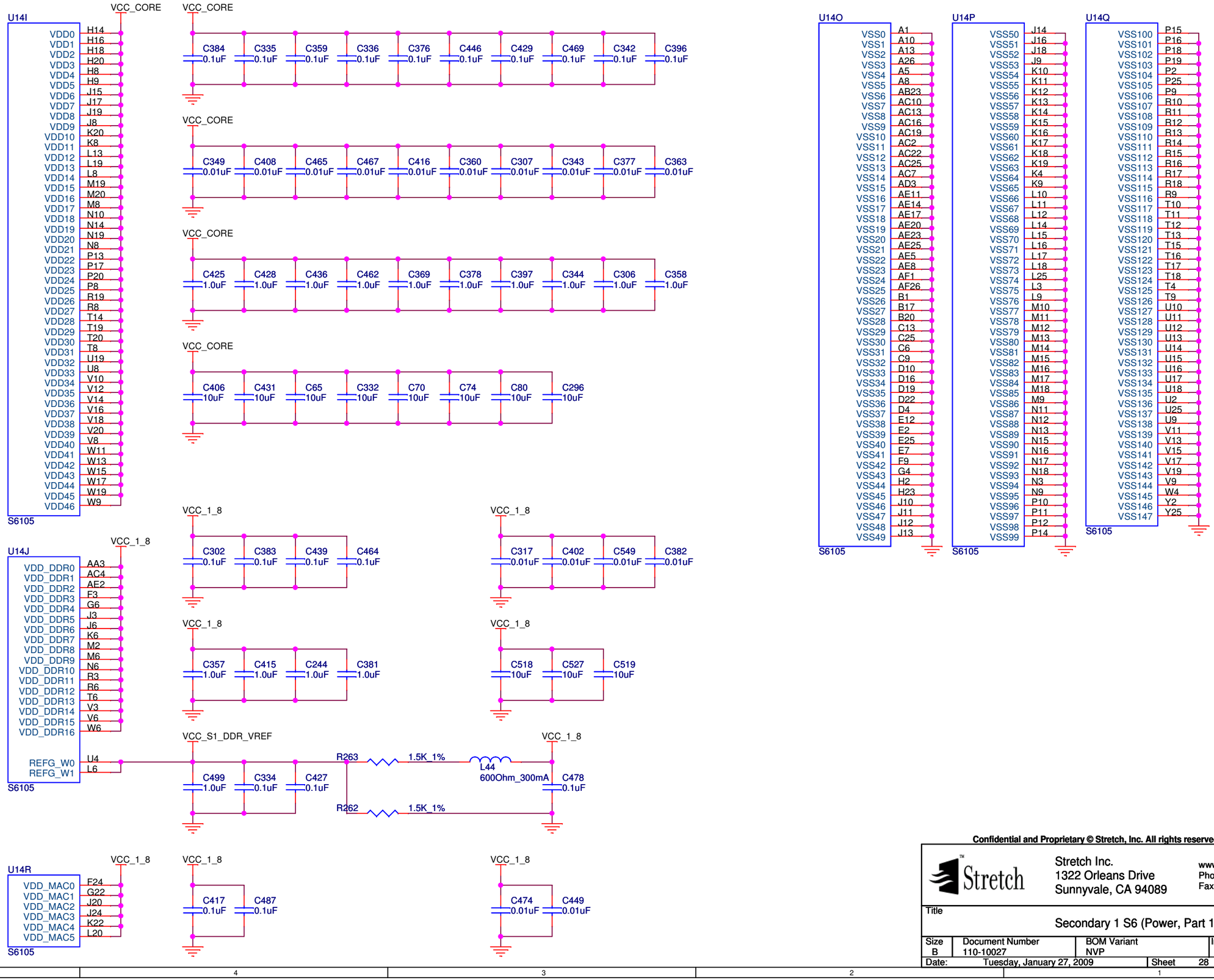

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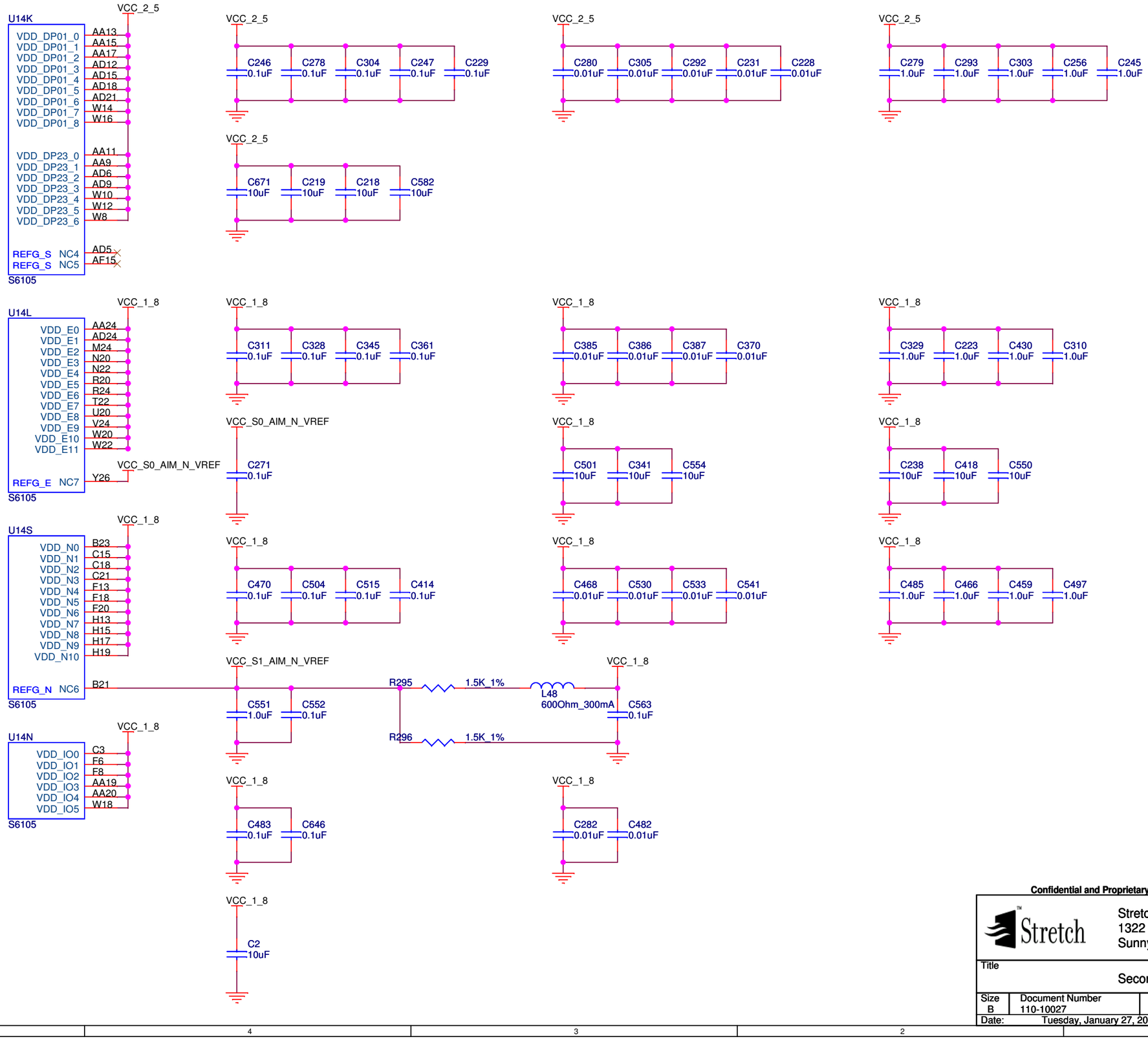
Title: Secondary 1 S6 (Power, Part 1)

Size	Document Number	BOM Variant	Internal Version	Rev
B	110-10027	NVP	N/A	5A

Date: Tuesday, January 27, 2009 Sheet 28 of 48



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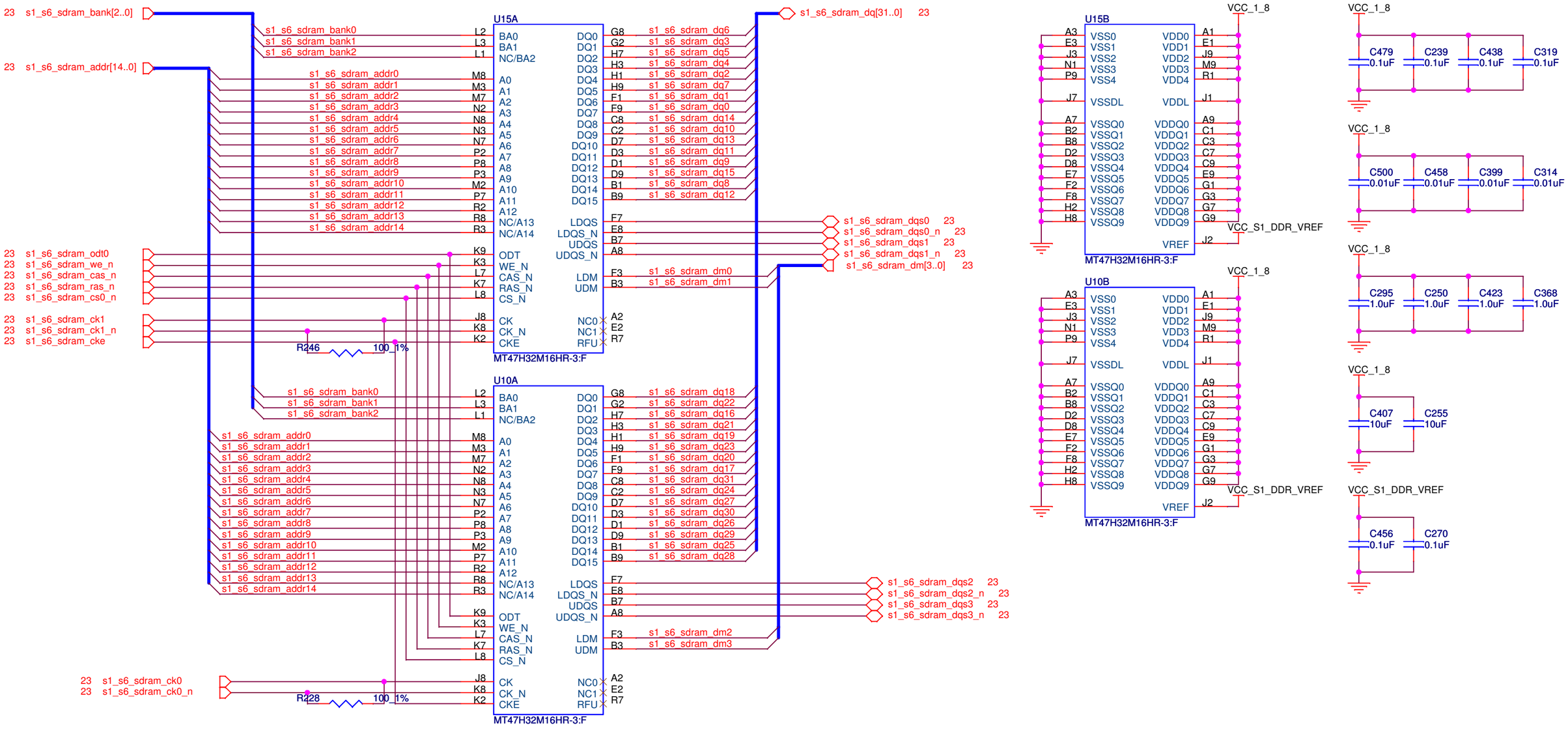
Title: Secondary 1 S6 (Power, Part 2)

Size	Document Number	BOM Variant	Internal Version	Rev
B	110-10027	NVP	N/A	5A

Date: Tuesday, January 27, 2009 Sheet 29 of 48



Place termination resistors close to ICs

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Title				
DDR ICs (Secondary 1 S6)				
Size: B	Document Number: 110-10027	BOM Variant: NVP	Internal Version: N/A	Rev: 5A
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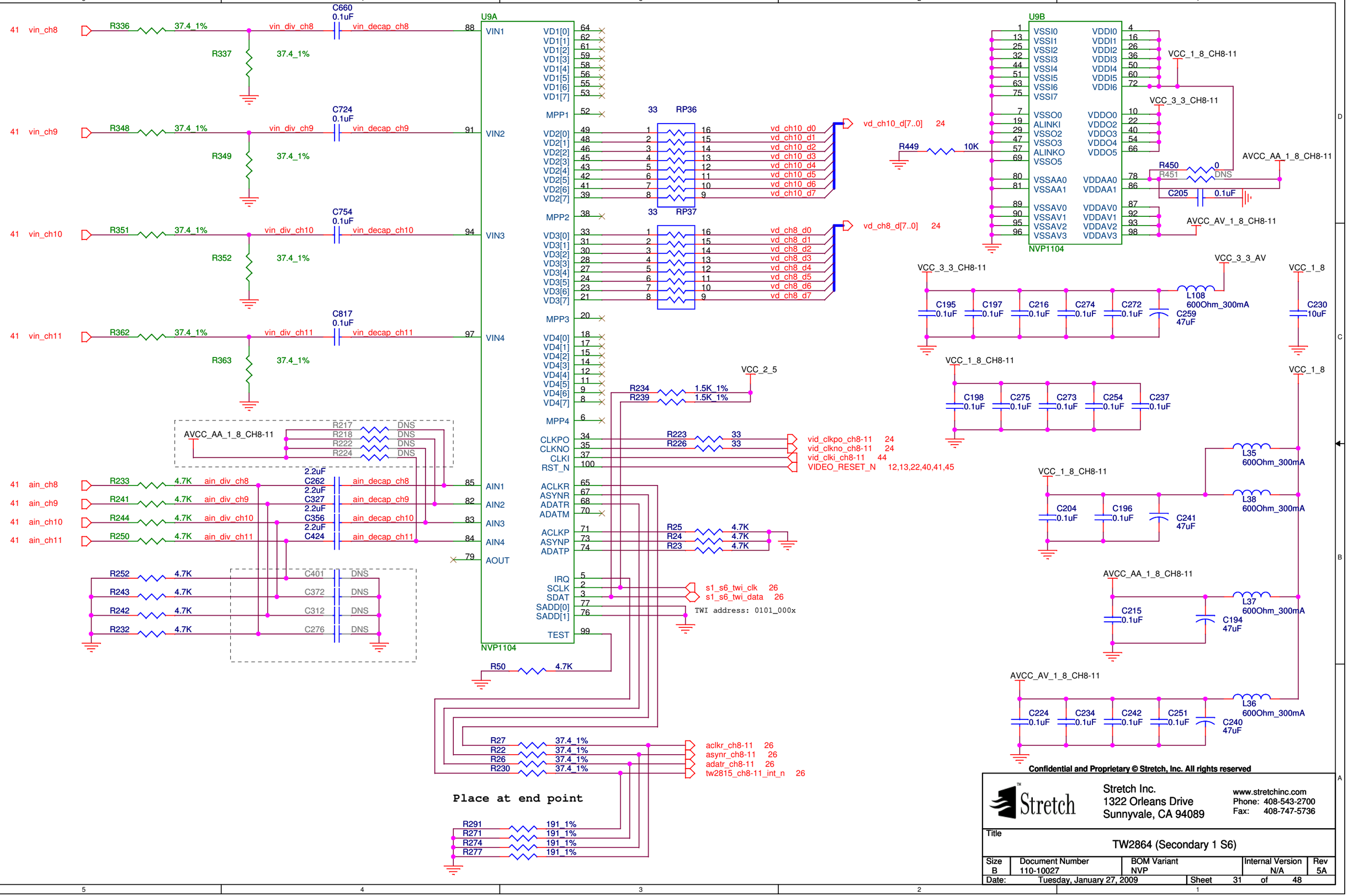

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Title: TW2864 (Secondary 1 S6)

Size	Document Number	BOM Variant	Internal Version	Rev
B	110-10027	NVP	N/A	5A

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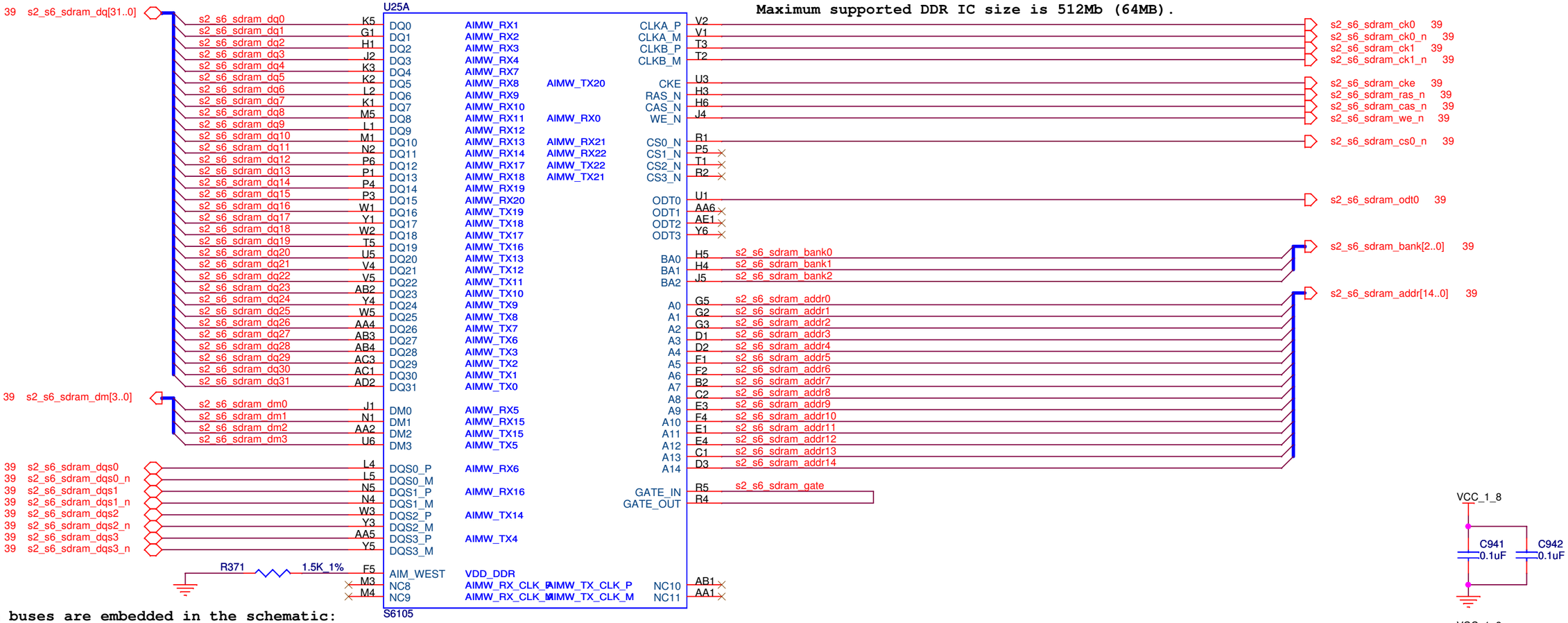

The following buses are embedded in the schematic:
S2_S6_DDR_DATA
->contains all the sdram_dq, sdam_dm, sdram_dqs, and sdram_dqs_n signals
S2_S6_DDR_CLK
->contains the sdram_ck and sdram_gate signals
S2_S6_DDR_ADDR
->contains the sdram_cke, sdram_ras_n, sdram_cas_n, sdram_we_n, sdram_cs0_n, sdram_bank, and sdram_addr signals

The following differential pairs are embedded in the schematic:
S2_S6_DDR_DQS0
S2_S6_DDR_DQS1
S2_S6_DDR_DQS2
S2_S6_DDR_DQS3
S2_S6_DDR_CK0
S2_S6_DDR_CK1

ROUTING RULES (S6100 package legths should be taken into consideration when determining the trace lengths):
1) Differential pairs should be matched to within +/- 5ps (25mil) .
2) The DDR_ADDR bus and clocks should be matched to within +/- 75ps (375mil).
3) The DDR_DATA bus should be matched to within +/- 50ps (250mil).
4) The signals in a byte lane should be matched to within +/- 30ps (150mil) and be routed on the same layer.
5) The clocks and dqs signals should be matched to within +/- 100ps (500mil).
6) s2_s6_sdram_gate signal should be as short as possible and accesible using a via.

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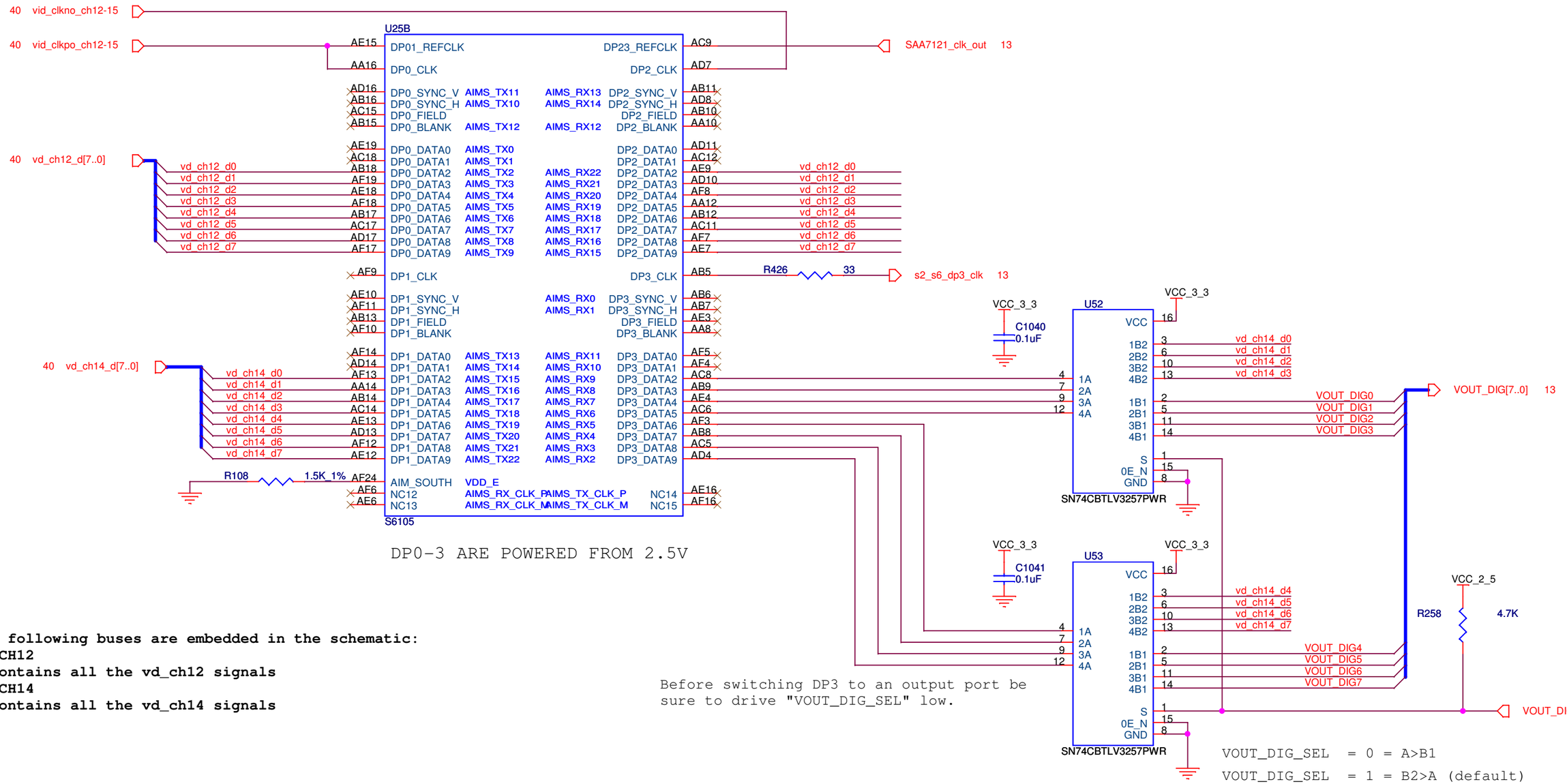
Title: Secondary 2 S6 (DDR Interface)

Size	Document Number	BOM Variant	Internal Version	Rev
B	110-10027	NVP	N/A	5A

Date: Tuesday, January 27, 2009 Sheet 32 of 48

dp0_clk_ref and dp2_clk_ref need to be driven for reset initialization.



The following buses are embedded in the schematic:
VD_CH12
->contains all the vd_ch12 signals
VD_CH14
->contains all the vd_ch14 signals

ROUTING RULES (S6100 package legths should be taken into consideration when determining the trace lengths):
The VD_CH12, VD_CH14, buses, vid_clkpo_ch12-15, and vid_clkno_ch12-15 should be matched to within +/- 250ps (1250mil).

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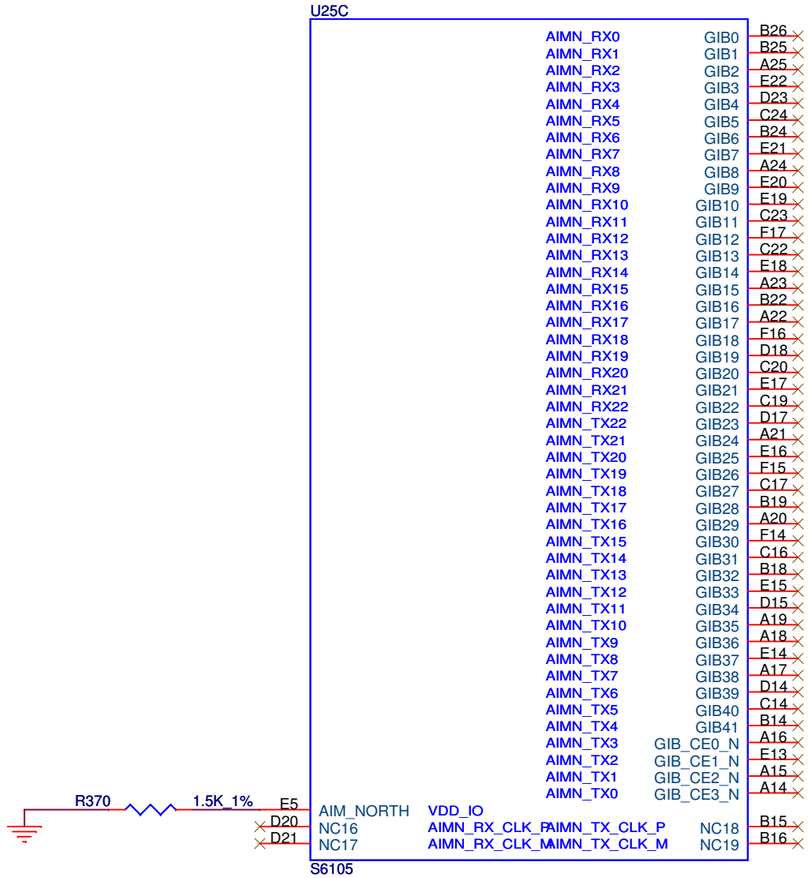
Title: Secondary 2 S6 (Data Port Interface)

Size	Document Number	BOM Variant	Internal Version	Rev
B	110-10027	NVP	N/A	5A

Date: Tuesday, January 27, 2009 Sheet 33 of 48



AIM NORTH IS POWERED FROM 2.5V

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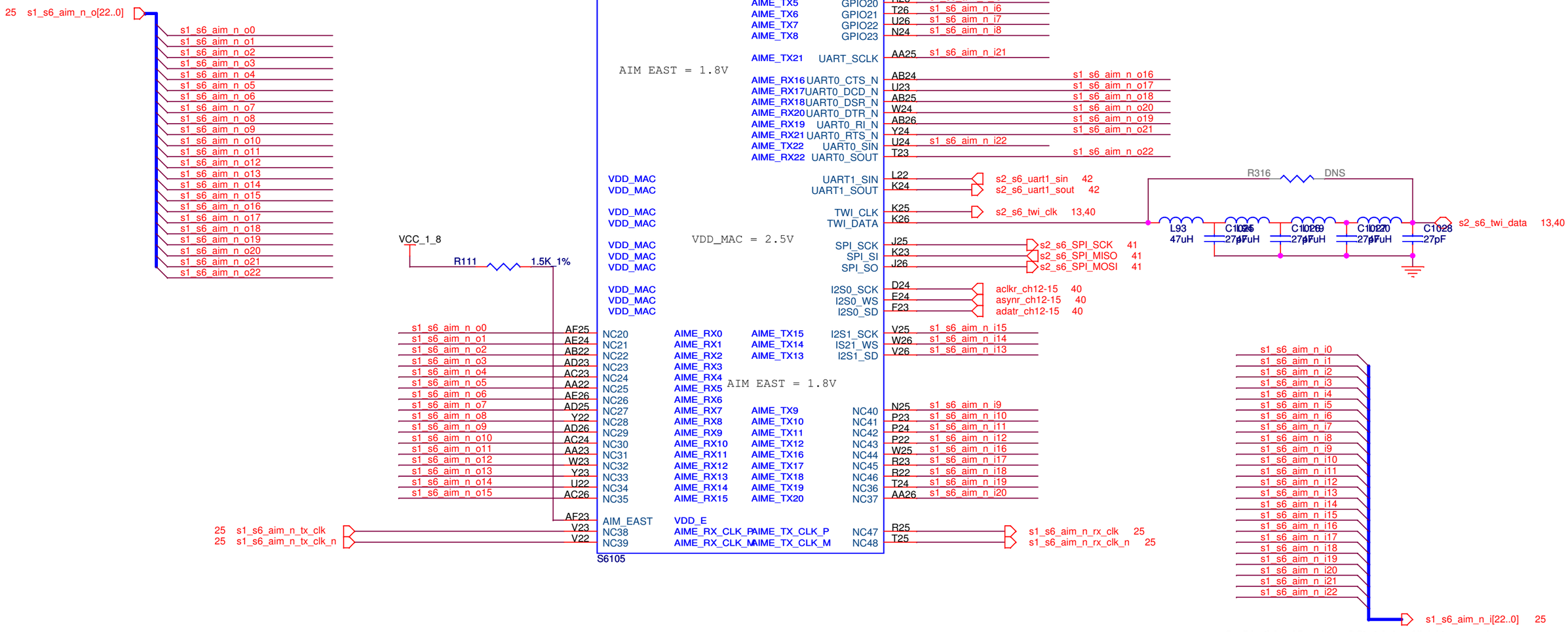
Title: Secondary 2 S6 (GIB Interface)

Size	Document Number	BOM Variant	Internal Version	Rev
B	110-10027	NVP	N/A	5A

Date: Tuesday, January 27, 2009 Sheet 34 of 48

ROUTING RULES (S6100 package legths should be taken into consideration when determining the trace lengths):
The AUDIO_R_CH12-15 bus should be matched to within +/- 500ps (2500mil).
The following buses are embedded in the schematic:
AUDIO_R_CH12-15
->contains aclkr_ch12-15, asynr_ch12-15, and adatr_ch12-15



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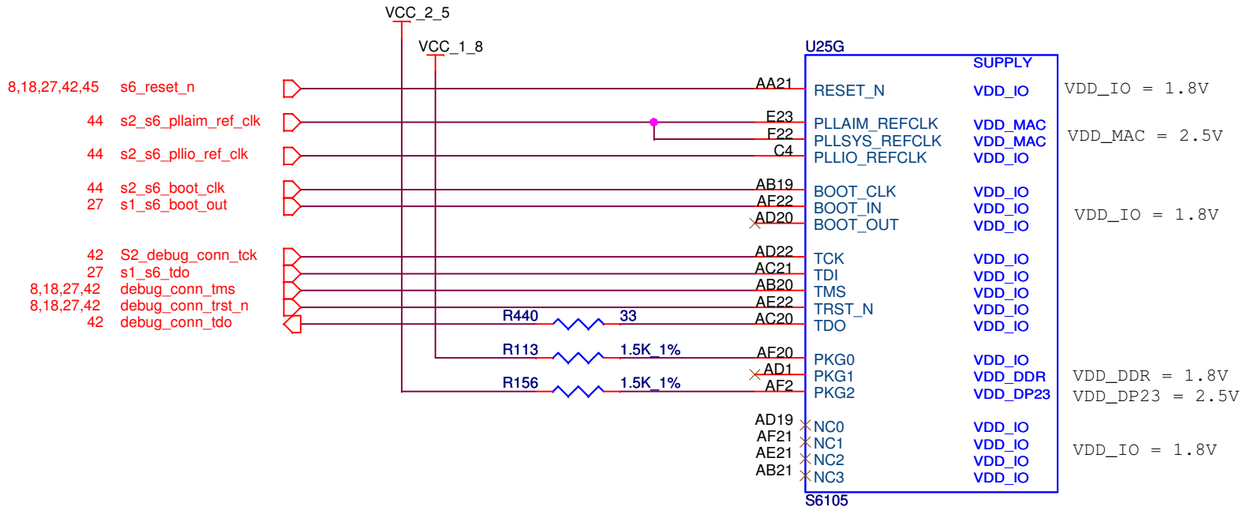
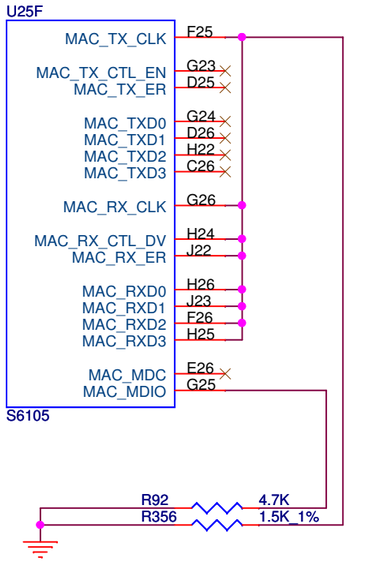
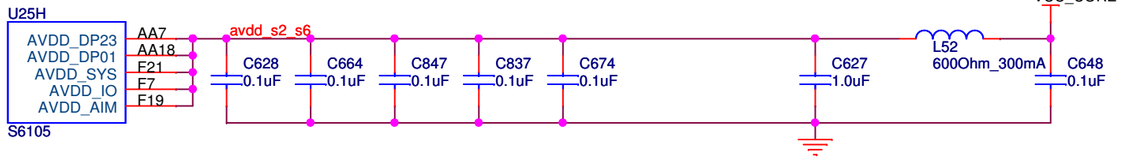
Title: Secondary 2 S6 (Low Speed Interfaces)

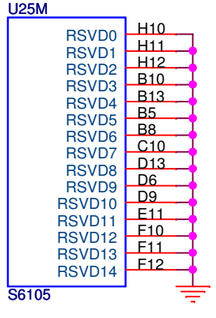
Size	Document Number	BOM Variant	Internal Version	Rev
B	110-10027	NVP	N/A	5A

Date: Tuesday, January 27, 2009 Sheet 35 of 48









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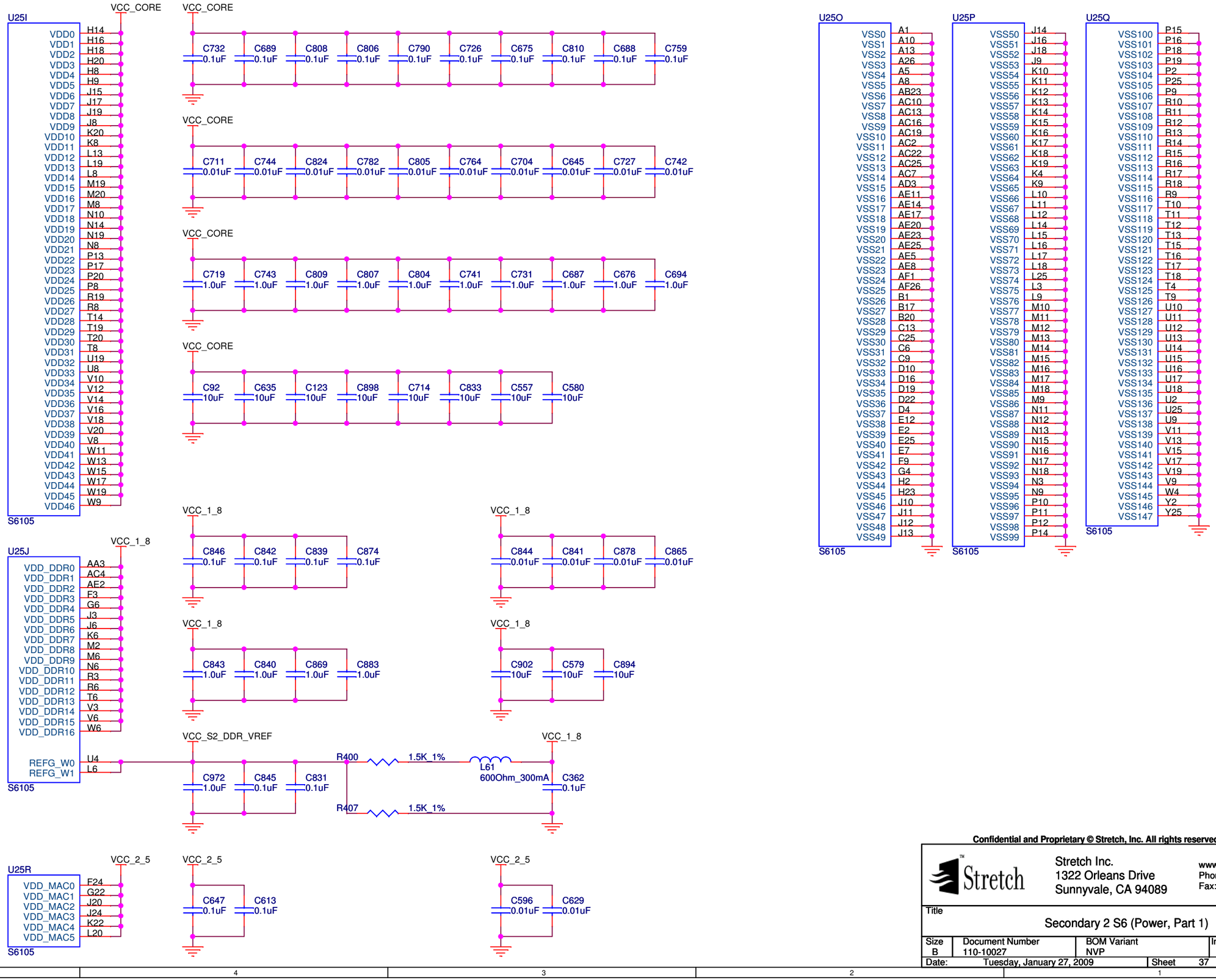
Title: Secondary 2 S6 (Miscellaneous Interfaces)

Size	Document Number	BOM Variant	Internal Version	Rev
B	110-10027	NVP	N/A	5A

Date: Tuesday, January 27, 2009 Sheet 36 of 48



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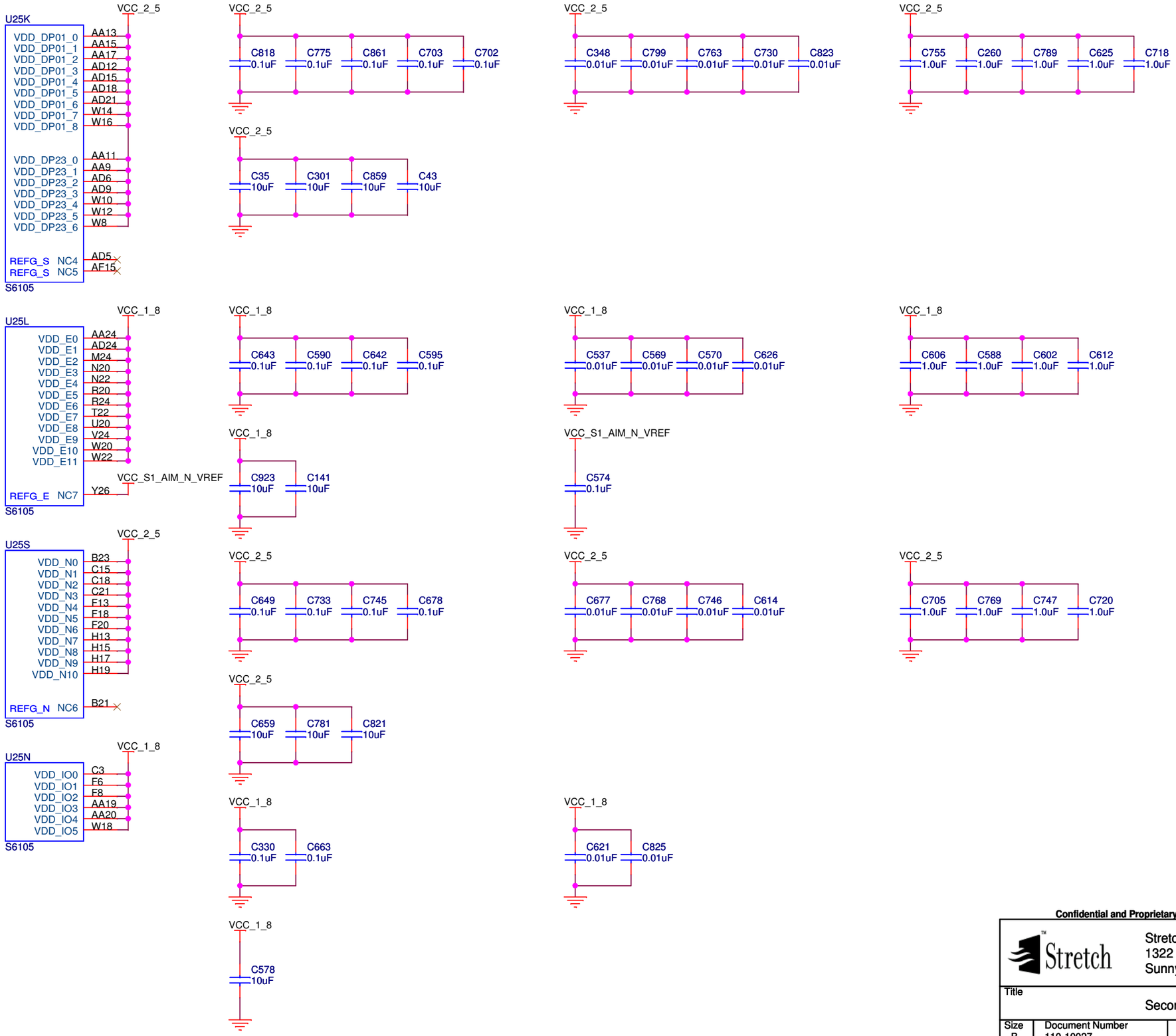
Title: Secondary 2 S6 (Power, Part 1)

Size	Document Number	BOM Variant	Internal Version	Rev
B	110-10027	NVP	N/A	5A

Date: Tuesday, January 27, 2009 Sheet 37 of 48



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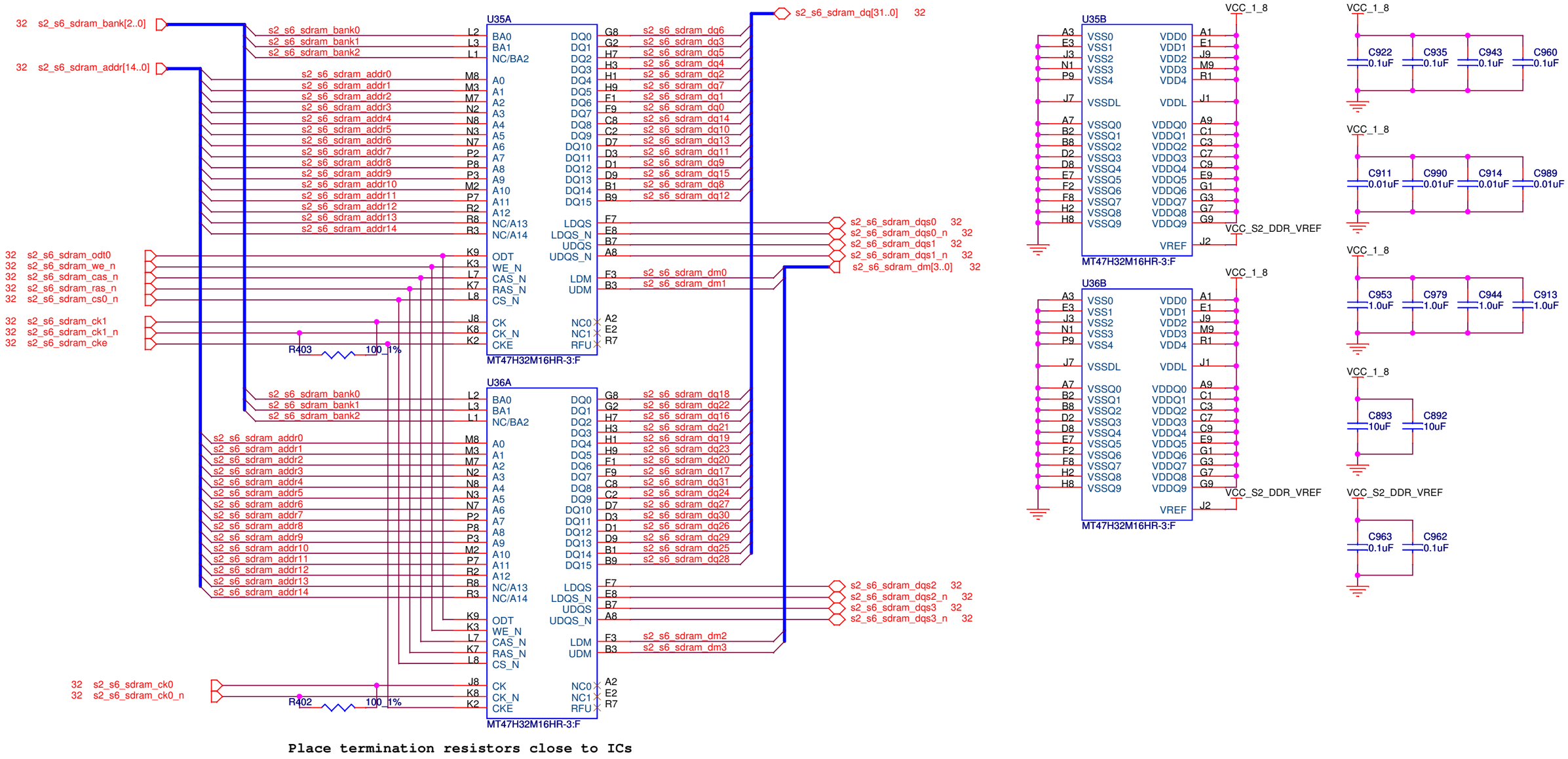
Title: Secondary 2 S6 (Power, Part 2)

Size	Document Number	BOM Variant	Internal Version	Rev
B	110-10027	NVP	N/A	5A

Date: Tuesday, January 27, 2009 Sheet 38 of 48



Place termination resistors close to ICs

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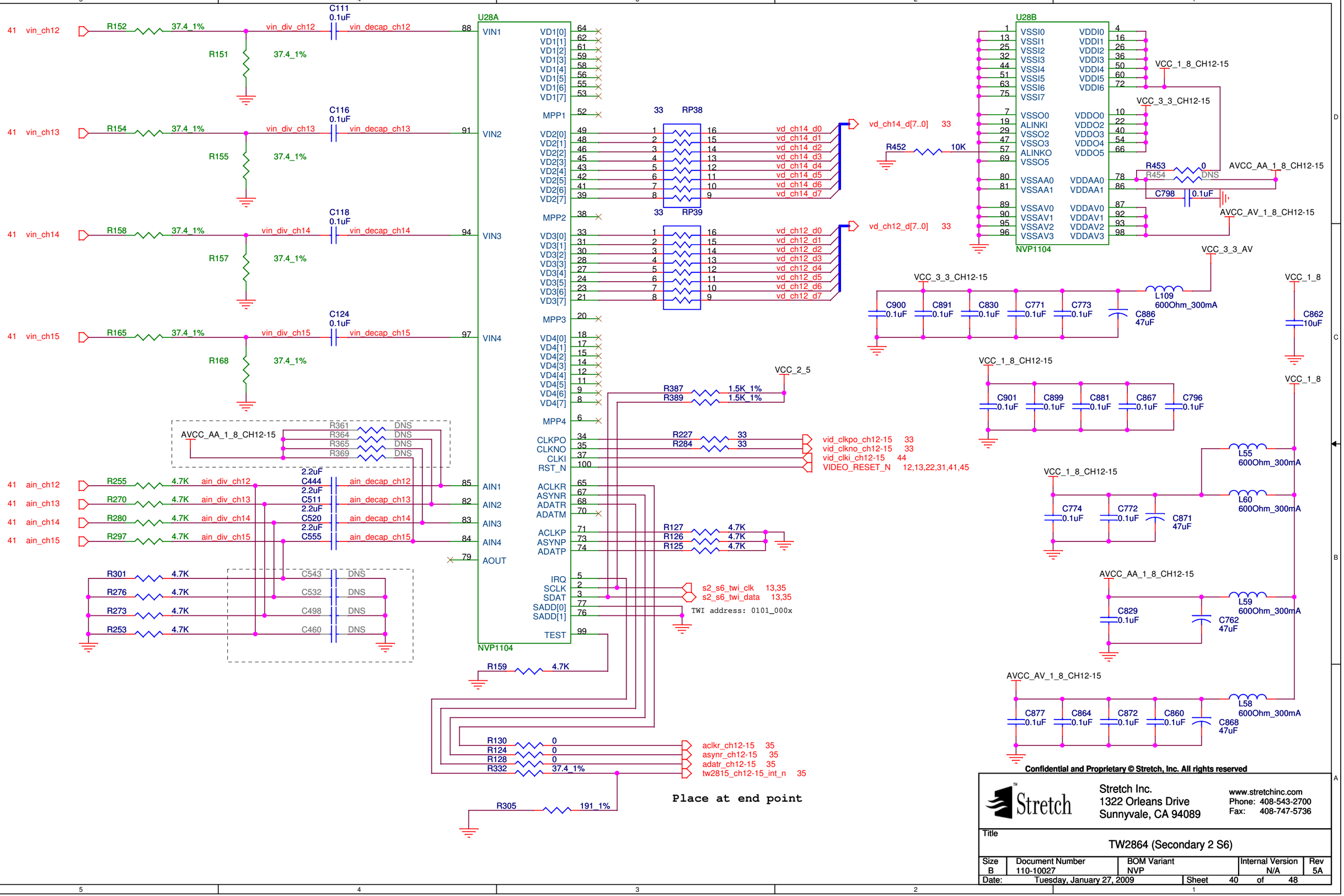
Title				
DDR ICs (Secondary 2 S6)				
Size: B	Document Number: 110-10027	BOM Variant: NVP	Internal Version: N/A	Rev: 5A
Date: Tuesday, January 27, 2009	Sheet 39 of 48			



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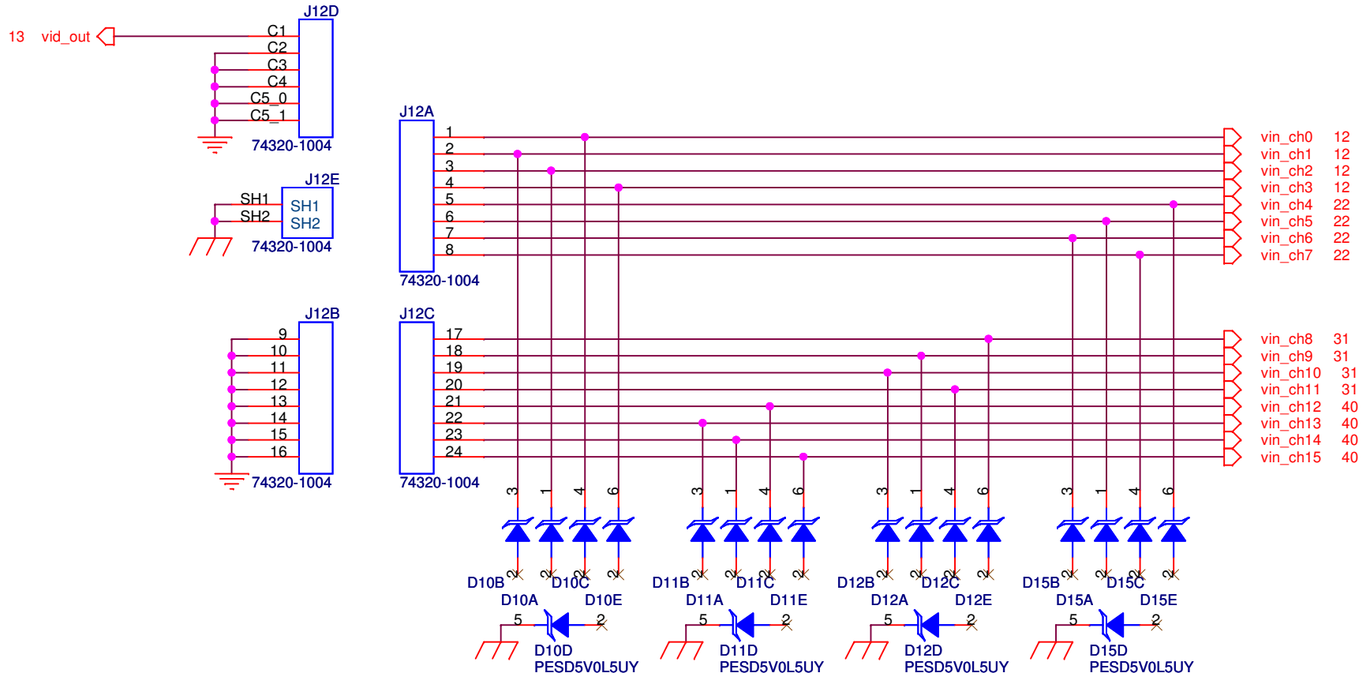
Title: TW2864 (Secondary 2 S6)

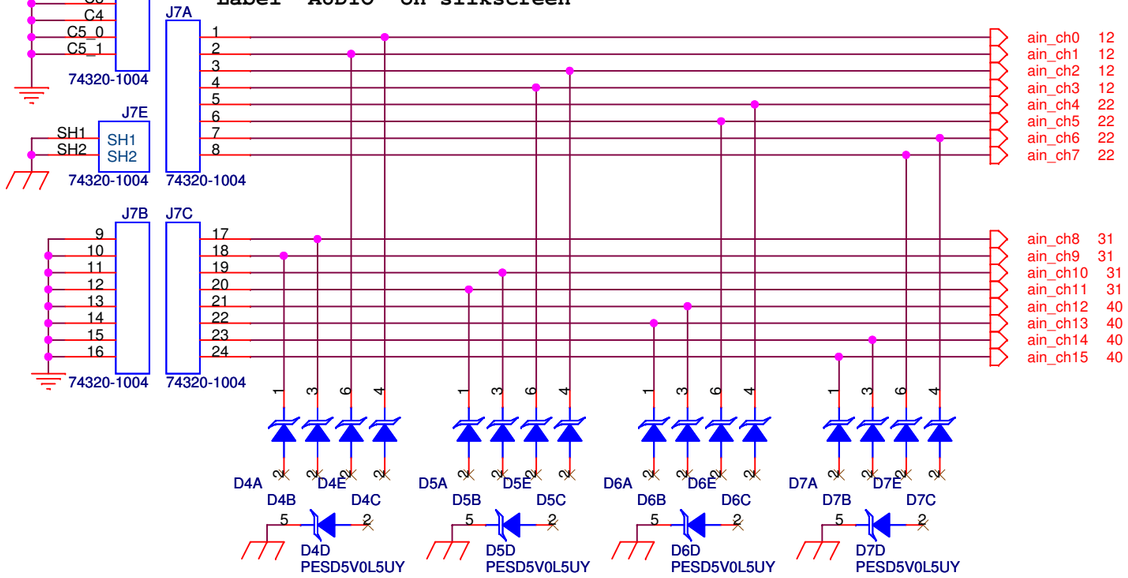
Size	Document Number	BOM Variant	Internal Version	Rev
B	110-10027	NVP	N/A	5A

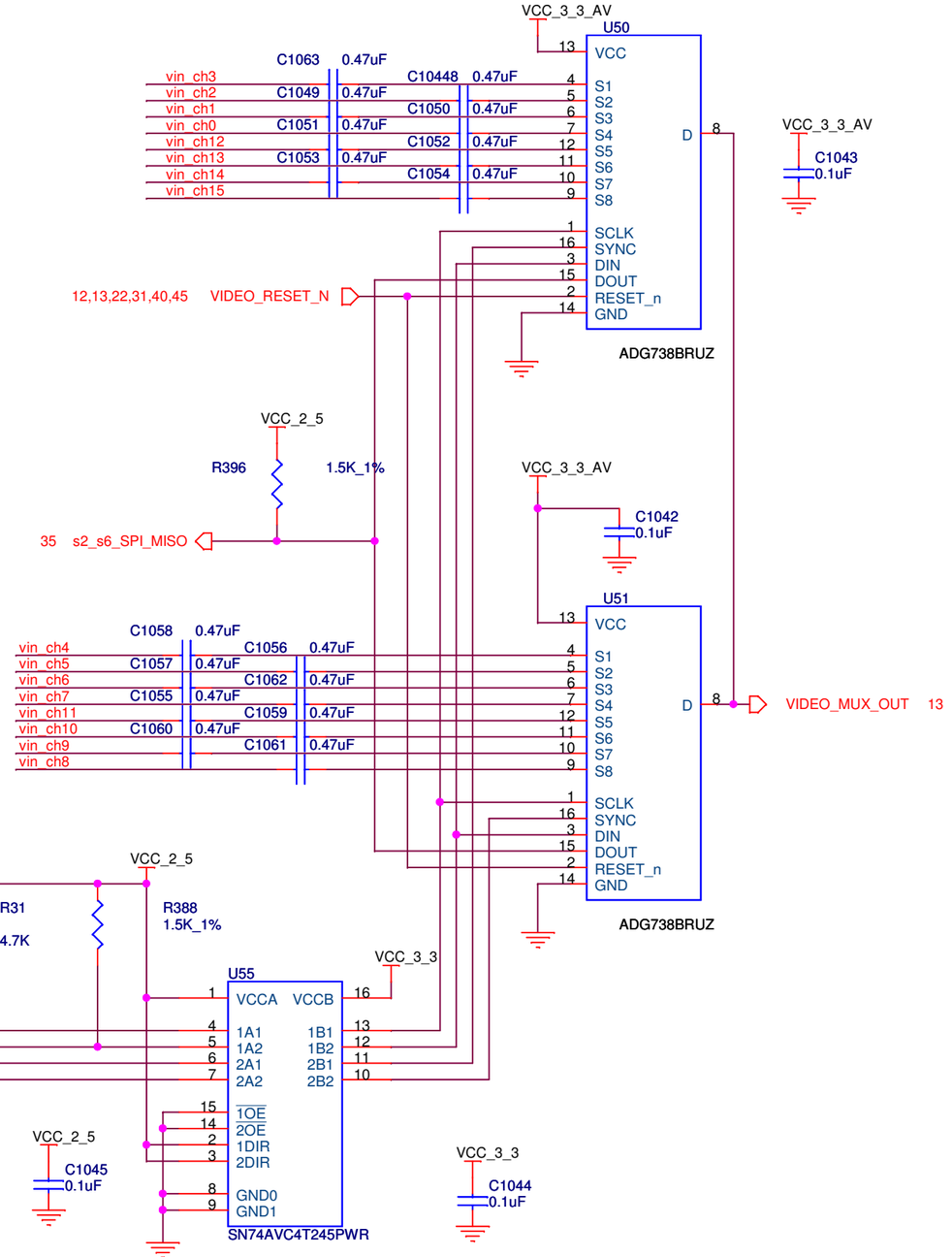
Date: Tuesday, January 27, 2009 Sheet 40 of 48

Label "VIDEO" on silkscreen



Label "AUDIO" on silkscreen





C163 DNS

L27 600Ohm_300mA

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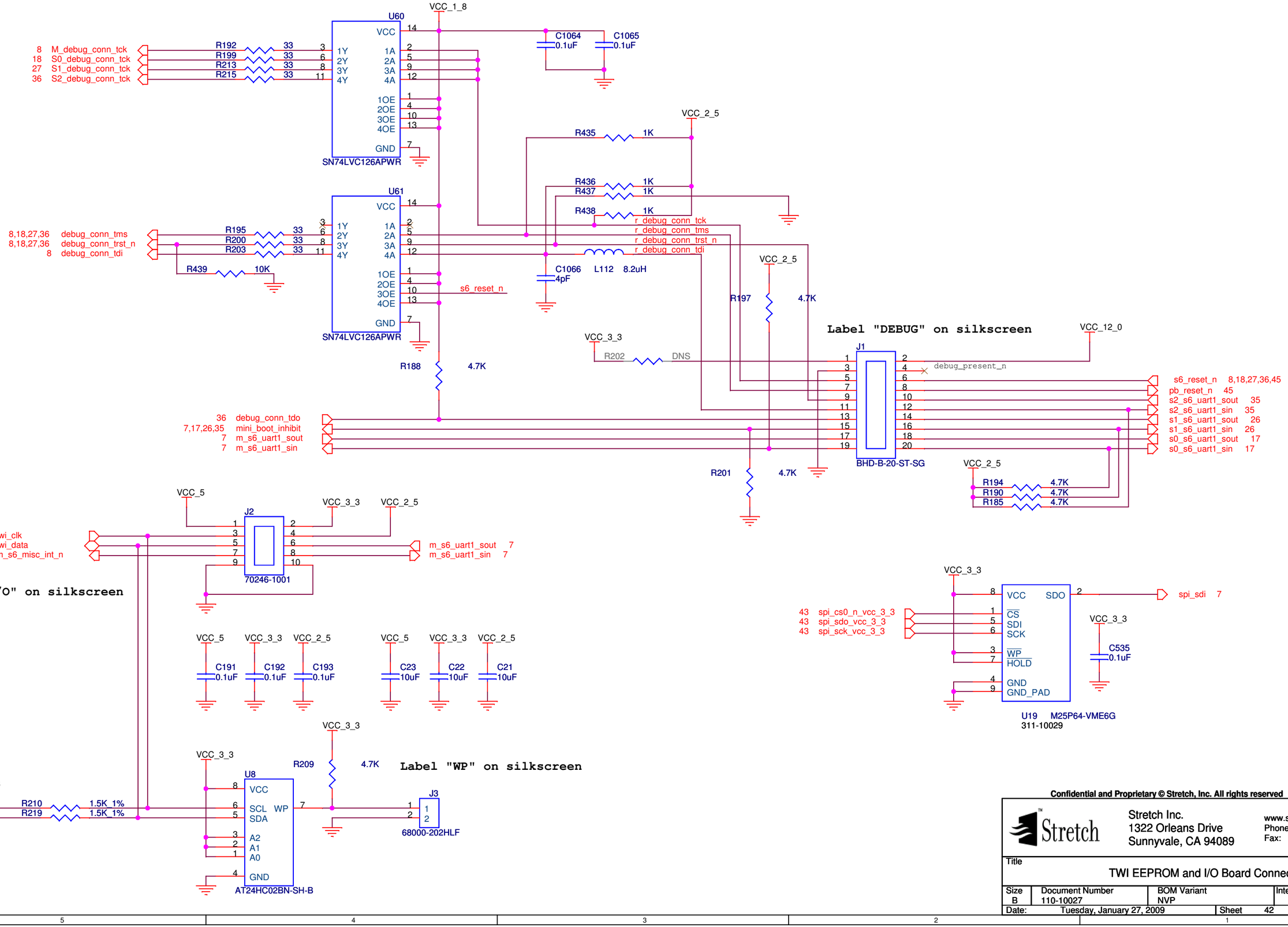
Title				
Video and Audio Connectors				
Size: B	Document Number: 110-10025	BOM Variant: NVP	Internal Version: N/A	Rev: 5A
Date: Tuesday, January 27, 2009		Sheet 41 of 48		



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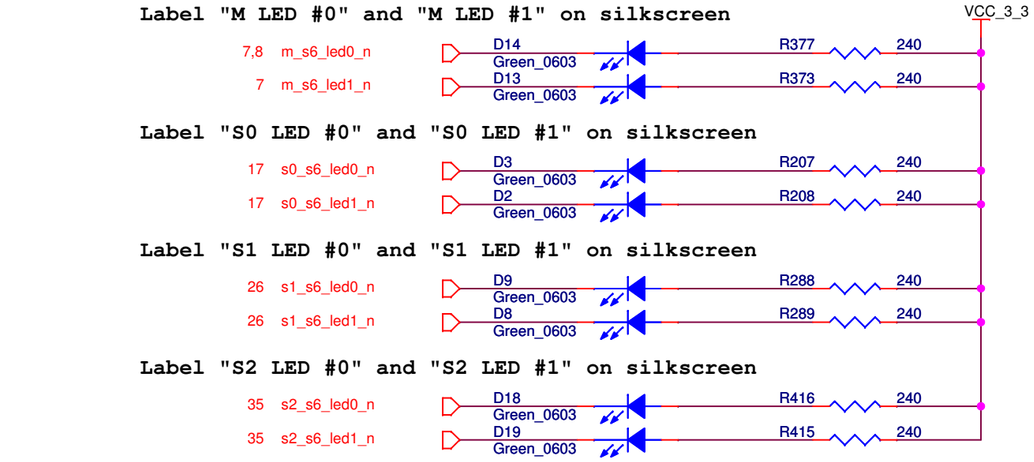
Title: TWI EEPROM and I/O Board Connectors

Size	Document Number	BOM Variant	Internal Version	Rev
B	110-10027	NVP	N/A	5A

Date: Tuesday, January 27, 2009 Sheet 42 of 48

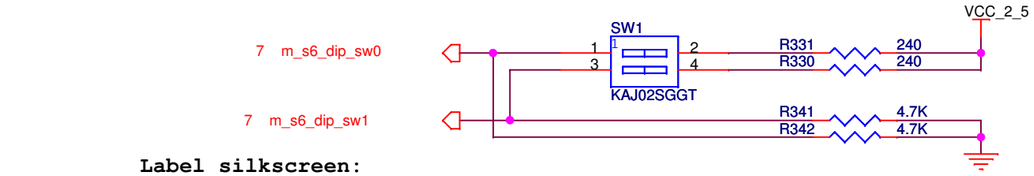
Label "M LED #0" and "M LED #1" on silkscreen



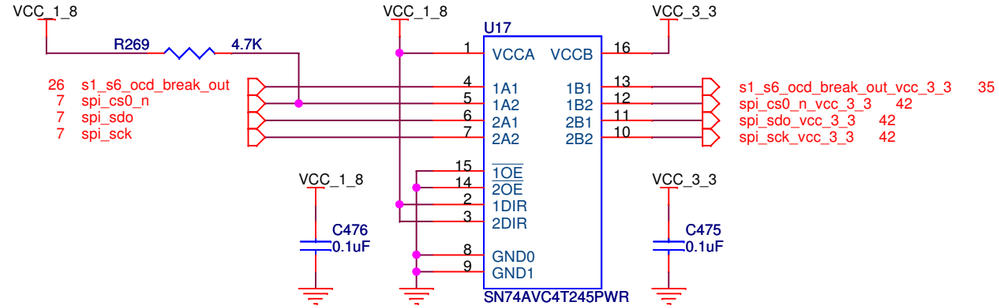
Label "S0 LED #0" and "S0 LED #1" on silkscreen

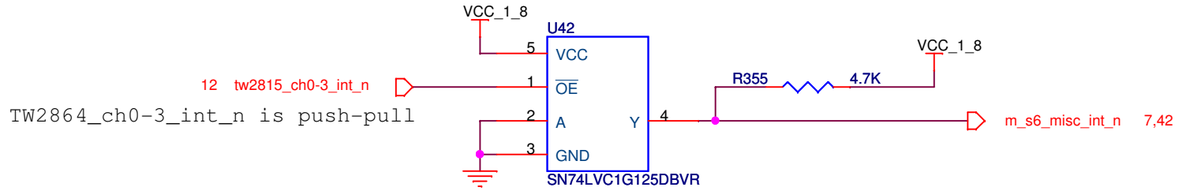
Label "S1 LED #0" and "S1 LED #1" on silkscreen

Label "S2 LED #0" and "S2 LED #1" on silkscreen



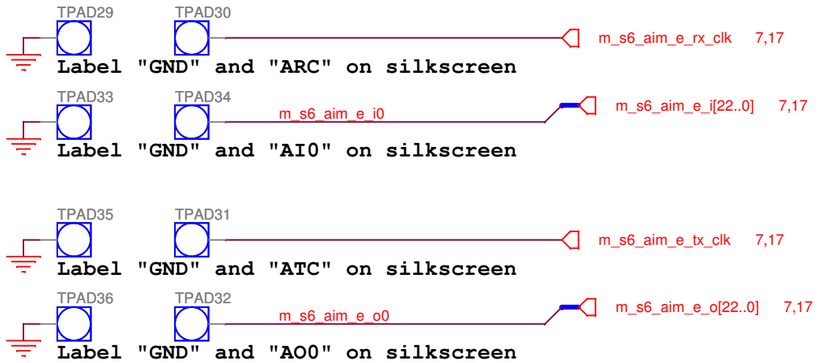
Label silkscreen:
M_SW0
M_SW1





Minimize stubs

Minimize stubs



Test components are not populated in production system.

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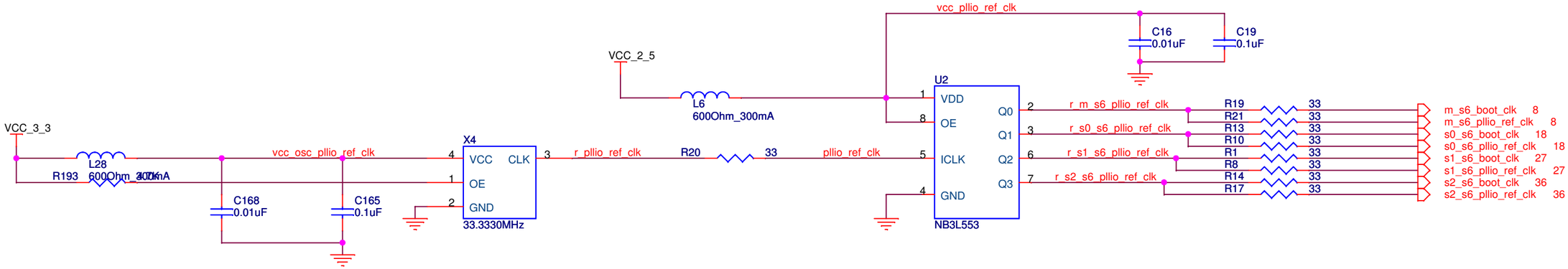
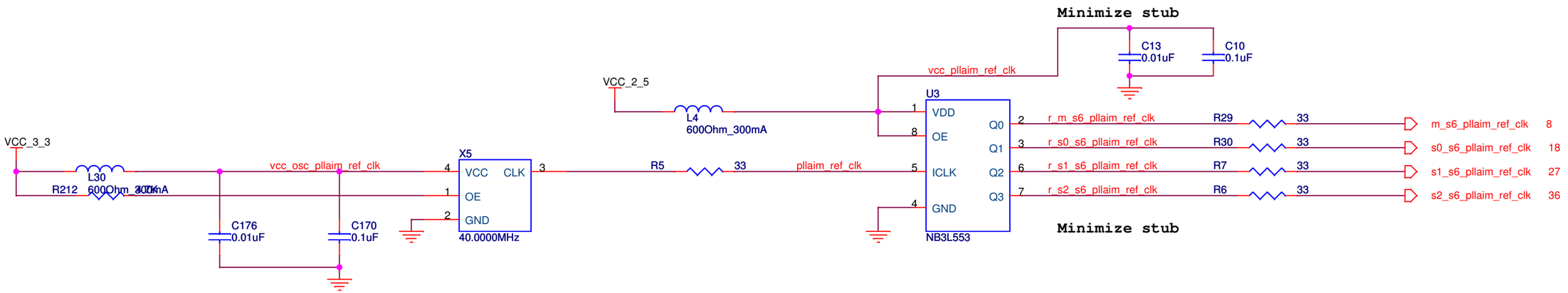
Title				
Test Components and Signal Test Points				
Size: B	Document Number: 110-10027	BOM Variant: NVP	Internal Version: N/A	Rev: 5A
Date: Tuesday, January 27, 2009		Sheet 43 of 48		

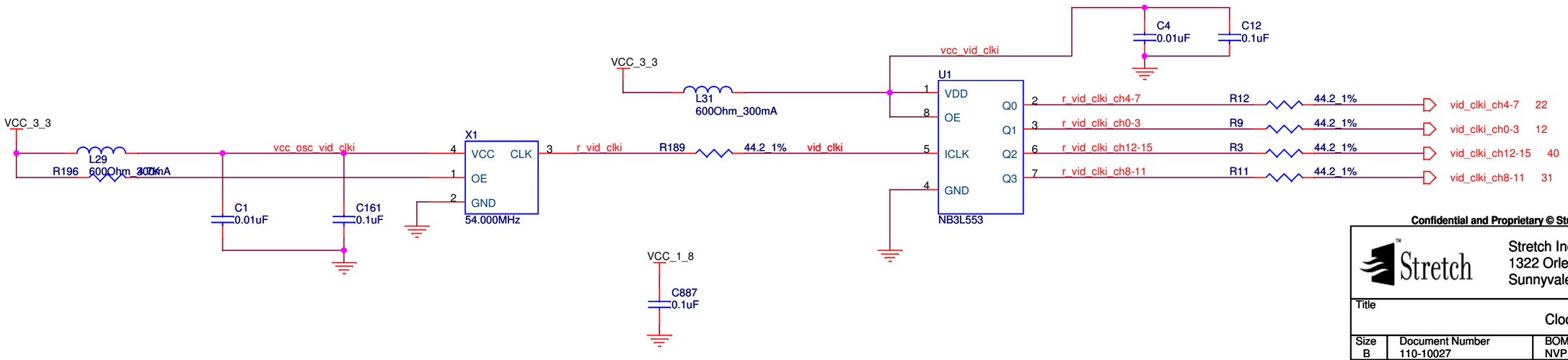


Minimize stub



Minimize stub

Make trace lengths from X5 to U39 and U3 equal.



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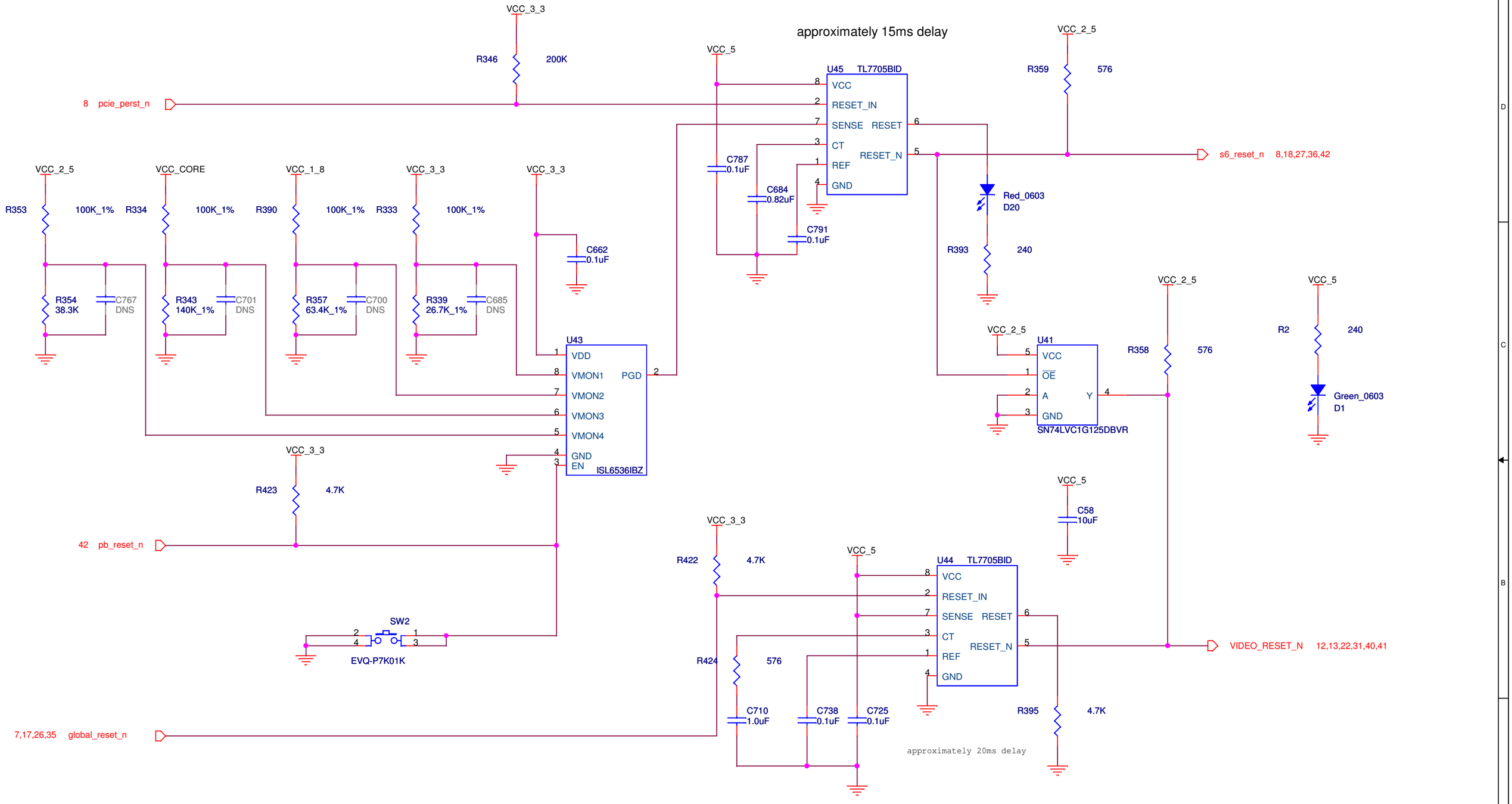
Title				
Clocks				
Size: B	Document Number: 110-10027	BOM Variant: NVP	Internal Version: N/A	Rev: 5A
Date: Tuesday, January 27, 2009	Sheet 44 of 48			



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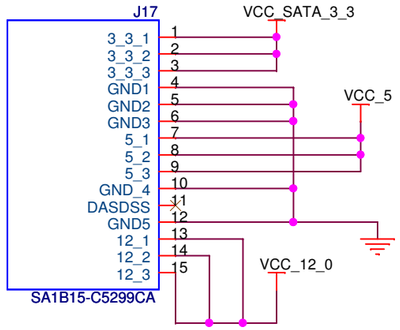
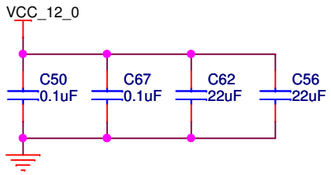
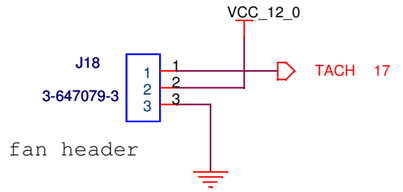
Title: Reset

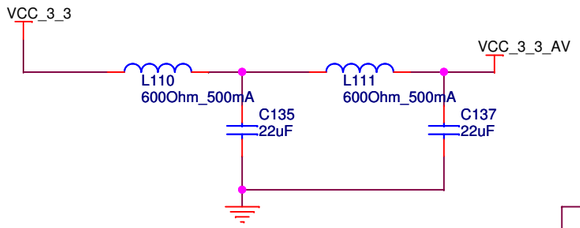
Size	Document Number	BOM Variant	Internal Version	Rev
B	110-10027	NVP	N/A	5A

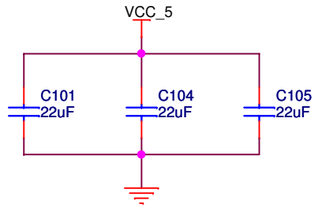
Date: Tuesday, January 27, 2009 | Sheet 45 of 48

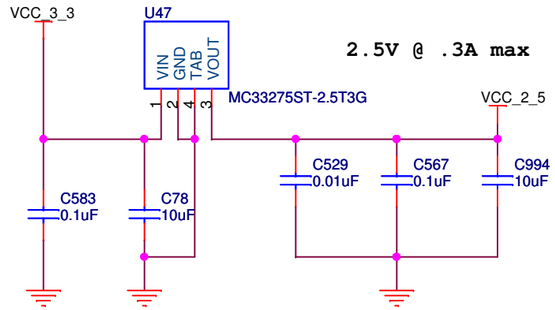


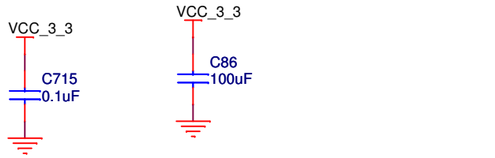


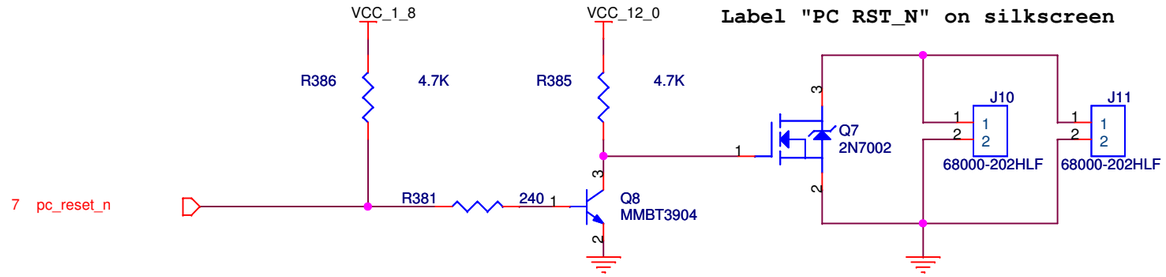


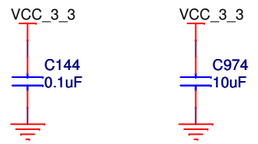


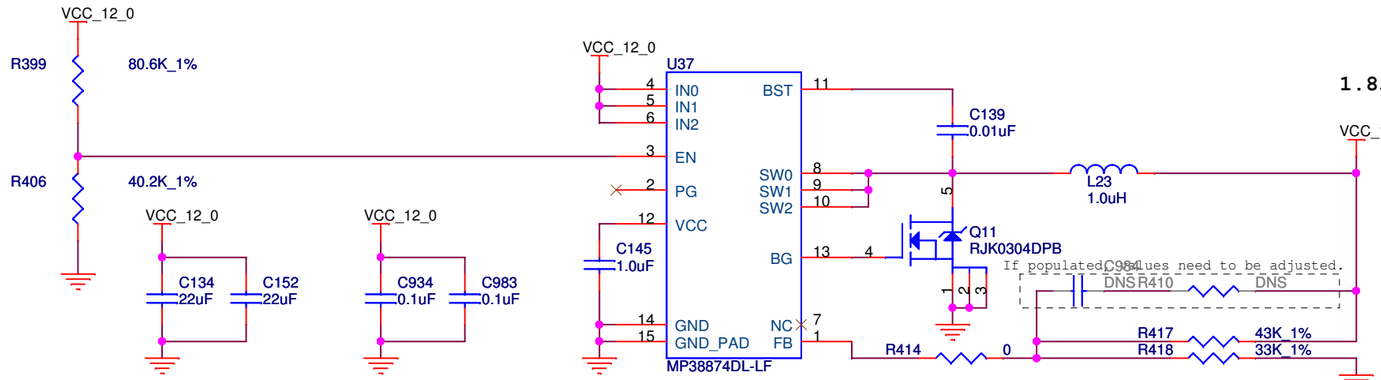


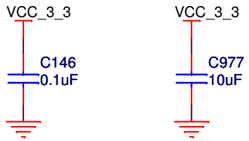












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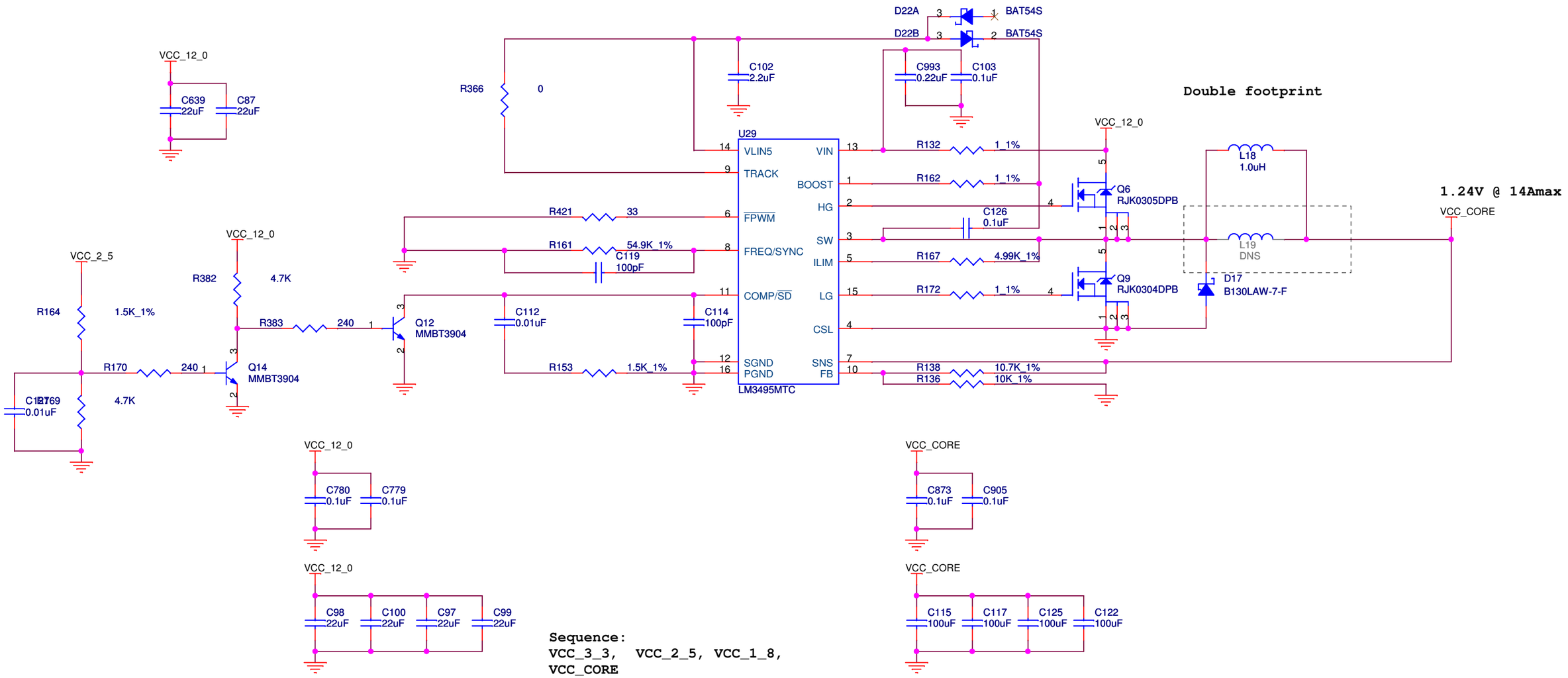
Title: VCC_1_8 and VCC_1_5 Power Supplies

Size	Document Number	BOM Variant	Internal Version	Rev
B	110-10027	NVP	N/A	5A

Date: Tuesday, January 27, 2009 Sheet 46 of 48



Sequence:
VCC_3_3, VCC_2_5, VCC_1_8, VCC_CORE

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Title				
VCC_CORE Power Supply				
Size: B	Document Number: 110-10027	BOM Variant: NVP	Internal Version: N/A	Rev: 5A
Date: Tuesday, January 27, 2009	Sheet 47 of 48			

Fab Number:
210-10027-5

JP1
JACK SCREW .250" ZINC/clear

JP2
JACK SCREW .250" ZINC/clear

JP3
JACK SCREW .250" ZINC/clear

JP4
JACK SCREW .250" ZINC/clear

BRK1
Bracket, PCI, 2 DVI cutout

hs1
Include Item 392-10020
Heat Sink, Quad S6, Cofan, w/tach

NET_PHYSICAL_TYPE:
POWER
-> Current carrying traces.
AVIDEO
-> Analog video signals
AAUDIO
-> Analog audio signals
100HM_DIFF
-> Differential signals (100 ohm).

NET_SPACING_TYPE:
WX1P5_GAP
-> 1.5x trace width spacing
WX2_GAP
-> 2.0x trace width spacing
WX2P5_GAP
-> 2.5x trace width spacing
WX3_GAP
-> 3.0x trace width spacing
WX5_GAP
-> 5.0x trace width spacing
AAUDIO
-> analog audio signal (3x trace width spacing)
AVIDEO
-> analog video signals (3.75x trace width spacing)

Revision History

Revision	Version	Date	Description
1	1	2/14/08	Created from 110-10025-10. Changed main power connector to SATA plug. Removed the 3.3V and 2.5V regulators. Replace 2.5V with LDO. Deleted mounting holes for PCI bracket. Changed to TW2864. Changed the video out circuit. Cost reduced the reset circuit. Changed the IO board connector power.
2	1	5/7/08	Changed clocks to data ports. SAA7121 was on wrong TWI bus. Trst buffer changed to be controlled by S6_reset. Soft reset pulse shortened. Changed pull up resistor values for S6 and soft reset. Added 27Mhz crystal to SAA7121 chip. Added provision for isolating 3.3V for audio/video functions. Added pull ups to Slave 2 SPI bus chip selects. Debug connector now gets S6_reset instead of soft reset. Clock out from SAA7121 goes to PE3 ref clk 2-3. clk N from PE3 TW goes to DP2 clk. AV connectors only use earth ground for the shell, no signals. Changed video out circuit, bias and output buffer, 16 video input caps. Load switch from PCI connector for 3.3V is now controlled by a jumper. Changed audio input resistor values per TW newest spec. fan header is now right angle. / 2.5V LDO moved to back side.
3	1	5/27/08	Moved video out filter to the output of the SAA7121. Changed S6_reset pulse width to 100ms.
3.1	1	6/6/08	Changed core voltage to 1.24V TYP.
3.2	1	6/16/08	Part number of the EEPROM was wrong.
3.B	1	7/15/08	AC termination for JTAG clock change
3.C	1	8/13/08	Changed reset time delay to 15ms
4.A	1	10/20/08	Changed SATA connector Tied PC reset FET source pin to gnd Deleted C136. Added TACH output from fan (to PE3). Added ICT fixes. Added header for SMO daisy chaining and GPIO 7 control for video output buffer Connected ref clocks to port clocks Removed connection to SATA 3.3V Changed the PCI bracket
5A	1	12/16/08	Changed analog SMO circuit
		01/26/09	Linked part to stretch database Add variant option for NVP1104

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Title: Mounting Holes and Revision Table

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