

a-Si TFT LCD Single Chip Driver 320RGBx480 Resolution and 262K-color

Specification ***Preliminary***

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1. Introduction

ILI9486L is a 262,144-color single-chip SoC driver for a-Si TFT liquid crystal display with resolution of 320RGBx480 dots, comprising a 960-channel source driver, a 480-channel gate driver, 345,600bytes GRAM for graphic data of 320RGBx480 dots, and power supply circuit.

The ILI9486L supports parallel CPU 8-/9-/16-/18-bit data bus interface and 3-/4-line serial peripheral interfaces (SPI). The ILI9486L is also compliant with RGB (16-/18-bit) data bus for video image display.

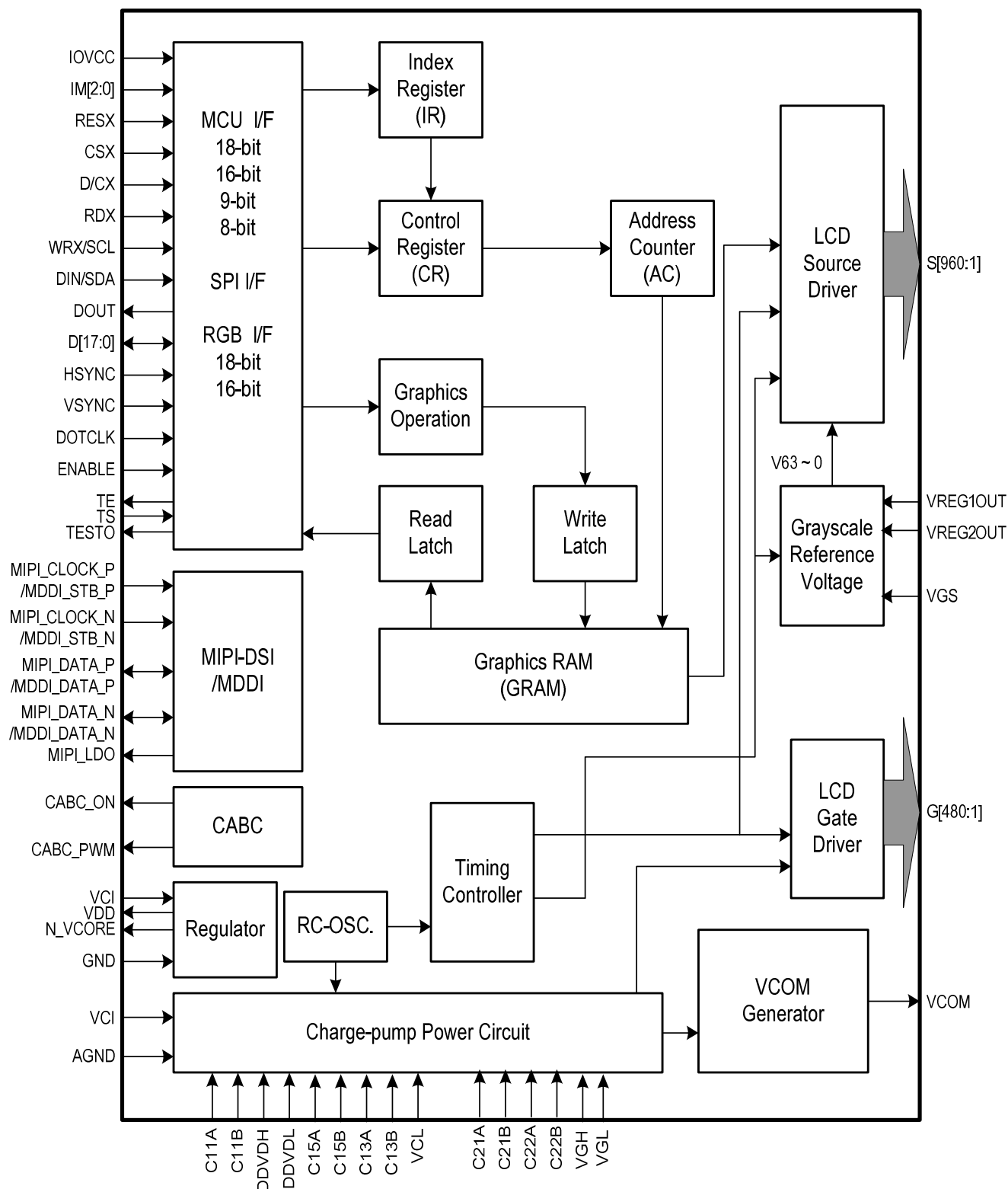
ILI9486L can operate with 1.65V I/O interface voltage and support wide analog power supply range. ILI9486L also supports a function to display in 8 colors and a sleep mode, allowing for precise power control by software and these features make the ILI9486L as an ideal LCD driver for medium or small size portable products such as digital cellular phones, smart phone, MP3 and PMP where long battery life is a major concern.

2. Features

- ◆ Display resolution: [320xRGB](H) x 480(V)
- ◆ Output:
 - 960 source outputs
 - 480 gate outputs
 - Common electrode output
- ◆ a-TFT LCD driver with on-chip full display RAM: 345,600 bytes
- ◆ Interface
 - 8-bits, 9-bits, 16-bits, 18-bits interface with 8080-series MCU
 - 16-bits, 18-bits RGB interface with graphic controller
 - 3-line / 4-line serial interface
- ◆ Display mode:
 - Full color mode (Idle mode OFF) : 262K-colors, 65K-colors.
 - Reduce color mode (Idle mode ON) : 8-color.
- ◆ Power saving mode:
 - Deep-standby mode
 - Sleep mode
- ◆ On chip functions:
 - DC VCOM generator and adjustment
 - Timing generator
 - Oscillator
 - DC/DC converter
 - Dot/Column/Z inversion
 - Separate RGB Gamma correction
 - CABC(Content adaptive brightness control)
- ◆ MTP (4 times):
 - 8-bits for ID1
 - 8-bits for ID2
 - 8-bits for ID3
 - 7-bits for VCOM adjustment
- ◆ Low -power consumption architecture
 - Low operating power supplies:
 - IOVCC = 1.65V ~ 3.6V (Digital)
 - VCI = 2.5V ~ 3.6V (Analog)

- ◆ LCD Voltage drive:
 - Source/VCOM power supply voltage
 - DDVDH - GND = 4.5V ~ 6.0V
 - VCL - GND = -2.0~-3.0V
 - VCI1 - VCL \leq 6.0V
 - Gate driver output voltage
 - VGH - GND = 10.0V ~ 20.0V
 - VGL - GND = -5.0V ~ -15.0V
 - VGH - VGL \leq 32.0V
 - VCOM driver output voltage
 - VCOM = 0~-2.0V
- ◆ Operate temperature range: -40°C to 85°C
- ◆ a-Si TFT LCD storage capacitor : Cst on Common structure only

3. Block Diagram



4. Pin Descriptions

Bus Interface Pins																																																	
Pin Name	I/O	Type	Descriptions																																														
IM[2:0]	I	MPU IOVCC/DGND	- Select the interface mode <table border="1"> <thead> <tr> <th>IM2</th><th>IM1</th><th>IM0</th><th>Interface</th><th>Data Pin in Use</th></tr> </thead> <tbody> <tr> <td>0</td><td>0</td><td>0</td><td>8080 18-bit bus interface</td><td>DB[17:0]</td></tr> <tr> <td>0</td><td>0</td><td>1</td><td>8080 9-bit bus interface</td><td>DB[8:0]</td></tr> <tr> <td>0</td><td>1</td><td>0</td><td>8080 16-bit bus interface</td><td>DB[15:0]</td></tr> <tr> <td>0</td><td>1</td><td>1</td><td>8080 8-bit bus interface</td><td>DB[7:0]</td></tr> <tr> <td>1</td><td>0</td><td>0</td><td>Prohibited</td><td>-</td></tr> <tr> <td>1</td><td>0</td><td>1</td><td>3-line SPI</td><td>SDA</td></tr> <tr> <td>1</td><td>1</td><td>0</td><td>Prohibited</td><td>-</td></tr> <tr> <td>1</td><td>1</td><td>1</td><td>4-line SPI</td><td>SDA</td></tr> </tbody> </table>		IM2	IM1	IM0	Interface	Data Pin in Use	0	0	0	8080 18-bit bus interface	DB[17:0]	0	0	1	8080 9-bit bus interface	DB[8:0]	0	1	0	8080 16-bit bus interface	DB[15:0]	0	1	1	8080 8-bit bus interface	DB[7:0]	1	0	0	Prohibited	-	1	0	1	3-line SPI	SDA	1	1	0	Prohibited	-	1	1	1	4-line SPI	SDA
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1	1	1	4-line SPI	SDA																																													
RESX	I	MPU/ Reset circuit	- The external reset input. - Initializes the chip with a low input. Be sure to execute a power-on reset after supplying power.																																														
CSX	I	MPU	- A chip select signal. Low: the chip is selected and accessible High: the chip is not selected and not accessible Fix to IOVCC or DGND level when not in use.																																														
D/CX	I	MPU	- Parallel interface (D/CX): The signal for command or parameter select. Low: Command. High: Parameter. Fix to IOVCC or DGND level when not in use.																																														
WRX/SCL	I	MPU IOVCC	- 8080 system (WRX): Serves as a write signal and writes data at the rising edge. - 3/4-line serial interface (SCL): The pin used as serial clock pin. Fix to IOVCC or DGND level when not in use.																																														
RDX	I	MPU	- 8080 system (RDX): Serves as a read signal and read data at the rising edge. Fix to IOVCC or DGND level when not in use.																																														
DIN/SDA	I/O	MPU	- Serial data input / output. Fix to IOVCC or DGND level when not in use.																																														
DOUT	O	MCU	- Serial data output Leave the pin to open when not in use.																																														
TE	O	MPU	- Tearing effect output. Leave the pin to open when not in use.																																														
CABC_PWM	O	VCI	- Back light control pin. Leave the pin to open when not in use.																																														
CABC_ON	O	VCI	- Back light control pin. Leave the pin to open when not in use.																																														
MIPI_CLOCK_P	I	MIPI	Leave the pin to open.																																														
MIPI_CLOCK_N	I	MIPI	Leave the pin to open.																																														
MIPI_DATA_P	I/O	MIPI	Leave the pin to open.																																														
MIPI_DATA_N	I/O	MIPI	Leave the pin to open.																																														

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DB[17:0]	I/O	MPU	A 18-bit parallel bi-directional data bus for MCU system														
			<table><tr><th>Interface Mode</th><th>Data Pin in Use</th></tr><tr><td>8-bit MCU System Interface Mode</td><td>DB[7:0]</td></tr><tr><td>9-bit MCU System Interface Mode</td><td>DB[8:0]</td></tr><tr><td>16-bit MCU System Interface Mode</td><td>DB[15:0]</td></tr><tr><td>18-bit MCU System Interface Mode</td><td>DB[17:0]</td></tr><tr><td>16-bit RGB Interface Mode</td><td>DB[15:0]</td></tr><tr><td>18-bit RGB Interface Mode</td><td>DB[17:0]</td></tr></table>	Interface Mode	Data Pin in Use	8-bit MCU System Interface Mode	DB[7:0]	9-bit MCU System Interface Mode	DB[8:0]	16-bit MCU System Interface Mode	DB[15:0]	18-bit MCU System Interface Mode	DB[17:0]	16-bit RGB Interface Mode	DB[15:0]	18-bit RGB Interface Mode	DB[17:0]
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			18-bit MCU System Interface Mode	DB[17:0]													
			16-bit RGB Interface Mode	DB[15:0]													
18-bit RGB Interface Mode	DB[17:0]																
<i>Fix to DGND level when not in use.</i>																	
VSYNC	I	MPU	Frame synchronizing signal for RGB interface operation. <i>Fix to DGND level when not in use.</i>														
HSYNC	I	MPU	- Line synchronizing signal for RGB interface operation. <i>Fix to DGND level when not in use.</i>														
ENABLE	I	MPU	- Data enable signal for RGB interface operation. Low : access enabled. High : access inhibited. <i>Fix to DGND level when not in use.</i>														
DOTCLK	I	MPU	- Dot clock signal for RGB interface operation. <i>Fix to IOVCC level when not in use.</i>														

LCD Driving Signals			
Pin Name	I/O	Type	Descriptions
S961~S1	O	LCD	- Source output voltage signals applied to liquid crystal. Leave the pin to open when not in use.
G480~G1	O	LCD	- Gate line output signals. VGH: the level selecting gate lines VGL: the level not selecting gate lines Leave the pin to open when not in use.
VCOM	O	-	- The power supply of common voltage in DC VCOM driving. - The voltage range is set between -2V to 0V.
VREG1OUT	O	-	- Internal generated stable power for source driver unit. - The voltage level can be set by VRH1[4:0]. - VREG1OUT is a positive grayscale reference voltage of source driver. - VREG1OUT =3.6~5.5V
VREG2OUT	O	-	- Internal generated stable power for source driver unit. - The voltage level can be set by VRH2[4:0]. - VREG2OUT is a negative grayscale reference voltage of source driver. - VREG2OUT =-3.6~-5.5V
VGS	I	-	Reference level for grayscale generating circuit.

Charge-pump and Regulator Circuit			
Pin Name	I/O	Type	Descriptions
VCI	P	Power supply	- A supply voltage to the analog circuit. Connect to an external power supply of 2.5 ~ 3.6V.
DDVDH	O	Stabilizing capacitor	- Power supply for the source driver and VCOM driver. - Connect to a stabilizing capacitor between DDVDH and GND.
DDVDL	O	Stabilizing capacitor	- Power supply for the source driver and VCOM driver. - Connect to a stabilizing capacitor between DDVDL and GND.
VGH	O	Stabilizing capacitor	- Power supply for the gate driver. - Connect to a stabilizing capacitor between VGH and GND.
VGL	O	Stabilizing	- Power supply for the gate driver. .

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		capacitor	- Connect to a stabilizing capacitor between VGL and GND.
VCL	O	Stabilizing capacitor	- VCOML driver power supply. - VCL = 0.5 ~ -VCI, place a stabilizing capacitor between VCL and GND.
C11A, C11B C15A, C15B	O	Step-up capacitor	- Capacitor connection pins for the step-up circuit 1
C13A, C13B C21A, C21B C22A, C22B	O	Step-up capacitor	- Capacitor connection pins for the step-up circuit 2.

Power Pads			
Pin Name	I/O	Type	Descriptions
IOVCC	P	Power supply	- A supply voltage to the digital circuit. Connect to an external power supply of 1.65 ~ 3.6V.
VDD	O	Power	- Digital circuit power pad. Connect these pins with the 1uF capacitor.
N_VCORE	O	Power	- Digital circuit negative power pad. Connect these pins with the 1uF capacitor.
DGND	P	Power supply	- DGND for the digital side: DGND = 0V. In case of COG, connect to GND on the FPC to prevent noise.
AGND	P	Power supply	- AGND for the analog side: AGND = 0V. In case of COG, connect to GND on the FPC to prevent noise.
VPD	P	Power supply	- Power supply pin for the NV memory programming. Please provide 7 volt to this pin for NV memory programming.
MIPI_LDO	P	Stabilizing capacitor	Leave this pad as open.

Test Pads			
Pin Name	I/O	Type	Descriptions
DUMMY	-	-	-- Dummy pad. Leave the pin to be open when not in use.
TS[2:0]	I	IOGND	- Test pins These pins are internal pulled low. Please leave these pins as open or connected to GND.
TEST[5:0]	O	-	-TEST[5:0]: When set in test mode, the pin are test pins. Leave these pins to be open when not in use.
V1T V62T VWT	I	-	- Test pins. Leave these pins to be open when not in use.

Liquid crystal power supply specifications Table

No.	Item		Description
1	TFT Source Driver		960 pins (320 x RGB)
2	TFT Gate Driver		480 pins
3	TFT Display's Capacitor Structure		Cst structure only (Cs on Common)
4	Liquid Crystal Drive Output	S1 ~ S960	V0 ~ V63 grayscales
		G1 ~ G480	VGH – VGL
		VCOM	0~-2.0V
5	Input Voltage	IOVCC	1.65 ~ 3.60V
		VCI	2.50 ~ 3.60V
6	Liquid Crystal Drive Voltages	DDVDH	4.5V ~ 6.5V
		DDVDL	-6.5V ~ -4.5V
		VGH	10.0V ~ 20.0V
		VGL	-5.0V ~ -15.0V
		VCL	-1.9 ~ -3.0V
		VGH – VGL	Max. 32.0V
7	Internal Step-up Circuits	DDVDH	VCI1 X2
		DDVDL	-(VCI1-VCL)
		VGH	VCI1 x4, x5, x6
		VGL	VCI1 x-3, x-4, x-5
		VCL	VCI1 x-1

5. Pad Arrangement and Coordination

Chip Size: 22850um x 850um

Chip thickness : 250um (typ.)

Pad Location: Pad Center.

Coordinate Origin: Chip center

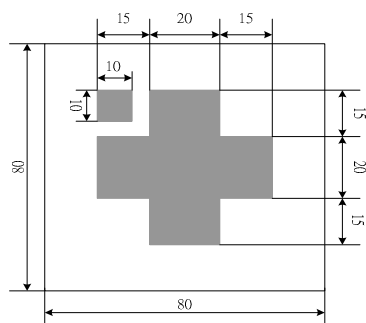
Au bump height: 15um (typ.)

Au Bump Size:

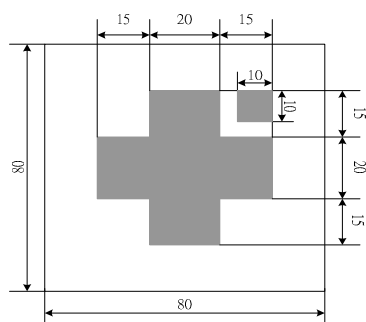
1. 15um x 100um
Gate: G1 ~ G480
Source: S1 ~ S961

2. 50um x 80um
Input Pads
Pad 1 to 320.

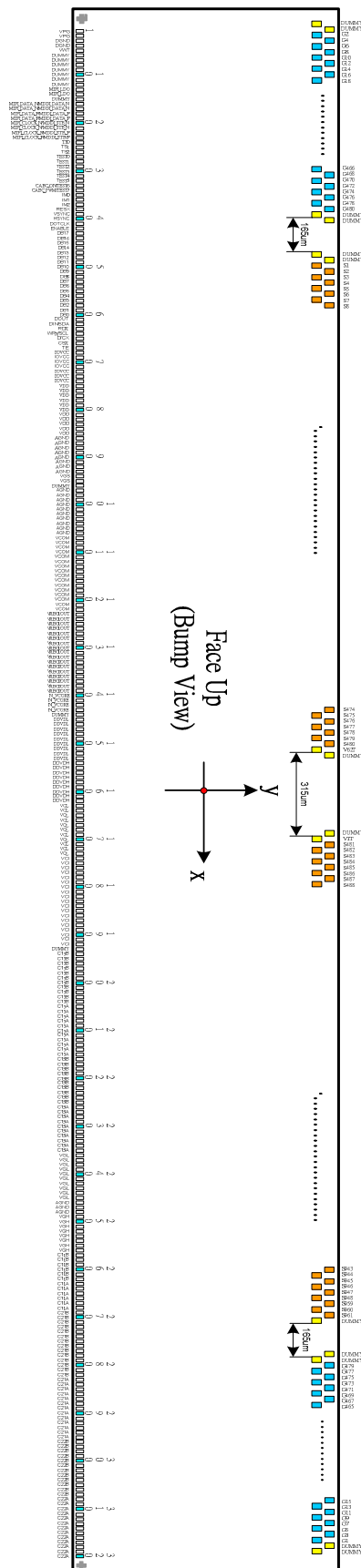
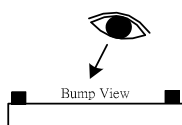
Alignment Marks



Alignment Mark: Left



Alignment Mark: Right



No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
1	VPG	-11165	-279	51	DB9	-7665	-279	101	AGND	-4165	-279	151	DDVDL	-665	-279	201	C13B	2835	-279
2	VPG	-11095	-279	52	DB8	-7595	-279	102	AGND	-4095	-279	152	DDVDL	-595	-279	202	C13B	2905	-279
3	DGND	-11025	-279	53	DB7	-7525	-279	103	AGND	-4025	-279	153	DDVDL	-525	-279	203	C13B	2975	-279
4	DGND	-10955	-279	54	DB6	-7455	-279	104	AGND	-3955	-279	154	DDVDH	-455	-279	204	C13B	3045	-279
5	VWT	-10885	-279	55	DB5	-7385	-279	105	AGND	-3885	-279	155	DDVDH	-385	-279	205	C13A	3115	-279
6	DUMMY	-10815	-279	56	DB4	-7315	-279	106	AGND	-3815	-279	156	DDVDH	-315	-279	206	C13A	3185	-279
7	DUMMY	-10745	-279	57	DB3	-7245	-279	107	VCOM	-3745	-279	157	DDVDH	-245	-279	207	C13A	3255	-279
8	DUMMY	-10675	-279	58	DB2	-7175	-279	108	VCOM	-3675	-279	158	DDVDH	-175	-279	208	C13A	3325	-279
9	DUMMY	-10605	-279	59	DB1	-7105	-279	109	VCOM	-3605	-279	159	DDVDH	-105	-279	209	C13A	3395	-279
10	DUMMY	-10535	-279	60	DB0	-7035	-279	110	VCOM	-3535	-279	160	DDVDH	-35	-279	210	C13A	3465	-279
11	DUMMY	-10465	-279	61	DOUT	-6965	-279	111	VCOM	-3465	-279	161	DDVDH	35	-279	211	C13A	3535	-279
12	DUMMY	-10395	-279	62	DIN/SDA	-6895	-279	112	VCOM	-3395	-279	162	DDVDH	105	-279	212	C13A	3605	-279
13	MIPI LDO	-10325	-279	63	RDX	-6825	-279	113	VCOM	-3325	-279	163	VCL	175	-279	213	C13A	3675	-279
14	MIPI LDO	-10255	-279	64	WRX/SCL	-6755	-279	114	VCOM	-3255	-279	164	VCL	245	-279	214	C13A	3745	-279
15	DUMMY	-10185	-279	65	D/CX	-6685	-279	115	VCOM	-3185	-279	165	VCL	315	-279	215	C13A	3815	-279
16	MIPI DATA N	-10115	-279	66	CSX	-6615	-279	116	VCOM	-3115	-279	166	VCL	385	-279	216	C15B	3885	-279
17	MIPI DATA N	-10045	-279	67	TE	-6545	-279	117	VCOM	-3045	-279	167	VCL	455	-279	217	C15B	3955	-279
18	MIPI DATA P	-9975	-279	68	IOVCC	-6475	-279	118	VCOM	-2975	-279	168	VCL	525	-279	218	C15B	4025	-279
19	MIPI DATA P	-9905	-279	69	IOVCC	-6405	-279	119	VCOM	-2905	-279	169	VCL	595	-279	219	C15B	4095	-279
20	MIPI CLOCK N	-9835	-279	70	IOVCC	-6335	-279	120	VCOM	-2835	-279	170	VCL	665	-279	220	C15B	4165	-279
21	MIPI CLOCK N	-9765	-279	71	IOVCC	-6265	-279	121	VCOM	-2765	-279	171	VCL	735	-279	221	C15B	4235	-279
22	MIPI CLOCK P	-9695	-279	72	IOVCC	-6195	-279	122	VCOM	-2695	-279	172	VCL	805	-279	222	C15B	4305	-279
23	MIPI CLOCK P	-9625	-279	73	IOVCC	-6125	-279	123	VREG1OUT	-2625	-279	173	VCL	875	-279	223	C15B	4375	-279
24	TS0	-9555	-279	74	IOVCC	-6055	-279	124	VREG1OUT	-2555	-279	174	VCI	945	-279	224	C15B	4445	-279
25	TS1	-9485	-279	75	VDD	-5985	-279	125	VREG1OUT	-2485	-279	175	VCI	1015	-279	225	C15B	4515	-279
26	TS2	-9415	-279	76	VDD	-5915	-279	126	VREG1OUT	-2415	-279	176	VCI	1085	-279	226	C15A	4585	-279
27	TEST0	-9345	-279	77	VDD	-5845	-279	127	VREG1OUT	-2345	-279	177	VCI	1155	-279	227	C15A	4655	-279
28	TEST1	-9275	-279	78	VDD	-5775	-279	128	VREG1OUT	-2275	-279	178	VCI	1225	-279	228	C15A	4725	-279
29	TEST2	-9205	-279	79	VDD	-5705	-279	129	VREG1OUT	-2205	-279	179	VCI	1295	-279	229	C15A	4795	-279
30	TEST3	-9135	-279	80	VDD	-5635	-279	130	VREG1OUT	-2135	-279	180	VCI	1365	-279	230	C15A	4865	-279
31	TEST4	-9065	-279	81	VDD	-5565	-279	131	VREG1OUT	-2065	-279	181	VCI	1435	-279	231	C15A	4935	-279
32	TEST5	-8995	-279	82	VDD	-5495	-279	132	VREG1OUT	-1995	-279	182	VCI	1505	-279	232	C15A	5005	-279
33	CABC_ON	-8925	-279	83	VDD	-5425	-279	133	VREG2OUT	-1925	-279	183	VCI	1575	-279	233	C15A	5075	-279
34	CABC_PWM	-8855	-279	84	VDD	-5355	-279	134	VREG2OUT	-1855	-279	184	VCI	1645	-279	234	C15A	5145	-279
35	IM0/ID	-8785	-279	85	VDD	-5285	-279	135	VREG2OUT	-1785	-279	185	VCI	1715	-279	235	C15A	5215	-279
36	IM1	-8715	-279	86	AGND	-5215	-279	136	VREG2OUT	-1715	-279	186	VCI	1785	-279	236	VGL	5285	-279
37	IM2	-8645	-279	87	AGND	-5145	-279	137	VREG2OUT	-1645	-279	187	VCI	1855	-279	237	VGL	5355	-279
38	RESX	-8575	-279	88	AGND	-5075	-279	138	VREG2OUT	-1575	-279	188	VCI	1925	-279	238	VGL	5425	-279
39	VSXNC	-8505	-279	89	AGND	-5005	-279	139	VREG2OUT	-1505	-279	189	VCI	1995	-279	239	VGL	5495	-279
40	HSXNC	-8435	-279	90	AGND	-4935	-279	140	N_VCORE	-1435	-279	190	VCI	2065	-279	240	VGL	5565	-279
41	DOTCLK	-8365	-279	91	AGND	-4865	-279	141	N_VCORE	-1365	-279	191	VCI	2135	-279	241	VGL	5635	-279
42	ENABLE	-8295	-279	92	AGND	-4795	-279	142	N_VCORE	-1295	-279	192	VCI	2205	-279	242	VGL	5705	-279
43	DB17	-8225	-279	93	AGND	-4725	-279	143	N_VCORE	-1225	-279	193	DUMMY	2275	-279	243	VGL	5775	-279
44	DB16	-8155	-279	94	VGS	-4655	-279	144	DUMMY	-1155	-279	194	C13B	2345	-279	244	VGL	5845	-279
45	DB15	-8085	-279	95	VGS	-4585	-279	145	DDVDL	-1085	-279	195	C13B	2415	-279	245	VGL	5915	-279
46	DB14	-8015	-279	96	DUMMY	-4515	-279	146	DDVDL	-1015	-279	196	C13B	2485	-279	246	AGND	5985	-279
47	DB13	-7945	-279	97	AGND	-4445	-279	147	DDVDL	-945	-279	197	C13B	2555	-279	247	AGND	6055	-279
48	DB12	-7875	-279	98	AGND	-4375	-279	148	DDVDL	-875	-279	198	C13B	2625	-279	248	AGND	6125	-279
49	DB11	-7805	-279	99	AGND	-4305	-279	149	DDVDL	-805	-279	199	C13B	2695	-279	249	VGH	6195	-279
50	DB10	-7735	-279	100	AGND	-4235	-279	150	DDVDL	-735	-279	200	C13B	2765	-279	250	VGH	6265	-279

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
251	VGH	6335	-279	301	C22B	9835	-279	351	G57	10755	164	401	G157	10005	164	451	G257	9255	164
252	VGH	6405	-279	302	C22B	9905	-279	352	G59	10740	289	402	G159	9990	289	452	G259	9240	289
253	VGH	6475	-279	303	C22B	9975	-279	353	G61	10725	164	403	G161	9975	164	453	G261	9225	164
254	VGH	6545	-279	304	C22B	10045	-279	354	G63	10710	289	404	G163	9960	289	454	G263	9210	289
255	VGH	6615	-279	305	C22B	10115	-279	355	G65	10695	164	405	G165	9945	164	455	G265	9195	164
256	VGH	6685	-279	306	C22B	10185	-279	356	G67	10680	289	406	G167	9930	289	456	G267	9180	289
257	C11B	6755	-279	307	C22B	10255	-279	357	G69	10665	164	407	G169	9915	164	457	G269	9165	164
258	C11B	6825	-279	308	C22A	10325	-279	358	G71	10650	289	408	G171	9900	289	458	G271	9150	289
259	C11B	6895	-279	309	C22A	10395	-279	359	G73	10635	164	409	G173	9885	164	459	G273	9135	164
260	C11B	6965	-279	310	C22A	10465	-279	360	G75	10620	289	410	G175	9870	289	460	G275	9120	289
261	C11B	7035	-279	311	C22A	10535	-279	361	G77	10605	164	411	G177	9855	164	461	G277	9105	164
262	C11B	7105	-279	312	C22A	10605	-279	362	G79	10590	289	412	G179	9840	289	462	G279	9090	289
263	C11A	7175	-279	313	C22A	10675	-279	363	G81	10575	164	413	G181	9825	164	463	G281	9075	164
264	C11A	7245	-279	314	C22A	10745	-279	364	G83	10560	289	414	G183	9810	289	464	G283	9060	289
265	C11A	7315	-279	315	C22A	10815	-279	365	G85	10545	164	415	G185	9795	164	465	G285	9045	164
266	C11A	7385	-279	316	C22A	10885	-279	366	G87	10530	289	416	G187	9780	289	466	G287	9030	289
267	C11A	7455	-279	317	C22A	10955	-279	367	G89	10515	164	417	G189	9765	164	467	G289	9015	164
268	C11A	7525	-279	318	C22A	11025	-279	368	G91	10500	289	418	G191	9750	289	468	G291	9000	289
269	C21B	7595	-279	319	C22A	11095	-279	369	G93	10485	164	419	G193	9735	164	469	G293	8985	164
270	C21B	7665	-279	320	C22A	11165	-279	370	G95	10470	289	420	G195	9720	289	470	G295	8970	289
271	C21B	7735	-279	321	DUMMY	11205	164	371	G97	10455	164	421	G197	9705	164	471	G297	8955	164
272	C21B	7805	-279	322	DUMMY	11190	289	372	G99	10440	289	422	G199	9690	289	472	G299	8940	289
273	C21B	7875	-279	323	G1	11175	164	373	G101	10425	164	423	G201	9675	164	473	G301	8925	164
274	C21B	7945	-279	324	G3	11160	289	374	G103	10410	289	424	G203	9660	289	474	G303	8910	289
275	C21B	8015	-279	325	G5	11145	164	375	G105	10395	164	425	G205	9645	164	475	G305	8895	164
276	C21B	8085	-279	326	G7	11130	289	376	G107	10380	289	426	G207	9630	289	476	G307	8880	289
277	C21B	8155	-279	327	G9	11115	164	377	G109	10365	164	427	G209	9615	164	477	G309	8865	164
278	C21B	8225	-279	328	G11	11100	289	378	G111	10350	289	428	G211	9600	289	478	G311	8850	289
279	C21B	8295	-279	329	G13	11085	164	379	G113	10335	164	429	G213	9585	164	479	G313	8835	164
280	C21B	8365	-279	330	G15	11070	289	380	G115	10320	289	430	G215	9570	289	480	G315	8820	289
281	C21B	8435	-279	331	G17	11055	164	381	G117	10305	164	431	G217	9555	164	481	G317	8805	164
282	C21B	8505	-279	332	G19	11040	289	382	G119	10290	289	432	G219	9540	289	482	G319	8790	289
283	C21A	8575	-279	333	G21	11025	164	383	G121	10275	164	433	G221	9525	164	483	G321	8775	164
284	C21A	8645	-279	334	G23	11010	289	384	G123	10260	289	434	G223	9510	289	484	G323	8760	289
285	C21A	8715	-279	335	G25	10995	164	385	G125	10245	164	435	G225	9495	164	485	G325	8745	164
286	C21A	8785	-279	336	G27	10980	289	386	G127	10230	289	436	G227	9480	289	486	G327	8730	289
287	C21A	8855	-279	337	G29	10965	164	387	G129	10215	164	437	G229	9465	164	487	G329	8715	164
288	C21A	8925	-279	338	G31	10950	289	388	G131	10200	289	438	G231	9450	289	488	G331	8700	289
289	C21A	8995	-279	339	G33	10935	164	389	G133	10185	164	439	G233	9435	164	489	G333	8685	164
290	C21A	9065	-279	340	G35	10920	289	390	G135	10170	289	440	G235	9420	289	490	G335	8670	289
291	C21A	9135	-279	341	G37	10905	164	391	G137	10155	164	441	G237	9405	164	491	G337	8655	164
292	C21A	9205	-279	342	G39	10890	289	392	G139	10140	289	442	G239	9390	289	492	G339	8640	289
293	C21A	9275	-279	343	G41	10875	164	393	G141	10125	164	443	G241	9375	164	493	G341	8625	164
294	C21A	9345	-279	344	G43	10860	289	394	G143	10110	289	444	G243	9360	289	494	G343	8610	289
295	C21A	9415	-279	345	G45	10845	164	395	G145	10095	164	445	G245	9345	164	495	G345	8595	164
296	C22B	9485	-279	346	G47	10830	289	396	G147	10080	289	446	G247	9330	289	496	G347	8580	289
297	C22B	9555	-279	347	G49	10815	164	397	G149	10065	164	447	G249	9315	164	497	G349	8565	164
298	C22B	9625	-279	348	G51	10800	289	398	G151	10050	289	448	G251	9300	289	498	G351	8550	289
299	C22B	9695	-279	349	G53	10785	164	399	G153	10035	164	449	G253	9285	164	499	G353	8535	164
300	C22B	9765	-279	350	G55	10770	289	400	G155	10020	289	450	G255	9270	289	500	G355	8520	289

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
501	G357	8505	164	551	G457	7755	164	601	S926	6855	164	651	S876	6105	164	701	S826	5355	164
502	G359	8490	289	552	G459	7740	289	602	S925	6840	289	652	S875	6090	289	702	S825	5340	289
503	G361	8475	164	553	G461	7725	164	603	S924	6825	164	653	S874	6075	164	703	S824	5325	164
504	G363	8460	289	554	G463	7710	289	604	S923	6810	289	654	S873	6060	289	704	S823	5310	289
505	G365	8445	164	555	G465	7695	164	605	S922	6795	164	655	S872	6045	164	705	S822	5295	164
506	G367	8430	289	556	G467	7680	289	606	S921	6780	289	656	S871	6030	289	706	S821	5280	289
507	G369	8415	164	557	G469	7665	164	607	S920	6765	164	657	S870	6015	164	707	S820	5265	164
508	G371	8400	289	558	G471	7650	289	608	S919	6750	289	658	S869	6000	289	708	S819	5250	289
509	G373	8385	164	559	G473	7635	164	609	S918	6735	164	659	S868	5985	164	709	S818	5235	164
510	G375	8370	289	560	G475	7620	289	610	S917	6720	289	660	S867	5970	289	710	S817	5220	289
511	G377	8355	164	561	G477	7605	164	611	S916	6705	164	661	S866	5955	164	711	S816	5205	164
512	G379	8340	289	562	G479	7590	289	612	S915	6690	289	662	S865	5940	289	712	S815	5190	289
513	G381	8325	164	563	DUMMY	7575	164	613	S914	6675	164	663	S864	5925	164	713	S814	5175	164
514	G383	8310	289	564	DUMMY	7560	289	614	S913	6660	289	664	S863	5910	289	714	S813	5160	289
515	G385	8295	164	565	DUMMY	7395	164	615	S912	6645	164	665	S862	5895	164	715	S812	5145	164
516	G387	8280	289	566	S961	7380	289	616	S911	6630	289	666	S861	5880	289	716	S811	5130	289
517	G389	8265	164	567	S960	7365	164	617	S910	6615	164	667	S860	5865	164	717	S810	5115	164
518	G391	8250	289	568	S959	7350	289	618	S909	6600	289	668	S859	5850	289	718	S809	5100	289
519	G393	8235	164	569	S958	7335	164	619	S908	6585	164	669	S858	5835	164	719	S808	5085	164
520	G395	8220	289	570	S957	7320	289	620	S907	6570	289	670	S857	5820	289	720	S807	5070	289
521	G397	8205	164	571	S956	7305	164	621	S906	6555	164	671	S856	5805	164	721	S806	5055	164
522	G399	8190	289	572	S955	7290	289	622	S905	6540	289	672	S855	5790	289	722	S805	5040	289
523	G401	8175	164	573	S954	7275	164	623	S904	6525	164	673	S854	5775	164	723	S804	5025	164
524	G403	8160	289	574	S953	7260	289	624	S903	6510	289	674	S853	5760	289	724	S803	5010	289
525	G405	8145	164	575	S952	7245	164	625	S902	6495	164	675	S852	5745	164	725	S802	4995	164
526	G407	8130	289	576	S951	7230	289	626	S901	6480	289	676	S851	5730	289	726	S801	4980	289
527	G409	8115	164	577	S950	7215	164	627	S900	6465	164	677	S850	5715	164	727	S800	4965	164
528	G411	8100	289	578	S949	7200	289	628	S899	6450	289	678	S849	5700	289	728	S799	4950	289
529	G413	8085	164	579	S948	7185	164	629	S898	6435	164	679	S848	5685	164	729	S798	4935	164
530	G415	8070	289	580	S947	7170	289	630	S897	6420	289	680	S847	5670	289	730	S797	4920	289
531	G417	8055	164	581	S946	7155	164	631	S896	6405	164	681	S846	5655	164	731	S796	4905	164
532	G419	8040	289	582	S945	7140	289	632	S895	6390	289	682	S845	5640	289	732	S795	4890	289
533	G421	8025	164	583	S944	7125	164	633	S894	6375	164	683	S844	5625	164	733	S794	4875	164
534	G423	8010	289	584	S943	7110	289	634	S893	6360	289	684	S843	5610	289	734	S793	4860	289
535	G425	7995	164	585	S942	7095	164	635	S892	6345	164	685	S842	5595	164	735	S792	4845	164
536	G427	7980	289	586	S941	7080	289	636	S891	6330	289	686	S841	5580	289	736	S791	4830	289
537	G429	7965	164	587	S940	7065	164	637	S890	6315	164	687	S840	5565	164	737	S790	4815	164
538	G431	7950	289	588	S939	7050	289	638	S889	6300	289	688	S839	5550	289	738	S789	4800	289
539	G433	7935	164	589	S938	7035	164	639	S888	6285	164	689	S838	5535	164	739	S788	4785	164
540	G435	7920	289	590	S937	7020	289	640	S887	6270	289	690	S837	5520	289	740	S787	4770	289
541	G437	7905	164	591	S936	7005	164	641	S886	6255	164	691	S836	5505	164	741	S786	4755	164
542	G439	7890	289	592	S935	6990	289	642	S885	6240	289	692	S835	5490	289	742	S785	4740	289
543	G441	7875	164	593	S934	6975	164	643	S884	6225	164	693	S834	5475	164	743	S784	4725	164
544	G443	7860	289	594	S933	6960	289	644	S883	6210	289	694	S833	5460	289	744	S783	4710	289
545	G445	7845	164	595	S932	6945	164	645	S882	6195	164	695	S832	5445	164	745	S782	4695	164
546	G447	7830	289	596	S931	6930	289	646	S881	6180	289	696	S831	5430	289	746	S781	4680	289
547	G449	7815	164	597	S930	6915	164	647	S880	6165	164	697	S830	5415	164	747	S780	4665	164
548	G451	7800	289	598	S929	6900	289	648	S879	6150	289	698	S829	5400	289	748	S779	4650	289
549	G453	7785	164	599	S928	6885	164	649	S878	6135	164	699	S828	5385	164	749	S778	4635	164
550	G455	7770	289	600	S927	6870	289	650	S877	6120	289	700	S827	5370	289	750	S777	4620	289

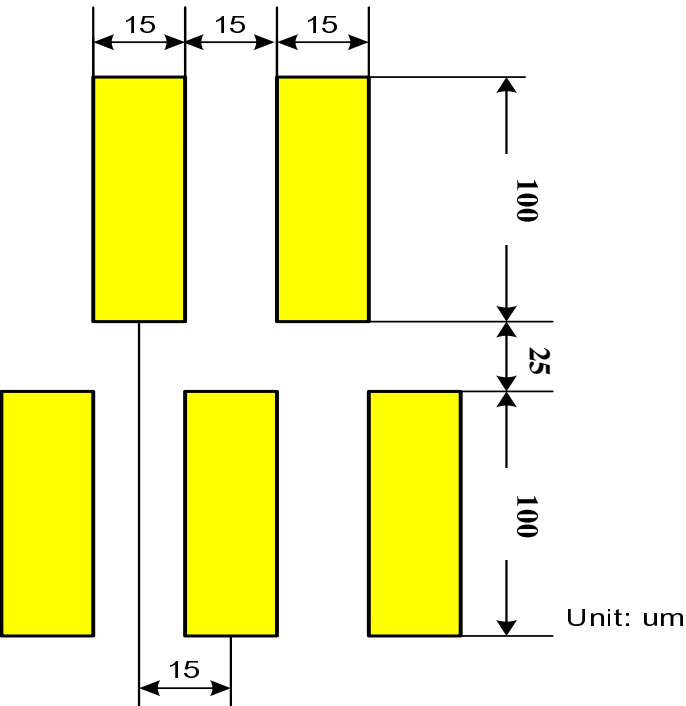
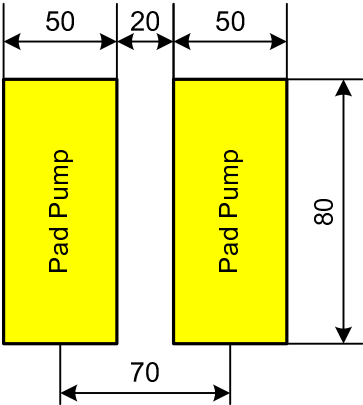
No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
751	S776	4605	164	801	S726	3855	164	851	S676	3105	164	901	S626	2355	164	951	S576	1605	164
752	S775	4590	289	802	S725	3840	289	852	S675	3090	289	902	S625	2340	289	952	S575	1590	289
753	S774	4575	164	803	S724	3825	164	853	S674	3075	164	903	S624	2325	164	953	S574	1575	164
754	S773	4560	289	804	S723	3810	289	854	S673	3060	289	904	S623	2310	289	954	S573	1560	289
755	S772	4545	164	805	S722	3795	164	855	S672	3045	164	905	S622	2295	164	955	S572	1545	164
756	S771	4530	289	806	S721	3780	289	856	S671	3030	289	906	S621	2280	289	956	S571	1530	289
757	S770	4515	164	807	S720	3765	164	857	S670	3015	164	907	S620	2265	164	957	S570	1515	164
758	S769	4500	289	808	S719	3750	289	858	S669	3000	289	908	S619	2250	289	958	S569	1500	289
759	S768	4485	164	809	S718	3735	164	859	S668	2985	164	909	S618	2235	164	959	S568	1485	164
760	S767	4470	289	810	S717	3720	289	860	S667	2970	289	910	S617	2220	289	960	S567	1470	289
761	S766	4455	164	811	S716	3705	164	861	S666	2955	164	911	S616	2205	164	961	S566	1455	164
762	S765	4440	289	812	S715	3690	289	862	S665	2940	289	912	S615	2190	289	962	S565	1440	289
763	S764	4425	164	813	S714	3675	164	863	S664	2925	164	913	S614	2175	164	963	S564	1425	164
764	S763	4410	289	814	S713	3660	289	864	S663	2910	289	914	S613	2160	289	964	S563	1410	289
765	S762	4395	164	815	S712	3645	164	865	S662	2895	164	915	S612	2145	164	965	S562	1395	164
766	S761	4380	289	816	S711	3630	289	866	S661	2880	289	916	S611	2130	289	966	S561	1380	289
767	S760	4365	164	817	S710	3615	164	867	S660	2865	164	917	S610	2115	164	967	S560	1365	164
768	S759	4350	289	818	S709	3600	289	868	S659	2850	289	918	S609	2100	289	968	S559	1350	289
769	S758	4335	164	819	S708	3585	164	869	S658	2835	164	919	S608	2085	164	969	S558	1335	164
770	S757	4320	289	820	S707	3570	289	870	S657	2820	289	920	S607	2070	289	970	S557	1320	289
771	S756	4305	164	821	S706	3555	164	871	S656	2805	164	921	S606	2055	164	971	S556	1305	164
772	S755	4290	289	822	S705	3540	289	872	S655	2790	289	922	S605	2040	289	972	S555	1290	289
773	S754	4275	164	823	S704	3525	164	873	S654	2775	164	923	S604	2025	164	973	S554	1275	164
774	S753	4260	289	824	S703	3510	289	874	S653	2760	289	924	S603	2010	289	974	S553	1260	289
775	S752	4245	164	825	S702	3495	164	875	S652	2745	164	925	S602	1995	164	975	S552	1245	164
776	S751	4230	289	826	S701	3480	289	876	S651	2730	289	926	S601	1980	289	976	S551	1230	289
777	S750	4215	164	827	S700	3465	164	877	S650	2715	164	927	S600	1965	164	977	S550	1215	164
778	S749	4200	289	828	S699	3450	289	878	S649	2700	289	928	S599	1950	289	978	S549	1200	289
779	S748	4185	164	829	S698	3435	164	879	S648	2685	164	929	S598	1935	164	979	S548	1185	164
780	S747	4170	289	830	S697	3420	289	880	S647	2670	289	930	S597	1920	289	980	S547	1170	289
781	S746	4155	164	831	S696	3405	164	881	S646	2655	164	931	S596	1905	164	981	S546	1155	164
782	S745	4140	289	832	S695	3390	289	882	S645	2640	289	932	S595	1890	289	982	S545	1140	289
783	S744	4125	164	833	S694	3375	164	883	S644	2625	164	933	S594	1875	164	983	S544	1125	164
784	S743	4110	289	834	S693	3360	289	884	S643	2610	289	934	S593	1860	289	984	S543	1110	289
785	S742	4095	164	835	S692	3345	164	885	S642	2595	164	935	S592	1845	164	985	S542	1095	164
786	S741	4080	289	836	S691	3330	289	886	S641	2580	289	936	S591	1830	289	986	S541	1080	289
787	S740	4065	164	837	S690	3315	164	887	S640	2565	164	937	S590	1815	164	987	S540	1065	164
788	S739	4050	289	838	S689	3300	289	888	S639	2550	289	938	S589	1800	289	988	S539	1050	289
789	S738	4035	164	839	S688	3285	164	889	S638	2535	164	939	S588	1785	164	989	S538	1035	164
790	S737	4020	289	840	S687	3270	289	890	S637	2520	289	940	S587	1770	289	990	S537	1020	289
791	S736	4005	164	841	S686	3255	164	891	S636	2505	164	941	S586	1755	164	991	S536	1005	164
792	S735	3990	289	842	S685	3240	289	892	S635	2490	289	942	S585	1740	289	992	S535	990	289
793	S734	3975	164	843	S684	3225	164	893	S634	2475	164	943	S584	1725	164	993	S534	975	164
794	S733	3960	289	844	S683	3210	289	894	S633	2460	289	944	S583	1710	289	994	S533	960	289
795	S732	3945	164	845	S682	3195	164	895	S632	2445	164	945	S582	1695	164	995	S532	945	164
796	S731	3930	289	846	S681	3180	289	896	S631	2430	289	946	S581	1680	289	996	S531	930	289
797	S730	3915	164	847	S680	3165	164	897	S630	2415	164	947	S580	1665	164	997	S530	915	164
798	S729	3900	289	848	S679	3150	289	898	S629	2400	289	948	S579	1650	289	998	S529	900	289
799	S728	3885	164	849	S678	3135	164	899	S628	2385	164	949	S578	1635	164	999	S528	885	164
800	S727	3870	289	850	S677	3120	289	900	S627	2370	289	950	S577	1620	289	1000	S527	870	289

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
1001	S526	855	164	1051	S480	-180	289	1101	S430	-930	289	1151	S380	-1680	289	1201	S330	-2430	289
1002	S525	840	289	1052	S479	-195	164	1102	S429	-945	164	1152	S379	-1695	164	1202	S329	-2445	164
1003	S524	825	164	1053	S478	-210	289	1103	S428	-960	289	1153	S378	-1710	289	1203	S328	-2460	289
1004	S523	810	289	1054	S477	-225	164	1104	S427	-975	164	1154	S377	-1725	164	1204	S327	-2475	164
1005	S522	795	164	1055	S476	-240	289	1105	S426	-990	289	1155	S376	-1740	289	1205	S326	-2490	289
1006	S521	780	289	1056	S475	-255	164	1106	S425	-1005	164	1156	S375	-1755	164	1206	S325	-2505	164
1007	S520	765	164	1057	S474	-270	289	1107	S424	-1020	289	1157	S374	-1770	289	1207	S324	-2520	289
1008	S519	750	289	1058	S473	-285	164	1108	S423	-1035	164	1158	S373	-1785	164	1208	S323	-2535	164
1009	S518	735	164	1059	S472	-300	289	1109	S422	-1050	289	1159	S372	-1800	289	1209	S322	-2550	289
1010	S517	720	289	1060	S471	-315	164	1110	S421	-1065	164	1160	S371	-1815	164	1210	S321	-2565	164
1011	S516	705	164	1061	S470	-330	289	1111	S420	-1080	289	1161	S370	-1830	289	1211	S320	-2580	289
1012	S515	690	289	1062	S469	-345	164	1112	S419	-1095	164	1162	S369	-1845	164	1212	S319	-2595	164
1013	S514	675	164	1063	S468	-360	289	1113	S418	-1110	289	1163	S368	-1860	289	1213	S318	-2610	289
1014	S513	660	289	1064	S467	-375	164	1114	S417	-1125	164	1164	S367	-1875	164	1214	S317	-2625	164
1015	S512	645	164	1065	S466	-390	289	1115	S416	-1140	289	1165	S366	-1890	289	1215	S316	-2640	289
1016	S511	630	289	1066	S465	-405	164	1116	S415	-1155	164	1166	S365	-1905	164	1216	S315	-2655	164
1017	S510	615	164	1067	S464	-420	289	1117	S414	-1170	289	1167	S364	-1920	289	1217	S314	-2670	289
1018	S509	600	289	1068	S463	-435	164	1118	S413	-1185	164	1168	S363	-1935	164	1218	S313	-2685	164
1019	S508	585	164	1069	S462	-450	289	1119	S412	-1200	289	1169	S362	-1950	289	1219	S312	-2700	289
1020	S507	570	289	1070	S461	-465	164	1120	S411	-1215	164	1170	S361	-1965	164	1220	S311	-2715	164
1021	S506	555	164	1071	S460	-480	289	1121	S410	-1230	289	1171	S360	-1980	289	1221	S310	-2730	289
1022	S505	540	289	1072	S459	-495	164	1122	S409	-1245	164	1172	S359	-1995	164	1222	S309	-2745	164
1023	S504	525	164	1073	S458	-510	289	1123	S408	-1260	289	1173	S358	-2010	289	1223	S308	-2760	289
1024	S503	510	289	1074	S457	-525	164	1124	S407	-1275	164	1174	S357	-2025	164	1224	S307	-2775	164
1025	S502	495	164	1075	S456	-540	289	1125	S406	-1290	289	1175	S356	-2040	289	1225	S306	-2790	289
1026	S501	480	289	1076	S455	-555	164	1126	S405	-1305	164	1176	S355	-2055	164	1226	S305	-2805	164
1027	S500	465	164	1077	S454	-570	289	1127	S404	-1320	289	1177	S354	-2070	289	1227	S304	-2820	289
1028	S499	450	289	1078	S453	-585	164	1128	S403	-1335	164	1178	S353	-2085	164	1228	S303	-2835	164
1029	S498	435	164	1079	S452	-600	289	1129	S402	-1350	289	1179	S352	-2100	289	1229	S302	-2850	289
1030	S497	420	289	1080	S451	-615	164	1130	S401	-1365	164	1180	S351	-2115	164	1230	S301	-2865	164
1031	S496	405	164	1081	S450	-630	289	1131	S400	-1380	289	1181	S350	-2130	289	1231	S300	-2880	289
1032	S495	390	289	1082	S449	-645	164	1132	S399	-1395	164	1182	S349	-2145	164	1232	S299	-2895	164
1033	S494	375	164	1083	S448	-660	289	1133	S398	-1410	289	1183	S348	-2160	289	1233	S298	-2910	289
1034	S493	360	289	1084	S447	-675	164	1134	S397	-1425	164	1184	S347	-2175	164	1234	S297	-2925	164
1035	S492	345	164	1085	S446	-690	289	1135	S396	-1440	289	1185	S346	-2190	289	1235	S296	-2940	289
1036	S491	330	289	1086	S445	-705	164	1136	S395	-1455	164	1186	S345	-2205	164	1236	S295	-2955	164
1037	S490	315	164	1087	S444	-720	289	1137	S394	-1470	289	1187	S344	-2220	289	1237	S294	-2970	289
1038	S489	300	289	1088	S443	-735	164	1138	S393	-1485	164	1188	S343	-2235	164	1238	S293	-2985	164
1039	S488	285	164	1089	S442	-750	289	1139	S392	-1500	289	1189	S342	-2250	289	1239	S292	-3000	289
1040	S487	270	289	1090	S441	-765	164	1140	S391	-1515	164	1190	S341	-2265	164	1240	S291	-3015	164
1041	S486	255	164	1091	S440	-780	289	1141	S390	-1530	289	1191	S340	-2280	289	1241	S290	-3030	289
1042	S485	240	289	1092	S439	-795	164	1142	S389	-1545	164	1192	S339	-2295	164	1242	S289	-3045	164
1043	S484	225	164	1093	S438	-810	289	1143	S388	-1560	289	1193	S338	-2310	289	1243	S288	-3060	289
1044	S483	210	289	1094	S437	-825	164	1144	S387	-1575	164	1194	S337	-2325	164	1244	S287	-3075	164
1045	S482	195	164	1095	S436	-840	289	1145	S386	-1590	289	1195	S336	-2340	289	1245	S286	-3090	289
1046	S481	180	289	1096	S435	-855	164	1146	S385	-1605	164	1196	S335	-2355	164	1246	S285	-3105	164
1047	V1T	165	164	1097	S434	-870	289	1147	S384	-1620	289	1197	S334	-2370	289	1247	S284	-3120	289
1048	DUMMY	150	289	1098	S433	-885	164	1148	S383	-1635	164	1198	S333	-2385	164	1248	S283	-3135	164
1049	DUMMY	-150	289	1099	S432	-900	289	1149	S382	-1650	289	1199	S332	-2400	289	1249	S282	-3150	289
1050	V62T	-165	164	1100	S431	-915	164	1150	S381	-1665	164	1200	S331	-2415	164	1250	S281	-3165	164

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
1251	S280	-3180	289	1301	S230	-3930	289	1351	S180	-4680	289	1401	S130	-5430	289	1451	S80	-6180	289
1252	S279	-3195	164	1302	S229	-3945	164	1352	S179	-4695	164	1402	S129	-5445	164	1452	S79	-6195	164
1253	S278	-3210	289	1303	S228	-3960	289	1353	S178	-4710	289	1403	S128	-5460	289	1453	S78	-6210	289
1254	S277	-3225	164	1304	S227	-3975	164	1354	S177	-4725	164	1404	S127	-5475	164	1454	S77	-6225	164
1255	S276	-3240	289	1305	S226	-3990	289	1355	S176	-4740	289	1405	S126	-5490	289	1455	S76	-6240	289
1256	S275	-3255	164	1306	S225	-4005	164	1356	S175	-4755	164	1406	S125	-5505	164	1456	S75	-6255	164
1257	S274	-3270	289	1307	S224	-4020	289	1357	S174	-4770	289	1407	S124	-5520	289	1457	S74	-6270	289
1258	S273	-3285	164	1308	S223	-4035	164	1358	S173	-4785	164	1408	S123	-5535	164	1458	S73	-6285	164
1259	S272	-3300	289	1309	S222	-4050	289	1359	S172	-4800	289	1409	S122	-5550	289	1459	S72	-6300	289
1260	S271	-3315	164	1310	S221	-4065	164	1360	S171	-4815	164	1410	S121	-5565	164	1460	S71	-6315	164
1261	S270	-3330	289	1311	S220	-4080	289	1361	S170	-4830	289	1411	S120	-5580	289	1461	S70	-6330	289
1262	S269	-3345	164	1312	S219	-4095	164	1362	S169	-4845	164	1412	S119	-5595	164	1462	S69	-6345	164
1263	S268	-3360	289	1313	S218	-4110	289	1363	S168	-4860	289	1413	S118	-5610	289	1463	S68	-6360	289
1264	S267	-3375	164	1314	S217	-4125	164	1364	S167	-4875	164	1414	S117	-5625	164	1464	S67	-6375	164
1265	S266	-3390	289	1315	S216	-4140	289	1365	S166	-4890	289	1415	S116	-5640	289	1465	S66	-6390	289
1266	S265	-3405	164	1316	S215	-4155	164	1366	S165	-4905	164	1416	S115	-5655	164	1466	S65	-6405	164
1267	S264	-3420	289	1317	S214	-4170	289	1367	S164	-4920	289	1417	S114	-5670	289	1467	S64	-6420	289
1268	S263	-3435	164	1318	S213	-4185	164	1368	S163	-4935	164	1418	S113	-5685	164	1468	S63	-6435	164
1269	S262	-3450	289	1319	S212	-4200	289	1369	S162	-4950	289	1419	S112	-5700	289	1469	S62	-6450	289
1270	S261	-3465	164	1320	S211	-4215	164	1370	S161	-4965	164	1420	S111	-5715	164	1470	S61	-6465	164
1271	S260	-3480	289	1321	S210	-4230	289	1371	S160	-4980	289	1421	S110	-5730	289	1471	S60	-6480	289
1272	S259	-3495	164	1322	S209	-4245	164	1372	S159	-4995	164	1422	S109	-5745	164	1472	S59	-6495	164
1273	S258	-3510	289	1323	S208	-4260	289	1373	S158	-5010	289	1423	S108	-5760	289	1473	S58	-6510	289
1274	S257	-3525	164	1324	S207	-4275	164	1374	S157	-5025	164	1424	S107	-5775	164	1474	S57	-6525	164
1275	S256	-3540	289	1325	S206	-4290	289	1375	S156	-5040	289	1425	S106	-5790	289	1475	S56	-6540	289
1276	S255	-3555	164	1326	S205	-4305	164	1376	S155	-5055	164	1426	S105	-5805	164	1476	S55	-6555	164
1277	S254	-3570	289	1327	S204	-4320	289	1377	S154	-5070	289	1427	S104	-5820	289	1477	S54	-6570	289
1278	S253	-3585	164	1328	S203	-4335	164	1378	S153	-5085	164	1428	S103	-5835	164	1478	S53	-6585	164
1279	S252	-3600	289	1329	S202	-4350	289	1379	S152	-5100	289	1429	S102	-5850	289	1479	S52	-6600	289
1280	S251	-3615	164	1330	S201	-4365	164	1380	S151	-5115	164	1430	S101	-5865	164	1480	S51	-6615	164
1281	S250	-3630	289	1331	S200	-4380	289	1381	S150	-5130	289	1431	S100	-5880	289	1481	S50	-6630	289
1282	S249	-3645	164	1332	S199	-4395	164	1382	S149	-5145	164	1432	S99	-5895	164	1482	S49	-6645	164
1283	S248	-3660	289	1333	S198	-4410	289	1383	S148	-5160	289	1433	S98	-5910	289	1483	S48	-6660	289
1284	S247	-3675	164	1334	S197	-4425	164	1384	S147	-5175	164	1434	S97	-5925	164	1484	S47	-6675	164
1285	S246	-3690	289	1335	S196	-4440	289	1385	S146	-5190	289	1435	S96	-5940	289	1485	S46	-6690	289
1286	S245	-3705	164	1336	S195	-4455	164	1386	S145	-5205	164	1436	S95	-5955	164	1486	S45	-6705	164
1287	S244	-3720	289	1337	S194	-4470	289	1387	S144	-5220	289	1437	S94	-5970	289	1487	S44	-6720	289
1288	S243	-3735	164	1338	S193	-4485	164	1388	S143	-5235	164	1438	S93	-5985	164	1488	S43	-6735	164
1289	S242	-3750	289	1339	S192	-4500	289	1389	S142	-5250	289	1439	S92	-6000	289	1489	S42	-6750	289
1290	S241	-3765	164	1340	S191	-4515	164	1390	S141	-5265	164	1440	S91	-6015	164	1490	S41	-6765	164
1291	S240	-3780	289	1341	S190	-4530	289	1391	S140	-5280	289	1441	S90	-6030	289	1491	S40	-6780	289
1292	S239	-3795	164	1342	S189	-4545	164	1392	S139	-5295	164	1442	S89	-6045	164	1492	S39	-6795	164
1293	S238	-3810	289	1343	S188	-4560	289	1393	S138	-5310	289	1443	S88	-6060	289	1493	S38	-6810	289
1294	S237	-3825	164	1344	S187	-4575	164	1394	S137	-5325	164	1444	S87	-6075	164	1494	S37	-6825	164
1295	S236	-3840	289	1345	S186	-4590	289	1395	S136	-5340	289	1445	S86	-6090	289	1495	S36	-6840	289
1296	S235	-3855	164	1346	S185	-4605	164	1396	S135	-5355	164	1446	S85	-6105	164	1496	S35	-6855	164
1297	S234	-3870	289	1347	S184	-4620	289	1397	S134	-5370	289	1447	S84	-6120	289	1497	S34	-6870	289
1298	S233	-3885	164	1348	S183	-4635	164	1398	S133	-5385	164	1448	S83	-6135	164	1498	S33	-6885	164
1299	S232	-3900	289	1349	S182	-4650	289	1399	S132	-5400	289	1449	S82	-6150	289	1499	S32	-6900	289
1300	S231	-3915	164	1350	S181	-4665	164	1400	S131	-5415	164	1450	S81	-6165	164	1500	S31	-6915	164

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
1501	S30	-6930	289	1551	G448	-7830	289	1601	G348	-8580	289	1651	G248	-9330	289	1701	G148	-10080	289
1502	S29	-6945	164	1552	G446	-7845	164	1602	G346	-8595	164	1652	G246	-9345	164	1702	G146	-10095	164
1503	S28	-6960	289	1553	G444	-7860	289	1603	G344	-8610	289	1653	G244	-9360	289	1703	G144	-10110	289
1504	S27	-6975	164	1554	G442	-7875	164	1604	G342	-8625	164	1654	G242	-9375	164	1704	G142	-10125	164
1505	S26	-6990	289	1555	G440	-7890	289	1605	G340	-8640	289	1655	G240	-9390	289	1705	G140	-10140	289
1506	S25	-7005	164	1556	G438	-7905	164	1606	G338	-8655	164	1656	G238	-9405	164	1706	G138	-10155	164
1507	S24	-7020	289	1557	G436	-7920	289	1607	G336	-8670	289	1657	G236	-9420	289	1707	G136	-10170	289
1508	S23	-7035	164	1558	G434	-7935	164	1608	G334	-8685	164	1658	G234	-9435	164	1708	G134	-10185	164
1509	S22	-7050	289	1559	G432	-7950	289	1609	G332	-8700	289	1659	G232	-9450	289	1709	G132	-10200	289
1510	S21	-7065	164	1560	G430	-7965	164	1610	G330	-8715	164	1660	G230	-9465	164	1710	G130	-10215	164
1511	S20	-7080	289	1561	G428	-7980	289	1611	G328	-8730	289	1661	G228	-9480	289	1711	G128	-10230	289
1512	S19	-7095	164	1562	G426	-7995	164	1612	G326	-8745	164	1662	G226	-9495	164	1712	G126	-10245	164
1513	S18	-7110	289	1563	G424	-8010	289	1613	G324	-8760	289	1663	G224	-9510	289	1713	G124	-10260	289
1514	S17	-7125	164	1564	G422	-8025	164	1614	G322	-8775	164	1664	G222	-9525	164	1714	G122	-10275	164
1515	S16	-7140	289	1565	G420	-8040	289	1615	G320	-8790	289	1665	G220	-9540	289	1715	G120	-10290	289
1516	S15	-7155	164	1566	G418	-8055	164	1616	G318	-8805	164	1666	G218	-9555	164	1716	G118	-10305	164
1517	S14	-7170	289	1567	G416	-8070	289	1617	G316	-8820	289	1667	G216	-9570	289	1717	G116	-10320	289
1518	S13	-7185	164	1568	G414	-8085	164	1618	G314	-8835	164	1668	G214	-9585	164	1718	G114	-10335	164
1519	S12	-7200	289	1569	G412	-8100	289	1619	G312	-8850	289	1669	G212	-9600	289	1719	G112	-10350	289
1520	S11	-7215	164	1570	G410	-8115	164	1620	G310	-8865	164	1670	G210	-9615	164	1720	G110	-10365	164
1521	S10	-7230	289	1571	G408	-8130	289	1621	G308	-8880	289	1671	G208	-9630	289	1721	G108	-10380	289
1522	S9	-7245	164	1572	G406	-8145	164	1622	G306	-8895	164	1672	G206	-9645	164	1722	G106	-10395	164
1523	S8	-7260	289	1573	G404	-8160	289	1623	G304	-8910	289	1673	G204	-9660	289	1723	G104	-10410	289
1524	S7	-7275	164	1574	G402	-8175	164	1624	G302	-8925	164	1674	G202	-9675	164	1724	G102	-10425	164
1525	S6	-7290	289	1575	G400	-8190	289	1625	G300	-8940	289	1675	G200	-9690	289	1725	G100	-10440	289
1526	S5	-7305	164	1576	G398	-8205	164	1626	G298	-8955	164	1676	G198	-9705	164	1726	G98	-10455	164
1527	S4	-7320	289	1577	G396	-8220	289	1627	G296	-8970	289	1677	G196	-9720	289	1727	G96	-10470	289
1528	S3	-7335	164	1578	G394	-8235	164	1628	G294	-8985	164	1678	G194	-9735	164	1728	G94	-10485	164
1529	S2	-7350	289	1579	G392	-8250	289	1629	G292	-9000	289	1679	G192	-9750	289	1729	G92	-10500	289
1530	S1	-7365	164	1580	G390	-8265	164	1630	G290	-9015	164	1680	G190	-9765	164	1730	G90	-10515	164
1531	DUMMY	-7380	289	1581	G388	-8280	289	1631	G288	-9030	289	1681	G188	-9780	289	1731	G88	-10530	289
1532	DUMMY	-7395	164	1582	G386	-8295	164	1632	G286	-9045	164	1682	G186	-9795	164	1732	G86	-10545	164
1533	DUMMY	-7560	289	1583	G384	-8310	289	1633	G284	-9060	289	1683	G184	-9810	289	1733	G84	-10560	289
1534	DUMMY	-7575	164	1584	G382	-8325	164	1634	G282	-9075	164	1684	G182	-9825	164	1734	G82	-10575	164
1535	G480	-7590	289	1585	G380	-8340	289	1635	G280	-9090	289	1685	G180	-9840	289	1735	G80	-10590	289
1536	G478	-7605	164	1586	G378	-8355	164	1636	G278	-9105	164	1686	G178	-9855	164	1736	G78	-10605	164
1537	G476	-7620	289	1587	G376	-8370	289	1637	G276	-9120	289	1687	G176	-9870	289	1737	G76	-10620	289
1538	G474	-7635	164	1588	G374	-8385	164	1638	G274	-9135	164	1688	G174	-9885	164	1738	G74	-10635	164
1539	G472	-7650	289	1589	G372	-8400	289	1639	G272	-9150	289	1689	G172	-9900	289	1739	G72	-10650	289
1540	G470	-7665	164	1590	G370	-8415	164	1640	G270	-9165	164	1690	G170	-9915	164	1740	G70	-10665	164
1541	G468	-7680	289	1591	G368	-8430	289	1641	G268	-9180	289	1691	G168	-9930	289	1741	G68	-10680	289
1542	G466	-7695	164	1592	G366	-8445	164	1642	G266	-9195	164	1692	G166	-9945	164	1742	G66	-10695	164
1543	G464	-7710	289	1593	G364	-8460	289	1643	G264	-9210	289	1693	G164	-9960	289	1743	G64	-10710	289
1544	G462	-7725	164	1594	G362	-8475	164	1644	G262	-9225	164	1694	G162	-9975	164	1744	G62	-10725	164
1545	G460	-7740	289	1595	G360	-8490	289	1645	G260	-9240	289	1695	G160	-9990	289	1745	G60	-10740	289
1546	G458	-7755	164	1596	G358	-8505	164	1646	G258	-9255	164	1696	G158	-10005	164	1746	G58	-10755	164
1547	G456	-7770	289	1597	G356	-8520	289	1647	G256	-9270	289	1697	G156	-10020	289	1747	G56	-10770	289
1548	G454	-7785	164	1598	G354	-8535	164	1648	G254	-9285	164	1698	G154	-10035	164	1748	G54	-10785	164
1549	G452	-7800	289	1599	G352	-8550	289	1649	G252	-9300	289	1699	G152	-10050	289	1749	G52	-10800	289
1550	G450	-7815	164	1600	G350	-8565	164	1650	G250	-9315	164	1700	G150	-10065	164	1750	G50	-10815	164

No.	Name	X	Y
1751	G48	-10830	289
1752	G46	-10845	164
1753	G44	-10860	289
1754	G42	-10875	164
1755	G40	-10890	289
1756	G38	-10905	164
1757	G36	-10920	289
1758	G34	-10935	164
1759	G32	-10950	289
1760	G30	-10965	164
1761	G28	-10980	289
1762	G26	-10995	164
1763	G24	-11010	289
1764	G22	-11025	164
1765	G20	-11040	289
1766	G18	-11055	164
1767	G16	-11070	289
1768	G14	-11085	164
1769	G12	-11100	289
1770	G10	-11115	164
1771	G8	-11130	289
1772	G6	-11145	164
1773	G4	-11160	289
1774	G2	-11175	164
1775	DUMMY	-11190	289
1776	DUMMY	-11205	164
Alignment mark -Left		-11300	-270
Alignment mark -Right		11300	-270

<p>S1 ~ S960 G1 ~ G480 (No. 321 ~ 1776)</p>	 <p>Unit: um</p>
<p>I/O pads (No.1 ~ 320)</p>	 <p>Unit: um</p>

6. Block Function Description

MCU System Interface

The ILI9486L supplies four kinds of MCU system interface with 8080-series parallel interface, 3-/4-line serial and RGB interface. The selection of the given interfaces are done by external IM [2:0] pins and shown as below:

IM2	IM1	IM0	Interface	Data Pin in Use
0	0	0	8080 18-bit bus interface	DB[17:0]
0	0	1	8080 9-bit bus interface	DB[8:0]
0	1	0	8080 16-bit bus interface	DB[15:0]
0	1	1	8080 8-bit bus interface	DB[7:0]
1	0	0	Prohibited	-
1	0	1	3-line SPI	SDA
1	1	0	Prohibited	
1	1	1	4-line SPI	SDA

ILI9486L has a 16-bit index register (IR), a 18-bit write-data register (WDR), and an 18-bit read-data register (RDR). The IR is the register to store index information from control registers and the internal GRAM. The WDR is the register to temporarily store data to be written to control registers and the internal GRAM. The RDR is the register to temporarily store data read from the GRAM. Data from the MPU to be written to the internal GRAM are first written to the WDR and then automatically written to the internal GRAM in internal operation. Data are read via the RDR from the internal GRAM. Therefore, invalid data are read out to the data bus when the ILI9486L read the first data from the internal GRAM. Valid data are read out after the ILI9486L performs the second read operation.

Register are written consecutively as the register execution time except starting oscillator takes 0 clock cycle.

8080-Series			Operation
D/CX	RDX	WRX	
"L"	"H"		Write command
"H"		"H"	Read parameter
"H"	"H"		Write parameter

Address Counter (AC)

The address counter (AC) gives an address to the internal GRAM. When the index of the register for setting a RAM address in the AC is written to the IR, the address information is sent from the IR to the AC. As writing data to the internal GRAM, the address in the AC is automatically updated plus or minus 1. The window address

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function enables writing data only in the rectangular area arbitrarily set by users on the GRAM.

Graphic RAM (GRAM)

The GRAM is graphics RAM storing bit-pattern data of 345,600 bytes with 18 bits per pixel, enabling a maximum 320(RGB) x480 dot graphic display.

Grayscale Voltage Generating Circuit

Grayscale voltage generating circuit generates a liquid crystal drive voltage, which corresponds to grayscale level set in the Gamma correction register. The ILI9486L can display 262k colors at the maximum.

Power Supply Circuit

The LCD drive power supply circuit generates the voltage levels as VREG1OUT, VGH, VGL and VCOM for driving TFT LCD panel.

Timing Generating

The timing generator generates timing signals for internal circuits such as the internal GRAM. The timing for display operation such as RAM read operation and the timing for internal operation such as RAM access by MPU is outputted separately so that they do not interfere with each other.

Oscillator

The ILI9486L incorporates RC oscillator circuit. The frame frequency is changeable by command settings.

Panel Driver Circuit

The liquid crystal display driver circuit consists of a 960-output source drivers (S1~S960) and a 480-output gate driver (G1~G480).

7. Function Description

7.1. MCU interfaces

ILI9486L provides the 18-/16-/9-/8-bit parallel system interface for 8080 series, and 3-/4-line serial system interface for serial data input. The input system interface is selected by external pins as IM [2:0] and the bit format per pixel color order is selected by DBI [2:0] bits.

7.1.1. MCU interface selection

The selection of a given interfaces are done by setting external pins IM [2:0] as show in the following table.

IM2	IM1	IM0	Interface	Data Pin in Use
0	0	0	8080 18-bit bus interface	DB[17:0]
0	0	1	8080 9-bit bus interface	DB[8:0]
0	1	0	8080 16-bit bus interface	DB[15:0]
0	1	1	8080 8-bit bus interface	DB[7:0]
1	0	0	Prohibited	-
1	0	1	3-line SPI	SDA
1	1	0	Prohibited	-
1	1	1	4-line SPI	SDA

7.1.2. 8080-Series Parallel Interface

ILI9486L can be accessed via 8-/9-/16-/18-bit MCU 8080-series parallel interface. The chip-select CSX (active low) is used to enable or disable ILI9486L chip. The RESX (active low) is an external reset signal. WRX is the parallel data write strobe, RDX is the parallel data read strobe and DB[17:0] is parallel data bus.

The MCU latches the input data at the rising edge of WRX signal. The D/CX is the signal of data/command selection. When D/CX='1', DB[17:0] bits are display RAM data or command parameters. When D/CX='0', DB[17:0] bits are commands.

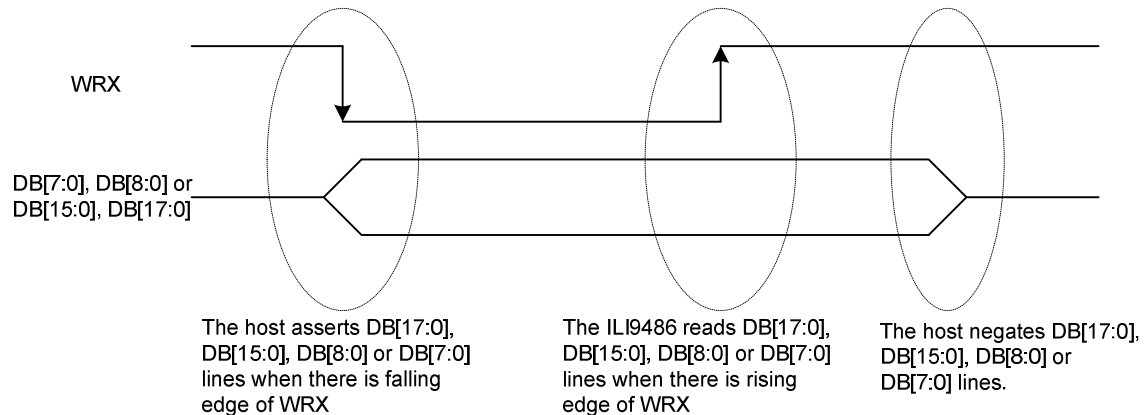
The 8080-series bi-directional interface can be used for communication between the MCU controller and LCD driver chip. The selection of 8080-series parallel interface is shown as the table in the following.

IM2	IM1	IM0	MPU-Interface Mode	WRX	RDX	D/CX	Function
0	0	0	8080 MCU 18-bit bus interface		"H"	"L"	Write command code.
				"H"		"H"	Read internal status.
					"H"	"H"	Write parameter or display data.
				"H"		"H"	Reads parameter or display data.
0	0	1	8080 MCU 9-bit bus interface		"H"	"L"	Write command code.
				"H"		"H"	Read internal status.
					"H"	"H"	Write parameter or display data.
				"H"		"H"	Reads parameter or display data.
0	1	0	8080 MCU 16-bit bus interface		"H"	"L"	Write command code.
				"H"		"H"	Read internal status.
					"H"	"H"	Write parameter or display data.
				"H"		"H"	Reads parameter or display data.
0	1	1	8080 MCU 8-bit bus interface		"H"	"L"	Write command code.
				"H"		"H"	Read internal status.
					"H"	"H"	Write parameter or display data.
				"H"		"H"	Reads parameter or display data.

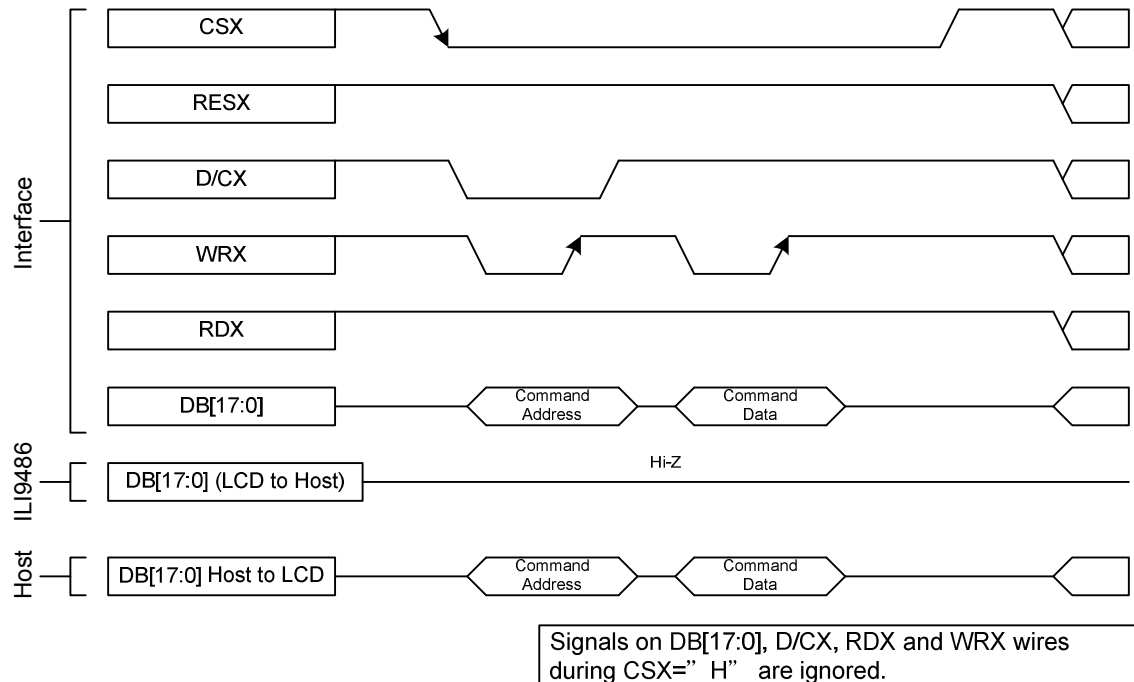
7.1.2.1. Write Cycle Sequence

The WRX signal is driven from high to low then pulled back to high during the write cycle. The host processor provides information during the write cycle when the display module captures the information from host processor on the rising edge of WRX. When the D/CX signal is driven to low level, then input data on the interface is interpreted as command information. The D/CX signal also can be pulled high level when the data on the interface is RAM data or command parameter.

The following figure shows a write cycle for the 8080 MCU interface.



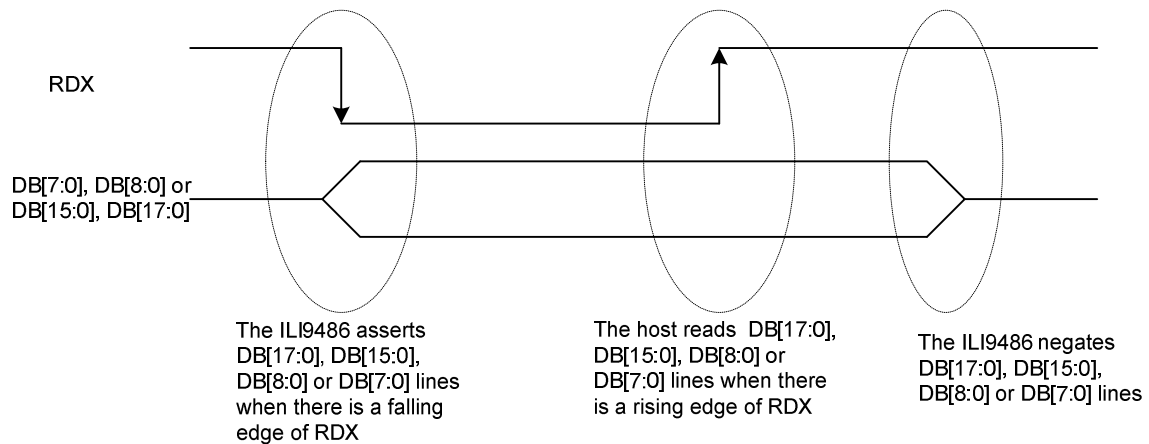
Note: WRX is an unsynchronized signal (It can be stopped)



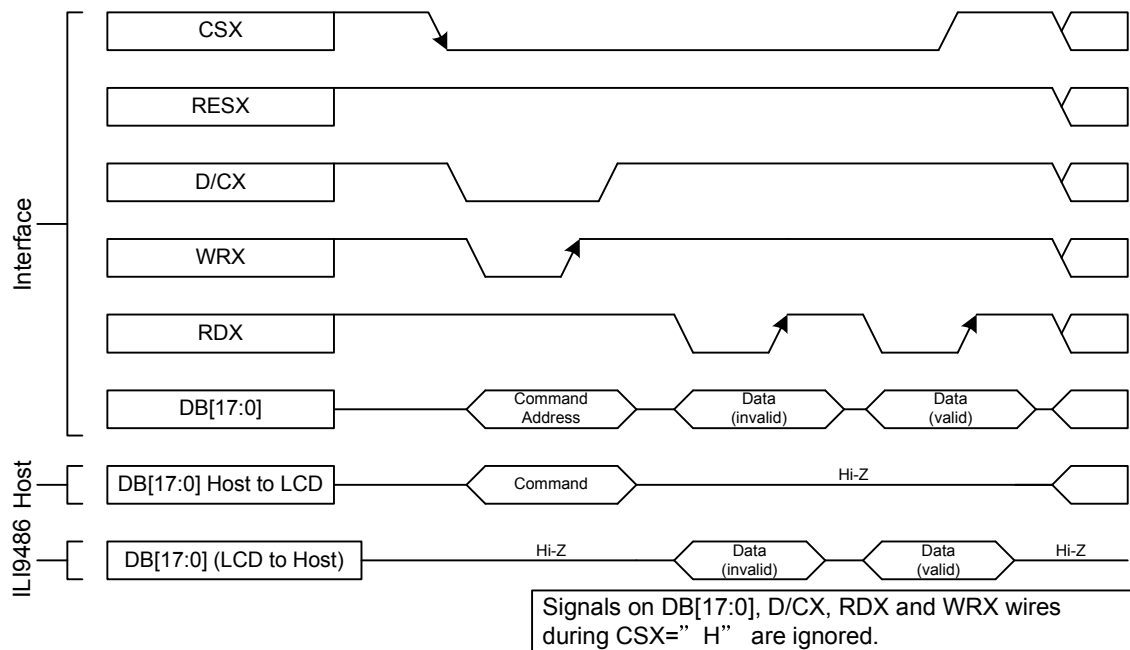
7.1.2.2. Read Cycle Sequence

The RDX signal is driven from high to low then allowed to be pulled back to high during the read cycle. The display module provides information to the host processor during the read cycle while the host processor reads the display module information on the rising edge of RDX signal. When the D/CX signal is driven to low level, then input data on the interface is interpreted as internal status or parameter. The D/CX signal also can be pulled high level when the data on the interface is RAM data or command parameter.

The following figure shows the read cycle for the 8080 MCU interface.



Note: RDX is an unsynchronized signal (It can be stopped).



Note: Read Data is only valid when the D/CX input is pulled high. If D/CX is driven low during read then the display information outputs will be High-Z.

7.1.3. Serial Interface

The selection of this interface is done by IM [2:0] bits. Please refer to the Table in the following.

IM2	IM1	IM0	MPU-Interface Mode	CSX	D/CX	SCL	Function
1	0	1	3-line serial interface	"L"	-		Read/Write command, parameter or display data.
1	1	1	4-line serial interface	"L"	"L"/"H"		Read/Write command, parameter or display data.

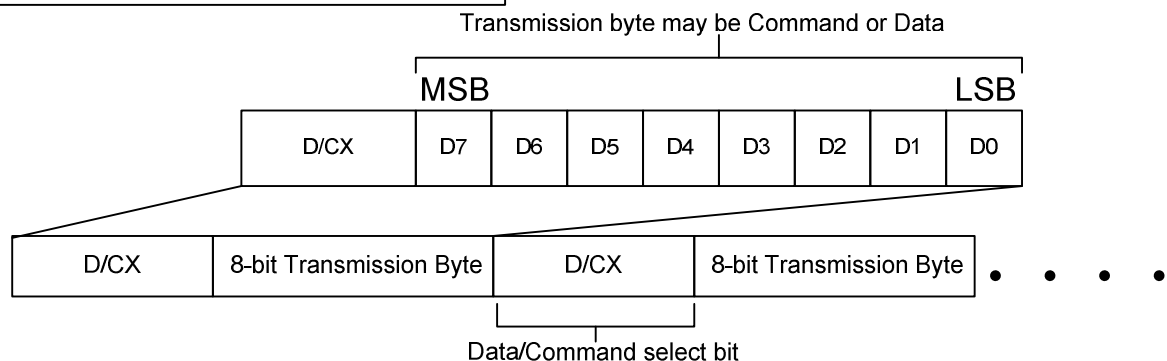
ILI9486L supplies 3-lines/ 9-bit and 4-line/8-bit bi-directional serial interfaces for communication between the host and ILI9486L. The 3-line serial mode consists of the chip enable input (CSX), the serial clock input (SCL) and serial data Input/Output (SDA). The 4-line serial mode consists of the Data/Command selection input (D/CX), chip enable input (CSX), the serial clock input (SCL) and serial data Input/Output (SDA) for data transmission. The data bus (D [17:0]) which are not used, must be leave these unused pins to open. Serial clock (SCL) is used for interface with MCU only, so it can be stopped when no communication is necessary.

7.1.3.1. Write Cycle Sequence

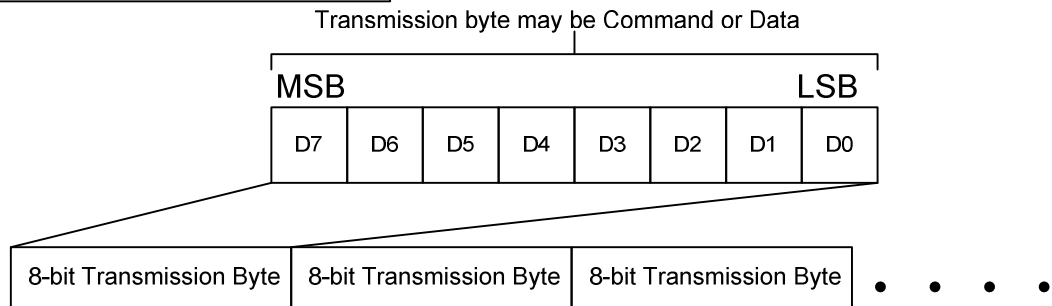
The write mode of the interface means the host writes commands and data to ILI9486L. The 3-lines serial data packet contains a data/command select bit (D/CX) and a transmission byte. If D/CX is "low", the transmission byte is interpreted as a command byte. If D/CX is "high", the transmission byte is stored in the display data RAM (Memory write command), or command register as parameter.

Any instruction can be sent in any order to the ILI9486L and the MSB is transmitted first. The serial interface is initialized when CSX is high status. In this state, SCL clock pulse and SDA data are no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission. See the detail of data format for 3-/4-line serial interface.

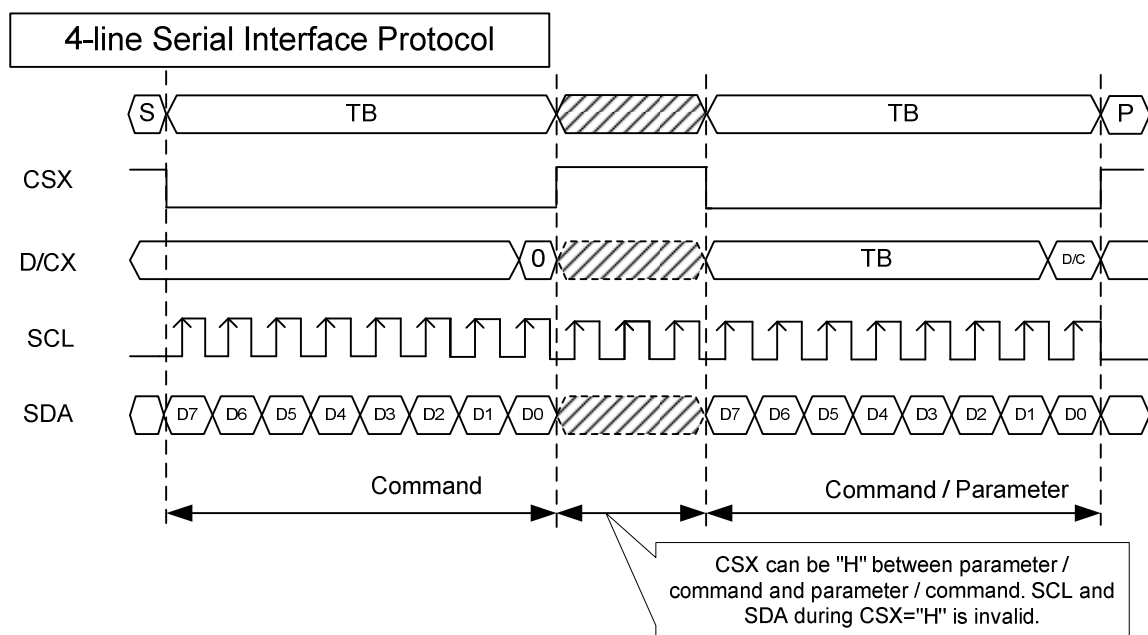
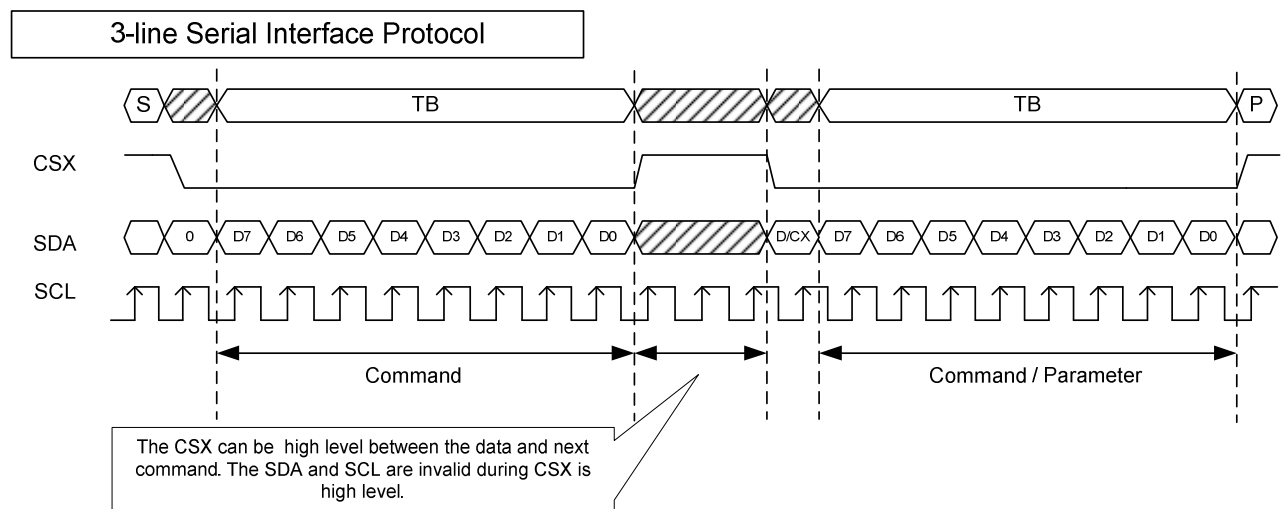
Data Format for 3-line Serial Interface



Data Format for 4-line Serial Interface



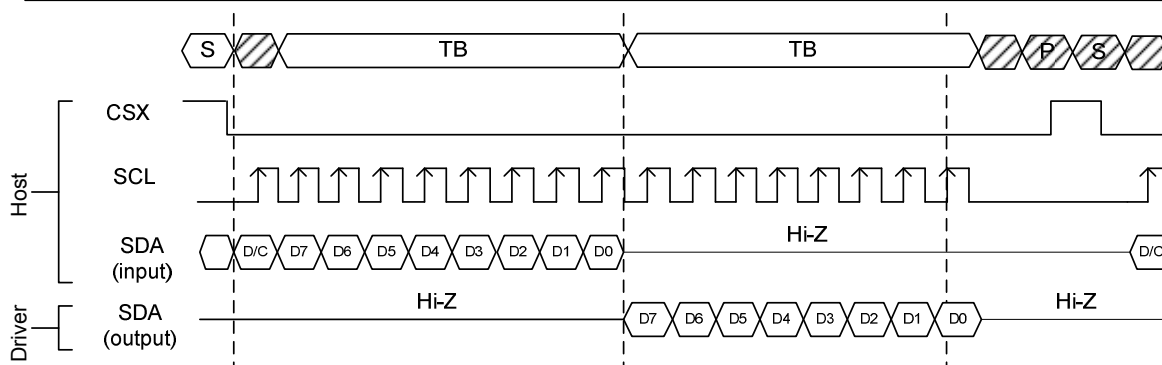
The host drives the CSX pin to low and starts by setting the D/CX bit on SDA. The bit is read by ILI9486L on the first rising edge of SCL signal. On the next falling edge of SCL, the MSB data bit (D7) is set on SDA by the host. On the next falling edge of SCL the next bit (D6) is set on SDA. If the optional D/CX signal is used, a byte is eight read cycle long. The 3/4-line serial interface writes sequence described in the Figure as below.



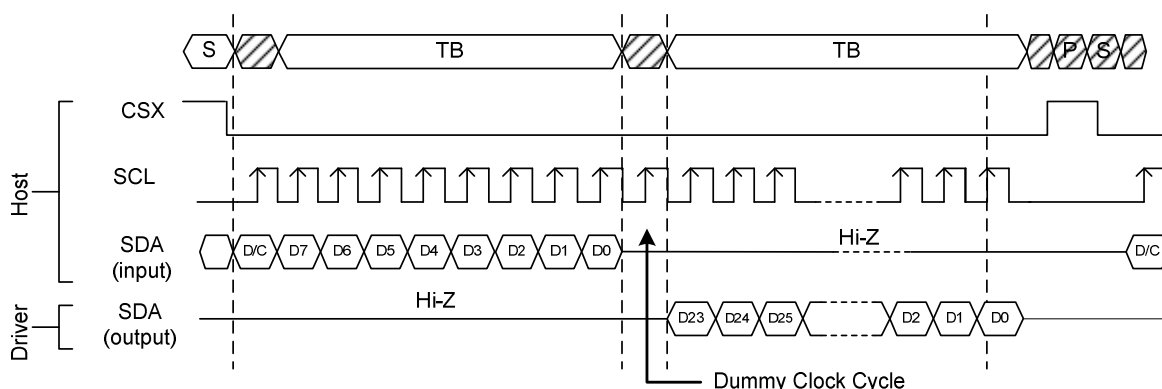
7.1.3.2. Read Cycle Sequence

The read mode of the interface means that the host reads register value from ILI9486L. The host has to send a command (Read ID or register command) and then the following byte is transmitted in the opposite direction. The ILI9486L samples the SDA (input data) at the rising edges of SCL (serial clock), but shifts SDA (output data) at falling edges of SCL (serial clock). After the read status command has been sent, the SDA line must be set to tri-state no later than at the falling edge of SCL of the last bit. The read mode has three types of transmitted command data (8-/24-/32-bit) according command code.

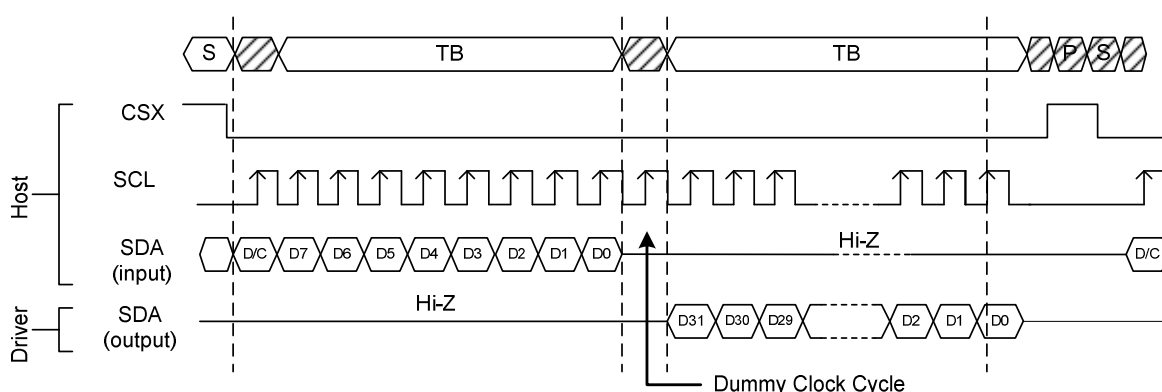
3-line Serial Protocol (for RDID1/RDID2/RDID3/0Ah/0Bh/0Ch/0Dh/0Eh/0Fh command: 8-bit read)



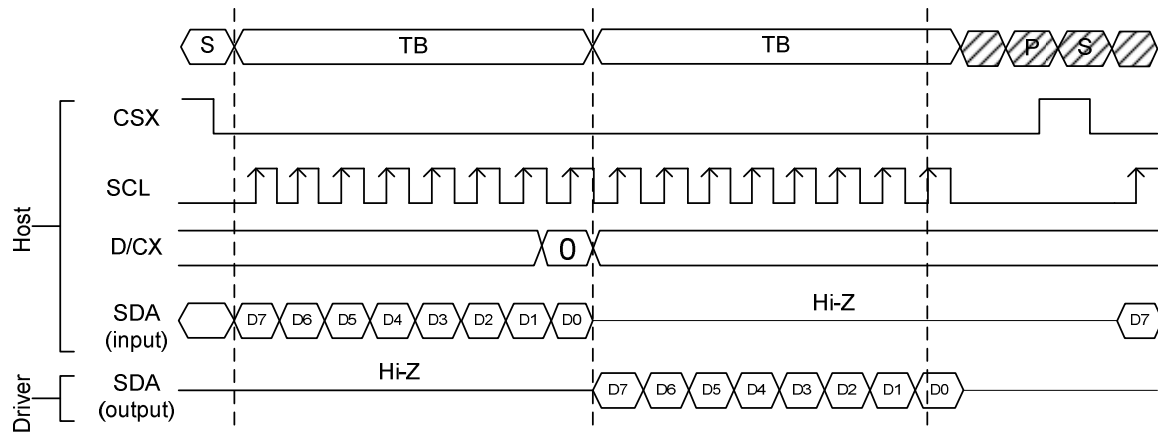
3-line Serial Protocol (for RDDID command: 24-bit read)



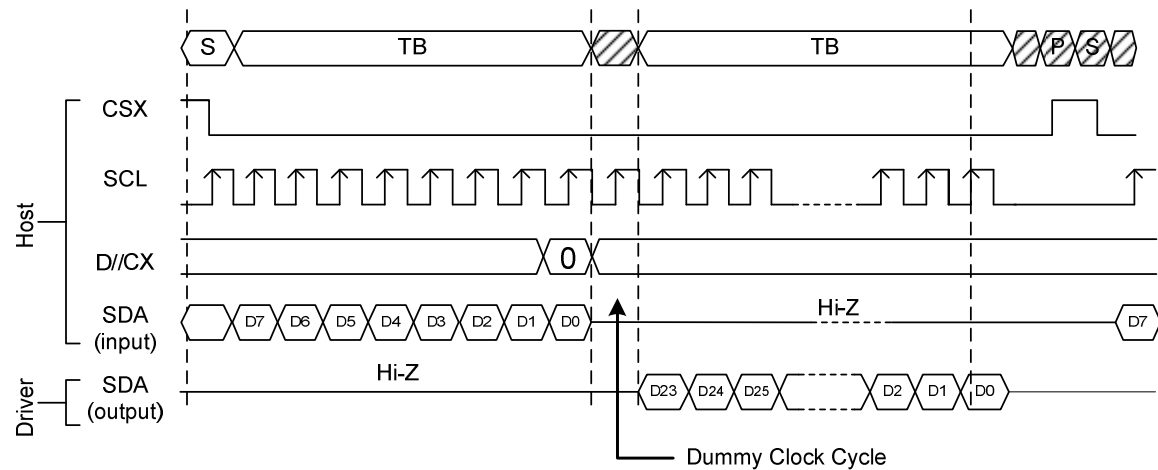
3-line Serial Protocol (for RDDST command: 32-bit read)



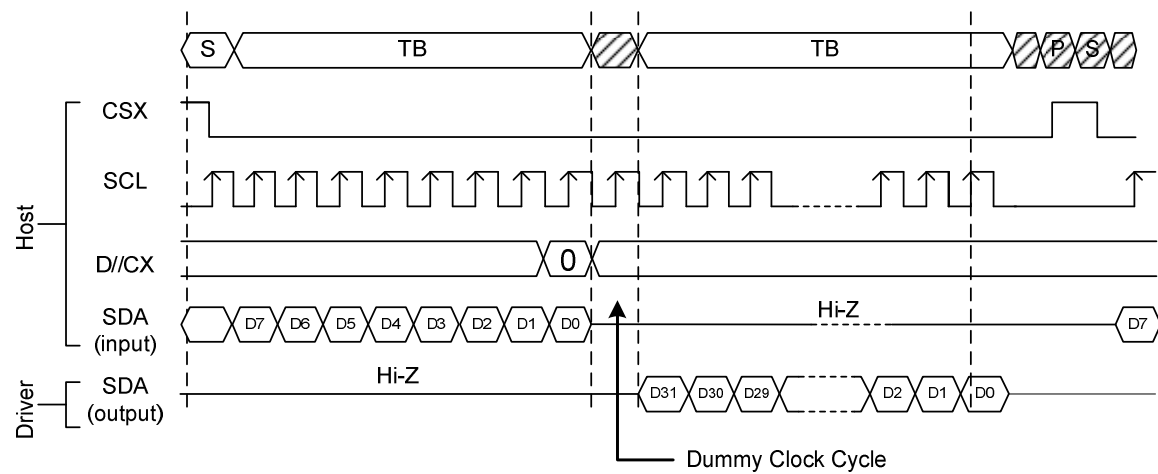
4-line Serial Protocol (for RDID1/RDID2/RDID3/0Ah/0Bh/0Ch/0Dh/0Eh/0Fh command: 8-bit read)



4-line Serial Protocol (for RDDID command: 24-bit read)

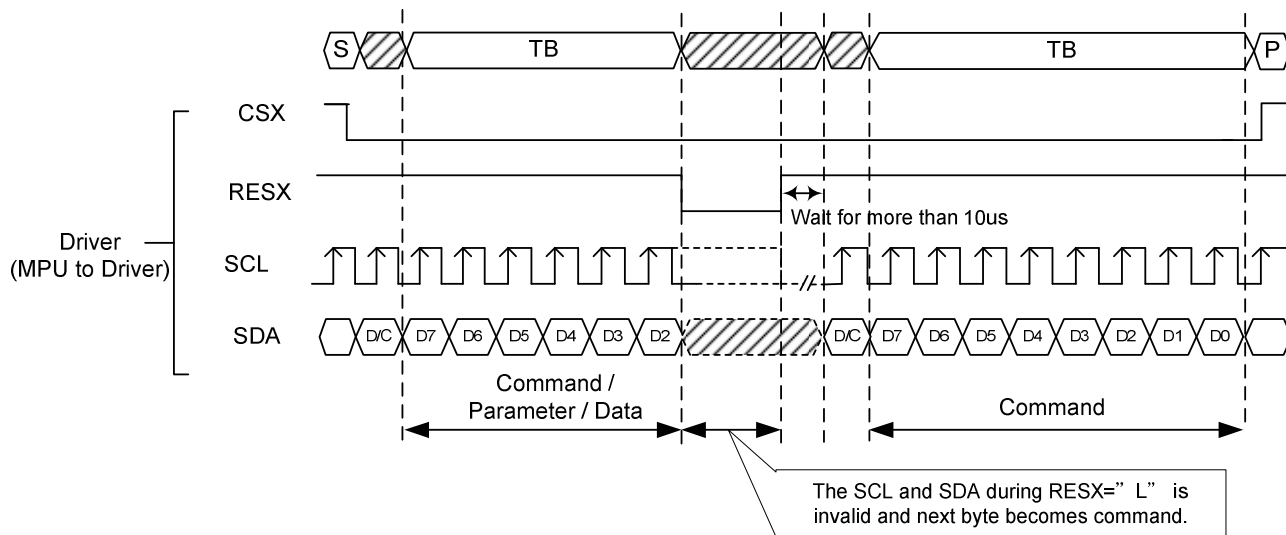


4-line Serial Protocol (for RDDST command: 32-bit read)

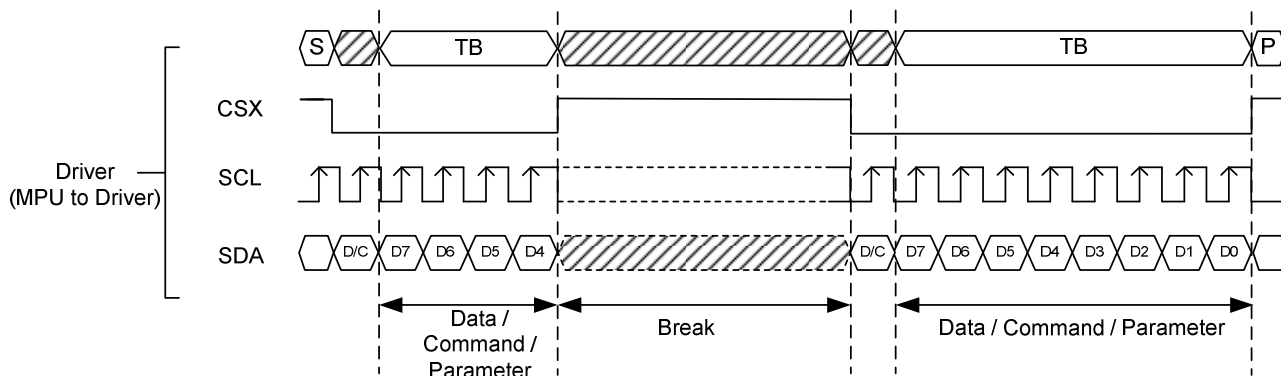


7.1.4. Data Transfer Break and Recovery

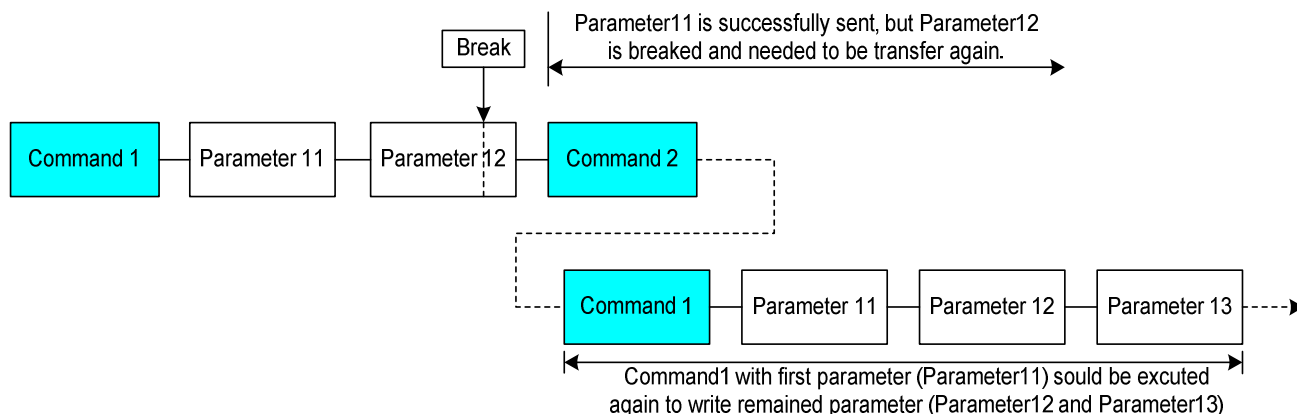
If there is a break in data transmission by RESX pulse, while transferring a Command or Frame Memory Data or Multiple Parameter command Data, before Bit D0 of the byte has been completed, then the driver will reject the previous bits and have reset the interface such that it will be ready to receive command data again when the chip select pin (CSX) is next activated after RESX have been High state.



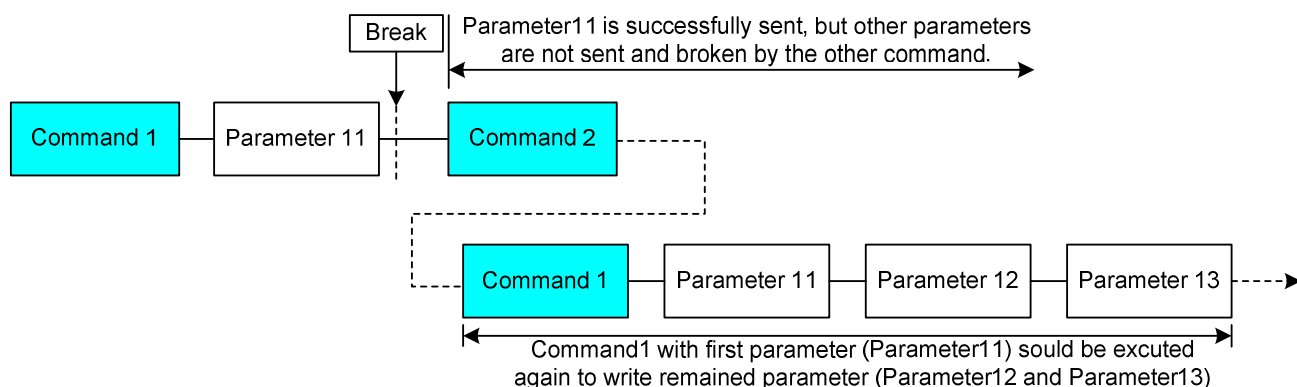
If there is a break in data transmission by CSX pulse, while transferring a Command or Frame Memory Data or Multiple Parameter command Data, before Bit D0 of the byte has been completed, then the driver will reject the previous bits and have reset the interface such that it will be ready to receive the same byte re-transmitted when the chip select pin (CSX) is next activated.



If a two or more parameter command is being sent and a break occurs while sending any parameter before the last one and if the host then sends a new command rather than continue to send the remained parameters that was interrupted, then the parameters that were successfully sent are stored and the parameter where the break occurred is rejected. The interface is ready to receive next byte as shown below.



If a two or more parameter command is being sent and a break occurs by the other command before the last one is sent, then the parameters that were successfully sent are stored and the other parameter of that command remains previous value.

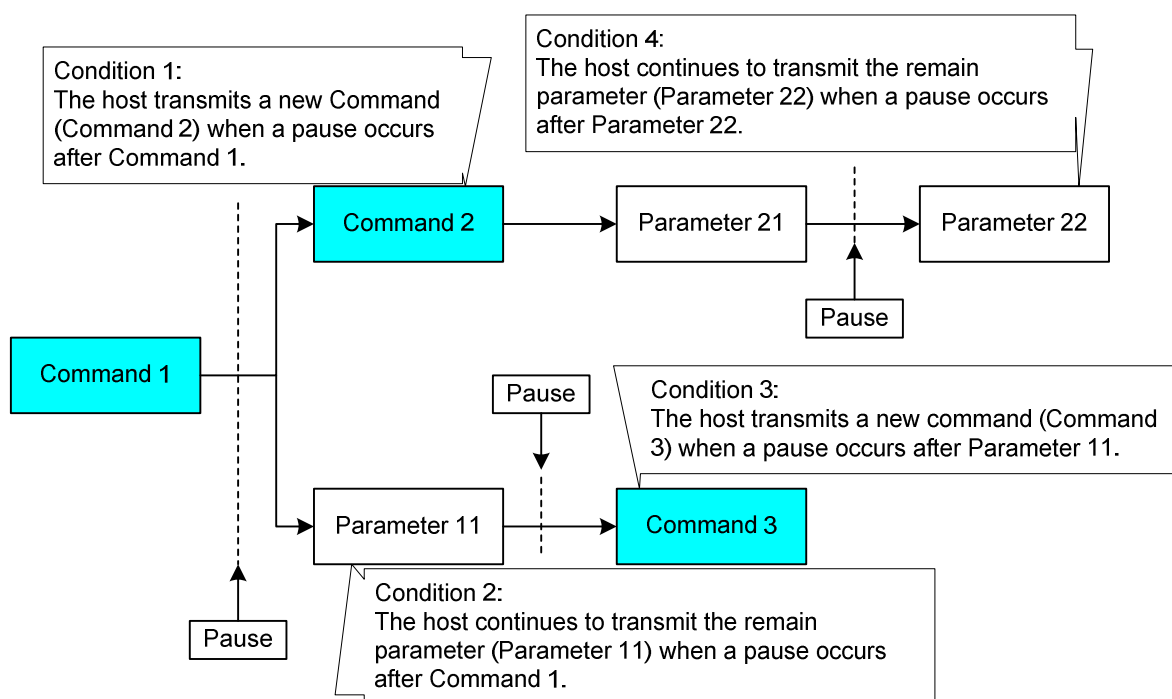


7.1.5. Data Transfer Pause

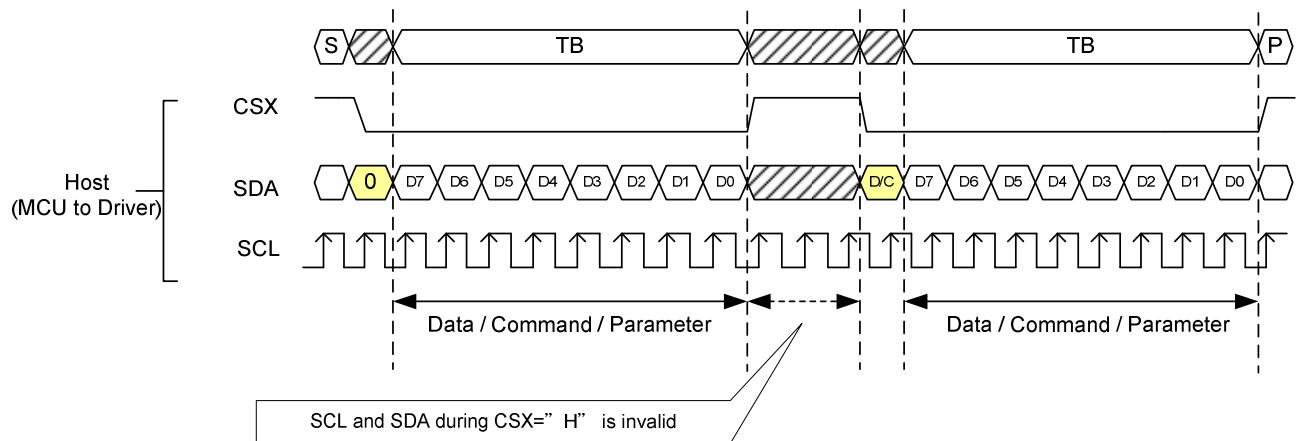
It will be possible when transferring a Command, Frame Memory Data or Multiple Parameter Data to invoke a pause in the data transmission. If the Chip Select pin (CSX) is released after a whole byte of a Frame Memory Data or Multiple Parameter Data has been completed, then ILI9486L will wait and continue the Frame Memory Data or Parameter Data Transmission from the point where it was paused. If the Chip Select pin is released after a whole byte of a command has been completed, then the display module will receive either the command's parameters (if appropriate) or a new command when the Chip Select Line is next enabled as shown below.

This applies to the following 4 conditions:

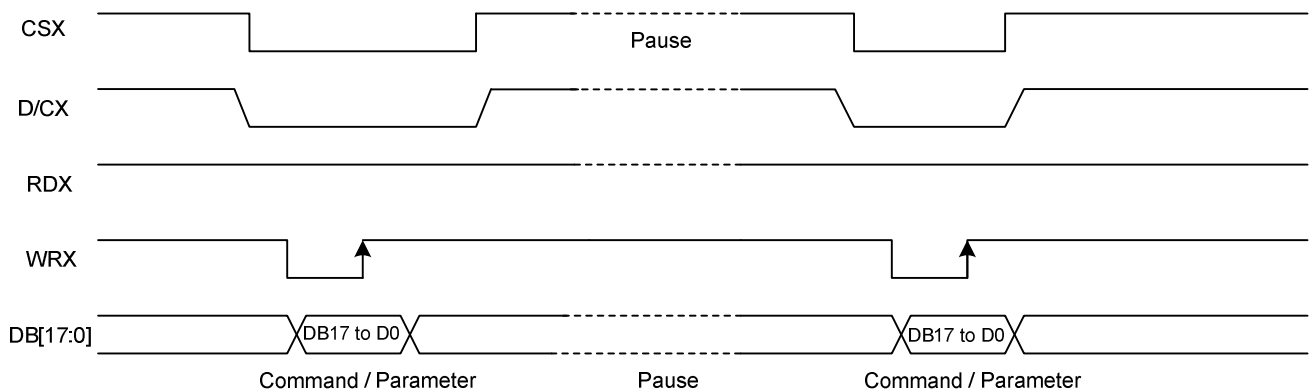
- 1) Command-Pause-Command
- 2) Command-Pause-Parameter
- 3) Parameter-Pause-Command
- 4) Parameter-Pause-Parameter



7.1.5.1. Serial Interface Pause



7.1.5.2. Parallel Interface Pause

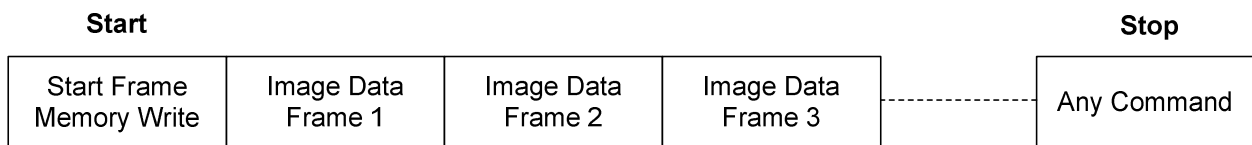


7.1.6. Data Transfer Mode

ILI9486L can provide four different kinds of color depth (8-bit/pixel, 9-bit/pixel, 16-bit/pixel and 18-bit/pixel) display data to the graphic RAM. The data format is described for each interface. Data can be downloaded to the Frame Memory by 2 methods.

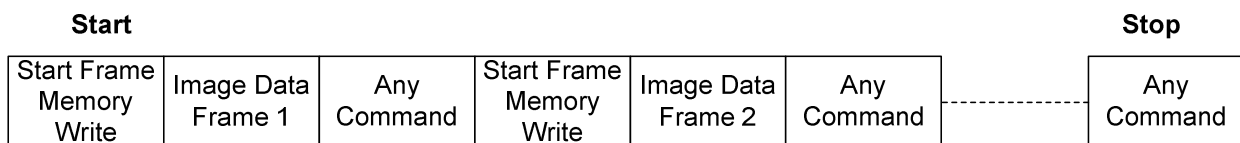
7.1.6.1. Method 1

The Image data is sent to the Frame Memory in the successive Frame writing, each time the Frame Memory is filled by image data, the Frame Memory pointer is reset to the start point and the next Frame is written.



7.1.6.2. Method 2

Image Data is sent and at the end of each Frame Memory download, a command is sent to stop Frame Memory Writing. Then Start Memory Write command is sent, and a new Frame is downloaded.



Note 1: These apply to all data transfer Color modes on both serial and parallel interfaces.

Note 2: The frame memory can contain both odd and even number of pixels for both methods. Only complete pixel data will be stored in the frame memory.

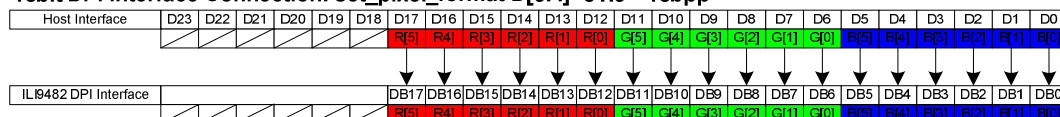
7.2. RGB Interface

7.2.1. RGB Interface Selection

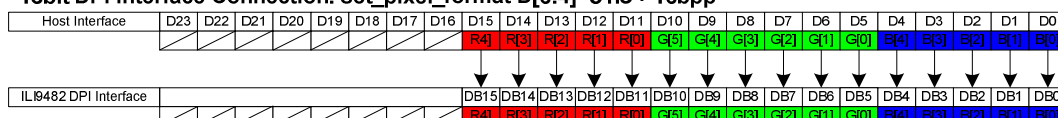
ILI9486L has the RGB interface and these interfaces can be selected by RCM bit. When RCM is set to “0”, the DE mode is selected which utilizes VSYNC, HSYNC, DOTCLK, DE, D [17:0] pins; when RCM is set to “1”, the SYNC mode is selected which utilizes VSYNC, HSYNC, DOTCLK, D [17:0] pins. ILI9486 supports several pixel format that can be selected by DPI[3:0] bits in “Pixel Format Set (3Ah)” command. The selection of a given interfaces are done by DPI[3:0] as show in the following table.

RCM	DPI[2:0]				RGB Interface Mode	RGB Mode	Used Pins
0	0	1	1	0	18-bit RGB interface (262K colors)	DE Mode Valid data is determined by the DE signal	VSYNC, HSYNC, DE, DOTCLK, D[17:0]
0	0	1	0	1	16-bit RGB interface (65K colors)		VSYNC, HSYNC, DE, DOTCLK, D[15:0]
1	0	1	1	0	18-bit RGB interface (262K colors)	SYNC Mode In SYNC mode, DE signal is ignored; blanking porch is determined by B5h command.	VSYNC, HSYNC, DOTCLK, D[17:0]
1	0	1	0	1	16-bit RGB interface (65K colors)		VSYNC, HSYNC, DOTCLK, D[15:0]

18bit DPI Interface Connection: set_pixel_format D[6:4]=3'h6 : 18bpp



16bit DPI Interface Connection: set_pixel_format D[6:4]=3'h5 : 16bpp



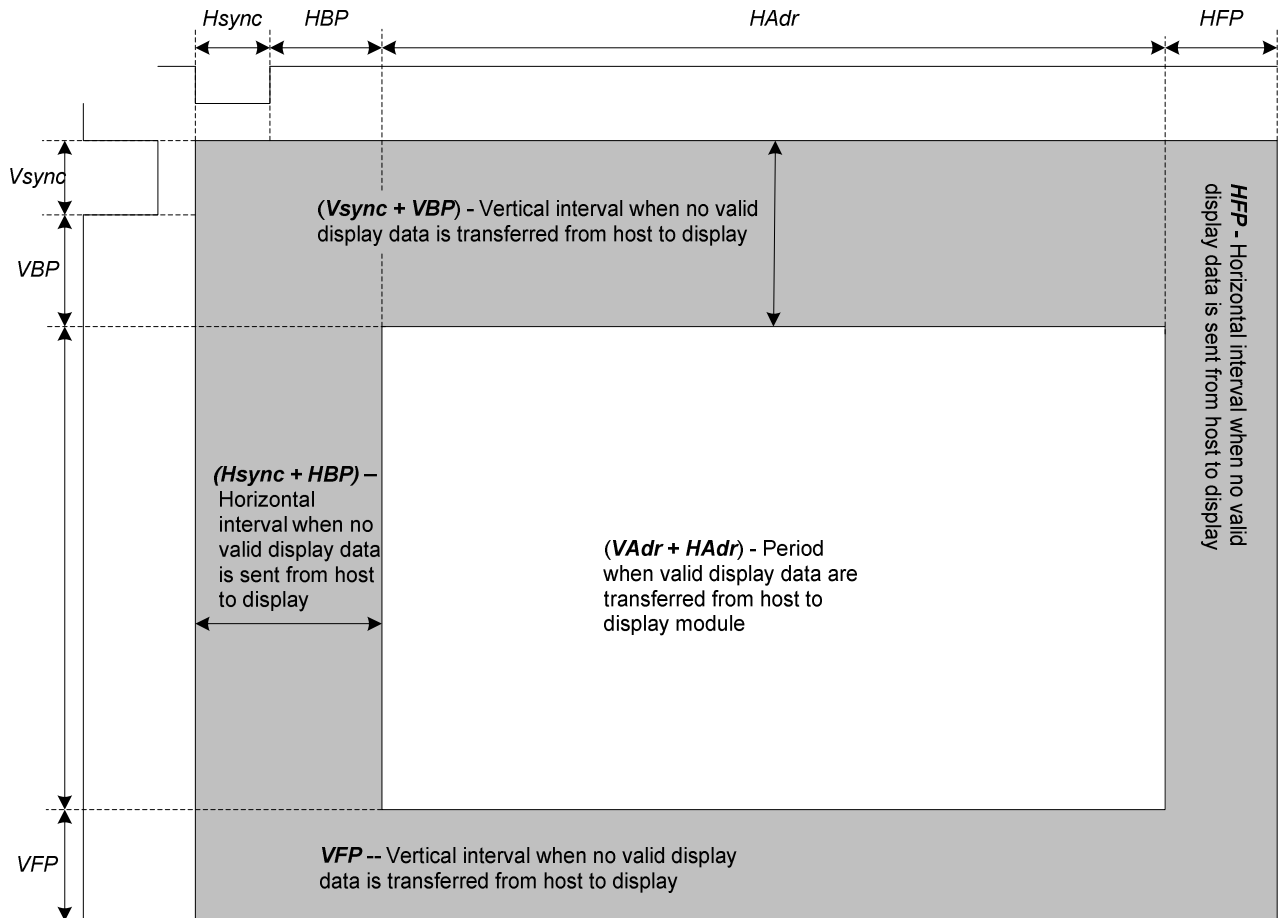
Pixel clock (DOTCLK) is running all the time without stopping and it is used to entering VSYNC, HSYNC, ENABLE and DB[17:0] states when there is a rising edge of the DOTCLK. The DOTCLK can not be used as continues internal clock for other functions of the display module.

Vertical synchronization (VSYNC) is used to tell when there is received a new frame of the display. This is low enable and its state is read to the display module by a rising edge of the DOTCLK signal.

Horizontal synchronization (HSYNC) is used to tell when there is received a new line of the frame. This is low enable and its state is read to the display module by a rising edge of the DOTCLK signal.

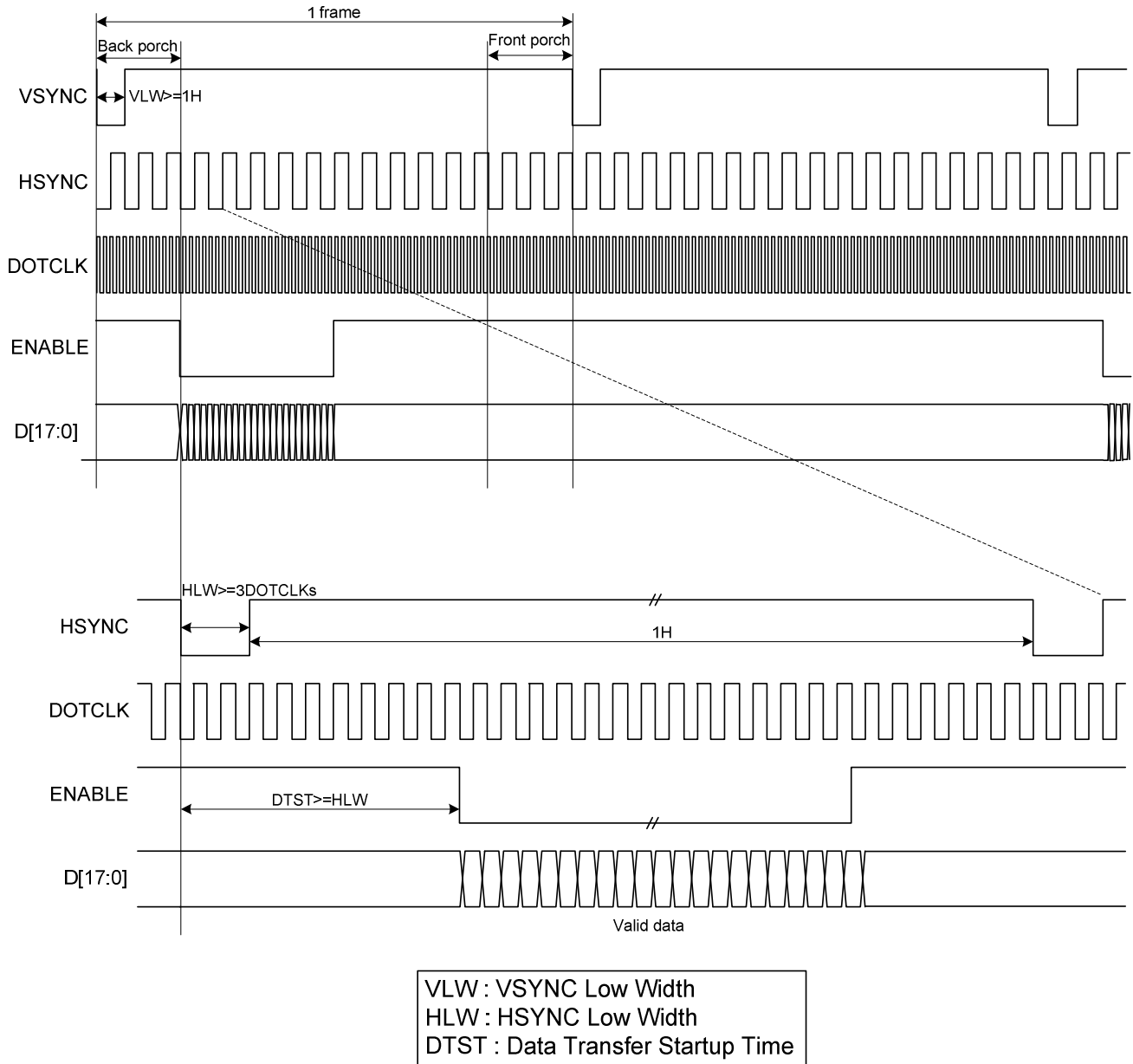
Data Enable (ENABLE) is used to tell when there is received RGB information that should be transferred on the display. This is a high enable and its state is read to the display module by a rising edge of the DOTCLK signal. DB[17:0] are used to tell what is the information of the image that is transferred on the display (When

ENABLE= '0' (low) and there is a rising edge of DOTCLK). DB[17:0] can be '0' (low) or '1' (high). These lines are read by a rising edge of the DOTCLK signal. In RGB interface modes, the input display data is written to GRAM first then outputs corresponding source voltage according the gray data from GRAM.



7.2.2. RGB Interface Timing

The timing chart of 18-/16-bit RGB interface mode is shown as below.



Note 1: The DE signal is not needed when RGB interface SYNC mode is selected.

Note 2: VSPL='0', HSPL='0', DPL='0' and EPL='0' of "Interface Mode Control (B0h)" command.

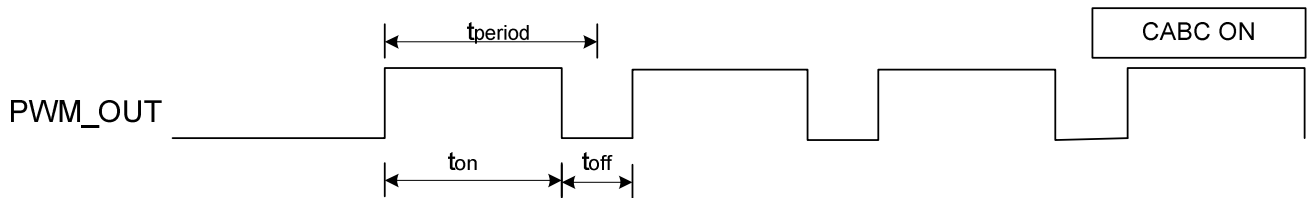
7.3. CABC (Content Adaptive Brightness Control)

ILI9486L provides a dynamic backlight control function as CABC (Content adaptive brightness control) to reduce the power consumption of the luminance source. ILI9486L will refer the gray scale content of display image to output a PWM waveform to LED driver for backlight brightness control. Content adaptation means that the content of gray sale can be increased while simultaneously lowering brightness of the backlight to achieve the same perceived brightness. The adjusted gray level scale and thus the power consumption reduction depend on the content of the image.

ILI9486L can calculate the backlight brightness level and send a PWM pulse to LED driver via PWM_OUT pin for backlight brightness control purpose. The PWM frequency can be adjusted by PWM_DIV parameters and the calculating equation as below:

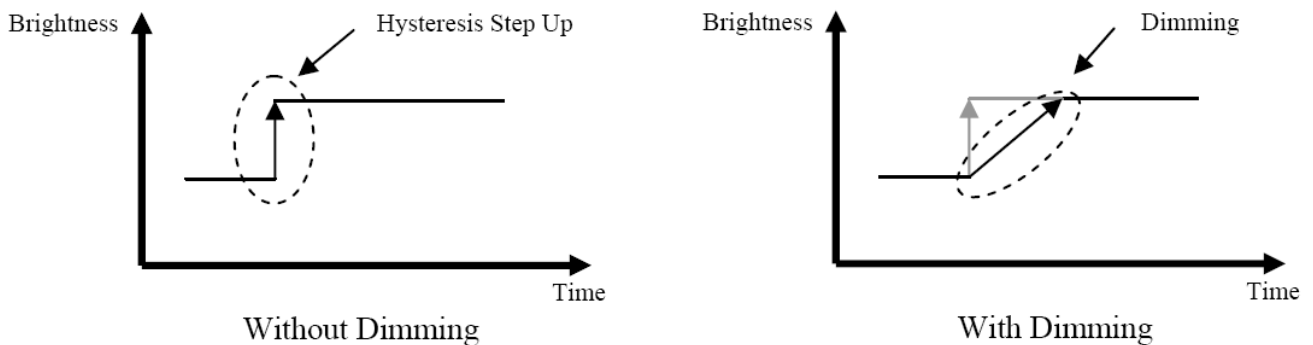
$$f_{\text{PWM_OUT}} = \frac{18\text{MHz}}{(\text{PWM_DIV}[7:0] + 1) \times 255}$$

The figure in the following is the basic timing diagram which is applied ILI9486L to control LED driver.



Display Backlight Dimming Control

A dimming function (how fast to change the brightness from old to new level and what are brightness levels during the change) is used when changing from brightness level to another. This dimming function curve is the same in increment and decrement directions. The basic idea is described below.



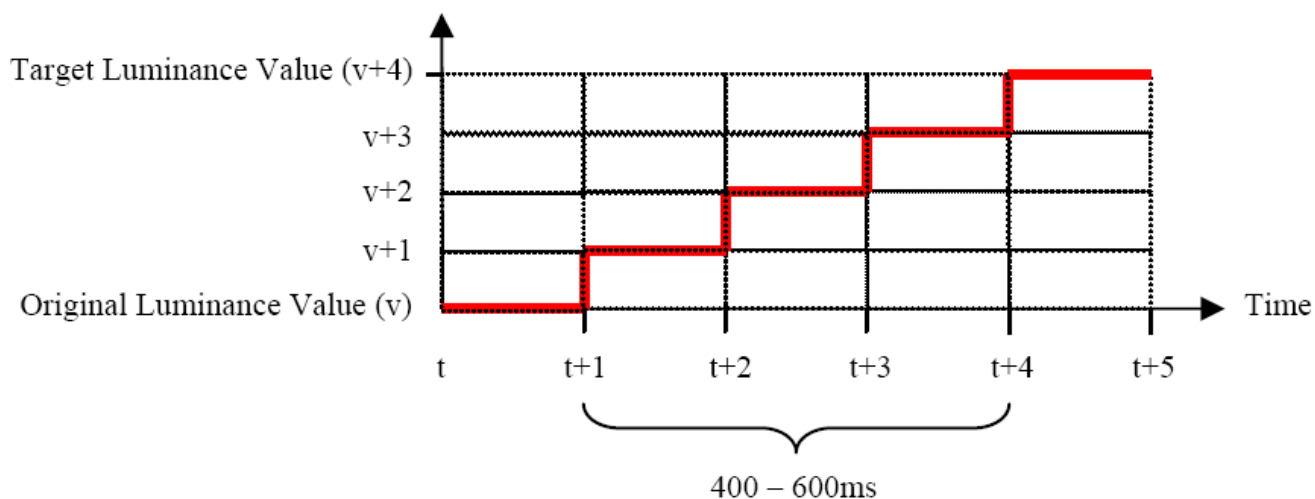
Dimming function can be enabled and disabled. See command "Write CTRL Display(53h), bit3(DD) for more information.

Dimming Requirement

Dimming function in the display module should be implemented so that 400 – 600ms is used for the transition between the original brightness value and the target brightness value. The transferring time steps between these two brightness values are equal making the transition linear.

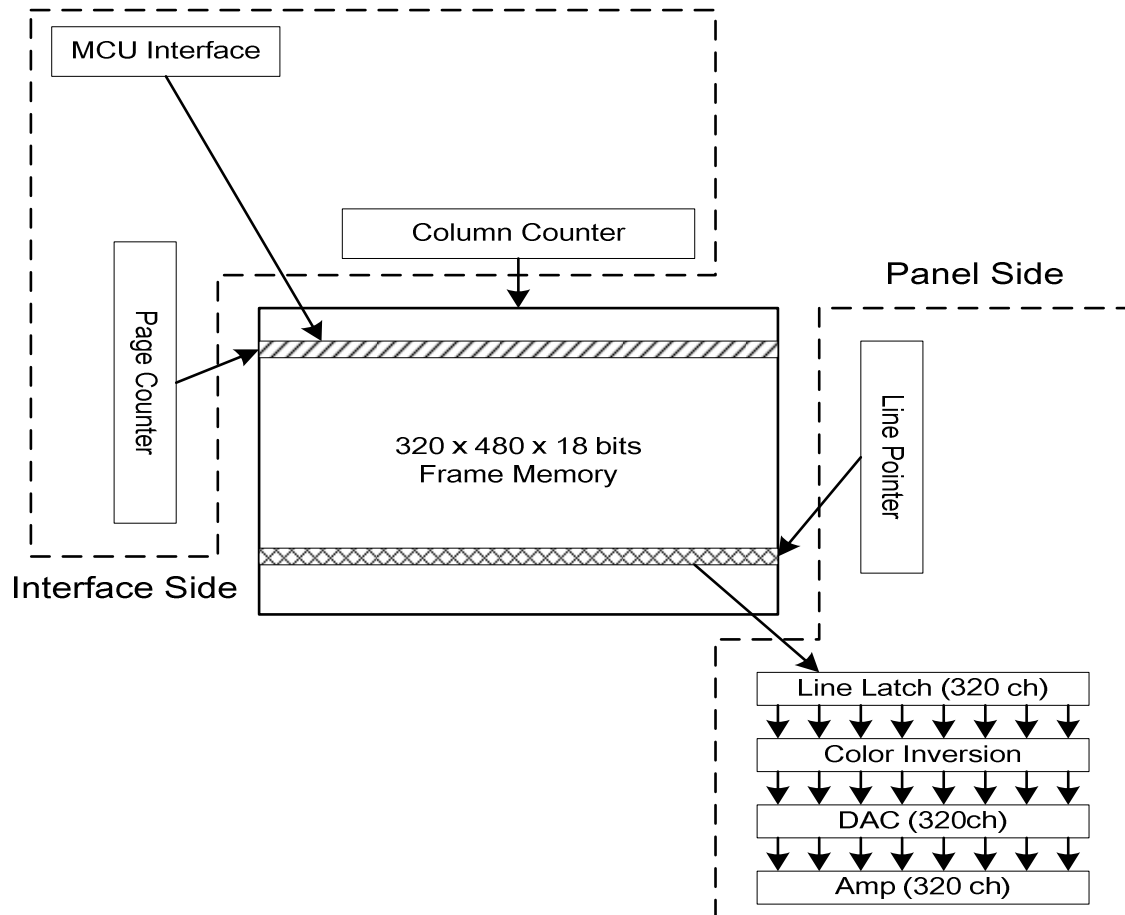
The dimming function is working similarly in both upward and downward directions.

An upward example is illustrated below.



7.4. Display Data RAM (DDRAM)

The ILI9486L has an integrated 320x480x18-bit graphic type static RAM. This 345,600-byte memory allows storing a 320xRGBx480 image with an 18-bit resolution (262K-color). There will be no abnormal visible effect on the display when there is a simultaneous Panel Read and Interface Read or Write to the same location of the Frame Memory.

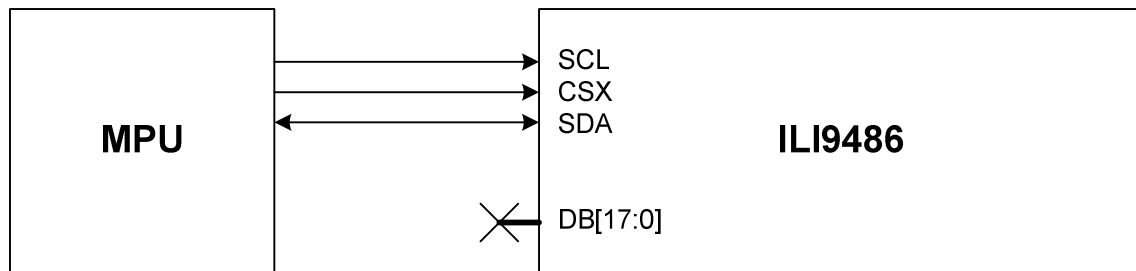


7.5. Display Data Format

ILI9486L supplies 18-/16-/9-/8-bit parallel MCU interface with 8080-series and 3-/4-line serial interface and 16-/18-bit parallel RGB interface. The parallel MCU interface and serial interface mode can be selected by external pins IM [2:0].

7.5.1. 3-line Serial Interface

The 3-line/9-bit serial bus interface of ILI9486L can be used by setting external pin as IM [2:0] to "101". The figure in the following is the example of interface with 8080 microcomputer system interface.

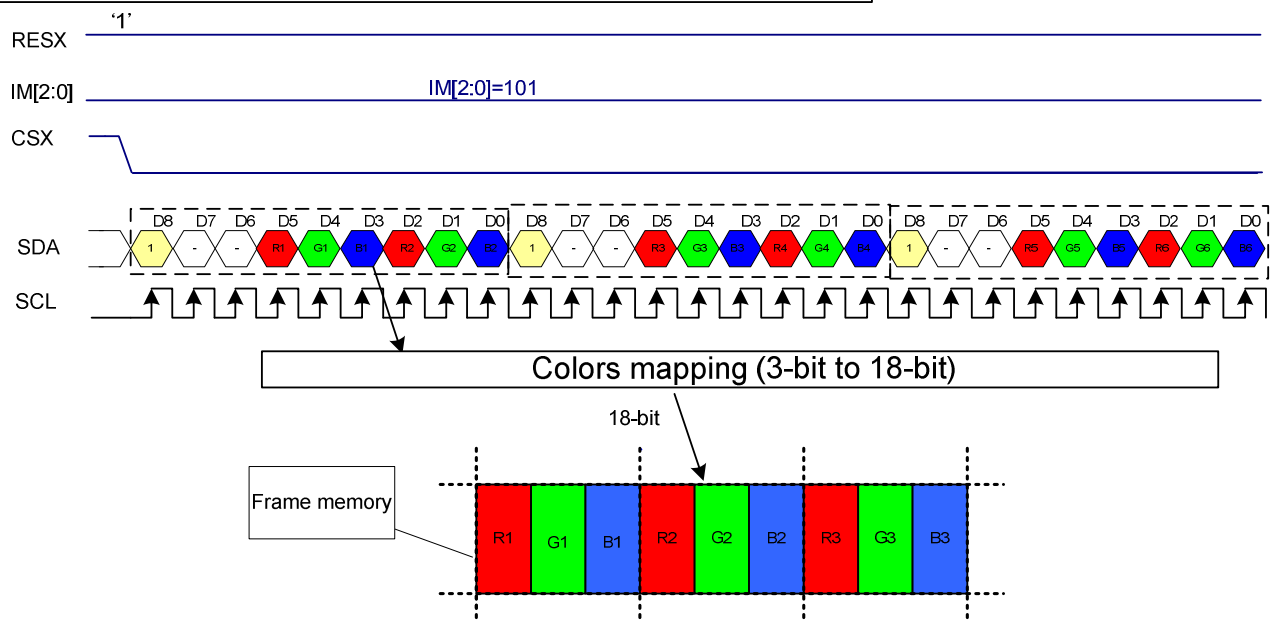


In 3-line serial interface, different display data formats are available for two color depths supported by the LCM listed below.

-8 colors, RGB 1, 1, 1 -bits input

-262k colors, RGB 6, 6, 6 -bits input.

3 bit/pixel color order (R:1-bit, G:1-bit, B:1-bit), 8 colors



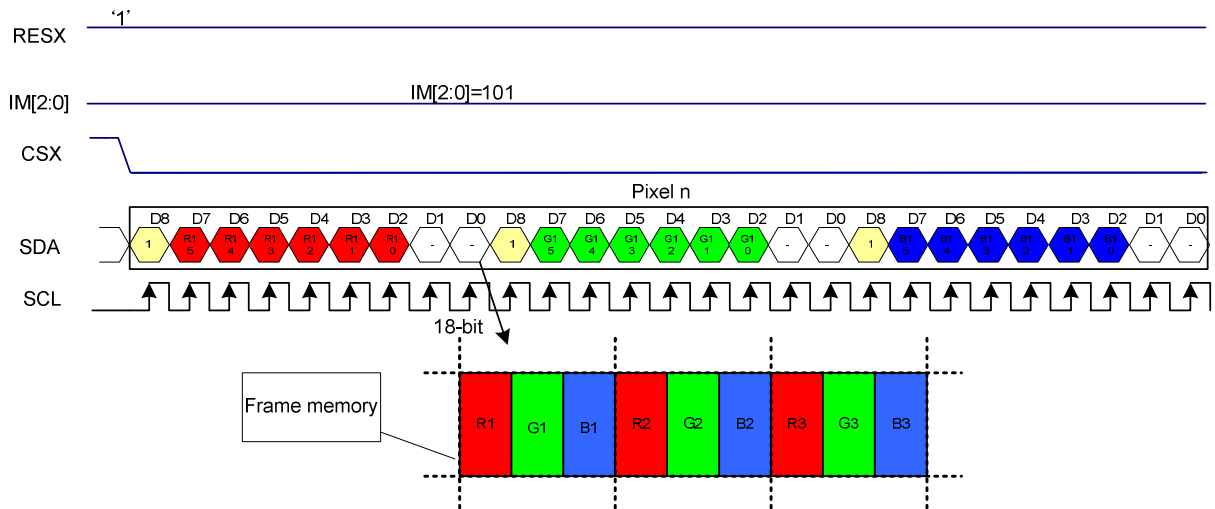
Note 1: The pixel data with 16-bit color depth information.

Note 2: The most significant bits are: Rx4, Gx5 and Bx4.

Note 3: The least significant bits are: Rx0, Gx0 and Bx0.

Note 4: '-'= Don't care – Leave these pins to Open.

18 bit/pixel color order (R:6-bit, G:6-bit, B:6-bit), 262,144 colors



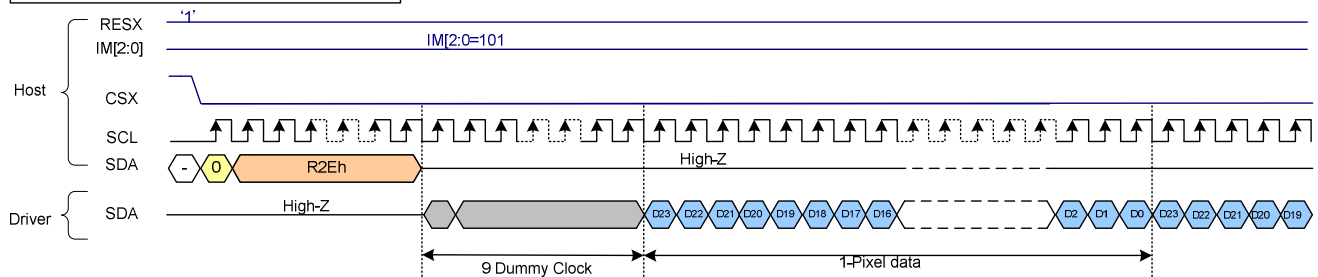
Note 1: The pixel data with 18-bit color depth information.

Note 2: The most significant bits are: Rx5, Gx5 and Bx5.

Note 3: The least significant bits are : Rx0, Gx0 and Bx0.

Note 4: '-'= Don't care - Leave these pins to Open.

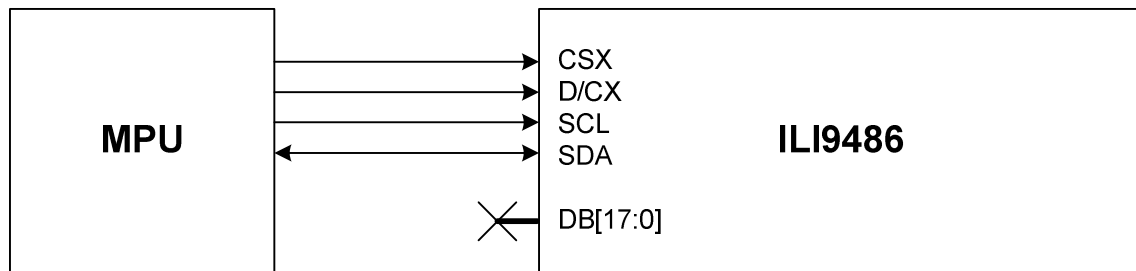
Read data through 3-line SPI mode



Note 1: '-'= Don't care – Leave these pins to Open.

7.5.2. 4-line Serial Interface

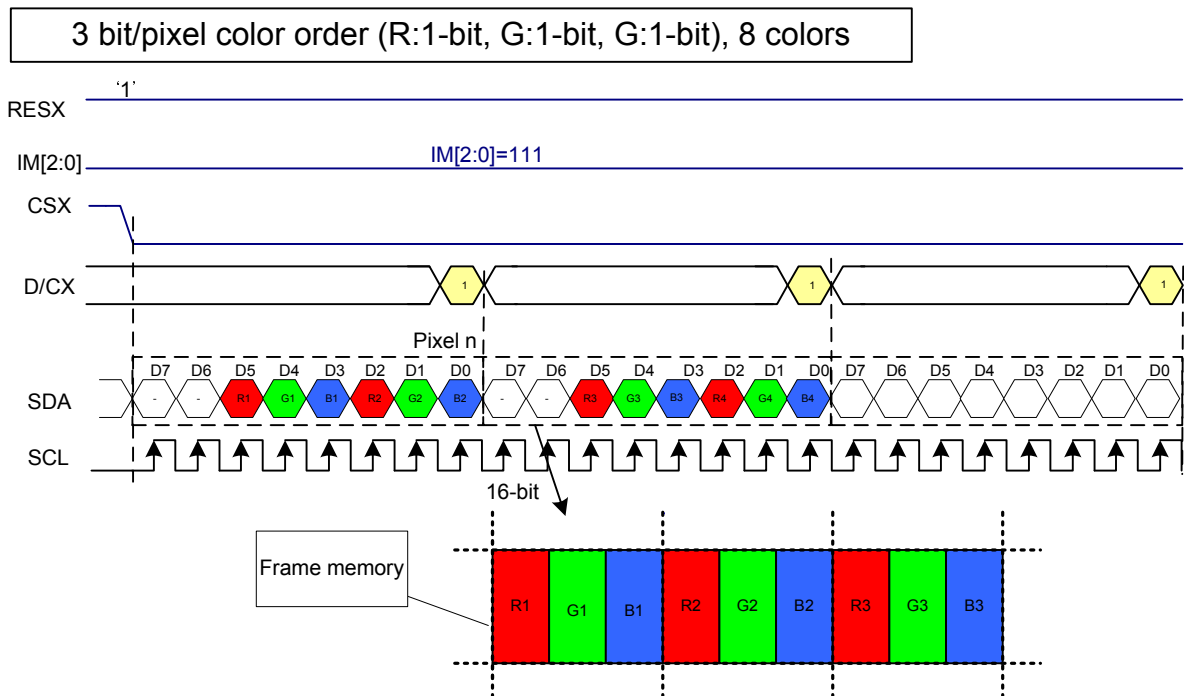
The 4-line/8-bit serial bus interface of ILI9486L can be used by setting external pin as IM [2:0] to "111". The figure in the following is the example of interface with 8080 microcomputer system interface.



In 4-line serial interface, different display data formats are available for two color depths supported by the LCM listed below.

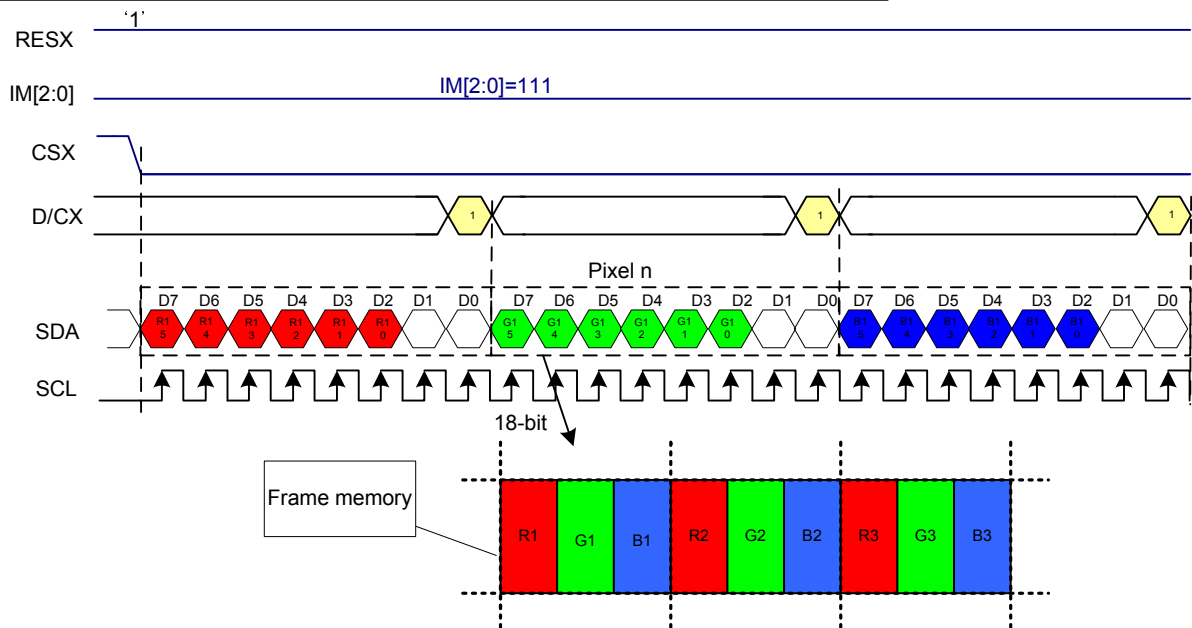
-8 colors, RGB 1, 1, 1 -bits input.

-262k colors, RGB 6, 6, 6 -bits input.



Note : '-'= Don't care – Leave these pins to Open.

18 bit/pixel color order (R:6-bit, G:6-bit, B:6-bit) , 262,144 colors



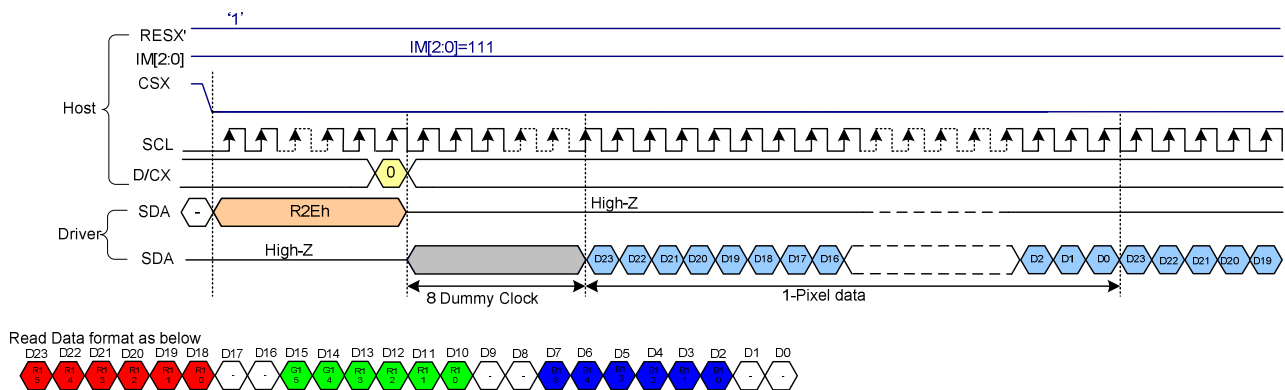
Note 1: The pixel data with 18-bit color depth information.

Note 2: The most significant bits are: Rx5, Gx5 and Bx5.

Note 3: The least significant bits are: Rx0, Gx0 and Bx0.

Note 4: '-=' Don't care – Leave these pins to Open.

Read data through 4-line SPI mode

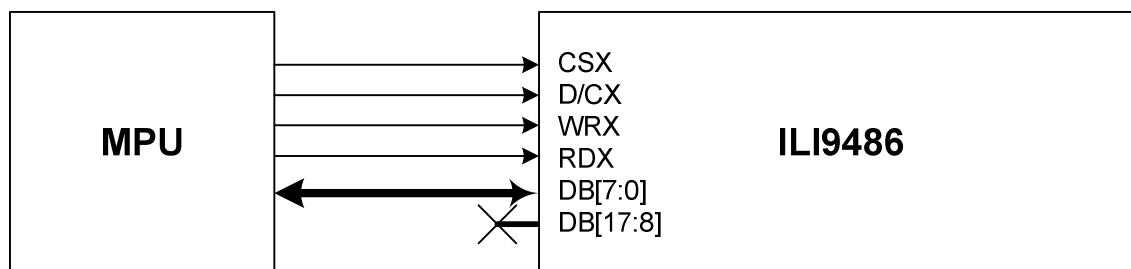


Note 1: '-=' Don't care – Leave these pins to Open.

7.5.3. 8-bit Parallel MCU Interface

The 8080-system 8-bit parallel bus interface of ILI9486L can be used by setting external pin as IM [2:0] to "011".

The figure in the following is the example of interface with 8080 microcomputer system interface.

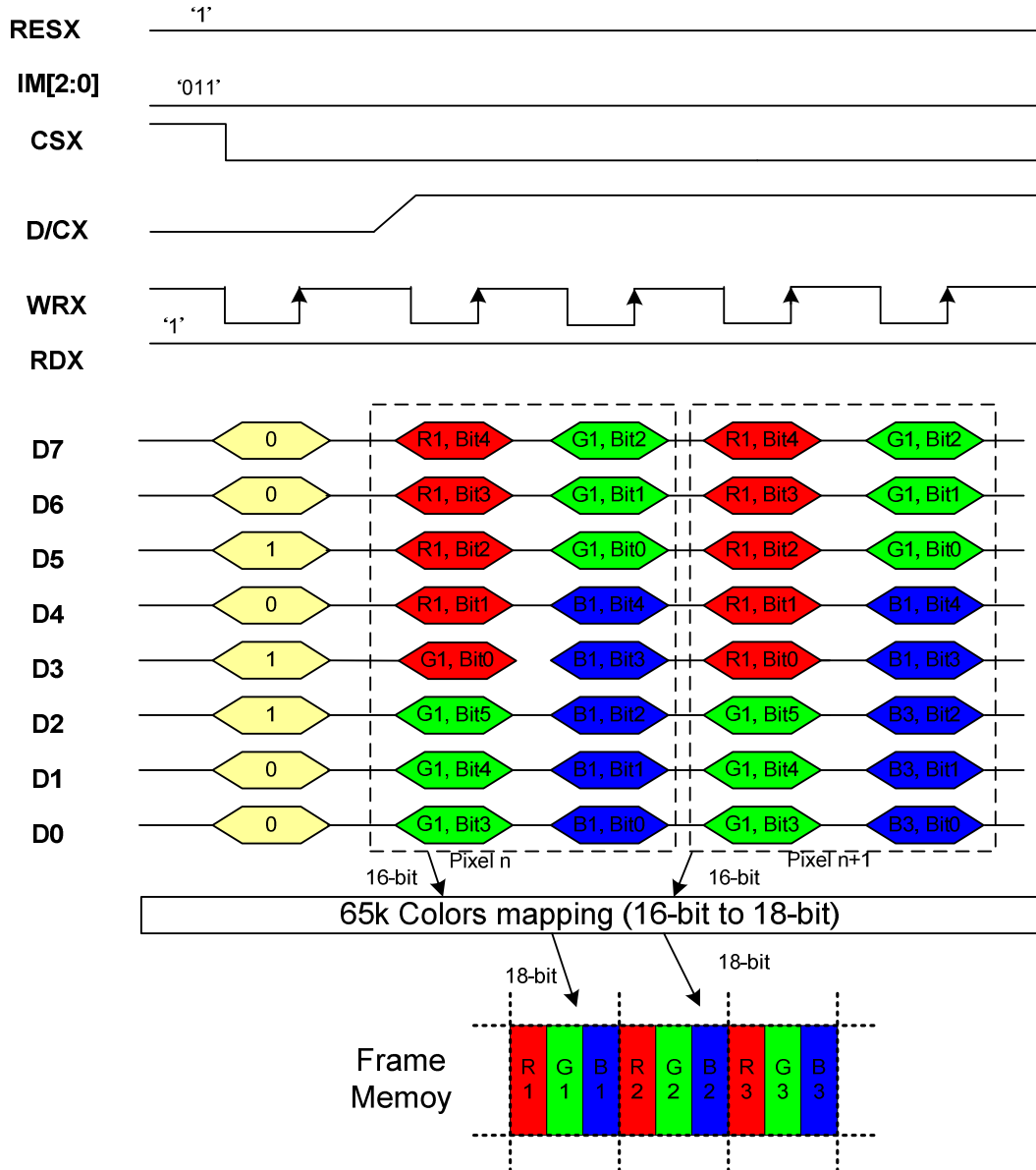


Different display data formats are available for two color depths supported by listed below.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

7.5.3.1. 8-bit Data Bus for 16-bit/pixel (RGB 5-6-5 bits input), 65K-color

16 bit/pixel color order (R:5-bit, G:6-bit, B:5-bit), 65,536 colors



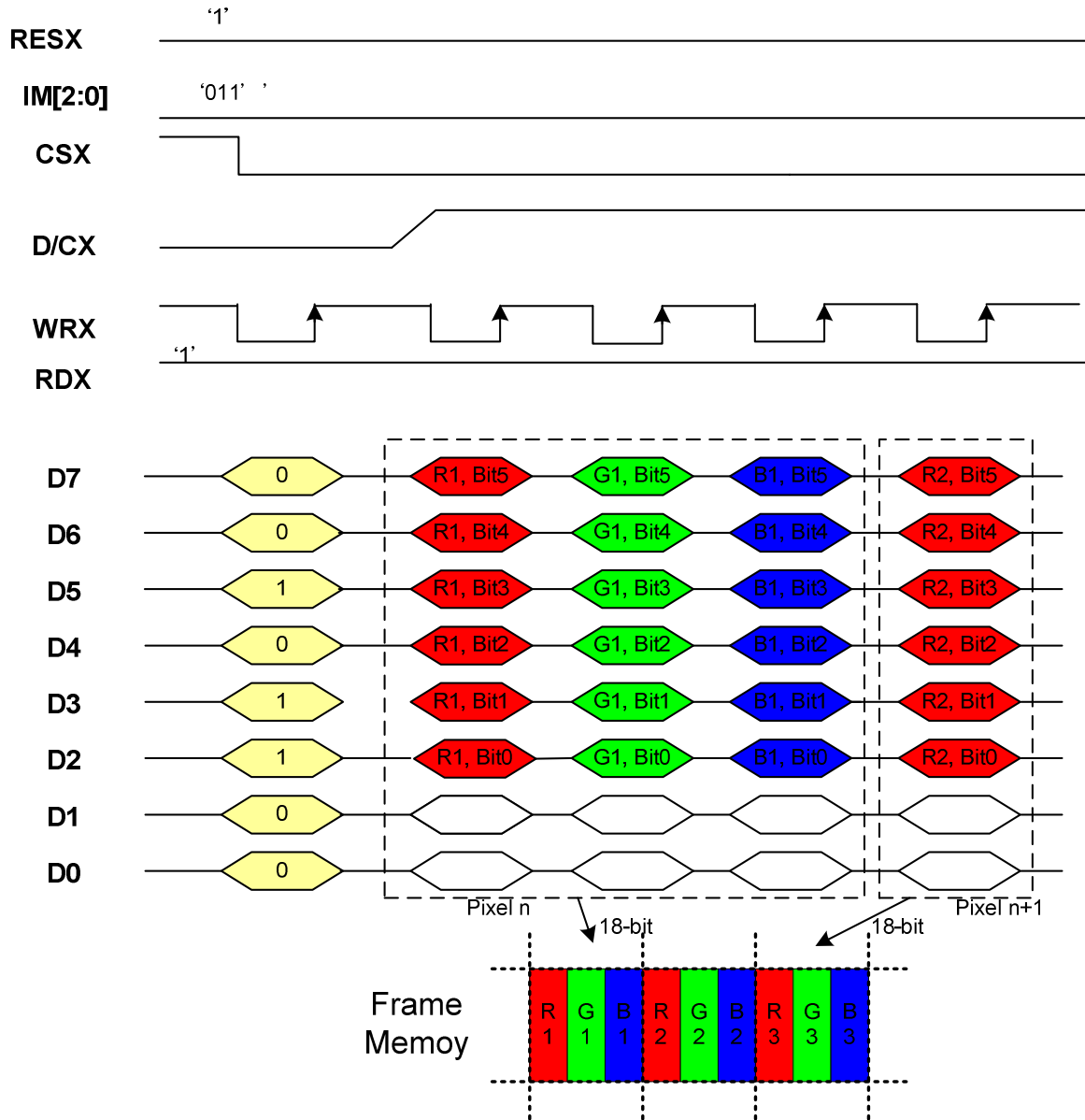
Note 1: The data order is as follows, MSB=D7, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green data and MSB=Bit 4, LSB=Bit0 for Red and Blue data.

Note 2: 2-times transfer is used to transmit 1 pixel data with the 16-bits color depth information.

Note 3: '-=' Don't care – Leave these pins to Open.

7.5.3.2. 8-bit Data Bus for 18-bit/pixel (RGB 6-6-6 bits input), 262K-color

18 bit/pixel color order (R:6-bit, G:6-bit, B:6-bit), 262,144 colors



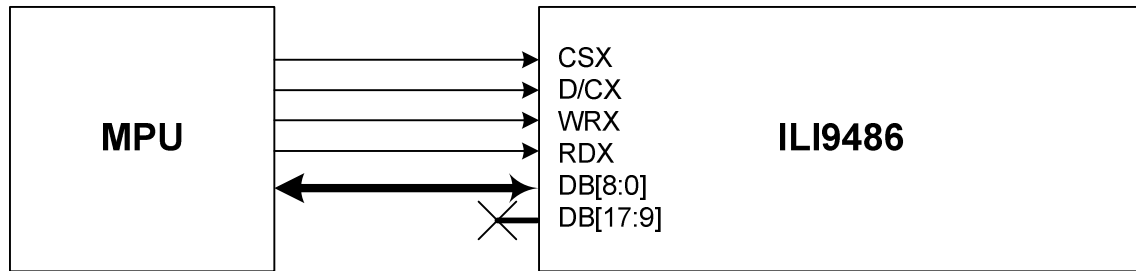
Note 1: The data order is as follows, MSB=D7, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green, Red and Blue data.

Note 2: 3-times transfer is used to transmit 1 pixel data with the 18-bits color depth information.

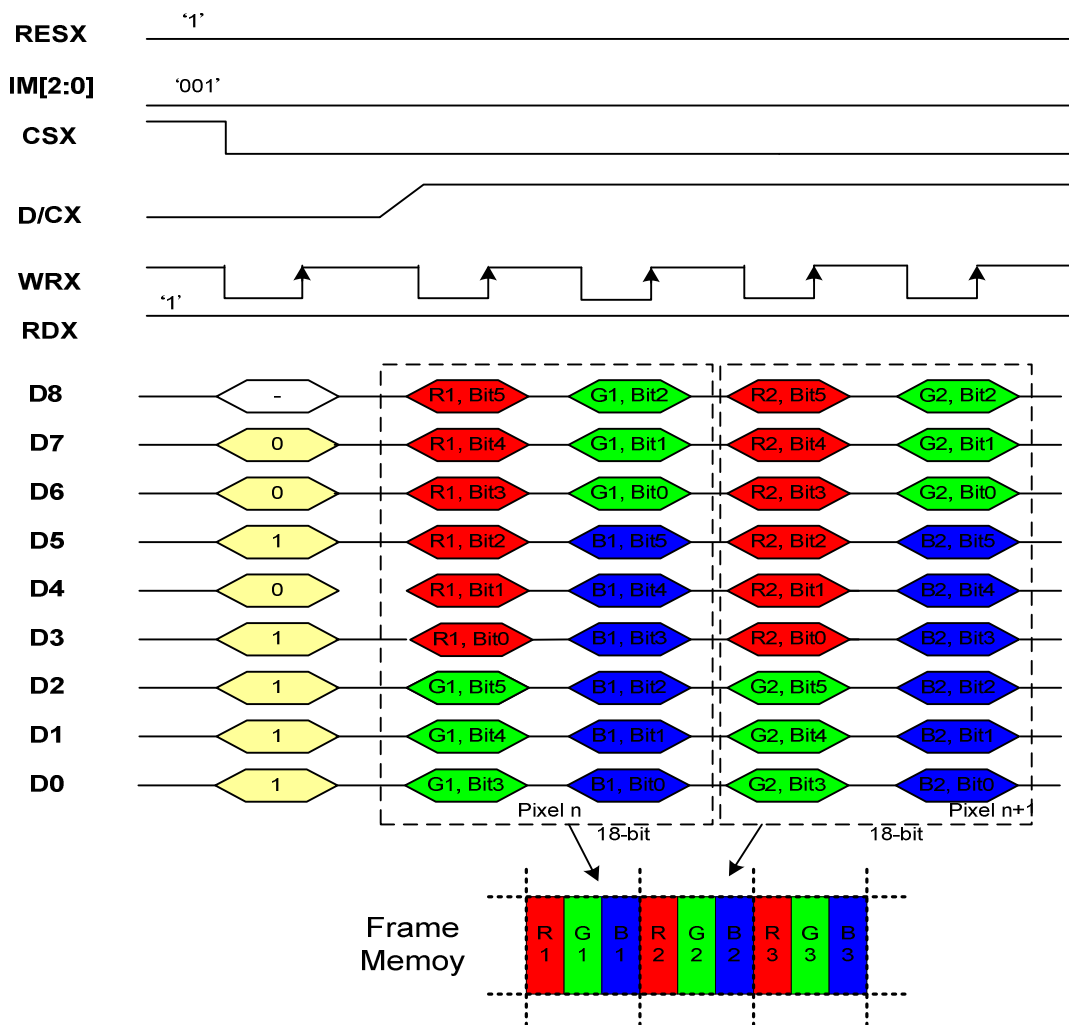
Note 3: '-'= Don't care – Leave these pins to Open.

7.5.4. 9-bit Parallel MCU Interface

The 8080-system 9-bit parallel bus interface of ILI9486L can be used by setting external pin as IM [2:0] to "001". The figure in the following is the example of interface with 8080 microcomputer system interface.



18 bit/pixel color order (R:6-bit, G:6-bit, B:6-bit), 262,144 colors



Note 1: The data order is as follows, MSB=D8, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green, Red and Blue data.

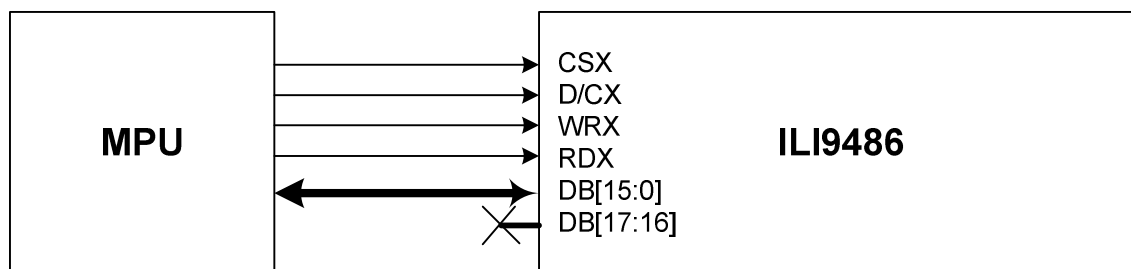
Note 2: 2-times transfer is used to transmit 1 pixel data with the 18-bits color depth information.

Note 3: '-'= Don't care – Leave these pins to Open.

7.5.5. 16-bit Parallel MCU Interface

The 8080-system 16-bit parallel bus interface of ILI9486L can be used by setting external pin as IM [2:0] to "010".

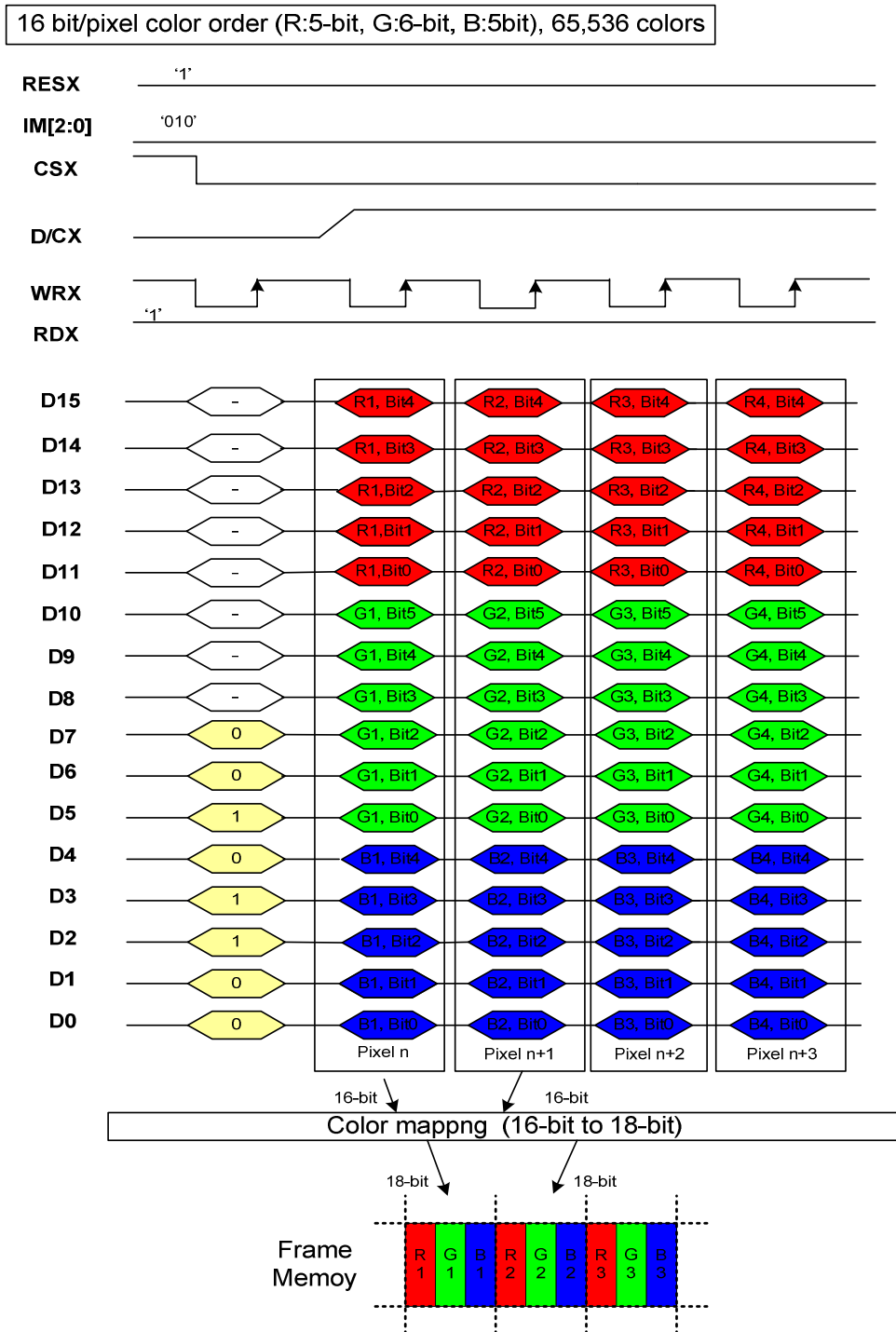
The figure in the following is the example of interface with 8080 microcomputer system interface.



Different display data formats are available for two colors depth supported by listed below.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

7.5.5.1. 16-bit Data Bus for 16-bit/pixel (RGB 5-6-5 bits input), 65K-color



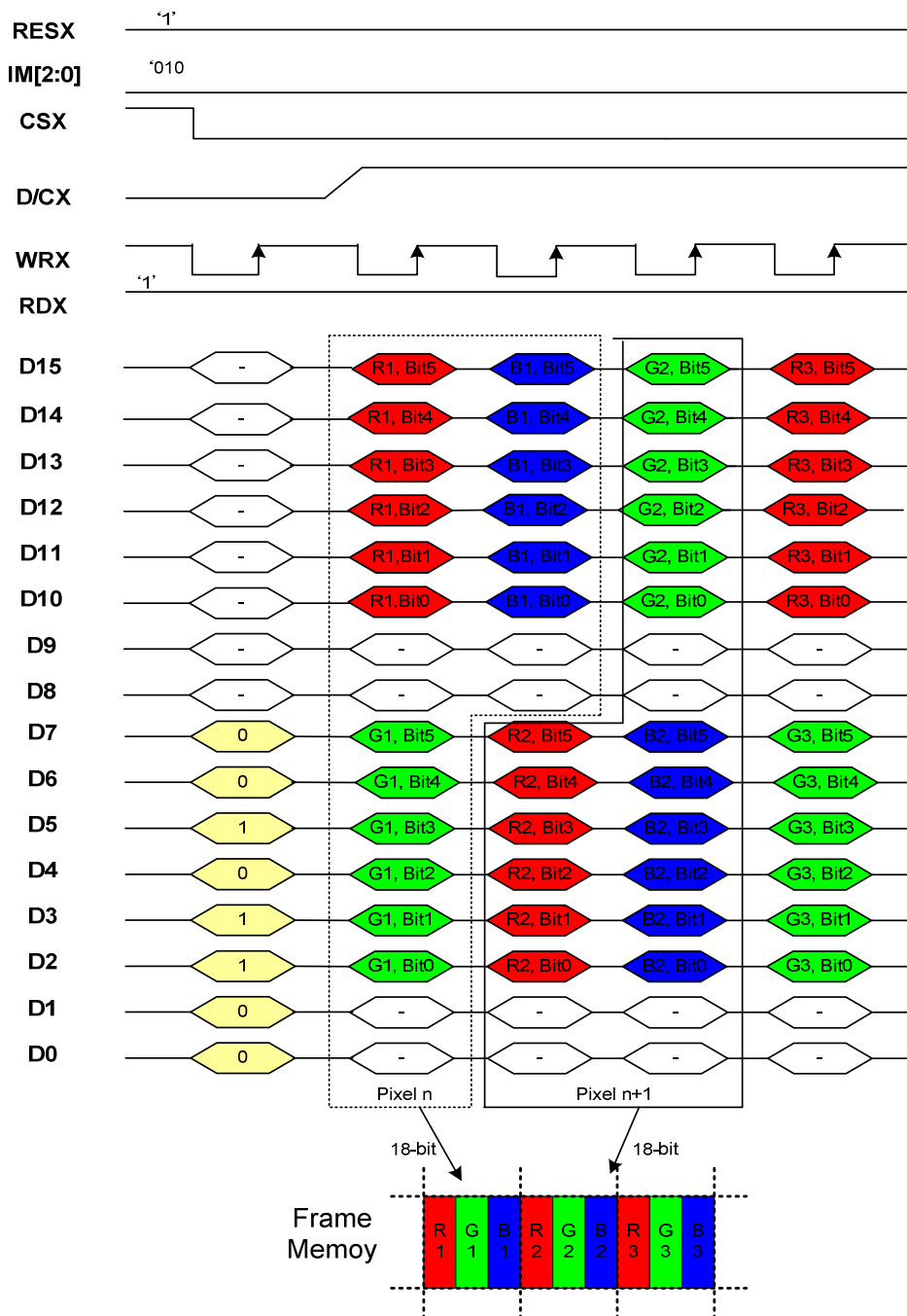
Note 1: The data order is as follows, MSB=D15, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green data and MSB=Bit 4, LSB=Bit0 for Red and Blue data.

Note 2: 1-times transfer is used to transmit 1 pixel data with the 16-bits color depth information.

Note 3: '-' = Don't care – Leave these pins to Open.

7.5.5.2. 16-bit Data Bus for 18-bit/pixel (RGB 6-6-6 bits input), 262K-color

18 bit/pixel color order (R:6-bit, G:6-bit, B:6-bit), 262,144 colors



Note 1: The data order is as follows, MSB=D15, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green, Red and Blue data.

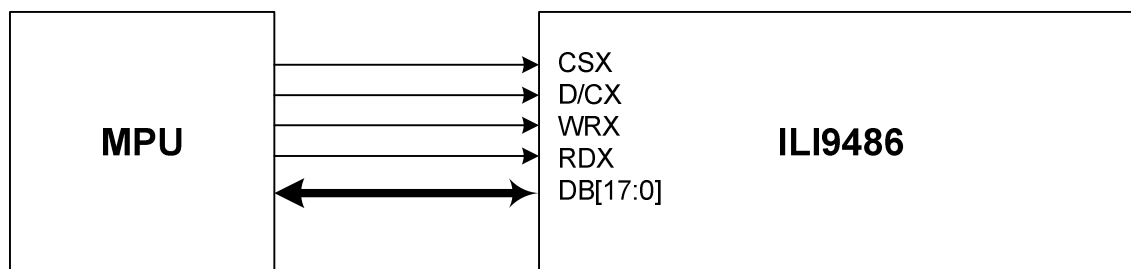
Note 2: 2-times transfer is used to transmit 1 pixel data with the 18-bits color depth information.

Note 3: '-'= Don't care – Leave these pins to Open.

7.5.6. 18-bit Parallel MCU Interface

The 8080-system 18-bit parallel bus interface of ILI9486L can be used by setting external pin as IM [2:0] to "000".

The figure in the following is the example of interface with 8080 microcomputer system interface.

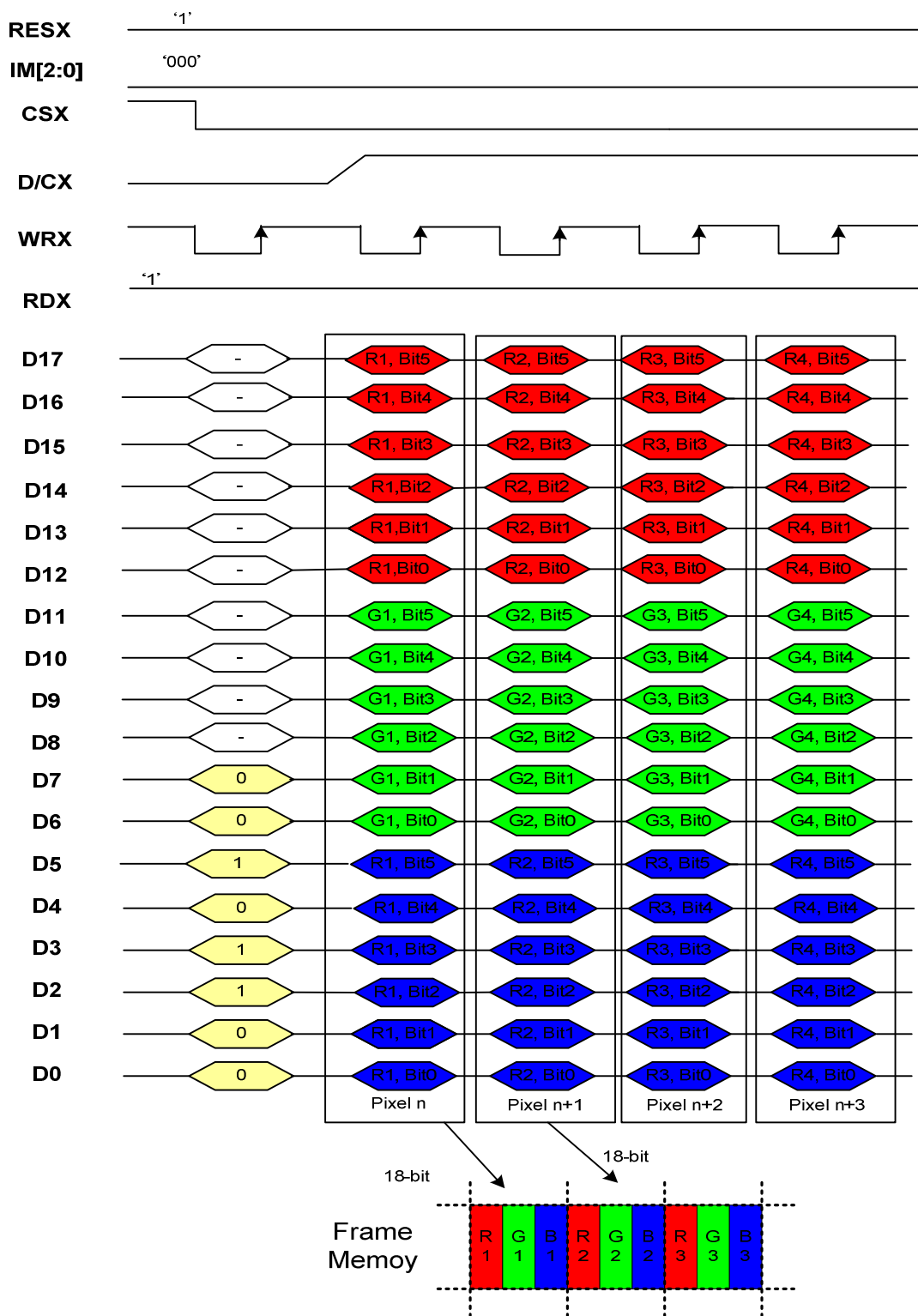


Different display data formats are available for one color depth only supported by listed below.

- 262K-Colors, RGB 6, 6, 6 -bits input data.

7.5.6.1. 18-bit Data Bus for 18-bit/pixel (RGB 6-6-6 bits input), 262K-color

18 bit/pixel color order (R:6-bit, G:6-bit, B:6-bit), 262,144 colors



Note 1: The data order is as follows, MSB=D17, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green and MSB=Bit4, LSB=Bit0 for Red and Blue data.

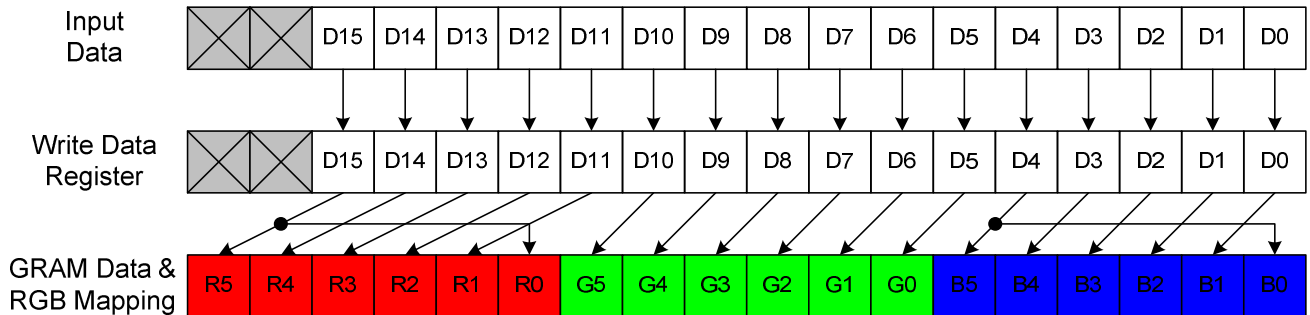
Note 2: 1-times transfer is used to transmit 1 pixel data with the 16-bits color depth information.

Note 3: '-'= Don't care – Leave these pins to Open.

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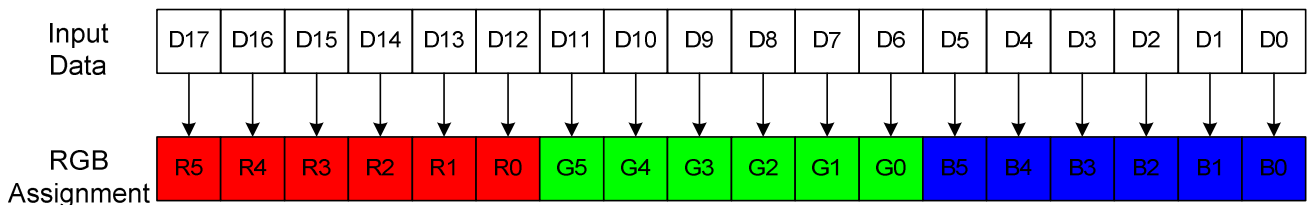
7.5.7. 16-bit Parallel RGB Interface

The 16-bit RGB interface is selected by setting the DPI[2:0] bits to “101”. The display operation is synchronized with VSYNC, HSYNC and DOTCLK signals. The display data are transferred to the internal GRAM in synchronization with the display operation via 16-bit RGB data bus (D[15:0]). Both D17 and D16 pins must be left to OPEN for ensure normally operation. Registers can be set by the system interface.



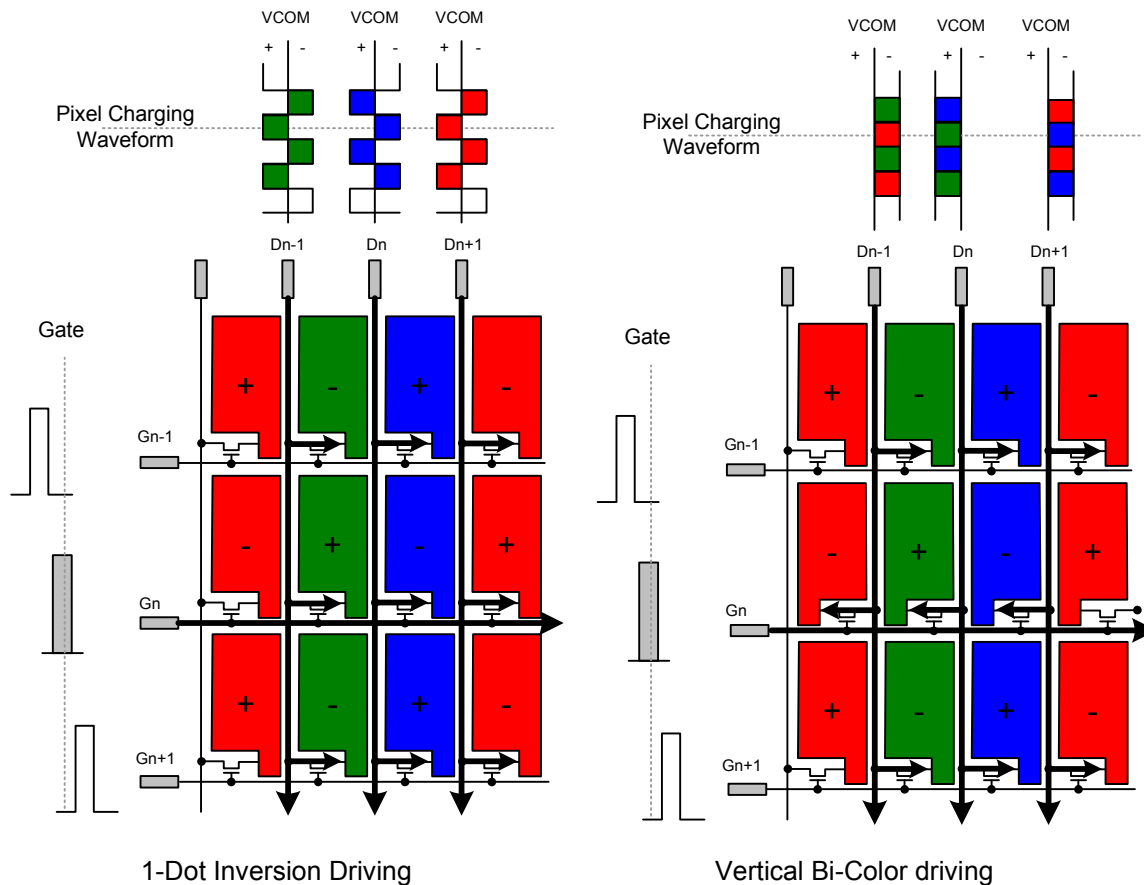
7.5.8. 18-bit Parallel RGB Interface

The 18-bit RGB interface is selected by setting the DPI[2:0] bits to “110”. The display operation is synchronized with VSYNC, HSYNC and DOTCLK signals. The display data are transferred to the internal GRAM in synchronization with the display operation via 18-bit RGB data bus (DB[17:0]) according to the data enable signal (ENABLE). Registers can be set by the system interface.



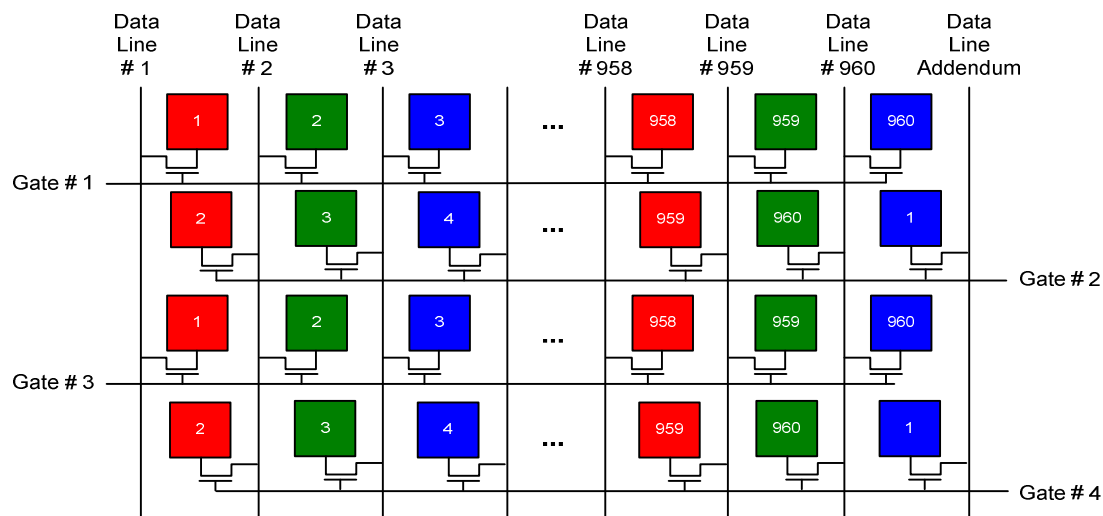
7.6. Z-inversion

The ILI9486L supports Z-inversion for reduce power consumption. The Zigzag can decrease the switching frequency, relative to the magnitude of the display power consumption, and the switching level. This method will have a addendum data line after the last data line.

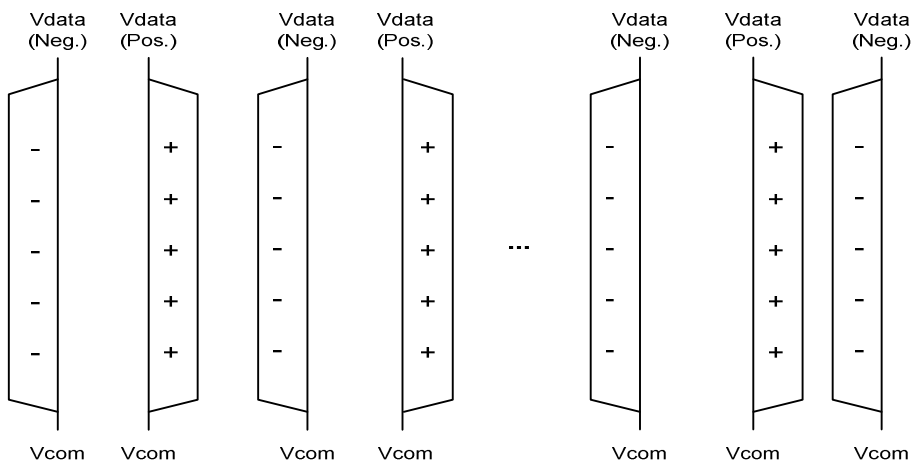


7.8.1 Z-inversion concept

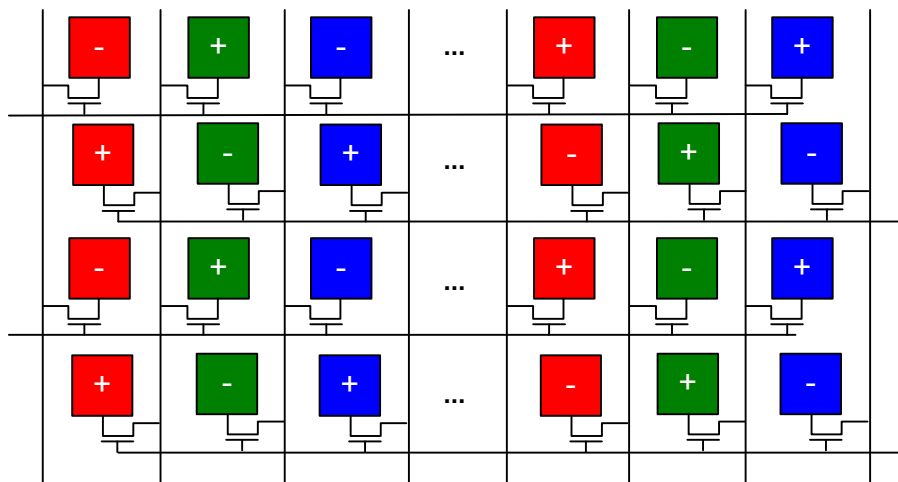
The Zigzag method uses the same polarity of data line of the column inversion to show out the 1-dot inversion.



Column Inversion



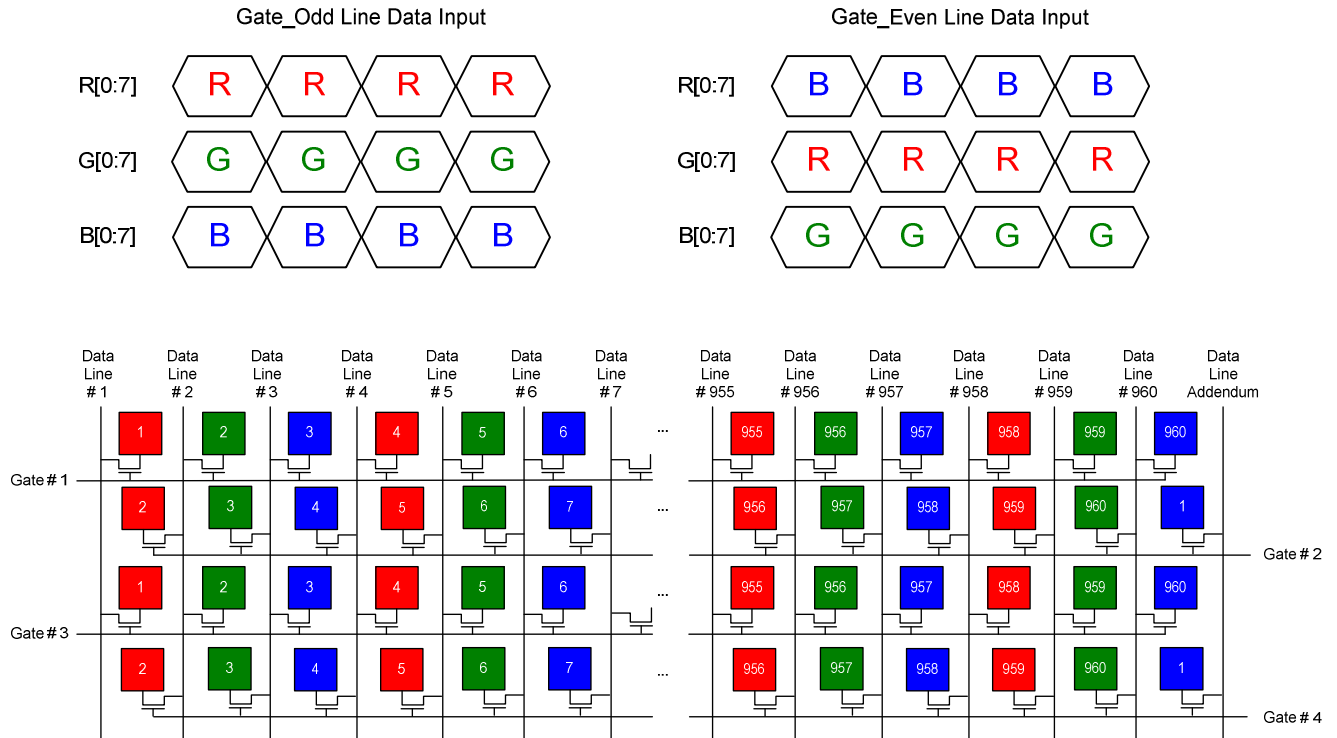
1-Dot Inversion



7.8.2 Z-inversion Odd/Even Gate data input method

Gate_Odd line : using the normally data input mode and put on the R, G, B data to sub-pixel R, G, B respectively.

Gate_Even line : put on the G, B, R data to sub-pixel R, G, B respectively.



7.8.3 Z-inversion data input method

The driving panel display method is that added the one sub pixel at the Gate_Even shift the data output.

Red

	Data # 1	Data # 2	Data # 3	Data # 4	Data # 5	Data # 6		Data # 955	Data # 956	Data # 957	Data # 958	Data # 959	Data # 960	Data Option
Gate_Odd	R	G	B	R	G	B	...	R	G	B	R	G	B	
Gate_Even	R	G	B	R	G	B		R	G	B	R	G	B	
Gate_Odd	R	G	B	R	G	B		R	G	B	R	G	B	
Gate_Even	R	G	B	R	G	B		R	G	B	R	G	B	

Green

	Data # 1	Data # 2	Data # 3	Data # 4	Data # 5	Data # 6		Data # 955	Data # 956	Data # 957	Data # 958	Data # 959	Data # 960	Data Option
Gate_Odd	R	G	B	R	G	B	...	R	G	B	R	G	B	
Gate_Even	R	G	B	R	G	B		R	G	B	R	G	B	
Gate_Odd	R	G	B	R	G	B		R	G	B	R	G	B	
Gate_Even	R	G	B	R	G	B		R	G	B	R	G	B	

Blue

	Data # 1	Data # 2	Data # 3	Data # 4	Data # 5	Data # 6		Data # 955	Data # 956	Data # 957	Data # 958	Data # 959	Data # 960	Data Option
Gate_Odd	R	G	B	R	G	B	...	R	G	B	R	G	B	
Gate_Even	R	G	B	R	G	B		R	G	B	R	G	B	
Gate_Odd	R	G	B	R	G	B		R	G	B	R	G	B	
Gate_Even	R	G	B	R	G	B		R	G	B	R	G	B	

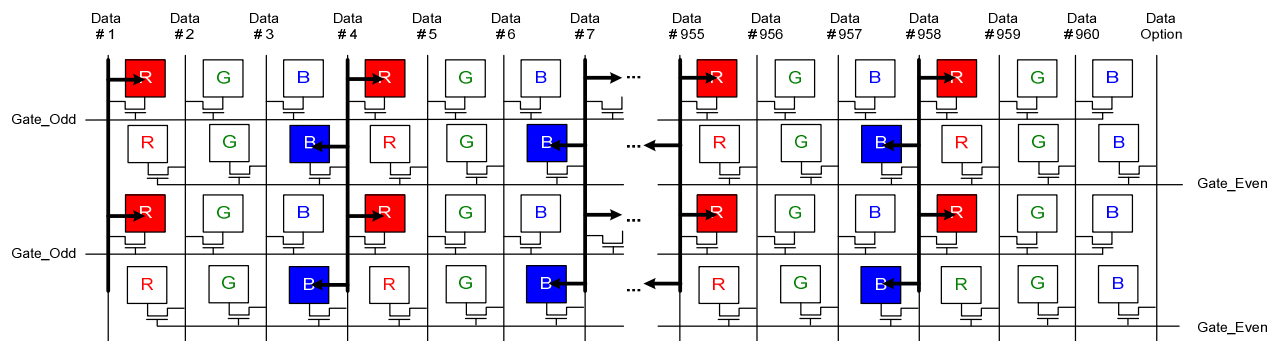
7.8.3.1 Z-inversion RED Data display

The below figure is normally panel driving method for Red data input. For driving Red pattern, the Red and Blue sub pixel will light up line by line when the data signal input.

Input Data Signal

	Data #1	Data #2	Data #3	Data #4	Data #5	Data #6		Data #955	Data #956	Data #957	Data #958	Data #959	Data #960	Data Option
Gate_Odd	R	G	B	R	G	B		R	G	B	R	G	B	
Gate_Even	R	G	B	R	G	B	...	R	G	B	R	G	B	
Gate_Odd	R	G	B	R	G	B		R	G	B	R	G	B	
Gate_Even	R	G	B	R	G	B		R	G	B	R	G	B	

Panel Driving

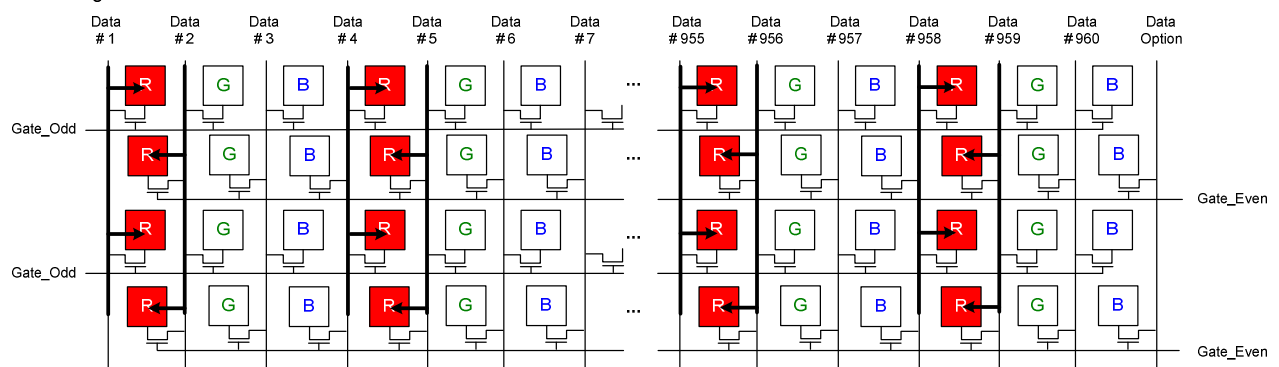


The below figure is Z-inversion panel driving method. The panel will be drive by the Red data input of the Gate_Odd and the Green data input of the Gate_Even.

Input Data Signal

	Data #1	Data #2	Data #3	Data #4	Data #5	Data #6		Data #955	Data #956	Data #957	Data #958	Data #959	Data #960	Data Option
Gate_Odd	R	G	B	R	G	B		R	G	B	R	G	B	
Gate_Even	R	G	B	R	G	B	...	R	G	B	R	G	B	
Gate_Odd	R	G	B	R	G	B		R	G	B	R	G	B	
Gate_Even	R	G	B	R	G	B		R	G	B	R	G	B	

Panel Driving



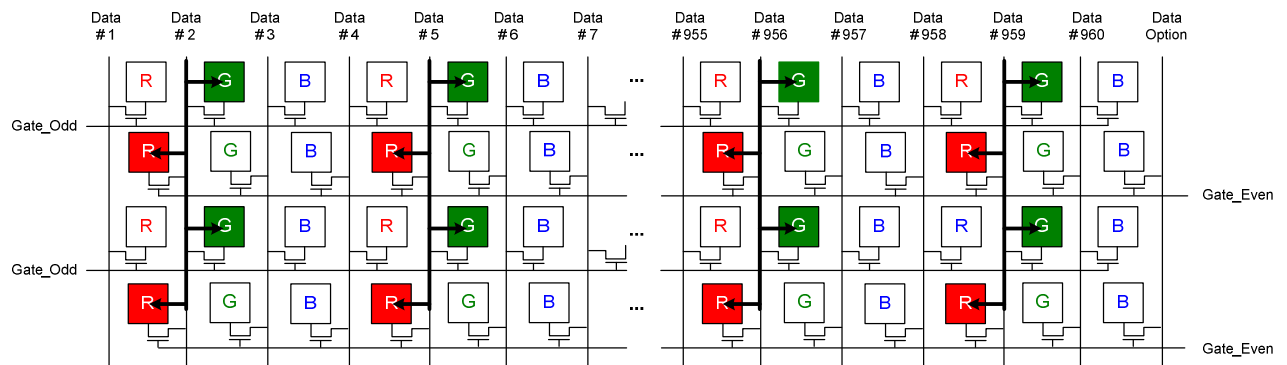
7.8.3.2 Z-inversion GREEN Data display

The below figure is normally panel driving method for Green data input. For driving Green pattern, the Green and Red sub pixel will light up line by line when the data signal input.

Input Data Signal

	Data #1	Data #2	Data #3	Data #4	Data #5	Data #6		Data #955	Data #956	Data #957	Data #958	Data #959	Data #960	Data Option
Gate_Odd	R	G	B	R	G	B		R	G	B	R	G	B	
Gate_Even	R	G	B	R	G	B	...	R	G	B	R	G	B	
Gate_Odd	R	G	B	R	G	B		R	G	B	R	G	B	
Gate_Even	R	G	B	R	G	B		R	G	B	R	G	B	

Panel Driving

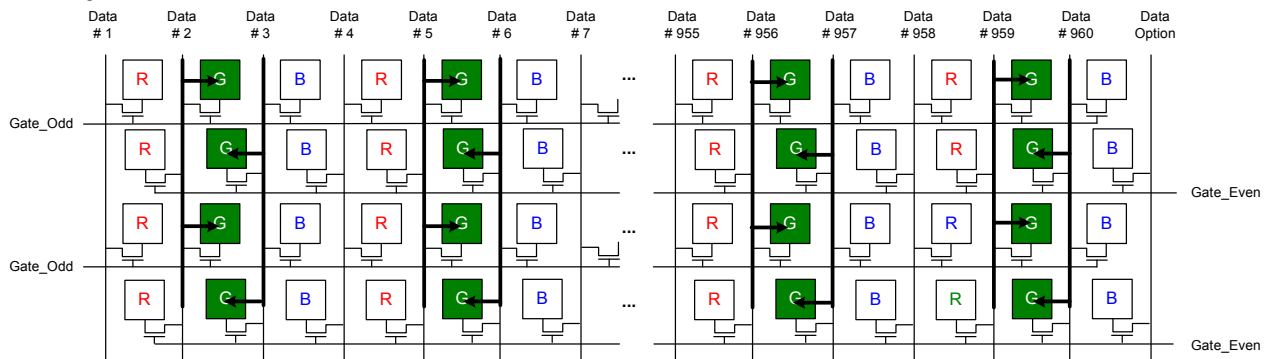


The below figure is Z-inversion panel driving method. The panel will be drive by the Green data input of the Gate_Odd and the Blue data input of the Gate_Even.

Input Data Signal

	Data #1	Data #2	Data #3	Data #4	Data #5	Data #6		Data #955	Data #956	Data #957	Data #958	Data #959	Data #960	Data Option
Gate_Odd	R	G	B	R	G	B		R	G	B	R	G	B	
Gate_Even	R	G	B	R	G	B	...	R	G	B	R	G	B	
Gate_Odd	R	G	B	R	G	B		R	G	B	R	G	B	
Gate_Even	R	G	B	R	G	B		R	G	B	R	G	B	

Panel Driving



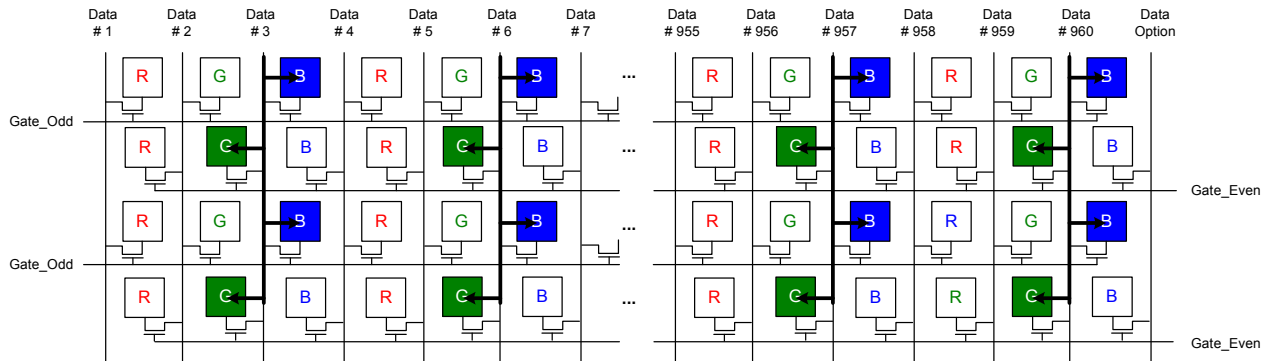
7.8.3.3 Z-inversion BLUE Data display

The below figure is normally panel driving method for Blue data input. For driving Blue pattern, the Blue and Green sub pixel will light up line by line when the data signal input.

Input Data Signal

	Data # 1	Data # 2	Data # 3	Data # 4	Data # 5	Data # 6		Data # 955	Data # 956	Data # 957	Data # 958	Data # 959	Data # 960	Data Option
Gate_Odd	R	G	B	R	G	B		R	G	B	R	G	B	
Gate_Even	R	G	B	R	G	B	...	R	G	B	R	G	B	
Gate_Odd	R	G	B	R	G	B		R	G	B	R	G	B	
Gate_Even	R	G	B	R	G	B		R	G	B	R	G	B	

Panel Driving

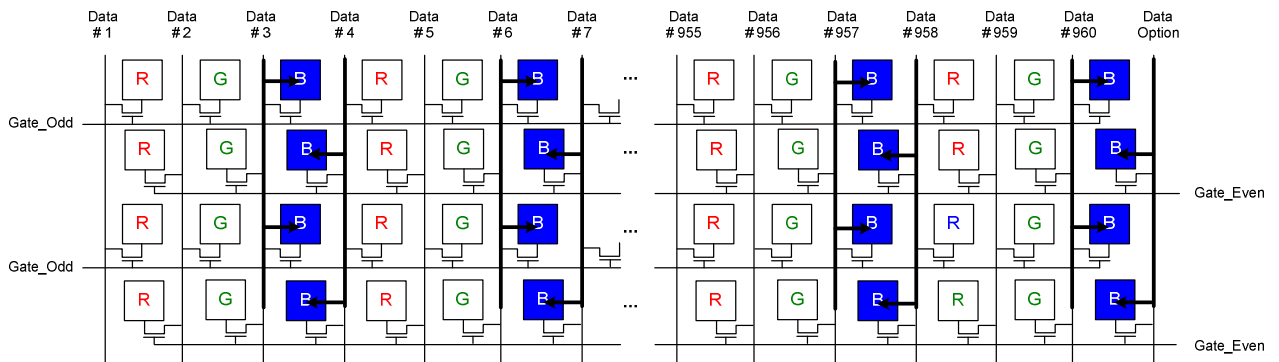


The below figure is Z-inversion panel driving method. The panel will be drive by the Blue data input of the Gate_Odd and the Red data input of the Gate_Even.

Input Data Signal

	Data # 1	Data # 2	Data # 3	Data # 4	Data # 5	Data # 6		Data # 955	Data # 956	Data # 957	Data # 958	Data # 959	Data # 960	Data Option
Gate_Odd	R	G	B	R	G	B		R	G	B	R	G	B	
Gate_Even	R	G	B	R	G	B	...	R	G	B	R	G	B	
Gate_Odd	R	G	B	R	G	B		R	G	B	R	G	B	
Gate_Even	R	G	B	R	G	B		R	G	B	R	G	B	

Panel Driving



8. Command

8.1. Command List

Regular Command Set														
Command Function	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex	
NOP	0	1	↑	XXXXXXXX	0	0	0	0	0	0	0	0	00h	
Soft Reset	0	1	↑	XXXXXXXX	0	0	0	0	0	0	0	1	01h	
Read display identification information	0	1	↑	XXXXXXXX	0	0	0	0	0	1	0	0	04h	
	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX	
	1	↑	1	XXXXXXXX	ID1 [7:0]							XX		
	1	↑	1	XXXXXXXX	ID2 [7:0]							XX		
	1	↑	1	XXXXXXXX	ID3 [7:0]							XX		
Read Number of the Errors on DSI	0	↑	1	XXXXXXXX	0	0	0	0	0	1	0	1	05h	
	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX	
	1	↑	1	XXXXXXXX	P[7:0]							XX		
Read Display Status	0	↑	1	XXXXXXXX	0	0	0	0	1	0	0	1	09h	
	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX	
	1	↑	1	XXXXXXXX	D[31:24]							XX		
	1	↑	1	XXXXXXXX	D[23:16]							XX		
	1	↑	1	XXXXXXXX	D[15:8]							XX		
	1	↑	1	XXXXXXXX	D[7:0]							XX		
Read Display Power Mode	0	↑	1	XXXXXXXX	0	0	0	0	1	0	1	0	0Ah	
	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX	
	1	↑	1	XXXXXXXX	D[7:2]							0	0	XX
Read Display MADCTL	0	↑	1	XXXXXXXX	0	0	0	0	1	0	1	1	0Bh	
	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX	
	1	↑	1	XXXXXXXX	D[7:2]							0	0	XX
Read Pixel Format	0	↑	1	XXXXXXXX	0	0	0	0	1	1	0	0	0Ch	
	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX	
	1	↑	1	XXXXXXXX	DPI[3:0]					0	DBI[2:0]		XX	
Read Display Image Mode	0	↑	1	XXXXXXXX	0	0	0	0	1	1	0	1	0Dh	
	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX	
	1	↑	1	XXXXXXXX	D[7:0]									XX
Read Display signal Mode	0	↑	1	XXXXXXXX	0	0	0	0	1	1	1	0	0Eh	
	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX	
	1	↑	1	XXXXXXXX	D7	D6	D5	D4	D3	D2	D1	D0	XX	
Read Display Self-Diagnostic Result	0	↑	1	XXXXXXXX	0	0	0	0	1	1	1	1	0Fh	
	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX	
	1	↑	1	XXXXXXXX	D7	D6	0	0	0	0	0	D0	XX	
Sleep IN	0	1	↑	XXXXXXXX	0	0	0	1	0	0	0	0	10h	
Sleep OUT	0	1	↑	XXXXXXXX	0	0	0	1	0	0	0	1	11h	
Partial Mode ON	0	1	↑	XXXXXXXX	0	0	0	1	0	0	1	0	12h	
Normal Display Mode ON	0	1	↑	XXXXXXXX	0	0	0	1	0	0	1	1	13h	
Display Inversion OFF	0	1	↑	XXXXXXXX	0	0	1	0	0	0	0	0	20h	
Display Inversion ON	0	1	↑	XXXXXXXX	0	0	1	0	0	0	0	1	21h	
Display OFF	0	1	↑	XXXXXXXX	0	0	1	0	1	0	0	0	28h	
Display ON	0	1	↑	XXXXXXXX	0	0	1	0	1	0	0	1	29h	
Column Address Set	0	1	↑	XXXXXXXX	0	0	1	0	1	0	1	0	2Ah	
	1	1	↑	XXXXXXXX	SC[15:8]									XX
	1	1	↑	XXXXXXXX	SC[7:0]									XX
	1	1	↑	XXXXXXXX	EC[15:8]									XX
	1	1	↑	XXXXXXXX	EC[7:0]									XX
Page Address Set	0	1	↑	XXXXXXXX	0	0	1	0	1	0	1	1	2Bh	
	1	1	↑	XXXXXXXX	SP[15:8]									XX
	1	1	↑	XXXXXXXX	SP[7:0]									XX
	1	1	↑	XXXXXXXX	EP[15:8]									XX
	1	1	↑	XXXXXXXX	EP[7:0]									XX
Memory Write	0	1	↑	XXXXXXXX	0	0	1	0	1	1	0	0	2Ch	
	1	1	↑	D1[15:0]										XX
	1	1	↑	Dx[15:0]										XX
	1	1	↑	Dn[15:0]										XX
Memory Read	0	↑	1	XXXXXXXX	0	0	1	0	1	1	1	0	2Eh	
	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX	

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	1	↑	1	D1[15:0]									XX
	1	↑	1	Dx[15:0]									XX
	1	↑	1	Dn[15:0]									XX
Partial Area	1	↑	1	XXXXXXXX	Pn[7:0]								XX
	0	1	↑	XXXXXXXX	0	0	1	1	0	0	0	0	30h
	1	1	↑	XXXXXXXX	SR[15:8]								XX
	1	1	↑	XXXXXXXX	SR[7:0]								XX
	1	1	↑	XXXXXXXX	ER[15:8]								XX
	1	1	↑	XXXXXXXX	ER[7:0]								XX
Vertical Scrolling Definition	0	1	↑	XXXXXXXX	0	0	1	1	0	0	1	1	33h
	1	1	↑	XXXXXXXX	TFA[15:8]								XX
	1	1	↑	XXXXXXXX	TFA[7:0]								XX
	1	1	↑	XXXXXXXX	VSA[15:8]								XX
	1	1	↑	XXXXXXXX	VSA[7:0]								XX
	1	1	↑	XXXXXXXX	BFA[15:8]								XX
	1	1	↑	XXXXXXXX	BFA[7:0]								XX
Tearing Effect Line OFF	0	1	↑	XXXXXXXX	0	0	1	1	0	1	0	0	34h
Tearing Effect Line ON	0	1	↑	XXXXXXXX	0	0	1	1	0	1	0	1	35h
Memory Access Control	0	1	↑	XXXXXXXX	0	0	1	1	0	1	1	0	36h
	1	1	↑	XXXXXXXX	MY	MX	MV	ML	BGR	MH	X	X	XX
Vertical Scrolling Start Address	0	1	↑	XXXXXXXX	0	0	1	1	0	1	1	1	37h
	1	1	↑	XXXXXXXX	VSP[15:8]								XX
	1	1	↑	XXXXXXXX	VSP[7:0]								XX
Idle Mode OFF	0	1	↑	XXXXXXXX	0	0	1	1	1	0	0	0	38h
Idle Mode ON	0	1	↑	XXXXXXXX	0	0	1	1	1	0	0	1	39h
Interface Pixel Format	0	1	↑	XXXXXXXX	0	0	1	1	1	0	1	0	3Ah
	1	1	↑	XXXXXXXX	0	DPI[6:4]			0	DBI[2:0]			XX
Memory Write Continue	0	1	↑	XXXXXXXX	0	0	1	1	1	1	0	0	3Ch
	1	1	↑	D1[15:0]									XX
	1	1	↑	Dx[15:0]									XX
	1	1	↑	Dn[15:0]									XX
Memory Read Continue	0	↑	1	XXXXXXXX	0	0	1	1	1	1	1	0	3Eh
	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX
	1	↑	1	D1[15:0]									XX
	1	↑	1	Dx[15:0]									XX
	1	↑	1	Dn[15:0]									XX
Write Tear Scan line	0	1	↑	XXXXXXXX	0	1	0	0	0	1	0	0	44h
	1	1	↑	XXXXXXXX	N[15:8]								XX
	1	1	↑	XXXXXXXX	N[7:0]								XX
Read Tear Scan Line	0	↑	1	XXXXXXXX	0	1	0	0	0	1	0	1	45h
	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XXXXXXXX	N[15:8]								XX
	1	↑	1	XXXXXXXX	N[7:0]								XX
Write Display Brightness value	0	1	↑	XXXXXXXX	0	1	0	1	0	0	0	1	51h
	1	1	↑	XXXXXXXX	DBV[7:0]								XX
Read Display Brightness Value	0	1	↑	XXXXXXXX	0	1	0	1	1	0	1	0	52h
	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XXXXXXXX	DBV[7:0]								XX
Write CTRL Display value	0	1	↑	XXXXXXXX	0	1	0	1	0	0	1	1	53h
	1	1	↑	XXXXXXXX	0	0	BCTRL	0	DD	BL	0	0	XX
Read CTRL Display value	0	1	↑	XXXXXXXX	0	1	0	1	0	1	0	0	54h
	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XXXXXXXX	0	0	BCTRL	0	DD	BL	0	0	XX
Write Content Adaptive Brightness Control value	0	1	↑	XXXXXXXX	0	1	0	1	0	1	0	1	55h
	1	1	↑	XXXXXXXX	0	0	0	0	0	0	C[1:0]		XX
Read Content Adaptive Brightness Control value	0	1	↑	XXXXXXXX	0	1	0	1	0	1	1	0	56h
	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XXXXXXXX	0	0	0	0	0	0	C[1:0]		XX
Write CABC Minimum Brightness	0	1	↑	XXXXXXXX	0	1	0	1	1	1	1	0	5Eh
	1	1	↑	XXXXXXXX	CMB[7:0]								XX
Read CABC Minimum Brightness	0	1	↑	XXXXXXXX	0	1	0	1	1	1	1	1	5Fh
	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XXXXXXXX	CMB[7:0]								XX
Read First Checksum	0	1	↑	XXXXXXXX	1	0	1	0	1	0	1	0	AAh
	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX

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	1	↑	1	XXXXXXXX	FCS[7:0]								XX
Read Continue Checksum	0	1	↑	XXXXXXXX	1	0	1	0	1	1	1	1	AFh
	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XXXXXXXX	CCS[7:0]								XX
Read ID1	0	1	↑	XXXXXXXX	1	1	0	1	1	0	1	0	DAh
	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XXXXXXXX	ID1[7:0]								XX
Read ID2	0	1	↑	XXXXXXXX	1	0	1	0	1	0	1	1	DBh
	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XXXXXXXX	ID2[7:0]								XX
Read ID3	0	1	↑	XXXXXXXX	1	0	1	0	1	1	0	0	DCh
	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XXXXXXXX	ID3[7:0]								XX

Extended Command Set													
Command Function	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Interface Mode Control	0	1	↑	XXXXXXXX	1	0	1	1	0	0	0	0	B0h
	1	1	↑	XXXXXXXX	SDA_EN	0	0	0	VSPL	HSPL	DPL	EPL	XX
Frame Rate Control (In Normal Mode/Full Colors)	0	1	↑	XXXXXXXX	1	0	1	1	0	0	0	1	B1h
	1	1	↑	XXXXXXXX	FRS[3:0]				0	0	DIVA[1:0]		XX
	1	1	↑	XXXXXXXX	0	0	0	RTNA[4:0]				XX	
Frame Rate Control (In Idle Mode/8 colors)	0	1	↑	XXXXXXXX	1	0	1	1	0	0	1	0	B2h
	1	1	↑	XXXXXXXX	0	0	0	0	0	0	DIVB[1:0]		XX
	1	1	↑	XXXXXXXX	0	0	0	RTNB[4:0]				XX	
Frame Rate Control (In Partial Mode/Full colors)	0	1	↑	XXXXXXXX	1	0	1	1	0	0	1	1	B3h
	1	1	↑	XXXXXXXX	0	0	0	0	0	0	DIVC[1:0]		XX
	1	1	↑	XXXXXXXX	0	0	0	RTN[4:0]				XX	
Display Inversion Control	0	1	↑	XXXXXXXX	1	0	1	1	0	1	0	0	B4h
	1	1	↑	XXXXXXXX	0	0	0	ZINV	0	0	DINV[1:0]		XX
Blanking Porch Control	0	1	↑	XXXXXXXX	1	0	1	1	0	1	0	1	B5h
	1	1	↑	XXXXXXXX	VFP[7:0]								XX
	1	1	↑	XXXXXXXX	VBP[7:0]								XX
	1	1	↑	XXXXXXXX	0	0	0	HFP[4:0]				XX	
	1	1	↑	XXXXXXXX	HBP[7:0]								XX
Display Function Control	0	1	↑	XXXXXXXX	1	0	1	1	0	1	1	0	B6h
	1	1	↑	XXXXXXXX	BYPASS	0	RM	DM	PTG[1:0]		PT[1:0]		XX
	1	1	↑	XXXXXXXX	0	GS	SS	SM	ISC[3:0]				XX
	1	1	↑	XXXXXXXX	0	0	NL[5:0]						XX
Entry Mode Set	0	1	↑	XXXXXXXX	1	0	1	1	0	1	1	1	B7h
	1	1	↑	XXXXXXXX	EPF[1:0]		0	0	DSTB	GON	DTE	GAS	XX
Power Control 1	0	1	↑	XXXXXXXX	1	1	0	0	0	0	0	0	C0h
	1	1	↑	XXXXXXXX	0	0	0	VRH1[4:0]				XX	
	1	1	↑	XXXXXXXX	0	0	0	VRH2[4:0]				XX	
Power Control 2	0	1	↑	XXXXXXXX	1	1	0	0	0	0	0	1	C1h
	1	1	↑	XXXXXXXX	0	0	0	0	0	BT[2:0]			XX
	1	1	↑	XXXXXXXX	0	0	0	0	0	VC[2:0]			XX
Power Control 3	0	1	↑	XXXXXXXX	1	1	0	0	0	0	1	0	C2h
	1	1	↑	XXXXXXXX	0	DCA1[2:0]			0	DCA0[2:0]			XX
Power Control 4	0	1	↑	XXXXXXXX	1	1	0	0	0	0	1	1	C3h
	1	1	↑	XXXXXXXX	0	DCB1[2:0]			0	DCB0[2:0]			XX
Power Control 5	0	1	↑	XXXXXXXX	1	1	0	0	0	1	0	0	C4h
	1	1	↑	XXXXXXXX	0	DCC2[2:0]			0	DCC0[2:0]			XX
VCOM Control 1	0	↑	1	XXXXXXXX	1	1	0	0	0	1	0	1	C5h
	1	1	↑	XXXXXXXX	0	0	0	0	0	0	0	nVM	XX
	1	1	↑	XXXXXXXX	VCM_REG[7:0]								XX
	1	1	↑	XXXXXXXX	VCM_REG_EN	0	0	0	0	0	0	0	XX
	1	↑	1	XXXXXXXX	VCM_OUT[7:0]								XX
CABC Control 1	0	1	↑	XXXXXXXX	1	1	0	0	0	1	1	0	C6h

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	1	1	↑	XXXXXXXXXX	SCD_VLINE[7:0]								XX	
	1	1	↑	XXXXXXXXXX	0	0	0	0	0	SCD_VLINE[10:8]			XX	
CABC Control 2	0	1	↑	XXXXXXXXXX	1	1	0	0	1	0	0	0	C8h	
	1	1	↑	XXXXXXXXXX	0	0	0	0	0	LEDONR	LEDONPOL	PWMPOL	XX	
	1	1	↑	XXXXXXXXXX	PWM_DIV[7:0]								XX	
	0	1	↑	XXXXXXXXXX	1	1	0	0	1	0	0	1	C9h	
CABC Control 3	1	1	↑	XXXXXXXXXX	THRES_MOV[3:0]				THRES_STILL[3:0]				XX	
	0	1	↑	XXXXXXXXXX	1	1	0	0	1	0	1	0	CAh	
CABC Control 4	1	1	↑	XXXXXXXXXX	0	0	0	0	THRES_UI[3:0]				XX	
	0	1	↑	XXXXXXXXXX	1	1	0	0	1	0	1	1	CBh	
CABC Control 5	1	1	↑	XXXXXXXXXX	DTH_MOV[3:0]				DTH_STILL[3:0]				XX	
	0	1	↑	XXXXXXXXXX	1	1	0	0	1	1	0	0	CCh	
CABC Control 6	1	1	↑	XXXXXXXXXX	0	0	0	0	DTH_UI[3:0]				XX	
	0	1	↑	XXXXXXXXXX	1	1	0	0	1	1	0	1	CDh	
CABC Control 7	1	1	↑	XXXXXXXXXX	0	DIM_MOV[2:0]			0	DIM_STILL[2:0]			XX	
	0	1	↑	XXXXXXXXXX	1	1	0	0	1	1	1	0	CEh	
CABC Control 8	1	1	↑	XXXXXXXXXX	DIM_MIN[3:0]				0	DIM_UI[2:0]			XX	
	0	1	↑	XXXXXXXXXX									CFh	
CABC Control 9	1	1	↑	XXXXXXXXXX	PWM_DIV[7:0]								XX	
	0	1	↑	XXXXXXXXXX	1	1	0	1	0	0	0	0	D0h	
NV Memory Write	1	1	↑	XXXXXXXXXX	0	0	0	PGM_ADR[4:0]						XX
	1	1	↑	XXXXXXXXXX	PGM_DATA[7:0]								XX	
	0	1	↑	XXXXXXXXXX	1	1	0	1	0	0	0	1	D1h	
NV Memory Protection Key	1	1	↑	XXXXXXXXXX	KEY[23:16]								XX	
	0	↑	1	XXXXXXXXXX	KEY[15:8]								XX	
	1	↑	1	XXXXXXXXXX	KEY[7:0]								XX	
	1	↑	1	XXXXXXXXXX	1	1	0	1	0	0	1	0	D2h	
NV Memory Status Read	1	↑	1	XXXXXXXXXX	X	X	X	X	X	X	X	X	XX	
	0	1	↑	XXXXXXXXXX	ID2_CNT[3:0]				ID1_CNT[3:0]				XX	
	1	1	↑	XXXXXXXXXX	VMF_CNT[3:0]				ID3_CNT[3:0]				XX	
	1	1	↑	XXXXXXXXXX	BUSY	0	0	0	0	0	0	0	XX	
	1	1	↑	XXXXXXXXXX	OTP_DATA[7:0]								XX	
	0	↑	1	XXXXXXXXXX	1	1	0	1	0	0	1	1	D3h	
Read ID4	1	↑	1	XXXXXXXXXX	X	X	X	X	X	X	X	X	XX	
	1	↑	1	XXXXXXXXXX	ID41[7:0]								XX	
	1	↑	1	XXXXXXXXXX	ID42[7:0]								XX	
	1	↑	1	XXXXXXXXXX	ID43[7:0]								XX	
	0	1	↑	XXXXXXXXXX	1	1	1	0	0	0	0	0	E0h	
PGAMCTRL (Positive Gamma Control)	1	1	↑	XXXXXXXXXX	0	0	0	0	VP0[3:0]				XX	
	1	1	↑	XXXXXXXXXX	0	0	VP1[5:0]						XX	
	1	1	↑	XXXXXXXXXX	0	0	VP2[5:0]						XX	
	1	1	↑	XXXXXXXXXX	0	0	0	0	VP4[3:0]				XX	
	1	1	↑	XXXXXXXXXX	0	0	0	VP6[4:0]					XX	
	1	1	↑	XXXXXXXXXX	0	0	0	0	VP13[3:0]				XX	
	1	1	↑	XXXXXXXXXX	0	VP20[6:0]						XX		
	1	1	↑	XXXXXXXXXX	VP36[3:0]				VP27[3:0]				XX	
	1	1	↑	XXXXXXXXXX	0	VP43[6:0]						XX		
	1	1	↑	XXXXXXXXXX	0	0	0	0	VP50[3:0]				XX	
	1	1	↑	XXXXXXXXXX	0	0	0	VP57[4:0]					XX	
	1	1	↑	XXXXXXXXXX	0	0	0	0	VP59[3:0]				XX	
	1	1	↑	XXXXXXXXXX	0	0	VP61[5:0]						XX	
	1	1	↑	XXXXXXXXXX	0	0	VP62[5:0]						XX	
	1	1	↑	XXXXXXXXXX	0	0	0	0	VP63[3:0]				XX	
	NGAMCTRL (Negative Gamma Control)	0	1	↑	XXXXXXXXXX	1	1	1	0	0	0	0	1	E1h
1		1	↑	XXXXXXXXXX	0	0	0	0	VN0[3:0]				XX	
1		1	↑	XXXXXXXXXX	0	0	VN1[5:0]						XX	
1		1	↑	XXXXXXXXXX	0	0	VN2[5:0]						XX	

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	1	1	↑	XXXXXXXX	0	0	0	0	VN4[3:0]				XX
	1	1	↑	XXXXXXXX	0	0	0	VN6[4:0]				XX	
	1	1	↑	XXXXXXXX	0	0	0	VN13[3:0]				XX	
	1	1	↑	XXXXXXXX	0	VN20[6:0]				XX			
	1	1	↑	XXXXXXXX	VN36[3:0]				VN27[3:0]				XX
	1	1	↑	XXXXXXXX	0	VN43[6:0]				XX			
	1	1	↑	XXXXXXXX	0	0	0	0	VN50[3:0]				XX
	1	1	↑	XXXXXXXX	0	0	0	VN57[4:0]				XX	
	1	1	↑	XXXXXXXX	0	0	0	0	VN59[3:0]				XX
	1	1	↑	XXXXXXXX	0	0	VN61[5:0]				XX		
	1	1	↑	XXXXXXXX	0	0	VN62[5:0]				XX		
	1	1	↑	XXXXXXXX	0	0	0	0	VN63[3:0]				XX
Digital Gamma Control 1	0	1	↑	XXXXXXXX	1	1	1	0	0	0	0	1	E2h
	1	1	↑	XXXXXXXX	RCA0[3:0]				BCA0[3:0]				XX
	1	1	↑	XXXXXXXX	RCAx[3:0]				BCAx[3:0]				XX
	1	1	↑	XXXXXXXX	RCA63[3:0]				BCA63[3:0]				XX
Digital Gamma Control 2	0	1	↑	XXXXXXXX	1	1	1	0	0	0	0	1	E3h
	1	1	↑	XXXXXXXX	RFA0[3:0]				BFA0[3:0]				XX
	1	1	↑	XXXXXXXX	RFAx[3:0]				BFAx[3:0]				XX
	1	1	↑	XXXXXXXX	RFA255[3:0]				BFA255[3:0]				XX
SPI Read Command Setting	0	1	↑	XXXXXXXX	1	1	1	1	1	0	1	1	FBh
	1	1	↑	XXXXXXXX	0	0	0	SPI READ EN		SPI CNT[3:0]			

8.2. Command Description

8.2.1. NOP (00h)

00h	NOP (No Operation)																								
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XXXXXXXX	0	0	0	0	0	0	0	0	00h												
Parameter	No parameter																								
Description	<p>This command is an empty command; it does not have any effect on ILI9486L. However it can be used to terminate Frame Memory Write or Read as described in RAMWR (Memory Write) and RAMRD (Memory Read) Commands.</p> <p>X = Don't care.</p>																								
Restriction	None																								
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>N/A</td></tr><tr><td>SW Reset</td><td>N/A</td></tr><tr><td>HW Reset</td><td>N/A</td></tr></table>													Status	Default Value	Power On Sequence	N/A	SW Reset	N/A	HW Reset	N/A				
Status	Default Value																								
Power On Sequence	N/A																								
SW Reset	N/A																								
HW Reset	N/A																								
Flow Chart	None																								

8.2.2. Soft Reset (01h)

01h	SWRESET (Soft Reset)																								
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XXXXXXXX	0	0	0	0	0	0	0	1	01h												
Parameter	No parameter																								
Description	<p>When the Software Reset command is written, it causes software reset. It resets the commands and parameters to their S/W Reset default values. (See default tables in each command description.)</p> <p>The display is blank immediately</p> <p>Note: The Frame Memory contents is kept or not by this command.</p> <p>X = Don't care</p>																								
Restriction	<p>It will be necessary to wait 5msec before sending new command following software reset. The display module loads all display supplier factory default values to the registers during this 5msec. If Software Reset is applied during Sleep Out mode, it will be necessary to wait 120msec before sending Sleep out command. Software Reset Command cannot be sent during Sleep Out sequence.</p>																								
Register Availability	<table><thead><tr><th>Status</th><th>Availability</th></tr></thead><tbody><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></tbody></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
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Sleep In	Yes																								
Default	<table><thead><tr><th>Status</th><th>Default Value</th></tr></thead><tbody><tr><td>Power On Sequence</td><td>N/A</td></tr><tr><td>SW Reset</td><td>N/A</td></tr><tr><td>HW Reset</td><td>N/A</td></tr></tbody></table>													Status	Default Value	Power On Sequence	N/A	SW Reset	N/A	HW Reset	N/A				
Status	Default Value																								
Power On Sequence	N/A																								
SW Reset	N/A																								
HW Reset	N/A																								
Flow Chart	<div><div><div>SWRESET(01h)</div><div>Display whole blank screen</div><div>Set Commands to S/W Default Values</div><div>Sleep In Mode</div></div><div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div></div>																								

8.2.3. Read display identification information (04h)

04h	RDDIDIF (Read Display Identification Information)																								
	D/CX	RDX	WRX	D[17:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	0	0	0	0	0	1	0	0	04h												
1 st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X												
2 nd Parameter	1	↑	1	XX	ID1 [7:0]								XX												
3 rd Parameter	1	↑	1	XX	ID2 [7:0]								XX												
4 th Parameter	1	↑	1	XX	ID3 [7:0]								XX												
Description	This read byte returns 24 bits display identification information.																								
	The 1 st parameter is dummy data.																								
	The 2 nd parameter (ID1 [7:0]): LCD module's manufacturer ID.																								
	The 3 rd parameter (ID2 [7:0]): LCD module/driver version ID.																								
	The 4 th parameter (ID3 [7:0]): LCD module/driver ID.																								
Restriction																									
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
	Status	Availability																							
	Normal Mode On, Idle Mode Off, Sleep Out	Yes																							
	Normal Mode On, Idle Mode On, Sleep Out	Yes																							
	Partial Mode On, Idle Mode Off, Sleep Out	Yes																							
	Partial Mode On, Idle Mode On, Sleep Out	Yes																							
Sleep In	Yes																								
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>See description</td></tr><tr><td>SW Reset</td><td>See description</td></tr><tr><td>HW Reset</td><td>See description</td></tr></table>													Status	Default Value	Power On Sequence	See description	SW Reset	See description	HW Reset	See description				
	Status	Default Value																							
	Power On Sequence	See description																							
	SW Reset	See description																							
HW Reset	See description																								
Flow Chart	<div><div><div>RDDIDIF(04h)</div><div>↓</div></div><div><div>Host</div><div>Driver</div></div><div><div>1st Parameter: Dummy Read 2nd Parameter: Send LCD module's manufacturer information 3rd Parameter: Send panel type and LCM/driver version information 4th Parameter: Send module/driver information</div></div></div> <div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div>																								

8.2.4. Read Number of the Errors on DSI (05h)

05h	RDNUMED (Read Number of the Errors on DSI)																								
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XXXXXXXX	0	0	0	0	0	1	0	1	05h												
1 st Parameter	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX												
2 nd Parameter	1	↑	1	XXXXXXXX	P[7:0]								XX												
Description	<p>The second parameter is telling a number of the errors on DSI. The more detailed description of the bits is below.</p> <p>P [6..0] bits are telling a number of the errors.</p> <p>P [7] is set to '1' if there is overflow with P[6..0] bits.</p> <p>P [7...0] bits are set to '0's (as well as RDDSM(0Eh)'s D0 is set '0' at the same time) after there is sent the second parameter information (= The read function is completed).</p> <p>This function is always returning P [7...0] = 00h if the parallel MCU interface is selected.</p> <p>X = can be '0' or '1'</p>																								
Restriction	<p>ILI9486L is sending 2nd parameter value on the data lines if the MCU wants to read more than one parameter (= more than 2 RDX cycle) on parallel MCU interface.</p> <p>Only 2nd parameter is sent on DSI (The 1st parameter is not sent).</p>																								
Register Availability	<table><thead><tr><th>Status</th><th>Availability</th></tr></thead><tbody><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></tbody></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><thead><tr><th>Status</th><th>Default Value</th></tr></thead><tbody><tr><td>Power On Sequence</td><td>08_{HEX}</td></tr><tr><td>SW Reset</td><td>08_{HEX}</td></tr><tr><td>HW Reset</td><td>08_{HEX}</td></tr></tbody></table>													Status	Default Value	Power On Sequence	08 _{HEX}	SW Reset	08 _{HEX}	HW Reset	08 _{HEX}				
Status	Default Value																								
Power On Sequence	08 _{HEX}																								
SW Reset	08 _{HEX}																								
HW Reset	08 _{HEX}																								
Flow Chart	<div><div><div>Read number of the Errors on DSI</div><div>Host</div><div>ILI9486</div><div>1st Parameter: Dummy Read 2nd Parameter: Read</div><div>P[7:0] = 00h RDDSM(0Eh)' s D0 = '0'</div></div><div><div>Legend</div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div>																								

8.2.5. Read Display Status (09h)

09h	RDDST (Read Display Status)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	0	1	0	0	1	09h
1 st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
2 nd Parameter	1	↑	1	XX	D [31:25]							0	XX
3 rd Parameter	1	↑	1	XX	0	D [22:20]			D [19:16]				XX
4 th Parameter	1	↑	1	XX	D15	0	D13	0	0	D [10:8]			XX
5 th Parameter	1	↑	1	XX	D [7:5]			0	0	0	0	0	XX
Description	This command indicates the current status of the display as described in the table below:												
	Bit	Description			Value	Status							
	D31	Booster voltage status		0	Booster OFF								
				1	Booster ON								
	D30	Row address order		0	Top to Bottom (When MADCTL B7='0')								
				1	Bottom to Top (When MADCTL B7='1')								
	D29	Column address order		0	Left to Right (When MADCTL B6='0').								
				1	Right to Left (When MADCTL B6='1').								
	D28	Row/column exchange		0	Normal Mode (When MADCTL B5='0').								
				1	Reverse Mode (When MADCTL B5='1').								
	D27	Vertical refresh		0	LCD Refresh Top to Bottom (When MADCTL B4='0')								
				1	LCD Refresh Bottom to Top (When MADCTL B4='1').								
	D26	RGB/BGR order		0	RGB (When MADCTL B3='0')								
				1	BGR (When MADCTL B3='1')								
	D25	Horizontal refresh order		0	LCD Refresh Left to Right (When MADCTL B2='0')								
				1	LCD Refresh Right to Left (When MADCTL B2='1')								
	D24	Not used		0	---								
	D23	Not used		0	---								
	D22	Interface color pixel format definition		011	12-bit/pixel								
	D21			101	16-bit/pixel								
	D20			110	18-bit/pixel								
	D19	Idle mode ON/OFF		0	Idle Mode OFF								
				1	Idle Mode ON								
	D18	Partial mode ON/OFF		0	Partial Mode OFF								
				1	Partial Mode ON.								
	D17	Sleep IN/OUT		0	Sleep IN Mode								
				1	Sleep OUT Mode.								
	D16	Display normal mode ON/OFF		0	Display Normal Mode OFF.								
				1	Display Normal Mode ON.								
	D15	Vertical scrolling status		0	Vertical Scroll OFF								
				1	Vertical Scroll ON								
	D14	Not used		0	---								
	D13	Inversion status		0	Inversion OFF								
				1	Inversion ON								
	D12	All pixel ON		0	Not defined								
	D11	All pixel OFF		0	Not defined								
	D10	Display ON/OFF		0	Display is OFF								
				1	Display is ON								
	D9	Tearing effect line ON/OFF		0	Tearing Effect Line OFF								
				1	Tearing Effect ON								
	D[8:6]	Gamma curve selection		000	GC0								
				001	GC1								
				010	GC2								
				011	GC3								
				other	Not defined								

		D5	Tearing effect line mode	0	Mode 1, V-Blanking only												
				1	Mode 2, both H-Blanking and V-Blanking.												
		D4	Not used	0	---												
		D3	Not used	0	---												
		D2	Not used	0	---												
		D1	Not used	0	---												
		D0	Not used	0	---												
X = Don't care																	
Restriction																	
Register Availability		<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>				Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																
Normal Mode On, Idle Mode Off, Sleep Out	Yes																
Normal Mode On, Idle Mode On, Sleep Out	Yes																
Partial Mode On, Idle Mode Off, Sleep Out	Yes																
Partial Mode On, Idle Mode On, Sleep Out	Yes																
Sleep In	Yes																
Default		<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>32'h00610000h</td></tr><tr><td>SW Reset</td><td>32'h00610000h</td></tr><tr><td>HW Reset</td><td>32'h00610000h</td></tr></table>				Status	Default Value	Power On Sequence	32'h00610000h	SW Reset	32'h00610000h	HW Reset	32'h00610000h				
Status	Default Value																
Power On Sequence	32'h00610000h																
SW Reset	32'h00610000h																
HW Reset	32'h00610000h																
Flow Chart		<div><div><div>RDDST(09h)</div><div></div></div><div><div></div><div>Host</div><div></div></div><div><div></div><div>Driver</div><div></div></div><div><div>1st Parameter: Dummy Read</div><div>2nd Parameter: Send D[31:25] display status</div><div>3rd Parameter: Send D[19:16] display status</div><div>4th Parameter: Send D[10:8] display status</div><div>5th Parameter: Send D[7:5] display status</div></div></div> <div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div>															

8.2.6. Read Display Power Mode (0Ah)

0Ah	RDDPM (Read Display Power Mode)																																							
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX																											
Command	0	1	↑	XXXXXXXX	0	0	0	0	1	0	1	0	0Ah																											
1 st Parameter	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX																											
2 nd Parameter	1	↑	1	XXXXXXXX	D[7:2]						0	0	XX																											
Description	This command indicates the current status of the display as described in the table below:																																							
	<table><tr><th>Bit</th><th>Description</th><th>Comment</th></tr><tr><td>D7</td><td>Booster Voltage Status</td><td></td></tr><tr><td>D6</td><td>Idle Mode On/Off</td><td></td></tr><tr><td>D5</td><td>Partial Mode On/Off</td><td></td></tr><tr><td>D4</td><td>Sleep In/Out</td><td></td></tr><tr><td>D3</td><td>Display Normal Mode On/Off</td><td></td></tr><tr><td>D2</td><td>Display On/Off</td><td></td></tr><tr><td>D1</td><td>Not Defined</td><td>Set to '0'</td></tr><tr><td>D0</td><td>Not Defined</td><td>Set to '0'</td></tr></table>													Bit	Description	Comment	D7	Booster Voltage Status		D6	Idle Mode On/Off		D5	Partial Mode On/Off		D4	Sleep In/Out		D3	Display Normal Mode On/Off		D2	Display On/Off		D1	Not Defined	Set to '0'	D0	Not Defined	Set to '0'
	Bit	Description	Comment																																					
	D7	Booster Voltage Status																																						
	D6	Idle Mode On/Off																																						
	D5	Partial Mode On/Off																																						
	D4	Sleep In/Out																																						
	D3	Display Normal Mode On/Off																																						
	D2	Display On/Off																																						
	D1	Not Defined	Set to '0'																																					
	D0	Not Defined	Set to '0'																																					
	Bit D7 – Booster Voltage Status																																							
	'0' = Booster Off or has a fault.																																							
	'1' = Booster On and working OK.																																							
	Bit D6 - Idle Mode On/Off																																							
	'0' = Idle Mode Off.																																							
	'1' = Idle Mode On.																																							
	Bit D5 – Partial Mode On/Off																																							
	'0' = Partial Mode Off.																																							
	'1' = Partial Mode On.																																							
	Bit D4 – Sleep In/Out																																							
	'0' = Sleep In Mode.																																							
	'1' = Sleep Out Mode.																																							
	Bit D3 – Display Normal Mode On/Off																																							
	'0' = Display Normal Mode Off.																																							
'1' = Display Normal Mode On.																																								
Bit D2 – Display On/Off																																								
'0' = Display is Off.																																								
'1' = Display is On.																																								
Bit D1 – Not Defined																																								
'This bit is not applicable for this project, so it is set to '0'																																								
Bit D0 – Not Defined																																								
'This bit is not applicable for this project, so it is set to '0'																																								
X = Don't care																																								

Restriction	<p>ILI9486L is sending 2nd parameter value on the data lines if the MCU wants to read more than one parameter (= more than 2 RDX cycle) on parallel MCU interface.</p> <p>Only 2nd parameter is sent on DSI (The 1st parameter is not sent).</p>												
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default	<table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>08_{HEX}</td></tr> <tr> <td>SW Reset</td><td>08_{HEX}</td></tr> <tr> <td>HW Reset</td><td>08_{HEX}</td></tr> </tbody> </table>	Status	Default Value	Power On Sequence	08 _{HEX}	SW Reset	08 _{HEX}	HW Reset	08 _{HEX}				
Status	Default Value												
Power On Sequence	08 _{HEX}												
SW Reset	08 _{HEX}												
HW Reset	08 _{HEX}												
Flow Chart	<pre> graph TD subgraph Host RDDPM[RDDPM 0Ah] end subgraph ILI9486 DummyRead[/Dummy Read/] SendParam[/Send 2nd Parameter/] end RDDPM --> DummyRead DummyRead --> SendParam </pre> <p>Legend</p> <ul style="list-style-type: none"> Command (trapezoid) Parameter (parallelogram) Display (rounded rectangle) Action (pentagon) Mode (oval) Sequential transfer (oval with arrow) 												

8.2.7. Read Display MADCTL (0Bh)

0Bh	RDDMADCTL (Read Display MADCTL)																																							
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX																											
Command	0	1	↑	XXXXXXXX	0	0	0	0	1	0	1	1	0Bh																											
1 st Parameter	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX																											
2 nd Parameter	1	↑	1	XXXXXXXX	D[7:2]						0	0	XX																											
Description	This command indicates the current status of the display as described in the table below:																																							
	<table><tr><th>Bit</th><th>Description</th><th>Comment</th></tr><tr><td>D7</td><td>Page Address Order</td><td></td></tr><tr><td>D6</td><td>Column Address Order</td><td></td></tr><tr><td>D5</td><td>Page/Column Order</td><td></td></tr><tr><td>D4</td><td>Line Address Order</td><td></td></tr><tr><td>D3</td><td>RGB/BGR Order</td><td></td></tr><tr><td>D2</td><td>Display Data Latch Data Order</td><td></td></tr><tr><td>D1</td><td>Reserved</td><td>Set to '0'</td></tr><tr><td>D0</td><td>Reserved</td><td>Set to '0'</td></tr></table>													Bit	Description	Comment	D7	Page Address Order		D6	Column Address Order		D5	Page/Column Order		D4	Line Address Order		D3	RGB/BGR Order		D2	Display Data Latch Data Order		D1	Reserved	Set to '0'	D0	Reserved	Set to '0'
	Bit	Description	Comment																																					
	D7	Page Address Order																																						
	D6	Column Address Order																																						
	D5	Page/Column Order																																						
	D4	Line Address Order																																						
	D3	RGB/BGR Order																																						
	D2	Display Data Latch Data Order																																						
	D1	Reserved	Set to '0'																																					
D0	Reserved	Set to '0'																																						
◆ Bit D7 – Page Address Order '0' = Top to Bottom '1' = Bottom to Top																																								
◆ Bit D6 – Column Address Order '0' = Left to Right '1' = Right to Left																																								
◆ Bit D5 - Page/Column Order '0' = Normal Mode '1' = Reverse Mode Note: For Bits D7 to D5, also refer to Section 9.3 MCU to memory write/read direction.																																								
◆ Bit D4 – Line Address Order '0' = LCD Refresh Top to Bottom '1' = LCD Refresh Bottom to Top																																								
◆ Bit D3 – RGB/BGR Order '0' = RGB '1' = BGR																																								
◆ Bit D2 – Display Data Latch Data Order '0' = LCD Refresh Left to Right '1' = LCD Refresh Right to Left																																								
Restriction	ILI9486L is sending 2nd parameter value on the data lines if the MCU wants to read more than one parameter (= more than 2 RDX cycle) on parallel MCU interface. Only 2nd parameter is sent on DSI (The 1st parameter is not sent).																																							
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes															
Status	Availability																																							
Normal Mode On, Idle Mode Off, Sleep Out	Yes																																							
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Partial Mode On, Idle Mode Off, Sleep Out	Yes																																							
Partial Mode On, Idle Mode On, Sleep Out	Yes																																							
Sleep In	Yes																																							

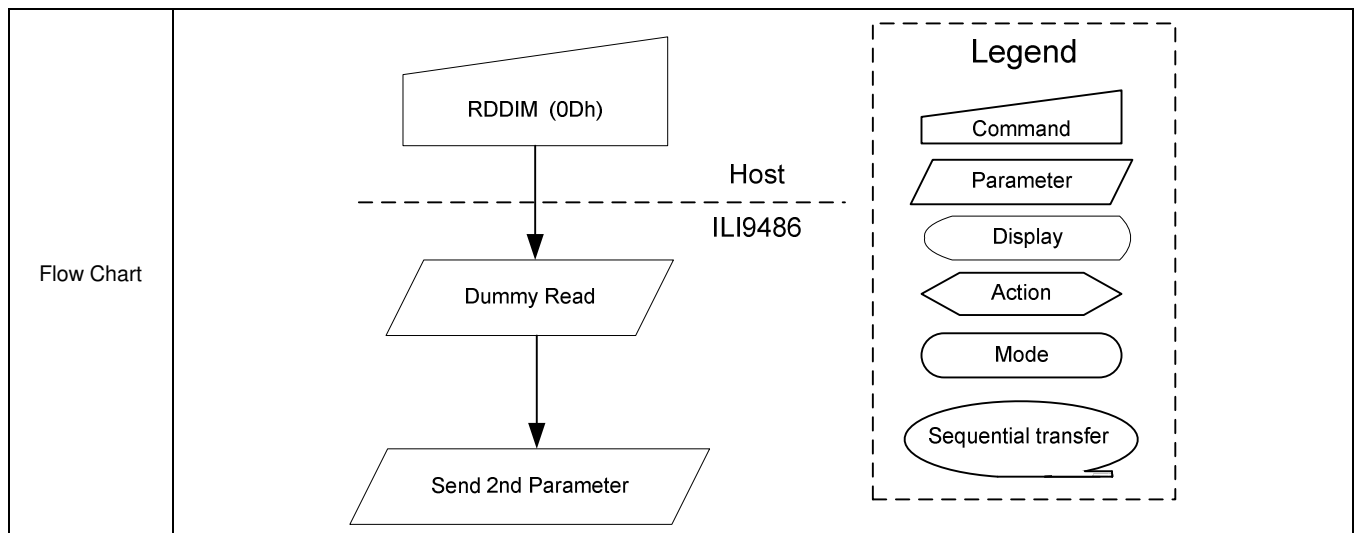
Default	<table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>00_{HEX}</td></tr> <tr> <td>SW Reset</td><td>No Change</td></tr> <tr> <td>HW Reset</td><td>00_{HEX}</td></tr> </tbody> </table>	Status	Default Value	Power On Sequence	00 _{HEX}	SW Reset	No Change	HW Reset	00 _{HEX}
Status	Default Value								
Power On Sequence	00 _{HEX}								
SW Reset	No Change								
HW Reset	00 _{HEX}								
Flow Chart	<pre> graph TD Host[Host] -- "RDDMADCTL (0Bh)" --> DummyRead[/Dummy Read/] DummyRead --> SendParam[/Send 2nd Parameter/] </pre> <p>Host ILI9486</p> <div style="border: 1px dashed black; padding: 5px; margin-top: 10px;"> <p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer </div>								

8.2.8. Read Display Pixel Format (0Ch)

0Ch	RDDCOLMOD (Read Display COLMOD)																																																																																								
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																																												
Command	0	1	↑	XXXXXXXX	0	0	0	0	1	1	0	0	0Ch																																																																												
1 st Parameter	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX																																																																												
2 nd Parameter	1	↑	1	XXXXXXXX	DPI[3:0]				0	DBI[2:0]			XX																																																																												
Description	This command indicates the current status of the display as described in the table below:																																																																																								
	<table><tr><th colspan="4">DPI[3:0]</th><th>RGB Interface Format</th></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>Reserved</td></tr><tr><td>0</td><td>0</td><td>0</td><td>1</td><td>Reserved</td></tr><tr><td>0</td><td>0</td><td>1</td><td>0</td><td>Reserved</td></tr><tr><td>0</td><td>0</td><td>1</td><td>1</td><td>Reserved</td></tr><tr><td>0</td><td>1</td><td>0</td><td>0</td><td>Reserved</td></tr><tr><td>0</td><td>1</td><td>0</td><td>1</td><td>16 bits / pixel</td></tr><tr><td>0</td><td>1</td><td>1</td><td>0</td><td>18 bits / pixel</td></tr><tr><td>0</td><td>1</td><td>1</td><td>1</td><td>Reserved</td></tr></table>				DPI[3:0]				RGB Interface Format	0	0	0	0	Reserved	0	0	0	1	Reserved	0	0	1	0	Reserved	0	0	1	1	Reserved	0	1	0	0	Reserved	0	1	0	1	16 bits / pixel	0	1	1	0	18 bits / pixel	0	1	1	1	Reserved	<table><tr><th colspan="3">DBI[2:0]</th><th>CPU Interface Format</th></tr><tr><td>0</td><td>0</td><td>0</td><td>Reserved</td></tr><tr><td>0</td><td>0</td><td>1</td><td>Reserved</td></tr><tr><td>0</td><td>1</td><td>0</td><td>Reserved</td></tr><tr><td>0</td><td>1</td><td>1</td><td>Reserved</td></tr><tr><td>1</td><td>0</td><td>0</td><td>Reserved</td></tr><tr><td>1</td><td>0</td><td>1</td><td>16 bits / pixel</td></tr><tr><td>1</td><td>1</td><td>0</td><td>18 bits / pixel</td></tr><tr><td>1</td><td>1</td><td>1</td><td>Reserved</td></tr></table>				DBI[2:0]			CPU Interface Format	0	0	0	Reserved	0	0	1	Reserved	0	1	0	Reserved	0	1	1	Reserved	1	0	0	Reserved	1	0	1	16 bits / pixel	1	1	0	18 bits / pixel	1	1	1	Reserved
	DPI[3:0]				RGB Interface Format																																																																																				
	0	0	0	0	Reserved																																																																																				
	0	0	0	1	Reserved																																																																																				
	0	0	1	0	Reserved																																																																																				
	0	0	1	1	Reserved																																																																																				
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DBI[2:0]			CPU Interface Format																																																																																						
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Restriction	ILI9486L is sending 2nd parameter value on the data lines if the MCU wants to read more than one parameter (= more than 2 RDX cycle) on parallel MCU interface. Only 2nd parameter is sent on DSI (The 1st parameter is not sent).																																																																																								
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes																																																																
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Sleep In	Yes																																																																																								
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>06_{HEX}</td></tr><tr><td>SW Reset</td><td>No Change</td></tr><tr><td>HW Reset</td><td>06_{HEX}</td></tr></table>													Status	Default Value	Power On Sequence	06 _{HEX}	SW Reset	No Change	HW Reset	06 _{HEX}																																																																				
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Power On Sequence	06 _{HEX}																																																																																								
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Flow Chart	<div><div><div>RDDCOLMOD (0Ch)</div><div>Dummy Read</div><div>Send 2nd Parameter</div></div><div>Host ILI9486</div></div> <div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div>																																																																																								

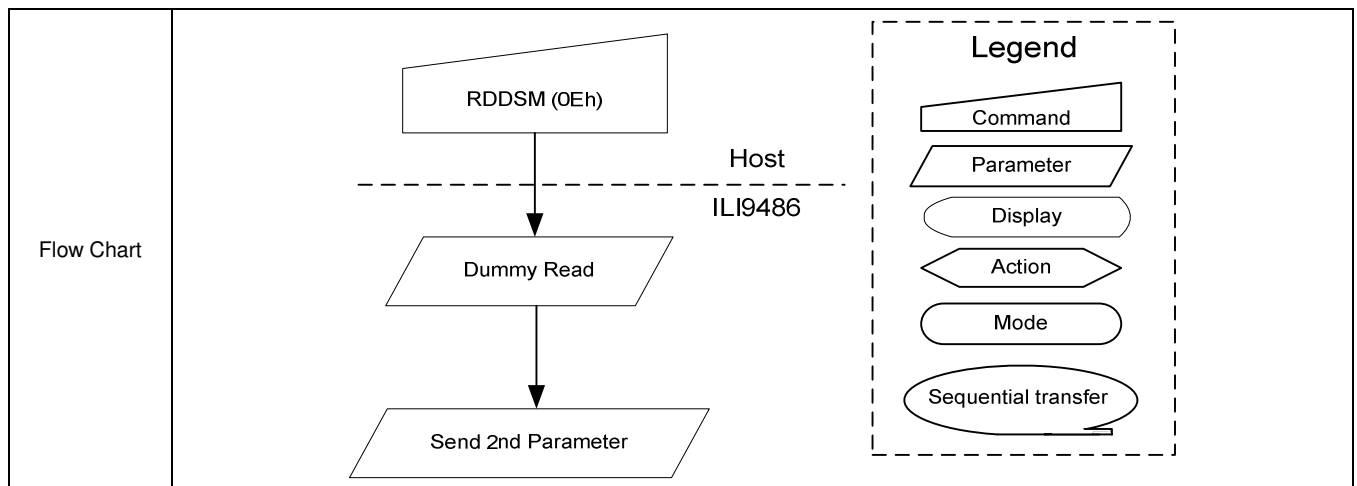
8.2.9. Read Display Image Mode (0Dh)

0Dh	RDDIM (Read Display Image Mode)																														
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX																		
Command	0	1	↑	XXXXXXXX	0	0	0	0	1	1	0	1	0Dh																		
1 st Parameter	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX																		
2 nd Parameter	1	↑	1	XXXXXXXX	D[7:0]								XX																		
Description	ILI9486L returns the Display Image Mode status.																														
	<table><tr><th>Bit</th><th>Description</th></tr><tr><td>D7</td><td>Vertical Scrolling Status</td></tr><tr><td>D6</td><td>Reserved</td></tr><tr><td>D5</td><td>Inversion On/Off</td></tr><tr><td>D4</td><td>Reserved</td></tr><tr><td>D3</td><td>Reserved</td></tr><tr><td>D2</td><td>Gamma Curve Selection</td></tr><tr><td>D1</td><td>Gamma Curve Selection</td></tr><tr><td>D0</td><td>Gamma Curve Selection</td></tr></table>													Bit	Description	D7	Vertical Scrolling Status	D6	Reserved	D5	Inversion On/Off	D4	Reserved	D3	Reserved	D2	Gamma Curve Selection	D1	Gamma Curve Selection	D0	Gamma Curve Selection
	Bit	Description																													
	D7	Vertical Scrolling Status																													
	D6	Reserved																													
	D5	Inversion On/Off																													
	D4	Reserved																													
	D3	Reserved																													
	D2	Gamma Curve Selection																													
	D1	Gamma Curve Selection																													
D0	Gamma Curve Selection																														
This command indicates the current status of the display as described in the table below:																															
◆ Bit D7 – Vertical Scrolling On/Off ‘0’ = Vertical Scrolling is Off. ‘1’ = Vertical Scrolling is On.																															
◆ Bit D6 – Reserved																															
◆ Bit D5 – Inversion On/Off ‘0’ = Inversion is Off. ‘1’ = Inversion is On.																															
◆ Bit D4 – Reserved																															
◆ Bit D3 – Reserved																															
◆ Bits D2, D1, D0 – Gamma Curve Selection These bits are not applicable for this project, so they are set to ‘000’, only support Gamma 2.2.																															
Restriction	ILI9486L is sending 2nd parameter value on the data lines if the MCU wants to read more than one parameter (= more than 2 RDX cycle) on parallel MCU interface. Only 2nd parameter is sent on DSI (The 1st parameter is not sent).																														
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes						
Status	Availability																														
Normal Mode On, Idle Mode Off, Sleep Out	Yes																														
Normal Mode On, Idle Mode On, Sleep Out	Yes																														
Partial Mode On, Idle Mode Off, Sleep Out	Yes																														
Partial Mode On, Idle Mode On, Sleep Out	Yes																														
Sleep In	Yes																														
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>00_{HEX}</td></tr><tr><td>SW Reset</td><td>00_{HEX}</td></tr><tr><td>HW Reset</td><td>00_{HEX}</td></tr></table>													Status	Default Value	Power On Sequence	00 _{HEX}	SW Reset	00 _{HEX}	HW Reset	00 _{HEX}										
Status	Default Value																														
Power On Sequence	00 _{HEX}																														
SW Reset	00 _{HEX}																														
HW Reset	00 _{HEX}																														



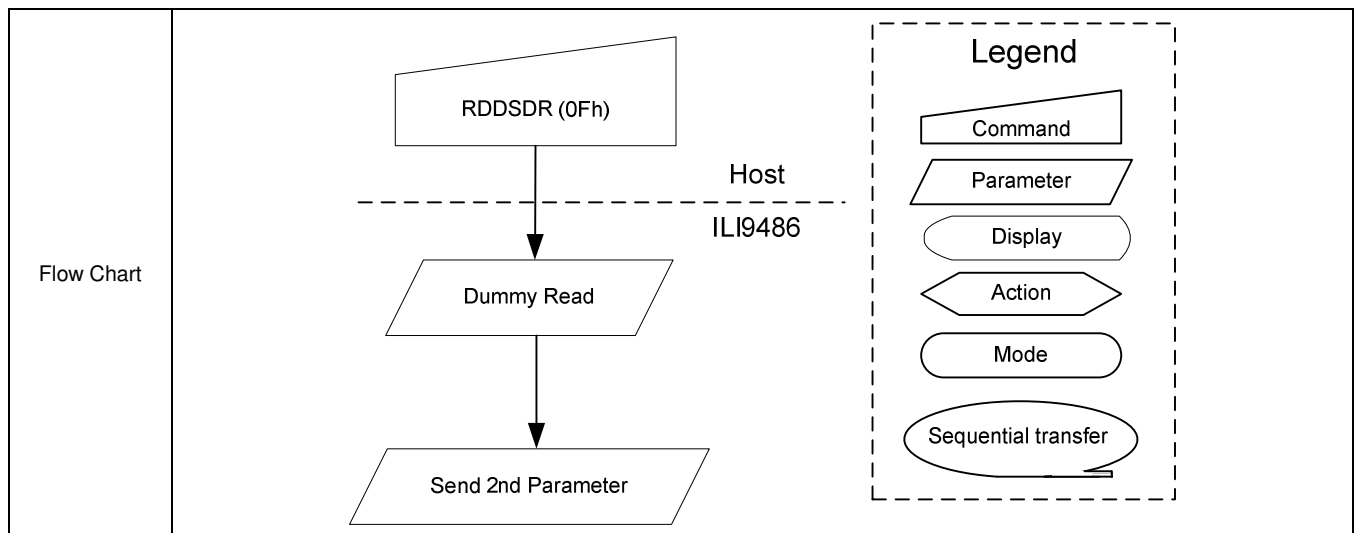
8.2.10. Read Display Signal Mode (0Eh)

0Eh	RDDSM (Read Display Signal Mode)																								
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XXXXXXXX	0	0	0	0	1	1	1	0	0Eh												
1 st Parameter	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX												
2 nd Parameter	1	↑	1	XXXXXXXX	D7	D6	D5	D4	D3	D2	D1	D0	XX												
Description	This command indicates the current status of the display as described in the table below:																								
	Bit		Value		Function																				
	D7	0		Tearing Effect Line OFF																					
		1		Tearing Effect Line ON																					
	D6	0		Tearing Effect Line Mode 1																					
		1		Tearing Effect Line Mode 2																					
	D5	0		Horizontal Sync (RGB interface) OFF																					
		1		Horizontal Sync (RGB interface) ON																					
	D4	0		Vertical Sync (RGB interface) OFF																					
		1		Vertical Sync (RGB interface) ON																					
	D3	0		Pixel Clock (DOTCLK, RGB interface) OFF																					
		1		Pixel Clock (DOTCLK, RGB interface) ON																					
	D2	0		Data Enable (DE, RGB interface) OFF																					
		1		Data Enable (DE, RGB interface) ON																					
	D1	0		Reserved																					
		1		Reserved																					
	D0	0		No Error on DSI																					
		1		Error on DSI																					
Restriction	ILI9486L is sending 2nd parameter value on the data lines if the MCU wants to read more than one parameter (= more than 2 RDX cycle) on parallel MCU interface. Only 2nd parameter is sent on DSI (The 1st parameter is not sent).																								
Register Availability	<table><thead><tr><th>Status</th><th>Availability</th></tr></thead><tbody><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></tbody></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><thead><tr><th>Status</th><th>Default Value</th></tr></thead><tbody><tr><td>Power On Sequence</td><td>00_{HEX}</td></tr><tr><td>SW Reset</td><td>00_{HEX}</td></tr><tr><td>HW Reset</td><td>00_{HEX}</td></tr></tbody></table>													Status	Default Value	Power On Sequence	00 _{HEX}	SW Reset	00 _{HEX}	HW Reset	00 _{HEX}				
Status	Default Value																								
Power On Sequence	00 _{HEX}																								
SW Reset	00 _{HEX}																								
HW Reset	00 _{HEX}																								



8.2.11. Read Display Self-Diagnostic Result (0Fh)

0Fh	RDDSDR (Read Display Self-Diagnostic Result)												
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	0	0	0	0	1	1	1	1	0Fh
1 st Parameter	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX
2 nd Parameter	1	↑	1	XXXXXXXX	D7	D6	0	0	0	0	0	D0	XX
Description	This command indicates the status of the display self-diagnostic results after Sleep Out -command as described in the table below:												
	Bit	Description				Action							
	D7	Register Loading Detection				Invert the D7 bit if register values loading work properly.							
	D6	Functionality Detection				Invert the D6 bit if the display is functionality							
	D5	Not Used				'0'							
	D4	Not Used				'0'							
	D3	Not Used				'0'							
	D2	Not Used				'0'							
	D1	Not Used				'0'							
D0	Checksums Comparison				'0' = Checksums are same '1' = Checksums are not same								
Restriction	It will be necessary to wait 300ms after there is the last write access on User area registers before there can read Bit D0 value.												
	ILI9486L is sending 2nd parameter value on the data lines if the MCU wants to read more than one parameter (= more than 2 RDX cycle) on parallel MCU interface.												
	Only 2nd parameter is sent on DSI (The 1st parameter is not sent).												
Register Availability													
	Status								Availability				
	Normal Mode On, Idle Mode Off, Sleep Out								Yes				
	Normal Mode On, Idle Mode On, Sleep Out								Yes				
	Partial Mode On, Idle Mode Off, Sleep Out								Yes				
	Partial Mode On, Idle Mode On, Sleep Out								Yes				
Sleep In								Yes					
Default													
	Status					Default Value							
	Power On Sequence					00 _{HEX}							
	SW Reset					00 _{HEX}							
HW Reset					00 _{HEX}								



8.2.12. Sleep IN (10h)

10h	SLPIN (Sleep IN)																								
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XXXXXXXX	0	0	0	1	0	0	0	0	10h												
Parameter	No parameter																								
Description	<p>This command causes ILI9486L to enter the minimum power consumption mode.</p> <p>In this mode e.g. the DC/DC converter is stopped, Internal oscillator is stopped, and panel scanning is stopped.</p> <div><div>Out</div><div>Blank</div><div>STOP</div></div> <p>MCU interface and memory are still working and the memory keeps its contents.</p> <p>Dimming function does not work when there is changing mode from Sleep OUT to Sleep IN.</p> <p>X = Don't care</p>																								
Restriction	<p>This command has no effect when module is already in sleep in mode. Sleep In Mode can only be left by the Sleep Out Command (11h). It will be necessary to wait 5msec before sending next command; this is to allow time for the supply voltages and clock circuits to stabilize. It will be necessary to wait 120msec after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent.</p>																								
Register Availability	<table><thead><tr><th>Status</th><th>Availability</th></tr></thead><tbody><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></tbody></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><thead><tr><th>Status</th><th>Default Value</th></tr></thead><tbody><tr><td>Power On Sequence</td><td>Sleep IN Mode</td></tr><tr><td>SW Reset</td><td>Sleep IN Mode</td></tr><tr><td>HW Reset</td><td>Sleep IN Mode</td></tr></tbody></table>													Status	Default Value	Power On Sequence	Sleep IN Mode	SW Reset	Sleep IN Mode	HW Reset	Sleep IN Mode				
Status	Default Value																								
Power On Sequence	Sleep IN Mode																								
SW Reset	Sleep IN Mode																								
HW Reset	Sleep IN Mode																								
Flow Chart	<div><div><div>Any Mode</div><div>SLPIN (10h)</div><div>Blank Display Device</div><div>Power OFF Device</div></div><div><div>Stop Power Supply</div><div>Stop Internal Oscillator</div><div>Sleep Mode ON</div></div><div><div>Legend</div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div>																								

8.2.13. Sleep OUT (11h)

11h	SLPOUT (Sleep OUT)																								
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XXXXXXXX	0	0	0	1	0	0	0	1	11h												
Parameter	No parameter																								
Description	<p>This command turns off sleep mode.</p> <p>In this mode e.g. the DC/DC converter is enabled, Internal oscillator is started, and panel scanning is started.</p> <div><div>OUT</div><div>STOP</div><div>Blank</div><div>Memory Contents</div></div> <p>X = Don't care</p>																								
Restriction	<p>Sleep Out Mode can only be left by the Sleep In Command (10h). It will be necessary to wait 5msec before sending next command; this is to allow time for the supply voltages and clock circuits to stabilize.</p> <p>ILI9486L loads all display supplier's factory default values to the registers during this 5msec and there cannot be any abnormal visual effect on the display image if factory default and register values are same when this load is done and when ILI9486L is already Sleep Out –mode.</p> <p>ILI9486L is doing self-diagnostic functions during this 5msec. It will be necessary to wait 120msec after sending Sleep In command (when in Sleep Out mode) before Sleep Out command can be sent.</p>																								
Register Availability	<table><thead><tr><th>Status</th><th>Availability</th></tr></thead><tbody><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></tbody></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><thead><tr><th>Status</th><th>Default Value</th></tr></thead><tbody><tr><td>Power On Sequence</td><td>Sleep IN Mode</td></tr><tr><td>SW Reset</td><td>Sleep IN Mode</td></tr><tr><td>HW Reset</td><td>Sleep IN Mode</td></tr></tbody></table>													Status	Default Value	Power On Sequence	Sleep IN Mode	SW Reset	Sleep IN Mode	HW Reset	Sleep IN Mode				
Status	Default Value																								
Power On Sequence	Sleep IN Mode																								
SW Reset	Sleep IN Mode																								
HW Reset	Sleep IN Mode																								
Flow Chart	<div><div><div>Sleep In Mode</div><div>SLPOUT (11h)</div><div>Start Internal Oscillator</div><div>Start Power Supply</div></div><div><div>Power ON Display Device</div><div>Blank Display Device</div><div>Sleep Mode OFF</div></div></div> <div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div>																								

8.2.14. Partial Mode ON (12h)

12h	PTLON (Partial Mode ON)																								
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XXXXXXXX	0	0	0	1	0	0	1	0	12h												
Parameter	No parameter																								
Description	This command turns on partial mode The partial mode window is described by the Partial Area command (30H). To leave Partial mode, the Normal Display Mode On command (13H) should be written.																								
Restriction	This command has no effect when Partial Display Mode is already active.																								
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Sleep IN Mode</td></tr><tr><td>SW Reset</td><td>Sleep IN Mode</td></tr><tr><td>HW Reset</td><td>Sleep IN Mode</td></tr></table>													Status	Default Value	Power On Sequence	Sleep IN Mode	SW Reset	Sleep IN Mode	HW Reset	Sleep IN Mode				
Status	Default Value																								
Power On Sequence	Sleep IN Mode																								
SW Reset	Sleep IN Mode																								
HW Reset	Sleep IN Mode																								
Flow Chart	See Partial Area (30h)																								

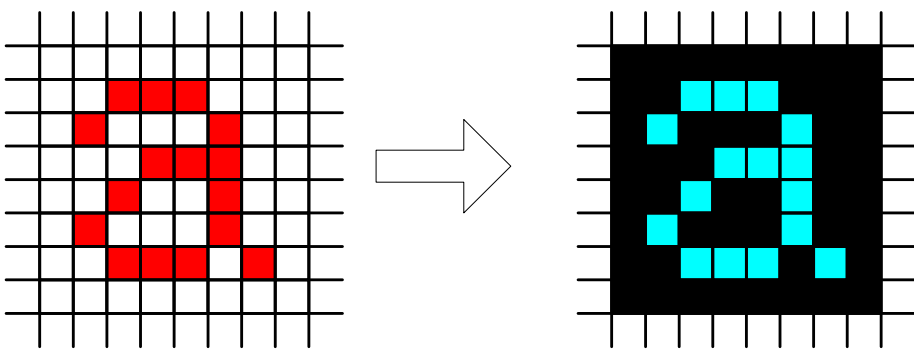
8.2.15. Normal Display Mode ON (13h)

13h	NORON (Normal Display Mode ON)																								
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XXXXXXXX	0	0	0	1	0	0	1	1	13h												
Parameter	No parameter																								
Description	This command returns the display to normal mode. Normal display mode on means Partial mode off and Scroll mode off. X = Don't care																								
Restriction	This command has no effect when Normal Display mode is active.																								
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Normal Display Mode On</td></tr><tr><td>SW Reset</td><td>Normal Display Mode On</td></tr><tr><td>HW Reset</td><td>Normal Display Mode On</td></tr></table>													Status	Default Value	Power On Sequence	Normal Display Mode On	SW Reset	Normal Display Mode On	HW Reset	Normal Display Mode On				
Status	Default Value																								
Power On Sequence	Normal Display Mode On																								
SW Reset	Normal Display Mode On																								
HW Reset	Normal Display Mode On																								
Flow Chart	See Partial Area Descriptions for details of when to use this command.																								

8.2.16. Display Inversion OFF (20h)

20h	INVOFF (Display Inversion OFF)																								
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XXXXXXXX	0	0	1	0	0	0	0	0	20h												
Parameter	No parameter																								
Description	<p>This command is used to recover from display inversion mode. Output from the Frame Memory is enabled.</p> <p>This command makes no change of the content of frame memory.</p> <p>This command doesn't change any other status.</p> <div><div>Memory</div><div></div><div>→</div><div><div>Display Panel</div><div></div></div><p>X = Don't care</p></div>																								
Restriction	This command has no effect when ILI9486L is already in Inversion off mode.																								
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Display Inversion OFF</td></tr><tr><td>SW Reset</td><td>Display Inversion OFF</td></tr><tr><td>HW Reset</td><td>Display Inversion OFF</td></tr></table>													Status	Default Value	Power On Sequence	Display Inversion OFF	SW Reset	Display Inversion OFF	HW Reset	Display Inversion OFF				
Status	Default Value																								
Power On Sequence	Display Inversion OFF																								
SW Reset	Display Inversion OFF																								
HW Reset	Display Inversion OFF																								
Flow Chart	<div><div><div>Invert Mode ON</div><div>↓</div><div>INVOFF (20h)</div><div>↓</div><div>Invert Mode OFF</div></div><div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div></div>																								

8.2.17. Display Inversion ON (21h)

21h	INVON (Display Inversion ON)																								
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XXXXXXXX	0	0	1	0	0	0	0	1	21h												
Parameter	No parameter																								
Description	<p>This command is used to enter into display inversion mode.</p> <p>This command makes no change of the content of frame memory. Every bit is inverted from the frame memory to the display.</p> <p>This command doesn't change any other status.</p> <p>To exit Display inversion mode, the Display inversion OFF command (20h) should be written.</p> <div></div> <p>X = Don't care</p>																								
Restriction	This command has no effect when ILI9486L is already in Inversion on mode.																								
Register Availability	<table><thead><tr><th>Status</th><th>Availability</th></tr></thead><tbody><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></tbody></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><thead><tr><th>Status</th><th>Default Value</th></tr></thead><tbody><tr><td>Power On Sequence</td><td>Display Inversion OFF</td></tr><tr><td>SW Reset</td><td>Display Inversion OFF</td></tr><tr><td>HW Reset</td><td>Display Inversion OFF</td></tr></tbody></table>													Status	Default Value	Power On Sequence	Display Inversion OFF	SW Reset	Display Inversion OFF	HW Reset	Display Inversion OFF				
Status	Default Value																								
Power On Sequence	Display Inversion OFF																								
SW Reset	Display Inversion OFF																								
HW Reset	Display Inversion OFF																								
Flow Chart	<div><div><div>Invert Mode OFF</div><div>↓</div><div>INVON (21h)</div><div>↓</div><div>Invert Mode ON</div></div><div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div></div>																								

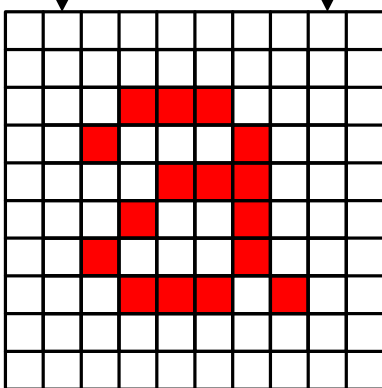
8.2.18. Display OFF (28h)

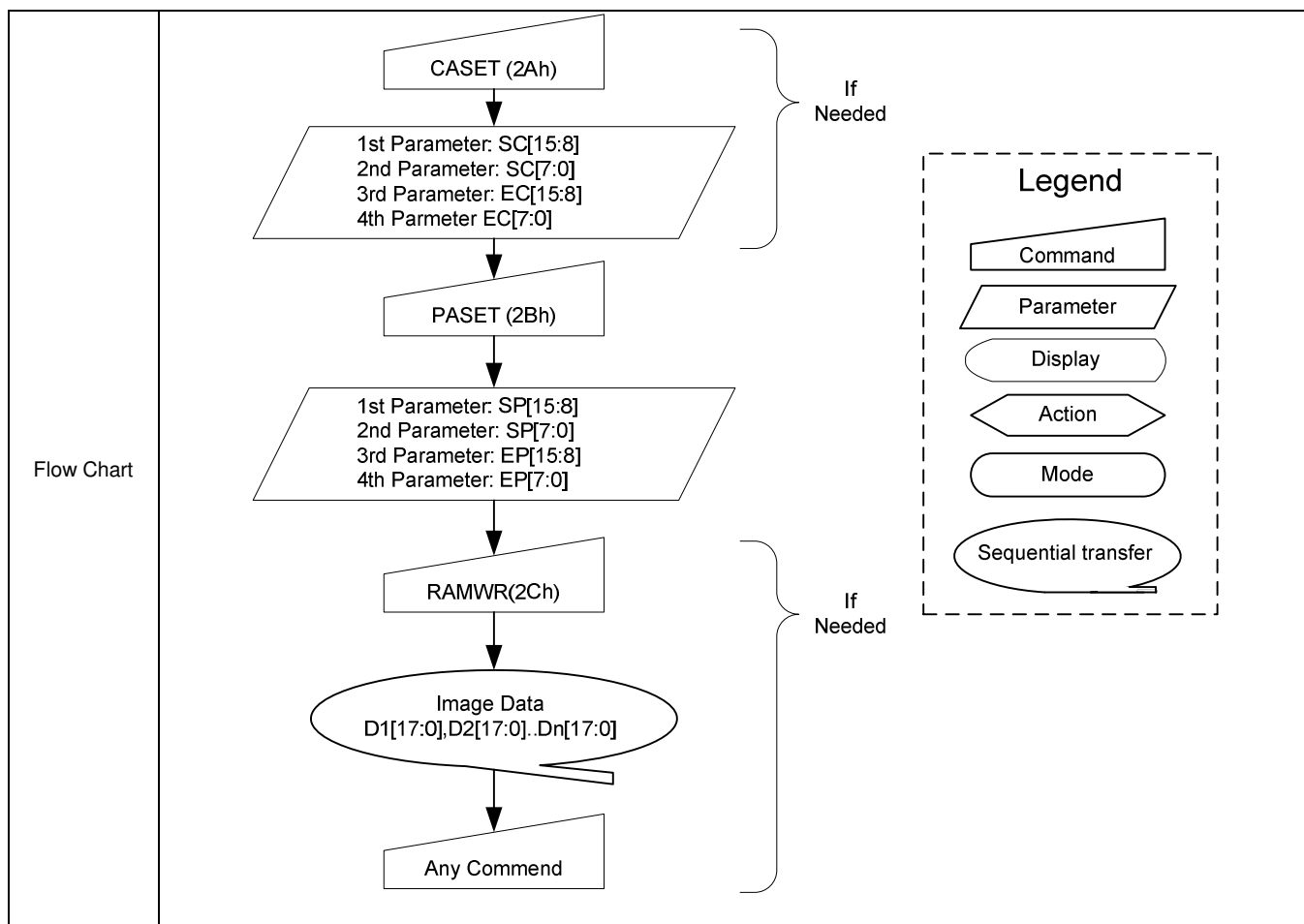
28h	DISOFF (Display OFF)																								
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XXXXXXXX	0	0	1	0	1	0	0	0	28h												
Parameter	No parameter																								
Description	<p>This command causes ILI9486L to stop displaying the image data on the display device. The frame memory contents remain unchanged. No status bits are changed.</p> <div><div><p>Memory</p><p>X = Don't care</p></div><div><p>Display Panel</p></div></div>																								
Restriction	This command has no effect when ILI9486L is already in Display off mode.																								
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Display OFF</td></tr><tr><td>SW Reset</td><td>Display OFF</td></tr><tr><td>HW Reset</td><td>Display OFF</td></tr></table>													Status	Default Value	Power On Sequence	Display OFF	SW Reset	Display OFF	HW Reset	Display OFF				
Status	Default Value																								
Power On Sequence	Display OFF																								
SW Reset	Display OFF																								
HW Reset	Display OFF																								
Flow Chart	<div><div><pre>graph TD; A([Display Panel ON]) --> B[/DISOFF (28h)/]; B --> C([Display Panel OFF]);</pre></div><div><p>Legend</p><ul style="list-style-type: none">CommandParameterDisplayActionModeSequential transfer</div></div>																								

8.2.19. Display ON (29h)

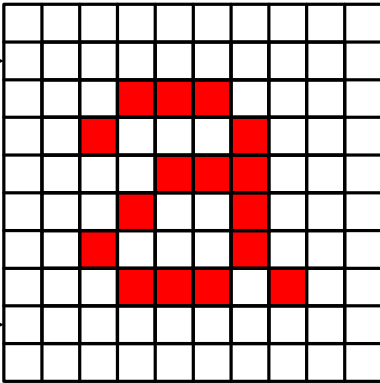
29h	DISON (Display ON)																								
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XXXXXXXX	0	0	1	0	1	0	0	1	29h												
Parameter	No parameter																								
Description	<p>This command causes ILI9486L to start displaying the image data on the display device. The frame memory contents remain unchanged. No status bits are changed.</p> <div><div><p>Memory</p></div><div></div><div><p>Display Panel</p></div></div> <p>X = Don't care</p>																								
Restriction	This command has no effect when ILI9486L is already in Display on mode.																								
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Display OFF</td></tr><tr><td>SW Reset</td><td>Display OFF</td></tr><tr><td>HW Reset</td><td>Display OFF</td></tr></table>													Status	Default Value	Power On Sequence	Display OFF	SW Reset	Display OFF	HW Reset	Display OFF				
Status	Default Value																								
Power On Sequence	Display OFF																								
SW Reset	Display OFF																								
HW Reset	Display OFF																								
Flow Chart	<div><div><p>Display OFF Mode</p><p>↓</p><p>DISON (29h)</p><p>↓</p><p>Display ON Mode</p></div><div><p>Legend</p><ul style="list-style-type: none">CommandParameterDisplayActionModeSequential transfer</div></div>																								

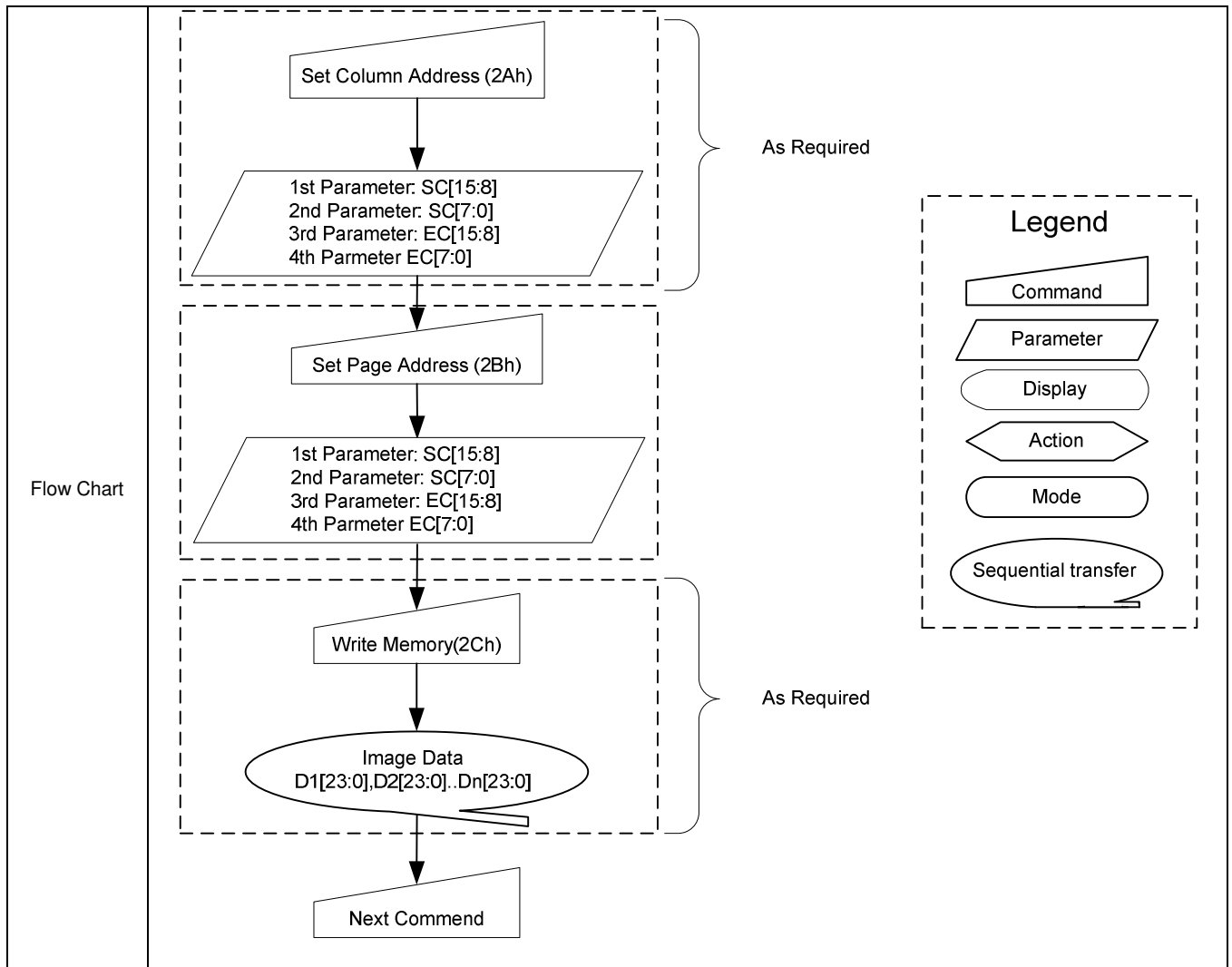
8.2.20. Column Address Set (2Ah)

2Ah	CASET (Column Address Set)																								
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XXXXXXXX	0	0	1	0	1	0	1	0	2Ah												
1 st Parameter	1	1	↑	XXXXXXXX	SC[15:8]								XX												
2 nd Parameter	1	1	↑	XXXXXXXX	SC[7:0]								XX												
3 rd Parameter	1	1	↑	XXXXXXXX	EC[15:8]								XX												
4 th Parameter	1	1	↑	XXXXXXXX	EC[7:0]								XX												
Description	<p>This command is used to define area of frame memory where MCU can access. This command makes no change on the other driver status. The values of SC[15:0] and EC[15:0] are referred when RAMWR command comes. Each value represents one column line in the Frame Memory.</p> <div><div>SC[15:0]</div><div>EC[15:0]</div></div>																								
Restriction	<p>SC[15:0] always must be equal to or less than EC[15:0].</p> <p>Note 1: When SC[15:0] or EC[15:0] is greater than 013Fh (When MADCTL's B5 = 0) or 01DFh (When MADCTL's B5 = 1), data of out of range will be ignored</p>																								
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><tr><th>Status</th><th colspan="2">Default Value</th></tr><tr><td>Power On Sequence</td><td>SC[15:0]=0000h</td><td>EC[15:0]=00EFh</td></tr><tr><td>SW Reset</td><td>SC[15:0]=0000h</td><td>If MADCTL's B5 = 0: EC[15:0]=013Fh If MADCTL's B5 = 1: EC[15:0]=01DFh</td></tr><tr><td>HW Reset</td><td>SC[15:0]=0000h</td><td>EC[15:0]=013Fh</td></tr></table>													Status	Default Value		Power On Sequence	SC[15:0]=0000h	EC[15:0]=00EFh	SW Reset	SC[15:0]=0000h	If MADCTL's B5 = 0: EC[15:0]=013Fh If MADCTL's B5 = 1: EC[15:0]=01DFh	HW Reset	SC[15:0]=0000h	EC[15:0]=013Fh
Status	Default Value																								
Power On Sequence	SC[15:0]=0000h	EC[15:0]=00EFh																							
SW Reset	SC[15:0]=0000h	If MADCTL's B5 = 0: EC[15:0]=013Fh If MADCTL's B5 = 1: EC[15:0]=01DFh																							
HW Reset	SC[15:0]=0000h	EC[15:0]=013Fh																							



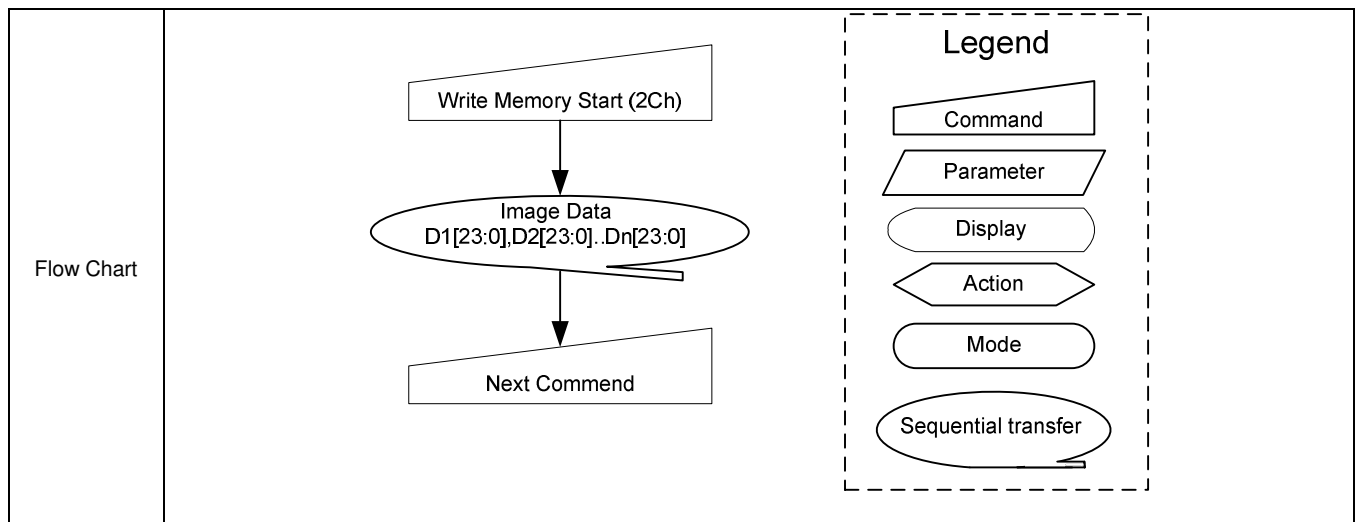
8.2.21. Page Address Set (2Bh)

2Bh	PASET (Page Address Set)																								
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XXXXXXXX	0	0	1	0	1	0	1	1	2Bh												
1 st Parameter	1	1	↑	XXXXXXXX	SP[15:8]								XX												
2 nd Parameter	1	1	↑	XXXXXXXX	SP[7:0]								XX												
3 rd Parameter	1	1	↑	XXXXXXXX	EP[15:8]								XX												
4 th Parameter	1	1	↑	XXXXXXXX	EP[7:0]								XX												
Description	<p>This command is used to define area of frame memory where MCU can access. This command makes no change on the other driver status. The values of SP[15:0] and EP[15:0] are referred when RAMWR command comes. Each value represents one Page line in the Frame Memory.</p> <div><div>SP[15:0] →</div><div>EP[15:0] →</div></div> <p>X = don't care</p>																								
Restriction	<p>SP[15:0] always must be equal to or less than EP[15:0]</p> <p>When SP[15:0] or EP[15:0] is greater than 01DFh (When MADCTL's B5 = 0) or 013Fh (When MADCTL's B5 = 1), data of out of range will be ignored.</p>																								
Register Availability	<table><thead><tr><th>Status</th><th>Availability</th></tr></thead><tbody><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></tbody></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><thead><tr><th>Status</th><th colspan="2">Default Value</th></tr></thead><tbody><tr><td>Power On Sequence</td><td>SP[15:0]=0000h</td><td>EP[15:0]=013Fh</td></tr><tr><td>SW Reset</td><td>SP[15:0]=0000h</td><td>If MADCTL's B5 = 0: EP[15:0]=01DFh If MADCTL's B5 = 1: EP[15:0]=013Fh</td></tr><tr><td>HW Reset</td><td>SP[15:0]=0000h</td><td>EP[15:0]=01EFh</td></tr></tbody></table>													Status	Default Value		Power On Sequence	SP[15:0]=0000h	EP[15:0]=013Fh	SW Reset	SP[15:0]=0000h	If MADCTL's B5 = 0: EP[15:0]=01DFh If MADCTL's B5 = 1: EP[15:0]=013Fh	HW Reset	SP[15:0]=0000h	EP[15:0]=01EFh
Status	Default Value																								
Power On Sequence	SP[15:0]=0000h	EP[15:0]=013Fh																							
SW Reset	SP[15:0]=0000h	If MADCTL's B5 = 0: EP[15:0]=01DFh If MADCTL's B5 = 1: EP[15:0]=013Fh																							
HW Reset	SP[15:0]=0000h	EP[15:0]=01EFh																							



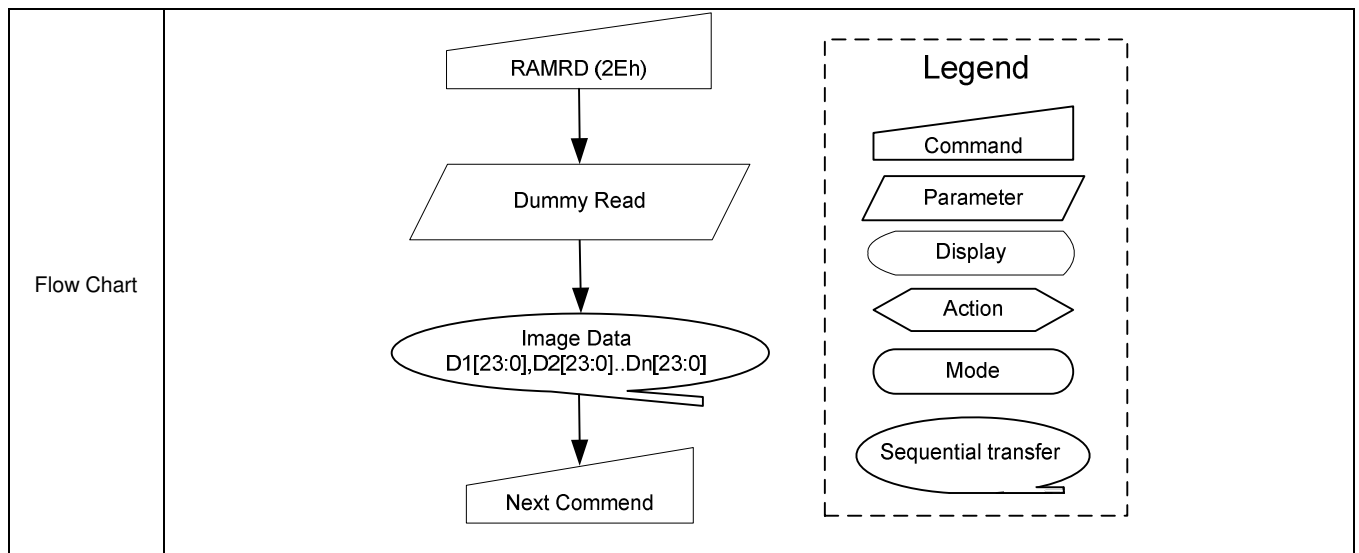
8.2.22. Memory Write (2Ch)

2Ch	RAMWR (Memory Write)																								
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XXXXXXXX	0	0	1	0	1	1	0	0	2Ch												
1 st Parameter	1	1	↑	D1[15:0]									XX												
:	1	1	↑	Dx[15:0]									XX												
N th Parameter	1	1	↑	Dn[15:0]									XX												
Description	This command transfers image data from the host processor to ILI9486L's frame memory starting at the pixel location specified by preceding Column Address Set (2Ah) and Page Address Set (2Bh) commands.																								
	If Memory Access Control (36h) B5 = 0:																								
	The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixel Data 1 is stored in frame memory at (SC, SP). The column register is then incremented and pixels are written to the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are written to the frame memory until the page register equals the End Page (EP) value or the host processor sends another command. If the number of pixels exceeds (EC – SC + 1) * (EP – SP + 1) the extra pixels are ignored.																								
	If Memory Access control (36h) B5 = 1:																								
	The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixel Data 1 is stored in frame memory at (SC, SP). The page register is then incremented and pixels are written to the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are written to the frame memory until the column register equals the End column (EC) value or the host processor sends another command. If the number of pixels exceeds (EC – SC + 1) * (EP – SP + 1) the extra pixels are ignored.																								
Restriction	There is no restriction on length of parameters.																								
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Contents of memory is set randomly</td></tr><tr><td>SW Reset</td><td>Contents of memory is set randomly</td></tr><tr><td>HW Reset</td><td>Contents of memory is set randomly</td></tr></table>													Status	Default Value	Power On Sequence	Contents of memory is set randomly	SW Reset	Contents of memory is set randomly	HW Reset	Contents of memory is set randomly				
Status	Default Value																								
Power On Sequence	Contents of memory is set randomly																								
SW Reset	Contents of memory is set randomly																								
HW Reset	Contents of memory is set randomly																								

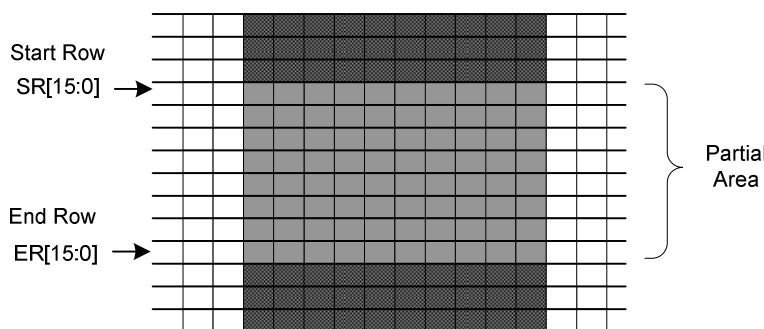
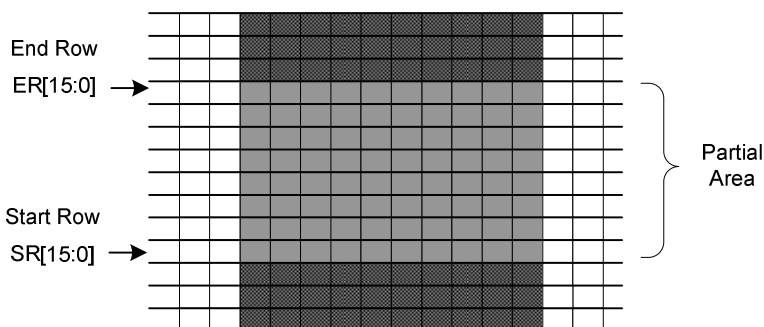
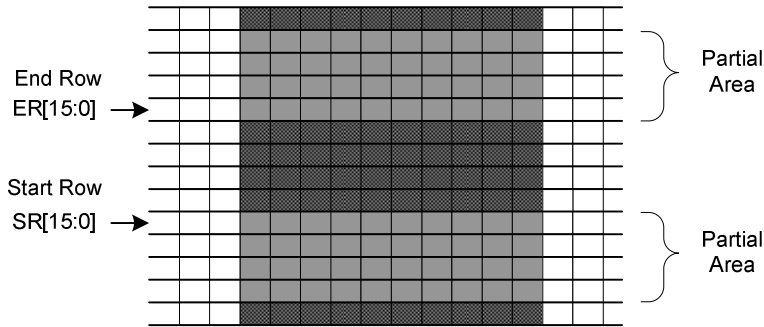


8.2.23. Memory Read (2Eh)

2Eh	RAMRD (Memory Read)																								
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XXXXXXXX	0	0	1	0	1	1	1	0	2Eh												
1 st Parameter	1	1	↑	XXXXXXXX	X	X	X	X	X	X	X	X	XX												
2 nd Parameter	1	1	↑	D1[15:0]									XX												
:	1	1	↑	Dx[15:0]									XX												
(N+1) th Parameter	1	1	↑	Dn[15:0]									XX												
Description	This command transfers image data from ILI9486L's frame memory to the host processor starting at the pixel location specified by preceding set_column_address and set_page_address commands.																								
	If Memory Access control B5 = 0:																								
	The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixels are read from frame memory at (SC, SP). The column register is then incremented and pixels read from the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are read from the frame memory until the page register equals the End Page (EP) value or the host processor sends another command.																								
	If Memory Access Control B5 = 1:																								
	The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixels are read from frame memory at (SC, SP). The page register is then incremented and pixels read from the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are read from the frame memory until the column register equals the End Column (EC) value or the host processor sends another command.																								
Restriction	There is no restriction on length of parameters.																								
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Contents of memory is set randomly</td></tr><tr><td>SW Reset</td><td>Contents of memory is set randomly</td></tr><tr><td>HW Reset</td><td>Contents of memory is set randomly</td></tr></table>													Status	Default Value	Power On Sequence	Contents of memory is set randomly	SW Reset	Contents of memory is set randomly	HW Reset	Contents of memory is set randomly				
Status	Default Value																								
Power On Sequence	Contents of memory is set randomly																								
SW Reset	Contents of memory is set randomly																								
HW Reset	Contents of memory is set randomly																								



8.2.24. Partial Area (30h)

30h	PLTAR (Partial Area)												
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	0	0	1	1	0	0	0	0	30h
1 st Parameter	1	1	↑	XXXXXXXX	SR[15:8]								XX
2 nd Parameter	1	1	↑	XXXXXXXX	SR[7:0]								XX
3 rd Parameter	1	1	↑	XXXXXXXX	ER[15:8]								XX
4 th Parameter	1	1	↑	XXXXXXXX	ER[7:0]								XX
Description	This command defines the Partial Display mode's display area. There are two parameters associated with this command, the first defines the Start Row (SR) and the second the End Row (ER), as illustrated in the following figure. SR and ER refer to the Frame Memory												
	If End Row>Start Row when MADCTL B4=0:-												
	<div><div>Start Row SR[15:0] →</div><div>End Row ER[15:0] →</div><div></div><div>Partial Area</div></div>												
	If End Row>Start Row when MADCTL B4=1:-												
	<div><div>End Row ER[15:0] →</div><div>Start Row SR[15:0] →</div><div></div><div>Partial Area</div></div>												
Restriction	If End Row<Start Row when MADCTL B4=0:-												
	<div><div>End Row ER[15:0] →</div><div>Start Row SR[15:0] →</div><div></div><div>Partial Area</div></div>												
	If End Row = Start Row then the Partial Area will be one row deep. X = don't care.												

Register Availability	<table><tr><th>Status</th><th colspan="2">Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td colspan="2">Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td colspan="2">Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td colspan="2">Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td colspan="2">Yes</td></tr><tr><td>Sleep In</td><td colspan="2">Yes</td></tr></table>			Status	Availability		Normal Mode On, Idle Mode Off, Sleep Out	Yes		Normal Mode On, Idle Mode On, Sleep Out	Yes		Partial Mode On, Idle Mode Off, Sleep Out	Yes		Partial Mode On, Idle Mode On, Sleep Out	Yes		Sleep In	Yes	
	Status	Availability																			
	Normal Mode On, Idle Mode Off, Sleep Out	Yes																			
	Normal Mode On, Idle Mode On, Sleep Out	Yes																			
	Partial Mode On, Idle Mode Off, Sleep Out	Yes																			
	Partial Mode On, Idle Mode On, Sleep Out	Yes																			
Sleep In	Yes																				
Default	<table><tr><th>Status</th><th colspan="2">Default Value</th></tr><tr><td>Power On Sequence</td><td>SR[15:0]=0000_{HEX}</td><td>ER[15:0]=01DF_{HEX}</td></tr><tr><td>SW Reset</td><td>SR[15:0]=0000_{HEX}</td><td>ER[15:0]=01DF_{HEX}</td></tr><tr><td>HW Reset</td><td>SR[15:0]=0000_{HEX}</td><td>ER[15:0]=01DF_{HEX}</td></tr></table>			Status	Default Value		Power On Sequence	SR[15:0]=0000 _{HEX}	ER[15:0]=01DF _{HEX}	SW Reset	SR[15:0]=0000 _{HEX}	ER[15:0]=01DF _{HEX}	HW Reset	SR[15:0]=0000 _{HEX}	ER[15:0]=01DF _{HEX}						
	Status	Default Value																			
	Power On Sequence	SR[15:0]=0000 _{HEX}	ER[15:0]=01DF _{HEX}																		
	SW Reset	SR[15:0]=0000 _{HEX}	ER[15:0]=01DF _{HEX}																		
HW Reset	SR[15:0]=0000 _{HEX}	ER[15:0]=01DF _{HEX}																			
Flow Chart	<div><div><div>1. To Enter Partial Mode</div><div><div>Any Mode</div><div>PTLAR (30h)</div><div>1st Parameter: SR[15:8] 2nd Parameter: SR[7:0]</div><div>3rd Parameter: ER[15:8] 4th Parameter: ER[7:0]</div><div>PTLON (12h)</div><div>Partial Mode ON</div></div></div><div><div>2. To Exit Partial Mode</div><div><div>Partial Mode ON</div><div>DISPOFF (28h)</div><div>NORON (13h)</div><div>Normal Mode ON</div><div>Optional (To avoid Tearing Effect)</div><div>RAMWR (2Ch)</div><div>Image Data D1[23:0], D2[23:0]..Dn[23:0]</div><div>DSIPON (29h)</div></div></div><div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div></div>																				

8.2.25. Vertical Scrolling Definition (33h)

33h	VSCRDEF (Vertical Scrolling Definition)												
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	0	0	1	1	0	0	1	1	33h
1 st Parameter	1	1	↑	XXXXXXXX	TFA[15:8]								XX
2 nd Parameter	1	1	↑	XXXXXXXX	TFA[7:0]								XX
3 rd Parameter	1	1	↑	XXXXXXXX	VSA[15:8]								XX
4 th Parameter	1	1	↑	XXXXXXXX	VSA[7:0]								XX
5 th Parameter	1	1	↑	XXXXXXXX	BFA[15:8]								XX
6 th Parameter	1	1	↑	XXXXXXXX	BFA[7:0]								XX

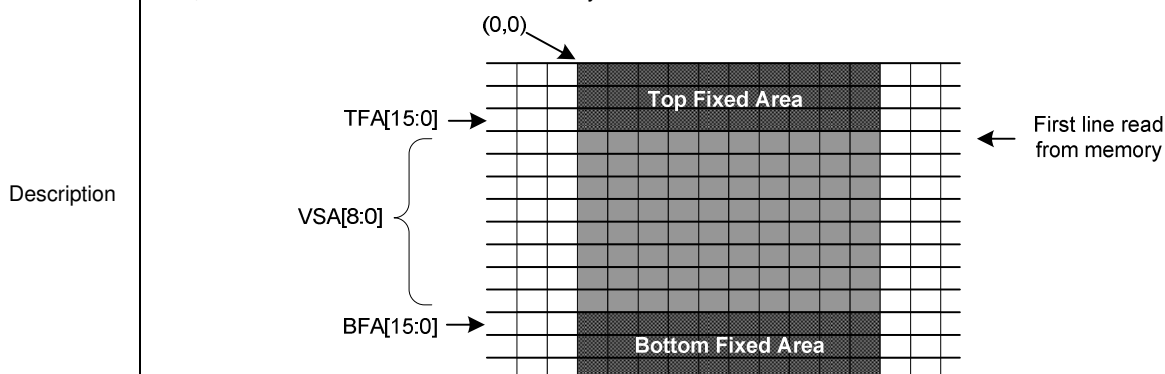
This command defines the display vertical scrolling area.

Memory Access Control (36h) B4 = 0:

The 1st & 2nd parameter, TFA[8:0], describes the Top Fixed Area in number of lines from the top of the frame memory. The top of the frame memory and top of the display device are aligned. The 3rd & 4th parameter, VSA[8:0], describes the height of the Vertical Scrolling Area in number of lines of frame memory from the Vertical Scrolling Start Address. The first line of the Vertical Scrolling Area starts immediately after the bottom most line of the Top Fixed Area. The last line of the Vertical Scrolling Area ends immediately before the top most line of the Bottom Fixed Area.

The 5th & 6th parameter, BFA[8:0], describes the Bottom Fixed Area in number of lines from the bottom of the frame memory. The bottom of the frame memory and bottom of the display device are aligned.

TFA, VSA and BFA refer to the Frame Memory Line Pointer.



Memory Access Control (36h) B4 = 1:

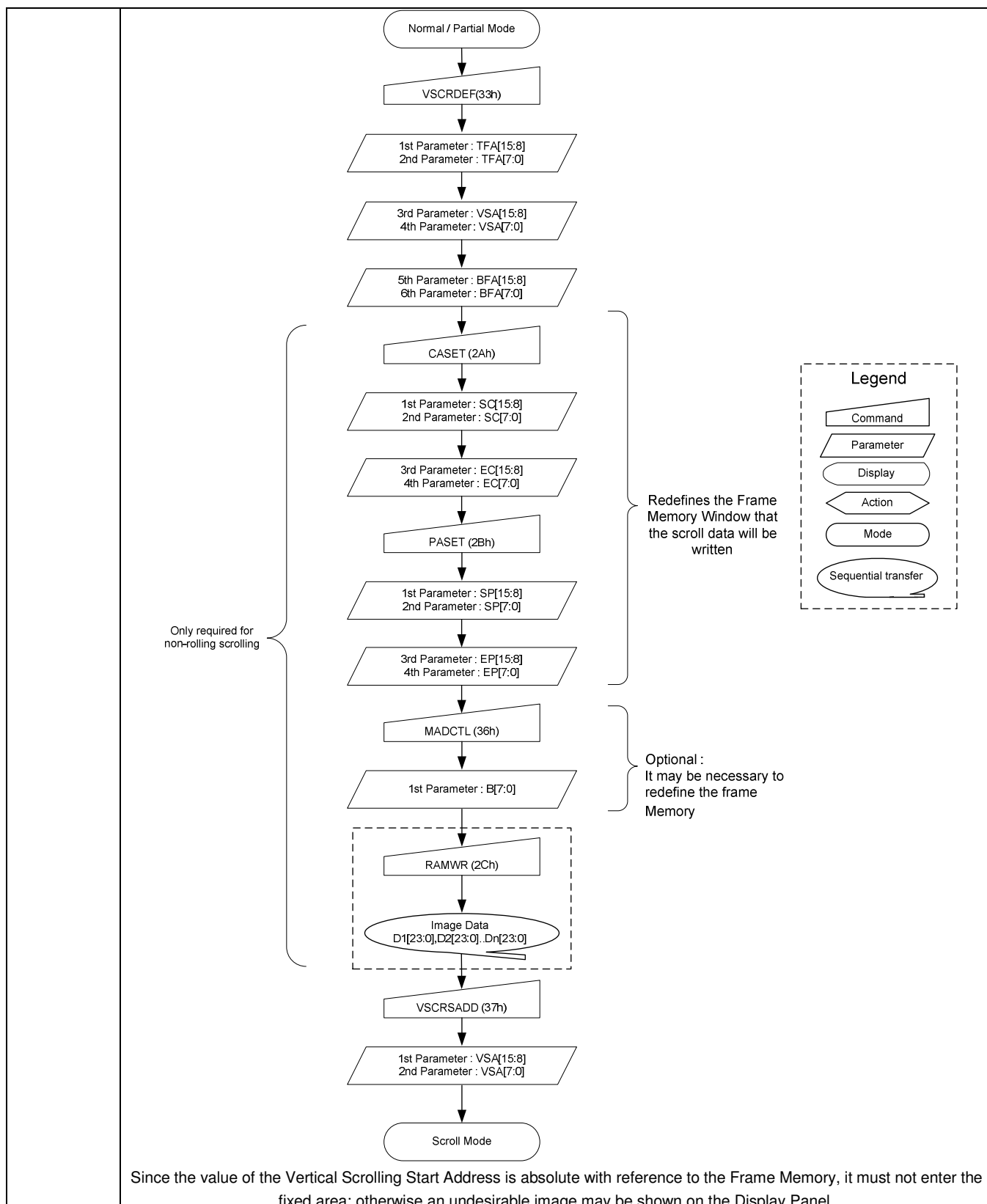
The 1st & 2nd parameter, TFA[8:0], describes the Top Fixed Area in number of lines from the bottom of the frame memory. The bottom of the frame memory and bottom of the display device are aligned.

The 3rd & 4th parameter, VSA[8:0], describes the height of the Vertical Scrolling Area in number of lines of frame memory from the Vertical Scrolling Start Address. The first line of the Vertical Scrolling Area starts immediately after the top most line of the Top Fixed Area. The last line of the Vertical Scrolling Area ends immediately before the bottom most line of the Bottom Fixed Area.

The 5th & 6th parameter, BFA[8:0], describes the Bottom Fixed Area in number of lines from the top of the frame memory. The top of the frame memory and top of the display device are aligned.

TFA, VSA and BFA refer to the Frame Memory Line Pointer.

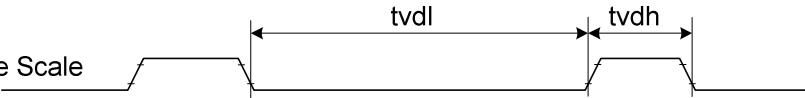
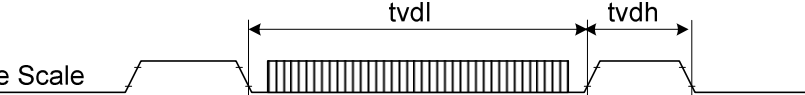
	<div><div><div><div><div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><d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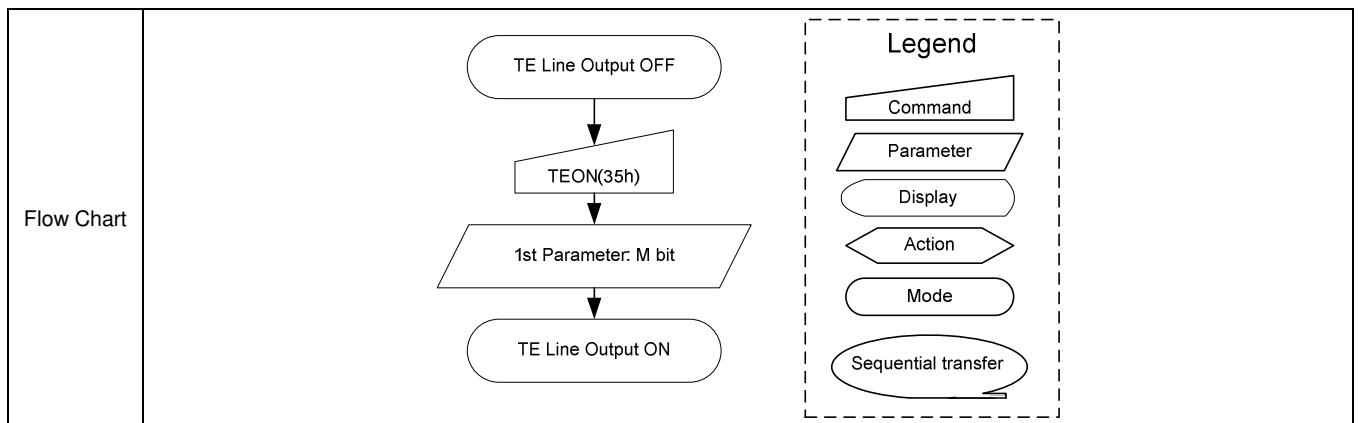


8.2.26. Tearing Effect Line OFF (34h)

34h	TEOFF (Tearing Effect Line OFF)																								
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XXXXXXXX	0	0	1	1	0	1	0	0	34h												
Parameter	No parameter																								
Description	This command turns off ILI9486L's Tearing Effect output signal on the TE signal line.																								
Restriction	This command has no effect when the Tearing Effect output is already off.																								
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>OFF</td></tr><tr><td>SW Reset</td><td>OFF</td></tr><tr><td>HW Reset</td><td>OFF</td></tr></table>													Status	Default Value	Power On Sequence	OFF	SW Reset	OFF	HW Reset	OFF				
Status	Default Value																								
Power On Sequence	OFF																								
SW Reset	OFF																								
HW Reset	OFF																								
Flow Chart	<div><div><div>TE Output ON or OFF</div><div>↓</div><div>TEOFF (34h)</div><div>↓</div><div>TE Output OFF</div></div><div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div></div>																								

8.2.27. Tearing Effect Line ON (35h)

35h	TEON (Tearing Effect Line ON)																									
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX													
Command	0	1	↑	XXXXXXXX	0	0	1	1	0	1	0	1	35h													
Parameter	1	1	↑	XXXXXXXX	X	X	X	X	X	X	X	M	XX													
Parameter	No parameter																									
Description	<p>This command is used to turn ON the Tearing Effect output signal from the TE signal line. This output is not affected by changing MADCTL bit B4. The Tearing Effect Line On has one parameter which describes the mode of the Tearing Effect Output Line.</p> <p>(X=Don't Care).</p> <p>When M=0:</p> <p>The Tearing Effect Output line consists of V-Blanking information only:</p> <div><p>Vertical Time Scale</p></div> <p>When M=1:</p> <p>The Tearing Effect Output Line consists of both V-Blanking and H-Blanking information:</p> <div><p>Vertical Time Scale</p></div> <p>Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.</p> <p>X = don't care.</p>																									
	Restriction	This command has no effect when the Tearing Effect output is already off.																								
	Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
	Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																									
Normal Mode On, Idle Mode On, Sleep Out	Yes																									
Partial Mode On, Idle Mode Off, Sleep Out	Yes																									
Partial Mode On, Idle Mode On, Sleep Out	Yes																									
Sleep In	Yes																									
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>OFF</td></tr><tr><td>SW Reset</td><td>OFF</td></tr><tr><td>HW Reset</td><td>OFF</td></tr></table>													Status	Default Value	Power On Sequence	OFF	SW Reset	OFF	HW Reset	OFF					
Status	Default Value																									
Power On Sequence	OFF																									
SW Reset	OFF																									
HW Reset	OFF																									



8.2.28. Memory Access Control (36h)

36h	MADCTL (Memory Access Control)												
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	0	0	1	1	0	1	1	0	36h
Parameter	1	1	↑	XXXXXXXX	MY	MX	MV	ML	BGR	MH	X	X	XX

This command defines read/write scanning direction of frame memory.

This command makes no change on the other driver status.

Bit	Symbol	Name	Description
D7	MY	Row Address Order	These 3 bits control MPU to memory write/read direction.
D6	MX	Column Address Order	
D5	MV	Row / Column Exchange	
D4	ML	Vertical Refresh Order	LCD vertical refresh direction control.
D3	BGR	RGB-BGR Order	Color selector switch control (0=RGB color filter panel, 1=BGR color filter panel)
D2	MH	Horizontal Refresh ORDER	LCD horizontal refreshing direction control.
D1	X	Reserved	Reserved
D0	X	Reserved	Reserved

X = don't care.

MV(Vertical refresh order bit)="0"

MV(Vertical refresh order bit)="1"

ML(Vertical refresh order bit)="0"

ML(Vertical refresh order bit)="1"

BGR(Vertical refresh order bit)="0"

BGR(Vertical refresh order bit)="1"

	<div> <div>MH(Horizontal refresh order control bit)="0"</div> </div> <div> <div>MH(Horizontal refresh order control bit)="1"</div> </div> <p>Note: Top-Left (0,0) means a physical memory location.</p>												
Restriction													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default	<table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>00h</td></tr> <tr> <td>SW Reset</td><td>No change</td></tr> <tr> <td>HW Reset</td><td>00h</td></tr> </tbody> </table>	Status	Default Value	Power On Sequence	00h	SW Reset	No change	HW Reset	00h				
Status	Default Value												
Power On Sequence	00h												
SW Reset	No change												
HW Reset	00h												
Flow Chart	<div> <div>MADCTR(36h)</div> <div>1st Parameter: MY, MX, MV, ML, RGB, MH</div> </div> <div> <p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer </div>												

8.2.29. Vertical Scrolling Start Address (37h)

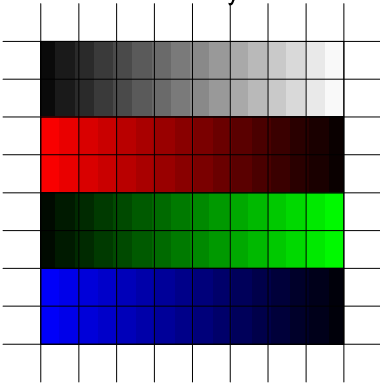
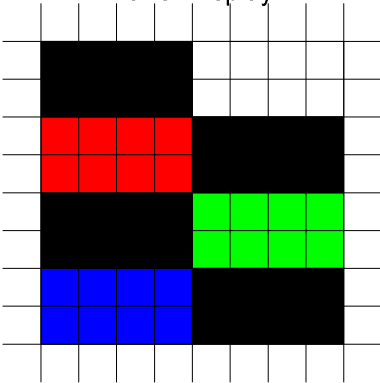
37h	VSCRSADD (Vertical Scrolling Start Address)																						
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX										
Command	0	1	↑	XXXXXXXX	0	0	1	1	0	1	1	1	37h										
1 st Parameter	1	1	↑	XXXXXXXX	VSP[15:8]								XX										
2 nd Parameter	1	1	↑	XXXXXXXX	VSP[7:0]								XX										
Description	<p>This command is used together with Vertical Scrolling Definition (33h). These two commands describe the scrolling area and the scrolling mode. The Vertical Scrolling Start Address command has one parameter which describes the address of the line in the Frame Memory that will be written as the first line after the last line of the Top Fixed Area on the display as illustrated below:-</p> <p>When MADCTL B4=0</p> <p>Example:</p> <p>When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 480 and VSP='3'.</p>																						
	<div><div><p>Frame Memory</p></div><div><p>Pointer B4=0</p><table><tr><td>0</td></tr><tr><td>1</td></tr><tr><td>2</td></tr><tr><td>3</td></tr><tr><td>4</td></tr><tr><td>..</td></tr><tr><td>..</td></tr><tr><td>477</td></tr><tr><td>478</td></tr><tr><td>479</td></tr></table></div><div><p>Display</p></div></div>													0	1	2	3	4	477	478	479
	0																						
	1																						
	2																						
3																							
4																							
..																							
..																							
477																							
478																							
479																							
<p>When MADCTL B4=1</p> <p>Example:</p> <p>When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 480 and VSP='3'.</p>																							
<div><div><p>Frame Memory</p></div><div><p>Pointer B4=1</p><table><tr><td>479</td></tr><tr><td>478</td></tr><tr><td>477</td></tr><tr><td>..</td></tr><tr><td>..</td></tr><tr><td>4</td></tr><tr><td>3</td></tr><tr><td>2</td></tr><tr><td>1</td></tr><tr><td>0</td></tr></table></div><div><p>Display</p></div></div>													479	478	477	4	3	2	1	0	
479																							
478																							
477																							
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..																							
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3																							
2																							
1																							
0																							
<p>Notes: (1) When new Pointer position and Picture Data are sent, the result on the display will happen at the next Panel Scan to avoid tearing effect.</p> <p>VSP refers to the Frame Memory line Pointer.</p> <p>X = Don't care</p>																							

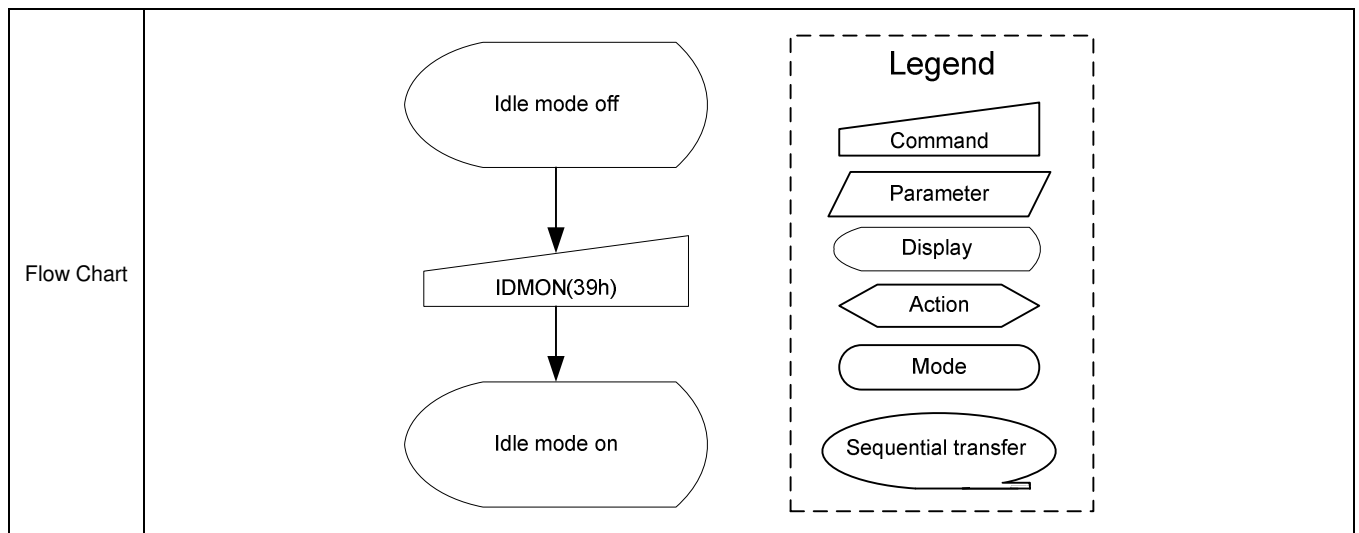
Restriction	Since the value of the Vertical Scrolling Start Address is absolute (with reference to the Frame Memory), it must not enter the fixed area (defined by Vertical Scrolling Definition (33h) – otherwise undesirable image will be displayed on the Panel.												
Register Availability	<table> <tr> <th>Status</th><th>Availability</th></tr> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default	<table> <tr> <th>Status</th><th>Default Value</th></tr> <tr> <td>Power On Sequence</td><td>00h</td></tr> <tr> <td>SW Reset</td><td>00h</td></tr> <tr> <td>HW Reset</td><td>00h</td></tr> </table>	Status	Default Value	Power On Sequence	00h	SW Reset	00h	HW Reset	00h				
Status	Default Value												
Power On Sequence	00h												
SW Reset	00h												
HW Reset	00h												
Flow Chart	See Vertical Scrolling Definition (33h) description.												

8.2.30. Idle Mode OFF (38h)

38h	IDMOFF (Idle Mode OFF)																								
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XXXXXXXX	0	0	1	1	1	0	0	0	38h												
Parameter	No parameter																								
Description	This command causes ILI9486L to exit Idle mode. In Idle OFF mode, display panel can display maximum 262,144 colors.																								
Restriction	This command has no effect when ILI9486L is not in Idle mode.																								
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Idle Mode Off</td></tr><tr><td>SW Reset</td><td>Idle Mode Off</td></tr><tr><td>HW Reset</td><td>Idle Mode Off</td></tr></table>													Status	Default Value	Power On Sequence	Idle Mode Off	SW Reset	Idle Mode Off	HW Reset	Idle Mode Off				
Status	Default Value																								
Power On Sequence	Idle Mode Off																								
SW Reset	Idle Mode Off																								
HW Reset	Idle Mode Off																								
Flow Chart	<div><div><div>Idle Mode ON</div><div>↓</div><div>IDMOFF (38h)</div><div>↓</div><div>Idle Mode OFF</div></div><div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div></div>																								

8.2.31. Idle Mode ON (39h)

39h	IDMON (Idle Mode ON)																																																																																																																																																																																																			
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																																																																																																																																																							
Command	0	1	↑	XXXXXXXX	0	0	1	1	1	0	0	1	39h																																																																																																																																																																																							
Parameter	No parameter																																																																																																																																																																																																			
Description	<p>This command is used to enter into Idle mode on.</p> <p>In the idle on mode, color expression is reduced. The primary and the secondary colors using MSB of each R, G and B in the Frame Memory, 8 color depth data is displayed.</p>																																																																																																																																																																																																			
	<div><div><p>Memory</p></div><div>→</div><div><p>Panel Display</p></div></div>																																																																																																																																																																																																			
	<table><tr><th colspan="12">Memory Contents vs Display Color</th></tr><tr><th></th><th>R₅</th><th>R₄</th><th>R₃</th><th>R₂</th><th>R₁</th><th>R₀</th><th>G₅</th><th>G₄</th><th>G₃</th><th>G₂</th><th>G₁</th><th>G₀</th><th>B₅</th><th>B₄</th><th>B₃</th><th>B₂</th><th>B₁</th><th>B₀</th></tr><tr><td>Black</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr><tr><td>Blue</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td></tr><tr><td>Red</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr><tr><td>Magenta</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td></tr><tr><td>Green</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr><tr><td>Cyan</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td></tr><tr><td>Yellow</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr><tr><td>White</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td></tr></table>													Memory Contents vs Display Color													R ₅	R ₄	R ₃	R ₂	R ₁	R ₀	G ₅	G ₄	G ₃	G ₂	G ₁	G ₀	B ₅	B ₄	B ₃	B ₂	B ₁	B ₀	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Memory Contents vs Display Color																																																																																																																																																																																																			
	R ₅	R ₄	R ₃	R ₂	R ₁	R ₀	G ₅	G ₄	G ₃	G ₂	G ₁	G ₀	B ₅	B ₄	B ₃	B ₂	B ₁	B ₀																																																																																																																																																																																		
Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0																																																																																																																																																																																		
Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1																																																																																																																																																																																		
Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0																																																																																																																																																																																		
Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1																																																																																																																																																																																		
Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0																																																																																																																																																																																		
Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1																																																																																																																																																																																		
Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0																																																																																																																																																																																		
White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1																																																																																																																																																																																		
	X = don't care.																																																																																																																																																																																																			
Restriction	This command has no effect when module is already in idle off mode.																																																																																																																																																																																																			
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes																																																																																																																																																																											
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Sleep In	Yes																																																																																																																																																																																																			
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Idle mode OFF</td></tr><tr><td>SW Reset</td><td>Idle mode OFF</td></tr><tr><td>HW Reset</td><td>Idle mode OFF</td></tr></table>													Status	Default Value	Power On Sequence	Idle mode OFF	SW Reset	Idle mode OFF	HW Reset	Idle mode OFF																																																																																																																																																																															
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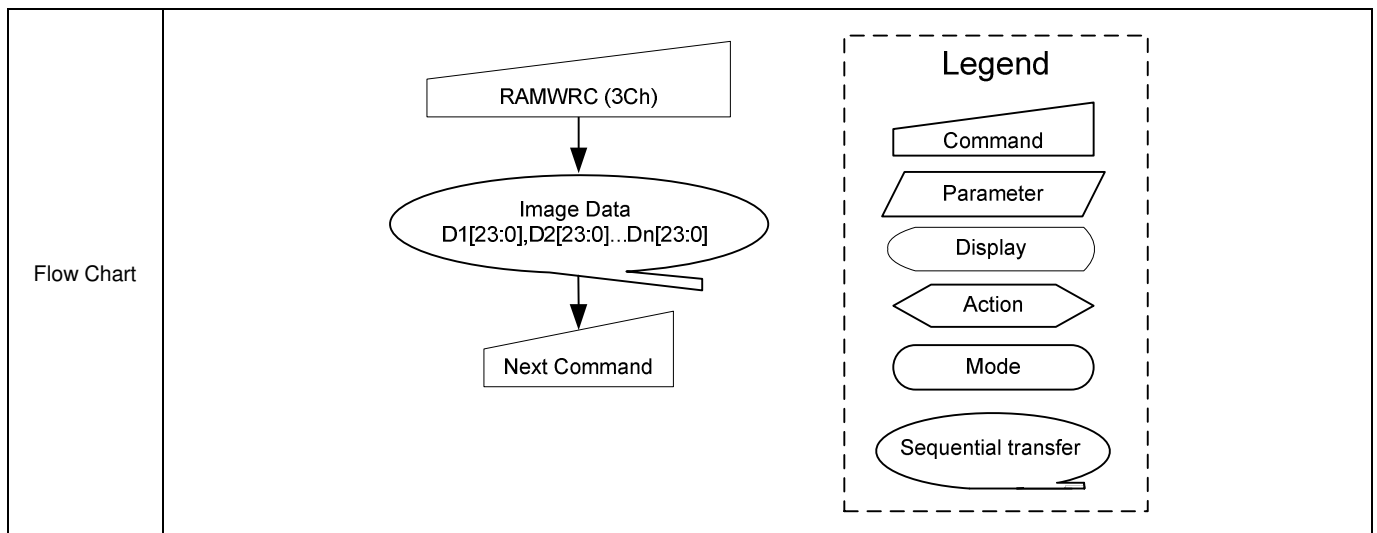


8.2.32. Interface Pixel Format (3Ah)

3Ah	COLMOD (Interface Pixel Format)																																																																																								
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																																												
Command	0	1	↑	XXXXXXXX	0	0	1	1	1	0	1	0	3Ah																																																																												
Parameter	1	1	↑	XXXXXXXX	DPI[3:0]				X	DBI[2:0]			XX																																																																												
Description	<p>This command sets the pixel format for the RGB image data used by the interface. DPI[3:0] is the pixel format select of RGB interface and DBI[2:0] is the pixel format of CPU interface. If a particular interface, either RGB interface or CPU interface, is not used then the corresponding bits in the parameter are ignored. The pixel format are shown in the table below.</p>																																																																																								
	<table><tr><th colspan="4">DPI[3:0]</th><th>RGB Interface Format</th></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>Reserved</td></tr><tr><td>0</td><td>0</td><td>0</td><td>1</td><td>Reserved</td></tr><tr><td>0</td><td>0</td><td>1</td><td>0</td><td>Reserved</td></tr><tr><td>0</td><td>0</td><td>1</td><td>1</td><td>Reserved</td></tr><tr><td>0</td><td>1</td><td>0</td><td>0</td><td>Reserved</td></tr><tr><td>0</td><td>1</td><td>0</td><td>1</td><td>16 bits / pixel</td></tr><tr><td>0</td><td>1</td><td>1</td><td>0</td><td>18 bits / pixel</td></tr><tr><td>0</td><td>1</td><td>1</td><td>1</td><td>Reserved</td></tr></table>				DPI[3:0]				RGB Interface Format	0	0	0	0	Reserved	0	0	0	1	Reserved	0	0	1	0	Reserved	0	0	1	1	Reserved	0	1	0	0	Reserved	0	1	0	1	16 bits / pixel	0	1	1	0	18 bits / pixel	0	1	1	1	Reserved	<table><tr><th colspan="3">DBI[2:0]</th><th>CPU Interface Format</th></tr><tr><td>0</td><td>0</td><td>0</td><td>Reserved</td></tr><tr><td>0</td><td>0</td><td>1</td><td>Reserved</td></tr><tr><td>0</td><td>1</td><td>0</td><td>Reserved</td></tr><tr><td>0</td><td>1</td><td>1</td><td>Reserved</td></tr><tr><td>1</td><td>0</td><td>0</td><td>Reserved</td></tr><tr><td>1</td><td>0</td><td>1</td><td>16 bits / pixel</td></tr><tr><td>1</td><td>1</td><td>0</td><td>18 bits / pixel</td></tr><tr><td>1</td><td>1</td><td>1</td><td>Reserved</td></tr></table>				DBI[2:0]			CPU Interface Format	0	0	0	Reserved	0	0	1	Reserved	0	1	0	Reserved	0	1	1	Reserved	1	0	0	Reserved	1	0	1	16 bits / pixel	1	1	0	18 bits / pixel	1	1	1	Reserved
	DPI[3:0]				RGB Interface Format																																																																																				
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	0	0	0	1	Reserved																																																																																				
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Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>06h</td></tr><tr><td>SW Reset</td><td>06h</td></tr><tr><td>HW Reset</td><td>06h</td></tr></table>													Status	Default Value	Power On Sequence	06h	SW Reset	06h	HW Reset	06h																																																																				
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HW Reset	06h																																																																																								
Flow Chart	<div><div><div>n-bit/Pixel Mode</div><div>↓</div><div>COLMOD (3Ah)</div><div>↓</div><div>1st parameter: D[2:0]=" XXX"</div><div>↓</div><div>New m-bit/Pixel Mode</div></div><div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div></div>																																																																																								

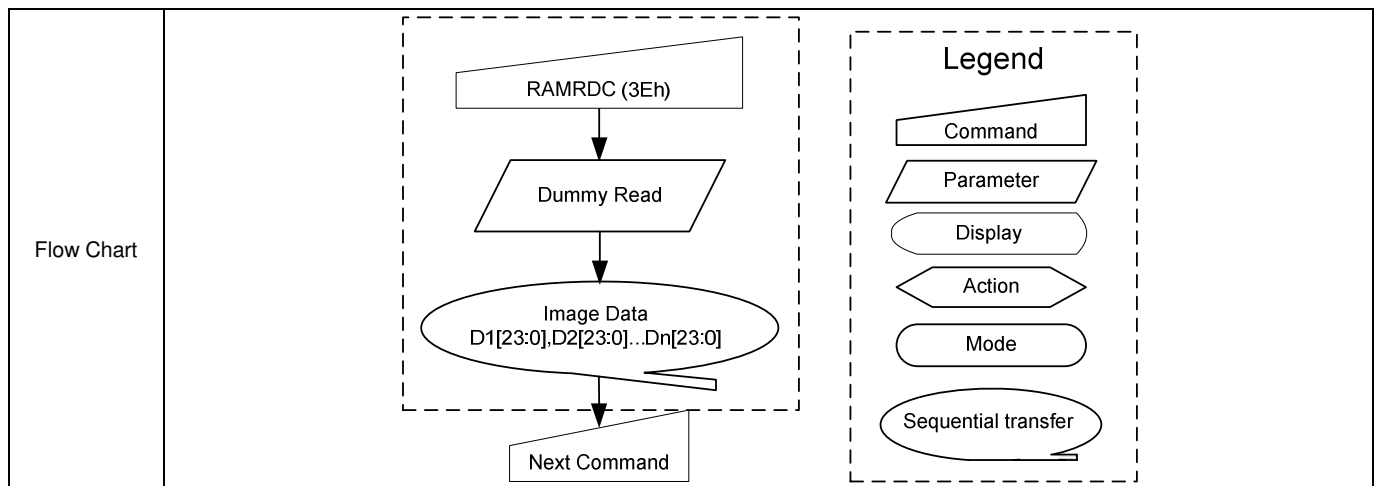
8.2.33. Memory Write Continue (3Ch)

3Ch	RAMWRC (Memory Write Continue)												
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	0	0	1	1	1	1	0	0	3Ch
1 st Parameter	1	1	↑	D1[15:0]									XX
:	1	1	↑	Dx[15:0]									XX
N th Parameter	1	1	↑	Dn[15:0]									XX
Description	This command is used to transfer data from MCU to frame memory, if there is wanted to continue memory write after “Memory Write (2Ch)” command.												
	This command makes no change to the other driver status.												
	When this command is accepted, the column register and the page register are not reset to the Start Column/Start Page positions as it has been done on “Memory Write (2Ch)” command.												
	Then D[15:0] is stored in frame memory and the column register and the page register incremented as table below: Column and Page Counter Control.												
	Condition						Column counter			Page Counter			
	When RAMWR/RAMRD command is accepted						Return to “Start Column”			Return to “Start Page”			
	Complete Pixel Read/Write action						Increment by 1			No change			
	The Column counter value is large than “End Column”						Return to “Start Column”			Increment by 1			
	The Page counter value is large than “End Page”						Return to “Start Column”			Return to “Start Page”			
	Sending any other command can stop frame Write.												
Restriction	X = don't care.												
	There is no restriction on length of parameters.												
Register Availability	No access in the frame memory in Sleep In mode.												
Default													
	Status						Availability						
	Power On Sequence						Contents of memory is set randomly						
	SW Reset						Contents of memory is set randomly						
	HW Reset						Contents of memory is set randomly						

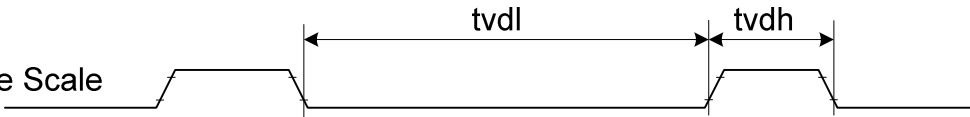
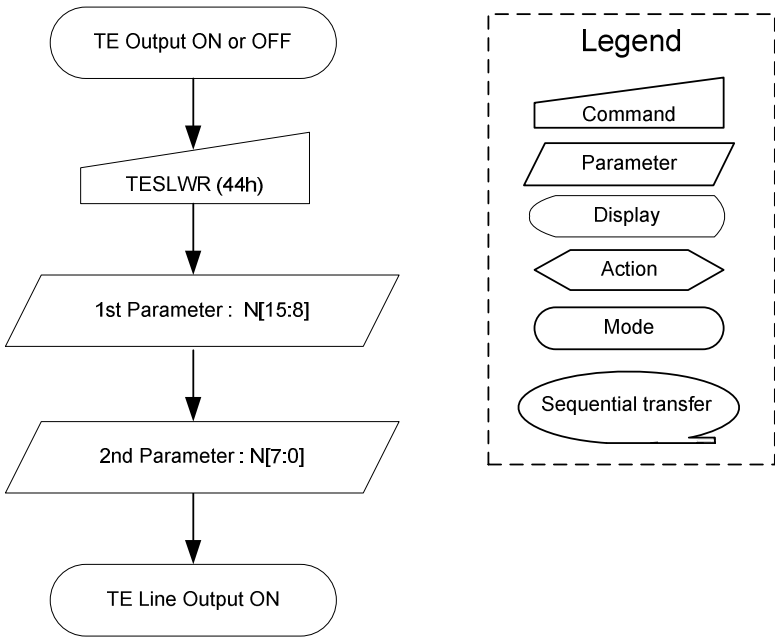


8.2.34. Memory Read Continue (3Eh)

3Eh	RAMRDRC (Memory Read Continue)												
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	0	0	1	1	1	1	1	0	3Eh
1 st Parameter	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX
2 nd Parameter	1	↑	1	D1[15:0]									XX
:	1	↑	1	Dx[15:0]									XX
N th Parameter	1	↑	1	Dn[15:0]									XX
Description	This command is used to transfer data from frame memory to MCU, if there is wanted to continue memory read after “Memory Read (2Eh)” command.												
	This command makes no change to the other driver status.												
	When this command is accepted, the column register and the page register are not reset to the Start Column/Start Page positions as it has been done on “Memory Read (2Eh)” command.												
	Then D[15:0] is read back from the frame memory and the column register and the page register incremented as table below:												
	Column and Page Counter Control.												
	Condition						Column counter			Page Counter			
	When RAMWR/RAMRD command is accepted						Return to “Start Column”			Return to “Start Page”			
	Complete Pixel Read/Write action						Increment by 1			No change			
	The Column counter value is large than “End Column”						Return to “Start Column”			Increment by 1			
	The Page counter value is large than “End Page”						Return to “Start Column”			Return to “Start Page”			
Frame Read can be stopped by sending any other command.													
X = can be ‘0’ or ‘1’													
Restriction	There is no restriction on length of parameters.												
	No access in the frame memory in Sleep In mode.												
Register Availability													
Default													



8.2.35. Write Tear Scan Line (44h)

44h	TESLWR (Write Tear Scan Line)																								
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XXXXXXXX	0	1	0	0	0	1	0	0	44h												
1 st Parameter	1	1	↑	XXXXXXXX	N[15:8]								XX												
2 nd Parameter	1	1	↑	XXXXXXXX	N[7:0]								XX												
Description	<p>This command turns on the display Tearing Effect output signal on the TE signal line when the display reaches line N. The TE signal is not affected by changing Memory Access Control bit B4. The Tearing Effect Line On has one parameter that describes the Tearing Effect Output Line mode. The Tearing Effect Output line consists of V-Blanking information only.</p> <p>Vertical Time Scale</p>  <p>Note that Set Tear Scan Line with N = 0 is equivalent to Tearing Effect Line ON with M = 0.</p> <p>The Tearing Effect Output line shall be active low when ILI9486L is in Sleep mode.</p>																								
Restriction	This command has no effect when Tearing Effect output is already ON.																								
Register Availability	<table><thead><tr><th>Status</th><th>Availability</th></tr></thead><tbody><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></tbody></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><thead><tr><th>Status</th><th>Default Value</th></tr></thead><tbody><tr><td>Power On Sequence</td><td>00h</td></tr><tr><td>SW Reset</td><td>No change</td></tr><tr><td>HW Reset</td><td>00h</td></tr></tbody></table>													Status	Default Value	Power On Sequence	00h	SW Reset	No change	HW Reset	00h				
Status	Default Value																								
Power On Sequence	00h																								
SW Reset	No change																								
HW Reset	00h																								
Flow Chart																									

8.2.36. Read Scan Line (45h)

45h	TESLRD (Read Tear Scan Line)																								
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XXXXXXXX	0	1	0	0	0	1	0	1	45h												
1 st Parameter	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX												
2 nd Parameter	1	↑	1	XXXXXXXX	N[15:8]								XX												
3 rd Parameter	1	↑	1	XXXXXXXX	N[7:0]								XX												
Description	<p>The display returns the current scan line, N, used to update the display device. The total number of scan lines on a display device is defined as VSYNC + VBP + VACT + VFP. The first scan line is defined as the first line of V-Sync and is denoted as Line 0.</p> <p>When in Sleep Mode, the value returned by Read Scan Line command is undefined.</p>																								
Restriction	None																								
Register Availability	<table><thead><tr><th>Status</th><th>Availability</th></tr></thead><tbody><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></tbody></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><thead><tr><th>Status</th><th>Default Value</th></tr></thead><tbody><tr><td>Power On Sequence</td><td>00h</td></tr><tr><td>SW Reset</td><td>No change</td></tr><tr><td>HW Reset</td><td>00h</td></tr></tbody></table>													Status	Default Value	Power On Sequence	00h	SW Reset	No change	HW Reset	00h				
Status	Default Value																								
Power On Sequence	00h																								
SW Reset	No change																								
HW Reset	00h																								
Flow Chart	<div><div><div>TESLRD (45h)</div><div>Dummy Read</div><div>2nd Parameter : N[15:8]</div><div>3rd Parameter : N[7:0]</div></div><div>Host ILI9486</div><div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div></div>																								

8.2.37. Write Display Brightness Value (51h)

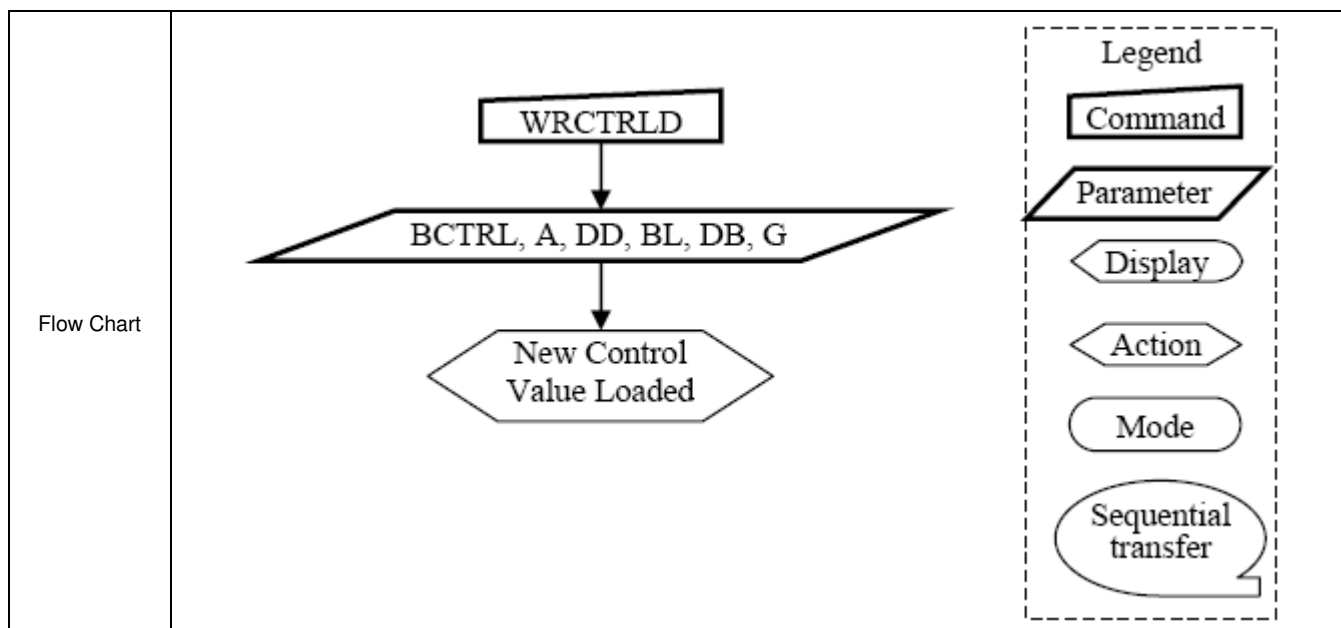
51h	WRDISBV (Write Display Brightness)																								
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XXXXXXXX	0	1	0	1	0	0	0	1	51h												
1 st Parameter	1	1	↑	XXXXXXXX	DBV[7:0]								XX												
Description	<p>This command is used to adjust the brightness value of the display.</p> <p>DBV[7:0]: 8 bit, for display brightness of manual brightness setting and CABC in ILI9486L. There is a PWM output signal, PWM_OUT pin, to control the LED driver IC in order to control display brightness.</p> <p>In principle relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.</p>																								
Restriction																									
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr><tr><td>Normal Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr><tr><td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr><tr><td>Partial Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr><tr><td>Sleep IN</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes	Normal Mode ON, Idle Mode ON, Sleep OUT	Yes	Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes	Partial Mode ON, Idle Mode ON, Sleep OUT	Yes	Sleep IN	Yes
Status	Availability																								
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes																								
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes																								
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes																								
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes																								
Sleep IN	Yes																								
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power ON Sequence</td><td>00h</td></tr><tr><td>H/W Reset</td><td>00h</td></tr></table>													Status	Default Value	Power ON Sequence	00h	H/W Reset	00h						
Status	Default Value																								
Power ON Sequence	00h																								
H/W Reset	00h																								
Flow Chart	<div><div><div>WRDISBV</div><div>↓</div><div>DBV[7..0]</div><div>↓</div><div>New Display Luminance Value Loaded</div></div><div><div>Legend</div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div>																								

8.2.38. Read Display Brightness Value (52h)

52h	RDDISBV (Read Display Brightness Value)																								
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XXXXXXXX	0	1	0	1	0	0	1	0	52h												
1 st Parameter	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX												
2 nd Parameter	1	↑	1	XXXXXXXX	DBV[7:0]							XX													
Description	<p>This command is used to return the brightness value of the display.</p> <p>DBV[7:0] is reset when display is in sleep-in mode.</p> <p>DBV[7:0] is '0' when bit BCTRL of "Write CTRL Display (53h)" command is '0'.</p> <p>DBV[7:0] is manual set brightness specified with "Write CTRL Display (53h)" command when BCTRL bit is '1'.</p> <p>When bit BCTRL of "Write CTRL Display (53h)" command is '1' and C1/C0 bit of "Write Content Adaptive Brightness Control (55h)" command are '0', DBV[7:0] output is the brightness value specified with " Write Display Brightness (51h)" command.</p>																								
Restriction	<p>ILI9486L is sending 2nd parameter value on the data lines if the MCU wants to read more than one parameter (= more than 2 RDX cycle) on parallel MCU interface.</p> <p>Only 2nd parameter is sent on DSI (The 1st parameter is not sent).</p>																								
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr><tr><td>Normal Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr><tr><td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr><tr><td>Partial Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr><tr><td>Sleep IN</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes	Normal Mode ON, Idle Mode ON, Sleep OUT	Yes	Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes	Partial Mode ON, Idle Mode ON, Sleep OUT	Yes	Sleep IN	Yes
Status	Availability																								
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes																								
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes																								
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes																								
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes																								
Sleep IN	Yes																								
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power ON Sequence</td><td>00h</td></tr><tr><td>H/W Reset</td><td>00h</td></tr></table>													Status	Default Value	Power ON Sequence	00h	H/W Reset	00h						
Status	Default Value																								
Power ON Sequence	00h																								
H/W Reset	00h																								
	<div><div><div>Serial I/F Mode (P/SX = Low)</div><div>Read RDDISBV</div><div>Send 2nd Parameter</div></div><div><div>Parallel I/F Mode (P/SX = High)</div><div>Read RDDISBV</div><div>Dummy Read</div><div>Send 2nd Parameter</div></div><div>Host</div><div>Display</div></div> <div><div>Legend</div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div>																								

8.2.39. Write CTRL Display Value (53h)

53h	WRCTRLD (Write Control Display)																								
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XXXXXXXX	0	1	0	1	0	0	1	1	53h												
1 st Parameter	1	1	↑	XXXXXXXX	X	X	BCTRL	X	DD	BL	X	X	XX												
Description	This command is used to control display brightness.																								
	BCTRL : Brightness Control Block On/Off, This bit is always used to switch brightness for display.																								
	<table><tr><th>BCTRL</th><th>Description</th></tr><tr><td>0</td><td>Brightness Control Block OFF (DBV[7:0]=00h)</td></tr><tr><td>1</td><td>Brightness Control Block ON (DBV[7:0] is active)</td></tr></table>													BCTRL	Description	0	Brightness Control Block OFF (DBV[7:0]=00h)	1	Brightness Control Block ON (DBV[7:0] is active)						
	BCTRL	Description																							
	0	Brightness Control Block OFF (DBV[7:0]=00h)																							
	1	Brightness Control Block ON (DBV[7:0] is active)																							
	DD : Display Dimming Control. This function is only for manual brightness setting.																								
	<table><tr><th>DD</th><th>Description</th></tr><tr><td>0</td><td>Display Dimming OFF</td></tr><tr><td>1</td><td>Display Dimming ON</td></tr></table>													DD	Description	0	Display Dimming OFF	1	Display Dimming ON						
	DD	Description																							
	0	Display Dimming OFF																							
1	Display Dimming ON																								
BL : Backlight Control On/Off																									
<table><tr><th>BL</th><th>Description</th></tr><tr><td>0</td><td>Backlight Control OFF</td></tr><tr><td>1</td><td>Backlight Control ON</td></tr></table>													BL	Description	0	Backlight Control OFF	1	Backlight Control ON							
BL	Description																								
0	Backlight Control OFF																								
1	Backlight Control ON																								
Dimming function is adapted to the brightness registers for display when bit BCTRL is changed at DD=1, e.g. BCTRL: 0 -> 1 or 1-> 0.																									
When BL bit change from “On” to “Off”, backlight is turned off without gradual dimming, even if dimming-on (DD=1) are selected.																									
X = Don’t care																									
Restriction																									
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr><tr><td>Normal Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr><tr><td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr><tr><td>Partial Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr><tr><td>Sleep IN</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes	Normal Mode ON, Idle Mode ON, Sleep OUT	Yes	Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes	Partial Mode ON, Idle Mode ON, Sleep OUT	Yes	Sleep IN	Yes
Status	Availability																								
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes																								
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes																								
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes																								
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes																								
Sleep IN	Yes																								
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power ON Sequence</td><td>00h</td></tr><tr><td>H/W Reset</td><td>00h</td></tr></table>													Status	Default Value	Power ON Sequence	00h	H/W Reset	00h						
Status	Default Value																								
Power ON Sequence	00h																								
H/W Reset	00h																								



8.2.40. Read CTRL Display Value (54h)

54h	RDCTRLD (Read Control Display Value)																								
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XXXXXXXX	0	1	0	1	0	1	0	0	54h												
1 st Parameter	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX												
2 nd Parameter	1	↑	1	XXXXXXXX	X	X	BCTRL	X	DD	BL	X	X	XX												
Description	This command is used to control display brightness.																								
	BCTRL: Brightness Control Block On/Off, This bit is always used to switch brightness for display.																								
	<table><tr><th>BCTRL</th><th>Description</th></tr><tr><td>0</td><td>Brightness Control Block OFF (DBV[7:0]=00h)</td></tr><tr><td>1</td><td>Brightness Control Block ON (DBV[7:0] is active)</td></tr></table>													BCTRL	Description	0	Brightness Control Block OFF (DBV[7:0]=00h)	1	Brightness Control Block ON (DBV[7:0] is active)						
	BCTRL	Description																							
	0	Brightness Control Block OFF (DBV[7:0]=00h)																							
	1	Brightness Control Block ON (DBV[7:0] is active)																							
	DD: Display Dimming Control. This function is only for manual brightness setting.																								
	<table><tr><th>DD</th><th>Description</th></tr><tr><td>0</td><td>Display Dimming OFF</td></tr><tr><td>1</td><td>Display Dimming ON</td></tr></table>													DD	Description	0	Display Dimming OFF	1	Display Dimming ON						
	DD	Description																							
	0	Display Dimming OFF																							
1	Display Dimming ON																								
BL: Backlight Control On/Off																									
<table><tr><th>BL</th><th>Description</th></tr><tr><td>0</td><td>Backlight Control OFF</td></tr><tr><td>1</td><td>Backlight Control ON</td></tr></table>													BL	Description	0	Backlight Control OFF	1	Backlight Control ON							
BL	Description																								
0	Backlight Control OFF																								
1	Backlight Control ON																								
X = Don't care																									
Restriction																									
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr><tr><td>Normal Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr><tr><td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr><tr><td>Partial Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr><tr><td>Sleep IN</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes	Normal Mode ON, Idle Mode ON, Sleep OUT	Yes	Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes	Partial Mode ON, Idle Mode ON, Sleep OUT	Yes	Sleep IN	Yes
Status	Availability																								
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes																								
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes																								
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes																								
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes																								
Sleep IN	Yes																								
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power ON Sequence</td><td>00h</td></tr><tr><td>H/W Reset</td><td>00h</td></tr></table>													Status	Default Value	Power ON Sequence	00h	H/W Reset	00h						
Status	Default Value																								
Power ON Sequence	00h																								
H/W Reset	00h																								
Flow Chart	<div><div><div>Serial I/F Mode (P/SX = Low)</div><div>Read RDCTRLD</div><div>Send 2nd Parameter</div></div><div><div>Parallel I/F Mode (P/SX = High)</div><div>Read RDCTRLD</div><div>Dummy Read</div><div>Send 2nd Parameter</div></div><div>Host Display</div></div> <div><div>Legend</div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div>																								

8.2.41. Write Content Adaptive Brightness Control Value (55h)

55h	WRCABC (Write Content Adaptive Brightness Control)																														
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX																		
Command	0	1	↑	XXXXXXXX	0	1	0	1	0	1	0	1	55h																		
1 st Parameter	1	1	↑	XXXXXXXX	X	X	X	X	X	X	C[1:0]		XX																		
Description	This command is used to set parameters for image content based adaptive brightness control functionality.																														
	There is possible to use 4 different modes for content adaptive image functionality, which are defined on a table below.																														
	<table><tr><td colspan="2">C[1:0]</td><td>Description</td></tr><tr><td>0</td><td>0</td><td>CABC OFF</td></tr><tr><td>0</td><td>1</td><td>User Interface Image</td></tr><tr><td>1</td><td>0</td><td>Still Picture</td></tr><tr><td>1</td><td>1</td><td>Moving Image</td></tr></table>													C[1:0]		Description	0	0	CABC OFF	0	1	User Interface Image	1	0	Still Picture	1	1	Moving Image			
	C[1:0]		Description																												
0	0	CABC OFF																													
0	1	User Interface Image																													
1	0	Still Picture																													
1	1	Moving Image																													
X = Don't care																															
Restriction																															
Register Availability	<table><tr><td colspan="2">Status</td><td>Availability</td></tr><tr><td colspan="2">Normal Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr><tr><td colspan="2">Normal Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr><tr><td colspan="2">Partial Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr><tr><td colspan="2">Partial Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr><tr><td colspan="2">Sleep IN</td><td>Yes</td></tr></table>													Status		Availability	Normal Mode ON, Idle Mode OFF, Sleep OUT		Yes	Normal Mode ON, Idle Mode ON, Sleep OUT		Yes	Partial Mode ON, Idle Mode OFF, Sleep OUT		Yes	Partial Mode ON, Idle Mode ON, Sleep OUT		Yes	Sleep IN		Yes
	Status		Availability																												
	Normal Mode ON, Idle Mode OFF, Sleep OUT		Yes																												
	Normal Mode ON, Idle Mode ON, Sleep OUT		Yes																												
	Partial Mode ON, Idle Mode OFF, Sleep OUT		Yes																												
	Partial Mode ON, Idle Mode ON, Sleep OUT		Yes																												
Sleep IN		Yes																													
Default	<table><tr><td>Status</td><td>Default Value</td></tr><tr><td>Power ON Sequence</td><td>00h</td></tr><tr><td>H/W Reset</td><td>00h</td></tr></table>													Status	Default Value	Power ON Sequence	00h	H/W Reset	00h												
	Status	Default Value																													
	Power ON Sequence	00h																													
	H/W Reset	00h																													
Flow Chart	<div><div>WRCABC</div><div>↓</div><div>1st parameter: C[1:0]</div><div>↓</div><div>New Adaptive Image Mode</div></div>																														
	<div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div>																														

8.2.42. Read Content Adaptive Brightness Control Value (56h)

56h	RDCABC (Read Content Adaptive Brightness Control)																											
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX															
Command	0	1	↑	XXXXXXXX	0	1	0	1	0	1	1	0	56h															
1 st Parameter	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX															
2 nd Parameter	1	↑	1	XXXXXXXX	X	X	X	X	X	X	C[1:0]		XX															
Description	<p>This command is used to read the settings for image content based adaptive brightness control functionality. There is possible to use 4 different modes for content adaptive image functionality which are defined on the table below.</p> <table><tr><th colspan="2">C[1:0]</th><th>Description</th></tr><tr><td>0</td><td>0</td><td>CABC OFF</td></tr><tr><td>0</td><td>1</td><td>User Interface Image</td></tr><tr><td>1</td><td>0</td><td>Still Picture</td></tr><tr><td>1</td><td>1</td><td>Moving Image</td></tr></table> <p>X = Don't care</p>													C[1:0]		Description	0	0	CABC OFF	0	1	User Interface Image	1	0	Still Picture	1	1	Moving Image
C[1:0]		Description																										
0	0	CABC OFF																										
0	1	User Interface Image																										
1	0	Still Picture																										
1	1	Moving Image																										
Restriction																												
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr><tr><td>Normal Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr><tr><td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr><tr><td>Partial Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr><tr><td>Sleep IN</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes	Normal Mode ON, Idle Mode ON, Sleep OUT	Yes	Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes	Partial Mode ON, Idle Mode ON, Sleep OUT	Yes	Sleep IN	Yes			
Status	Availability																											
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes																											
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes																											
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes																											
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes																											
Sleep IN	Yes																											
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power ON Sequence</td><td>00h</td></tr><tr><td>H/W Reset</td><td>00h</td></tr></table>													Status	Default Value	Power ON Sequence	00h	H/W Reset	00h									
Status	Default Value																											
Power ON Sequence	00h																											
H/W Reset	00h																											
Flow Chart	<div><div><div>Serial I/F Mode (P/SX = Low)</div><div>Read RDCABC</div><div>Send 2nd Parameter</div></div><div><div>Parallel I/F Mode (P/SX = High)</div><div>Read RDCABC</div><div>Dummy Read</div><div>Send 2nd Parameter</div></div><div>Host Display</div></div> <div><div>Legend</div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div>																											

8.2.43. Write CABC Minimum Brightness (5Eh)

5Eh	WRCABCMB (Write CABC Minimum Brightness)																								
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XXXXXXXX	0	1	0	1	1	1	1	0	5Eh												
1 st Parameter	1	1	↑	XXXXXXXX	CMB[7:0]								XX												
Description	<p>This command is used to set the minimum brightness value of the display for CABC function.</p> <p>CMB[7:0]: CABC minimum brightness control, this parameter is used to avoid too much brightness reduction.</p> <p>When CABC is active, CABC can not reduce the display brightness to less than CABC minimum brightness setting. Image processing function is worked as normal, even if the brightness can not be changed.</p> <p>This function does not affect to the other function, manual brightness setting. Manual brightness can be set the display brightness to less than CABC minimum brightness. Smooth transition and dimming function can be worked as normal.</p> <p>When display brightness is turned off (BCTRL=0 of “Write CTRL Display (53h)”), CABC minimum brightness setting is ignored.</p> <p>In principle relationship is that 00h value means the lowest brightness for CABC and FFh value means the highest brightness for CABC.</p>																								
Restriction																									
Register Availability	<table><thead><tr><th>Status</th><th>Availability</th></tr></thead><tbody><tr><td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr><tr><td>Normal Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr><tr><td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr><tr><td>Partial Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr><tr><td>Sleep IN</td><td>Yes</td></tr></tbody></table>													Status	Availability	Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes	Normal Mode ON, Idle Mode ON, Sleep OUT	Yes	Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes	Partial Mode ON, Idle Mode ON, Sleep OUT	Yes	Sleep IN	Yes
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Sleep IN	Yes																								
Default	<table><thead><tr><th>Status</th><th>Default Value</th></tr></thead><tbody><tr><td>Power ON Sequence</td><td>00h</td></tr><tr><td>H/W Reset</td><td>00h</td></tr></tbody></table>													Status	Default Value	Power ON Sequence	00h	H/W Reset	00h						
Status	Default Value																								
Power ON Sequence	00h																								
H/W Reset	00h																								
Flow Chart	<div><div><div>WRCABCMB</div><div>CMB[7..0]</div><div>New Display Luminance Value Loaded</div></div><div><div>Legend</div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div>																								

8.2.44. Read CABC Minimum Brightness (5Fh)

5Fh	RDCABCMB (Read CABC Minimum Brightness)																								
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XXXXXXXX	0	1	0	1	1	1	1	1	5Fh												
1 st Parameter	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX												
2 nd Parameter	1	↑	1	XXXXXXXX	CMB[7:0]								XX												
Description	<p>This command returns the minimum brightness value of CABC function.</p> <p>In principle the relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.</p> <p>CMB[7:0] is CABC minimum brightness specified with “Write CABC minimum brightness (5Eh)” command.</p>																								
Restriction	<p>ILI9486L is sending 2nd parameter value on the data lines if the MCU wants to read more than one parameter (= more than 2 RDX cycle) on parallel MCU interface.</p> <p>Only 2nd parameter is sent on DSI (The 1st parameter is not sent).</p>																								
Register Availability	<table><thead><tr><th>Status</th><th>Availability</th></tr></thead><tbody><tr><td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr><tr><td>Normal Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr><tr><td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr><tr><td>Partial Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr><tr><td>Sleep IN</td><td>Yes</td></tr></tbody></table>													Status	Availability	Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes	Normal Mode ON, Idle Mode ON, Sleep OUT	Yes	Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes	Partial Mode ON, Idle Mode ON, Sleep OUT	Yes	Sleep IN	Yes
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Normal Mode ON, Idle Mode ON, Sleep OUT	Yes																								
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes																								
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes																								
Sleep IN	Yes																								
Default	<table><thead><tr><th>Status</th><th>Default Value</th></tr></thead><tbody><tr><td>Power ON Sequence</td><td>00h</td></tr><tr><td>H/W Reset</td><td>00h</td></tr></tbody></table>													Status	Default Value	Power ON Sequence	00h	H/W Reset	00h						
Status	Default Value																								
Power ON Sequence	00h																								
H/W Reset	00h																								
Flow Chart	<div><div><div>Serial I/F Mode (P/SX = Low)</div><div>Read RDCABCMB</div><div>Send 2nd Parameter</div></div><div><div>Parallel I/F Mode (P/SX = High)</div><div>Read RDCABCMB</div><div>Dummy Read</div><div>Send 2nd Parameter</div></div><div>Host</div><div>Display</div></div> <div><div>Legend</div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div>																								

8.2.45. Read First Checksum (AAh)

AAh	RDFCS (Read First Checksum)																								
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XXXXXXXX	1	0	1	0	1	0	1	0	AAh												
1 st Parameter	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX												
2 nd Parameter	1	↑	1	XXXXXXXX	FCS[7:0]								XX												
Description	This command returns the first checksum what has been calculated from User's area registers and the frame memory after the write access to those registers and/or frame memory has been done. X = can be '0' or '1'																								
Restriction	It will be necessary to wait 150ms after there is the last write access on User area registers before there can read this checksum value. ILI9486L is sending 2nd parameter value on the data lines if the MCU wants to read more than one parameter (= more than 2 RDX cycle) on parallel MCU interface. Only 2nd parameter is sent on DSI (The 1st parameter is not sent).																								
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr><tr><td>Normal Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr><tr><td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr><tr><td>Partial Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr><tr><td>Sleep IN</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes	Normal Mode ON, Idle Mode ON, Sleep OUT	Yes	Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes	Partial Mode ON, Idle Mode ON, Sleep OUT	Yes	Sleep IN	Yes
Status	Availability																								
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes																								
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes																								
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes																								
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes																								
Sleep IN	Yes																								
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power ON Sequence</td><td>00h</td></tr><tr><td>H/W Reset</td><td>00h</td></tr></table>													Status	Default Value	Power ON Sequence	00h	H/W Reset	00h						
Status	Default Value																								
Power ON Sequence	00h																								
H/W Reset	00h																								
Flow Chart	<div><div><div>RDFCS</div><div>↓</div><div>Send 1st Parameter</div><div>↓</div><div>Send FCS[7:0]</div></div><div>Host Display</div></div> <div><div>Legend</div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div>																								

8.2.46. Read Continue Checksum (AFh)

AFh	RDCFCS (Read Continue Checksum)																								
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XXXXXXXX	1	0	1	0	1	1	1	1	AFh												
1 st Parameter	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX												
2 nd Parameter	1	↑	1	XXXXXXXX	CCS[7:0]							XX													
Description	This command returns the continue checksum what has been calculated continuously after the first checksum has calculated from User's area registers and the frame memory after the write access to those registers and/or frame memory has been done. X = can be '0' or '1'																								
Restriction	It will be necessary to wait 300ms after there is the last write access on User area registers before there can read this checksum value in the first time. ILI9486L is sending 2nd parameter value on the data lines if the MCU wants to read more than one parameter (= more than 2 RDX cycle) on parallel MCU interface. Only 2nd parameter is sent on DSI (The 1st parameter is not sent).																								
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr><tr><td>Normal Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr><tr><td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr><tr><td>Partial Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr><tr><td>Sleep IN</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes	Normal Mode ON, Idle Mode ON, Sleep OUT	Yes	Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes	Partial Mode ON, Idle Mode ON, Sleep OUT	Yes	Sleep IN	Yes
Status	Availability																								
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes																								
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes																								
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes																								
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes																								
Sleep IN	Yes																								
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power ON Sequence</td><td>00h</td></tr><tr><td>H/W Reset</td><td>00h</td></tr></table>													Status	Default Value	Power ON Sequence	00h	H/W Reset	00h						
Status	Default Value																								
Power ON Sequence	00h																								
H/W Reset	00h																								
Flow Chart	<div><div><div>RDCCS</div><div>↓</div><div>Send 1st Parameter</div><div>↓</div><div>Send CCS[7:0]</div></div><div>Host Display</div></div> <div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div>																								

8.2.47. Read ID1 (DAh)

DAh	RDID1 (Read ID1)																								
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XXXXXXXX	1	1	0	1	1	0	1	0	DAh												
1 st parameter	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX												
2 nd arameter	1	↑	1	XXXXXXXX	ID1[7:0]								XX												
Description	<p>This read byte identifies the LCD module's manufacturer ID and it is specified by User</p> <p>The 1st parameter is dummy data.</p> <p>The 2nd parameter is LCD module's manufacturer ID.</p> <p>X = Don't care</p>																								
Restriction	<p>ILI9486L is sending 2nd parameter value on the data lines if the MCU wants to read more than one parameter (= more than 2 RDX cycle) on parallel MCU interface.</p> <p>Only 2nd parameter is sent on DSI (The 1st parameter is not sent).</p>																								
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>XXh</td></tr><tr><td>HW Reset</td><td>XXh</td></tr></table>													Status	Default Value	Power On Sequence	XXh	HW Reset	XXh						
Status	Default Value																								
Power On Sequence	XXh																								
HW Reset	XXh																								
Flow Chart	<div><div><div>RDID1(DAh)</div><div>↓</div><div>1st Parameter: Dummy Read</div><div>↓</div><div>2nd Parameter: Send ID1[7:0]</div></div><div>Host Driver</div><div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div></div>																								

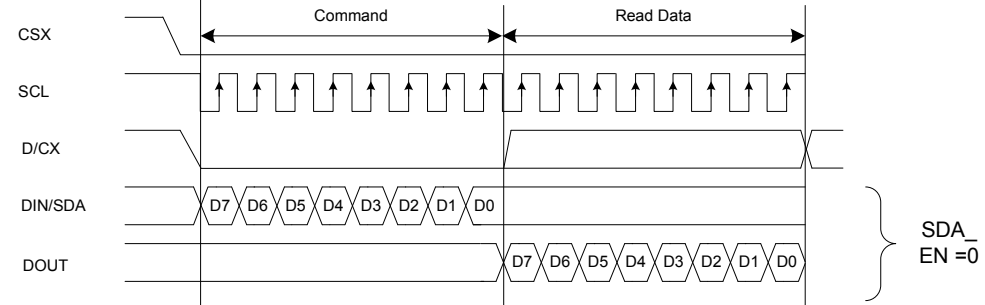
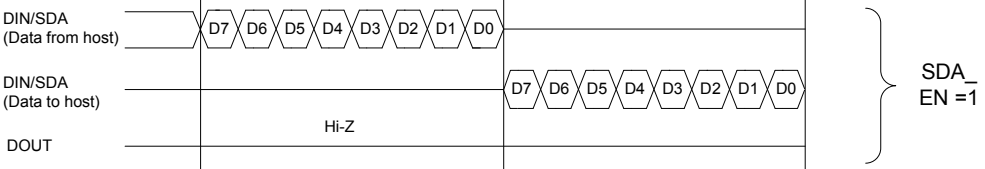
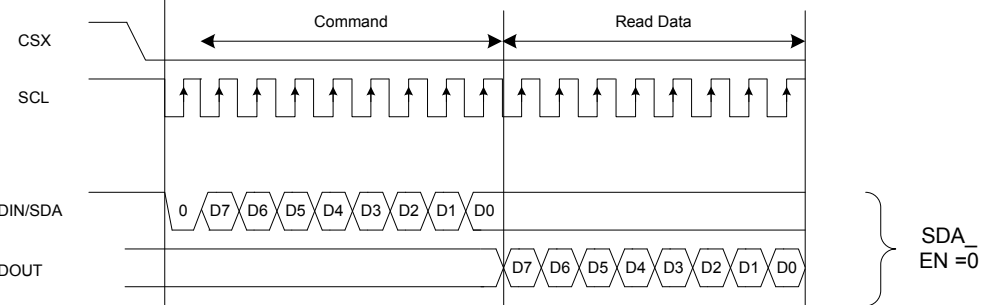
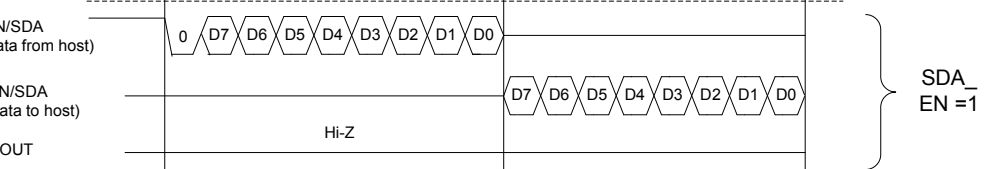
8.2.48. Read ID2 (DBh)

DBh	RDID2 (Read ID2)																								
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XXXXXXXX	1	1	0	1	1	0	1	1	DBh												
1 st parameter	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX												
2 nd arameter	1	↑	1	XXXXXXXX	1	ID2[6:0]							XX												
Description	<p>This read byte is used to track the LCD module/driver version. It is defined by display supplier (with User's agreement) and changes each time a revision is made to the display, material or construction specifications.</p> <p>The 1st parameter is dummy data.</p> <p>The 2nd parameter is LCD module/driver version ID and the ID parameter range is from 80h to FFh.</p> <p>The ID2 can be programmed by OTP function.</p> <p>X = Don't care</p>																								
Restriction	<p>ILI9486L is sending 2nd parameter value on the data lines if the MCU wants to read more than one parameter (= more than 2 RDX cycle) on parallel MCU interface.</p> <p>Only 2nd parameter is sent on DSI (The 1st parameter is not sent).</p>																								
Register Availability	<table><thead><tr><th>Status</th><th>Availability</th></tr></thead><tbody><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></tbody></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><thead><tr><th>Status</th><th>Default Value (Before OTP program)</th><th>Default Value (After OTP program)</th></tr></thead><tbody><tr><td>Power On Sequence</td><td>80h</td><td>OTP value</td></tr><tr><td>SW Reset</td><td>80h</td><td>OTP value</td></tr><tr><td>HW Reset</td><td>80h</td><td>OTP value</td></tr></tbody></table>													Status	Default Value (Before OTP program)	Default Value (After OTP program)	Power On Sequence	80h	OTP value	SW Reset	80h	OTP value	HW Reset	80h	OTP value
Status	Default Value (Before OTP program)	Default Value (After OTP program)																							
Power On Sequence	80h	OTP value																							
SW Reset	80h	OTP value																							
HW Reset	80h	OTP value																							
Flow Chart	<div><div><div>RDID2(DBh)</div><div>↓</div><div>1st Parameter: Dummy Read</div><div>↓</div><div>2nd Parameter: Send ID2[7:0]</div></div><div>Host Driver</div><div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div></div>																								

8.2.49. Read ID3 (DCh)

DCh	RDID3 (Read ID3)																								
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XXXXXXXX	1	1	0	1	1	1	0	0	DCh												
1 st parameter	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX												
2 nd parameter	1	↑	1	XXXXXXXX	ID3[7:0]							XX													
Description	<p>This read byte identifies the LCD module/driver and It is specified by User.</p> <p>The 1st parameter is dummy data.</p> <p>The 2nd parameter is LCD module/driver ID.</p> <p>The ID3 can be programmed by OTP function.</p> <p>X = Don't care</p>																								
Restriction	<p>ILI9486L is sending 2nd parameter value on the data lines if the MCU wants to read more than one parameter (= more than 2 RDX cycle) on parallel MCU interface.</p> <p>Only 2nd parameter is sent on DSI (The 1st parameter is not sent).</p>																								
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><tr><th>Status</th><th>Default Value (Before OTP program)</th><th>Default Value (After OTP program)</th></tr><tr><td>Power On Sequence</td><td>00h</td><td>OTP value</td></tr><tr><td>SW Reset</td><td>00h</td><td>OTP value</td></tr><tr><td>HW Reset</td><td>00h</td><td>OTP value</td></tr></table>													Status	Default Value (Before OTP program)	Default Value (After OTP program)	Power On Sequence	00h	OTP value	SW Reset	00h	OTP value	HW Reset	00h	OTP value
Status	Default Value (Before OTP program)	Default Value (After OTP program)																							
Power On Sequence	00h	OTP value																							
SW Reset	00h	OTP value																							
HW Reset	00h	OTP value																							
Flow Chart	<div><div><div>RDID3(DCh)</div><div>↓</div><div>1st Parameter: Dummy Read</div><div>↓</div><div>2nd Parameter: Send ID3[7:0]</div></div><div>Host Driver</div><div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div></div>																								

8.2.50. Interface Mode Control (B0h)

B0h	IFMODE (Interface Mode Control)												
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	1	0	1	1	0	0	0	0	B0h
1 st Parameter	1	1	↑	XXXXXXXX	SDA_EN	0	0	0	VSPL	HSPL	DPL	EPL	XX
Description	Sets the operation status of the display interface. The setting becomes effective as soon as the command is received.												
	EPL : DE polarity ("0"= High enable for RGB interface, "1"=Low enable for RGB interface)												
	DPL : PCLK polarity set ("0"=data fetched at the rising time, "1"=data fetched at the falling time)												
	HSPL : HSYNC polarity ("0"=Low level sync clock, "1"=High level sync clock)												
	VSPL : VSYNC polarity ("0"= Low level sync clock, "1"= High level sync clock)												
	SDA_EN : 3/4 wire serial interface selection												
	SDA_EN = "0", DIN and DOUT pins are used for 3/4 wire serial interface.												
	SDA_EN = "1", DIN/SDA pin is used for 3/4 wire serial interface and DOUT pin is not used.												
													
													
													
													
Restriction													

Register Availability	<table><tr><th>Status</th><th colspan="5">Availability</th></tr><tr><td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td><td colspan="5">Yes</td></tr><tr><td>Normal Mode ON, Idle Mode ON, Sleep OUT</td><td colspan="5">Yes</td></tr><tr><td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td><td colspan="5">Yes</td></tr><tr><td>Partial Mode ON, Idle Mode ON, Sleep OUT</td><td colspan="5">Yes</td></tr><tr><td>Sleep IN</td><td colspan="5">Yes</td></tr></table>						Status	Availability					Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes					Normal Mode ON, Idle Mode ON, Sleep OUT	Yes					Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes					Partial Mode ON, Idle Mode ON, Sleep OUT	Yes					Sleep IN	Yes				
	Status	Availability																																								
	Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes																																								
	Normal Mode ON, Idle Mode ON, Sleep OUT	Yes																																								
	Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes																																								
	Partial Mode ON, Idle Mode ON, Sleep OUT	Yes																																								
Sleep IN	Yes																																									
Default	<table><tr><th rowspan="2">Status</th><th colspan="5">Default Value</th></tr><tr><th>SDA_EN</th><th>EPL</th><th>DPL</th><th>HSPL</th><th>VSPL</th></tr><tr><td>Power ON Sequence</td><td>0b</td><td>0b</td><td>0b</td><td>0b</td><td>0b</td></tr><tr><td>H/W Reset</td><td>0b</td><td>0b</td><td>0b</td><td>0b</td><td>0b</td></tr></table>						Status	Default Value					SDA_EN	EPL	DPL	HSPL	VSPL	Power ON Sequence	0b	0b	0b	0b	0b	H/W Reset	0b	0b	0b	0b	0b													
	Status	Default Value																																								
		SDA_EN	EPL	DPL	HSPL	VSPL																																				
	Power ON Sequence	0b	0b	0b	0b	0b																																				
H/W Reset	0b	0b	0b	0b	0b																																					

8.2.51. Frame Rate Control (In Normal Mode/Full Colors) (B1h)

B1h	FRMCTR1 (Frame Rate Control (In Normal Mode / Full colors))																																																																																																	
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																																																					
Command	0	1	↑	XXXXXXXX	1	0	1	1	0	0	0	1	B1h																																																																																					
1 st Parameter	1	1	↑	XXXXXXXX	FRS[3:0]				0	0	DIVA[1:0]		XX																																																																																					
2 nd parameter	1	1	↑	XXXXXXXX	0	0	0	RTNA[4:0]					XX																																																																																					
Description	FRS[3:0]: Sets the frame frequency of full color normal mode.																																																																																																	
	<table><tr><th colspan="4">FRS[3:0]</th><th>Frame rate(Hz)</th></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>28</td></tr><tr><td>0</td><td>0</td><td>0</td><td>1</td><td>30</td></tr><tr><td>0</td><td>0</td><td>1</td><td>0</td><td>32</td></tr><tr><td>0</td><td>0</td><td>1</td><td>1</td><td>34</td></tr><tr><td>0</td><td>1</td><td>0</td><td>0</td><td>36</td></tr><tr><td>0</td><td>1</td><td>0</td><td>1</td><td>39</td></tr><tr><td>0</td><td>1</td><td>1</td><td>0</td><td>42</td></tr><tr><td>0</td><td>1</td><td>1</td><td>1</td><td>46</td></tr><tr><td>1</td><td>0</td><td>0</td><td>0</td><td>50</td></tr><tr><td>1</td><td>0</td><td>0</td><td>1</td><td>56</td></tr><tr><td>1</td><td>0</td><td>1</td><td>0</td><td>62</td></tr><tr><td>1</td><td>0</td><td>1</td><td>1</td><td>70</td></tr><tr><td>1</td><td>1</td><td>0</td><td>0</td><td>81</td></tr><tr><td>1</td><td>1</td><td>0</td><td>1</td><td>96</td></tr><tr><td>1</td><td>1</td><td>1</td><td>0</td><td>117</td></tr><tr><td>1</td><td>1</td><td>1</td><td>1</td><td>117</td></tr></table>													FRS[3:0]				Frame rate(Hz)	0	0	0	0	28	0	0	0	1	30	0	0	1	0	32	0	0	1	1	34	0	1	0	0	36	0	1	0	1	39	0	1	1	0	42	0	1	1	1	46	1	0	0	0	50	1	0	0	1	56	1	0	1	0	62	1	0	1	1	70	1	1	0	0	81	1	1	0	1	96	1	1	1	0	117	1	1	1	1	117
	FRS[3:0]				Frame rate(Hz)																																																																																													
	0	0	0	0	28																																																																																													
	0	0	0	1	30																																																																																													
	0	0	1	0	32																																																																																													
	0	0	1	1	34																																																																																													
	0	1	0	0	36																																																																																													
	0	1	0	1	39																																																																																													
	0	1	1	0	42																																																																																													
	0	1	1	1	46																																																																																													
	1	0	0	0	50																																																																																													
	1	0	0	1	56																																																																																													
	1	0	1	0	62																																																																																													
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	<table><tr><th colspan="2">DIVA[1:0]</th><th>Division Ratio</th></tr><tr><td>0</td><td>0</td><td>fosc</td></tr><tr><td>0</td><td>1</td><td>fosc / 2</td></tr><tr><td>1</td><td>0</td><td>fosc / 4</td></tr><tr><td>1</td><td>1</td><td>fosc / 8</td></tr></table>													DIVA[1:0]		Division Ratio	0	0	fosc	0	1	fosc / 2	1	0	fosc / 4	1	1	fosc / 8																																																																						
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0	1	0	1	0	Setting prohibited	1	0	1	0	1	21 clocks					
Restriction																
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr><tr><td>Normal Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr><tr><td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr><tr><td>Partial Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr><tr><td>Sleep IN</td><td>Yes</td></tr></table>	Status	Availability	Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes	Normal Mode ON, Idle Mode ON, Sleep OUT	Yes	Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes	Partial Mode ON, Idle Mode ON, Sleep OUT	Yes	Sleep IN	Yes			
Status	Availability															
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes															
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes															
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes															
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes															
Sleep IN	Yes															
Default	<table><tr><th rowspan="2">Status</th><th colspan="3">Default Value</th></tr><tr><th>FRS [3:0]</th><th>DIVA[1:0]</th><th>RTNA[4:0]</th></tr><tr><td>Power ON Sequence</td><td>4'b1011</td><td>2'b00</td><td>5'b10001</td></tr><tr><td>H/W Reset</td><td>4'b1011</td><td>2'b00</td><td>5'b10001</td></tr></table>	Status	Default Value			FRS [3:0]	DIVA[1:0]	RTNA[4:0]	Power ON Sequence	4'b1011	2'b00	5'b10001	H/W Reset	4'b1011	2'b00	5'b10001
Status	Default Value															
	FRS [3:0]	DIVA[1:0]	RTNA[4:0]													
Power ON Sequence	4'b1011	2'b00	5'b10001													
H/W Reset	4'b1011	2'b00	5'b10001													

8.2.52. Frame Rate Control (In Idle Mode/8 colors) (B2h)

B2h				FRMCTR2 (Frame Rate Control (In Idle Mode / 8 colors))																																																																																	
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																																								
Command	0	1	↑	XXXXXXXX	1	0	1	1	0	0	1	0	B2h																																																																								
1 st Parameter	1	1	↑	XXXXXXXX	0	0	0	0	0	0	DIVB[1:0]		XX																																																																								
2 nd parameter	1	1	↑	XXXXXXXX	0	0	0	RTNB[4:0]					XX																																																																								
Description	Sets the division ratio for internal clocks of Idle mode at CPU interface.																																																																																				
	DIVB [1:0] : division ratio for internal clocks when Idle mode.																																																																																				
	<table><tr><th colspan="2">DIVB[1:0]</th><th>Division Ratio</th></tr><tr><td>0</td><td>0</td><td>fosc</td></tr><tr><td>0</td><td>1</td><td>fosc / 2</td></tr><tr><td>1</td><td>0</td><td>fosc / 4</td></tr><tr><td>1</td><td>1</td><td>fosc / 8</td></tr></table>													DIVB[1:0]		Division Ratio	0	0	fosc	0	1	fosc / 2	1	0	fosc / 4	1	1	fosc / 8																																																									
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	RTNB[4:0]					Clock per Line																																																																															
	0	0	0	0	0	Setting prohibited																																																																															
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<table><tr><th colspan="5">RTNB[4:0]</th><th>Clock per Line</th></tr><tr><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>Setting prohibited</td></tr><tr><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>Setting prohibited</td></tr><tr><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>Setting prohibited</td></tr><tr><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>Setting prohibited</td></tr><tr><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>Setting prohibited</td></tr><tr><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>16 clocks</td></tr><tr><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>17 clocks</td></tr><tr><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>18 clocks</td></tr><tr><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>19 clocks</td></tr><tr><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>20 clocks</td></tr><tr><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>21 clocks</td></tr></table>													RTNB[4:0]					Clock per Line	0	1	0	1	1	Setting prohibited	0	1	1	0	0	Setting prohibited	0	1	1	0	1	Setting prohibited	0	1	1	1	0	Setting prohibited	0	1	1	1	1	Setting prohibited	1	0	0	0	0	16 clocks	1	0	0	0	1	17 clocks	1	0	0	1	0	18 clocks	1	0	0	1	1	19 clocks	1	0	1	0	0	20 clocks	1	0	1	0	1	21 clocks	
RTNB[4:0]					Clock per Line																																																																																
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<table><tr><th colspan="5">RTNB[4:0]</th><th>Clock per Line</th></tr><tr><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>22 clocks</td></tr><tr><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>23 clocks</td></tr><tr><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>24 clocks</td></tr><tr><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>25 clocks</td></tr><tr><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>26 clocks</td></tr><tr><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>27 clocks</td></tr><tr><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>28 clocks</td></tr><tr><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>29 clocks</td></tr><tr><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>30 clocks</td></tr><tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>31 clocks</td></tr></table>													RTNB[4:0]					Clock per Line	1	0	1	1	0	22 clocks	1	0	1	1	1	23 clocks	1	0	0	0	0	24 clocks	1	0	0	0	1	25 clocks	1	0	0	1	0	26 clocks	1	0	1	1	1	27 clocks	1	1	0	0	0	28 clocks	1	1	0	0	1	29 clocks	1	1	0	1	0	30 clocks	1	1	1	1	1	31 clocks							
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Restriction																																																																																					
Register Availability	<table><tr><th colspan="2">Status</th><th>Availability</th></tr><tr><td colspan="2">Normal Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr><tr><td colspan="2">Normal Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr><tr><td colspan="2">Partial Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr><tr><td colspan="2">Partial Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr><tr><td colspan="2">Sleep IN</td><td>Yes</td></tr></table>													Status		Availability	Normal Mode ON, Idle Mode OFF, Sleep OUT		Yes	Normal Mode ON, Idle Mode ON, Sleep OUT		Yes	Partial Mode ON, Idle Mode OFF, Sleep OUT		Yes	Partial Mode ON, Idle Mode ON, Sleep OUT		Yes	Sleep IN		Yes																																																						
Status		Availability																																																																																			
Normal Mode ON, Idle Mode OFF, Sleep OUT		Yes																																																																																			
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Sleep IN		Yes																																																																																			
Default	<table><tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr><tr><th>DIVB[1:0]</th><th>RTNB[4:0]</th></tr><tr><td>Power ON Sequence</td><td>2'b00</td><td>5'b10001</td></tr><tr><td>H/W Reset</td><td>2'b00</td><td>5'b10001</td></tr></table>													Status	Default Value		DIVB[1:0]	RTNB[4:0]	Power ON Sequence	2'b00	5'b10001	H/W Reset	2'b00	5'b10001																																																													
Status	Default Value																																																																																				
	DIVB[1:0]	RTNB[4:0]																																																																																			
Power ON Sequence	2'b00	5'b10001																																																																																			
H/W Reset	2'b00	5'b10001																																																																																			

8.2.53. Frame Rate control (In Partial Mode/Full Colors) (B3h)

_B3h				FRMCTR3 (Frame Rate Control (In Partial Mode / Full colors))																																																																																	
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																																								
Command	0	1	↑	XXXXXXXX	1	0	1	1	0	0	1	1	B3h																																																																								
1 st Parameter	1	1	↑	XXXXXXXX	0	0	0	0	0	0	DIVC[1:0]		XX																																																																								
2 nd parameter	1	1	↑	XXXXXXXX	0	0	0	RTNC[4:0]					XX																																																																								
Description	Sets the division ratio for internal clocks of Partial mode (Idle mode off) at CPU interface.																																																																																				
	DIVC [1:0] : division ratio for internal clocks when Partial mode.																																																																																				
	<table><tr><th colspan="2">DIVC[1:0]</th><th>Division Ratio</th></tr><tr><td>0</td><td>0</td><td>fosc</td></tr><tr><td>0</td><td>1</td><td>fosc / 2</td></tr><tr><td>1</td><td>0</td><td>fosc / 4</td></tr><tr><td>1</td><td>1</td><td>fosc / 8</td></tr></table>													DIVC[1:0]		Division Ratio	0	0	fosc	0	1	fosc / 2	1	0	fosc / 4	1	1	fosc / 8																																																									
	DIVC[1:0]		Division Ratio																																																																																		
	0	0	fosc																																																																																		
	0	1	fosc / 2																																																																																		
	1	0	fosc / 4																																																																																		
	1	1	fosc / 8																																																																																		
	RTNC [4:0] : RTNC[4:0] is used to set 1H (line) period of Partial mode at CPU interface.																																																																																				
	<table><tr><th colspan="5">RTNC[4:0]</th><th>Clock per Line</th></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>Setting prohibited</td></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>Setting prohibited</td></tr><tr><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>Setting prohibited</td></tr><tr><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>Setting prohibited</td></tr><tr><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>Setting prohibited</td></tr><tr><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>Setting prohibited</td></tr><tr><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>Setting prohibited</td></tr><tr><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>Setting prohibited</td></tr><tr><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>Setting prohibited</td></tr><tr><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>Setting prohibited</td></tr><tr><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>Setting prohibited</td></tr></table>													RTNC[4:0]					Clock per Line	0	0	0	0	0	Setting prohibited	0	0	0	0	1	Setting prohibited	0	0	0	1	0	Setting prohibited	0	0	0	1	1	Setting prohibited	0	0	1	0	0	Setting prohibited	0	0	1	0	1	Setting prohibited	0	0	1	1	0	Setting prohibited	0	0	1	1	1	Setting prohibited	0	1	0	0	0	Setting prohibited	0	1	0	0	1	Setting prohibited	0	1	0	1	0	Setting prohibited
	RTNC[4:0]					Clock per Line																																																																															
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<table><tr><th colspan="5">RTNC[4:0]</th><th>Clock per Line</th></tr><tr><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>Setting prohibited</td></tr><tr><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>Setting prohibited</td></tr><tr><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>Setting prohibited</td></tr><tr><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>Setting prohibited</td></tr><tr><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>Setting prohibited</td></tr><tr><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>16 clocks</td></tr><tr><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>17 clocks</td></tr><tr><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>18 clocks</td></tr><tr><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>19 clocks</td></tr><tr><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>20 clocks</td></tr><tr><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>21 clocks</td></tr></table>													RTNC[4:0]					Clock per Line	0	1	0	1	1	Setting prohibited	0	1	1	0	0	Setting prohibited	0	1	1	0	1	Setting prohibited	0	1	1	1	0	Setting prohibited	0	1	1	1	1	Setting prohibited	1	0	0	0	0	16 clocks	1	0	0	0	1	17 clocks	1	0	0	1	0	18 clocks	1	0	0	1	1	19 clocks	1	0	1	0	0	20 clocks	1	0	1	0	1	21 clocks	
RTNC[4:0]					Clock per Line																																																																																
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1	0	1	0	0	20 clocks																																																																																
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Default	<table><tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr><tr><th>DIVC[1:0]</th><th>RTNC[4:0]</th></tr><tr><td>Power ON Sequence</td><td>2'b00</td><td>5'b10001</td></tr><tr><td>H/W Reset</td><td>2'b00</td><td>5'b10001</td></tr></table>													Status	Default Value		DIVC[1:0]	RTNC[4:0]	Power ON Sequence	2'b00	5'b10001	H/W Reset	2'b00	5'b10001																																																													
Status	Default Value																																																																																				
	DIVC[1:0]	RTNC[4:0]																																																																																			
Power ON Sequence	2'b00	5'b10001																																																																																			
H/W Reset	2'b00	5'b10001																																																																																			

8.2.54. Display Inversion Control (B4h)

_B4h				INVTR (Display Inversion Control)																																																																																																																																																																																																																																									
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																																																																																																																																																																																																
Command	0	1	↑	XXXXXXXX	1	0	1	1	0	1	0	0	B4h																																																																																																																																																																																																																																
1 st Parameter	1	1	↑	XXXXXXXX	0	0	0	ZINV	0	0	DINV[1:0]		XX																																																																																																																																																																																																																																
Description	ZINV : Set Z-inversion mode 0 : Disable Z-inversion 1 : Enable Z-inversion mode DINV[1:0] : Set the inversion mode																																																																																																																																																																																																																																												
	<table><tr><th>DINV [1:0]</th><th colspan="12">Dot inversion mode</th></tr><tr><td rowspan="5">2'b00</td><td rowspan="5">Column inversion</td><td colspan="6">1st frame</td><td colspan="6">2nd frame</td></tr><tr><td>1 line</td><td>+</td><td>-</td><td>+</td><td>-</td><td>+</td><td>-</td><td>1 line</td><td>-</td><td>+</td><td>-</td><td>+</td><td>-</td></tr><tr><td>2 line</td><td>+</td><td>-</td><td>+</td><td>-</td><td>+</td><td>-</td><td>2 line</td><td>-</td><td>+</td><td>-</td><td>+</td><td>-</td></tr><tr><td>3 line</td><td>+</td><td>-</td><td>+</td><td>-</td><td>+</td><td>-</td><td>3 line</td><td>-</td><td>+</td><td>-</td><td>+</td><td>-</td></tr><tr><td>4 line</td><td>+</td><td>-</td><td>+</td><td>-</td><td>+</td><td>-</td><td>4 line</td><td>-</td><td>+</td><td>-</td><td>+</td><td>-</td></tr><tr><td>2'b01</td><td colspan="12">Setting prohibited</td></tr><tr><td rowspan="5">2'b10</td><td rowspan="5">2-dot inversion</td><td colspan="6">1st frame</td><td colspan="6">2nd frame</td></tr><tr><td>1 line</td><td>+</td><td>-</td><td>+</td><td>-</td><td>+</td><td>-</td><td>1 line</td><td>-</td><td>+</td><td>-</td><td>+</td><td>-</td></tr><tr><td>2 line</td><td>+</td><td>-</td><td>+</td><td>-</td><td>+</td><td>-</td><td>2 line</td><td>-</td><td>+</td><td>-</td><td>+</td><td>-</td></tr><tr><td>3 line</td><td>-</td><td>+</td><td>-</td><td>+</td><td>-</td><td>+</td><td>3 line</td><td>+</td><td>-</td><td>+</td><td>-</td><td>+</td></tr><tr><td>4 line</td><td>-</td><td>+</td><td>-</td><td>+</td><td>-</td><td>+</td><td>4 line</td><td>+</td><td>-</td><td>+</td><td>-</td><td>+</td></tr><tr><td rowspan="5">2'b11</td><td rowspan="5">4-dot inversion</td><td colspan="6">1st frame</td><td colspan="6">2nd frame</td></tr><tr><td>1 line</td><td>+</td><td>-</td><td>+</td><td>-</td><td>+</td><td>-</td><td>1 line</td><td>-</td><td>+</td><td>-</td><td>+</td><td>-</td></tr><tr><td>2 line</td><td>+</td><td>-</td><td>+</td><td>-</td><td>+</td><td>-</td><td>2 line</td><td>-</td><td>+</td><td>-</td><td>+</td><td>-</td></tr><tr><td>3 line</td><td>+</td><td>-</td><td>+</td><td>-</td><td>+</td><td>-</td><td>3 line</td><td>-</td><td>+</td><td>-</td><td>+</td><td>-</td></tr><tr><td>4 line</td><td>+</td><td>-</td><td>+</td><td>-</td><td>+</td><td>-</td><td>4 line</td><td>-</td><td>+</td><td>-</td><td>+</td><td>-</td></tr></table>													DINV [1:0]	Dot inversion mode												2'b00	Column inversion	1st frame						2nd frame						1 line	+	-	+	-	+	-	1 line	-	+	-	+	-	2 line	+	-	+	-	+	-	2 line	-	+	-	+	-	3 line	+	-	+	-	+	-	3 line	-	+	-	+	-	4 line	+	-	+	-	+	-	4 line	-	+	-	+	-	2'b01	Setting prohibited												2'b10	2-dot inversion	1st frame						2nd frame						1 line	+	-	+	-	+	-	1 line	-	+	-	+	-	2 line	+	-	+	-	+	-	2 line	-	+	-	+	-	3 line	-	+	-	+	-	+	3 line	+	-	+	-	+	4 line	-	+	-	+	-	+	4 line	+	-	+	-	+	2'b11	4-dot inversion	1st frame						2nd frame						1 line	+	-	+	-	+	-	1 line	-	+	-	+	-	2 line	+	-	+	-	+	-	2 line	-	+	-	+	-	3 line	+	-	+	-	+	-	3 line	-	+	-	+	-	4 line	+	-	+	-	+	-	4 line	-	+	-	+	-
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Default	<table><tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr><tr><th>ZINV</th><th>DINV[1:0]</th></tr><tr><td>Power ON Sequence</td><td>1'b0</td><td>2'b00</td></tr><tr><td>H/W Reset</td><td>1'b0</td><td>2'b00</td></tr></table>													Status	Default Value		ZINV	DINV[1:0]	Power ON Sequence	1'b0	2'b00	H/W Reset	1'b0	2'b00																																																																																																																																																																																																																					
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H/W Reset	1'b0	2'b00																																																																																																																																																																																																																																											

8.2.55. Blanking Porch Control (B5h)

_B5h		PRCTR (Blanking Porch)																																																		
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																							
Command	0	1	↑	XXXXXXXX	1	0	1	1	0	1	0	1	B5h																																							
1 st parameter	1	1	↑	XXXXXXXX	VFP[7:0]								XX																																							
2 nd parameter	1	1	↑	XXXXXXXX	VBP[7:0]								XX																																							
3 rd parameter	1	1	↑	XXXXXXXX	0	0	0	HFP[4:0]						XX																																						
4 nd parameter	1	1	↑	XXXXXXXX	HBP[7:0]								XX																																							
Description	VFP [7:0] / VBP [7:0]: The FP [7:0] and BP [7:0] bits specify the line number of vertical front and back porch period respectively.																																																			
	<table><tr><th>FP[7:0]</th><th>Number of lines of front porch</th></tr><tr><td>00000000</td><td>Setting prohibited</td></tr><tr><td>00000001</td><td>Setting prohibited</td></tr><tr><td>00000010</td><td>2</td></tr><tr><td>00000011</td><td>3</td></tr><tr><td>:</td><td>:</td></tr><tr><td>:</td><td>:</td></tr><tr><td>11111100</td><td>252</td></tr><tr><td>11111101</td><td>253</td></tr><tr><td>11111110</td><td>254</td></tr><tr><td>11111111</td><td>255</td></tr></table>				FP[7:0]	Number of lines of front porch	00000000	Setting prohibited	00000001	Setting prohibited	00000010	2	00000011	3	:	:	:	:	11111100	252	11111101	253	11111110	254	11111111	255	<table><tr><th>BP[7:0]</th><th>Number of lines of back porch</th></tr><tr><td>00000000</td><td>Setting prohibited</td></tr><tr><td>00000001</td><td>Setting prohibited</td></tr><tr><td>00000010</td><td>2</td></tr><tr><td>00000011</td><td>3</td></tr><tr><td>:</td><td>:</td></tr><tr><td>:</td><td>:</td></tr><tr><td>11111100</td><td>252</td></tr><tr><td>11111101</td><td>253</td></tr><tr><td>11111110</td><td>254</td></tr><tr><td>11111111</td><td>254</td></tr></table>				BP[7:0]	Number of lines of back porch	00000000	Setting prohibited	00000001	Setting prohibited	00000010	2	00000011	3	:	:	:	:	11111100	252	11111101	253	11111110	254	11111111	254
	FP[7:0]	Number of lines of front porch																																																		
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	00000010	2																																																		
	00000011	3																																																		
	:	:																																																		
	:	:																																																		
	11111100	252																																																		
11111101	253																																																			
11111110	254																																																			
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11111100	252																																																			
11111101	253																																																			
11111110	254																																																			
11111111	254																																																			
HFP [4:0]: The HFP [4:0] bits specify the dotclk number of horizontal front porch period.																																																				
<table><tr><th>HFP[4:0]</th><th>Number of dotclk of front porch</th></tr><tr><td>00000</td><td>Setting prohibited</td></tr><tr><td>00001</td><td>Setting prohibited</td></tr><tr><td>00010</td><td>2</td></tr><tr><td>00011</td><td>3</td></tr><tr><td>:</td><td>:</td></tr><tr><td>:</td><td>:</td></tr><tr><td>11100</td><td>28</td></tr><tr><td>11101</td><td>29</td></tr><tr><td>11110</td><td>30</td></tr><tr><td>11111</td><td>31</td></tr></table>													HFP[4:0]	Number of dotclk of front porch	00000	Setting prohibited	00001	Setting prohibited	00010	2	00011	3	:	:	:	:	11100	28	11101	29	11110	30	11111	31																		
HFP[4:0]	Number of dotclk of front porch																																																			
00000	Setting prohibited																																																			
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00010	2																																																			
00011	3																																																			
:	:																																																			
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<table><tr><th>HBP[7:0]</th><th>Number of dotclk of front porch</th></tr><tr><td>00000000</td><td>Setting prohibited</td></tr><tr><td>00000001</td><td>Setting prohibited</td></tr><tr><td>00000010</td><td>2</td></tr><tr><td>00000011</td><td>3</td></tr><tr><td>:</td><td>:</td></tr><tr><td>:</td><td>:</td></tr><tr><td>11111100</td><td>252</td></tr><tr><td>11111101</td><td>253</td></tr><tr><td>11111110</td><td>254</td></tr><tr><td>11111111</td><td>255</td></tr></table>													HBP[7:0]	Number of dotclk of front porch	00000000	Setting prohibited	00000001	Setting prohibited	00000010	2	00000011	3	:	:	:	:	11111100	252	11111101	253	11111110	254	11111111	255																		
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11111100	252																																																			
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11111110	254																																																			
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Register Availability	<table><tr><td colspan="3">Status</td><td>Availability</td></tr><tr><td colspan="3">Normal Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr><tr><td colspan="3">Normal Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr><tr><td colspan="3">Partial Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr><tr><td colspan="3">Partial Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr><tr><td colspan="3">Sleep IN</td><td>Yes</td></tr></table>				Status			Availability	Normal Mode ON, Idle Mode OFF, Sleep OUT			Yes	Normal Mode ON, Idle Mode ON, Sleep OUT			Yes	Partial Mode ON, Idle Mode OFF, Sleep OUT			Yes	Partial Mode ON, Idle Mode ON, Sleep OUT			Yes	Sleep IN			Yes
	Status			Availability																								
	Normal Mode ON, Idle Mode OFF, Sleep OUT			Yes																								
	Normal Mode ON, Idle Mode ON, Sleep OUT			Yes																								
	Partial Mode ON, Idle Mode OFF, Sleep OUT			Yes																								
	Partial Mode ON, Idle Mode ON, Sleep OUT			Yes																								
Sleep IN			Yes																									
Default	Status	Default Value																										
		VFP[7:0]	VBP[7:0]	HFP[4:0]	HBP[7:0]																							
		Power ON Sequence	8'b00000010	8'b00000010	8'b00001010	8'b00000100																						
		H/W Reset	8'b00000010	8'b00000010	8'b00001010	8'b00000100																						

8.2.56. Display Function Control (B6h)

B6h	DISCTRL (Display Function Control)																															
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX																			
Command	0	1	↑	XXXXXXXX	1	0	1	1	0	1	1	0	B6h																			
1 st parameter	1	1	↑	XXXXXXXX	BYPASS	RCM	RM	DM	PTG[1:0]		PT[1:0]		XX																			
2 nd parameter	1	1	↑	XXXXXXXX	0	GS	SS	SM	ISC[3:0]				XX																			
3 rd Parameter	1	1	↑	XXXXXXXX	0	0	NL[5:0]						XX																			
Description	DM: Select the display operation mode.																															
	<table><tr><th>DM</th><th>Interface Mode</th></tr><tr><td>0</td><td>Internal system clock</td></tr><tr><td>1</td><td>RGB interface</td></tr></table>													DM	Interface Mode	0	Internal system clock	1	RGB interface													
	DM	Interface Mode																														
	0	Internal system clock																														
	1	RGB interface																														
	RM: Select the interface to access the GRAM. When RM='0', the driver will write display data to GRAM via system interface and the driver will write display data to GRAM via RGB interface when RM='1'.																															
	<table><tr><th>RM</th><th>Interface for RAM access</th></tr><tr><td>0</td><td>System interface</td></tr><tr><td>1</td><td>RGB interface</td></tr></table>													RM	Interface for RAM access	0	System interface	1	RGB interface													
	RM	Interface for RAM access																														
	0	System interface																														
	1	RGB interface																														
	RCM: RGB interface selection (refer to the RGB interface section).																															
	<table><tr><th>RCM</th><th>RGB transfer mode</th></tr><tr><td>0</td><td>DE Mode</td></tr><tr><td>1</td><td>SYNC Mode</td></tr></table>													RCM	RGB transfer mode	0	DE Mode	1	SYNC Mode													
	RCM	RGB transfer mode																														
	0	DE Mode																														
1	SYNC Mode																															
BYPASS: Select the display data path whether memory or direct to shift register when RGB interface is used.																																
<table><tr><th>BYPASS</th><th>Display data path</th></tr><tr><td>0</td><td>Memory</td></tr><tr><td>1</td><td>Direct to shift register</td></tr></table>													BYPASS	Display data path	0	Memory	1	Direct to shift register														
BYPASS	Display data path																															
0	Memory																															
1	Direct to shift register																															
Note: RGB input signal, when set to bypass mode the Hsync low ≥ 3, HBP ≥ 3, HFP ≥ 10.																																
PTG [1:0]: Set the scan mode in non-display area.																																
<table><tr><th>PTG1</th><th>PTG0</th><th>Gate outputs in non-display area</th><th>Source outputs in non-display area</th></tr><tr><td>0</td><td>0</td><td>Normal scan</td><td>Set with the PT[2:0] bits</td></tr><tr><td>0</td><td>1</td><td>Setting prohibited</td><td>---</td></tr><tr><td>1</td><td>0</td><td>Interval scan</td><td>Set with the PT[2:0] bits</td></tr><tr><td>1</td><td>1</td><td>Setting prohibited</td><td>---</td></tr></table>													PTG1	PTG0	Gate outputs in non-display area	Source outputs in non-display area	0	0	Normal scan	Set with the PT[2:0] bits	0	1	Setting prohibited	---	1	0	Interval scan	Set with the PT[2:0] bits	1	1	Setting prohibited	---
PTG1	PTG0	Gate outputs in non-display area	Source outputs in non-display area																													
0	0	Normal scan	Set with the PT[2:0] bits																													
0	1	Setting prohibited	---																													
1	0	Interval scan	Set with the PT[2:0] bits																													
1	1	Setting prohibited	---																													
PT [1:0]: Determine source/VCOM output in a non-display area in the partial display mode.																																
<table><tr><th colspan="2">PT[1:0]</th><th>Source output on non-display area</th></tr><tr><td>0</td><td>0</td><td>V63</td></tr><tr><td>0</td><td>1</td><td>V0</td></tr><tr><td>1</td><td>0</td><td>AGND</td></tr><tr><td>1</td><td>1</td><td>Hi-Z</td></tr></table>													PT[1:0]		Source output on non-display area	0	0	V63	0	1	V0	1	0	AGND	1	1	Hi-Z					
PT[1:0]		Source output on non-display area																														
0	0	V63																														
0	1	V0																														
1	0	AGND																														
1	1	Hi-Z																														

SS: Select the shift direction of outputs from the source driver.

SS	Source Output Scan Direction
0	S1 → S960
1	S960 → S1

In addition to the shift direction, the settings for both SS and BGR bits are required to change the assignment of R, G, B dots to the source driver pins.

To assign R, G, B dots to the source driver pins from S1 to S960, set SS = 0.

To assign R, G, B dots to the source driver pins from S960 to S1, set SS = 1.

ISC[3:0]: Set the scan cycle when PTG selects interval scan in non-display area drive period. The scan cycle is defined by n frame periods, where n is an odd number from 3 to 31. The polarity of liquid crystal drive voltage from the gate driver is inverted in the same timing as the interval scan cycle.

ISC[3:0]	Scan cycle	(f _{FRAME})=60Hz
4'h0	Setting inhibited	—
4'h1	3 frames	50ms
4'h2	5 frames	84ms
4'h3	7 frames	117ms
4'h4	9 frames	150ms
4'h5	11 frames	184ms
4'h6	13 frames	217ms
4'h7	15 frames	251ms
4'h8	17 frames	284ms
4'h9	19 frames	317ms
4'hA	21 frames	351ms
4'hB	23 frames	384ms
4'hC	25 frames	418ms
4'hD	27 frames	451ms
4'hE	29 frames	484ms
4'hF	31 frames	518ms

GS: Sets the direction of scan by the gate driver.

GS	Gate Output Scan Direction
0	G1 → G480
1	G480 → G1

SM: Sets the gate driver pin arrangement in combination with the GS bit (R60h) to select the optimal scan mode for the module.

SM	GS	Scan Direction	Gate Output Sequence
0	0		G1, G2, G3, G4, ..., G476 G477, G478, G479, G480

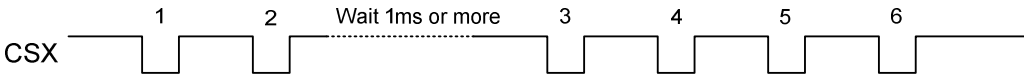

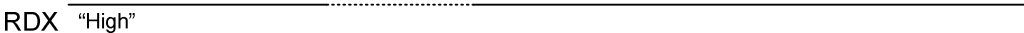

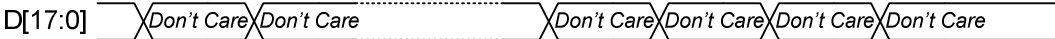
		<table><tr><td>0</td><td>1</td><td><p>Odd-number</p><p>Even-number</p><p>TFT Panel</p><p>IC</p></td><td>G480, G479, G478, ..., G9 G7, G5, G4, G3, G2, G1</td></tr><tr><td>1</td><td>0</td><td><p>Odd-number</p><p>Even-number</p><p>TFT Panel</p><p>IC</p></td><td>G1, G3, G5, G7, ...,G471 G473, G475, G477, G479 G2, G4, G6, G8, ...,G472 G474, G476, G478, G480</td></tr><tr><td>1</td><td>1</td><td><p>Odd-number</p><p>Even-number</p><p>TFT Panel</p><p>IC</p></td><td>G480, G478, G476, ...,G14 G12, G10, G8, G6, G4, G2 G479, G477, G475,...,G13 G11, G9, G7, G5, G3, G1</td></tr></table>	0	1	<p>Odd-number</p> <p>Even-number</p> <p>TFT Panel</p> <p>IC</p>	G480, G479, G478, ..., G9 G7, G5, G4, G3, G2, G1	1	0	<p>Odd-number</p> <p>Even-number</p> <p>TFT Panel</p> <p>IC</p>	G1, G3, G5, G7, ...,G471 G473, G475, G477, G479 G2, G4, G6, G8, ...,G472 G474, G476, G478, G480	1	1	<p>Odd-number</p> <p>Even-number</p> <p>TFT Panel</p> <p>IC</p>	G480, G478, G476, ...,G14 G12, G10, G8, G6, G4, G2 G479, G477, G475,...,G13 G11, G9, G7, G5, G3, G1	<p>NL [5:0]: Sets the number of lines to drive the LCD at an interval of 8 lines. The GRAM address mapping is not affected by the number of lines set by NL[5:0]. The number of lines must be the same or more than the number of lines necessary for the size of the liquid crystal panel.</p> <table><tr><th>NL[5:0]</th><th>LCD Drive Line</th></tr><tr><td>6'h00 ~ 6'h3B</td><td>8 * (NL5:0)+1) lines</td></tr><tr><td>Others</td><td>Setting inhibited</td></tr></table>	NL[5:0]	LCD Drive Line	6'h00 ~ 6'h3B	8 * (NL5:0)+1) lines	Others	Setting inhibited
0	1	<p>Odd-number</p> <p>Even-number</p> <p>TFT Panel</p> <p>IC</p>	G480, G479, G478, ..., G9 G7, G5, G4, G3, G2, G1																		
1	0	<p>Odd-number</p> <p>Even-number</p> <p>TFT Panel</p> <p>IC</p>	G1, G3, G5, G7, ...,G471 G473, G475, G477, G479 G2, G4, G6, G8, ...,G472 G474, G476, G478, G480																		
1	1	<p>Odd-number</p> <p>Even-number</p> <p>TFT Panel</p> <p>IC</p>	G480, G478, G476, ...,G14 G12, G10, G8, G6, G4, G2 G479, G477, G475,...,G13 G11, G9, G7, G5, G3, G1																		
NL[5:0]	LCD Drive Line																				
6'h00 ~ 6'h3B	8 * (NL5:0)+1) lines																				
Others	Setting inhibited																				
Restriction																					
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr><tr><td>Normal Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr><tr><td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr><tr><td>Partial Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr><tr><td>Sleep IN</td><td>Yes</td></tr></table>			Status	Availability	Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes	Normal Mode ON, Idle Mode ON, Sleep OUT	Yes	Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes	Partial Mode ON, Idle Mode ON, Sleep OUT	Yes	Sleep IN	Yes						
Status	Availability																				
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes																				
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes																				
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes																				
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes																				
Sleep IN	Yes																				

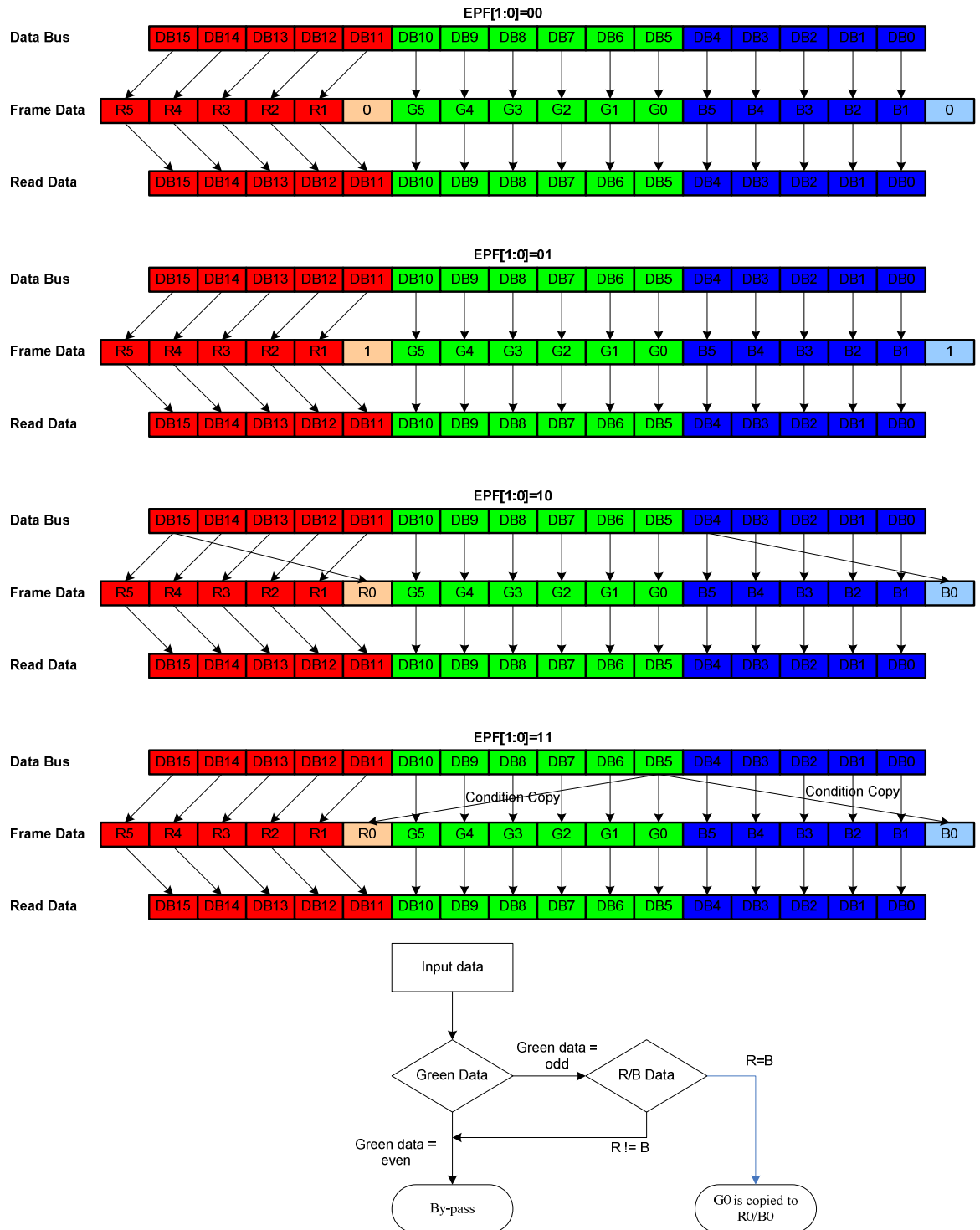
Default

Status	Default Value						
	PTG[1:0]	PT[1:0]	GS	SS	SM	ISC[3:0]	NL[5:0]
Power ON Sequence	2'b00	2'b00	1'b0	1'b0	1'b0	4'b0010	6'b111011
H/W Reset	2'b00	2'b00	1'b0	1'b0	1'b0	4'b0010	6'b111011

Status	Default Value		
	RM	DM	BYPASS
Power ON Sequence	1'b0	1'b0	1'b1
H/W Reset	1'b0	1'b0	1'b1

8.2.57. Entry Mode Set (B7h)

B7h	ETMOD (Entry Mode Set)																											
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX															
Command	0	1	↑	XXXXXXXX	1	0	1	1	0	1	1	1	B7h															
Parameter	1	1	↑	XXXXXXXX	EPF[1:0]		0	0	DSTB	GON	DTE	GAS	XX															
Description	<p>DSTB: The ILI9486L driver enters the Deep Standby Mode when DSTB is set to high (“1”). In Deep Standby mode, both internal logic power and SRAM power are turn off, the display data stored in the Frame Memory and the instructions are not saved. Rewrite Frame Memory content and instructions after the Deep Standby Mode is exited.</p> <p><i>Note: ILI9486L provides two ways to exit the Deep Standby Mode:</i></p> <p>(1) Exit Deep Standby Mode by pull down CSX to low (“0”) 6 times.</p> <p>(2) Input a RESX pulse with effective low level duration to start up the inside logic regulator and makes a transition to the initial state.</p> <div></div> <div></div> <div></div> <div></div> <div></div>																											
	<p>GAS: Low voltage detection control.</p> <table><tr><th>GAS</th><th>Low voltage detection</th></tr><tr><td>0</td><td>Enable</td></tr><tr><td>1</td><td>Disable</td></tr></table>													GAS	Low voltage detection	0	Enable	1	Disable									
	GAS	Low voltage detection																										
	0	Enable																										
	1	Disable																										
	<p>GON/DTE: Set the output level of gate driver G1 ~ G320 as follows</p> <table><tr><th>GON</th><th>DTE</th><th>G1~G320 Gate Output</th></tr><tr><td>0</td><td>0</td><td>VGH</td></tr><tr><td>0</td><td>1</td><td>VGH</td></tr><tr><td>1</td><td>0</td><td>VGL</td></tr><tr><td>1</td><td>1</td><td>Normal display</td></tr></table>													GON	DTE	G1~G320 Gate Output	0	0	VGH	0	1	VGH	1	0	VGL	1	1	Normal display
	GON	DTE	G1~G320 Gate Output																									
	0	0	VGH																									
	0	1	VGH																									
	1	0	VGL																									
1	1	Normal display																										
<p>EPF[1:0] Set the data format when 16bbp (R,G,B) to 18 bbp (r, g, b) is stored in the internal GRAM</p>																												



Restriction

Register Availability	<table><tr><td colspan="4">Status</td><td colspan="2">Availability</td></tr><tr><td colspan="4">Normal Mode ON, Idle Mode OFF, Sleep OUT</td><td colspan="2">Yes</td></tr><tr><td colspan="4">Normal Mode ON, Idle Mode ON, Sleep OUT</td><td colspan="2">Yes</td></tr><tr><td colspan="4">Partial Mode ON, Idle Mode OFF, Sleep OUT</td><td colspan="2">Yes</td></tr><tr><td colspan="4">Partial Mode ON, Idle Mode ON, Sleep OUT</td><td colspan="2">Yes</td></tr><tr><td colspan="4">Sleep IN</td><td colspan="2">Yes</td></tr></table>						Status				Availability		Normal Mode ON, Idle Mode OFF, Sleep OUT				Yes		Normal Mode ON, Idle Mode ON, Sleep OUT				Yes		Partial Mode ON, Idle Mode OFF, Sleep OUT				Yes		Partial Mode ON, Idle Mode ON, Sleep OUT				Yes		Sleep IN				Yes	
	Status				Availability																																					
	Normal Mode ON, Idle Mode OFF, Sleep OUT				Yes																																					
	Normal Mode ON, Idle Mode ON, Sleep OUT				Yes																																					
	Partial Mode ON, Idle Mode OFF, Sleep OUT				Yes																																					
	Partial Mode ON, Idle Mode ON, Sleep OUT				Yes																																					
Sleep IN				Yes																																						
Default	<table><tr><td rowspan="2">Status</td><td colspan="5">Default Value</td></tr><tr><td>EPF[1:0]</td><td>DSTB</td><td>GON</td><td>DTE</td><td>GAS</td></tr><tr><td>Power ON Sequence</td><td>2'b00</td><td>1'b0</td><td>1'b1</td><td>1'b1</td><td>1'b0</td></tr><tr><td>H/W Reset</td><td>2b'00</td><td>1'b0</td><td>1'b1</td><td>1'b1</td><td>1'b0</td></tr></table>						Status	Default Value					EPF[1:0]	DSTB	GON	DTE	GAS	Power ON Sequence	2'b00	1'b0	1'b1	1'b1	1'b0	H/W Reset	2b'00	1'b0	1'b1	1'b1	1'b0													
	Status	Default Value																																								
		EPF[1:0]	DSTB	GON	DTE	GAS																																				
	Power ON Sequence	2'b00	1'b0	1'b1	1'b1	1'b0																																				
H/W Reset	2b'00	1'b0	1'b1	1'b1	1'b0																																					

8.2.58. Power Control 1 (C0h)

C0h	PWCTRL 1 (Power Control 1)																																																																															
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																																			
Command	0	1	↑	XXXXXXXX	1	1	0	0	0	0	0	0	C0h																																																																			
1 st Parameter	1	1	↑	XXXXXXXX	0	0	0	VRH1[4:0]					XX																																																																			
2 nd Parameter	1	1	↑	XXXXXXXX	0	0	0	VRH2[4:0]					XX																																																																			
Description	VRH1[4:0]: Sets the VREG1OUT voltage for positive gamma																																																																															
	<table><tr><th>VRH1[4:0]</th><th>VREG1OUT</th><th>VRH1[4:0]</th><th>VREG1OUT</th></tr><tr><td>5'h00</td><td>Halt (Vreg1out =Hiz)</td><td>5'h10</td><td>1.25 x 3.65 = 4.5625</td></tr><tr><td>5'h01</td><td>1.25 x 2.90 = 3.6250</td><td>5'h11</td><td>1.25 x 3.70 = 4.6250</td></tr><tr><td>5'h02</td><td>1.25 x 2.95 = 3.6875</td><td>5'h12</td><td>1.25 x 3.75 = 4.6875</td></tr><tr><td>5'h03</td><td>1.25 x 3.00 = 3.7500</td><td>5'h13</td><td>1.25 x 3.80 = 4.7500</td></tr><tr><td>5'h04</td><td>1.25 x 3.05 = 3.8125</td><td>5'h14</td><td>1.25 x 3.85 = 4.8125</td></tr><tr><td>5'h05</td><td>1.25 x 3.10 = 3.8750</td><td>5'h15</td><td>1.25 x 3.90 = 4.8750</td></tr><tr><td>5'h06</td><td>1.25 x 3.15 = 3.9375</td><td>5'h16</td><td>1.25 x 3.95 = 4.9375</td></tr><tr><td>5'h07</td><td>1.25 x 3.20 = 4.0000</td><td>5'h17</td><td>1.25 x 4.00 = 5.0000</td></tr><tr><td>5'h08</td><td>1.25 x 3.25 = 4.0625</td><td>5'h18</td><td>1.25 x 4.05 = 5.0625</td></tr><tr><td>5'h09</td><td>1.25 x 3.30 = 4.1250</td><td>5'h19</td><td>1.25 x 4.10 = 5.1250</td></tr><tr><td>5'h0A</td><td>1.25 x 3.35 = 4.1875</td><td>5'h1A</td><td>1.25 x 4.15 = 5.1875</td></tr><tr><td>5'h0B</td><td>1.25 x 3.40 = 4.2500</td><td>5'h1B</td><td>1.25 x 4.20 = 5.2500</td></tr><tr><td>5'h0C</td><td>1.25 x 3.45 = 4.3125</td><td>5'h1C</td><td>1.25 x 4.25 = 5.3125</td></tr><tr><td>5'h0D</td><td>1.25 x 3.50 = 4.3750</td><td>5'h1D</td><td>1.25 x 4.30 = 5.3750</td></tr><tr><td>5'h0E</td><td>1.25 x 3.55 = 4.4375</td><td>5'h1E</td><td>1.25 x 4.35 = 5.4375</td></tr><tr><td>5'h0F</td><td>1.25 x 3.60 = 4.5000</td><td>5'h1F</td><td>1.25 x 4.40 = 5.5000</td></tr></table>													VRH1[4:0]	VREG1OUT	VRH1[4:0]	VREG1OUT	5'h00	Halt (Vreg1out =Hiz)	5'h10	1.25 x 3.65 = 4.5625	5'h01	1.25 x 2.90 = 3.6250	5'h11	1.25 x 3.70 = 4.6250	5'h02	1.25 x 2.95 = 3.6875	5'h12	1.25 x 3.75 = 4.6875	5'h03	1.25 x 3.00 = 3.7500	5'h13	1.25 x 3.80 = 4.7500	5'h04	1.25 x 3.05 = 3.8125	5'h14	1.25 x 3.85 = 4.8125	5'h05	1.25 x 3.10 = 3.8750	5'h15	1.25 x 3.90 = 4.8750	5'h06	1.25 x 3.15 = 3.9375	5'h16	1.25 x 3.95 = 4.9375	5'h07	1.25 x 3.20 = 4.0000	5'h17	1.25 x 4.00 = 5.0000	5'h08	1.25 x 3.25 = 4.0625	5'h18	1.25 x 4.05 = 5.0625	5'h09	1.25 x 3.30 = 4.1250	5'h19	1.25 x 4.10 = 5.1250	5'h0A	1.25 x 3.35 = 4.1875	5'h1A	1.25 x 4.15 = 5.1875	5'h0B	1.25 x 3.40 = 4.2500	5'h1B	1.25 x 4.20 = 5.2500	5'h0C	1.25 x 3.45 = 4.3125	5'h1C	1.25 x 4.25 = 5.3125	5'h0D	1.25 x 3.50 = 4.3750	5'h1D	1.25 x 4.30 = 5.3750	5'h0E	1.25 x 3.55 = 4.4375	5'h1E	1.25 x 4.35 = 5.4375	5'h0F	1.25 x 3.60 = 4.5000	5'h1F
VRH1[4:0]	VREG1OUT	VRH1[4:0]	VREG1OUT																																																																													
5'h00	Halt (Vreg1out =Hiz)	5'h10	1.25 x 3.65 = 4.5625																																																																													
5'h01	1.25 x 2.90 = 3.6250	5'h11	1.25 x 3.70 = 4.6250																																																																													
5'h02	1.25 x 2.95 = 3.6875	5'h12	1.25 x 3.75 = 4.6875																																																																													
5'h03	1.25 x 3.00 = 3.7500	5'h13	1.25 x 3.80 = 4.7500																																																																													
5'h04	1.25 x 3.05 = 3.8125	5'h14	1.25 x 3.85 = 4.8125																																																																													
5'h05	1.25 x 3.10 = 3.8750	5'h15	1.25 x 3.90 = 4.8750																																																																													
5'h06	1.25 x 3.15 = 3.9375	5'h16	1.25 x 3.95 = 4.9375																																																																													
5'h07	1.25 x 3.20 = 4.0000	5'h17	1.25 x 4.00 = 5.0000																																																																													
5'h08	1.25 x 3.25 = 4.0625	5'h18	1.25 x 4.05 = 5.0625																																																																													
5'h09	1.25 x 3.30 = 4.1250	5'h19	1.25 x 4.10 = 5.1250																																																																													
5'h0A	1.25 x 3.35 = 4.1875	5'h1A	1.25 x 4.15 = 5.1875																																																																													
5'h0B	1.25 x 3.40 = 4.2500	5'h1B	1.25 x 4.20 = 5.2500																																																																													
5'h0C	1.25 x 3.45 = 4.3125	5'h1C	1.25 x 4.25 = 5.3125																																																																													
5'h0D	1.25 x 3.50 = 4.3750	5'h1D	1.25 x 4.30 = 5.3750																																																																													
5'h0E	1.25 x 3.55 = 4.4375	5'h1E	1.25 x 4.35 = 5.4375																																																																													
5'h0F	1.25 x 3.60 = 4.5000	5'h1F	1.25 x 4.40 = 5.5000																																																																													
Description	VRH2[4:0]: Sets the VREG2OUT voltage for negative gamma																																																																															
	<table><tr><th>VRH2[4:0]</th><th>VREG2OUT</th><th>VRH2[4:0]</th><th>VREG2OUT</th></tr><tr><td>5'h00</td><td>Halt (Vreg2out =Hiz)</td><td>5'h10</td><td>-1.25 x 3.65 = -4.5625</td></tr><tr><td>5'h01</td><td>-1.25 x 2.90 = -3.6250</td><td>5'h11</td><td>-1.25 x 3.70 = -4.6250</td></tr><tr><td>5'h02</td><td>-1.25 x 2.95 = -3.6875</td><td>5'h12</td><td>-1.25 x 3.75 = -4.6875</td></tr><tr><td>5'h03</td><td>-1.25 x 3.00 = -3.7500</td><td>5'h13</td><td>-1.25 x 3.80 = -4.7500</td></tr><tr><td>5'h04</td><td>-1.25 x 3.05 = -3.8125</td><td>5'h14</td><td>-1.25 x 3.85 = -4.8125</td></tr><tr><td>5'h05</td><td>-1.25 x 3.10 = -3.8750</td><td>5'h15</td><td>-1.25 x 3.90 = -4.8750</td></tr><tr><td>5'h06</td><td>-1.25 x 3.15 = -3.9375</td><td>5'h16</td><td>-1.25 x 3.95 = -4.9375</td></tr><tr><td>5'h07</td><td>-1.25 x 3.20 = -4.0000</td><td>5'h17</td><td>-1.25 x 4.00 = -5.0000</td></tr><tr><td>5'h08</td><td>-1.25 x 3.25 = -4.0625</td><td>5'h18</td><td>-1.25 x 4.05 = -5.0625</td></tr><tr><td>5'h09</td><td>-1.25 x 3.30 = -4.1250</td><td>5'h19</td><td>-1.25 x 4.10 = -5.1250</td></tr><tr><td>5'h0A</td><td>-1.25 x 3.35 = -4.1875</td><td>5'h1A</td><td>-1.25 x 4.15 = -5.1875</td></tr><tr><td>5'h0B</td><td>-1.25 x 3.40 = -4.2500</td><td>5'h1B</td><td>-1.25 x 4.20 = -5.2500</td></tr><tr><td>5'h0C</td><td>-1.25 x 3.45 = -4.3125</td><td>5'h1C</td><td>-1.25 x 4.25 = -5.3125</td></tr><tr><td>5'h0D</td><td>-1.25 x 3.50 = -4.3750</td><td>5'h1D</td><td>-1.25 x 4.30 = -5.3750</td></tr><tr><td>5'h0E</td><td>-1.25 x 3.55 = -4.4375</td><td>5'h1E</td><td>-1.25 x 4.35 = -5.4375</td></tr><tr><td>5'h0F</td><td>-1.25 x 3.60 = -4.5000</td><td>5'h1F</td><td>-1.25 x 4.40 = -5.5000</td></tr></table>													VRH2[4:0]	VREG2OUT	VRH2[4:0]	VREG2OUT	5'h00	Halt (Vreg2out =Hiz)	5'h10	-1.25 x 3.65 = -4.5625	5'h01	-1.25 x 2.90 = -3.6250	5'h11	-1.25 x 3.70 = -4.6250	5'h02	-1.25 x 2.95 = -3.6875	5'h12	-1.25 x 3.75 = -4.6875	5'h03	-1.25 x 3.00 = -3.7500	5'h13	-1.25 x 3.80 = -4.7500	5'h04	-1.25 x 3.05 = -3.8125	5'h14	-1.25 x 3.85 = -4.8125	5'h05	-1.25 x 3.10 = -3.8750	5'h15	-1.25 x 3.90 = -4.8750	5'h06	-1.25 x 3.15 = -3.9375	5'h16	-1.25 x 3.95 = -4.9375	5'h07	-1.25 x 3.20 = -4.0000	5'h17	-1.25 x 4.00 = -5.0000	5'h08	-1.25 x 3.25 = -4.0625	5'h18	-1.25 x 4.05 = -5.0625	5'h09	-1.25 x 3.30 = -4.1250	5'h19	-1.25 x 4.10 = -5.1250	5'h0A	-1.25 x 3.35 = -4.1875	5'h1A	-1.25 x 4.15 = -5.1875	5'h0B	-1.25 x 3.40 = -4.2500	5'h1B	-1.25 x 4.20 = -5.2500	5'h0C	-1.25 x 3.45 = -4.3125	5'h1C	-1.25 x 4.25 = -5.3125	5'h0D	-1.25 x 3.50 = -4.3750	5'h1D	-1.25 x 4.30 = -5.3750	5'h0E	-1.25 x 3.55 = -4.4375	5'h1E	-1.25 x 4.35 = -5.4375	5'h0F	-1.25 x 3.60 = -4.5000	5'h1F
VRH2[4:0]	VREG2OUT	VRH2[4:0]	VREG2OUT																																																																													
5'h00	Halt (Vreg2out =Hiz)	5'h10	-1.25 x 3.65 = -4.5625																																																																													
5'h01	-1.25 x 2.90 = -3.6250	5'h11	-1.25 x 3.70 = -4.6250																																																																													
5'h02	-1.25 x 2.95 = -3.6875	5'h12	-1.25 x 3.75 = -4.6875																																																																													
5'h03	-1.25 x 3.00 = -3.7500	5'h13	-1.25 x 3.80 = -4.7500																																																																													
5'h04	-1.25 x 3.05 = -3.8125	5'h14	-1.25 x 3.85 = -4.8125																																																																													
5'h05	-1.25 x 3.10 = -3.8750	5'h15	-1.25 x 3.90 = -4.8750																																																																													
5'h06	-1.25 x 3.15 = -3.9375	5'h16	-1.25 x 3.95 = -4.9375																																																																													
5'h07	-1.25 x 3.20 = -4.0000	5'h17	-1.25 x 4.00 = -5.0000																																																																													
5'h08	-1.25 x 3.25 = -4.0625	5'h18	-1.25 x 4.05 = -5.0625																																																																													
5'h09	-1.25 x 3.30 = -4.1250	5'h19	-1.25 x 4.10 = -5.1250																																																																													
5'h0A	-1.25 x 3.35 = -4.1875	5'h1A	-1.25 x 4.15 = -5.1875																																																																													
5'h0B	-1.25 x 3.40 = -4.2500	5'h1B	-1.25 x 4.20 = -5.2500																																																																													
5'h0C	-1.25 x 3.45 = -4.3125	5'h1C	-1.25 x 4.25 = -5.3125																																																																													
5'h0D	-1.25 x 3.50 = -4.3750	5'h1D	-1.25 x 4.30 = -5.3750																																																																													
5'h0E	-1.25 x 3.55 = -4.4375	5'h1E	-1.25 x 4.35 = -5.4375																																																																													
5'h0F	-1.25 x 3.60 = -4.5000	5'h1F	-1.25 x 4.40 = -5.5000																																																																													
Restriction																																																																																

Register Availability	<table><tr><th>Status</th><th colspan="2">Availability</th></tr><tr><td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td><td colspan="2">Yes</td></tr><tr><td>Normal Mode ON, Idle Mode ON, Sleep OUT</td><td colspan="2">Yes</td></tr><tr><td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td><td colspan="2">Yes</td></tr><tr><td>Partial Mode ON, Idle Mode ON, Sleep OUT</td><td colspan="2">Yes</td></tr><tr><td>Sleep IN</td><td colspan="2">Yes</td></tr></table>			Status	Availability		Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes		Normal Mode ON, Idle Mode ON, Sleep OUT	Yes		Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes		Partial Mode ON, Idle Mode ON, Sleep OUT	Yes		Sleep IN	Yes	
	Status	Availability																			
	Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes																			
	Normal Mode ON, Idle Mode ON, Sleep OUT	Yes																			
	Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes																			
	Partial Mode ON, Idle Mode ON, Sleep OUT	Yes																			
Sleep IN	Yes																				
Default	<table><tr><th>Status</th><th>VRH1</th><th>VRH2</th></tr><tr><td>Power ON Sequence</td><td>5'b01110</td><td>5'b01110</td></tr><tr><td>H/W Reset</td><td>5'b01110</td><td>5'b01110</td></tr></table>			Status	VRH1	VRH2	Power ON Sequence	5'b01110	5'b01110	H/W Reset	5'b01110	5'b01110									
	Status	VRH1	VRH2																		
	Power ON Sequence	5'b01110	5'b01110																		
H/W Reset	5'b01110	5'b01110																			

8.2.59. Power Control 2 (C1h)

C1h	PWCTRL 2 (Power Control 2)																																								
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX																												
Command	0	1	↑	XXXXXXXX	1	1	0	0	0	0	0	1	C1h																												
1 st parameter	1	1	↑	XXXXXXXX	0	1	0	0	0	BT[2:0]			4X																												
2 nd parameter	1	1	↑	XXXXXXXX	0	0	0	0	0	VC[2:0]			XX																												
Description	BT [2:0]: Sets the factor used in the step-up circuits. Select the optimal step-up factor for the operating voltage. To reduce power consumption, set a smaller factor.																																								
	<table><tr><th>BT[2:0]</th><th>DDVDH</th><th>DDVDL</th><th>VCL</th><th>VGH</th><th>VGL</th></tr><tr><td>4'h0</td><td rowspan="8">Vci1 x 2</td><td rowspan="8">-(VCI1-VCL)</td><td rowspan="8">- Vci1</td><td rowspan="3">Vci1 x 6</td><td>- Vci1 x 5</td></tr><tr><td>4'h1</td><td>- Vci1 x 4</td></tr><tr><td>4'h2</td><td>- Vci1 x 3</td></tr><tr><td>4'h3</td><td rowspan="3">Vci1 x 5</td><td>- Vci1 x 5</td></tr><tr><td>4'h4</td><td>- Vci1 x 4</td></tr><tr><td>4'h5</td><td>- Vci1 x 3</td></tr><tr><td>4'h6</td><td rowspan="2">Vci1 x 4</td><td>- Vci1 x4</td></tr><tr><td>4'h7</td><td>- Vci1 x3</td></tr></table>													BT[2:0]	DDVDH	DDVDL	VCL	VGH	VGL	4'h0	Vci1 x 2	-(VCI1-VCL)	- Vci1	Vci1 x 6	- Vci1 x 5	4'h1	- Vci1 x 4	4'h2	- Vci1 x 3	4'h3	Vci1 x 5	- Vci1 x 5	4'h4	- Vci1 x 4	4'h5	- Vci1 x 3	4'h6	Vci1 x 4	- Vci1 x4	4'h7	- Vci1 x3
	BT[2:0]	DDVDH	DDVDL	VCL	VGH	VGL																																			
	4'h0	Vci1 x 2	-(VCI1-VCL)	- Vci1	Vci1 x 6	- Vci1 x 5																																			
	4'h1					- Vci1 x 4																																			
	4'h2					- Vci1 x 3																																			
	4'h3				Vci1 x 5	- Vci1 x 5																																			
	4'h4					- Vci1 x 4																																			
	4'h5					- Vci1 x 3																																			
	4'h6				Vci1 x 4	- Vci1 x4																																			
4'h7	- Vci1 x3																																								
<i>Note: To prevent the device damage, please keep VGH – DDVDH < 8V condition.</i>																																									
VC [2:0]: Sets VCI1 regulator output voltage.																																									
<table><tr><th>VC[2:0]</th><th>Vci1 voltage</th></tr><tr><td>3'h0</td><td>External VCI</td></tr></table>													VC[2:0]	Vci1 voltage	3'h0	External VCI																									
VC[2:0]	Vci1 voltage																																								
3'h0	External VCI																																								
Restriction																																									
Register Availability	<table><tr><th colspan="2">Status</th><th>Availability</th></tr><tr><td colspan="2">Normal Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr><tr><td colspan="2">Normal Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr><tr><td colspan="2">Partial Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr><tr><td colspan="2">Partial Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr><tr><td colspan="2">Sleep IN</td><td>Yes</td></tr></table>													Status		Availability	Normal Mode ON, Idle Mode OFF, Sleep OUT		Yes	Normal Mode ON, Idle Mode ON, Sleep OUT		Yes	Partial Mode ON, Idle Mode OFF, Sleep OUT		Yes	Partial Mode ON, Idle Mode ON, Sleep OUT		Yes	Sleep IN		Yes										
	Status		Availability																																						
	Normal Mode ON, Idle Mode OFF, Sleep OUT		Yes																																						
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	Partial Mode ON, Idle Mode OFF, Sleep OUT		Yes																																						
	Partial Mode ON, Idle Mode ON, Sleep OUT		Yes																																						
Sleep IN		Yes																																							
Default	<table><tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr><tr><th>BT[2:0]</th><th>VC[2:0]</th></tr><tr><td>Power ON Sequence</td><td>3'b000</td><td>3'b000</td></tr><tr><td>H/W Reset</td><td>3'b000</td><td>3'b000</td></tr></table>													Status	Default Value		BT[2:0]	VC[2:0]	Power ON Sequence	3'b000	3'b000	H/W Reset	3'b000	3'b000																	
	Status	Default Value																																							
		BT[2:0]	VC[2:0]																																						
	Power ON Sequence	3'b000	3'b000																																						
H/W Reset	3'b000	3'b000																																							

8.2.60. Power Control 3 (For Normal Mode) (C2h)

C2h	PWCTRL 3 (Power Control 3)																																																							
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																											
Command	0	1	↑	XXXXXXXX	1	1	0	0	0	0	1	0	C2h																																											
1 st parameter	1	1	↑	XXXXXXXX	0	DCA1[2:0]			0	DCA0[2:0]			XX																																											
Description	<p>DCA0 [2:0]: Selects the operating frequency of the step-up circuit 1/4/5 for Normal mode. The higher step-up operating frequency enhances the drivability of the step-up circuit and the quality of display but increases the current consumption. Adjust the frequency taking the trade-off between the display quality and the current consumption into account.</p> <p>DCA1 [2:0]: Selects the operating frequency of the step-up circuit 2/3 for Normal mode. The higher step-up operating frequency enhances the drivability of the step-up circuit and the quality of display but increases the current consumption. Adjust the frequency taking the trade-off between the display quality and the current consumption into account.</p>																																																							
	<table><tr><th colspan="3">DCA0[2:0]</th><th>Step-up cycle for step-up circuit 1/4/5</th></tr><tr><td>0</td><td>0</td><td>0</td><td>1/8 H</td></tr><tr><td>0</td><td>0</td><td>1</td><td>1/4 H</td></tr><tr><td>0</td><td>1</td><td>0</td><td>1/2 H</td></tr><tr><td>0</td><td>1</td><td>1</td><td>1 H</td></tr><tr><td>1</td><td>0</td><td>0</td><td>2 H</td></tr></table>				DCA0[2:0]			Step-up cycle for step-up circuit 1/4/5	0	0	0	1/8 H	0	0	1	1/4 H	0	1	0	1/2 H	0	1	1	1 H	1	0	0	2 H	<table><tr><th colspan="3">DCA1[2:0]</th><th>Step-up cycle for step-up circuit 2/3</th></tr><tr><td>0</td><td>0</td><td>0</td><td>1/2 H</td></tr><tr><td>0</td><td>0</td><td>1</td><td>1 H</td></tr><tr><td>0</td><td>1</td><td>0</td><td>2 H</td></tr><tr><td>0</td><td>1</td><td>1</td><td>4 H</td></tr><tr><td>1</td><td>0</td><td>0</td><td>8 H</td></tr></table>				DCA1[2:0]			Step-up cycle for step-up circuit 2/3	0	0	0	1/2 H	0	0	1	1 H	0	1	0	2 H	0	1	1	4 H	1	0	0	8 H
	DCA0[2:0]			Step-up cycle for step-up circuit 1/4/5																																																				
	0	0	0	1/8 H																																																				
	0	0	1	1/4 H																																																				
	0	1	0	1/2 H																																																				
	0	1	1	1 H																																																				
	1	0	0	2 H																																																				
	DCA1[2:0]			Step-up cycle for step-up circuit 2/3																																																				
	0	0	0	1/2 H																																																				
0	0	1	1 H																																																					
0	1	0	2 H																																																					
0	1	1	4 H																																																					
1	0	0	8 H																																																					
Restriction																																																								
Register Availability	<table><tr><th colspan="2">Status</th><th>Availability</th></tr><tr><td colspan="2">Normal Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr><tr><td colspan="2">Normal Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr><tr><td colspan="2">Partial Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr><tr><td colspan="2">Partial Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr><tr><td colspan="2">Sleep IN</td><td>Yes</td></tr></table>													Status		Availability	Normal Mode ON, Idle Mode OFF, Sleep OUT		Yes	Normal Mode ON, Idle Mode ON, Sleep OUT		Yes	Partial Mode ON, Idle Mode OFF, Sleep OUT		Yes	Partial Mode ON, Idle Mode ON, Sleep OUT		Yes	Sleep IN		Yes																									
	Status		Availability																																																					
	Normal Mode ON, Idle Mode OFF, Sleep OUT		Yes																																																					
	Normal Mode ON, Idle Mode ON, Sleep OUT		Yes																																																					
	Partial Mode ON, Idle Mode OFF, Sleep OUT		Yes																																																					
	Partial Mode ON, Idle Mode ON, Sleep OUT		Yes																																																					
Sleep IN		Yes																																																						
Default	<table><tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr><tr><th>DCA0[2:0]</th><th>DCA1[2:0]</th></tr><tr><td>Power ON Sequence</td><td>3'b011</td><td>3'b011</td></tr><tr><td>H/W Reset</td><td>3'b011</td><td>3'b011</td></tr></table>													Status	Default Value		DCA0[2:0]	DCA1[2:0]	Power ON Sequence	3'b011	3'b011	H/W Reset	3'b011	3'b011																																
	Status	Default Value																																																						
		DCA0[2:0]	DCA1[2:0]																																																					
	Power ON Sequence	3'b011	3'b011																																																					
H/W Reset	3'b011	3'b011																																																						

8.2.61. Power Control 4 (For Idle Mode) (C3h)

C3h	PWCTRL 4 (Power Control 4)																																																												
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																
Command	0	1	↑	XXXXXXXX	1	1	0	0	0	0	1	1	C3h																																																
1 st Parameter	1	1	↑	XXXXXXXX	0	DCB1[2:0]			0	DCB0[2:0]			XX																																																
Description	<p>DCB0 [2:0]: Selects the operating frequency of the step-up circuit 1/4/5 for Idle mode. The higher step-up operating frequency enhances the drivability of the step-up circuit and the quality of display but increases the current consumption. Adjust the frequency taking the trade-off between the display quality and the current consumption into account.</p> <p>DCB1 [2:0]: Selects the operating frequency of the step-up circuit 2/3 for Idle mode. The higher step-up operating frequency enhances the drivability of the step-up circuit and the quality of display but increases the current consumption. Adjust the frequency taking the trade-off between the display quality and the current consumption into account.</p> <table><tr><th colspan="3">DCB0[2:0]</th><th>Step-up cycle for step-up circuit 1/4/5</th></tr><tr><td>0</td><td>0</td><td>0</td><td>1/8 H</td></tr><tr><td>0</td><td>0</td><td>1</td><td>1/4 H</td></tr><tr><td>0</td><td>1</td><td>0</td><td>1/2 H</td></tr><tr><td>0</td><td>1</td><td>1</td><td>1 H</td></tr><tr><td>1</td><td>0</td><td>0</td><td>2 H</td></tr></table> <table><tr><th colspan="3">DCB1[2:0]</th><th>Step-up cycle for step-up circuit 2/3</th></tr><tr><td>0</td><td>0</td><td>0</td><td>1/2 H</td></tr><tr><td>0</td><td>0</td><td>1</td><td>1 H</td></tr><tr><td>0</td><td>1</td><td>0</td><td>2 H</td></tr><tr><td>0</td><td>1</td><td>1</td><td>4 H</td></tr><tr><td>1</td><td>0</td><td>0</td><td>8 H</td></tr></table>													DCB0[2:0]			Step-up cycle for step-up circuit 1/4/5	0	0	0	1/8 H	0	0	1	1/4 H	0	1	0	1/2 H	0	1	1	1 H	1	0	0	2 H	DCB1[2:0]			Step-up cycle for step-up circuit 2/3	0	0	0	1/2 H	0	0	1	1 H	0	1	0	2 H	0	1	1	4 H	1	0	0	8 H
	DCB0[2:0]			Step-up cycle for step-up circuit 1/4/5																																																									
	0	0	0	1/8 H																																																									
	0	0	1	1/4 H																																																									
	0	1	0	1/2 H																																																									
	0	1	1	1 H																																																									
	1	0	0	2 H																																																									
	DCB1[2:0]			Step-up cycle for step-up circuit 2/3																																																									
	0	0	0	1/2 H																																																									
	0	0	1	1 H																																																									
0	1	0	2 H																																																										
0	1	1	4 H																																																										
1	0	0	8 H																																																										
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Register Availability	<table><tr><th colspan="2">Status</th><th>Availability</th></tr><tr><td colspan="2">Normal Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr><tr><td colspan="2">Normal Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr><tr><td colspan="2">Partial Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr><tr><td colspan="2">Partial Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr><tr><td colspan="2">Sleep IN</td><td>Yes</td></tr></table>													Status		Availability	Normal Mode ON, Idle Mode OFF, Sleep OUT		Yes	Normal Mode ON, Idle Mode ON, Sleep OUT		Yes	Partial Mode ON, Idle Mode OFF, Sleep OUT		Yes	Partial Mode ON, Idle Mode ON, Sleep OUT		Yes	Sleep IN		Yes																														
Status		Availability																																																											
Normal Mode ON, Idle Mode OFF, Sleep OUT		Yes																																																											
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Sleep IN		Yes																																																											
Default	<table><tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr><tr><th>DCB0[2:0]</th><th>DCB1[2:0]</th></tr><tr><td>Power ON Sequence</td><td>3'b011</td><td>3'b011</td></tr><tr><td>H/W Reset</td><td>3'b011</td><td>3'b011</td></tr></table>													Status	Default Value		DCB0[2:0]	DCB1[2:0]	Power ON Sequence	3'b011	3'b011	H/W Reset	3'b011	3'b011																																					
Status	Default Value																																																												
	DCB0[2:0]	DCB1[2:0]																																																											
Power ON Sequence	3'b011	3'b011																																																											
H/W Reset	3'b011	3'b011																																																											

8.2.62. Power Control 5 (For Partial Mode) (C4h)

C4h	PWCTRL 5 (Power Control 5)																																																																																															
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																																																			
Command	0	1	↑	XXXXXXXX	1	1	0	0	0	1	0	0	C4h																																																																																			
1 st Parameter	1	1	↑	XXXXXXXX	0	DCC1[2:0]			0	DCC0[2:0]			XX																																																																																			
Description	<p>DCC0 [2:0]: Selects the operating frequency of the step-up circuit 1/4/5 for Partial mode. The higher step-up operating frequency enhances the drivability of the step-up circuit and the quality of display but increases the current consumption. Adjust the frequency taking the trade-off between the display quality and the current consumption into account.</p> <p>DCC1 [2:0]: Selects the operating frequency of the step-up circuit 2/3 for Partial mode. The higher step-up operating frequency enhances the drivability of the step-up circuit and the quality of display but increases the current consumption. Adjust the frequency taking the trade-off between the display quality and the current consumption into account.</p>																																																																																															
	<table><tr><td colspan="3">DCC0[2:0]</td><td>Step-up cycle for step-up circuit 1/4/5</td></tr><tr><td>0</td><td>0</td><td>0</td><td>1/8 H</td></tr><tr><td>0</td><td>0</td><td>1</td><td>1/4 H</td></tr><tr><td>0</td><td>1</td><td>0</td><td>1/2 H</td></tr><tr><td>0</td><td>1</td><td>1</td><td>1 H</td></tr><tr><td>1</td><td>0</td><td>0</td><td>2 H</td></tr></table>				DCC0[2:0]			Step-up cycle for step-up circuit 1/4/5	0	0	0	1/8 H	0	0	1	1/4 H	0	1	0	1/2 H	0	1	1	1 H	1	0	0	2 H	<table><tr><td colspan="3">DCC1[2:0]</td><td>Step-up cycle for step-up circuit 2/3</td></tr><tr><td>0</td><td>0</td><td>0</td><td>1/2 H</td></tr><tr><td>0</td><td>0</td><td>1</td><td>1 H</td></tr><tr><td>0</td><td>1</td><td>0</td><td>2 H</td></tr><tr><td>0</td><td>1</td><td>1</td><td>4 H</td></tr><tr><td>1</td><td>0</td><td>0</td><td>8 H</td></tr></table>				DCC1[2:0]			Step-up cycle for step-up circuit 2/3	0	0	0	1/2 H	0	0	1	1 H	0	1	0	2 H	0	1	1	4 H	1	0	0	8 H																																								
	DCC0[2:0]			Step-up cycle for step-up circuit 1/4/5																																																																																												
	0	0	0	1/8 H																																																																																												
	0	0	1	1/4 H																																																																																												
	0	1	0	1/2 H																																																																																												
	0	1	1	1 H																																																																																												
	1	0	0	2 H																																																																																												
	DCC1[2:0]			Step-up cycle for step-up circuit 2/3																																																																																												
	0	0	0	1/2 H																																																																																												
0	0	1	1 H																																																																																													
0	1	0	2 H																																																																																													
0	1	1	4 H																																																																																													
1	0	0	8 H																																																																																													
Restriction																																																																																																
Register Availability	<table><tr><td colspan="10">Status</td><td colspan="3">Availability</td></tr><tr><td colspan="13">Normal Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr><tr><td colspan="13">Normal Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr><tr><td colspan="13">Partial Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr><tr><td colspan="13">Partial Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr><tr><td colspan="13">Sleep IN</td><td>Yes</td></tr></table>													Status										Availability			Normal Mode ON, Idle Mode OFF, Sleep OUT													Yes	Normal Mode ON, Idle Mode ON, Sleep OUT													Yes	Partial Mode ON, Idle Mode OFF, Sleep OUT													Yes	Partial Mode ON, Idle Mode ON, Sleep OUT													Yes	Sleep IN													Yes
	Status										Availability																																																																																					
	Normal Mode ON, Idle Mode OFF, Sleep OUT													Yes																																																																																		
	Normal Mode ON, Idle Mode ON, Sleep OUT													Yes																																																																																		
	Partial Mode ON, Idle Mode OFF, Sleep OUT													Yes																																																																																		
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Sleep IN													Yes																																																																																			
Default	<table><tr><td rowspan="2">Status</td><td colspan="12">Default Value</td></tr><tr><td colspan="6">DCC0[2:0]</td><td colspan="6">DCC1[2:0]</td></tr><tr><td colspan="6">Power ON Sequence</td><td colspan="6">3'b011</td><td colspan="2">3'b011</td></tr><tr><td colspan="6">H/W Reset</td><td colspan="6">3'b011</td><td colspan="2">3'b011</td></tr></table>													Status	Default Value												DCC0[2:0]						DCC1[2:0]						Power ON Sequence						3'b011						3'b011		H/W Reset						3'b011						3'b011																															
	Status	Default Value																																																																																														
		DCC0[2:0]						DCC1[2:0]																																																																																								
	Power ON Sequence						3'b011						3'b011																																																																																			
H/W Reset						3'b011						3'b011																																																																																				

8.2.63. VCOM Control (C5h)

C5h	VMCTRL (VCOM Control)												
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	1	1	0	0	0	1	0	1	C5h
1 st Parameter	1	↑	1	XXXXXXXX	0	0	0	0	0	0	0	nVM	XX
2 nd Parameter	1	1	↑	XXXXXXXX	VCM_REG[7:0]								XX
3 rd Parameter	1	1	↑	XXXXXXXX	VCM_REG_EN	0	0	0	0	0	0	0	XX
4 rd Parameter	1	↑	1	XXXXXXXX	VCM_OUT[7:0]								XX
Description	nVM : When the NV memory is programmed, the nVM will be set as '1' automatically. 0 : NV memory is not programmed 1 : NV memory is programmed												
	VCM_REG [7:0] is used to set factor to generate VCOM voltage from the reference voltage VREG2OUT.												
	VCM[7:0]								VCOM				
	0	0	0	0	0	0	0	0	-2				
	0	0	0	0	0	0	0	1	-1.98438				
	0	0	0	0	0	0	1	0	-1.96875				
	0	0	0	0	0	0	1	1	-1.95313				
	0	0	0	0	0	1	0	0	-1.9375				
	0	0	0	0	0	1	0	1	-1.92188				
	0	0	0	0	0	1	1	0	-1.90625				
	0	0	0	0	0	1	1	1	-1.89063				
	0	0	0	0	1	0	0	0	-1.875				
	0	0	0	0	1	0	0	1	-1.85938				
	0	0	0	0	1	0	1	0	-1.84375				
	0	0	0	0	1	0	1	1	-1.82813				
	0	0	0	0	1	1	0	0	-1.8125				
	0	0	0	0	1	1	0	1	-1.79688				
	0	0	0	0	1	1	1	0	-1.78125				
	0	0	0	0	1	1	1	1	-1.76563				
	0	0	0	1	0	0	0	0	-1.75				
	0	0	0	1	0	0	0	1	-1.73438				
	0	0	0	1	0	0	1	0	-1.71875				
	0	0	0	1	0	0	1	1	-1.70313				
	0	0	0	1	0	1	0	0	-1.6875				
	0	0	0	1	0	1	0	1	-1.67188				
	0	0	0	1	0	1	1	0	-1.65625				
	0	0	0	1	0	1	1	1	-1.64063				
	0	0	0	1	1	0	0	0	-1.625				
	0	0	0	1	1	0	0	1	-1.60938				
	0	0	0	1	1	0	1	0	-1.59375				
	0	0	0	1	1	0	1	1	-1.57813				
	0	0	0	1	1	1	0	0	-1.5625				
	0	0	0	1	1	1	0	1	-1.54688				
	0	0	0	1	1	1	1	0	-1.53125				
	0	0	0	1	1	1	1	1	-1.51563				
	0	0	1	0	0	0	0	0	-1.5				
	0	0	1	0	0	0	0	1	-1.48438				
	0	0	1	0	0	0	1	0	-1.46875				
	0	0	1	0	0	0	1	1	-1.45313				
	0	0	1	0	0	1	0	0	-1.4375				
	0	0	1	0	0	1	0	1	-1.42188				
	0	0	1	0	0	1	1	0	-1.40625				
	0	0	1	0	0	1	1	1	-1.39063				
	0	0	1	0	1	0	0	0	-1.375				
	0	0	1	0	1	0	0	1	-1.35938				
	0	0	1	0	1	0	1	0	-1.34375				
0	0	1	0	1	0	1	1	-1.32813					

		0	0	1	0	1	1	0	0	-1.3125	
		0	0	1	0	1	1	0	1	-1.29688	
		0	0	1	0	1	1	1	0	-1.28125	
		0	0	1	0	1	1	1	1	-1.26563	
		0	0	1	1	0	0	0	0	-1.25	
		0	0	1	1	0	0	0	1	-1.23438	
		0	0	1	1	0	0	1	0	-1.21875	
		0	0	1	1	0	0	1	1	-1.20313	
		0	0	1	1	0	1	0	0	-1.1875	
		0	0	1	1	0	1	0	1	-1.17188	
		0	0	1	1	0	1	1	0	-1.15625	
		0	0	1	1	0	1	1	1	-1.14063	
		0	0	1	1	1	0	0	0	-1.125	
		0	0	1	1	1	0	0	1	-1.10938	
		0	0	1	1	1	0	1	0	-1.09375	
		0	0	1	1	1	0	1	1	-1.07813	
		0	0	1	1	1	1	0	0	-1.0625	
		0	0	1	1	1	1	0	1	-1.04688	
		0	0	1	1	1	1	1	0	-1.03125	
		0	0	1	1	1	1	1	1	-1.01563	
		0	1	0	0	0	0	0	0	-1	
		0	1	0	0	0	0	0	1	-0.98438	
		0	1	0	0	0	0	1	0	-0.96875	
		0	1	0	0	0	0	1	1	-0.95313	
		0	1	0	0	0	1	0	0	-0.9375	
		0	1	0	0	0	1	0	1	-0.92188	
		0	1	0	0	0	1	1	0	-0.90625	
		0	1	0	0	0	1	1	1	-0.89063	
		0	1	0	0	1	0	0	0	-0.875	
		0	1	0	0	1	0	0	1	-0.85938	
		0	1	0	0	1	0	1	0	-0.84375	
		0	1	0	0	1	0	1	1	-0.82813	
		0	1	0	0	1	1	0	0	-0.8125	
		0	1	0	0	1	1	0	1	-0.79688	
		0	1	0	0	1	1	1	0	-0.78125	
		0	1	0	0	1	1	1	1	-0.76563	
		0	1	0	1	0	0	0	0	-0.75	
		0	1	0	1	0	0	0	1	-0.73438	
		0	1	0	1	0	0	1	0	-0.71875	
		0	1	0	1	0	0	1	1	-0.70313	
		0	1	0	1	0	1	0	0	-0.6875	
		0	1	0	1	0	1	0	1	-0.67188	
		0	1	0	1	0	1	1	0	-0.65625	
		0	1	0	1	0	1	1	1	-0.64063	
		0	1	0	1	1	0	0	0	-0.625	
		0	1	0	1	1	0	0	1	-0.60938	
		0	1	0	1	1	0	1	0	-0.59375	
		0	1	0	1	1	0	1	1	-0.57813	
		0	1	0	1	1	1	0	0	-0.5625	
		0	1	0	1	1	1	0	1	-0.54688	
		0	1	0	1	1	1	1	0	-0.53125	
		0	1	0	1	1	1	1	1	-0.51563	
		0	1	1	0	0	0	0	0	-0.5	
		0	1	1	0	0	0	0	1	-0.48438	
		0	1	1	0	0	0	1	0	-0.46875	
		0	1	1	0	0	0	1	1	-0.45313	
		0	1	1	0	0	1	0	0	-0.4375	
		0	1	1	0	0	1	0	1	-0.42188	

	<table><tr><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>-0.40625</td></tr><tr><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>-0.39063</td></tr><tr><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>-0.375</td></tr><tr><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>-0.35938</td></tr><tr><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>-0.34375</td></tr><tr><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>-0.32813</td></tr><tr><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>-0.3125</td></tr><tr><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>-0.29688</td></tr><tr><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>-0.28125</td></tr><tr><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>-0.26563</td></tr><tr><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>-0.25</td></tr><tr><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>-0.23438</td></tr><tr><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>-0.21875</td></tr><tr><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>-0.20313</td></tr><tr><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>-0.1875</td></tr><tr><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>-0.17188</td></tr><tr><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>-0.15625</td></tr><tr><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>-0.14063</td></tr><tr><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>-0.125</td></tr><tr><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>-0.10938</td></tr><tr><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>-0.09375</td></tr><tr><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>-0.07813</td></tr><tr><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>-0.0625</td></tr><tr><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>-0.04688</td></tr><tr><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>-0.03125</td></tr><tr><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>-0.01563</td></tr><tr><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr><tr><td colspan="8">10000001~11111110</td><td>Inhibit</td></tr><tr><td colspan="8">11111111</td><td>Halt</td></tr></table> <p>VCM_REG_EN: Select the Vcom value from VCM_REG [7:0] or NV memory. 0: VCOM value from NV memory. 1: VCOM value from VCM_REG [7:0].</p> <p>VCM_OUT [7:0]: NV memory programmed value.</p>	0	1	1	0	0	1	1	0	-0.40625	0	1	1	0	0	1	1	1	-0.39063	0	1	1	0	1	0	0	0	-0.375	0	1	1	0	1	0	0	1	-0.35938	0	1	1	0	1	0	1	0	-0.34375	0	1	1	0	1	0	1	1	-0.32813	0	1	1	0	1	1	0	0	-0.3125	0	1	1	0	1	1	0	1	-0.29688	0	1	1	0	1	1	1	0	-0.28125	0	1	1	0	1	1	1	1	-0.26563	0	1	1	1	0	0	0	0	-0.25	0	1	1	1	0	0	0	1	-0.23438	0	1	1	1	0	0	1	0	-0.21875	0	1	1	1	0	0	1	1	-0.20313	0	1	1	1	0	1	0	0	-0.1875	0	1	1	1	0	1	0	1	-0.17188	0	1	1	1	0	1	1	0	-0.15625	0	1	1	1	0	1	1	1	-0.14063	0	1	1	1	1	0	0	0	-0.125	0	1	1	1	1	0	0	1	-0.10938	0	1	1	1	1	0	1	0	-0.09375	0	1	1	1	1	0	1	1	-0.07813	0	1	1	1	1	1	0	0	-0.0625	0	1	1	1	1	1	0	1	-0.04688	0	1	1	1	1	1	1	0	-0.03125	0	1	1	1	1	1	1	1	-0.01563	1	0	0	0	0	0	0	0	0	10000001~11111110								Inhibit	11111111								Halt
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Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr><tr><td>Normal Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr><tr><td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr><tr><td>Partial Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr><tr><td>Sleep IN</td><td>Yes</td></tr></table>	Status	Availability	Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes	Normal Mode ON, Idle Mode ON, Sleep OUT	Yes	Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes	Partial Mode ON, Idle Mode ON, Sleep OUT	Yes	Sleep IN	Yes																																																																																																																																																																																																																																																									
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Default	<table><tr><th rowspan="2">Status</th><th colspan="4">Default Value</th></tr><tr><th>VCM_OUT[7:0]</th><th>VCM_REG_EN</th><th>VCM_REG[7:0]</th><th>nVM</th></tr><tr><td>Power ON Sequence</td><td>8'bXXXXXXXX</td><td>1'b0</td><td>8'b01100000</td><td>X</td></tr><tr><td>H/W Reset</td><td>8'bXXXXXXXX</td><td>1'b0</td><td>8'b01100000</td><td>X</td></tr></table>	Status	Default Value				VCM_OUT[7:0]	VCM_REG_EN	VCM_REG[7:0]	nVM	Power ON Sequence	8'bXXXXXXXX	1'b0	8'b01100000	X	H/W Reset	8'bXXXXXXXX	1'b0	8'b01100000	X																																																																																																																																																																																																																																																		
Status	Default Value																																																																																																																																																																																																																																																																					
	VCM_OUT[7:0]	VCM_REG_EN	VCM_REG[7:0]	nVM																																																																																																																																																																																																																																																																		
Power ON Sequence	8'bXXXXXXXX	1'b0	8'b01100000	X																																																																																																																																																																																																																																																																		
H/W Reset	8'bXXXXXXXX	1'b0	8'b01100000	X																																																																																																																																																																																																																																																																		

8.2.64. CABC Control 1 (C6h)

C6h	CABCCTRL9 (CABC Control 9)																								
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XXXXXXXX	1	1	0	0	0	1	1	0	C6h												
1 st Parameter	1	1	↑	XXXXXXXX	SCD_VLINE[7:0]								XX												
2 nd Parameter	1	1	↑	XXXXXXXX	0	0	0	0	0	SCD_VLINE[10:8]			XX												
Description	SCD_VLINE [10:0]: This parameter is used set the display line per frame while partial mode ON.																								
	SCD_VLINE[8:0]											Display line													
	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0														
	0	0	0	0	0	0	0	0	0	0	0	Setting prohibited													
	0	0	0	0	0	0	0	0	0	0	1	1 line													
	0	0	0	0	0	0	0	0	0	1	0	2 lines													
	0	0	0	0	0	0	0	0	0	1	1	3 lines													
	0	0	0	0	0	0	0	1	0	0	0	4 lines													
	:											:													
	:											:													
	0	0	1	1	1	0	1	1	1	0	1	477 lines													
	0	0	1	1	1	0	1	1	1	1	0	478 lines													
	0	0	1	1	1	0	1	1	1	1	1	479 lines													
	0	0	1	1	1	1	0	0	0	0	0	480 lines													
	Others											Setting prohibited													
	Restriction																								
	Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr><tr><td>Normal Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr><tr><td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr><tr><td>Partial Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr><tr><td>Sleep IN</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes	Normal Mode ON, Idle Mode ON, Sleep OUT	Yes	Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes	Partial Mode ON, Idle Mode ON, Sleep OUT	Yes	Sleep IN
Status	Availability																								
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes																								
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes																								
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes																								
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes																								
Sleep IN	Yes																								
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power ON Sequence</td><td>11'b00111100000</td></tr><tr><td>S/W Reset</td><td>11'b00111100000</td></tr><tr><td>H/W Reset</td><td>11'b00111100000</td></tr></table>													Status	Default Value	Power ON Sequence	11'b00111100000	S/W Reset	11'b00111100000	H/W Reset	11'b00111100000				
Status	Default Value																								
Power ON Sequence	11'b00111100000																								
S/W Reset	11'b00111100000																								
H/W Reset	11'b00111100000																								

8.2.65. CABC Control 2 (C8h)

C8h	CABCCTRL1 (CABC Control 1)																															
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX																			
Command	0	1	↑	XXXXXXXX	1	1	0	0	1	0	0	0	C8h																			
1 st Parameter	1	1	↑	XXXXXXXX	0	0	0	0	0	LEDONR	LEDONPOL	PWMPOL	XX																			
Description	PWMPOL: The bit is used to define polarity of CABC_PWM signal.																															
	<table><tr><th>BL</th><th>LEDPWMPOL</th><th>CABC_PWM pin</th></tr><tr><td>0</td><td>0</td><td>Always low</td></tr><tr><td>0</td><td>1</td><td>Always high</td></tr><tr><td>1</td><td>0</td><td>Original polarity of PWM signal</td></tr><tr><td>1</td><td>1</td><td>Inversed polarity of PWM signal</td></tr></table>													BL	LEDPWMPOL	CABC_PWM pin	0	0	Always low	0	1	Always high	1	0	Original polarity of PWM signal	1	1	Inversed polarity of PWM signal				
	BL	LEDPWMPOL	CABC_PWM pin																													
	0	0	Always low																													
	0	1	Always high																													
	1	0	Original polarity of PWM signal																													
	1	1	Inversed polarity of PWM signal																													
	LEDONPOL: This bit is used to control CABC_ON pin.																															
	<table><tr><th>BL</th><th>LEDONPOL</th><th>CABC_ON pin</th></tr><tr><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>1</td><td>1</td></tr><tr><td>1</td><td>0</td><td>LEDONR</td></tr><tr><td>1</td><td>1</td><td>Inversed LEDONR</td></tr></table>													BL	LEDONPOL	CABC_ON pin	0	0	0	0	1	1	1	0	LEDONR	1	1	Inversed LEDONR				
	BL	LEDONPOL	CABC_ON pin																													
0	0	0																														
0	1	1																														
1	0	LEDONR																														
1	1	Inversed LEDONR																														
LEDONR: This bit is used to control CABC_ON pin.																																
<table><tr><th>LEDONR</th><th>Description</th></tr><tr><td>0</td><td>Low</td></tr><tr><td>1</td><td>High</td></tr></table>													LEDONR	Description	0	Low	1	High														
LEDONR	Description																															
0	Low																															
1	High																															
Restriction																																
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr><tr><td>Normal Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr><tr><td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr><tr><td>Partial Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr><tr><td>Sleep IN</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes	Normal Mode ON, Idle Mode ON, Sleep OUT	Yes	Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes	Partial Mode ON, Idle Mode ON, Sleep OUT	Yes	Sleep IN	Yes							
Status	Availability																															
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes																															
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes																															
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes																															
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes																															
Sleep IN	Yes																															
Default	<table><tr><th rowspan="2">Status</th><th colspan="3">Default Value</th></tr><tr><th>LEDONR</th><th>LEDONPOL</th><th>LEDPWMPOL</th></tr><tr><td>Power On Sequence</td><td>1'b0</td><td>1'b0</td><td>1'b0</td></tr><tr><td>SW Reset</td><td>No change</td><td>No change</td><td>No change</td></tr><tr><td>HW Reset</td><td>1'b0</td><td>1'b0</td><td>1'b0</td></tr></table>													Status	Default Value			LEDONR	LEDONPOL	LEDPWMPOL	Power On Sequence	1'b0	1'b0	1'b0	SW Reset	No change	No change	No change	HW Reset	1'b0	1'b0	1'b0
Status	Default Value																															
	LEDONR	LEDONPOL	LEDPWMPOL																													
Power On Sequence	1'b0	1'b0	1'b0																													
SW Reset	No change	No change	No change																													
HW Reset	1'b0	1'b0	1'b0																													

8.2.66. CABC Control 3 (C9h)

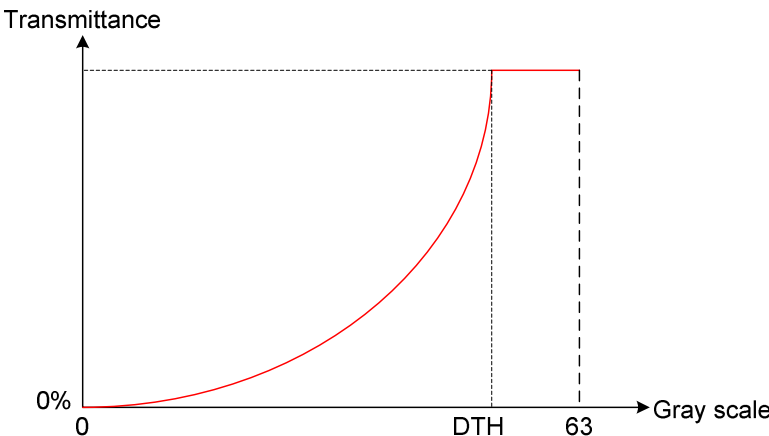
C9h	CABCCTRL2 (CABC Control 2)																																																																																																											
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																																																															
Command	0	1	↑	XXXXXXXX	1	1	0	0	1	0	0	1	C9h																																																																																															
1 st Parameter	1	1	↑	XXXXXXXX	THRES_MOV[3:0]				THRES_STILL[3:0]				XX																																																																																															
Description	<p>THRES_MOV [3:0]: This parameter is used to set the ratio (percentage) of the maximum number of pixels that makes display image white (data="63") to the total of pixels by image process in MOVING image mode. After this parameter sets the number of pixels that makes display image white, threshold grayscale value (DTH) that makes display image white is set so that the number of the pixels set by this parameter does not change.</p>																																																																																																											
	<table><tr><th colspan="4">THRES_MOV[3:0]</th><th rowspan="2">Description</th></tr><tr><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>99 %</td></tr><tr><td>0</td><td>0</td><td>0</td><td>1</td><td>98 %</td></tr><tr><td>0</td><td>0</td><td>1</td><td>0</td><td>96 %</td></tr><tr><td>0</td><td>0</td><td>1</td><td>1</td><td>94 %</td></tr><tr><td>0</td><td>1</td><td>0</td><td>0</td><td>92 %</td></tr><tr><td>0</td><td>1</td><td>0</td><td>1</td><td>90 %</td></tr><tr><td>0</td><td>1</td><td>1</td><td>0</td><td>88 %</td></tr><tr><td>0</td><td>1</td><td>1</td><td>1</td><td>86 %</td></tr></table>					THRES_MOV[3:0]				Description	D3	D2	D1	D0	0	0	0	0	99 %	0	0	0	1	98 %	0	0	1	0	96 %	0	0	1	1	94 %	0	1	0	0	92 %	0	1	0	1	90 %	0	1	1	0	88 %	0	1	1	1	86 %	<table><tr><th colspan="4">THRES_MOV[3:0]</th><th rowspan="2">Description</th></tr><tr><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr><tr><td>1</td><td>0</td><td>0</td><td>0</td><td>84 %</td></tr><tr><td>1</td><td>0</td><td>0</td><td>1</td><td>82 %</td></tr><tr><td>1</td><td>0</td><td>1</td><td>0</td><td>80 %</td></tr><tr><td>1</td><td>0</td><td>1</td><td>1</td><td>78 %</td></tr><tr><td>1</td><td>1</td><td>0</td><td>0</td><td>76 %</td></tr><tr><td>1</td><td>1</td><td>0</td><td>1</td><td>74 %</td></tr><tr><td>1</td><td>1</td><td>1</td><td>0</td><td>72 %</td></tr><tr><td>1</td><td>1</td><td>1</td><td>1</td><td>70 %</td></tr></table>					THRES_MOV[3:0]				Description	D3	D2	D1	D0	1	0	0	0	84 %	1	0	0	1	82 %	1	0	1	0	80 %	1	0	1	1	78 %	1	1	0	0	76 %	1	1	0	1	74 %	1	1	1	0	72 %	1	1	1	1	70 %
	THRES_MOV[3:0]				Description																																																																																																							
	D3	D2	D1	D0																																																																																																								
	0	0	0	0	99 %																																																																																																							
	0	0	0	1	98 %																																																																																																							
	0	0	1	0	96 %																																																																																																							
	0	0	1	1	94 %																																																																																																							
	0	1	0	0	92 %																																																																																																							
	0	1	0	1	90 %																																																																																																							
	0	1	1	0	88 %																																																																																																							
0	1	1	1	86 %																																																																																																								
THRES_MOV[3:0]				Description																																																																																																								
D3	D2	D1	D0																																																																																																									
1	0	0	0	84 %																																																																																																								
1	0	0	1	82 %																																																																																																								
1	0	1	0	80 %																																																																																																								
1	0	1	1	78 %																																																																																																								
1	1	0	0	76 %																																																																																																								
1	1	0	1	74 %																																																																																																								
1	1	1	0	72 %																																																																																																								
1	1	1	1	70 %																																																																																																								
<p>THRES_STILL [3:0]: This parameter is used to set the ratio (percentage) of the maximum number of pixels that makes display image white (data="63") to the total of pixels by image process in STILL mode. After this parameter sets the number of pixels that makes display image white, threshold grayscale value (DTH) that makes display image white is set so that the number of the pixels set by this parameter does not change.</p>																																																																																																												
<table><tr><th colspan="4">THRES_STILL[3:0]</th><th rowspan="2">Description</th></tr><tr><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>99 %</td></tr><tr><td>0</td><td>0</td><td>0</td><td>1</td><td>98 %</td></tr><tr><td>0</td><td>0</td><td>1</td><td>0</td><td>96 %</td></tr><tr><td>0</td><td>0</td><td>1</td><td>1</td><td>94 %</td></tr><tr><td>0</td><td>1</td><td>0</td><td>0</td><td>92 %</td></tr><tr><td>0</td><td>1</td><td>0</td><td>1</td><td>90 %</td></tr><tr><td>0</td><td>1</td><td>1</td><td>0</td><td>88 %</td></tr><tr><td>0</td><td>1</td><td>1</td><td>1</td><td>86 %</td></tr></table>					THRES_STILL[3:0]				Description	D3	D2	D1	D0	0	0	0	0	99 %	0	0	0	1	98 %	0	0	1	0	96 %	0	0	1	1	94 %	0	1	0	0	92 %	0	1	0	1	90 %	0	1	1	0	88 %	0	1	1	1	86 %	<table><tr><th colspan="4">THRES_STILL[3:0]</th><th rowspan="2">Description</th></tr><tr><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr><tr><td>1</td><td>0</td><td>0</td><td>0</td><td>84 %</td></tr><tr><td>1</td><td>0</td><td>0</td><td>1</td><td>82 %</td></tr><tr><td>1</td><td>0</td><td>1</td><td>0</td><td>80 %</td></tr><tr><td>1</td><td>0</td><td>1</td><td>1</td><td>78 %</td></tr><tr><td>1</td><td>1</td><td>0</td><td>0</td><td>76 %</td></tr><tr><td>1</td><td>1</td><td>0</td><td>1</td><td>74 %</td></tr><tr><td>1</td><td>1</td><td>1</td><td>0</td><td>72 %</td></tr><tr><td>1</td><td>1</td><td>1</td><td>1</td><td>70 %</td></tr></table>					THRES_STILL[3:0]				Description	D3	D2	D1	D0	1	0	0	0	84 %	1	0	0	1	82 %	1	0	1	0	80 %	1	0	1	1	78 %	1	1	0	0	76 %	1	1	0	1	74 %	1	1	1	0	72 %	1	1	1	1	70 %	
THRES_STILL[3:0]				Description																																																																																																								
D3	D2	D1	D0																																																																																																									
0	0	0	0	99 %																																																																																																								
0	0	0	1	98 %																																																																																																								
0	0	1	0	96 %																																																																																																								
0	0	1	1	94 %																																																																																																								
0	1	0	0	92 %																																																																																																								
0	1	0	1	90 %																																																																																																								
0	1	1	0	88 %																																																																																																								
0	1	1	1	86 %																																																																																																								
THRES_STILL[3:0]				Description																																																																																																								
D3	D2	D1	D0																																																																																																									
1	0	0	0	84 %																																																																																																								
1	0	0	1	82 %																																																																																																								
1	0	1	0	80 %																																																																																																								
1	0	1	1	78 %																																																																																																								
1	1	0	0	76 %																																																																																																								
1	1	0	1	74 %																																																																																																								
1	1	1	0	72 %																																																																																																								
1	1	1	1	70 %																																																																																																								
<div><div>Histogram</div><div><div>100%</div><div>0%</div></div><div><div>0</div><div>DTH</div><div>63</div></div><div>Gray scale</div><div><div>THRES_MOV[3:0] / THRES_STILL[3:0]</div></div></div>																																																																																																												
Restriction																																																																																																												

Register Availability	<table><tr><td>Status</td><td colspan="2">Availability</td></tr><tr><td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td><td colspan="2">Yes</td></tr><tr><td>Normal Mode ON, Idle Mode ON, Sleep OUT</td><td colspan="2">Yes</td></tr><tr><td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td><td colspan="2">Yes</td></tr><tr><td>Partial Mode ON, Idle Mode ON, Sleep OUT</td><td colspan="2">Yes</td></tr><tr><td>Sleep IN</td><td colspan="2">Yes</td></tr></table>			Status	Availability		Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes		Normal Mode ON, Idle Mode ON, Sleep OUT	Yes		Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes		Partial Mode ON, Idle Mode ON, Sleep OUT	Yes		Sleep IN	Yes	
	Status	Availability																			
	Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes																			
	Normal Mode ON, Idle Mode ON, Sleep OUT	Yes																			
	Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes																			
	Partial Mode ON, Idle Mode ON, Sleep OUT	Yes																			
Sleep IN	Yes																				
Default	<table><tr><td rowspan="2">Status</td><td colspan="2">Default Value</td></tr><tr><td>THRES_MOV[3:0]</td><td>THRES_STILL[3:0]</td></tr><tr><td>Power ON Sequence</td><td>4'b1011 b</td><td>4'b1011 b</td></tr><tr><td>S/W Reset</td><td>4'b1011 b</td><td>4'b1011 b</td></tr><tr><td>H/W Reset</td><td>4'b1011 b</td><td>4'b1011 b</td></tr></table>			Status	Default Value		THRES_MOV[3:0]	THRES_STILL[3:0]	Power ON Sequence	4'b1011 b	4'b1011 b	S/W Reset	4'b1011 b	4'b1011 b	H/W Reset	4'b1011 b	4'b1011 b				
	Status	Default Value																			
		THRES_MOV[3:0]	THRES_STILL[3:0]																		
	Power ON Sequence	4'b1011 b	4'b1011 b																		
	S/W Reset	4'b1011 b	4'b1011 b																		
H/W Reset	4'b1011 b	4'b1011 b																			

8.2.67. CABC Control 4 (CAh)

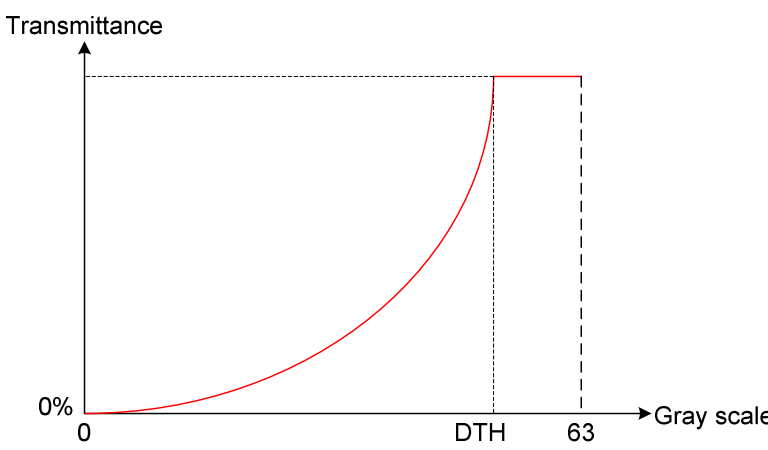
CAh	CABCCTRL3 (CABC Control 3)																																																																																																											
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																																																															
Command	0	1	↑	XXXXXXXX	1	1	0	0	1	0	1	0	CAh																																																																																															
1 st Parameter	1	1	↑	XXXXXXXX	0	0	0	0	THRES_UI[3:0]				XX																																																																																															
Description	<p>THRES_UI [3:0]: This parameter is used to set the ratio (percentage) of the maximum number of pixels that makes display image white (data="63") to the total of pixels by image process in USER INTERFACE mode. After this parameter sets the number of pixels that makes display image white, threshold grayscale value (DTH) that makes display image white is set so that the number of the pixels set by this parameter does not change.</p>																																																																																																											
	<table><thead><tr><th colspan="4">THRES_UI[3:0]</th><th rowspan="2">Description</th></tr><tr><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr></thead><tbody><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>99 %</td></tr><tr><td>0</td><td>0</td><td>0</td><td>1</td><td>98 %</td></tr><tr><td>0</td><td>0</td><td>1</td><td>0</td><td>96 %</td></tr><tr><td>0</td><td>0</td><td>1</td><td>1</td><td>94 %</td></tr><tr><td>0</td><td>1</td><td>0</td><td>0</td><td>92 %</td></tr><tr><td>0</td><td>1</td><td>0</td><td>1</td><td>90 %</td></tr><tr><td>0</td><td>1</td><td>1</td><td>0</td><td>88 %</td></tr><tr><td>0</td><td>1</td><td>1</td><td>1</td><td>86 %</td></tr></tbody></table>					THRES_UI[3:0]				Description	D3	D2	D1	D0	0	0	0	0	99 %	0	0	0	1	98 %	0	0	1	0	96 %	0	0	1	1	94 %	0	1	0	0	92 %	0	1	0	1	90 %	0	1	1	0	88 %	0	1	1	1	86 %	<table><thead><tr><th colspan="4">THRES_UI[3:0]</th><th rowspan="2">Description</th></tr><tr><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr></thead><tbody><tr><td>1</td><td>0</td><td>0</td><td>0</td><td>84 %</td></tr><tr><td>1</td><td>0</td><td>0</td><td>1</td><td>82 %</td></tr><tr><td>1</td><td>0</td><td>1</td><td>0</td><td>80 %</td></tr><tr><td>1</td><td>0</td><td>1</td><td>1</td><td>78 %</td></tr><tr><td>1</td><td>1</td><td>0</td><td>0</td><td>76 %</td></tr><tr><td>1</td><td>1</td><td>0</td><td>1</td><td>74 %</td></tr><tr><td>1</td><td>1</td><td>1</td><td>0</td><td>72 %</td></tr><tr><td>1</td><td>1</td><td>1</td><td>1</td><td>70 %</td></tr></tbody></table>					THRES_UI[3:0]				Description	D3	D2	D1	D0	1	0	0	0	84 %	1	0	0	1	82 %	1	0	1	0	80 %	1	0	1	1	78 %	1	1	0	0	76 %	1	1	0	1	74 %	1	1	1	0	72 %	1	1	1	1	70 %
	THRES_UI[3:0]				Description																																																																																																							
	D3	D2	D1	D0																																																																																																								
	0	0	0	0	99 %																																																																																																							
	0	0	0	1	98 %																																																																																																							
	0	0	1	0	96 %																																																																																																							
	0	0	1	1	94 %																																																																																																							
	0	1	0	0	92 %																																																																																																							
	0	1	0	1	90 %																																																																																																							
0	1	1	0	88 %																																																																																																								
0	1	1	1	86 %																																																																																																								
THRES_UI[3:0]				Description																																																																																																								
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1	1	1	1	70 %																																																																																																								
Restriction																																																																																																												
Register Availability	<table><thead><tr><th>Status</th><th>Availability</th></tr></thead><tbody><tr><td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr><tr><td>Normal Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr><tr><td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr><tr><td>Partial Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr><tr><td>Sleep IN</td><td>Yes</td></tr></tbody></table>													Status	Availability	Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes	Normal Mode ON, Idle Mode ON, Sleep OUT	Yes	Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes	Partial Mode ON, Idle Mode ON, Sleep OUT	Yes	Sleep IN	Yes																																																																																			
Status	Availability																																																																																																											
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes																																																																																																											
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Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes																																																																																																											
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes																																																																																																											
Sleep IN	Yes																																																																																																											
Default	<table><thead><tr><th>Status</th><th>Default Value</th></tr></thead><tbody><tr><td>Power ON Sequence</td><td>4'b1011 b</td></tr><tr><td>S/W Reset</td><td>4'b1011 b</td></tr><tr><td>H/W Reset</td><td>4'b1011 b</td></tr></tbody></table>													Status	Default Value	Power ON Sequence	4'b1011 b	S/W Reset	4'b1011 b	H/W Reset	4'b1011 b																																																																																							
Status	Default Value																																																																																																											
Power ON Sequence	4'b1011 b																																																																																																											
S/W Reset	4'b1011 b																																																																																																											
H/W Reset	4'b1011 b																																																																																																											

8.2.68. CABC Control 5 (CBh)

CBh	CABCCTRL4 (CABC Control 4)																								
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XXXXXXXX	1	1	0	0	1	0	1	1	CBh												
1 st Parameter	1	1	↑	XXXXXXXX	DTH_MOV[3:0]				DTH_STILL[3:0]				XX												
Description	DTH_MOV [3:0]: This parameter is used set the minimum limitation of grayscale threshold value in MOVING image mode.																								
	DTH_MOV[3:0]				Description	DTH_MOV[3:0]				Description															
	D3	D2	D1	D0		D3	D2	D1	D0																
	0	0	0	0	224	1	0	0	0	192															
	0	0	0	1	220	1	0	0	1	188															
	0	0	1	0	216	1	0	1	0	184															
	0	0	1	1	212	1	0	1	1	180															
	0	1	0	0	208	1	1	0	0	176															
	0	1	0	1	204	1	1	0	1	172															
	0	1	1	0	200	1	1	1	0	168															
	0	1	1	1	196	1	1	1	1	164															
DTH_OPT [2:0]: This parameter is used to set the minimum limitation of grayscale threshold value in STILL image mode.																									
DTH_STILL[3:0]				Description	DTH_STILL[3:0]				Description																
D3	D2	D1	D0		D3	D2	D1	D0																	
0	0	0	0	224	1	0	0	0	192																
0	0	0	1	220	1	0	0	1	188																
0	0	1	0	216	1	0	1	0	184																
0	0	1	1	212	1	0	1	1	180																
0	1	0	0	208	1	1	0	0	176																
0	1	0	1	204	1	1	0	1	172																
0	1	1	0	200	1	1	1	0	168																
0	1	1	1	196	1	1	1	1	164																
																									
Restriction																									
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr><tr><td>Normal Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr><tr><td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr><tr><td>Partial Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr><tr><td>Sleep IN</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes	Normal Mode ON, Idle Mode ON, Sleep OUT	Yes	Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes	Partial Mode ON, Idle Mode ON, Sleep OUT	Yes	Sleep IN	Yes
Status	Availability																								
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes																								
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes																								
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes																								
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes																								
Sleep IN	Yes																								

Default			
	Status	Default Value	
		DTH_MOV[3:0]	DTH_STILL[3:0]
	Power ON Sequence	4'b1010 b	4'b1000 b
	S/W Reset	4'b1010 b	4'b1000 b
	H/W Reset	4'b1010 b	4'b1000 b

8.2.69. CABC Control 6 (CCh)

CCh	CABCCTRL5 (CABC Control 5)																																																																																																									
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																																																													
Command	0	1	↑	XXXXXXXX	1	1	0	0	1	1	0	0	CCh																																																																																													
1 st Parameter	1	1	↑	XXXXXXXX	0	0	0	0	DTH_UI[3:0]				XX																																																																																													
Description	DTH_UI [3:0]: This parameter is used set the minimum limitation of grayscale threshold value in USER INTERFACE mode.																																																																																																									
	<table><tr><th colspan="4">DTH_UI[3:0]</th><th rowspan="2">Description</th></tr><tr><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>252</td></tr><tr><td>0</td><td>0</td><td>0</td><td>1</td><td>248</td></tr><tr><td>0</td><td>0</td><td>1</td><td>0</td><td>244</td></tr><tr><td>0</td><td>0</td><td>1</td><td>1</td><td>240</td></tr><tr><td>0</td><td>1</td><td>0</td><td>0</td><td>236</td></tr><tr><td>0</td><td>1</td><td>0</td><td>1</td><td>232</td></tr><tr><td>0</td><td>1</td><td>1</td><td>0</td><td>228</td></tr><tr><td>0</td><td>1</td><td>1</td><td>1</td><td>224</td></tr></table>				DTH_UI[3:0]				Description	D3	D2	D1	D0	0	0	0	0	252	0	0	0	1	248	0	0	1	0	244	0	0	1	1	240	0	1	0	0	236	0	1	0	1	232	0	1	1	0	228	0	1	1	1	224	<table><tr><th colspan="4">DTH_UI[3:0]</th><th rowspan="2">Description</th></tr><tr><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr><tr><td>1</td><td>0</td><td>0</td><td>0</td><td>220</td></tr><tr><td>1</td><td>0</td><td>0</td><td>1</td><td>216</td></tr><tr><td>1</td><td>0</td><td>1</td><td>0</td><td>212</td></tr><tr><td>1</td><td>0</td><td>1</td><td>1</td><td>208</td></tr><tr><td>1</td><td>1</td><td>0</td><td>0</td><td>204</td></tr><tr><td>1</td><td>1</td><td>0</td><td>1</td><td>200</td></tr><tr><td>1</td><td>1</td><td>1</td><td>0</td><td>196</td></tr><tr><td>1</td><td>1</td><td>1</td><td>1</td><td>192</td></tr></table>				DTH_UI[3:0]				Description	D3	D2	D1	D0	1	0	0	0	220	1	0	0	1	216	1	0	1	0	212	1	0	1	1	208	1	1	0	0	204	1	1	0	1	200	1	1	1	0	196	1	1	1	1	192
	DTH_UI[3:0]				Description																																																																																																					
	D3	D2	D1	D0																																																																																																						
	0	0	0	0	252																																																																																																					
	0	0	0	1	248																																																																																																					
	0	0	1	0	244																																																																																																					
	0	0	1	1	240																																																																																																					
	0	1	0	0	236																																																																																																					
	0	1	0	1	232																																																																																																					
0	1	1	0	228																																																																																																						
0	1	1	1	224																																																																																																						
DTH_UI[3:0]				Description																																																																																																						
D3	D2	D1	D0																																																																																																							
1	0	0	0	220																																																																																																						
1	0	0	1	216																																																																																																						
1	0	1	0	212																																																																																																						
1	0	1	1	208																																																																																																						
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1	1	0	1	200																																																																																																						
1	1	1	0	196																																																																																																						
1	1	1	1	192																																																																																																						
 <p>Transmittance</p> <p>0% 0 DTH 63 Gray scale</p>																																																																																																										
Restriction																																																																																																										
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr><tr><td>Normal Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr><tr><td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr><tr><td>Partial Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr><tr><td>Sleep IN</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes	Normal Mode ON, Idle Mode ON, Sleep OUT	Yes	Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes	Partial Mode ON, Idle Mode ON, Sleep OUT	Yes	Sleep IN	Yes																																																																																	
	Status	Availability																																																																																																								
	Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes																																																																																																								
	Normal Mode ON, Idle Mode ON, Sleep OUT	Yes																																																																																																								
	Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes																																																																																																								
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes																																																																																																									
Sleep IN	Yes																																																																																																									
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power ON Sequence</td><td>4'b0100 b</td></tr><tr><td>S/W Reset</td><td>4'b0100 b</td></tr><tr><td>H/W Reset</td><td>4'b0100 b</td></tr></table>													Status	Default Value	Power ON Sequence	4'b0100 b	S/W Reset	4'b0100 b	H/W Reset	4'b0100 b																																																																																					
	Status	Default Value																																																																																																								
	Power ON Sequence	4'b0100 b																																																																																																								
	S/W Reset	4'b0100 b																																																																																																								
H/W Reset	4'b0100 b																																																																																																									

8.2.70. CABC Control 7 (CDh)

CDh	CABCCTRL6 (CABC Control 6)																																																			
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																							
Command	0	1	↑	XXXXXXXX	1	1	0	0	1	1	0	1	CDh																																							
1 st Parameter	1	1	↑	XXXXXXXX	0	DIM_MOV[2:0]			0	DIM_STILL[2:0]			XX																																							
Description	<p>DIM_STILL [2:0]: This parameter is used set the transition time of brightness level change to avoid the sharp brightness change on vision in still mode.</p> <p>DIM_MOV [2:0]: This parameter is used set the transition time of brightness level change to avoid the sharp brightness change on vision in still mode.</p> <table><tr><th colspan="3">DIM_MOV[2:0]/DIM_STILL[2:0]</th><th rowspan="2">Description</th></tr><tr><th>D2</th><th>D1</th><th>D0</th></tr><tr><td>0</td><td>0</td><td>0</td><td>1 frame</td></tr><tr><td>0</td><td>0</td><td>1</td><td>1 frame</td></tr><tr><td>0</td><td>1</td><td>0</td><td>2 frames</td></tr><tr><td>0</td><td>1</td><td>1</td><td>4 frames</td></tr><tr><td>1</td><td>0</td><td>0</td><td>8 frames</td></tr><tr><td>1</td><td>0</td><td>1</td><td>16 frames</td></tr><tr><td>1</td><td>1</td><td>0</td><td>32 frames</td></tr><tr><td>1</td><td>1</td><td>1</td><td>64 frames</td></tr></table> <p><i>Note: As above picture DIM1[2:0] mean DIM_MOV[2:0] or DIM_STILL[2:0] or DIM_UI[2:0] in different mode.</i></p>													DIM_MOV[2:0]/DIM_STILL[2:0]			Description	D2	D1	D0	0	0	0	1 frame	0	0	1	1 frame	0	1	0	2 frames	0	1	1	4 frames	1	0	0	8 frames	1	0	1	16 frames	1	1	0	32 frames	1	1	1	64 frames
	DIM_MOV[2:0]/DIM_STILL[2:0]			Description																																																
	D2	D1	D0																																																	
	0	0	0	1 frame																																																
	0	0	1	1 frame																																																
	0	1	0	2 frames																																																
	0	1	1	4 frames																																																
	1	0	0	8 frames																																																
	1	0	1	16 frames																																																
	1	1	0	32 frames																																																
1	1	1	64 frames																																																	
Restriction																																																				
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr><tr><td>Normal Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr><tr><td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr><tr><td>Partial Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr><tr><td>Sleep IN</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes	Normal Mode ON, Idle Mode ON, Sleep OUT	Yes	Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes	Partial Mode ON, Idle Mode ON, Sleep OUT	Yes	Sleep IN	Yes																											
Status	Availability																																																			
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes																																																			
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes																																																			
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes																																																			
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes																																																			
Sleep IN	Yes																																																			
Default	<table><tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr><tr><th>DIM_MOV[2:0]</th><th>DIM_STILL[2:0]</th></tr><tr><td>Power ON Sequence</td><td>4'b100 b</td><td>3'b011 b</td></tr><tr><td>S/W Reset</td><td>4'b100 b</td><td>3'b011 b</td></tr><tr><td>H/W Reset</td><td>4'b100 b</td><td>3'b011 b</td></tr></table>													Status	Default Value		DIM_MOV[2:0]	DIM_STILL[2:0]	Power ON Sequence	4'b100 b	3'b011 b	S/W Reset	4'b100 b	3'b011 b	H/W Reset	4'b100 b	3'b011 b																									
Status	Default Value																																																			
	DIM_MOV[2:0]	DIM_STILL[2:0]																																																		
Power ON Sequence	4'b100 b	3'b011 b																																																		
S/W Reset	4'b100 b	3'b011 b																																																		
H/W Reset	4'b100 b	3'b011 b																																																		

8.2.71. CABC Control 8 (CEh)

CEh	CABCCTRL7 (CABC Control 7)																																																			
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																							
Command	0	1	↑	XXXXXXXX	1	1	0	0	1	1	1	0	CEh																																							
1 st Parameter	1	1	↑	XXXXXXXX	DIM_MIN[3:0]				0	DIM_UI[2:0]			XX																																							
Description	<p>DIM_UI [2:0]: This parameter is used set the transition time of brightness level change to avoid the sharp brightness change on vision in UI mode.</p> <table><thead><tr><th colspan="3">DIM_MOV[2:0]/DIM_STILL[2:0]</th><th rowspan="2">Description</th></tr><tr><th>D2</th><th>D1</th><th>D0</th></tr></thead><tbody><tr><td>0</td><td>0</td><td>0</td><td>1 frame</td></tr><tr><td>0</td><td>0</td><td>1</td><td>1 frame</td></tr><tr><td>0</td><td>1</td><td>0</td><td>2 frames</td></tr><tr><td>0</td><td>1</td><td>1</td><td>4 frames</td></tr><tr><td>1</td><td>0</td><td>0</td><td>8 frames</td></tr><tr><td>1</td><td>0</td><td>1</td><td>16 frames</td></tr><tr><td>1</td><td>1</td><td>0</td><td>32 frames</td></tr><tr><td>1</td><td>1</td><td>1</td><td>64 frames</td></tr></tbody></table> <p>Note1: As above picture DIM1[2:0] mean DIM_MOV[2:0] or DIM_STILL[2:0] or DIM_UI[2:0] in different mode.</p> <p>Note2: As above picture DIM2[3:0] mean DIM_MIN[3:0].</p> <p>DIM_MIN [3:0]: The parameter is used to set the imitation of minimum brightness change. If the parameter is large than the difference between target brightness and current brightness, then the brightness will not change.</p>													DIM_MOV[2:0]/DIM_STILL[2:0]			Description	D2	D1	D0	0	0	0	1 frame	0	0	1	1 frame	0	1	0	2 frames	0	1	1	4 frames	1	0	0	8 frames	1	0	1	16 frames	1	1	0	32 frames	1	1	1	64 frames
	DIM_MOV[2:0]/DIM_STILL[2:0]			Description																																																
	D2	D1	D0																																																	
	0	0	0	1 frame																																																
	0	0	1	1 frame																																																
	0	1	0	2 frames																																																
	0	1	1	4 frames																																																
	1	0	0	8 frames																																																
	1	0	1	16 frames																																																
	1	1	0	32 frames																																																
1	1	1	64 frames																																																	
Restriction																																																				
Register Availability	<table><thead><tr><th>Status</th><th>Availability</th></tr></thead><tbody><tr><td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr><tr><td>Normal Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr><tr><td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr><tr><td>Partial Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr><tr><td>Sleep IN</td><td>Yes</td></tr></tbody></table>													Status	Availability	Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes	Normal Mode ON, Idle Mode ON, Sleep OUT	Yes	Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes	Partial Mode ON, Idle Mode ON, Sleep OUT	Yes	Sleep IN	Yes																											
Status	Availability																																																			
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes																																																			
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes																																																			
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes																																																			
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes																																																			
Sleep IN	Yes																																																			
Default	<table><thead><tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr><tr><th>DIM_MIN[3:0]</th><th>DIM_UI[2:0]</th></tr></thead><tbody><tr><td>Power ON Sequence</td><td>4'b0000 b</td><td>3'b010 b</td></tr><tr><td>S/W Reset</td><td>4'b0000 b</td><td>3'b010 b</td></tr><tr><td>H/W Reset</td><td>4'b0000 b</td><td>3'b010 b</td></tr></tbody></table>													Status	Default Value		DIM_MIN[3:0]	DIM_UI[2:0]	Power ON Sequence	4'b0000 b	3'b010 b	S/W Reset	4'b0000 b	3'b010 b	H/W Reset	4'b0000 b	3'b010 b																									
Status	Default Value																																																			
	DIM_MIN[3:0]	DIM_UI[2:0]																																																		
Power ON Sequence	4'b0000 b	3'b010 b																																																		
S/W Reset	4'b0000 b	3'b010 b																																																		
H/W Reset	4'b0000 b	3'b010 b																																																		

8.2.72. CABC Control 9 (CFh)

CFh	CABCCTRL8 (CABC Control 8)																																																																																																																																									
	DCX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																																																																																													
Command	0	1	↑	XXXXXXXX	1	1	0	0	1	1	1	1	CFh																																																																																																																													
1 st Parameter	1	1	↑	XXXXXXXX	PWM_DIV[7:0]								XX																																																																																																																													
Description	PWM_DIV [7:0]: PWM_OUT output period control. This command is used to adjust the PWM waveform period of PWM_OUT. The PWM period can be calculated using the equation in the following.																																																																																																																																									
	$f_{\text{PWM_OUT}} = \frac{18\text{MHz}}{(\text{PWM_DIV}[7:0] + 1) \times 255}$																																																																																																																																									
	<table><tr><th colspan="8">PWM_DIV[7:0]</th><th rowspan="2">f_{PWM_OUT}</th></tr><tr><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>70.58 KHz</td></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>35.29 KHz</td></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>23.53 KHz</td></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>17.64 KHz</td></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>14.11KHz</td></tr><tr><td colspan="8">:</td><td>:</td></tr><tr><td colspan="8">:</td><td>:</td></tr><tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>280.0Hz</td></tr><tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>279.0 Hz</td></tr><tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>277.9 Hz</td></tr><tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>276.8 Hz</td></tr><tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>275.8 Hz</td></tr></table>													PWM_DIV[7:0]								f _{PWM_OUT}	D7	D6	D5	D4	D3	D2	D1	D0	0	0	0	0	0	0	0	0	70.58 KHz	0	0	0	0	0	0	0	1	35.29 KHz	0	0	0	0	0	0	1	0	23.53 KHz	0	0	0	0	0	0	1	1	17.64 KHz	0	0	0	0	0	1	0	0	14.11KHz	:								:	:								:	1	1	1	1	1	0	1	1	280.0Hz	1	1	1	1	1	1	0	0	279.0 Hz	1	1	1	1	1	1	0	1	277.9 Hz	1	1	1	1	1	1	1	0	276.8 Hz	1	1	1	1	1	1	1	1	275.8 Hz
	PWM_DIV[7:0]								f _{PWM_OUT}																																																																																																																																	
	D7	D6	D5	D4	D3	D2	D1	D0																																																																																																																																		
	0	0	0	0	0	0	0	0	70.58 KHz																																																																																																																																	
	0	0	0	0	0	0	0	1	35.29 KHz																																																																																																																																	
	0	0	0	0	0	0	1	0	23.53 KHz																																																																																																																																	
	0	0	0	0	0	0	1	1	17.64 KHz																																																																																																																																	
	0	0	0	0	0	1	0	0	14.11KHz																																																																																																																																	
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:								:																																																																																																																																		
1	1	1	1	1	0	1	1	280.0Hz																																																																																																																																		
1	1	1	1	1	1	0	0	279.0 Hz																																																																																																																																		
1	1	1	1	1	1	0	1	277.9 Hz																																																																																																																																		
1	1	1	1	1	1	1	0	276.8 Hz																																																																																																																																		
1	1	1	1	1	1	1	1	275.8 Hz																																																																																																																																		
<div><div>PWM_OUT</div><div><div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div></div><div><div>f_{PWM_OUT}</div><div>ton</div><div>toff</div></div></div><div>CABC ON</div></div>																																																																																																																																										
Note : The output frequency tolerance of internal frequency divider in CABC is ±10%																																																																																																																																										
Restriction	EXTC should be high to enable this command																																																																																																																																									
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr><tr><td>Normal Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr><tr><td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr><tr><td>Partial Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr><tr><td>Sleep IN</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes	Normal Mode ON, Idle Mode ON, Sleep OUT	Yes	Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes	Partial Mode ON, Idle Mode ON, Sleep OUT	Yes	Sleep IN	Yes																																																																																																																	
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Partial Mode ON, Idle Mode ON, Sleep OUT	Yes																																																																																																																																									
Sleep IN	Yes																																																																																																																																									
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power ON Sequence</td><td>8'b00011000</td></tr><tr><td>H/W Reset</td><td>8'b00011000</td></tr></table>													Status	Default Value	Power ON Sequence	8'b00011000	H/W Reset	8'b00011000																																																																																																																							
Status	Default Value																																																																																																																																									
Power ON Sequence	8'b00011000																																																																																																																																									
H/W Reset	8'b00011000																																																																																																																																									

8.2.73. NV Memory Write (D0h)

D0h	NVMWR (NV Memory Write)																																																																																										
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																																														
Command	0	1	↑	XXXXXXXX	1	1	0	1	0	0	0	0	D0h																																																																														
1 st Parameter	1	1	↑	XXXXXXXX	0	0	0	PGM_ADR[4:0]					XX																																																																														
2 nd Parameter	1	1	↑	XXXXXXXX	PGM_DATA[7:0]								XX																																																																														
Description	This command is used to program the NV memory data. After a successful OTP operation, the information of PGM_DATA [7:0] will programmed to NV memory.																																																																																										
	PGM_ADR [4:0]: The select bits of ID1, ID2, ID3, VMF[6:0] programming.																																																																																										
	<table><tr><th colspan="5">PGM_ADR[4:0]</th><th colspan="8">Programmed NV Memory Selection</th></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td colspan="8">ID1 programming</td></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td colspan="8">ID2 programming</td></tr><tr><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td colspan="8">ID3 programming</td></tr><tr><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td colspan="8">VMF[6:0] programming</td></tr><tr><td colspan="5">Others</td><td colspan="8">Reserved</td></tr></table>													PGM_ADR[4:0]					Programmed NV Memory Selection								0	0	0	0	0	ID1 programming								0	0	0	0	1	ID2 programming								0	0	0	1	0	ID3 programming								0	0	0	1	1	VMF[6:0] programming								Others					Reserved							
	PGM_ADR[4:0]					Programmed NV Memory Selection																																																																																					
	0	0	0	0	0	ID1 programming																																																																																					
	0	0	0	0	1	ID2 programming																																																																																					
0	0	0	1	0	ID3 programming																																																																																						
0	0	0	1	1	VMF[6:0] programming																																																																																						
Others					Reserved																																																																																						
PGM_DATA [7:0]: The PGM_DATA is set by user.																																																																																											
Restriction																																																																																											
Register Availability																																																																																											
	<table><tr><th colspan="8">Status</th><th colspan="5">Availability</th></tr><tr><td colspan="8">Normal Mode ON, Idle Mode OFF, Sleep OUT</td><td colspan="5">Yes</td></tr><tr><td colspan="8">Normal Mode ON, Idle Mode ON, Sleep OUT</td><td colspan="5">Yes</td></tr><tr><td colspan="8">Partial Mode ON, Idle Mode OFF, Sleep OUT</td><td colspan="5">Yes</td></tr><tr><td colspan="8">Partial Mode ON, Idle Mode ON, Sleep OUT</td><td colspan="5">Yes</td></tr><tr><td colspan="8">Sleep IN</td><td colspan="5">Yes</td></tr></table>													Status								Availability					Normal Mode ON, Idle Mode OFF, Sleep OUT								Yes					Normal Mode ON, Idle Mode ON, Sleep OUT								Yes					Partial Mode ON, Idle Mode OFF, Sleep OUT								Yes					Partial Mode ON, Idle Mode ON, Sleep OUT								Yes					Sleep IN								Yes				
	Status								Availability																																																																																		
	Normal Mode ON, Idle Mode OFF, Sleep OUT								Yes																																																																																		
	Normal Mode ON, Idle Mode ON, Sleep OUT								Yes																																																																																		
	Partial Mode ON, Idle Mode OFF, Sleep OUT								Yes																																																																																		
Partial Mode ON, Idle Mode ON, Sleep OUT								Yes																																																																																			
Sleep IN								Yes																																																																																			
Default																																																																																											
	<table><tr><th rowspan="2">Status</th><th colspan="12">Default Value</th></tr><tr><th colspan="5">PGM_ADR[4:0]</th><th colspan="7">PGM_DATA[7:0]</th></tr><tr><td colspan="5">Power ON Sequence</td><td colspan="5">3'b000000</td><td colspan="7">8'bXXXXXXXXXX</td></tr><tr><td colspan="5">H/W Reset</td><td colspan="5">3'b000000</td><td colspan="7">8'bXXXXXXXXXX</td></tr></table>													Status	Default Value												PGM_ADR[4:0]					PGM_DATA[7:0]							Power ON Sequence					3'b000000					8'bXXXXXXXXXX							H/W Reset					3'b000000					8'bXXXXXXXXXX																									
	Status	Default Value																																																																																									
		PGM_ADR[4:0]					PGM_DATA[7:0]																																																																																				
Power ON Sequence					3'b000000					8'bXXXXXXXXXX																																																																																	
H/W Reset					3'b000000					8'bXXXXXXXXXX																																																																																	

8.2.74. NV Memory Protection Key (D1h)

D1h	NVMPKEY (NV Memory Protection Key)																								
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XXXXXXXX	1	1	0	1	0	0	0	1	D1h												
1 st Parameter	1	1	↑	XXXXXXXX	KEY[23:16]								55h												
2 nd Parameter	1	1	↑	XXXXXXXX	KEY[15:8]								AAh												
3 rd Parameter	1	1	↑	XXXXXXXX	KEY[7:0]								66h												
Description	KEY [23:0]: NV memory programming protection key. When writing OTP data to D0h, this register must be set to 0x55AA66h to enable OTP programming. If D1h register is not written with 0x55AA66h, then NV memory programming will be aborted.																								
Restriction																									
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr><tr><td>Normal Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr><tr><td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr><tr><td>Partial Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr><tr><td>Sleep IN</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes	Normal Mode ON, Idle Mode ON, Sleep OUT	Yes	Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes	Partial Mode ON, Idle Mode ON, Sleep OUT	Yes	Sleep IN	Yes
Status	Availability																								
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes																								
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes																								
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes																								
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes																								
Sleep IN	Yes																								
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power ON Sequence</td><td>24'h55AA66h</td></tr><tr><td>H/W Reset</td><td>24'h55AA66h</td></tr></table>													Status	Default Value	Power ON Sequence	24'h55AA66h	H/W Reset	24'h55AA66h						
Status	Default Value																								
Power ON Sequence	24'h55AA66h																								
H/W Reset	24'h55AA66h																								

8.2.75. NV Memory Status Read (D2h)

D2h	RDNVM (NV Memory Status Read)																																											
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX																															
Command	0	1	↑	XXXXXXXX	1	1	0	1	0	0	1	0	D2h																															
1 st Parameter	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX																															
2 nd Parameter	1	↑	1	XXXXXXXX	ID2_CNT[3:0]				ID1_CNT[3:0]				XX																															
3 rd Parameter	1	↑	1	XXXXXXXX	VMF_CNT[3:0]				ID3_CNT[3:0]				XX																															
4 th Parameter	1	↑	1	XXXXXXXX	BUSY	0	0	0	0	0	0	0	XX																															
Description	PGM_CNT [1:0]: NV memory program record. The bits will increase “+1” automatically after writing the NV_VMF [5:0] to NV memory.																																											
	<table><tr><th colspan="4">ID1_CNT[3:0]/ID2_CNT[3:0] / ID3_CNT[3:0] / VMF_CNT[3:0]</th><th>Description</th></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>No Programmed</td></tr><tr><td>0</td><td>0</td><td>0</td><td>1</td><td>Programmed 1 time</td></tr><tr><td>0</td><td>0</td><td>1</td><td>1</td><td>Programmed 2 times</td></tr><tr><td>0</td><td>1</td><td>1</td><td>1</td><td>Programmed 3 times</td></tr><tr><td>1</td><td>1</td><td>1</td><td>1</td><td>Programmed 4 times</td></tr></table>													ID1_CNT[3:0]/ID2_CNT[3:0] / ID3_CNT[3:0] / VMF_CNT[3:0]				Description	0	0	0	0	No Programmed	0	0	0	1	Programmed 1 time	0	0	1	1	Programmed 2 times	0	1	1	1	Programmed 3 times	1	1	1	1	Programmed 4 times	
	ID1_CNT[3:0]/ID2_CNT[3:0] / ID3_CNT[3:0] / VMF_CNT[3:0]				Description																																							
	0	0	0	0	No Programmed																																							
	0	0	0	1	Programmed 1 time																																							
	0	0	1	1	Programmed 2 times																																							
	0	1	1	1	Programmed 3 times																																							
	1	1	1	1	Programmed 4 times																																							
	BUSY: The status bit of NV memory programming.																																											
	<table><tr><th>BUSY</th><th>The Status of NV Memory</th></tr><tr><td>0</td><td>Idle</td></tr><tr><td>1</td><td>Busy</td></tr></table>													BUSY	The Status of NV Memory	0	Idle	1	Busy																									
BUSY	The Status of NV Memory																																											
0	Idle																																											
1	Busy																																											
Restriction																																												
Register Availability																																												
	<table><tr><th colspan="2">Status</th><th>Availability</th></tr><tr><td colspan="2">Normal Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr><tr><td colspan="2">Normal Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr><tr><td colspan="2">Partial Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr><tr><td colspan="2">Partial Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr><tr><td colspan="2">Sleep IN</td><td>Yes</td></tr></table>													Status		Availability	Normal Mode ON, Idle Mode OFF, Sleep OUT		Yes	Normal Mode ON, Idle Mode ON, Sleep OUT		Yes	Partial Mode ON, Idle Mode OFF, Sleep OUT		Yes	Partial Mode ON, Idle Mode ON, Sleep OUT		Yes	Sleep IN		Yes													
	Status		Availability																																									
	Normal Mode ON, Idle Mode OFF, Sleep OUT		Yes																																									
	Normal Mode ON, Idle Mode ON, Sleep OUT		Yes																																									
	Partial Mode ON, Idle Mode OFF, Sleep OUT		Yes																																									
	Partial Mode ON, Idle Mode ON, Sleep OUT		Yes																																									
Sleep IN		Yes																																										
Default																																												
	<table><tr><th rowspan="2">Status</th><th colspan="7">Default Value</th></tr><tr><th></th><th>ID3_CNT</th><th>ID2_CNT</th><th>ID1_CNT</th><th>VMF_CNT</th><th>BUSY</th><th>OTP_DATA</th></tr><tr><td>Power ON Sequence</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr><tr><td>H/W Reset</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr></table>													Status	Default Value								ID3_CNT	ID2_CNT	ID1_CNT	VMF_CNT	BUSY	OTP_DATA	Power ON Sequence	X	X	X	X	X	X	X	H/W Reset	X	X	X	X	X	X	X
	Status	Default Value																																										
			ID3_CNT	ID2_CNT	ID1_CNT	VMF_CNT	BUSY	OTP_DATA																																				
	Power ON Sequence	X	X	X	X	X	X	X																																				
H/W Reset	X	X	X	X	X	X	X																																					

8.2.76. Read ID4 (D3h)

D3h	RDID4 (Read ID4)												
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	1	1	0	1	0	0	1	1	D3h
1 st Parameter	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX
2 nd Parameter	1	↑	1	XXXXXXXX	0	0	0	0	0	0	0	0	00h
3 rd Parameter	1	↑	1	XXXXXXXX	1	0	0	1	0	1	0	0	94h
4 th Parameter	1	↑	1	XXXXXXXX	1	0	0	0	0	0	1	0	86h
Description	Read IC device code.												
	The 1 st parameter is dummy read period.												
	The 2 nd parameter means the IC version.												
	The 3 rd and 4 th parameter mean the IC model name.												
Restriction													
Register Availability													
Default													

8.2.77. PGAMCTRL(Positive Gamma Control) (E0h)

	PGAMCTRL (Positive Gamma Control)																								
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XXXXXXXX	1	1	1	0	0	0	0	0	E0h												
1 st Parameter	1	1	↑	XXXXXXXX	0	0	0	VP0[4:0]					XX												
2 nd Parameter	1	1	↑	XXXXXXXX	0	0	VP1[5:0]					XX													
3 rd Parameter	1	1	↑	XXXXXXXX	0	0	VP2[5:0]					XX													
4 th Parameter	1	1	↑	XXXXXXXX	0	0	0	0	VP4[3:0]				XX												
5 th Parameter	1	1	↑	XXXXXXXX	0	0	0	VP6[4:0]				XX													
6 th Parameter	1	1	↑	XXXXXXXX	0	0	0	0	VP13[3:0]				XX												
7 th Parameter	1	1	↑	XXXXXXXX	0	VP20[6:0]					XX														
8 th Parameter	1	1	↑	XXXXXXXX	VP36[3:0]				VP27[3:0]				XX												
9 th Parameter	1	1	↑	XXXXXXXX	0	VP43[6:0]					XX														
10 th Parameter	1	1	↑	XXXXXXXX	0	0	0	0	VP50[3:0]				XX												
11 th Parameter	1	1	↑	XXXXXXXX	0	0	0	VP57[4:0]				XX													
12 th Parameter	1	1	↑	XXXXXXXX	0	0	0	0	VP59[3:0]				XX												
13 th Parameter	1	1	↑	XXXXXXXX	0	0	VP61[5:0]					XX													
14 th Parameter	1	1	↑	XXXXXXXX	0	0	VP62[5:0]					XX													
15 th Parameter	1	1	↑	XXXXXXXX	0	0	0	VP63[4:0]					XX												
Description	Set the gray scale voltage to adjust the gamma characteristics of the TFT panel.																								
Restriction																									
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr><tr><td>Normal Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr><tr><td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr><tr><td>Partial Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr><tr><td>Sleep IN</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes	Normal Mode ON, Idle Mode ON, Sleep OUT	Yes	Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes	Partial Mode ON, Idle Mode ON, Sleep OUT	Yes	Sleep IN	Yes
Status	Availability																								
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes																								
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes																								
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes																								
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes																								
Sleep IN	Yes																								

8.2.78. NGAMCTRL (Negative Gamma Correction) (E1h)

	NGAMCTRL (Negative Gamma Correction)																								
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XXXXXXXX	1	1	1	0	0	0	0	1	E1h												
1 st Parameter	1	1	↑	XXXXXXXX	0	0	0	VN0[4:0]					XX												
2 nd Parameter	1	1	↑	XXXXXXXX	0	0	VN1[5:0]					XX													
3 rd Parameter	1	1	↑	XXXXXXXX	0	0	VN2[5:0]					XX													
4 th Parameter	1	1	↑	XXXXXXXX	0	0	0	0	VN4[3:0]				XX												
5 th Parameter	1	1	↑	XXXXXXXX	0	0	0	RVN6[4:0]					XX												
6 th Parameter	1	1	↑	XXXXXXXX	0	0	0	0	VN13[3:0]				XX												
7 th Parameter	1	1	↑	XXXXXXXX	0	VN20[6:0]					XX														
8 th Parameter	1	1	↑	XXXXXXXX	VN36[3:0]				VN27[3:0]				XX												
9 th Parameter	1	1	↑	XXXXXXXX	0	VN43[6:0]							XX												
10 th Parameter	1	1	↑	XXXXXXXX	0	0	0	0	VN50[3:0]				XX												
11 th Parameter	1	1	↑	XXXXXXXX	0	0	0	VN57[4:0]					XX												
12 th Parameter	1	1	↑	XXXXXXXX	0	0	0	0	VN59[3:0]				XX												
13 th Parameter	1	1	↑	XXXXXXXX	0	0	VN61[5:0]					XX													
14 th Parameter	1	1	↑	XXXXXXXX	0	0	VN62[5:0]					XX													
15 th Parameter	1	1	↑	XXXXXXXX	0	0	0	VN63[4:0]					XX												
Description	Set the gray scale voltage to adjust the gamma characteristics of the TFT panel.																								
Restriction																									
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr><tr><td>Normal Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr><tr><td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr><tr><td>Partial Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr><tr><td>Sleep IN</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes	Normal Mode ON, Idle Mode ON, Sleep OUT	Yes	Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes	Partial Mode ON, Idle Mode ON, Sleep OUT	Yes	Sleep IN	Yes
Status	Availability																								
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes																								
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes																								
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes																								
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes																								
Sleep IN	Yes																								

8.2.79. Digital Gamma Control 1 (E2h)

E2h	DGAMCTRL (Digital Gamma Control 1)																								
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XXXXXXXX	1	1	1	0	0	0	1	0	E2h												
1 st Parameter	1	1	↑	XXXXXXXX	RCA0[3:0]				BCA0[3:0]				XX												
:	1	1	↑	XXXXXXXX	RCAx[3:0]				BCAx[3:0]				XX												
16 rd Parameter	1	1	↑	XXXXXXXX	RCA15[3:0]				BCA15[3:0]				XX												
Description	RCAx [3:0]: Gamma Macro-adjustment registers for red gamma curve. BCAx [3:0]: Gamma Macro-adjustment registers for blue gamma curve.																								
Restriction																									
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr><tr><td>Normal Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr><tr><td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr><tr><td>Partial Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr><tr><td>Sleep IN</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes	Normal Mode ON, Idle Mode ON, Sleep OUT	Yes	Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes	Partial Mode ON, Idle Mode ON, Sleep OUT	Yes	Sleep IN	Yes
Status	Availability																								
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes																								
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes																								
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes																								
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes																								
Sleep IN	Yes																								
Default	<table><tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr><tr><th>RCAx[3:0]</th><th>BCAx[3:0]</th></tr><tr><td>Power ON Sequence</td><td>TBD</td><td>TBD</td></tr><tr><td>H/W Reset</td><td>TBD</td><td>TBD</td></tr></table>													Status	Default Value		RCAx[3:0]	BCAx[3:0]	Power ON Sequence	TBD	TBD	H/W Reset	TBD	TBD	
Status	Default Value																								
	RCAx[3:0]	BCAx[3:0]																							
Power ON Sequence	TBD	TBD																							
H/W Reset	TBD	TBD																							

8.2.80. Digital Gamma Control 2 (E3h)

E3h	DGAMCTRL (Digital Gamma Control 2)																								
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XXXXXXXX	1	1	1	0	0	0	1	1	E3h												
1 st Parameter	1	1	↑	XXXXXXXX	RFA0[3:0]				BFA0[3:0]				XX												
:	1	1	↑	XXXXXXXX	RFAx[3:0]				BFAx[3:0]				XX												
64 rd Parameter	1	1	↑	XXXXXXXX	RFA63[3:0]				BFA63[3:0]				XX												
Description	RFax [3:0]: Gamma Micro-adjustment register for red gamma curve. BFAx [3:0]: Gamma Micro-adjustment register for blue gamma curve.																								
Restriction																									
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr><tr><td>Normal Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr><tr><td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr><tr><td>Partial Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr><tr><td>Sleep IN</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes	Normal Mode ON, Idle Mode ON, Sleep OUT	Yes	Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes	Partial Mode ON, Idle Mode ON, Sleep OUT	Yes	Sleep IN	Yes
Status	Availability																								
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes																								
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes																								
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes																								
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes																								
Sleep IN	Yes																								
Default	<table><tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr><tr><th>RFax[3:0]</th><th>BFAx[3:0]</th></tr><tr><td>Power ON Sequence</td><td>TBD</td><td>TBD</td></tr><tr><td>H/W Reset</td><td>TBD</td><td>TBD</td></tr></table>													Status	Default Value		RFax[3:0]	BFAx[3:0]	Power ON Sequence	TBD	TBD	H/W Reset	TBD	TBD	
Status	Default Value																								
	RFax[3:0]	BFAx[3:0]																							
Power ON Sequence	TBD	TBD																							
H/W Reset	TBD	TBD																							

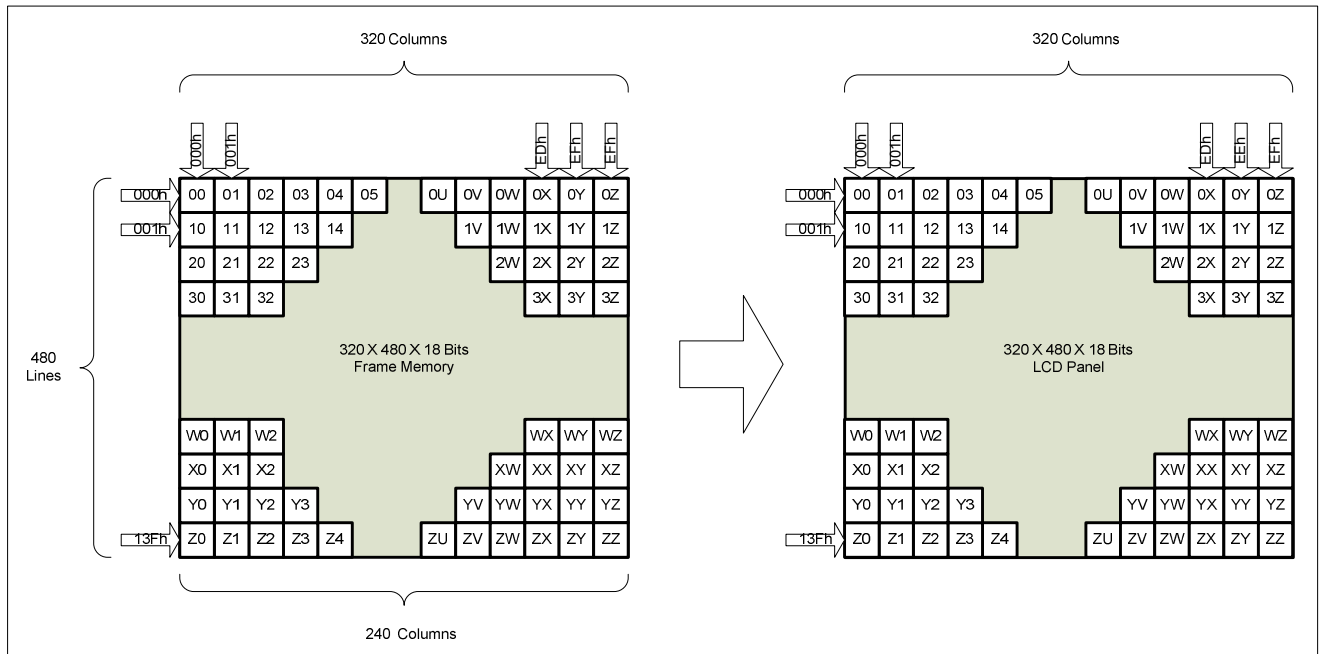
8.2.81. SPI Read Command Setting(FBh)

FBh	DGAMCTRL (Digital Gamma Control 2)																								
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XXXXXXXX	1	1	1	1	1	0	1	1	FBh												
1 st Parameter	1	1	↑	XXXXXXXX	0	0	0	SPI_READ_EN	SPI_CNT[3:0]			XX													
Description	SPI_READ_EN: SPI read enable (see note). SPI_CNT [3:0]: SPI read parameter number (see note) <i>Note: Set “RFBh” once only usefull to read one parameter of register one time, the next read need to set “RFBh” again.</i>																								
Restriction																									
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr><tr><td>Normal Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr><tr><td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr><tr><td>Partial Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr><tr><td>Sleep IN</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes	Normal Mode ON, Idle Mode ON, Sleep OUT	Yes	Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes	Partial Mode ON, Idle Mode ON, Sleep OUT	Yes	Sleep IN	Yes
Status	Availability																								
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes																								
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes																								
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes																								
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes																								
Sleep IN	Yes																								
Default	<table><tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr><tr><th>SPI_READ_EN</th><th>SPI_CNT[3:0]</th></tr><tr><td>Power ON Sequence</td><td>1'b0</td><td>4'b0000</td></tr><tr><td>H/W Reset</td><td>1'b0</td><td>4'b0000</td></tr></table>													Status	Default Value		SPI_READ_EN	SPI_CNT[3:0]	Power ON Sequence	1'b0	4'b0000	H/W Reset	1'b0	4'b0000	
Status	Default Value																								
	SPI_READ_EN	SPI_CNT[3:0]																							
Power ON Sequence	1'b0	4'b0000																							
H/W Reset	1'b0	4'b0000																							

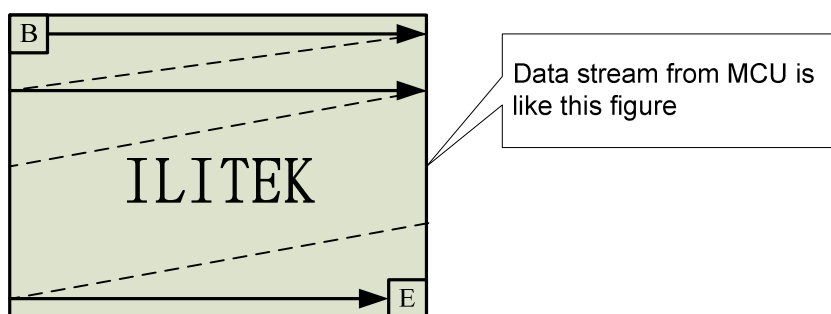
9.2. Memory to Display Address Mapping

In this mode, the content of the frame memory within an area where column pointer is 0000h to 013Fh and page pointer is 0000h to 01DFh is displayed.

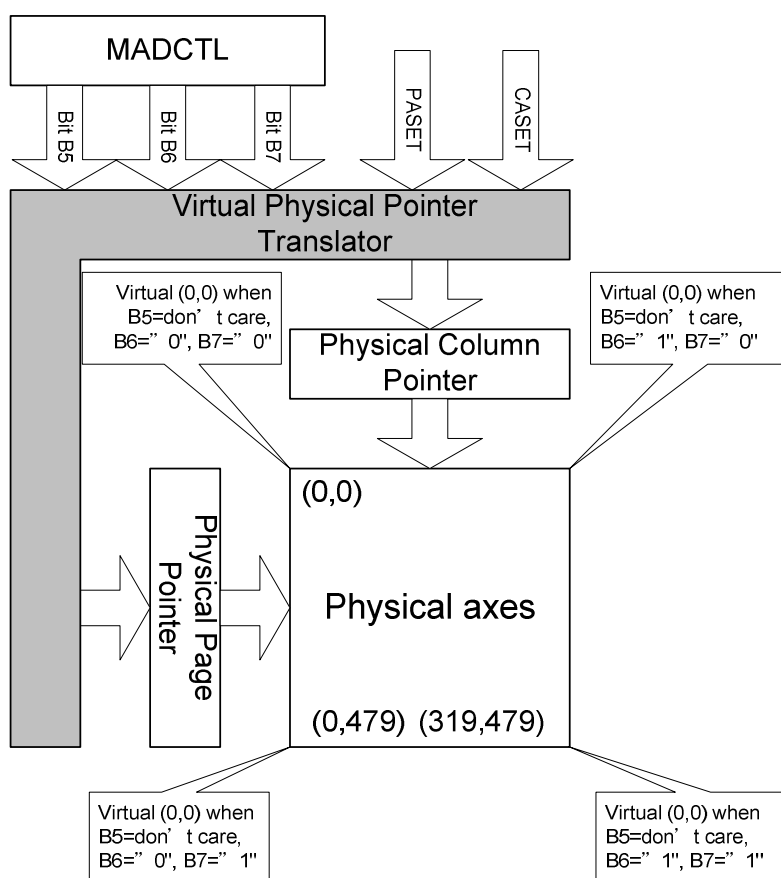
To display a dot on leftmost top corner, store the dot data at (column pointer, page pointer) = (0,0)



9.3. MCU to memory write/read direction



The data is written in the order illustrated above. The Counter which dictates where in the physical memory the data is to be written is controlled by "Memory Data Access Control" Command, Bits B5, B6, and B7 as described below.



B5	B6	B7	CASET	PASET
0	0	0	Direct to Physical Column Pointer	Direct to Physical Page Pointer
0	0	1	Direct to Physical Column Pointer	Direct to (479-Physical Page Pointer)
0	1	0	Direct to (319-Physical Column Pointer)	Direct to Physical Page Pointer
0	1	1	Direct to (319-Physical Column Pointer)	Direct to (479-Physical Page Pointer)
1	0	0	Direct to Physical Page Pointer	Direct to Physical Column Pointer
1	0	1	Direct to (479-Physical Page Pointer)	Direct to Physical Column Pointer
1	1	0	Direct to Physical Page Pointer	Direct to (319-Physical Column Pointer)
1	1	1	Direct to (479-Physical Page Pointer)	Direct to (319-Physical Column Pointer)

Condition	Column Counter	Page counter
When RAMWR/RAMRD command is accepted	Return to "Start column"	Return to "Start Page"
Complete Pixel Read/Write action	Increment by 1	No change
The Column values is large than "End Column"	Return to "Start column"	Increment by 1
The Page counter is large than "End Page"	Return to "Start column"	Return to "Start Page"

Note: Data is always written to the Frame Memory in the same order, regardless of the Memory Write Direction set by MADCTL bits B7, B6 and B5.

The write order for each pixel unit is

D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

One pixel unit represents 1 column and 1 page counter value on the Frame Memory.

Display Data Direction	MADCTR Parameter			Image in the Memory (MPU)	Image in the Driver (Frame Memory)
	MV	MX	MY		
Normal	0	0	0		
Y-Mirror	0	0	1		
X-Mirror	0	1	0		
X-Mirror Y-Mirror	0	1	1		
X-Y Exchange	1	0	0		
X-Y Exchange Y-Mirror	1	0	1		
XY Exchange X-Mirror	1	1	0		
XY Exchange X-YMirror	1	1	1		

10. Tearing Effect Information

The Tearing Effect output supplies to the MCU a Panel synchronization information (= Tearing Effect Information) which is telling the position of the refreshing on the display panel, to the MCU which can decide when it can send image information to ILI9486L (Mainly used for a moving image e.g. video clips) that there can avoid the abnormal visual effect on the display panel of ILI9486L.

This information can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect Signal is defined by the parameter of the Tearing Effect Line Off & On commands.

This Tearing Effect information can be sent in two different ways:

- Separated Line, which is so-called Tearing Effect (TE) line.
- Bus, which is so-called Tearing Effect (TEE) Bus Trigger, when ILI9486L is sending a trigger to the MCU.

The TE line is used in MCU parallel interface. The TE line can also be used in DSI case if the tearing Effect (TEE) Bus Trigger is not possible to use. The Tearing Effect (TEE) Bus Trigger is only used in DSI case.

10.1. Tearing Effect Line

10.1.1. Tearing Effect Line Modes

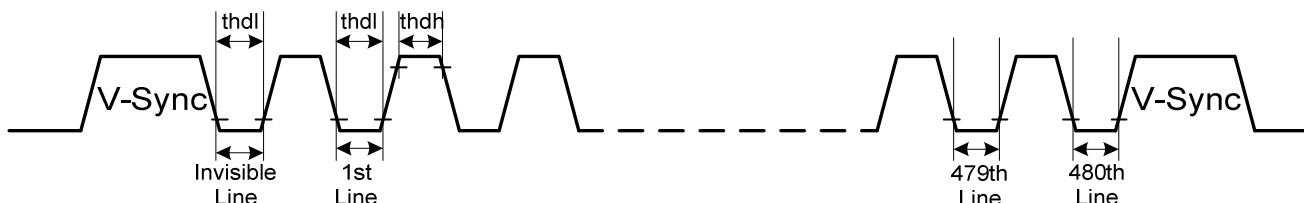
Mode 1, the Tearing Effect Output signal consists of V-Sync information only:



tvdh = The LCD display is not updated from the Frame Memory.

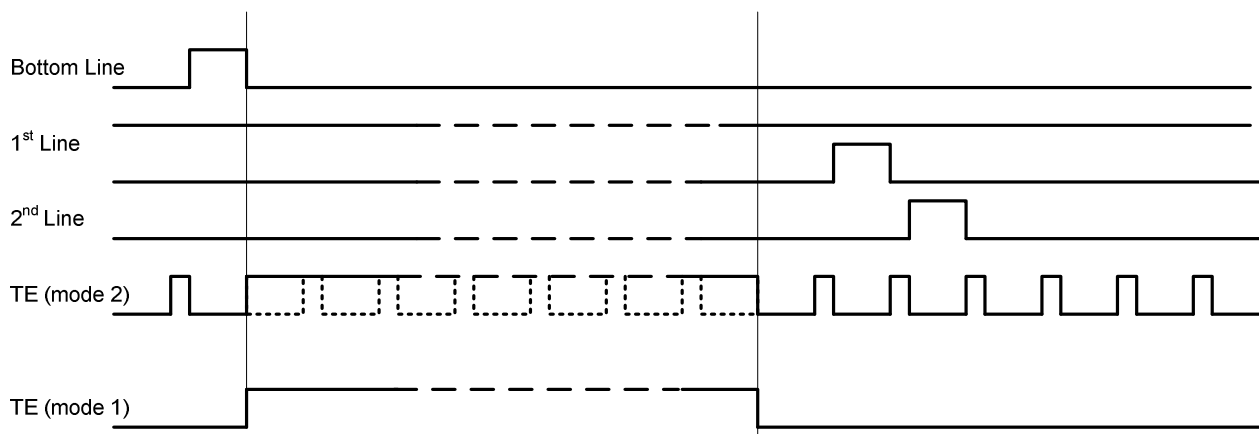
tvdI = The LCD display is updated from the Frame Memory (except Invisible Line – see below).

Mode 2, the tearing effect output signal consists of V-Sync and H-Sync information; there is one V-sync and 480 H-sync pulses per field:



thdh = The LCD display is not updated from the Frame Memory.

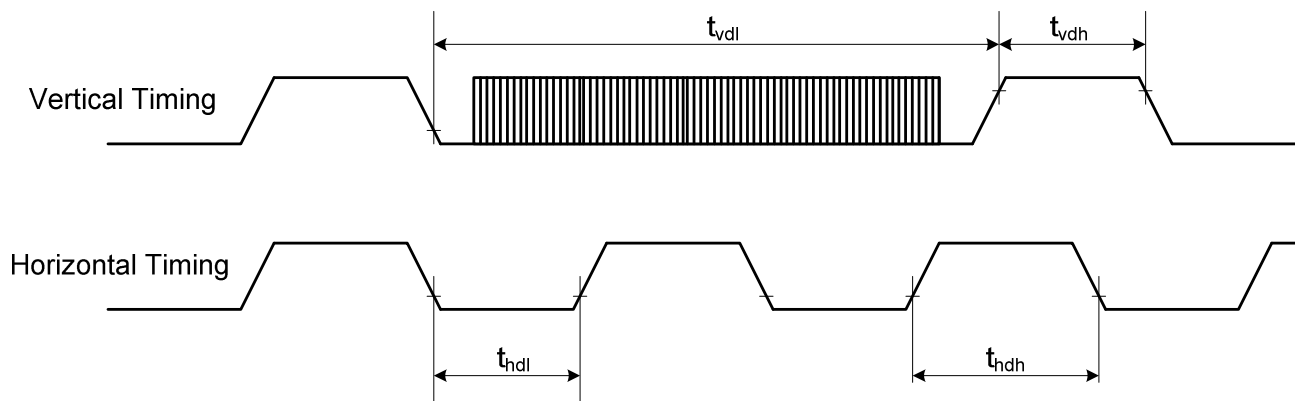
thdI = The LCD display is updated from the Frame Memory (except Invisible Line – see above).



Note: During Sleep In Mode, the Tearing Effect Output Pin is active Low.

10.1.2. Tearing Effect Line Timing

The tearing effect signal is described below:



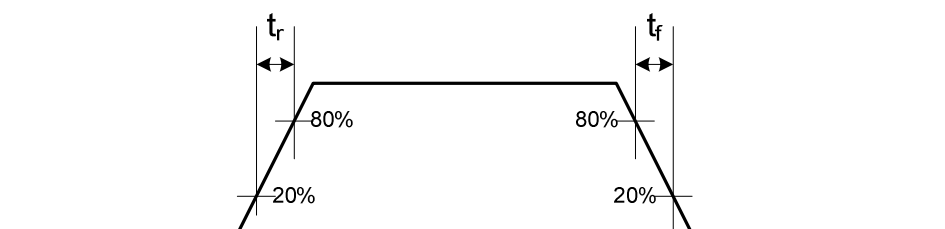
AC characteristics of Tearing Effect Signal (Frame Rate = 60.5Hz)

Symbol	Parameter	Min.	Max.	Unit	Description
t_{vdl}	Vertical timing low duration	TBD	TBD	ms	
t_{vdh}	Vertical timing high duration	1000	TBD	us	
t_{hdl}	Horizontal timing low duration	TBD	TBD	us	
t_{hdh}	Horizontal timing high duration	TBD	500	us	

Notes: 1. The timings in Table as above apply when MADCTL B4=0 and B4=1

2. Minimum frequency of the TE-line can not be less than 25Hz when the TE-line is active on Mode 1.

3. The signal's rise and fall times (t_f , t_r) are stipulated to be equal to or less than 15ns.



The Tearing Effect Output Line is fed back to the MCU and should be used to avoid Tearing Effect.

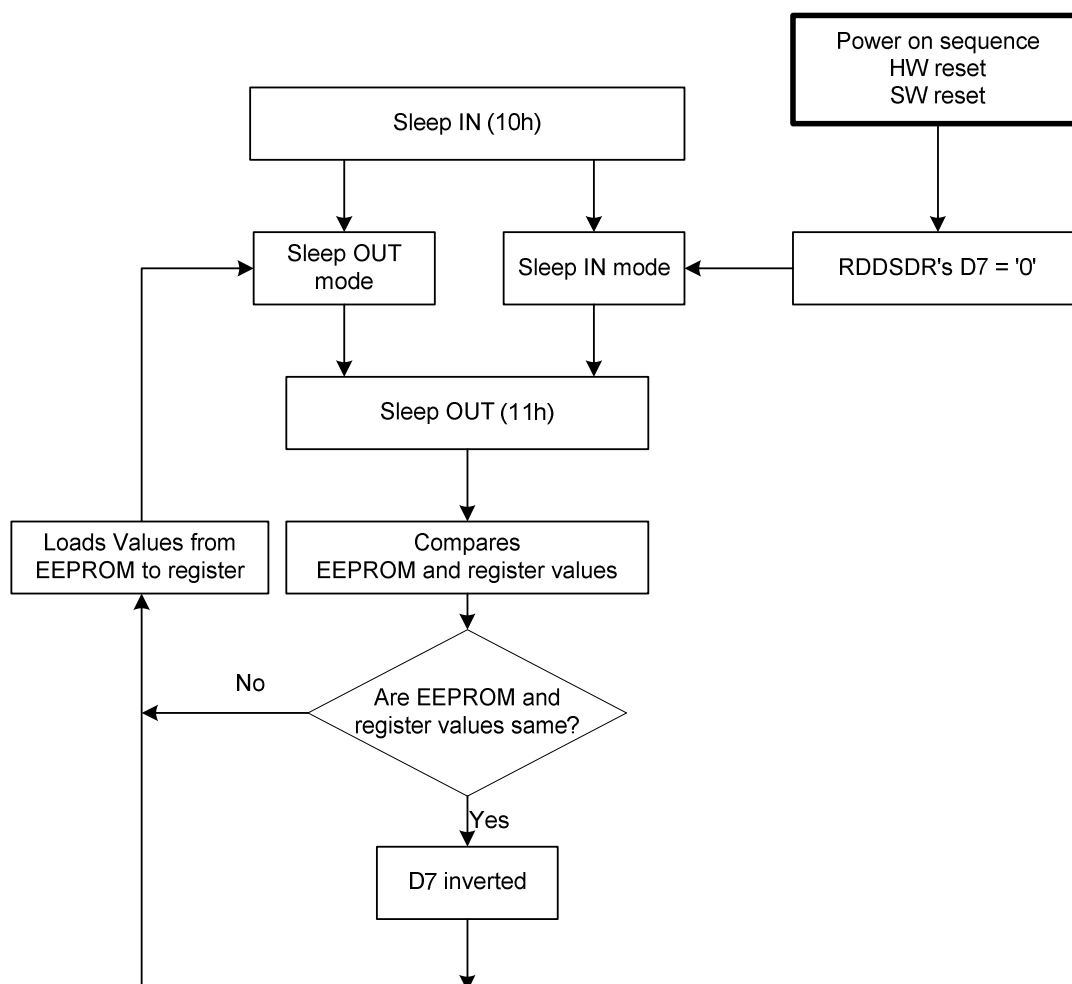
11. Sleep Out – Command and Self-Diagnostic Functions

11.1. Register loading Detection

Sleep Out-command (Command “Sleep Out (11h)”) is a trigger for an internal function of ILI9486L, which indicates, if ILI9486L loading function of factory default values from EEPROM (or similar device) to registers of the display controller is working properly.

There are compared factory values of the EEPROM and register values of the display controller by the display controller (1st step: compares register and EEPROM values, 2nd step: loads EEPROM values to registers). If those both values (EEPROM and register values) are same, there is inverted (= increased by 1) a bit, which is defined in command “Read Display Self-Diagnostic Result (0Fh)” (= RDDSDR) (The used bit of this command is D7). If those both values are not same, this bit (D7) is not inverted (= not increased by 1).

The flow chart for this internal function is following:



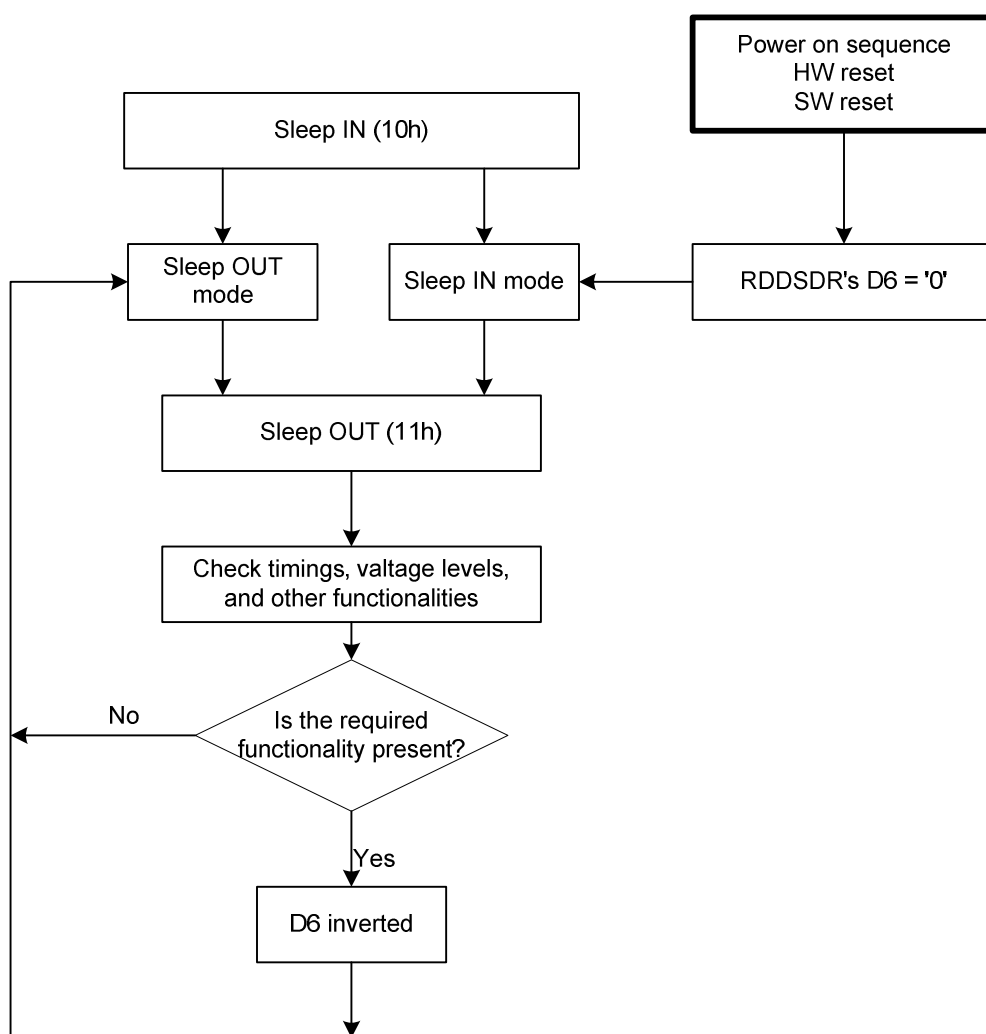
Note 1: There is not compared and loaded register values, which can be changed by User (User area commands: 00h to AFh and DAh to DDh), by ILI9486L.

11.2. Functionality Detection

Sleep Out-command (Command "Sleep Out (11h)") is a trigger for an internal function of ILI9486L, which indicates, if ILI9486L is still running and meets functionality requirements.

The internal function (= the display controller) is comparing, if ILI9486L is still meeting functionality requirements (e.g. booster voltage levels, timings, etc.) If functionality requirement is met, there is an inverted (= increased by 1) bit, which defined in command "Read Display Self- Diagnostic Result (0Fh)" (= RDDSDR) (The used bit of this command is D6). If functionality requirement is not same, this bit (D6) is not inverted (= increased by 1). The flow chart for this internal function is shown as below.

The flow chart for this internal function is following:



Note 1: There is needed 120msec after Sleep Out -command, when there is changing from Sleep In -mode to Sleep Out -mode, before there is possible to check if User's functionality requirements are met and a value of RDDSDR's D6 is valid. Otherwise, there is 5msec delay for D6's value, when Sleep Out -command is sent in Sleep Out -mode.

12. Power ON/OFF Sequence

IOVCC and VCI can be applied in any order. VCI and IOVCC can be powered down in any order. During power off, if LCD is in the Sleep Out mode, VCI and IOVCC must be powered down minimum 120msec after RESX has been released.

During power off, if LCD is in the Sleep In mode, IOVCC or VCI can be powered down minimum 0msec after RESX has been released.

Note 1: There will be no damage to ILI9486L if the power sequences are not met.

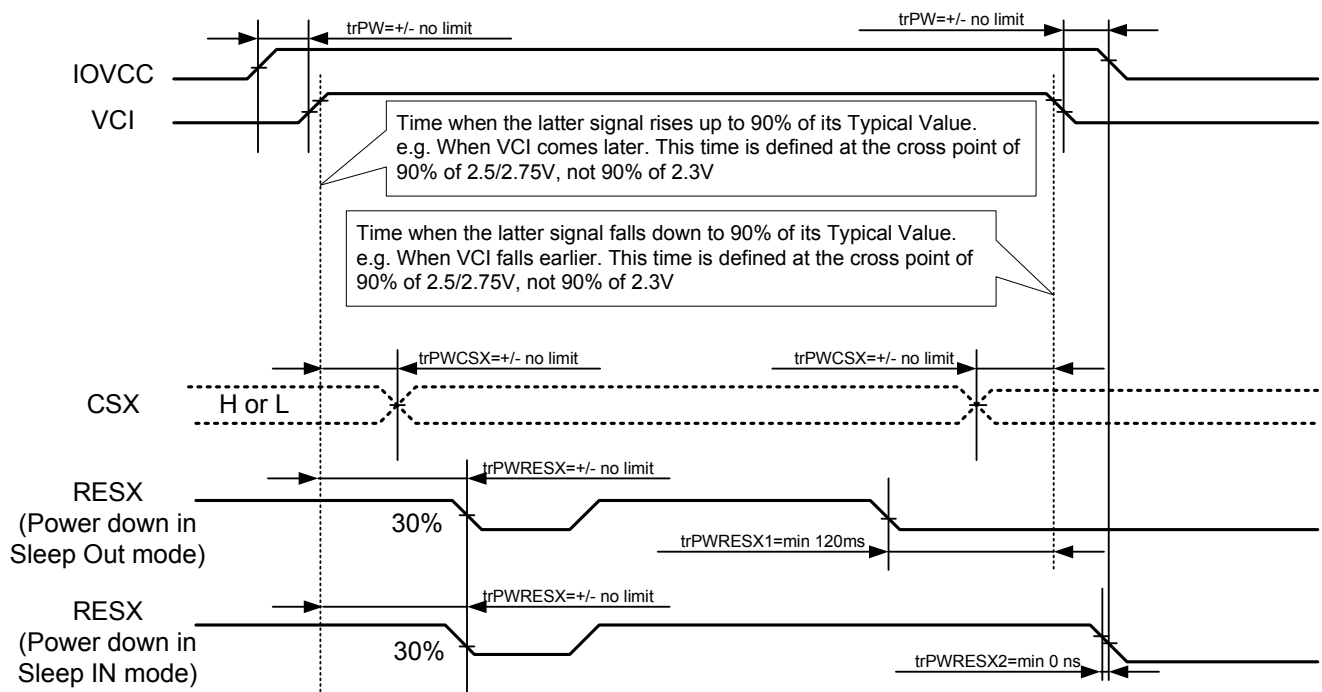
Note 2: There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.

Note 3: There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence.

Note 4: If RESX line is not held stable by host during Power On Sequence as defined in Sections 12.1 and 12.2, then it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.

12.1. Case 1 – RESX line is held High or Unstable by Host at Power ON

If RESX line is held High or unstable by the host during Power On, then a Hardware Reset must be applied after both VCI and IOVCC have been applied – otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.

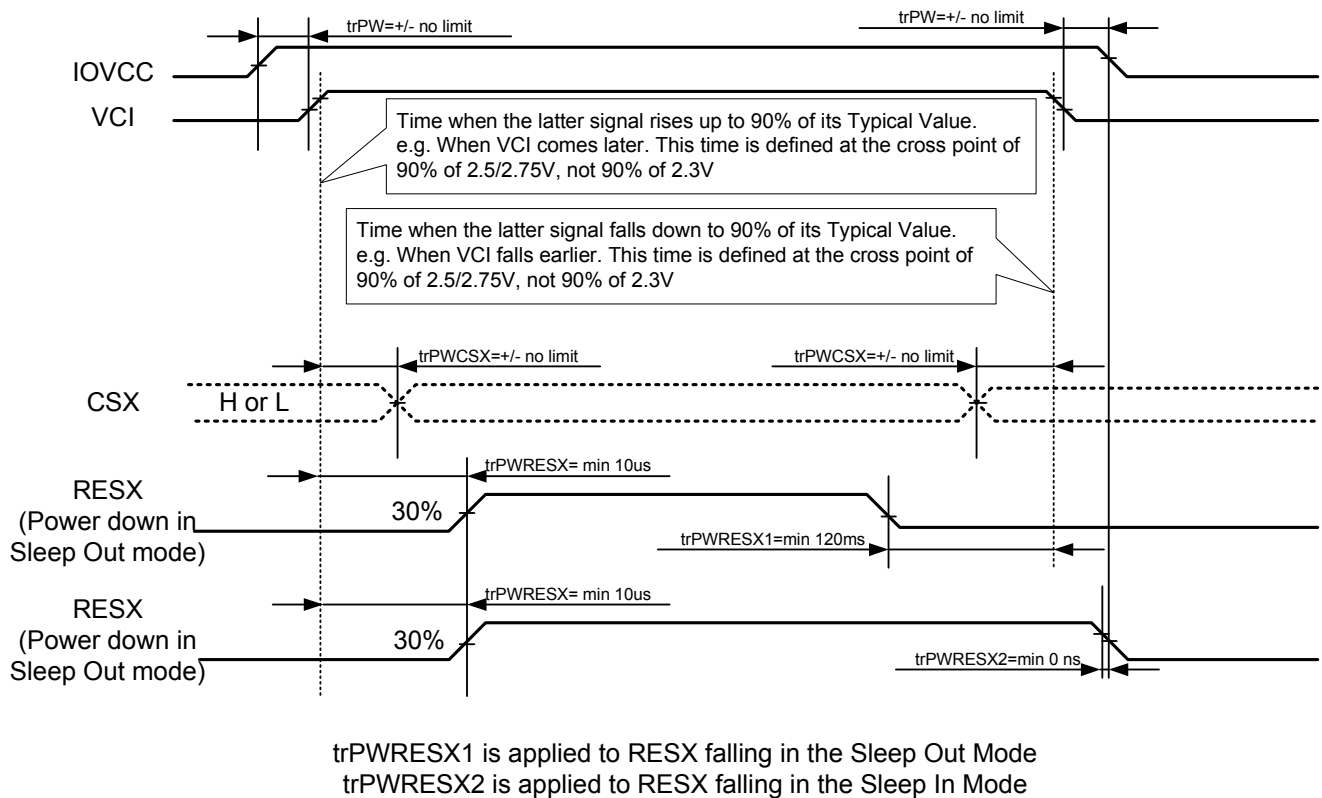


Note 1: Unless otherwise specified, timings herein show cross point at 50% of signal power level.

12.2. Case 2 – RESX line is held Low by Host at Power ON

If RESX line is held Low (and stable) by the host during Power On, then the RESX must be held low for minimum

10μsec after both VCI and IOVCC have been applied.



Note 1: Unless otherwise specified, timings herein show cross point at 50% of signal power level.

12.3. Uncontrolled Power Off

The uncontrolled power off means a situation when e.g. there is removed a battery without the controlled power off sequence. There will not be any damages for ILI9486L or ILI9486L will not cause any damages for the host or lines of the interface. At an uncontrolled power off event, ILI9486L will force the display to blank and will not be any abnormal visible effects with in 1 second on the display and remains blank until “Power On Sequence” powers it up.

13. Power Level Definition

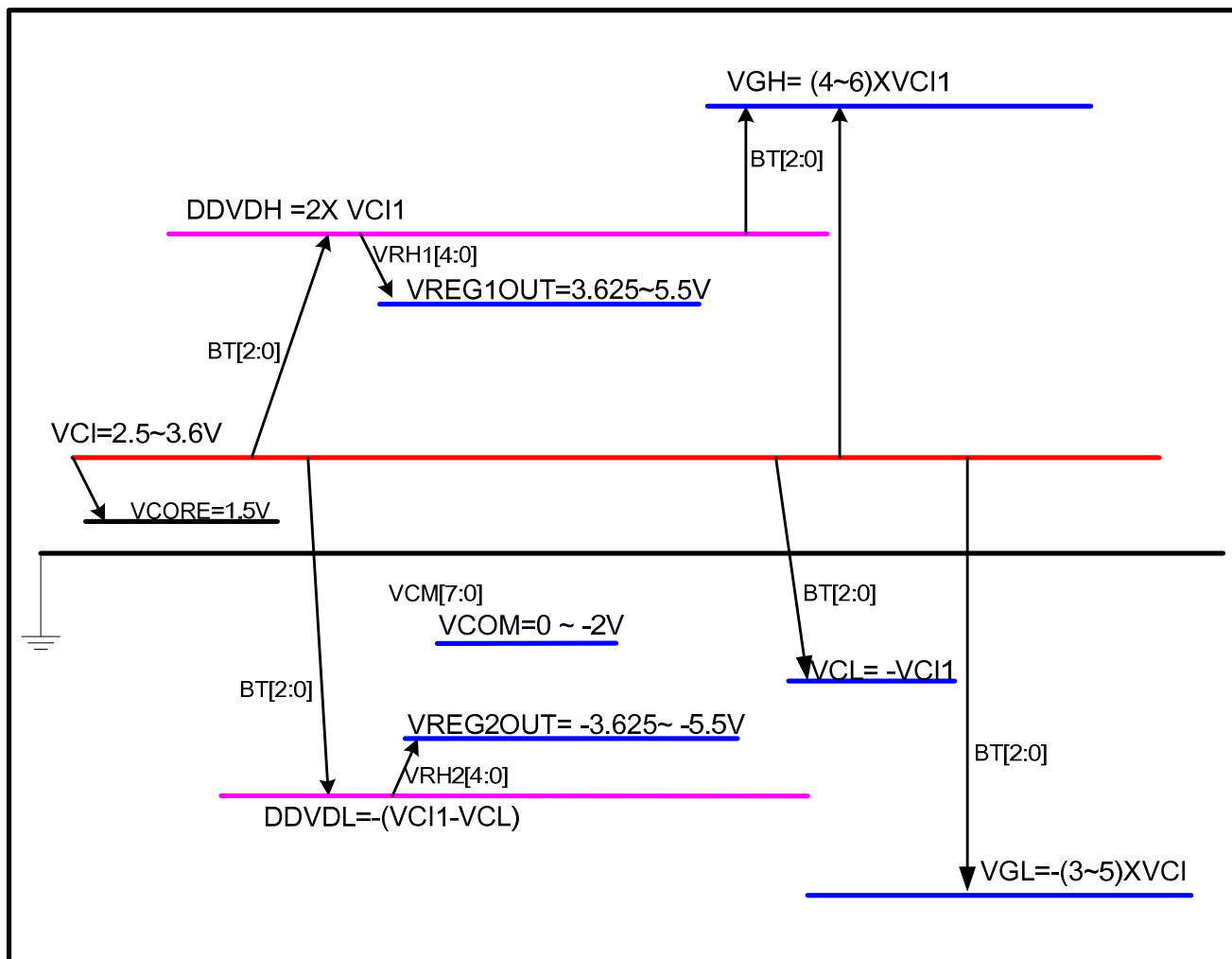
13.1. Power Levels

6 level modes are defined they are in order of Maximum Power consumption to Minimum Power Consumption:

1. Normal Mode On (full display), Idle Mode Off, Sleep Out.
In this mode, the display is able to show maximum 262,144 colors.
2. Partial Mode On, Idle Mode Off, Sleep Out.
In this mode part of the display is used with maximum 262,144 colors.
3. Normal Mode On (full display), Idle Mode On, Sleep Out.
In this mode, the full display area is used but with 8 colors.
4. Partial Mode On, Idle Mode On, Sleep Out.
In this mode, part of the display is used but with 8 colors.
5. Sleep In Mode.
In this mode, the DC:DC converter, Internal oscillator and panel driver circuit are stopped. Only the MCU interface and memory works with IOVCC power supply. Contents of the memory are safe.
6. Power Off Mode.
In this mode, both VCI and IOVCC are removed.

Note1: Transition between modes 1-5 is controllable by MCU commands. Mode 6 is entered only when both Power supplies are removed.

13.3. LCM Voltage Generation



14. Reset

14.1. Registers

The registers that are initialized are listed as below:

Register	After Powered ON	After Hardware Reset	After Software Reset
Frame Memory	Random	Random	Random
Sleep	In	In	In
Display Mode	Normal	Normal	Normal
Display Status	Display Off	Display Off	Display Off
Idle Mode	Off	Off	Off
Column Start Address	0000 h	0000 h	0000 h
Column End Address	013F h	013F h	013F h
Page Start Address	0000 h	0000 h	0000 h
Page End Address	01F h	013F h	013F h
Gamma Setting	GC0	GC0	GC0
Partial Area Start	0000 h	0000 h	0000 h
Partial Area End	01DF h	01DF h	01DF h
Memory Data Access Control	00 h	00 h	00h
RDNUMED	00 h	00 h	00h
RDDPM	08 h	08 h	08 h
RDDMADCTL	00 h	00 h	00 h
RDDCOLMOD	07 h	07 h	07 h
RDDIM	00 h	00 h	00 h
RDDSM	00 h	00 h	00 h
RDDSDR	00 h	00 h	00 h
RDDISBV	00 h	00 h	00 h
RDCTRLD	00 h	00 h	00 h
RDCABC	00 h	00 h	00 h
RDCABCMB	00 h	00 h	00 h
TE Output Line	Off	Off	Off
TE Line Mode	Mode 1 (Note 3)	Mode 1 (Note 3)	Mode 1 (Note 3)

Note 1: There will be no abnormal visible effects on the display when S/W or H/W Resets are applied.

Note 2: After Powered-On Reset finishes within 10 μ s after both VCI & IOVCC are applied.

Note 3: Mode 1 means Tearing Effect Output Line consists of V-Blanking Information only.

14.2. Output Pins, I/O Pins

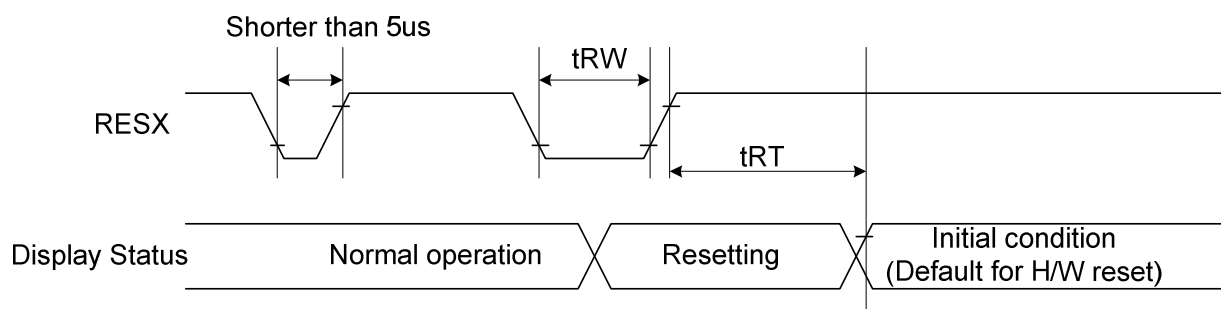
	After Power ON	After Hardware Reset	After Software Reset
TE line	Low	Low	Low
DB[17:0] (output driver), SDA	Hi-Z (Inactive)	Hi-Z (Inactive)	Hi-Z (Inactive)

Note 1: There will be no output from DB[17:0] during Power ON/OFF sequence, hardware reset and software reset.

14.3. Input Pins

	During Power ON Process	After Power ON	After Hardware Reset	After Software Reset	During Power OFF Process
RESX	See Chapter 12	Input valid	Input valid	Input valid	See Chapter 12
CSX	Input invalid	Input valid	Input valid	Input valid	Input invalid
D/CX	Input invalid	Input valid	Input valid	Input valid	Input invalid
WRX	Input invalid	Input valid	Input valid	Input valid	Input invalid
RDX	Input invalid	Input valid	Input valid	Input valid	Input invalid
RWX	Input invalid	Input valid	Input valid	Input valid	Input invalid
SCL	Input invalid	Input valid	Input valid	Input valid	Input invalid
DB[17:0] (input driver), SDA	Input invalid	Input valid	Input valid	Input valid	Input invalid

14.4. Reset Timing



Signal	Symbol	Parameter	Min	Max	Unit
RESX	tRW	Reset pulse duration	10		uS
	tRT	Reset cancel		5 (note 1,5)	mS
				120 (note 1,6,7)	mS

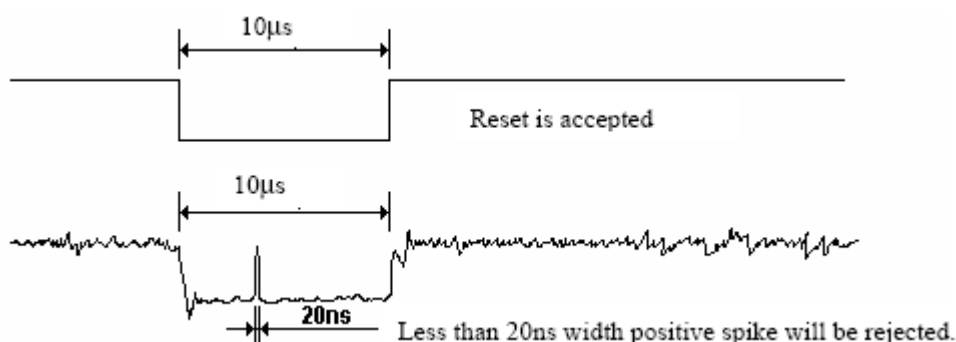
Note 1: The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from EEPROM to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

Note 2: Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

Note 3: During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In -mode.) and then return to Default condition for Hardware Reset.

Note 4: Spike Rejection also applies during a valid reset pulse as shown below:

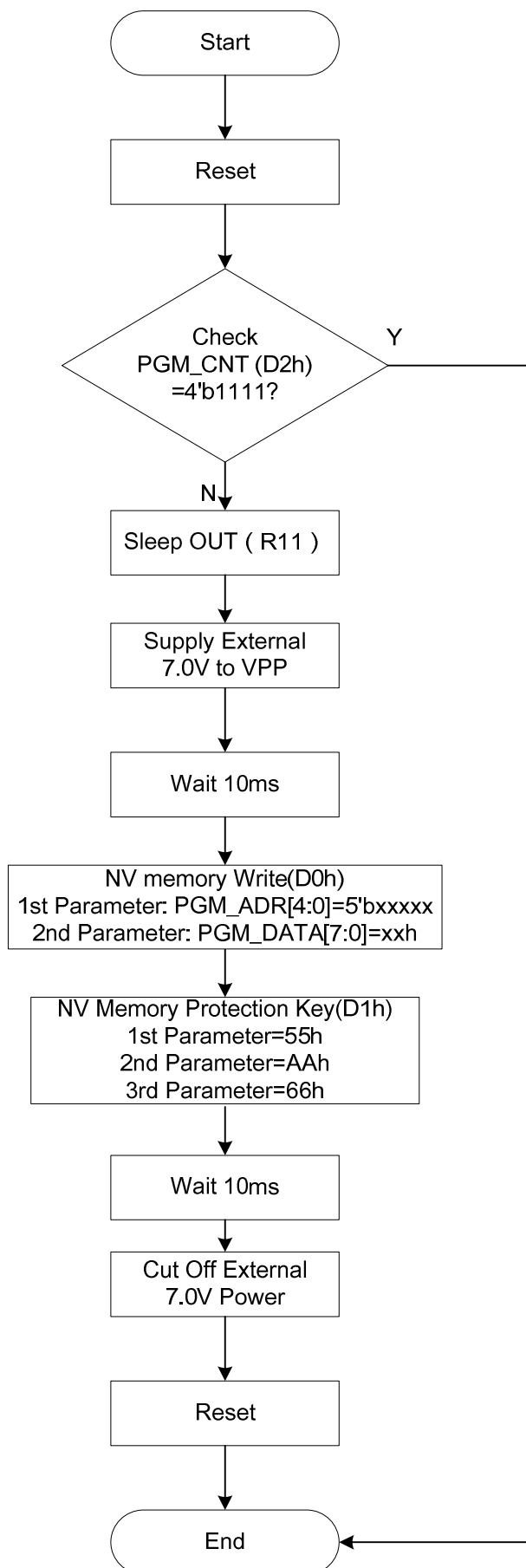


Note 5: When Reset applied during Sleep In Mode.

Note 6: When Reset applied during Sleep Out Mode.

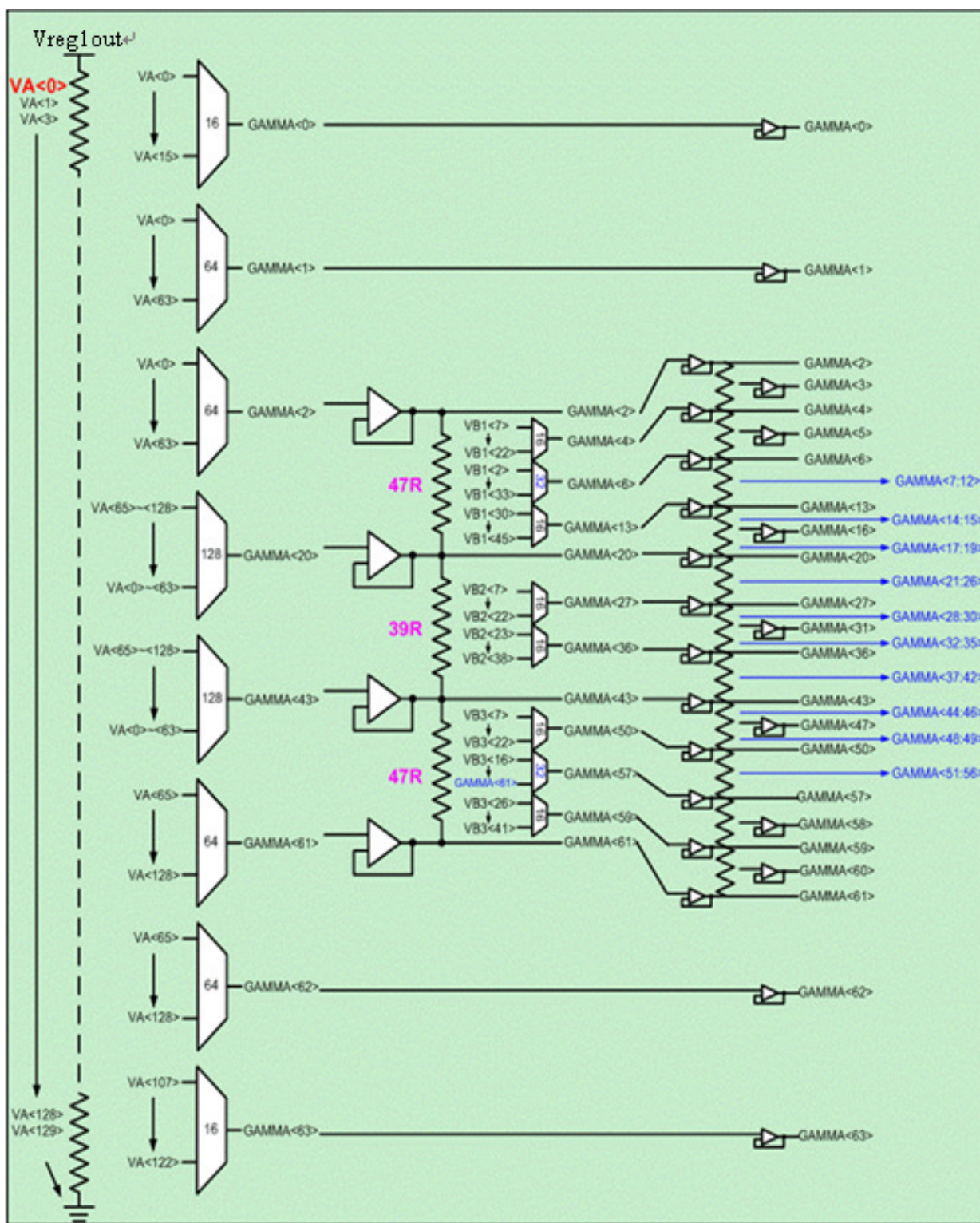
Note 7: It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

15. NV Memory Programming Flow

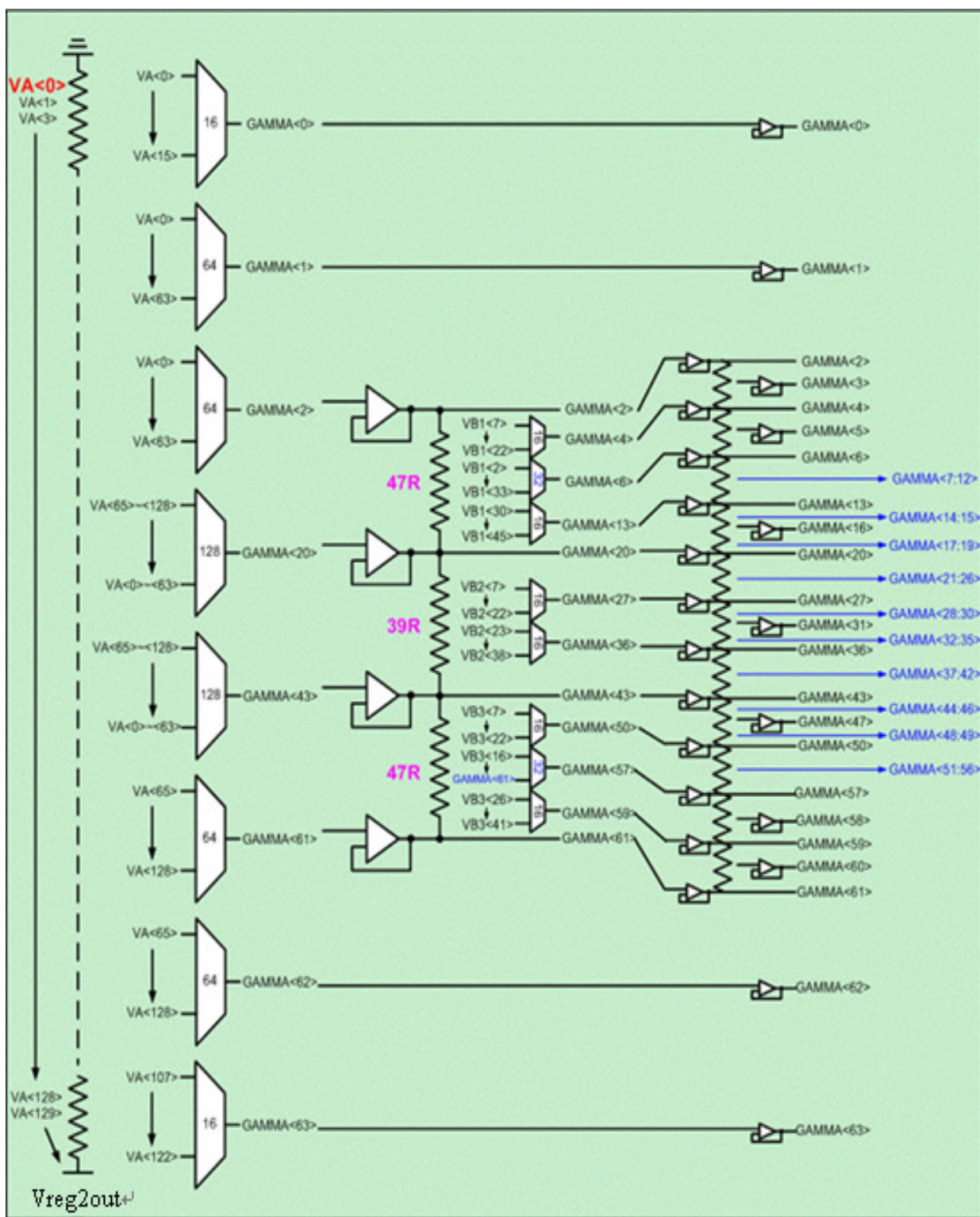


16. Gamma Correction

Positive Gamma Control (E0h)



Negative Gamma Control (E1h)



17. Electrical Characteristics

17.1. Absolute Maximum Ratings

The absolute maximum rating is listed on following table. When ILI9486L is used out of the absolute maximum ratings, ILI9486L may be permanently damaged. To use ILI9486L within the following electrical characteristics limit is strongly recommended for normal operation. If these electrical characteristic conditions are exceeded during normal operation, ILI9486 will malfunction and cause poor reliability.

Item	Symbol	Unit	Value
Supply voltage	VCI	V	-0.3 ~ +5.0
Supply voltage (Logic)	IOVCC	V	-0.3 ~ +4.6
Supply voltage (Digital)	VCORE	V	-0.3 ~ +2.4
Driver supply voltage	VGH-VGL	V	-0.3 ~ +33.0
Logic input voltage range	VIN	V	-0.3 ~ IOVCC + 0.3
Logic output voltage range	VOUT	V	-0.3 ~ IOVCC + 0.3
Operating temperature	Topr	°C	-40 ~ +85
Storage temperature	Tstg	°C	-55 ~ +110
Notes: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.			

17.2. DC Characteristics

DSI is using different state codes which are depending on DC voltage levels of the clock and data lanes. The meaning of the state codes is defined on the following table.

State Code	Line DC Voltage Levels	
	CLOCK P or DATA N	CLOCK N or DATA P
HS-0	Low (HS)	High (HS)
HS-1	High (HS)	Low (HS)
LP-00	Low (LP)	Low (LP)
LP-01	Low (LP)	High (LP)
LP-10	High (LP)	Low (LP)
LP-11	High (LP)	Low (LP)

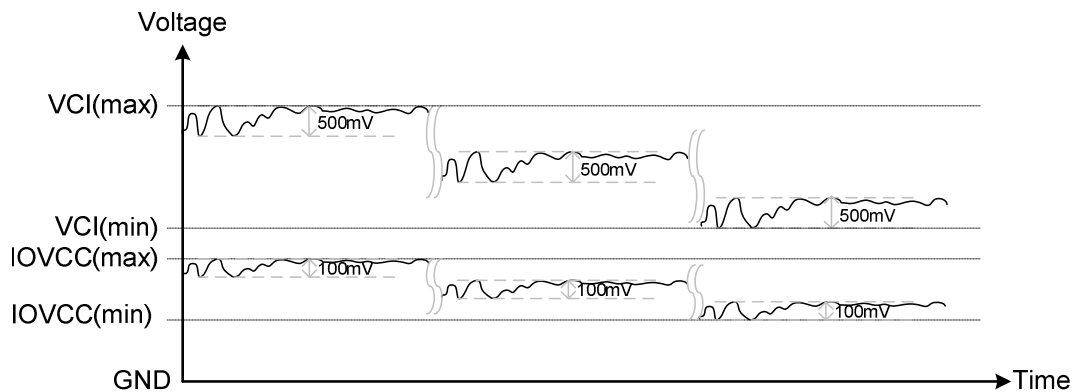
Note: $T_a = -30^{\circ}\text{C}$ to 70°C (to $+85^{\circ}\text{C}$ no damage)

17.2.1. DC characteristics for Power Lines

Parameter	Symbol	Condition	Specification			Unit
			Min.	Typ.	Max.	
Analog power supply voltage	V_{CI}	Operating voltage	2.5	3.7	4.8	V
Digital power supply voltage	V_{IOVCC}	I/O supply voltage	1.65	1.8	1.95	V
Analog power supply voltage noise	V_{CI_NOISE}	Noise window, 0 to 100MHz	-	-	500	mV
Digital power supply voltage noise	V_{IOVCC_NOISE}	Noise window, 0 to 100MHz	-	-	500	mV

Note 1: $T_a = -30^{\circ}\text{C}$ to 70°C (to $+85^{\circ}\text{C}$ no damage)

Note 2: These values are not symmetric amplitude, which centre points are $IOVCC$ or V_{CI} . See examples as reference purposes, when V_{CI_NOISE} and $IOVCC_NOISE$ are maximums, below.



17.2.2. DC characteristics for DSI LP mode

DC levels of the LP-00, LP-01, LP-10 and LP-11 are defined on table below: DC Characteristics for DSI LP mode when LP-RX, LP-CD or LP-TX is mentioned on the condition column. Other logical levels of the table are for MCU interface.

Parameter	Symbol	Condition	Specification			Unit
Logic High level output voltage	V_{OH}	$I_{OUT}=-1mA$; Note 2	$0.8 V_{IOVCC}$	-	V_{IOVCC}	V
Logic Low level output voltage	V_{OL}	$I_{OUT}=-1mA$; Note 2	0.0	-	$0.2V_{IOVCC}$	V
Logic High level input voltage	V_{IHLPCD}	LP-CD ; Note 3	450	-	1350	mV
Logic Low level input voltage	V_{ILLPCD}	LP-CD ; Note 3	0.0	-	200	mV
Logic High level input voltage	V_{IHLPRX}	LP-RX (CLOCK, DATA) ; Note 3	880	-	1350	mV
Logic Low level input voltage	V_{ILLPRX}	LP-RX (CLOCK, DATA) ; Note 3	0.0	-	550	mV
Logic Low level input voltage	$V_{ILLPRXULP}$	LP-RX (CLOCK ULP mode), Note 3	0.0	-	300	mV
Logic high level output voltage	V_{OHLPTX}	LP-TX (DATA), Note 3	1.1	-	1.3	V
Logic Low level output voltage	V_{OLLPTX}	LP-TX (DATA), Note 3	-50	-	50	mV
Logic High level input current	I_{IH}	LP-CD, LP-RX, Note 3	-	-	10	uA
Logic Low level input current	I_{IL}	LP-CD, LP-RX, Note 3	-10	-	-	uA

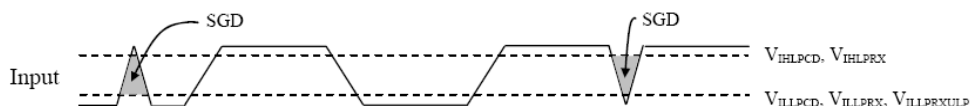
Note: (1) $T_a=-30^{\circ}C$ to $70^{\circ}C$ (to $+85^{\circ}C$ no damage)

(2) PWM_OUT, TE

(3) DSI High Speed mode is off

17.2.3. Spike / Glitch Rejection

Spike / Glitch Rejection – DSI					
Signal	Symbol	Parameter	Min	Max	Unit
Input (DSI-CLOCK P/N, DSI-CLOCK P/N)	SGD	Input pulse rejection for DSI	--	300	Vps



17.2.4. DC Characteristics for DSI HS mode

DC levels of the HS-0 and HS-0 are defined on table below: DC Characteristics for DSI HS mode.

Parameter	Symbol	Condition	Specification			Unit
Input Common Mode Voltage for Clock	V_{CMCLK}	DSI-CLOCK_P/N ; Note 2,3	70	-	330	mV
Input Common Mode Voltage for Data	V_{CMDATA}	DSI-DATA_P/N ; Note 2,3	70	-	330	mV
Common Mode Ripple for Clock Equal or Less than 450MHz	$V_{CMRCLKL450}$	DSI-CLOCK_P/N ; Note 4	-50	-	50	mV
Common Mode Ripple for Data Equal or Less than 450MHz	$V_{CMRDATAL450}$	DSI-DATA_P/N ; Note 4	-50	-	50	mV
Common Mode Ripple for Clock More than 450MHz (peak sine wave)	$V_{CMRCLKM450}$	DSI-CLOCK_P/N	-	-	100	mV
Common Mode Ripple for Data More than 450MHz (peak sine wave)	$V_{CMRDATAM450}$	DSI-DATA_P/N	-	-	100	mV
Differential Input Low Level Threshold Voltage for Clock	$V_{THLCLK-}$	DSI-CLOCK_P/N	-70	-	-	mV
Differential Input Low Level Threshold Voltage for Data	$V_{THLDATA-}$	DSI-DATA_P/N	-70	-	-	mV
Differential Input High Level Threshold Voltage for Clock	$V_{THHCLK+}$	DSI-CLOCK_P/N	-	-	70	mV
Differential Input High Level Threshold Voltage for Data	$V_{THHDATA+}$	DSI-DATA_P/N	-	-	70	mV
Single-ended Input Low Voltage	V_{ILHS}	DSI-CLOCK_P/N, DSI-DATA_P/N ; Note 3	-40	-	-	mV
Single-ended Input High Voltage	V_{IHHS}	DSI-CLOCK_P/N, DSI-DATA_P/N ; Note 3	-	-	460	mV
Differential Termination Resistor	R_{TERM}	DSI-CLOCK_P/N, DSI-DATA_P/N	80	100	125	Ω
Single-ended Threshold Voltage for Termination Enable	$V_{TERM-EN}$	DSI-CLOCK_P/N, DSI-DATA_P/N	-	-	450	mV
Termination Capacitor	C_{TERM}	DSI-CLOCK_P/N, DSI-DATA_P/N	-	-	14	pF

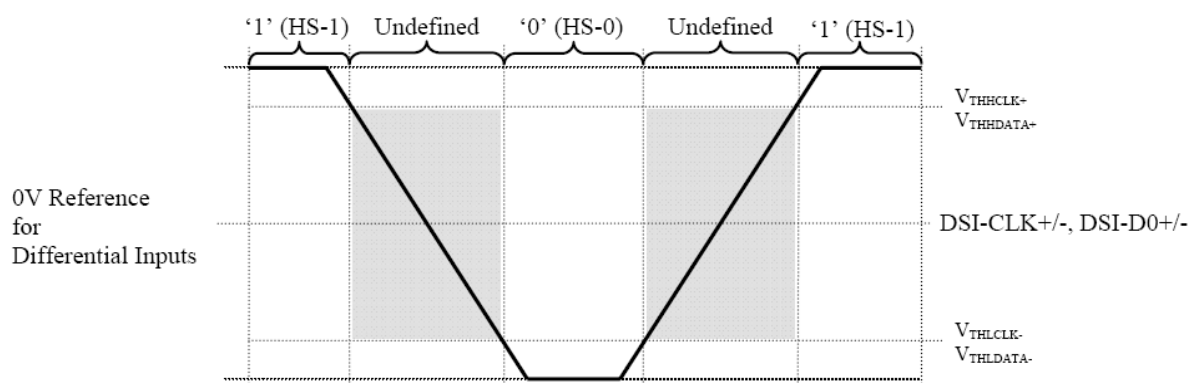
Note: (1) $T_a = -30$ to 70 °C (to $+85$ °C no damage), $IOVCC = 1.65$ to $1.95V$, $GND = 0V$

(2) Includes 50mV (-50mV to 50mV) ground difference

(3) Without $V_{CMRCLKM450}/V_{CMRDATAM450}$

(4) Without 50mV (-50mV to 50mV) ground difference

The DSI receiver (HS mode) is understanding that there is logical '1' (HS-1) when a differential voltage is more than V_{THH} (CLK+/DATA+) and the DSI receiver (HS mode) is understanding that there is logical '0' (HS-0) when a differential voltage is more than V_{THL} (CLK-/DATA-). There is undefined state if the differential voltage is less than V_{THH} (CLK+/DATA+) and less than V_{THL} (CLK-/DATA-). A reference figure is below.



17.2.5. DC Characteristics for Panel Driving

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Power & Operation Voltage							
Analog operating voltage	VCI	-	2.5	2.8	3.6	V	
Logic operating voltage	IOVCC	-	1.65	2.8	3.6	V	
Digital operating voltage	VCORE	Digital block power supply	-	1.5	-	V	Note2
Gate Driver High Voltage	VGH	-	10.0	-	16.0	V	Note3
Gate Driver Low Voltage	VGL	-	-16.0	-	-9.0	V	Note3
Driver Supply Voltage	-	VGH-VGL	19	-	32	V	Note3
VCOM Operation							
VCOM Amplitude Voltage	VCOM	-	0	-	-2.0	V	Note3
Source Driver							
Source Output Range	Vsout	-	0.1	-	VREG1OUT-0.1	V	Note4
Positive Gamma Reference Voltage	VREG1OUT	-	3.6	-	5.5	V	Note3
Negative Gamma Reference Voltage	VREG2OUT	-	-5.5	-	-3.6	V	Note3
Source Output Setting Time	Tr	Below with 99% precision	-	15	20	μs	Note4,5
Output Deviation Voltage (Source Output channel)	Vdev	Sout≥4.2V	-	-	20	mV	Note4
		Sout≤0.8V	-	-	15	mV	-
Output Offset Voltage	VOFSET	-	-	-	35	mV	Note6
Booster Operation							
1 st Booster (VCI1x2) Voltage	DDVDH	-	4.5	-	6.0	V	Note3
1 st Booster (VCI1x2) Voltage	DDVDL	-	-6.0	-	-4.5	V	Note3
1 st Booster (VCI1x2 Drop Voltage	VCI1x2 drop	loading=1mA	-	-	5	%	Note3
Liner Range	Vliner	-	0.2	-	DDVDH-0.2	V	

Note 1: IOVCC=1.65 to 3.6V, VCI=2.5 to 3.6V, AGND=DGND=0V, Ta=-30 to 70 (to +85 no damage) °C.

Note2: Please supply digital IOVCC voltage equal or less than analog VCI voltage.

Note2, 3, 4: When the measurements are performed with LCD module. Measurement Points are like below.

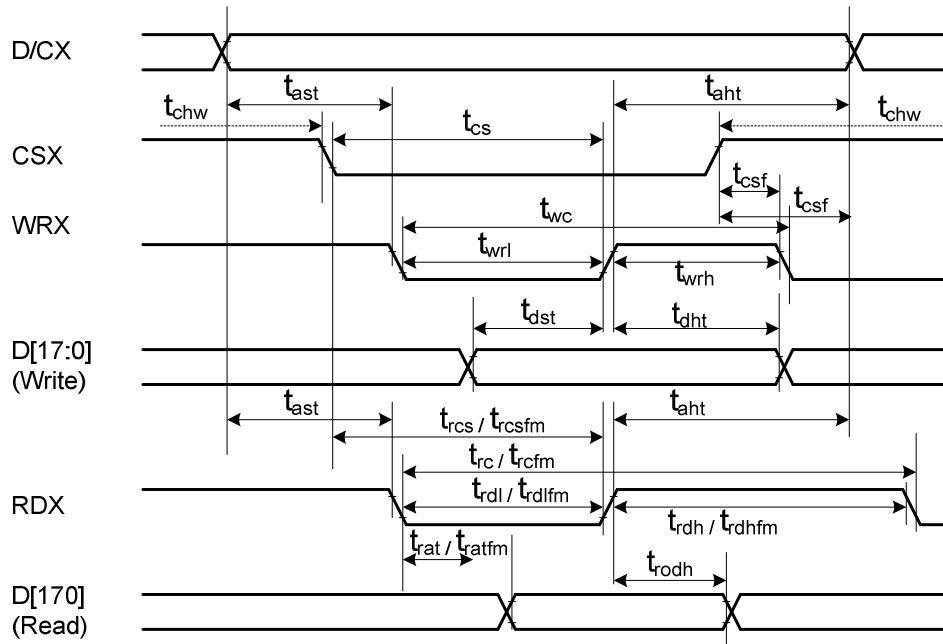
Note3: CSX, RDX, WRX, DB[17:0], D/CX, RESX, TE, SDA, SCL, IM2, IM1, IM0, and Test pins.

Note5: Source channel loading = 10pF/channel, Gate channel loading = 50pF/channel

Note6: The Max. Value is between with Note 4 measure point and Gamma setting value

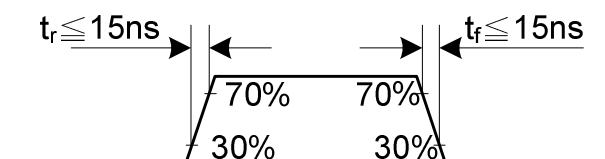
17.3. AC Characteristics

17.3.1. Display Parallel 18/16/9/8-bit Interface Timing Characteristics (8080-series)

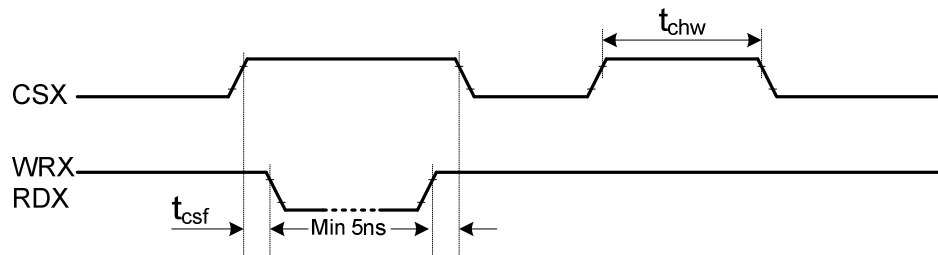


Signal	Symbol	Parameter	min	max	Unit	Description
DCX	t _{ast}	Address setup time	0	-	ns	-
	t _{ah}	Address hold time (Write/Read)	0	-	ns	-
CSX	t _{chw}	CSX "H" pulse width	0	-	ns	-
	t _{cs}	Chip Select setup time (Write)	15	-	ns	-
	t _{rcs}	Chip Select setup time (Read ID)	45	-	ns	-
	t _{rcsfm}	Chip Select setup time (Read FM)	355	-	ns	-
	t _{csf}	Chip Select Wait time (Write/Read)	0	-	ns	-
WRX	t _{wc}	Write cycle	50	-	ns	-
	t _{wrh}	Write Control pulse H duration	15	-	ns	-
	t _{wrl}	Write Control pulse L duration	15	-	ns	-
RDX (FM)	t _{rcfm}	Read Cycle (FM)	450	-	ns	When read from Frame Memory
	t _{rdhfm}	Read Control H duration (FM)	90	-	ns	
	t _{rdlfm}	Read Control L duration (FM)	355	-	ns	
RDX (ID)	t _{rc}	Read cycle (ID)	160	-	ns	When read ID data
	t _{rdh}	Read Control pulse H duration	90	-	ns	
	t _{rdl}	Read Control pulse L duration	45	-	ns	
DB[17:0], DB[15:0], DB[8:0] DB[7:0]	t _{dst}	Write data setup time	10	-	ns	For maximum CL=30pF For minimum CL=8pF
	t _{dht}	Write data hold time	10	-	ns	
	t _{rat}	Read access time	-	40	ns	
	t _{ratfm}	Read access time	-	340	ns	
	t _{rod}	Read output disable time	20	80	ns	

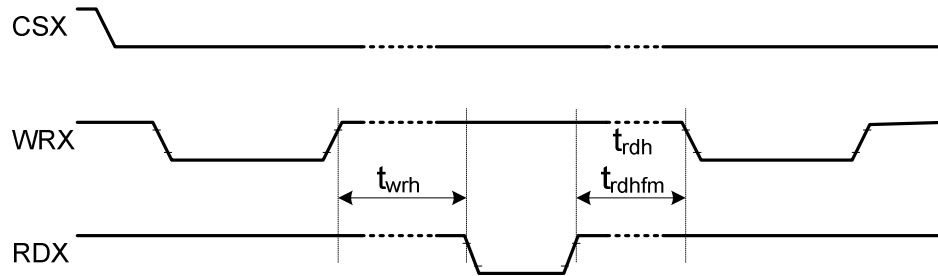
Note: (1) $T_a = -30$ to $70\text{ }^{\circ}\text{C}$, $IOVCC=1.65\text{V}$ to 3.6V , $VCI=2.5\text{V}$ to 3.6V , $AGND=DGND=0\text{V}$



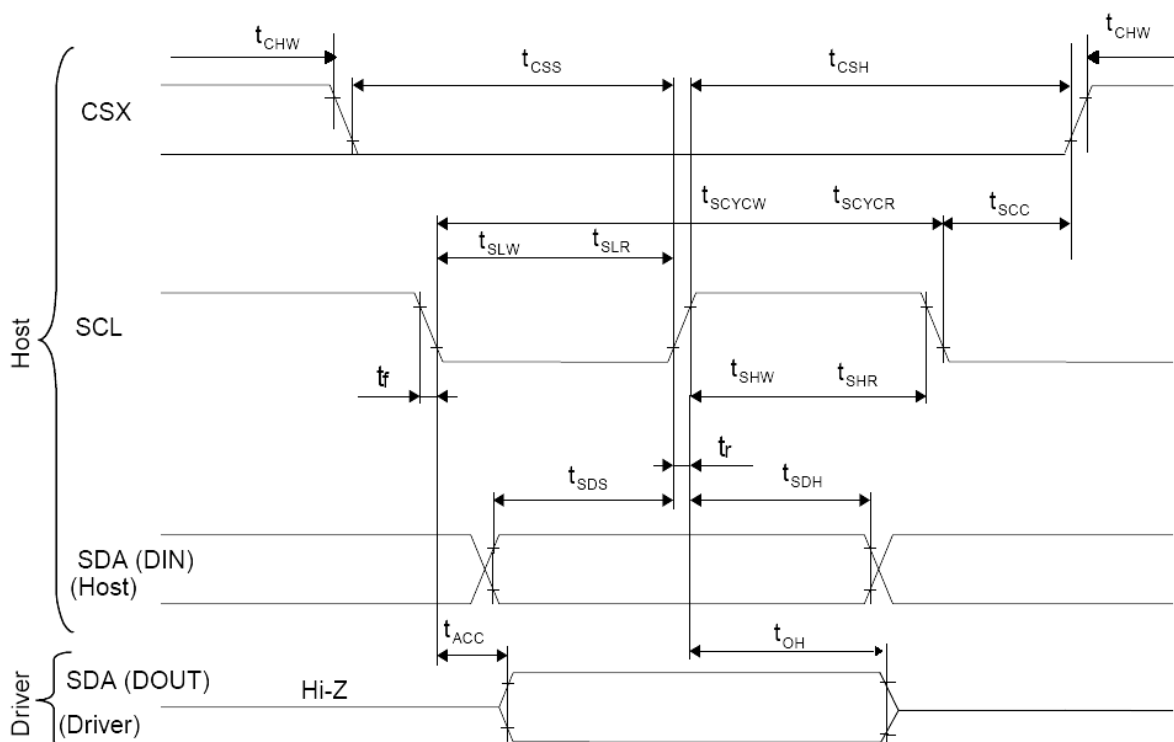
(2) Logic high and low levels are specified as 30% and 70% of IOVCC for input signals.



(3) Logic high and low levels are specified as 30% and 70% of IOVCC for input signals.

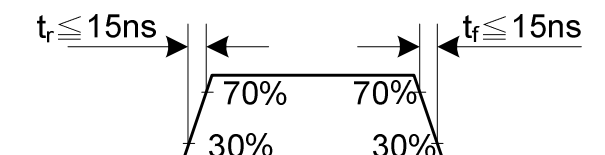


17.3.2. Display Serial Interface Timing Characteristics (3-line SPI system)

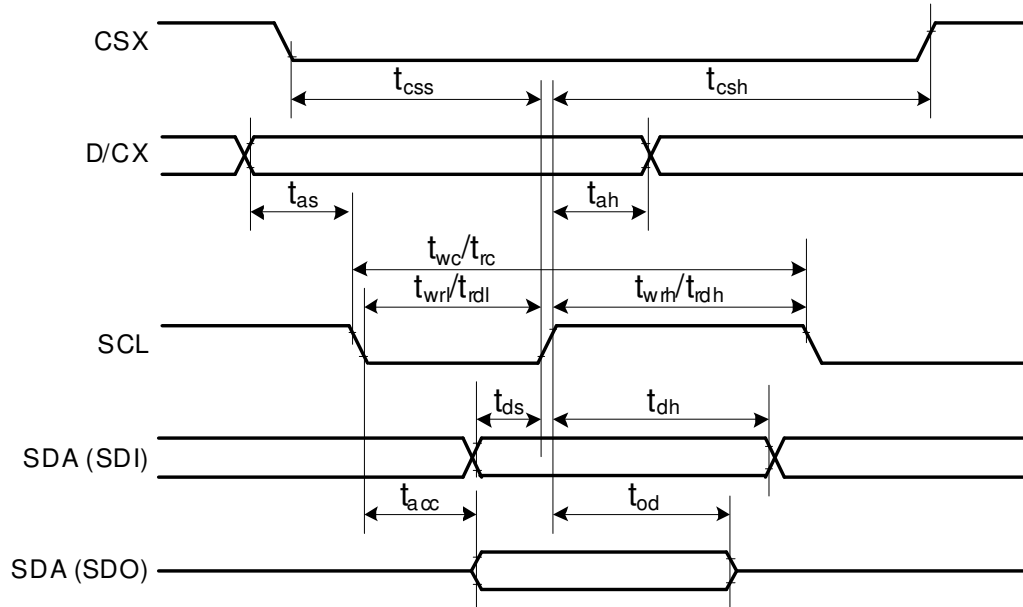


Signal	Symbol	Parameter	min	max	Unit	Description
SCL	tscycw	Serial Clock Cycle (Write)	66	-	ns	
	tshw	SCL "H" Pulse Width (Write)	15	-	ns	
	tslw	SCL "L" Pulse Width (Write)	15	-	ns	
	tscycr	Serial Clock Cycle (Read)	150	-	ns	
	tshr	SCL "H" Pulse Width (Read)	60	-	ns	
	tslr	SCL "L" Pulse Width (Read)	60	-	ns	
SDA / SDI (Input)	tsds	Data setup time (Write)	10	-	ns	
	tsdh	Data hold time (Write)	10	-	ns	
SDA / SDO (Output)	tacc	Access time (Read)	10	50	ns	
	toh	Output disable time (Read)	15	50	ns	
CSX	tsc	SCL-CSX	15	-	ns	
	tch	CSX "H" Pulse Width	40	-	ns	
	tc	CSX-SCL Time	60	-	ns	
	tc		65	-	ns	

Note: $T_a = -30$ to 70 °C, $IOVCC=1.65V$ to $3.6V$, $VCI=2.5V$ to $3.6V$, $AGND=DGND=0V$, $T=10\pm0.5ns$



17.3.3. Display Serial Interface Timing Characteristics (4-line SPI system)

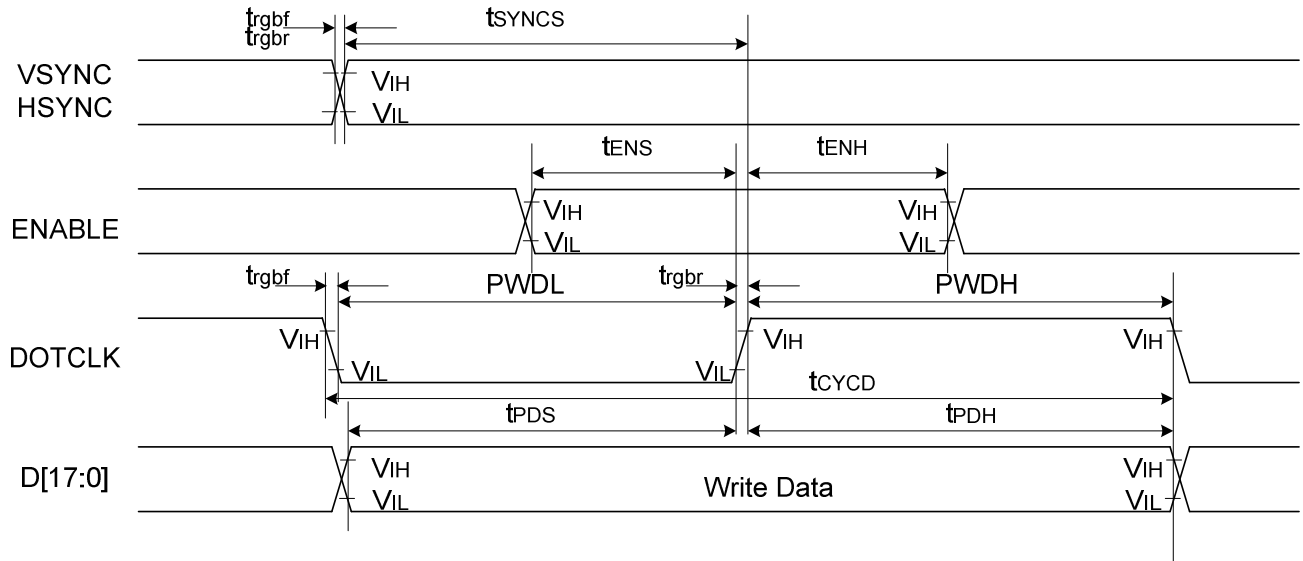


Signal	Symbol	Parameter	min	max	Unit	Description
CSX	tcss	Chip select time (Write)	15	-	ns	
	tcsh	Chip select hold time (Read)	60	-	ns	
SCL	twc	Serial clock cycle (Write)	66	-	ns	
	twrh	SCL "H" pulse width (Write)	15	-	ns	
	twrl	SCL "L" pulse width (Write)	15	-	ns	
	trc	Serial clock cycle (Read)	150	-	ns	
	trdh	SCL "H" pulse width (Read)	60	-	ns	
	trdl	SCL "L" pulse width (Read)	60	-	ns	
D/CX	tas	D/CX setup time	10	-	ns	
	tah	D/CX hold time (Write / Read)	10	-	ns	
SDA / SDI (Input)	tds	Data setup time (Write)	10	-	ns	
	tdh	Data hold time (Write)	10	-	ns	
SDA / SDO (Output)	tacc	Access time (Read)	10	50	ns	For maximum CL=30pF
	tod	Output disable time (Read)	15	50	ns	For minimum CL=8pF

Note: (1) $T_a = -30$ to $70\text{ }^{\circ}\text{C}$, $IOVCC=1.65\text{V}$ to 3.6V , $VCI=2.5\text{V}$ to 3.6V , $AGND=DGND=0\text{V}$, $T=10\pm 0.5\text{ns}$.

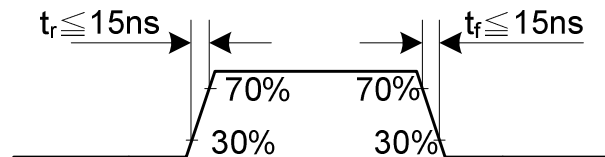
(2) Does not include signal rise and fall times.

17.3.4. Parallel 18/16-bit RGB Interface Timing Characteristics

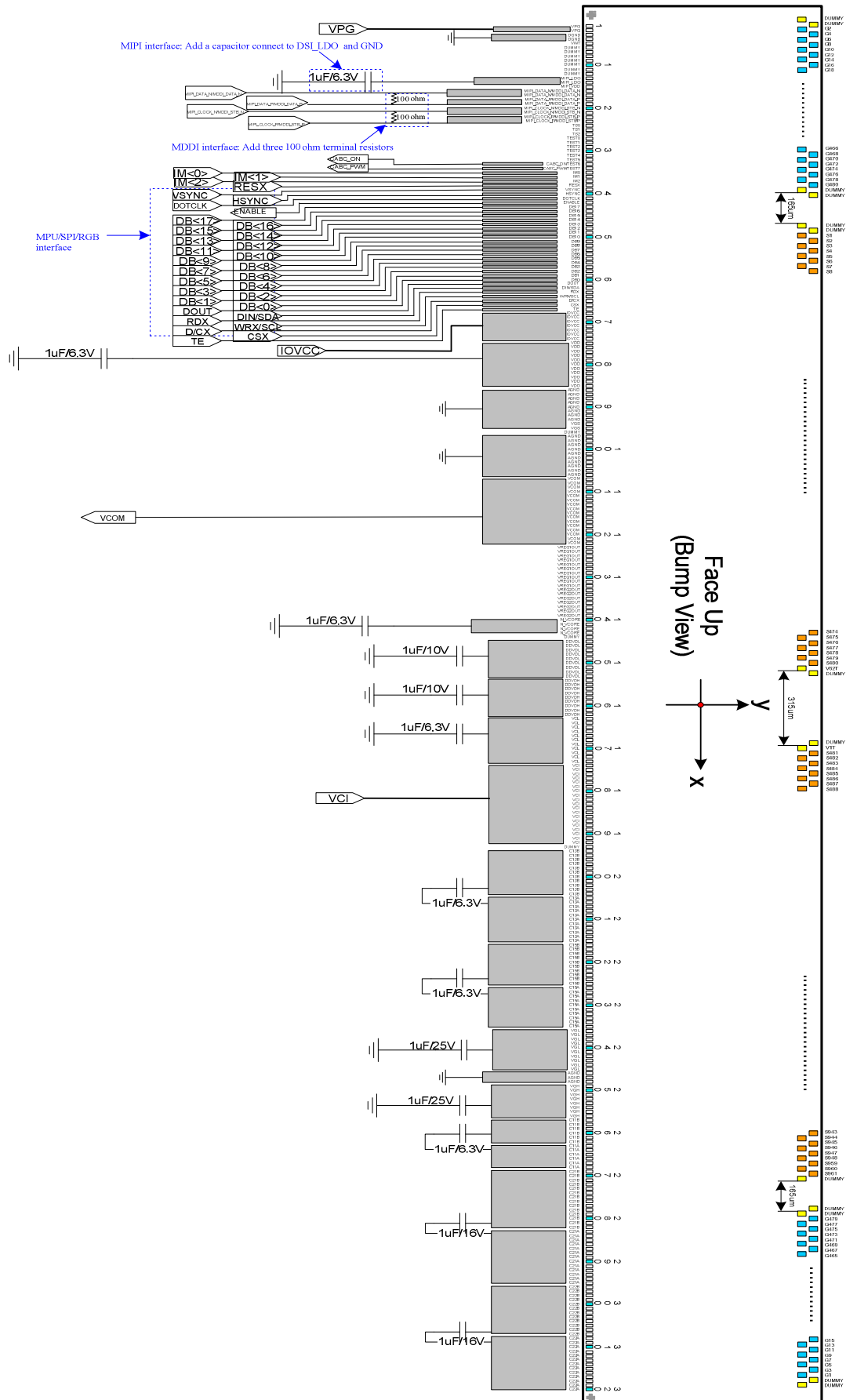


Signal	Symbol	Parameter	min	max	Unit	Description
VSYNC / HSYNC	tSYNCS	VSYNC/HSYNC setup time	15	-	ns	18/16-bit bus RGB interface mode
	tSYNCH	VSYNC/HSYNC hold time	15	-	ns	
ENABLE	tENS	ENABLE setup time	15	-	ns	
	tENH	ENABLE hold time	15	-	ns	
DB[17:0]	tPOS	Data setup time	15	-	ns	
	tPDH	Data hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level period	15	-	ns	
	PWDL	DOTCLK low-level period	15	-	ns	
	tCYCD	DOTCLK cycle time	66	-	ns	
	trgbbr, trgbfr	DOTCLK, HSYNC, VSYNC rise/fall time	-	15	ns	

Note: Ta = -30 to 70 °C, IOVCC=1.65V to 3.6V, VCI=2.5V to 3.3V, AGND=DGND=0V



18. Application Circuit



The following table shows specifications of external elements connected to ILI9486L's power supply circuit.

Items	Recommended Specification	Pin connection
Capacity 1 μ F (B characteristics)	6.3V	C11A/B, C13A/B, C15A/B, VCL, VDD, N_VCORE(back up)
	10V	DDVDH, DDVDL
	16V	C21 A/B, C22A/B(for +6,-3 backup)
	25V	VGH, VGL

19. Revision History

Version No.	Date	Page	Description
V.001	2010/09/02	All	New created
V.001	2010/11/04	147 286 310	Modify command list Add LCM voltage generation Application circuit
V.001	2010/11/23	230	Modify command
V.001	2011/01/03	10 25 239 257 297	Modify VCOM and VGH-VGL voltage Modify pad size Modify command RC1 (Remove SAP) Modify command RD0 Modify write cycle (66ns -> 50ns)
V.001	2011/02/25	290 291	Modify Gamma Correction
V.001	2011/03/01	16 18-24	Modify pad size Modify source and gate pad locations
V.001	2011/03/25	12-13 240-242 235 259 289 311	Modify pin description Modify command RC2 RC3 RC4 Modify command RB7 Modify command RD2 (Remove OTP_DATA) Modify NV Memory programming flow Modify capacity
V.002	2011/04/01	239 289	Modify command RC1 Modify NV Memory programming flow
V.003	2011/04/08	16	Modify the chip thickness
V.004	2011/04/22	227 239	Modify the inversion mode (DINV[1:0]) Modify the VCI1 output voltage selection (VC[2:0])
V.005	2011/05/04	227	Modify the inversion mode (DINV[1:0])
V.006	2011/05/11	18	Modify the C22B (No.296) pad location typo