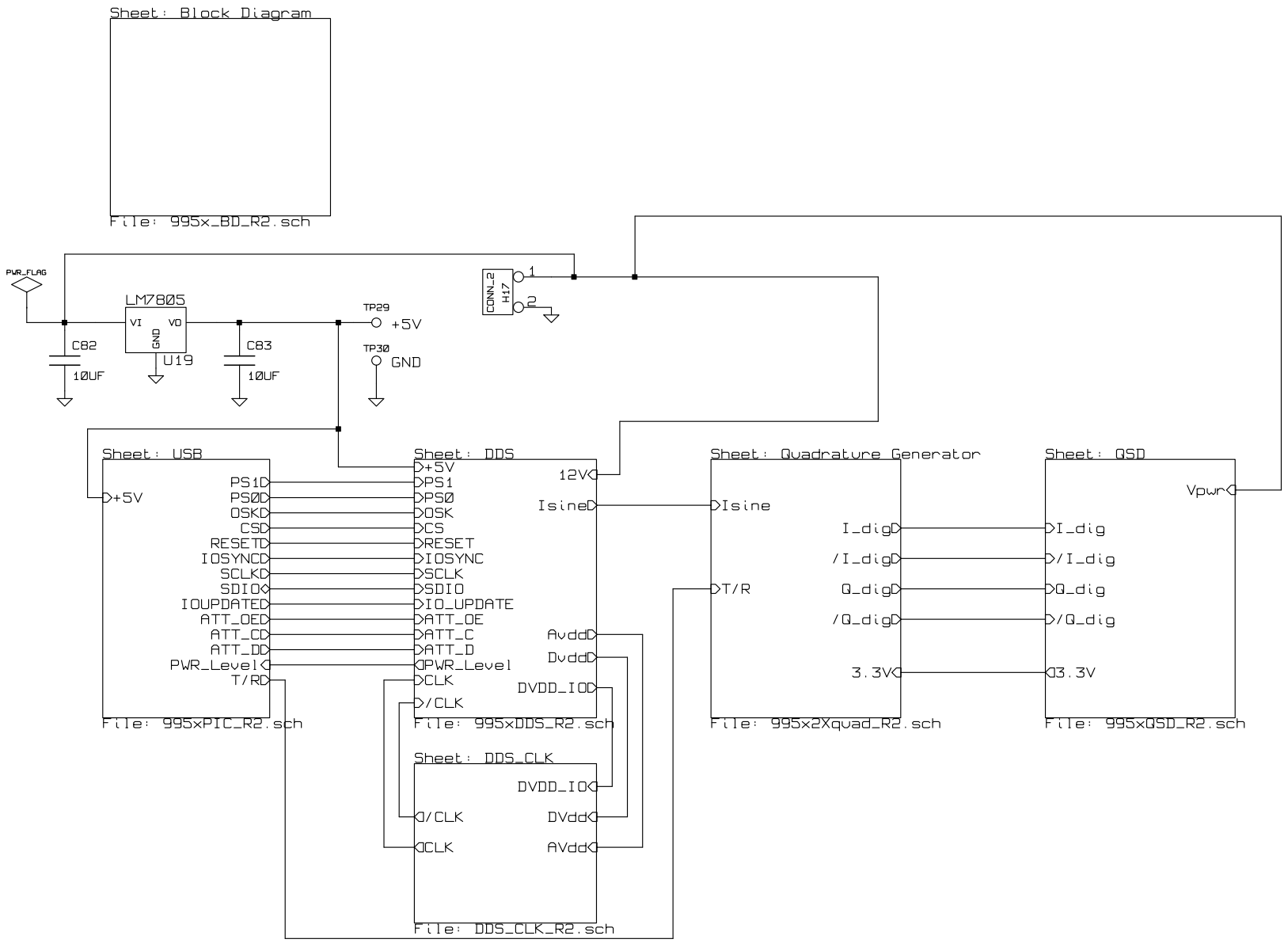
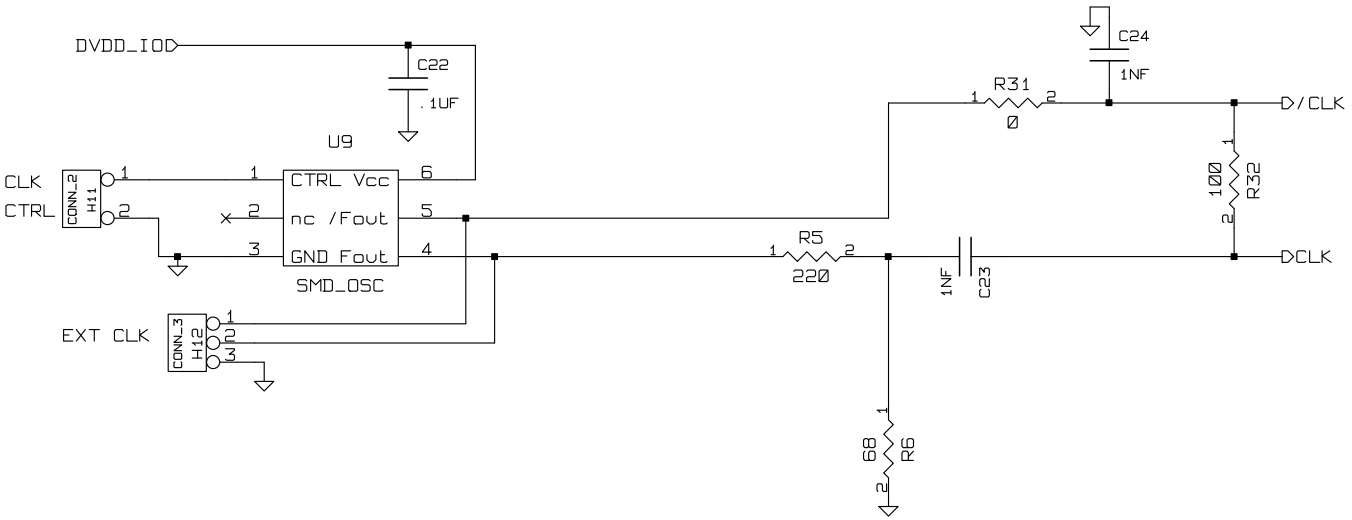


Designed by David A. Brainerd		
Bluebird Originals		
Title: AD995x Root Sheet		
Size: A	Date: 2 apr 2008	Rev:
KiCad E.D.A. EESchema (2007-11-29-c)		Sheet: 1/7

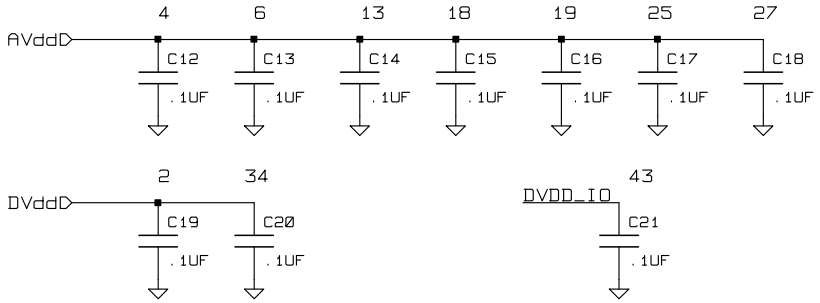


CLOCK OPTIONS:

CMOS OSC: Put 1nF from /CLK to GND., Omit R31,R32
The 220 and 68 ohm resistors are for a 3.3V clock. Change as required for other amplititudes.

LVDS OSC Replace R5 with 0ohm, delete R6, Replace C23 with 0ohm, delete C24

EXT OSC: Omit SMD_OSC (or disable from pin 1), If single-ended put 1nF from /CLK to GND, adjust 220 and 68 for proper amplitude. Omit R31.



DDS Chip Power Bypass Caps

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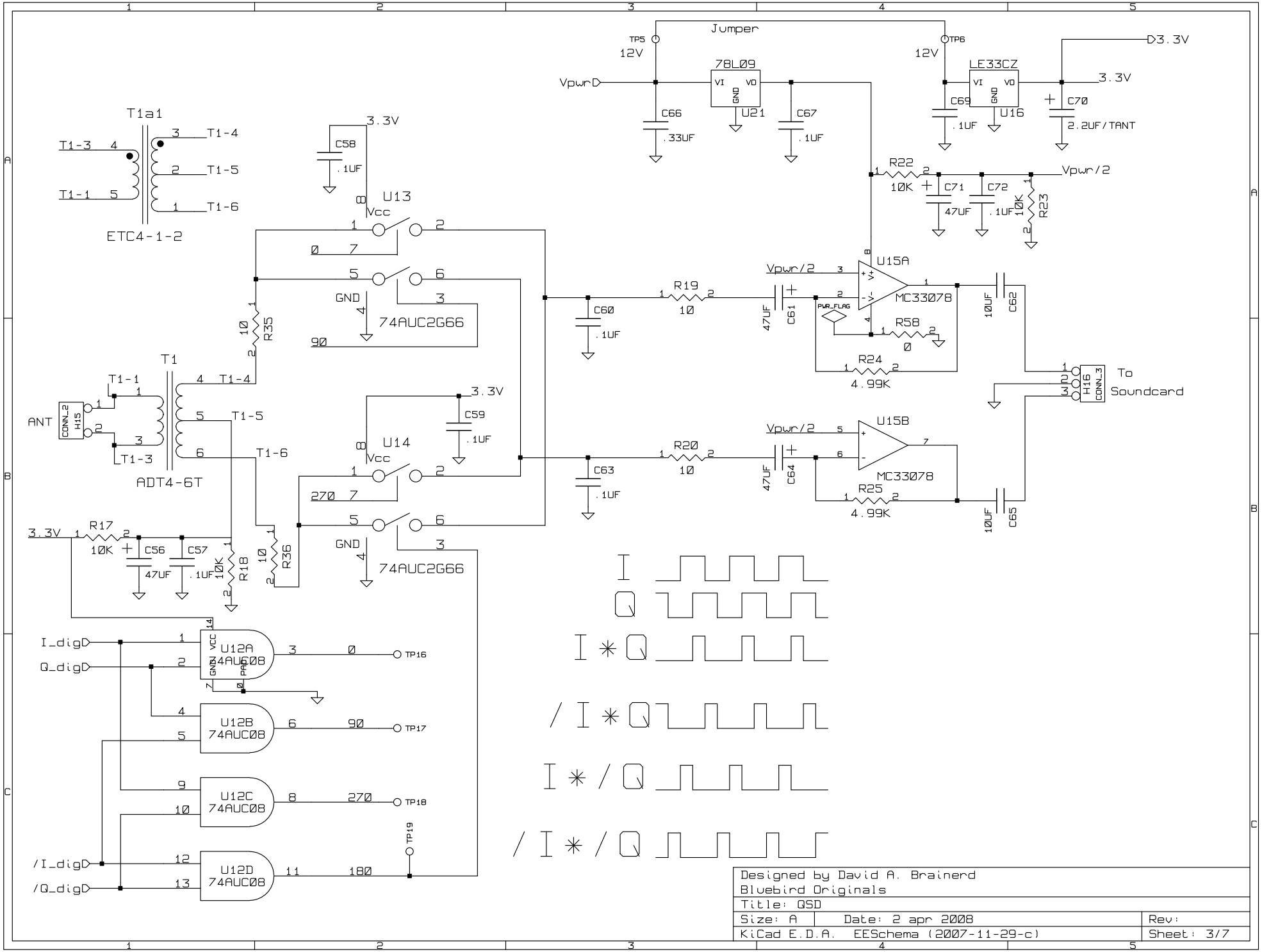
Title: DDS Clock Circuit		
Size: A	Date: 2 apr 2008	Rev:
KiCad E.D.A. EESchema (2007-11-29-c)		Sheet: 2/7



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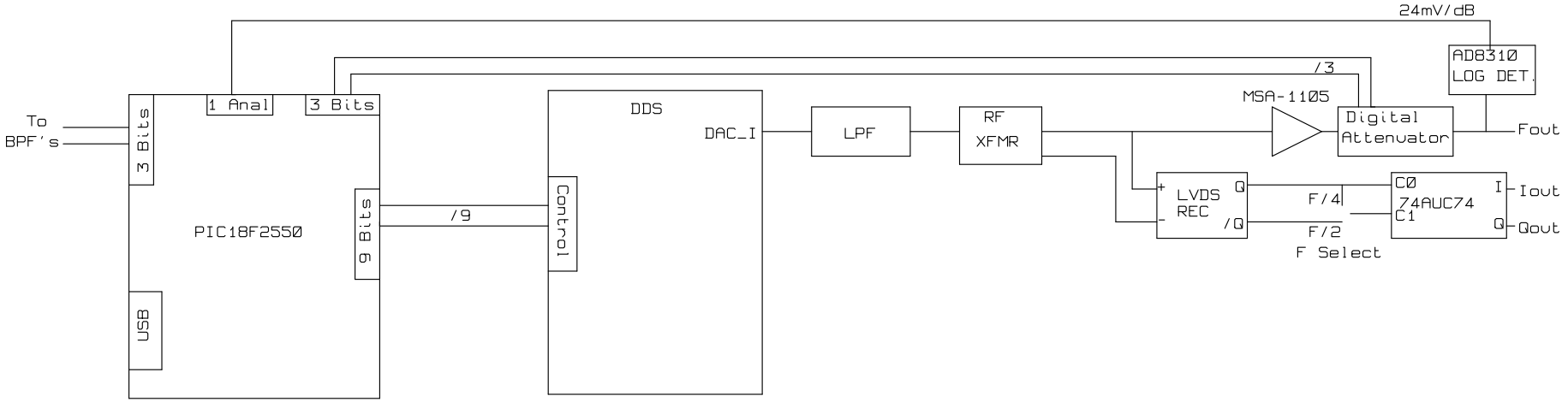
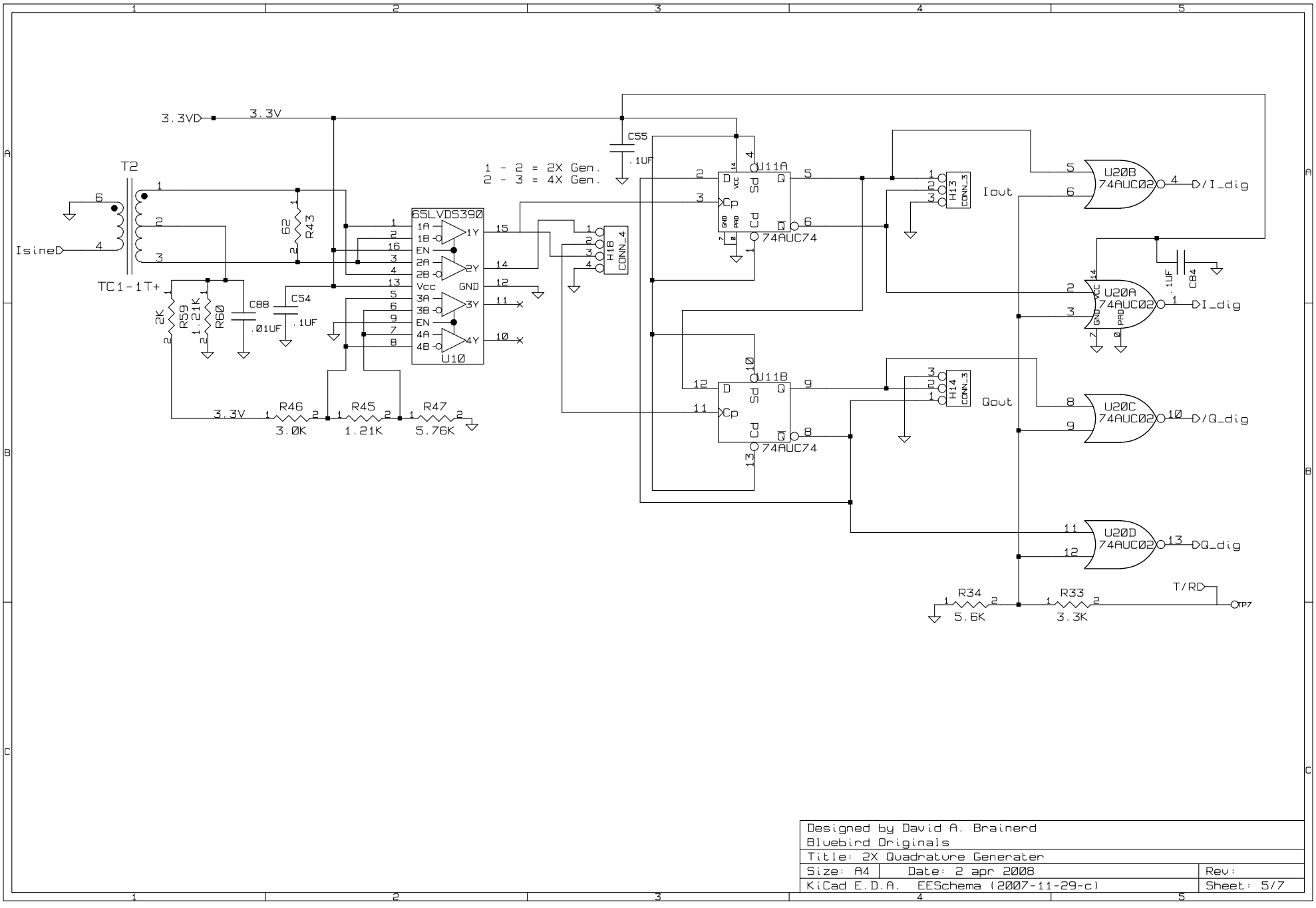
Title: QSD		
Size: A	Date: 2 apr 2008	Rev:
KiCad E.D.A. EESchema (2007-11-29-c)		Sheet: 3/7



Designed by David A. Brainerd Bluebird Originals		
Title: Block Diagram		
Size: A	Date: 2 apr 2008	Rev:
KiCad E.D.A. EESchema (2007-11-29-c)		Sheet: 4/7



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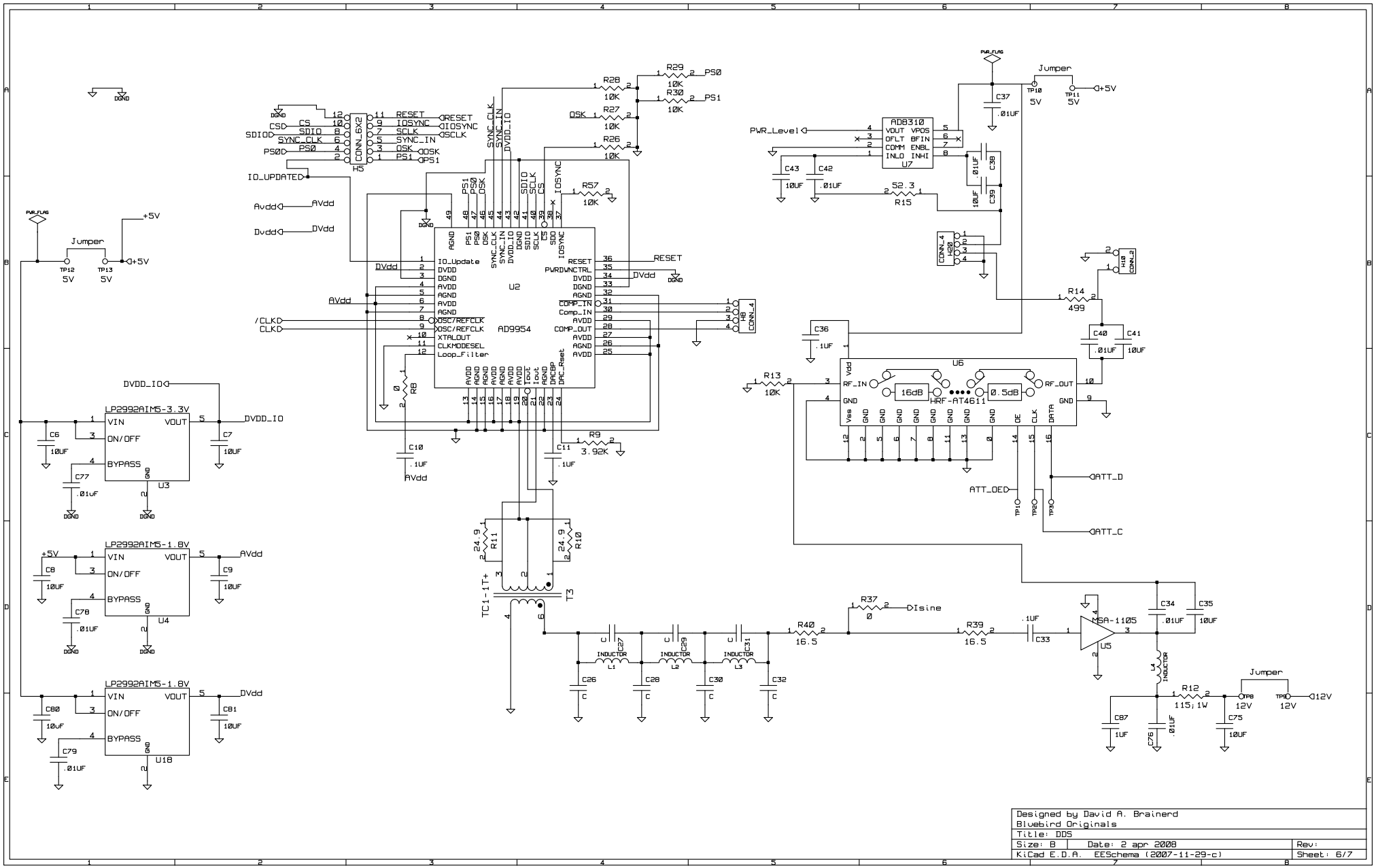
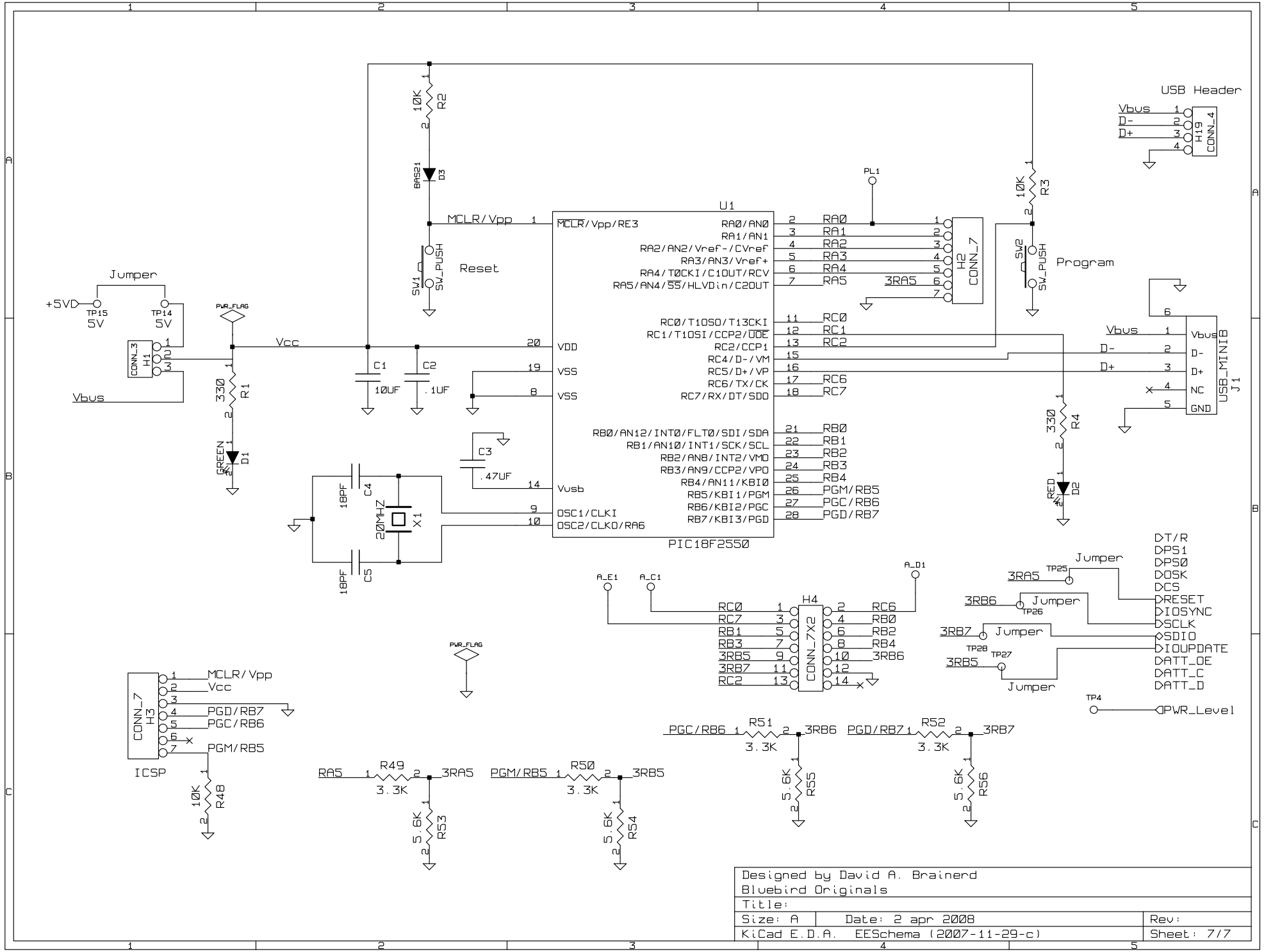
Title: 2X Quadrature Generater		
Size: A4	Date: 2 apr 2008	Rev:
KiCad E.D.A. EESchema (2007-11-29-c)		Sheet: 5/7


Designed by David A. Brainerd
Bluebird Originals
Title: DDS
Size: B
Date: 2 apr 2008
Rev:
KiCad E.D.A. EESchema (2007-11-29-c)
Sheet: 6/7


USB Header
Vbus
D-
D+
H19
CONN_4
10K
R2
BAS21
D3
MCLR/Vpp
SW1
SW_PUSH
Reset
U1
PL1
10K
R3
SW2
SW_PUSH
Program
H2
CONN_7
3RA5
Jumper
+5VD
TP15
5V
TP14
5V
PWR_FLAG
CONN_3
H1
Vcc
Vbus
330
R1
GREEN
D1
C1
10UF
C2
.1UF
C3
.47UF
18PF
C4
20MHZ
X1
18PF
C5
MCLR/Vpp/RE3
VDD
VSS
VSS
Vusb
OSC1/CLKI
OSC2/CLKO/RA6
RA0/AN0
RA1/AN1
RA2/AN2/Vref-/CVref
RA3/AN3/Vref+
RA4/T0CKI/C1OUT/RCV
RA5/AN4/SS/HLVDin/C2OUT
RC0/T1OSO/T13CKI
RC1/T1OSI/CCP2/UOE
RC2/CCP1
RC4/D-/VM
RC5/D+/VP
RC6/TX/CK
RC7/RX/DT/SDO
RB0/AN12/INT0/FLT0/SDI/SDA
RB1/AN10/INT1/SCK/SCL
RB2/AN8/INT2/VMO
RB3/AN9/CCP2/VPO
RB4/AN11/KBI0
RB5/KBI1/PGM
RB6/KBI2/PGC
RB7/KBI3/PGD
PIC18F2550
USB_MINIB
J1
Vbus
D-
D+
NC
GND
330
R4
RED
D2
A_E1
A_C1
A_D1
H4
CONN_7X2
RC0
RC7
RB1
RB3
3RB5
3RB7
RC2
RC6
RB0
RB2
RB4
3RB6
3RA5
TP25
3RB6
TP26
3RB7
TP28
TP27
3RB5
DT/R
PS1
PS0
OSK
CS
RESET
IOSYNC
SCLK
SDIO
IOUPDATE
ATT_OE
ATT_C
ATT_D
TP4
PWR_Level
ICSP
CONN_7
H3
MCLR/Vpp
Vcc
PGD/RB7
PGC/RB6
PGM/RB5
10K
R48
RA5
R49
3.3K
3RA5
5.6K
R53
PGM/RB5
R50
3.3K
3RB5
5.6K
R54
PGC/RB6
R51
3.3K
3RB6
5.6K
R55
PGD/RB7
R52
3.3K
3RB7
5.6K
R56
Designed by David A. Brainerd
Bluebird Originals
Title:
Size: A
Date: 2 apr 2008
Rev:
KiCad E.D.A. EESchema (2007-11-29-c)
Sheet: 7/7