Section 59. Oscillators with DCO

HIGHLIGHTS

This section of the manual contains the following major topics:

Note:	This family reference manual section is meant to serve as a complement to device data sheets. Depending on the device variant, this manual section may not apply to all PIC32 devices. Please consult the note at the beginning of the **"Oscillator Configuration"** chapter in the current device data sheet to check whether this document supports the device you are using. Device data sheets and family reference manual sections are available for download from the Microchip Worldwide Web site at: http://www.microchip.com

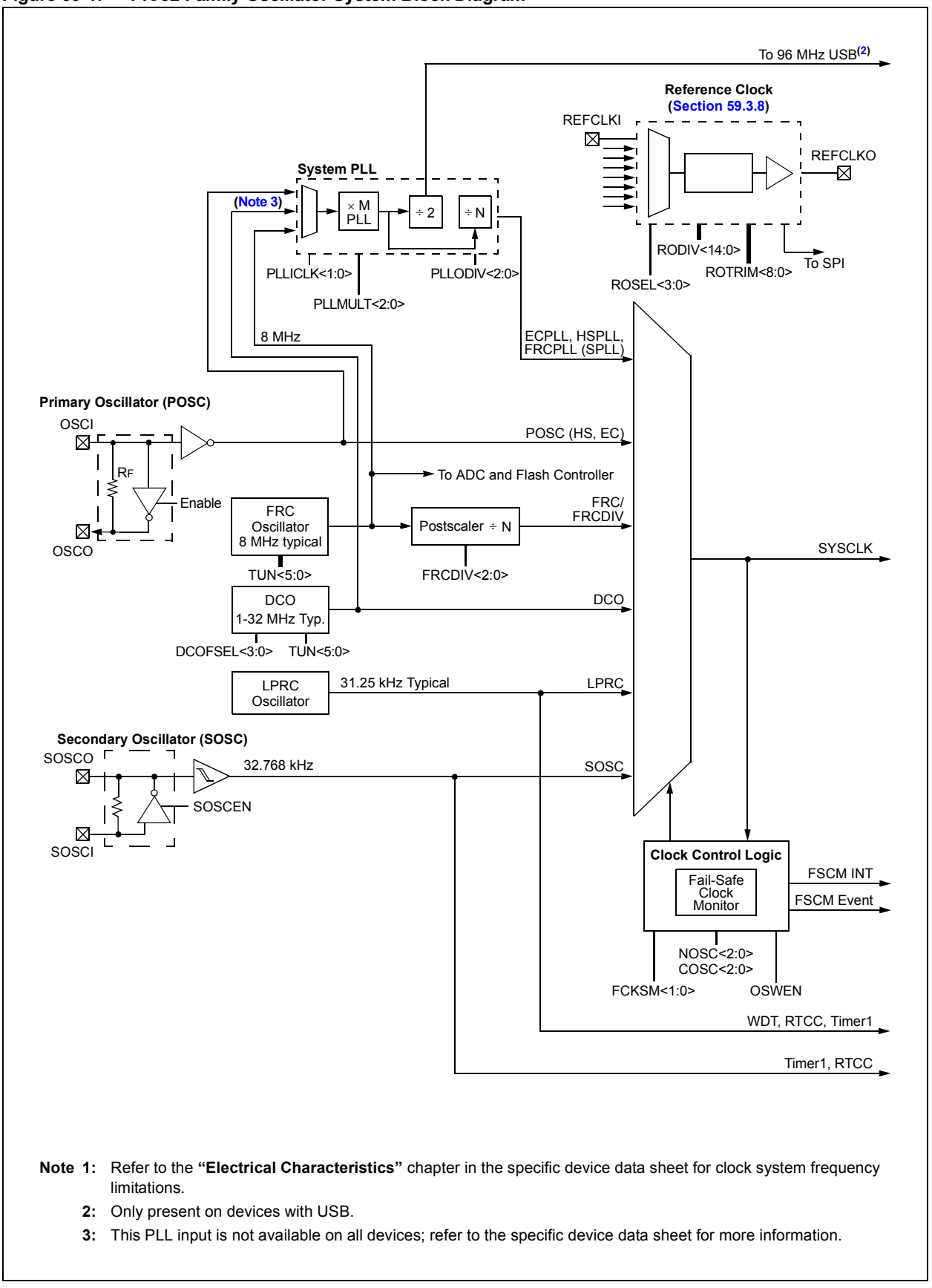
59.1 INTRODUCTION

The PIC32 oscillator system has the following modules and features:

- Five external and internal oscillator options as clock sources
- On-chip Phase-Locked Loop (PLL) with a user-selectable multiplier and output divider to boost operating frequency on select internal and external oscillator sources
- Internal Digitally Controlled Oscillator (DCO) that combines fast start-up times and low current consumption
- Software-controllable switching between various clock sources
- Flexible Reference Clock Generator (REFO)
- A Fail-Safe Clock Monitor (FSCM) that detects clock failure and permits safe application recovery or shutdown

A block diagram of the oscillator system is shown in Figure 59-1.

Figure 59-1: PIC32 Family Oscillator System Block Diagram(1)



Note 1: Refer to the **"Electrical Characteristics"** chapter in the specific device data sheet for clock system frequency limitations.

2: Only present on devices with USB.

3: This PLL input is not available on all devices; refer to the specific device data sheet for more information.

59.2 CONTROL REGISTERS

The oscillator module consists of the following Special Function Registers (SFRs):

- **OSCCON: Oscillator Control Register(1)**
  This register controls clock switching and provides status information that allows current clock source, PLL lock and clock fail conditions to be monitored.
- **SPLLCON: System PLL Control Register(1,2)**
  This register is used to control the System Clock PLL. It allows the input frequency to be used to generate a higher system frequency.
- **REFOCON: Reference Oscillator Control Register**
  This register controls the Reference Clock Generator.
- **REFOTRIM: Reference Oscillator Trim Register(1,2,3)**
  This register fine-tunes the Reference Clock Generator.
- **CLKSTAT: Clock Source Status Register**
  This register provides status information on all of the oscillators.
- **OSCTUN: FRC Tuning Register(1)**
  This register is used to tune the internal FRC oscillator frequency in software. It allows the FRC oscillator frequency to be adjusted over a range of ±12%.
- **DCOCON: Digitally Controlled Oscillator Control Register**
  This register controls the operation and frequency selection for the DCO.

Note:	Device Configuration Word registers also provide additional configuration settings that are related to the oscillator module. Refer to the **"Special Features"** chapter in the specific device data sheet for detailed information on these registers.

59.2.1 Special Function Register Summary

Table 59-1 provides a brief summary of the related Oscillator registers. The corresponding registers appear after the summary, which include detailed descriptions.

In addition, the Oscillator registers in Table 59-1 all have associated Clear, Set and Invert registers, suffixed: -CLR, -SET and -INV, at address offsets of 0x4, 0x8 and 0xC bytes, respectively. These associated registers are used to modify their main registers. Writing a '1' to a bit position in an associated register will clear, set or invert the valid corresponding bit in the main register. Reads from these registers should be ignored.

Table 59-1: Oscillator SFR Summary

Name	Bit Range	Bit 31/15	Bit 30/14	Bit 29/13	Bit 28/12	Bit 27/11	Bit 26/10	Bit 25/9	Bit 24/8	Bit 23/7	Bit 22/6	Bit 21/5	Bit 20/4	Bit 19/3	Bit 18/2	Bit 17/1	Bit 16/0
OSCCON	31:16	—	—	—	—	—	FRCDIV<2:0>			—	—	SLP2SPD	—	—	—	—	—
	15:0	—	COSC<2:0>		—	NOSC<2:0>				CLKLOCK	r	r	SLPEN	CF	—	SOSCEN	OSWEN
SPLLCON	31:16	—	—	—	—	—	PLLODIV<2:0>			—	—	—	—	—	PLLMULT<2:0>		
	15:0	—	—	—	—	—	—	—	—	PLLICLK<1:0>		—	—	—	—	—	—
REFOCON	31:16	—	RODIV<14:0>														
	15:0	ON	—	SIDL	OE	RSLP	—	DIVSWEN	ACTIVE	—	—	—	—	ROSEL<3:0>			
REFOTRIM	31:16	ROTRIM<8:0>									—	—	—	—	—	—	—
	15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
CLKSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
	15:0	—	—	—	—	—	—	—	—	SPLLRDY	—	LPRCRDY	SOSCRDY	DCORDY	POSCRDY	DIVSPLLRDY	FRCRDY
OSCTUN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
	15:0	ON	r	SIDL	SRC	LOCK	POL	ORNG	ORNGPOL	—	—	TUN<5:0>					
DCOCON	31:16	—	—	ON	—	DCOFSEL<3:0>				—	—	—	—	—	—	—	—
	15:0	—	—	SIDL	—	—	—	—	—	—	—	TUN<5:0>					

Legend: — = Unimplemented, read as '0'; r = Reserved bit.

Register 59-1: OSCCON: Oscillator Control Register(1)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-1
	—	—	—	—	—	FRCDIV<2:0>		
23:16	U-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
	—	—	SLP2SPD(4)	—	—	—	—	—
15:8	U-0	R-y	R-y	R-y	U-0	R/W-y	R/W-y	R/W-y
	—	COSC<2:0>(2)			—	NOSC<2:0>(2)		
7:0	R/W-0	r-0	r-0	R/W-0	R/W-0, HS	U-0	R/W-y	R/W-y
	CLKLOCK	—	—	SLPEN	CF(3)	—	SOSCEN	OSWEN

Legend:	HS = Hardware Settable bit	y = Value set from Configuration bits on POR
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared r = Reserved bit

bit 31-27 **Unimplemented:** Read as '0'

bit 26-24 **FRCDIV<2:0>:** Internal Fast RC (FRC) Oscillator Clock Divider bits
- 111 = Divide-by-256
- 110 = Divide-by-64
- 101 = Divide-by-32
- 100 = Divide-by-16
- 011 = Divide-by-8
- 010 = Divide-by-4
- 001 = Divide-by-2
- 000 = Divide-by-1 (POR default setting)

bit 23-22 **Unimplemented:** Read as '0'

bit 21 **SLP2SPD:** Two-Speed Wake-up from Sleep bit(4)
- 1 = Device wakes up and runs on FRC clock until clock source selected by the NOSCx bits is ready, then it switches to the source selected by the NOSCx bits
- 0 = Device wakes up and does not run until the clock source selected by the NOSCx bits is ready

bit 20-15 **Unimplemented:** Read as '0'

bit 14-12 **COSC<2:0>:** Current Oscillator Selection bits(2)
- 111 = Reserved (selects FRC Oscillator with Postscaler (FRCDIV))
- 110 = Reserved (selects FRC Oscillator with Postscaler (FRCDIV))
- 101 = Low-Power RC Oscillator (LPRC)
- 100 = Secondary Oscillator (SOSC)
- 011 = Digitally Controlled Oscillator (DCO)
- 010 = Primary Oscillator (POSC; HS and EC modes)
- 001 = System PLL (SPLL; ECPLL, HSPLL and FRCPLL modes)
- 000 = FRC Oscillator with Postscaler (FRCDIV)

bit 11 **Unimplemented:** Read as '0'

Note 1: An unlock sequence is required before writing to this register. Refer to **Section 59.3.6.2 "Oscillator Switching Sequence"** for details.

2: Initial values are determined by the FNOSC<2:0> Configuration bits on device Reset. Definitions shown are typical, and may vary by device. For device-specific details, please refer to the **"Oscillator Configuration"** chapter in the device data sheet.

3: When the Fail-Safe Clock Monitor is enabled, writing a '1' to this bit will also cause a FSCM clock switchover.

4: Not implemented on all devices; refer to the specific device data sheet for more information.

Register 59-1: OSCCON: Oscillator Control Register(1) (Continued)

bit 10-8 **NOSC<2:0>:** New Oscillator Selection bits(2)
- 111 = Reserved (selects FRC Oscillator with Postscaler (FRCDIV))
- 110 = Reserved (selects FRC Oscillator with Postscaler (FRCDIV))
- 101 = Low-Power RC Oscillator (LPRC)
- 100 = Secondary Oscillator (SOSC)
- 011 = Digitally Controlled Oscillator (DCO)
- 010 = Primary Oscillator (POSC; HS and EC modes)
- 001 = System PLL (SPLL; ECPLL, HSPLL and FRCPLL modes)
- 000 = FRC Oscillator with Postscaler (FRCDIV)

bit 7 **CLKLOCK:** Clock Selection Lock Enable bit
- 1 = Clock and PLL configurations are locked (cleared only by device Reset)
- 0 = Clock and PLL configurations can be modified

When active, this bit prevents writes to the NOSC<2:0> and OSWEN bits.

bit 6-5 **Reserved:** Read as '0'

bit 4 **SLPEN:** Sleep Mode Enable bit
- 1 = Device will enter Sleep mode when a WAIT instruction is executed
- 0 = Device will enter Idle mode when a WAIT instruction is executed

bit 3 **CF:** Clock Fail Detect bit(3)
- 1 = FSCM has detected a clock failure
- 0 = No clock failure has been detected

bit 2 **Unimplemented:** Read as '0'

bit 1 **SOSCEN:** Secondary Oscillator (SOSC) Enable bit
- 1 = Enables SOSC
- 0 = Disables SOSC

The POR default is set by the FSOSCEN Configuration bit.

bit 0 **OSWEN:** Oscillator Switch Enable bit
- 1 = Initiates an oscillator switch to a selection specified by the NOSC<2:0> bits
- 0 = Oscillator switch is complete

Note 1: An unlock sequence is required before writing to this register. Refer to **Section 59.3.6.2 "Oscillator Switching Sequence"** for details.

2: Initial values are determined by the FNOSC<2:0> Configuration bits on device Reset. Definitions shown are typical, and may vary by device. For device-specific details, please refer to the **"Oscillator Configuration"** chapter in the device data sheet.

3: When the Fail-Safe Clock Monitor is enabled, writing a '1' to this bit will also cause a FSCM clock switchover.

4: Not implemented on all devices; refer to the specific device data sheet for more information.

Register 59-2: SPLLCON: System PLL Control Register(1,2)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	R/W-0(3)	R/W-0(3)	R/W-0(3)
	—	—	—	—	—	PLLODIV<2:0>		
23:16	U-0	U-0	U-0	U-0	U-0	R/W-0(3)	R/W-0(3)	R/W-0(3)
	—	—	—	—	—	PLLMULT<2:0>		
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-y	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0
	PLLICLK<1:0>(4,5)		—	—	—	—	—	—

Legend:	y = Value set from Configuration bits on POR		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-27 **Unimplemented:** Read as '0'

bit 26-24 **PLLODIV<2:0>:** SPLL Output Clock Divider bits(3)

111 = Divide-by-256
110 = Divide-by-64
101 = Divide-by-32
100 = Divide-by-16
011 = Divide-by-8
010 = Divide-by-4
001 = Divide-by-2
000 = Divide-by-1

bit 23-19 **Unimplemented:** Read as '0'

bit 18-16 **PLLMULT<2:0>:** System Clock PLL Multiplier bits(3)

111 = Reserved
110 = x24
101 = x12
100 = x8
011 = x6
010 = x4
001 = x3
000 = x2

bit 15-8 **Unimplemented:** Read as '0'

Note 1: An unlock sequence is required before writing to this register. Refer to **Section 59.3.6.2 "Oscillator Switching Sequence"** for details.

2: Writes to this register are not allowed if the SPLL is selected as the clock source (COSC<2:0> = 001).

3: Reset values for PLLODIVx and PLLMULTx are typical and may vary by device. Refer to the specific device data sheet for more information.

4: The POR default is specified by the FPLLICLK Configuration bit. Refer to the **"Special Features"** chapter in the specific device data sheet for details. Only the POSC and FRC can be selected as the PLL using the device Configuration bits.

5: The width of this field is device-dependent; refer to the specific device data sheet for more information.

Register 59-2: SPLLCON: System PLL Control Register(1,2) (Continued)

bit 7-6 **PLLICLK<1:0>:** SPLL Input Clock Source bits(4,5)

Bit Values when Bit 6 is Implemented:
11 = Reserved
10 = FRC
01 = DCO
00 = POSC

Bit 7 Values when Bit 6 is not Implemented:
1 = FRC
0 = POSC

bit 5-0 **Unimplemented:** Read as '0'

Note 1: An unlock sequence is required before writing to this register. Refer to **Section 59.3.6.2 "Oscillator Switching Sequence"** for details.

2: Writes to this register are not allowed if the SPLL is selected as the clock source (COSC<2:0> = 001).

3: Reset values for PLLODIVx and PLLMULTx are typical and may vary by device. Refer to the specific device data sheet for more information.

4: The POR default is specified by the FPLLICLK Configuration bit. Refer to the **"Special Features"** chapter in the specific device data sheet for details. Only the POSC and FRC can be selected as the PLL using the device Configuration bits.

5: The width of this field is device-dependent; refer to the specific device data sheet for more information.

Register 59-3: REFOCON: Reference Oscillator Control Register

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	RODIV<14:8>(1,3)						
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RODIV<7:0>(1,3)							
15:8	R/W-0	U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0, HC	R-0, HS, HC
	ON(4)	—	SIDL	OE	RSLP(2)	—	DIVSWEN	ACTIVE
7:0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	ROSEL<3:0>(1,3)			

Legend:	HC = Hardware Clearable bit	HS = Hardware Settable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **Unimplemented:** Read as '0'

bit 30-16 **RODIV<14:0>** Reference Clock Divider bits(1,3)

Output clock frequency is the source clock frequency divided by 2 * [RODIV<14:0> + (ROTRIM<8:0> ÷ 512)]. This value selects the reference clock divider bits. See Equation 59-2 for more information.

111111111111111 = Output clock is the source clock frequency divided by 65,534
111111111111110 = Output clock is the source clock frequency divided by 65,532
•
•
•
000000000000010 = Output clock is the source clock frequency divided by 4
000000000000001 = Output clock is the source clock frequency divided by 2
000000000000000 = Output clock is the same frequency as the source clock (no divider)

bit 15 **ON:** Output Enable bit(4)

1 = Reference oscillator module is enabled
0 = Reference oscillator module is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Peripheral Stop in Idle Mode bit

1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12 **OE:** Reference Clock Output Enable bit

1 = Reference clock is driven out on the REFCLKO pin
0 = Reference clock is not driven out on the REFCLKO pin

bit 11 **RSLP:** Reference Oscillator Module Run in Sleep bit(2)

1 = Reference oscillator module output continues to run in Sleep
0 = Reference oscillator module output is disabled in Sleep

bit 10 **Unimplemented:** Read as '0'

bit 9 **DIVSWEN:** Divider Switch Enable bit

1 = Divider switch is in progress
0 = Divider switch is complete

Note 1: Do not write ROSEL<3:0> and/or RODIV<14:0> while ACTIVE = 1, as undefined behavior may result.

2: This bit is ignored when ROSEL<3:0> = 0000 or 0001.

3: While ON = 1, writes to these bits do not take effect until DIVSWEN is set to '1'.

4: Do not write to this register when the ON bit is not equal to the ACTIVE bit.

Register 59-3: REFOCON: Reference Oscillator Control Register (Continued)

bit 8 **ACTIVE:** Reference Clock Request Status bit
1 = Reference clock request is active
0 = Reference clock request is not active

bit 7-4 **Unimplemented:** Read as '0'

bit 3-0 **ROSEL<3:0>:** Reference Clock Source Select bits(1,3)
1111 = Reserved; do not use
•
•
•
1001 = Reserved, do not use
1000 = REFCLKI pin
0111 = System PLL
0110 = DCO
0101 = SOSC
0100 = LPRC
0011 = FRC
0010 = POSC
0001 = Reserved
0000 = SYSCLK

Note 1: Do not write ROSEL<3:0> and/or RODIV<14:0> while ACTIVE = 1, as undefined behavior may result.
2: This bit is ignored when ROSEL<3:0> = 0000 or 0001.
3: While ON = 1, writes to these bits do not take effect until DIVSWEN is set to '1'.
4: Do not write to this register when the ON bit is not equal to the ACTIVE bit.

Register 59-4: REFOTRIM: Reference Oscillator Trim Register(1,2,3)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ROTRIM<8:1>							
23:16	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	ROTRIM0	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-23 **ROTRIM<8:0>:** Reference Oscillator Trim bits

Output clock frequency is the source clock frequency divided by 2 * [RODIV<14:0> + (ROTRIM<8:0> ÷ 512)]. This value selects the reference clock divider bits. See Equation 59-2 for more information.

111111111 = 511/512 divisor added to the RODIVx value
111111110 = 510/512 divisor added to the RODIVx value
•
•
•
100000000 = 256/512 divisor added to the RODIVx value
•
•
•
000000010 = 2/512 divisor added to the RODIVx value
000000001 = 1/512 divisor added to the RODIVx value
000000000 = 0/512 divisor added to the RODIVx value

bit 22-0 **Unimplemented:** Read as '0'

Note 1: While the ON bit (REFOCON<15>) is '1', writes to this register do not take effect until the DIVSWEN bit is set to '1'.

2: Do not write to this register when the ON bit (REFOCON<15>) is not equal to the ACTIVE bit (REFOCON<8>).

3: Specified values in this register do not take effect if RODIV<14:0> (REFOCON<30:16>) = 0.

Register 59-5: CLKSTAT: Clock Source Status Register

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R-0, HSC	R-0	R-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC
	SPLLRDY	—	LPRCRDY	SOSCRDY	DCORDY	POSCRDY	DIVSPLLRDY	FRCRDY

Legend:	HSC = Hardware Settable/Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **SPLLRDY:** System PLL (without postscaler) Clock Ready Status bit
1 = SPLL is stable and ready for use
0 = SPLL is not ready

bit 6 **Unimplemented:** Read as '0'

bit 5 **LPRCRDY:** Low-Power RC (LPRC) Clock Ready Status bit
1 = LPRC is stable and ready for use
0 = LPRC is not ready

bit 4 **SOSCRDY:** Secondary Oscillator (SOSC) Clock Ready Status bit
1 = SOSC is stable and ready for use
0 = SOSC is not ready

bit 3 **DCORDY:** Digitally Controlled Oscillator (DCO) Clock Ready Status bit
1 = DCO is stable and ready for use
0 = DCO is not ready

bit 2 **POSCRDY:** Primary Oscillator (POSC) Clock Ready Status bit
1 = POSC is stable and ready for use
0 = POSC is not ready

bit 1 **DIVSPLLRDY:** System PLL (with postscaler, SPLLDIV) Clock Ready Status bit
1 = SPLLDIV is stable and ready for use
0 = SPLLDIV is not ready

bit 0 **FRCRDY:** Fast RC Oscillator (FRC) Clock Ready Status bit
1 = FRC is stable and ready for use
0 = FRC is not ready

Register 59-6: OSCTUN: FRC Tuning Register(1)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	r-0	R/W-0	R/W-1	R-0	R/W-0	R-0	R/W-0
	ON(3)	—	SIDL(3)	SRC(3)	LOCK(3)	POL(3)	ORNG(3)	ORNGPOL(3)
7:0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	TUN<5:0>(2,4,5)					

Legend:	r = Reserved bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Self-Tune Enable bit(3)
- 1 = FRC self-tuning is enabled; the TUNx bits are controlled by hardware
- 0 = FRC self-tuning is disabled; the TUNx bits are readable and writable

bit 14 **Reserved:** Used by debugger

bit 13 **SIDL:** FRC Self-Tune Stop in Idle bit(3)
- 1 = Self-tuning stops during Idle mode
- 0 = Self-tuning continues during Idle mode

bit 12 **SRC:** FRC Self-Tune Reference Clock Source bit(3)
- 1 = The USB host clock is used to tune the FRC
- 0 = The 32.768 kHz SOSC clock is used to tune the FRC

bit 11 **LOCK:** FRC Self-Tune Lock Status bit(3)
- 1 = FRC accuracy is currently within ±0.2% of the STSRC reference accuracy
- 0 = FRC accuracy may not be within ±0.2% of the STSRC reference accuracy

bit 10 **POL:** FRC Self-Tune Lock Interrupt Polarity bit(3)
- 1 = A self-tune lock interrupt is generated when STLOCK is '0'
- 0 = A self-tune lock interrupt is generated when STLOCK is '1'

bit 9 **ORNG:** FRC Self-Tune Out of Range Status bit(3)
- 1 = STSRC reference clock error is beyond the range of TUN<5:0>; no tuning is performed
- 0 = STSRC reference clock is within the tunable range; tuning is performed

bit 8 **ORNGPOL:** FRC Self-Tune Out of Range Interrupt Polarity bit(3)
- 1 = A self-tune out of range interrupt is generated when STOR is '0'
- 0 = A self-tune out of range interrupt is generated when STOR is '1'

bit 7-6 **Unimplemented:** Read as '0'

Note 1: An unlock sequence is required before writing to this register. Refer to **Section 59.3.6.2 "Oscillator Switching Sequence"** for details.

2: Refer to the specific device data sheet for the minimum and maximum frequency deviation values.

3: This bit is not present on all devices; refer to the specific device data sheet for more information.

4: These bits are only writable when STEN = 0.

5: The number of bits in this field is device-dependent; refer to the specific device data sheet for more information.

Register 59-6: OSCTUN: FRC Tuning Register(1) (Continued)

bit 5-0 **TUN<5:0>:** FRC Oscillator Tuning bits(2,4,5)

100000 = Minimum frequency
100001 =
•
•
•
111111 =
000000 = Center frequency; oscillator runs at calibrated frequency (8 MHz)
000001 =
•
•
•
011110 =
011111 = Maximum frequency

Note 1: An unlock sequence is required before writing to this register. Refer to **Section 59.3.6.2 "Oscillator Switching Sequence"** for details.

2: Refer to the specific device data sheet for the minimum and maximum frequency deviation values.

3: This bit is not present on all devices; refer to the specific device data sheet for more information.

4: These bits are only writable when STEN = 0.

5: The number of bits in this field is device-dependent; refer to the specific device data sheet for more information.

Register 59-7: DCOCON: Digitally Controlled Oscillator Control Register

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-1
	—	—	ON	—	DCOFSEL<3:0>(3)			
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
	—	—	SIDL	—	—	—	—	—
7:0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	TUN<5:0>(1,2)					

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-30 **Unimplemented:** Read as '0'

bit 29 **ON:** Output Enable bit
1 = DCO is enabled and running
0 = DCO is disabled, but can be activated if a consumer module requests it

bit 28 **Unimplemented:** Read as '0'

bit 27-24 **DCOFSEL<3:0>:** DCO Frequency Select bits (refer to the device data sheet for frequency values)(3)

bit 23-14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** DCO Stop in Idle Mode bit
1 = Discontinues operation when device enters Idle mode
0 = Continues operation in Idle mode

bit 12-6 **Unimplemented:** Read as '0'

bit 5-0 **TUN<5:0>:** DCO Tuning bits(1,2)
100000 = Minimum frequency
100001 =
•
•
•
111111 =
000000 = Center frequency; oscillator runs at calibrated frequency
000001 =
•
•
•
011110 =
011111 = Maximum frequency

Note 1: Refer to the specific device data sheet for the minimum and maximum frequency deviation values.
2: The number of bits in this field is device-dependent; refer to the specific device data sheet for more information.
3: Refer to the specific device data sheet for available frequencies.

59.3 OPERATION: CLOCK GENERATION AND CLOCK SOURCES

The PIC32 family of devices has multiple internal clocks that are derived from internal or external clock sources. Some of these clock sources have Phase-Locked Loops (PLLs), a programmable output divider and/or an input divider to scale the input frequency to suit the application. The clock source can be changed on-the-fly by software. The Oscillator Control register is locked by hardware; it must be unlocked by a series of writes before software can perform a clock switch.

One clock source, the System Clock (SYSCLK), provides a single device clock to the CPU and most peripherals. A second source, the Reference Clock Generator (REFO), provides a user-configurable output clock to drive or synchronize external devices, and may also be used by some on-chip peripherals; it cannot be used as a System Clock source.

The clocks are derived from one of the following sources:

- Primary Oscillator (POSC) on the OSCI and OSCO Pins
- Secondary Oscillator (SOSC) on the SOSCI and SOSCO Pins
- Internal Fast RC (FRC) Oscillator
- Digitally-Controlled Oscillator (DCO)
- Internal Low-Power RC (LPRC) Oscillator

Each of the clock sources has unique configurable options, such as a PLL, an input divider and/or output divider, which are detailed in their respective sections.

Note:	Clock sources for peripherals that use external clocks, such as the Real-Time Clock and Calendar (RTCC) and Timer1, are covered in their respective family reference manual sections. Refer to **Section 14. "Timers"** (DS61105) and **Section 29. "Real-Time Clock and Calendar (RTCC)"** (DS61125) for further details.

59.3.1 System Clock (SYSCLK) Generation

The SYSCLK is derived from one of five clock sources:

- POSC
- SOSC
- Internal FRC Oscillator
- DCO
- LPRC Oscillator

Some of the clock sources have specific clock multipliers and/or divider options. No clock scaling is applied other than the user-specified values.

The SYSCLK source is selected by the device configuration and can be changed by software during operation. The ability to switch clock sources during operation allows the application to reduce power consumption by reducing the clock speed.

For a list of SYSCLK sources and how they can be combined with the System PLL to produce the SYSCLK, refer to Table 59-2.

Table 59-2: Clock Selection Configuration Bit Values

Oscillator Mode	Oscillator Source	Configuration Bits		PLLICLK<1:0>(5)	Notes
		POSCMOD<1:0>	FNOSC<2:0>		
FRC Oscillator with Postscaler (FRCDIV)	Internal	xx	111, 100, 000	xx	1, 2
LPRC Oscillator	Internal	xx	101	xx	1
SOSC (Timer1/RTCC)	Secondary	xx	100	xx	1
Digitally Controlled Oscillator (DCO)	Internal	xx	011	xx	—
POSC in HS mode with PLL Module (HSPLL)	Primary	10	001	10	3
POSC in EC mode with PLL Module (ECPLL)	Primary	00	001	10	3
POSC in HS mode	Primary	10	010	xx	—
POSC in EC mode	Primary	00	010	xx	—
FRC Oscillator with PLL Module (FRCPLL)	Internal	10	001	00	1
DCOPLL	Internal	01	010	10	3, 4

Note 1: When OSCO is not required by the Oscillator mode, it may be configured as a digital I/O pin using the OSCIOFNC Configuration bit.

2: FOSC<2:0> = 111 is the default Oscillator mode for an unprogrammed (erased) device.

3: When using the PLL modes, the input frequency to the PLL must be in the range that is specified in the **"Electrical Characteristics"** chapter in the specific device data sheet.

4: This option is not available on all devices; refer to the specific device data sheet for more information.

5: The number of bits in this field is device dependent; refer to the specific device data sheet for more information.

59.3.1.1 PRIMARY OSCILLATOR (POSC)

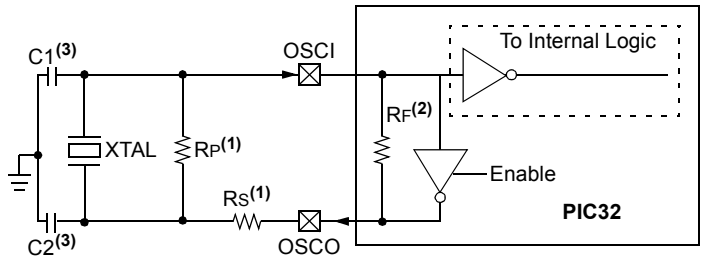
The Primary Oscillator (POSC) has four operating modes, as summarized in Table 59-3. The POSC is connected to the OSCI and OSCO pins in this device family. The POSC can be configured for an external clock input, or an external crystal or resonator. The POSCMD<1:0> Configuration bits determine the Primary Oscillator mode and the oscillator pin function. Figure 59-2 show various configurations of the POSC.

Table 59-3: Primary Oscillator Operating Modes

Oscillator Mode	Description
HS	High-Speed Crystal
EC	External Clock Input
HSPLL	Crystal, PLL Enabled
ECPLL	External Clock Input, PLL Enabled

Note: The clock applied to the CPU, after applicable prescalers, postscalers and PLL multipliers, must not exceed the maximum allowable processor frequency. Refer to the **"Electrical Characteristics"** chapter in the specific device data sheet for more information.

Figure 59-2: Crystal or Ceramic Resonator Operation (HS or HSPLL Oscillator Mode)



Note 1: A Series Resistor, Rs, may be required for AT strip cut crystals or to eliminate clipping. Alternatively, to increase oscillator circuit gain, add a Parallel Resistor, RP, with a value of 1 MΩ.

2: The internal Feedback Resistor, RF, is typically in the range of 2 MΩ to 10 MΩ.

3: See **Section 59.7.3.1 "Determining the Best Values for Oscillator Components"**.

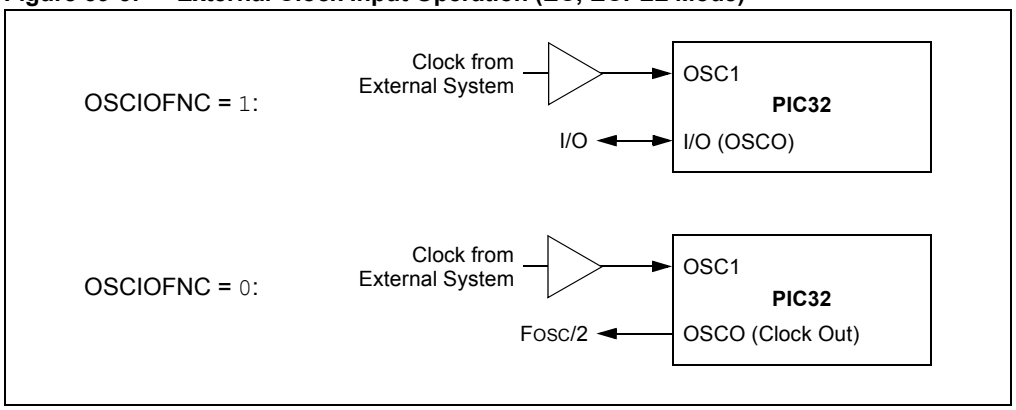
The HS and HSPLL modes are External Crystal or Resonator Controller Oscillator modes. OSCO provides crystal/resonator feedback in HS Oscillator mode and is not available for use as an input or output in this mode. The HSPLL mode uses the System Phase-Locked Loop (SPLL) with a user-selectable PLL multiplier and an output divider to provide a wide range of output frequencies. The oscillator circuit will consume more current when the PLL is enabled. For more information on the PLL, see **Section 59.3.2.1 "System Clock Phase-Locked Loop (SPLL)"**.

The External Clock modes, EC and ECPLL, allow the SYSCLK to be derived from an external clock source. The EC/ECPLL modes configure the OSCI pin as a high-impedance input that can be driven by a CMOS driver. The External Clock can be used to drive the SYSCLK directly (EC) or with the SPLL module (ECPLL mode) to change the clock frequency. For more information on the PLL, see **Section 59.3.2.1 "System Clock Phase-Locked Loop (SPLL)"**.

The External Clock mode also disables the internal feedback buffer, allowing the OSCO pin to be used for other functions: either as an additional device I/O pin or as a FOSC/2 output pin. The OSCIOFNC Configuration bit determines the pin function. By default (OSCIOFNC = 1), the OSCO pin functions as a digital port pin (see Figure 59-3).

Note: When using the PLL modes, the input frequency to the PLL must be in the range that is specified in the **"Electrical Characteristics"** chapter in the specific device data sheet.

Figure 59-3: External Clock Input Operation (EC, ECPLL Mode)



59.3.1.1.1 Primary Oscillator Configuration

To configure the POSC, perform the following steps:

1. Select the POSC as the default oscillator in the appropriate Configuration register by setting FNOSC<2:0> to '010' (without PLL) or to '001' (with PLL). If using the PLL, set the FPLLICLK Configuration bit so that the SYSCLK is driven by the PLL and the POSC, instead of the PLL and FRC.
2. Select the desired mode, HS or EC, using the POSCMOD<1:0> Configuration bits.
3. The values from the Configuration register are copied to the OSCCON register upon a device Reset. In addition, adjustments may be made during run time by modifying these registers.

Note 1:	Refer to the **"Special Features"** chapter in the specific device data sheet for information on device configuration.
2:	An unlock sequence is required before a write to the OSCCON register can occur. Refer to **Section 59.3.6.2 "Oscillator Switching Sequence"** for more information.

59.3.1.1.2 Oscillator Start-up Timer (OST)

In order to ensure that a crystal oscillator (or ceramic resonator) has started and stabilized, an Oscillator Start-up Timer (OST) is provided. The OST is a simple 10-bit counter that counts 1024 TOSC cycles before releasing the oscillator clock to the rest of the system. This time-out period is designated as TOST. The amplitude of the oscillator signal must reach the VIL and VIH thresholds for the oscillator pins before the OST can begin to count cycles.

The TOST interval is required every time the oscillator has to restart (i.e., on a Power-on Reset (POR), Brown-out Reset (BOR) or a wake-up from Sleep mode). The OST is applied to the HS mode for the POSC and the SOSC (see **Section 59.3.1.2 "Secondary Oscillator (SOSC)"**).

Note:	The Oscillator Start-up Timer is disabled when POSC is configured for EC mode or ECPLL mode.

59.3.1.1.3 Primary Oscillator Start-up from Sleep Mode

To ensure reliable wake-up from Sleep, care must be taken to design the Primary Oscillator circuit. This is because the load capacitors have both partially charged to some quiescent value and phase differential at wake-up is minimal. Therefore, more time is required to achieve stable oscillation. Also, low voltage, high temperatures and lower frequency clock modes also impose limitations on loop gain, which in turn, affects start-up.

Each of the following factors increases the start-up time:

- Low-frequency design (with a Low Gain Clock mode)
- Quiet environment (such as a battery-operated device)
- Operating in a shielded box (away from the noisy RF area)
- Low voltage
- High temperature
- Wake-up from Sleep mode

59.3.1.2 SECONDARY OSCILLATOR (SOSC)

The Secondary Oscillator (SOSC) is designed specifically for low-power operation with an external 32.768 kHz crystal. The oscillator is located on the SOSCO and SOSCI device pins and serves as a secondary crystal clock source for low-power operation. It can also drive Timer1 and/or the Real-Time Clock and Calendar (RTCC) module for Real-Time Clock (RTC) applications.

59.3.1.2.1 Enabling the SOSC

The SOSC is hardware-enabled by the SOSCEN bit (OSCCON<1>). Setting SOSCEN enables the oscillator; the SOSCO and SOSCI pins are controlled by the oscillator and cannot be used for port I/O or other functions.

Note:	An unlock sequence is required before a write to OSCCON can occur. Refer to **Section 59.3.6.2 "Oscillator Switching Sequence"** for more information.

The SOSC requires a warm-up period before it can be used as a clock source. When the oscillator is enabled, a warm-up counter increments to 1024. When the counter expires, the SOSCRDY bit (CLKSTAT<4>) is set to '1'. Refer to **Section 59.3.1.1.2 "Oscillator Start-up Timer (OST)"**.

59.3.1.2.2 SOSC Continuous Operation

The SOSC is always enabled when the SOSCEN bit (OSCCON<1>) is set. Leaving the oscillator running at all times allows a fast switch to the 32 kHz SYSCLK for lower power operation. Returning to the faster main oscillator will still require an oscillator start-up time if it is a crystal type source and/or uses the PLL (see **Section 59.3.1.1.2 "Oscillator Start-up Timer (OST)"**).

In addition, the oscillator will need to remain running at all times for Real-Time Clock applications and may be required for Timer1. Refer to **Section 14. "Timers"** (DS61105) and **Section 29. "Real-Time Clock and Calendar (RTCC)"** (DS61125) for further details.

Example 59-1: Enabling the SOSC

```
SYSKEY = 0x0;              // Ensure OSCCON is locked
SYSKEY = 0xAA996655;       // Write Key1 to SYSKEY
SYSKEY = 0x556699AA;       // Write Key2 to SYSKEY
                           // OSCCON is now unlocked
                           // Make the desired change
OSCCON |= 2;               // Enable Secondary Oscillator
                           // Relock the SYSKEY
SYSKEY = 0x0;              // Write any value other than Key1 or Key2
                           // OSCCON is relocked
```

59.3.1.2.3 SOSC External Clocking

The SOSC input to a peripheral can be used with an external clock source using the SCLKIN pin. When the SOSC is disabled, the SCLKIN pin becomes the SOSC input source for the system and peripherals that use the SOSC as a clock source.

59.3.1.3 INTERNAL DIGITALLY CONTROLLED OSCILLATOR (DCO)

The DCO is a low-power, fast starting (< 2 µs) internal oscillator that can be configured to operate at several fixed frequencies, from 1 to 32 MHz nominal. The desired frequency is selected using the DCOFSEL<3:0> bits (DCOCON<27:24>). The output frequency may be calibrated as required by up to +4.65%/-4.8% using the TUN<5:0> bits (DCOCON<5:0>).

By default, the DCO is only active when it is selected as the SYSCLK source or if another module requests it as a clock source. To avoid start-up delays or to use the DCO in Sleep mode, it can be kept running at all times by setting the ON bit (DCOCON<29>).

The DCORDY bit (CLKSTAT<3>) shows the status of the oscillator. When set, the DCO is ready to use.

59.3.1.3.1 DCO Oscillator with PLL Mode (DCOPLL)

The output of the DCO may also be combined with a user-selectable PLL multiplier and output divider to produce a SYSCLK across a wide range of frequencies. The DCO PLL mode is selected whenever the COSC<2:0> bits (OSCCON<14:12>) are '001' and the PLLICLK<1:0> bits (SPLLCON<7:6>) are '10'. The desired PLL multiplier and output divider values can be chosen to provide the desired device frequency. The user must ensure the DCO output frequency meets the minimum input frequency.

Note:	This PLL input source is not available on all devices. Consult the specific device data sheet for availability.

59.3.1.4 INTERNAL FAST RC (FRC) OSCILLATOR

The FRC oscillator is a fast (8 MHz nominal), user-trimmable, internal RC oscillator with a user-selectable input divider, PLL multiplier and output divider. Refer to the **"Oscillator Configuration"** chapter in the specific device data sheet for more information about the FRC oscillator.

59.3.1.4.1 FRC Postscaler Mode (FRCDIV)

Users are not limited to the nominal 8 MHz FRC output if they want to use the fast internal oscillator as a clock source. An additional FRC mode, FRCDIV, implements a selectable output divider that allows the choice of a lower clock frequency from seven different options, plus the direct 8 MHz output. The output divider is configured using the FRCDIV<2:0> bits (OSCCON<26:24>). Assuming a nominal 8 MHz output, available lower frequency options range from 4 MHz (divide-by-2) to 31 kHz (divide-by-256). The range of frequencies allows users the ability to save power at any time in an application by simply changing the FRCDIV<2:0> bits.

59.3.1.4.2 FRC Oscillator with PLL Mode (FRCPLL)

The output of the FRC may also be combined with a user-selectable PLL multiplier and output divider to produce a SYSCLK across a wide range of frequencies. The FRC PLL mode is selected whenever the COSC<2:0> bits are '001' and the PLLICLK<1:0> bits are '01'. The desired PLL multiplier and output divider values can be chosen to provide the desired device frequency.

59.3.1.4.3 FRC Oscillator Tuning Register (OSCTUN)

The FRC Oscillator Tuning register, OSCTUN, allows the user to fine-tune the FRC oscillator over a range of approximately ±12% (typical). Each bit increment or decrement changes the factory calibrated frequency of the FRC oscillator by a fixed amount.

Note:	An unlock sequence is required before a write to OSCTUN register can occur. Refer to **Section 59.3.6.2 "Oscillator Switching Sequence"** for more information.

59.3.1.4.4 FRC Self-Tune Active Clock Tuning

The FRC active clock tuning is an automatic mechanism to calibrate the FRC during run time. This system uses active clock tuning from a source of known accuracy to maintain the FRC within a very narrow margin of its nominal 8 MHz frequency. This allows for a frequency accuracy that is well within the requirements of the *"USB 2.0 Specification"* regarding full-speed USB devices.

Note:	The self-tune feature maintains sufficient accuracy for operation in USB Device mode. For applications that function as a USB host, a high-accuracy clock source (±0.05%) is still required.

The self-tune system is controlled by the bits in the OSCTUN register. Setting the STEN bit (OSCTUN<15>) enables the self-tuning feature, allowing the hardware to calibrate to a source selected by the STSRC bit (OSCTUN<12>). When STSRC = 1, the system uses the Start-of-Frame (SOF) packets from an external USB host for its source. When STSRC = 0, the system uses the crystal-controlled SOSC for its calibration source. Regardless of the source, the system uses the TUN<5:0> bits (OSCTUN<5:0>) to change the FRC oscillator's frequency. Frequency monitoring and adjustment is dynamic, occurring continuously during run time. While the system is active, the TUNx bits cannot be written to by software.

Note:	To use the USB as a reference clock tuning source (STSRC = 1), the device must be configured for USB device operation and connected to a non-suspended USB host or hub port. If the SOSC is to be used as the reference clock tuning source (STSRC = 0), the SOSC must be enabled for clock tuning to occur.

The self-tune system can generate a hardware interrupt, FSTIF. The interrupt can result from a drift of the FRC from the reference by greater than 0.2%, in either direction, or whenever the frequency deviation is beyond the ability of the TUNx bits to correct (i.e., greater than 1.5%). The STLOCK and STOR status bits (OSCTUN<11,9>) are used to indicate these conditions. The STPOL and STORPOL bits (OSCTUN<10,8>) configure the FSTIF interrupt to occur in the presence or absence of these conditions. It is the user's responsibility to test both the STLOCK and STOR bits to determine the exact cause of the interrupt.

Note:	The STLPOL and STORPOL bits should be ignored when the self-tune system is disabled (STEN = 0). FRC active clock tuning is not available on all devices.

59.3.1.5 INTERNAL LOW-POWER RC (LPRC) OSCILLATOR

The LPRC oscillator is separate from the FRC. It oscillates at a nominal frequency of 31.25 kHz. The LPRC oscillator is the clock source for the Watchdog Timer (WDT), Fail-Safe Clock Monitor (FSCM), Timer1 and the RTCC. It may also be used to provide a low-frequency clock source option for the device in those applications where power consumption is critical and timing accuracy is not required.

59.3.1.5.1 Enabling the LPRC Oscillator

The LPRC oscillator is disabled at a POR. It will be enabled if any one of the following is true:

- The Fail-Safe Clock Monitor is enabled
- The WDT is enabled
- The LPRC oscillator is selected as the SYSCLK (COSC<2:0> = 100)
- LPRC is the selected clock source for Timer1
- LPRC is the selected clock source for the RTCC

59.3.2 PLL Clock Generator

59.3.2.1 SYSTEM CLOCK PHASE-LOCKED LOOP (SPLL)

The System Clock PLL provides a user-configurable wide-range PLL multiplier and an output divider. The SPLL can be used with the HS and EC POSC modes, and with the Internal FRC Oscillator mode to create a variety of clock frequencies from a single clock source.

The values of the PLL multiplier and output divider are contained in the PLLMULT<2:0> and PLLODIV<2:0> bits, respectively, in the SPLLCON register (Register 59-2). The Reset values for these bits determine the default PLL configuration and are device-specific. At run time, the multiplier and output divider can be changed by software to scale the clock frequency to suit the application.

The input clock source for the SPLL is determined by the PLLICLK<1:0> bits (SPLLCON<7:6>). The SPLL input can be the FRC or POSC. When these bits are set, the SPLL uses the 8 MHz output of the FRC as its input. The default Reset value for the PLLICLKx bits is determined by the FPLLICLK Configuration bit. This allows the user to automatically determine the SPLL clock source on device Reset.

Note: The Configuration bits cannot select the DCO as the default PLL clock source.

Combinations of the PLL multiplier and output divider provide a combined multiplier of 1/128 to 24 times the input frequency. The SPLL output frequency is calculated as shown in Equation 59-1.

Equation 59-1: Calculating the SPLL Output Frequency

$$F_{SPLL} = \frac{F_{OSC} \bullet PLLMULT<2:0>}{2 \bullet PLLODIV<2:0>}$$

Where: F_{OSC} = Input Frequency (from POSC, FRC or DCO)
$PLLMULT<2:0>$ = Multiplier Value Selected by PLLMULT<2:0>
$PLLODIV<2:0>$ = Divider Value Selected by PLLODIV<2:0>

For reliable operation, the output of the PLL module must not exceed the maximum clock frequency of the device. The PLL input divider value should be chosen to limit the input frequency to the PLL to the range that is appropriate for the device.

To configure the SPLL:

1. Calculate the appropriate PLL multiplier and output divider values, based on the input frequency and the desired System Clock frequency.
2. Set the start-up clock source for the SPLL with the FPLLICLK Configuration bit when programming the device.
3. At run time, change the SPLL settings in the SPLLCON register as needed to suit the application.

Note: Refer to the **"Special Features"** chapter in the specific device data sheet for information on device configuration.

59.3.2.2 PLL LOCK STATUS

Due to the time required for the PLL to provide a stable output, the PLL Lock Status bit, SPLLRDY (CLKSTAT<7>), is provided. SPLLRDY indicates the lock status of the PLL. It is set automatically after a typical time delay for the PLL to achieve lock, also designated as T_{LOCK}. After the PLL has achieved a lock or the PLL start-up timer has expired, the bit is set. The bit will be set upon the expiration of the timer even if the PLL has not achieved a lock. The SPLLRDY bit is cleared on a POR and on clock switches when the PLL is selected as a destination clock source.

If the PLL does not stabilize during start-up, SPLLRDY may not reflect the status of the PLL lock, nor does it detect when the PLL loses lock during normal operation. It remains clear when any clock source not using the PLL is selected. Refer to the **"Electrical Characteristics"** chapter in the specific device data sheet for further information on the PLL lock interval.

59.3.3 Two-Speed Start-up

Two-Speed Start-up mode can be used to reduce the device start-up latency when using all External Crystal POSC modes, including PLL. Two-Speed Start-up uses the FRC clock as the SYSCLK source until the Primary Oscillator (POSC) has stabilized. After the user-selected oscillator has stabilized, the clock source will switch to POSC. This allows the CPU to begin running code at a lower speed while the oscillator is stabilizing. When the POSC has met the start-up criteria, an automatic clock switch occurs to switch to POSC.

This mode is enabled by the IESO Configuration bit. Refer to the **"Special Features"** chapter in the specific device data sheet for information on device configuration.

Two-Speed Start-up operates after a POR or on exit from Sleep. Software can determine the oscillator source currently in use by reading the COSC<2:0> bits (OSCCON<14:12>).

Note:	The Watchdog Timer (WDT), if enabled, will continue to count at the same rate regardless of the SYSCLK frequency. Care must be taken to service the WDT during Two-Speed Start-up, taking into account the change in SYSCLK.

59.3.4 Two-Speed Wake-up from Sleep

Two-speed wake-up from Sleep can be used to reduce the wake-up latency from Sleep when using external oscillators, the PLL or a combination of these. Two-Speed wake from Sleep uses the FRC clock as the SYSCLK until the desired clock source has stabilized. After the user-selected clock source has stabilized, the system will switch to the user-selected clock. This feature is controlled by the SLP2SPD bit (OSCCCON<13>).

The status of the clock switches can be monitored by firmware using the NOSCx, COSCx and OSWEN bits. When the device wakes up, COSCx will be '000', reflecting the FRC as the clock source. The NOSCx bits will be the value of the clock source before the device entered Sleep. When the oscillator source selected by the NOSCx bits is stable, the system will switch to that clock source. The OSWEN bit will be '1' until the switch to the source selected by NOSCx is complete.

Note:	This feature is not available on all devices; consult the device data sheet for availability.

59.3.5 Fail-Safe Clock Monitor (FSCM) Operation

The Fail-Safe Clock Monitor (FSCM) is designed to allow continued device operation if the current oscillator fails. The FSCM automatically switches the SYSCLK to an internal FRC oscillator if a failure is detected on the original clock source. The switch to an internal FRC oscillator allows continued device operation and the ability to retry the POSC or to execute code appropriate for a clock failure.

The FSCM feature is enabled by the FSCMEN Configuration bit. Any of the POSC modes can be used with FSCM. Refer to the **"Special Features"** chapter in the specific device data sheet for information on device configuration.

When a clock failure is detected by the FSCM, a Non-Maskable Interrupt (NMI) is generated. The Interrupt Service Routine (ISR) attached to the NMI can read the CF bit in the RMNICON register to detect that the NMI was generated by the FSCM. Refer to the **"Resets"** chapter in the specific device data sheet for details.

The FSCM module takes the following actions when a clock failure is detected:

1. The COSC<2:0> bits (OSCCON<14:12>) are loaded with '000'.
2. The CF bit (OSCCON<3>) is set to indicate the clock failure.
3. The OSWEN control bit (OSCCON<0>) is cleared to cancel any pending clock switches.

59.3.5.1 FSCM DELAY

On a POR, BOR or wake from a Sleep mode event, a nominal delay (TFSCM) may be inserted before the FSCM begins to monitor the SYSCLK source. The purpose of the FSCM delay is to provide time for the oscillator and/or PLL to stabilize. The FSCM delay will be generated after the internal System Reset signal, $\overline{\text{SYSRST}}$, has been released. Refer to **Section 7. "Resets"** (DS60001118) for FSCM delay timing information.

The TFSCM interval is applied whenever the FSCM is enabled and the HS, HSPLL or SOSC modes are selected as the SYSCLK.

Note:	Please refer to the **"Electrical Characteristics"** chapter in the specific device data sheet for TFSCM specification values.

59.3.5.2 FSCM AND SLOW OSCILLATOR START-UP

If the chosen device oscillator has a slow start-up time coming out of POR, BOR or Sleep mode, it is possible that the FSCM delay will expire before the oscillator has started. In this case, the FSCM will initiate a clock failure trap. As this happens, the COSC<2:0> bits (OSCCON<14:12>) are loaded with the FRC oscillator selection. This will effectively shut off the original oscillator that was trying to start. Software can detect a clock failure using the NMI ISR or by polling the CF bit (OSCCON<3>).

59.3.5.3 FSCM AND WDT

The FSCM and the WDT both use the LPRC oscillator as their time base. In the event of a clock failure on these devices, the WDT is unaffected and continues to run.

59.3.5.4 SOFTWARE TRIGGER OF FSCM

Triggering a FSCM switchover sequence through software is useful for the purpose of testing how the PIC32 application handles this event without having to physically remove a clock source.

To trigger a FSCM event in software, execute the following procedure:

1. Unlock the OSCCON register for writing using the unlock sequence, which is described in **Section 59.3.6.2 "Oscillator Switching Sequence"**.
2. Write a '1' to the CF bit (OSCCON<3>).

The NMI ISR will then be entered once the switchover has completed.

It is also possible to trigger the NMI ISR without actually switching the clock to the FRC. This is done by writing a '1' to the CF bit in the RNMICON register. Refer to **Section 7. "Resets"** (DS60001118) in the *"PIC32 Family Reference Manual"* for information.

59.3.5.5 CLEARING A FSCM EVENT CONDITION

The NMI handler procedure (`_nmi_handler`), which is available through the MPLAB® XC32 C Compiler, can be used to attempt a restart of the main oscillator.

59.3.6 Clock Switching Operation

With few limitations, applications are free to switch between any of the five clock sources (POSC, SOSC, FRC, LPRC and DCO) under software control and at any time. To limit the possible side effects that could result from this flexibility, PIC32 devices have a safeguard lock built into the switch process.

Note 1: Primary Oscillator mode has two different submodes (HS, and EC), which are determined by the POSCMOD<1:0> Configuration bits. While an application can switch to and from Primary Oscillator mode in software, it cannot switch between the different primary submodes without reprogramming the device. Refer to the **"Special Features"** chapter in the specific device data sheet for information on device configuration.

2: The user application should not change the PLL multiplier, prescaler or postscaler values when running from the affected PLL source. To perform any of these clock switching functions, the clock switch should be performed in two steps. The clock source should first be switched to a non-PLL source, such as FRC, and then switched to the desired source. This requirement only applies to PLL-based clock sources.

59.3.6.1 ENABLING CLOCK SWITCHING

To enable clock switching, the FSCMEN Configuration bit must be programmed to '1'.

The NOSC<2:0> Control bits (OSCCON<10:8>) do not control the clock selection when clock switching is disabled. However, the COSC<2:0> bits (OSCCON<14:12>) will reflect the clock source selected by the FNOSC<2:0> Configuration bits.

The OSWEN Control bit (OSCCON<0>) has no effect when clock switching is disabled; it is held at '0' at all times.

59.3.6.2 OSCILLATOR SWITCHING SEQUENCE

The unlock sequence unlocks all registers that are secured by the lock function. It is recommended that the amount of time the system is unlocked is kept to a minimum.The following is a recommended code sequence for a clock switch:

1. If desired, read the COSC<2:0> bits (OSCCON<14:12>) to determine the current oscillator source.
2. Disable interrupts and DMA prior to the system unlock sequence.
3. Execute the system unlock sequence by writing the key values of 0xAA996655 and 0x556699AA to the SYSKEY register in two back-to-back assembly or 'C' instructions.
4. Write the new oscillator source value to the NOSC<2:0> control bits.
5. Set the OSWEN bit in the OSCCON register to initiate the clock switch.
6. Optionally, write a non-key value (such as 0x00000000) to the SYSKEY register to perform a lock. Continue to execute code that is not clock-sensitive (optional).
7. Check if the OSWEN bit is '0'. If it is, the switch was successful. Loop until the bit is '0'.
8. Re-enable interrupts and DMA.

For an example of code to unlock the OSCCON register, refer to Example 59-1.

Note: There are no timing requirements for the steps other than the initial back-to-back writing of the key values to perform the unlock sequence.

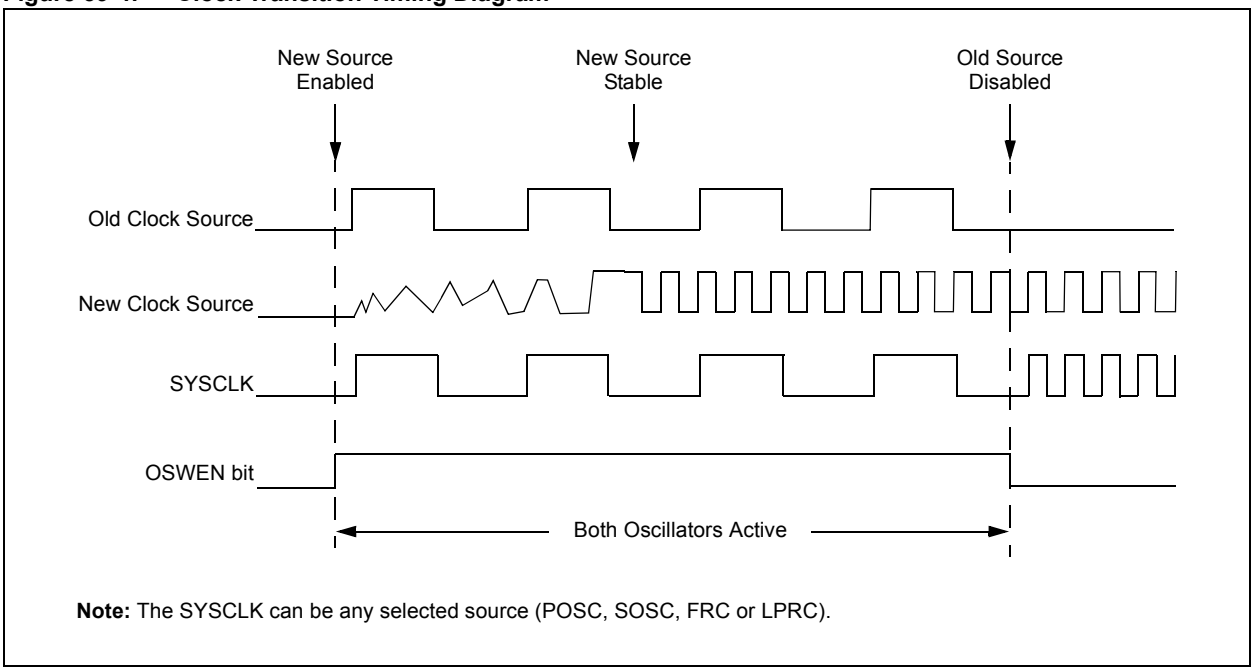
After the basic sequence is completed, the SYSCLK hardware responds automatically as follows:

1. The clock switching hardware compares the COSC<2:0> status bits with the new value of the NOSC<2:0> control bits. If they are the same, then the clock switch is a redundant operation. In this case, the OSWEN bit is cleared automatically and the clock switch is aborted.
2. The new oscillator is turned on by the hardware if it is not currently running. If a crystal oscillator must be turned on, the hardware will wait until the Oscillator Start-up Timer (OST) expires. If the new source is using the PLL, then the hardware waits until a PLL lock is detected (SPLLRDY = 1).
3. The hardware clears the OSWEN bit to indicate a successful clock transition. In addition, the NOSC<2:0> bit values are transferred to the COSC<2:0> status bits.
4. The old clock source is turned off at this time if the clock is not being used by any modules.

The transition timing between the clock sources is shown in Figure 59-4.

Note: The processor will continue to execute code throughout the clock switching sequence. Timing-sensitive code should not be executed during this time.

Figure 59-4: Clock Transition Timing Diagram



Note: The SYSCLK can be any selected source (POSC, SOSC, FRC or LPRC).

59.3.6.3 CLOCK SWITCHING CONSIDERATIONS

When incorporating clock switching into an application, consider the following issues when designing its code:

- The SYSKEY unlock sequence is not timing-critical. However, the two key values must be written back-to-back with no in-between peripheral register access. Prevent unintended peripheral register accesses by disabling all interrupts and DMA transfers.
- The system will not relock automatically. Perform the relock sequence as soon as possible after the clock switch.
- The unlock sequence unlocks other registers, such as the those related to Real-Time Clock control.
- If the destination clock source is a crystal oscillator, the clock switch time is dictated by the oscillator start-up time.
- If the new clock source does not start, or is not present, the OSWEN bit remains set.
- A clock switch to a different frequency affects the clocks to the peripherals. Peripherals may require reconfiguration to continue operation at the same rate as they did before the clock switch occurred.
- If the new clock source uses the PLL, a clock switch does not occur until a lock has been achieved.
- If the WDT is used, care must be taken to ensure it can be serviced in a timely manner at the new clock rate.

Note 1: When the Fail-Safe Clock Monitor is enabled, the application should not attempt to switch to a clock that has a frequency lower than 100 kHz. Clock switching in these instances may generate a false oscillator fail event and result in a switch to the FRC oscillator.

2: The user application should not change the PLL multiplier, prescaler or postscaler values when running from the affected PLL source. To perform either of the above clock switching functions, the clock switch should be performed in two steps. The clock source should first be switched to a non-PLL source, such as FRC, and then, switched to the desired source. This requirement only applies to PLL-based clock sources.

59.3.6.4 ENTERING SLEEP MODE DURING A CLOCK SWITCH

If, during a clock switch operation, the device enters Sleep mode, the clock switch operation is not aborted. If the clock switch does not complete before the device enters Sleep mode, the device will perform the switch when it exits Sleep, and then the code after the `WAIT` instruction executes normally.

59.3.7 Using the Secondary Oscillator with Peripherals

Although it is a low-power option, the Secondary Oscillator (SOSC) is also a precision oscillator because of its use of an external 32.768 kHz crystal connected to the SOSCI and SOSCO pins. Because of this, the SOSC can also be used as a dedicated clock source for the Real-Time Clock and Calendar (RTCC), and the Timer1 module. For the RTCC, the SOSC provides a precision time base for accurate timekeeping. For Timer1, the SOSC time base provides a precision reference for measuring the time intervals between events.

As it can be used by several peripherals as well as a System Clock, the SOSC is controlled by a combination of software and hardware. Setting the SOSCEN bit (OSCCON<1>) to '1' enables the SOSC. The SOSC is disabled when it is not being used by the CPU module and the SOSCEN bit is '0'. If the SOSC is being used as SYSCLK, such as after a clock switch, it cannot be disabled by writing a '0' to the SOSCEN bit. If the SOSC is enabled by the SOSCEN bit, it will continue to operate when the device is in Sleep. To prevent inadvertent clock changes, the OSCCON register is locked. It must be unlocked prior to software enabling or disabling the SOSC.

Note: If the RTCC or Timer1 is to be used when the CPU clock source is to be switched between SOSC and another clock source, the SOSCEN bit should be set to '1' in software. Failure to set the bit will cause the SOSC to be disabled when the CPU is switched to another clock source.

Due to the start-up time for an external crystal, the user should wait for stable SOCSC oscillator output before enabling the RTCC, or for using Timer1 for accurate measurements. Refer to the data sheet concerning the external crystal for information on the crystal's start-up time. Once the clock is stable, 256 cycles (approximately 8 ms) must pass before the RTCC module is turned on. The actual time required will depend on the crystal in use and the application.

There are numerous system and peripheral registers that are protected from inadvertent writes by the SYSREG lock. Performing a lock or unlock affects access to all registers protected by SYSREG, including the OSCCON register.

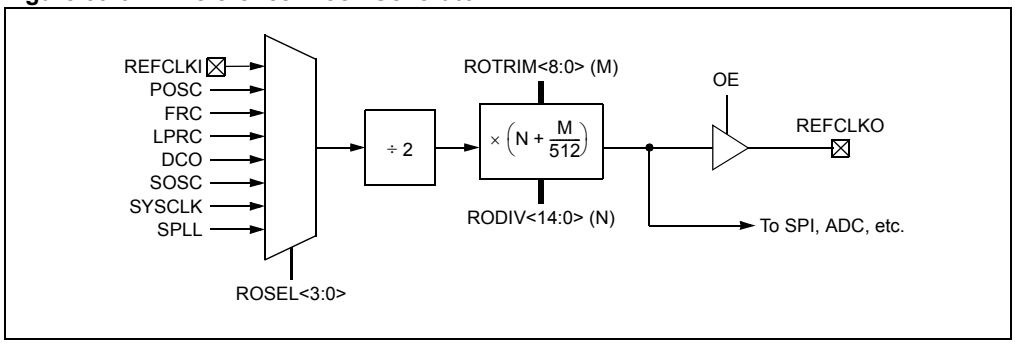
59.3.7.1 LPRC CONTROL AND RTCC

On certain PIC32 devices, the RTCC module can also be driven by the LPRC oscillator. If this is done, the timing of the RTCC module will not be accurate for date/time purposes.

59.3.8 Reference Clock Output

The reference clock output provides a clock signal on the REFCLKO pin. The reference clock can be selected from various clock sources. Refer to Figure 59-5 for a block diagram of the reference clock.

Figure 59-5: Reference Clock Generator



Depending on the particular device, these sources may include any of the following:

- External REFCLKI pin
- Internal FRC oscillator
- Internal LPRC oscillator
- DCO
- SOSC
- SYSCLK

The REFOCON and REFOTRIM registers (Register 59-3 and Register 59-4) control the operation of the reference clock output. The ROSEL<3:0> bits (REFOCON<3:0>) select between the available clock sources. After the clock source has been selected, it may be further divided by using the RODIV<14:0> bits (REFOCON<30:16>) and the ROTRIM<8:0> bits (REFOTRIM<31:23>). The formula for determining the final frequency output is shown in Equation 59-2.

Equation 59-2: Calculating Final Frequency Output

$$F_{REFOUT} = \frac{F_{REFIN}}{2 \cdot \left(N + \frac{M}{512}\right)}$$

Where: F_{REFOUT} = Output Frequency
F_{REFIN} = Input Frequency
N = Value of RODIV<14:0>
M = Value of ROTRIM<8:0>
When $N = 0$, the initial clock is the same as the input clock

For example, for an input frequency of 100 MHz, an N of 5 and an M of 256, the resulting frequency would be:

$$F_{REFOUT} = \frac{10MHz}{2 \cdot \left(5 + \frac{256}{512}\right)} \cong 909.1kHz$$

59.3.9 USB Operation

The USB module's clock input is the system PLL output prior to the postscaler. The USB module has a dedicated divide-by-2 prescaler (refer to Figure 59-1). To satisfy the USB requirement of a 48 MHz clock, the PLL VCO frequency must be 96 MHz. The PLL input source can be POSC, EC or FRC. Because of the timing requirements imposed by USB, a PLL VCO frequency of 96 MHz is required at all times while the USB module is enabled and not in a suspended operating state. The PLLODIV<2:0> bits are used to divide the 96 MHz VCO frequency down to provide SYSCLK frequency within the device operating range.

59.4 INTERRUPTS

The only interrupt generated by the oscillator module is a Non-Maskable Interrupt (NMI), which is detectable through a special Clock Fail Detect bit, CF, in the RNMICON register.

59.4.1 FSCM Non-Maskable Interrupt

The ISR attached to the NMI (i.e., `_nmi_handler`) can read the CF bit (RNMICON<1>) to detect that the FSCM has generated the NMI. Refer to the **"Resets"** chapter in the specific device data sheet for information on the RNMICON register and to determine whether the CF bit is available on your device.

59.5 OPERATION IN POWER-SAVING MODES

59.5.1 Oscillator Operation in Sleep Mode

Clock sources are disabled in Sleep unless they are being used by a peripheral. The following sections outline the behavior of each of the clock sources in Sleep mode.

59.5.1.1 PRIMARY OSCILLATOR (POSC) IN SLEEP MODE

The POSC is always disabled in Sleep. Start-up delays apply when exiting Sleep.

59.5.1.2 SECONDARY OSCILLATOR (SOSC) IN SLEEP MODE

The SOSC is disabled in Sleep unless the SOSCEN bit is set or it is in use by an enabled module that operates in Sleep. Start-up delays apply when exiting Sleep if the SOSC is not already running.

59.5.1.3 FAST RC (FRC) OSCILLATOR IN SLEEP MODE

The FRC oscillator is disabled in Sleep.

59.5.1.4 LOW-POWER (LPRC) OSCILLATOR IN SLEEP MODE

The LPRC oscillator is disabled in Sleep if the WDT is disabled.

59.5.2 Oscillator Operation in Idle Mode

Clock sources are not disabled in Idle mode. Start-up delays do not apply when exiting Idle mode.

59.5.3 Oscillator Operation in Debug Mode

The oscillator module continues to operate while the device is in Debug mode.

59.6 EFFECTS OF VARIOUS RESETS

On all forms of device Reset, OSCCON and SPLLCON are set to the default values, and the COSC<2:0> and PLLICLK<1:0> bits values are forced to the values defined in the device Configuration registers. The oscillator source is transferred to the source defined in the appropriate Configuration register. Oscillator start-up delays will apply.

Note:	Refer to the **"Special Features"** chapter in the specific device data sheet for information on device configuration.

59.7 CLOCKING GUIDELINES

59.7.1 Crystal Oscillators and Ceramic Resonators

In HS mode, a crystal or ceramic resonator is connected to the OSC1 and OSC2 pins to establish oscillation. The PIC32 oscillator design requires the use of a parallel cut crystal. Using a series cut crystal may give a frequency out of the crystal manufacturer's specifications.

In general, users should select the oscillator option with the lowest possible gain that still meets their specifications. This will result in lower dynamic currents (I_{DD}). The frequency range of each oscillator mode is the recommended frequency cutoff, but the selection of a different gain mode is acceptable as long as a thorough validation is performed (voltage, temperature and component variations, such as resistor, capacitor and internal oscillator circuitry).

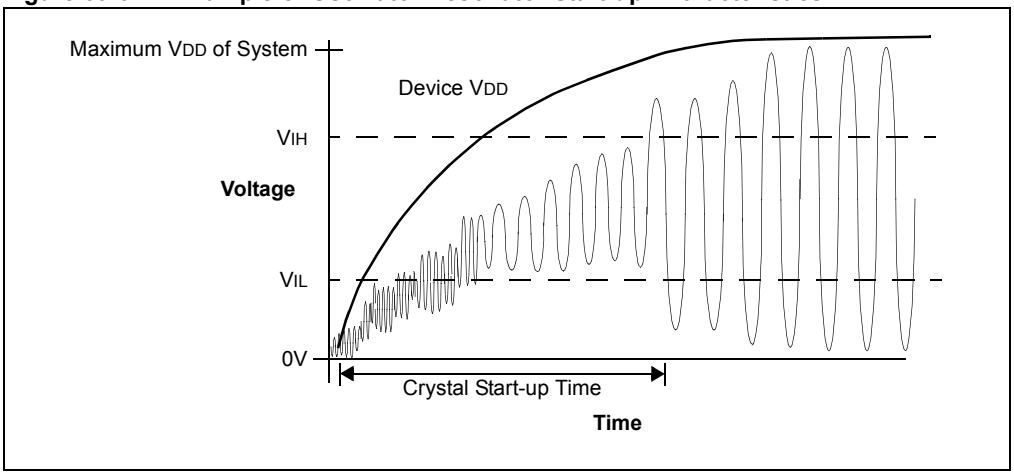
59.7.2 Oscillator/Resonator Start-up

As the device voltage increases from V_{SS}, the oscillator will start its oscillations. The time required for the oscillator to start oscillating depends on many factors, including the following:

- Crystal/resonator frequency
- Capacitor values used
- Series resistor, if used, and its value and type
- Device V_{DD} rise time
- System temperature
- Oscillator mode selection of device (selects the gain of the internal oscillator inverter)
- Crystal quality
- Oscillator circuit layout
- System noise

The course of a typical crystal or resonator start-up is shown in Figure 59-6. Notice that the time to achieve stable oscillation is not instantaneous. Refer to the **"Electrical Characteristics"** chapter in the specific device data sheet for further information regarding frequency range for each crystal mode.

Figure 59-6: Example of Oscillator/Resonator Start-up Characteristics



59.7.3 Tuning the Oscillator Circuit

Since Microchip devices have wide operating ranges (frequency, voltage and temperature; depending on the part and version ordered), and external components (crystals, capacitors, etc.) of varying quality and manufacture, validation of operation needs to be performed to ensure that the component selection will comply with the requirements of the application. There are many factors that go into the selection and arrangement of these external components. Depending on the application, these may include one of the following:

- Amplifier gain
- Desired frequency
- Resonant frequency of the crystal
- Temperature of operation
- Supply voltage range
- Start-up time
- Stability
- Crystal life
- Power consumption
- Simplification of the circuit
- Use of standard components
- Component count

59.7.3.1 DETERMINING THE BEST VALUES FOR OSCILLATOR COMPONENTS

The best method for selecting components is to apply a little knowledge and a lot of trial measurement and testing. Crystals are usually selected by their parallel resonant frequency only; however, other parameters may be important to your design, such as temperature or frequency tolerance. The Microchip application note, *AN588, "PIC® Microcontroller Oscillator Design Guide"* (DS00588), is an excellent reference from which to learn more about crystal operation.

The PIC32 internal oscillator circuit is a parallel oscillator circuit which requires that a parallel resonant crystal be selected. The load capacitance is usually specified in the 22 pF to 33 pF range. The crystal will oscillate closest to the desired frequency with a load capacitance in this range. It may be necessary to alter these values, as described later, in order to achieve other benefits.

C1 and C2 should be initially selected based on the load capacitance, as suggested by the crystal manufacturer, and the tables supplied in the device data sheet. The values given in the device data sheet can only be used as a starting point, since the crystal manufacturer, supply voltage, PCB layout and other factors already mentioned, may cause your circuit to differ from those used in the factory characterization process.

Ideally, the capacitance is chosen so that it will oscillate at the highest temperature and the lowest V_{DD} that the circuit will be expected to perform under. High-temperature and low V_{DD} both have a limiting effect on the loop gain, such that if the circuit functions at these extremes, the designer can be more assured of proper operation at other temperatures and supply voltage combinations. The output sine wave should not be clipped in the highest gain environment (highest V_{DD} and lowest temperature) and the sine output amplitude should be large enough in the lowest gain environment (lowest V_{DD} and highest temperature) to cover the logic input requirements of the clock as listed in the specific device data sheet.

A method for improving start-up is to use a value of C2 that is greater than the value of C1. This causes a greater phase shift across the crystal at power-up which speeds oscillator start-up. Besides loading the crystal for proper frequency response, these capacitors can have the effect of lowering loop gain if their value is increased. C2 can be selected to affect the overall gain of the circuit. A higher C2 can lower the gain if the crystal is being overdriven (also, see discussion on R_S). Capacitance values that are too high can store and dump too much current through the crystal, so C1 and C2 should not become excessively large. Measuring the wattage through a crystal is difficult, but if you do not stray too far from the suggested values, you should not have to be concerned with this.

A Series Resistor, RS, is added to the circuit if, after all other external components are selected to satisfaction, the crystal is still being overdriven. This can be determined by looking at the OSC2 pin, which is the driven pin, with an oscilloscope. Connecting the probe to the OSC1 pin will load the pin too much and negatively affect performance. Remember that a scope probe adds its own capacitance to the circuit, so this may have to be accounted for in your design (i.e., if the circuit worked best with a C2 of 22 pF and the scope probe was 10 pF, a 33 pF capacitor may actually be called for). The output signal should not be clipping or flattened. Overdriving the crystal can also lead to the circuit jumping to a higher harmonic level, or even crystal damage.

The OSC2 signal should be a clean sine wave that easily spans the input minimum and maximum of the clock input pin. An easy way to set this is to again test the circuit at the minimum temperature and maximum VDD that the design will be expected to perform in, then look at the output. This should be the maximum amplitude of the clock output. If there is clipping, or the sine wave is distorted near VDD and VSS, increasing load capacitors may cause too much current to flow through the crystal or push the value too far from the manufacturer's load specification. To adjust the crystal current, add a trimmer potentiometer between the crystal inverter output pin and C2, and adjust it until the sine wave is clean. The crystal will experience the highest drive currents at the low temperature and high VDD extremes.

The trimmer potentiometer should be adjusted at these limits to prevent overdriving. A Series Resistor, RS, of the closest standard value can now be inserted in place of the trimmer. If RS is too high, perhaps more than 20 kΩ, the input will be too isolated from the output, making the clock more susceptible to noise. If you find a value this high is needed to prevent overdriving the crystal, try increasing C2 to compensate or changing the oscillator operating mode. Try to get a combination where RS is around 10 kΩ or less and load capacitance is not too far from the manufacturer's specification.

59.8 RELATED APPLICATION NOTES

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the PIC32 device family, but the concepts are pertinent and could be used with modification and possible limitations. The current application notes related to the Oscillators with DCO module are:

Title	Application Note #
PIC® Microcontroller Oscillator Design Guide	AN588
Practical PIC® Microcontroller Oscillator Analysis and Design	AN943
Making Your Oscillator Work	AN949
Crystal Selection for Low-Power Secondary Oscillator	AN1798

Note: Please visit the Microchip web site (www.microchip.com) for additional application notes and code examples for the PIC32 family of devices.

59.9 REVISION HISTORY

Revision A (March 2015)

This is the initial version of this document.

Revision B (June 2015)

This revision incorporates the following updates:

- Figures:
  - Updated Figure 59-1
- Tables:
  - Updated Table 59-1 and Table 59-2
- Registers:
  - Updated Register 59-1, Register 59-2, Register 59-5, Register 59-6 and Register 59-7
- Equations:
  - Updated Equation 59-1
- Sections:
  - Updated **Section 59.3.1.2.3 “SOSC External Clocking”**, **Section 59.3.1.4.2 “FRC Oscillator with PLL Mode (FRCPLL)”**, **Section 59.3.1.5 “Internal Low-Power RC (LPRC) Oscillator”**, **Section 59.3.1.5.1 “Enabling the LPRC Oscillator”**, **Section 59.3.2.1 “System Clock Phase-Locked Loop (SPLL)”**, **Section 59.3.5.1 “FSCM Delay”**, **Section 59.3.5.5 “Clearing a FSCM Event Condition”**, **Section 59.3.6 “Clock Switching Operation”**, **Section 59.3.6.2 “Oscillator Switching Sequence”** and **Section 59.3.6.3 “Clock Switching Considerations”**
  - Inserted new **Section 59.3.1.3.1 “DCO Oscillator with PLL Mode (DCOPLL)”**, **Section 59.3.1.4.4 “FRC Self-Tune Active Clock Tuning”**, **Section 59.3.4 “Two-Speed Wake-up from Sleep”** and **Section 59.3.9 “USB Operation”**

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
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