Section 45. Control Digital-to-Analog Converter (CDAC)

HIGHLIGHTS

This section of the manual contains the following major topics:

Note:	This family reference manual section is meant to serve as a complement to device data sheets. Depending on the device variant, this manual section may not apply to all PIC32 devices. Please consult the note at the beginning of the **"Control Digital-to-Analog Converter (CDAC)"** chapter in the current device data sheet to determine whether this document supports the device you are using. Device data sheets and family reference manual sections are available for download from the Microchip Web site at: http://www.microchip.com

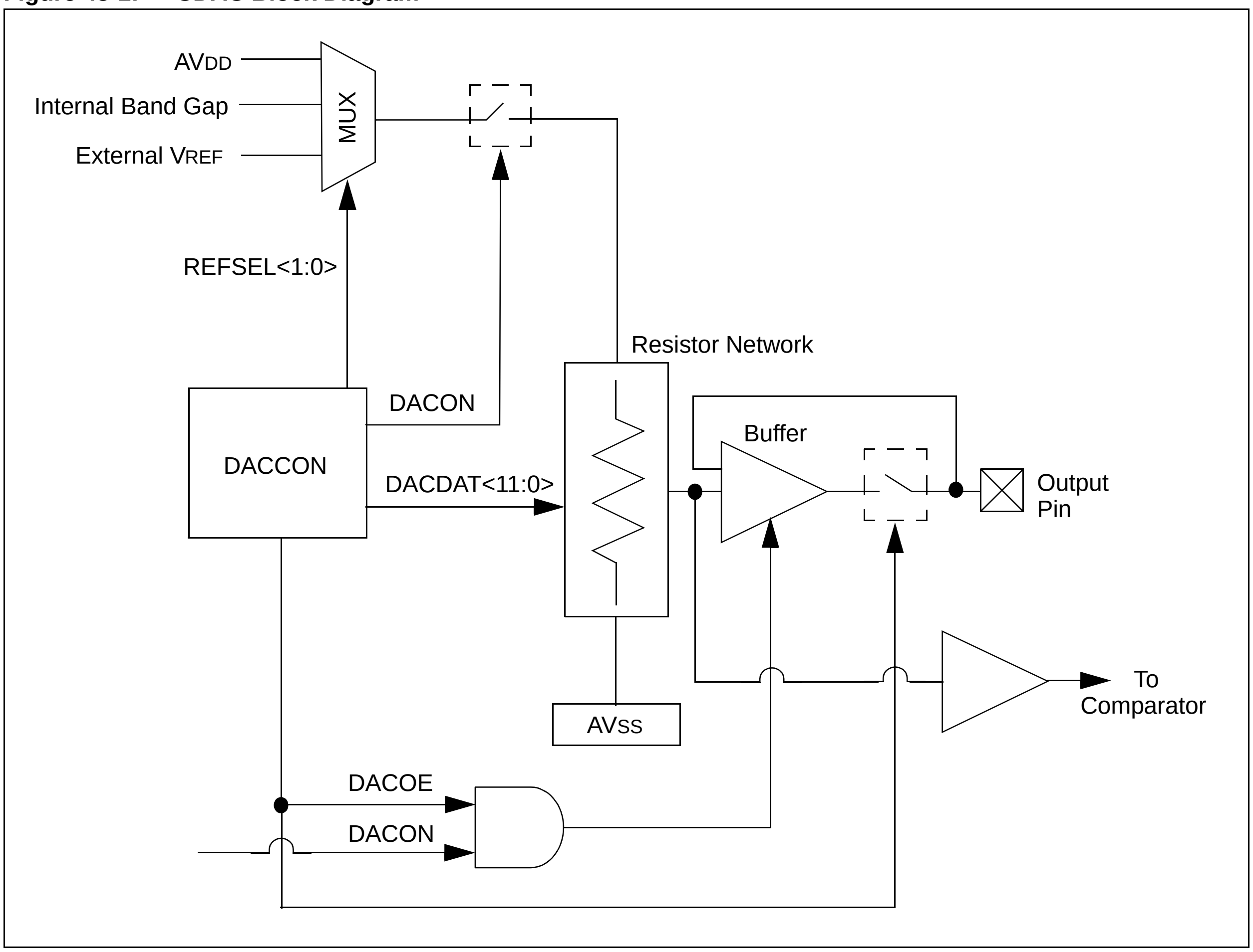
45.1 INTRODUCTION

The Control Digital-to-Analog Converter (CDAC) modules generate analog voltage corresponding to the digital inputs. The voltage can be used as a reference source for comparators or can be used as an offset to an Op amp. This module is targeted for control applications, as opposed to other DAC modules, which are used for audio applications.

Key features of this module include:

- Wide voltage range (Refer to electrical specification)
- 12-bit resolution
- Fast conversion times, 1 Msps
- Output of CDAC can be internally connected to Opamp/Comparator input as reference voltage.

Figure 45-1: CDAC Block Diagram



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45.2 CONTROL REGISTERS

The Control Digital-to-Analog Converter (CDAC) for PIC32 devices contains the following Special Function Registers (SFRs).

DACCONx: CDAC Control Register 'x' ('x' = 1 through 3)

These registers contain control bits for configuring and enabling the CDAC module, including the selection of the reference source.

Table 45-1 provides a brief summary of the related CDAC registers. The corresponding register table appears after the summary, followed by a detailed description of each bit.

Table 45-1: CDAC SFR Summary

Register Name	Bit Range	Bit 31/15	Bit 30/14	Bit 29/13	Bit 28/12	Bit 27/11	Bit 26/10	Bit 25/9	Bit 24/8	Bit 23/7	Bit 22/6	Bit 21/5	Bit 20/4	Bit 19/3	Bit 118/2	Bit 17/1	Bit 16/0
DACCON1	31:16	—	—	—	—	DACDAT<11:0>											
	15:0	DACON	—	—	—	—	—	—	DACOE	—	—	—	—	—	—	REFSEL<1:0>	
DACCON2	31:16	—	—	—	—	DACDAT<11:0>											
	15:0	DACON	—	—	—	—	—	—	DACOE	—	—	—	—	—	—	REFSEL<1:0>	
DACCON3	31:16	—	—	—	—	DACDAT<11:0>											
	15:0	DACON	—	—	—	—	—	—	DACOE	—	—	—	—	—	—	REFSEL<1:0>	

Legend: — = unimplemented, read as '0'.

Register 45-1: DACCONx: CDAC Control Register ‘x’ (‘x’ = 1 through 3)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	DACDAT<11:8>[1]			
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DACDAT<7:0>[1]							
15:8	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
	DACON[1]	—	—	—	—	—	—	DACOE[1]
7:0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	—	—	—	—	—	REFSEL<1:0>[1,2,3]	

Legend:	y = Value set from Configuration bits on POR		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-28 **Unimplemented:** Read as ‘0’

bit 27-14 **DACDAT<11:0>:** CDAC Data Port bits[1]
Data input register bits for the CDAC.

bit 15 **DACON:** CDAC Enable bit
1 = The CDAC is enabled
0 = The CDAC is disabled

bit 14-9 **Unimplemented:** Read as ‘0’

bit 8 **DACOE:** CDAC Output Buffer Enable bit
1 = Output is enabled; CDAC voltage is connected to the pin
0 = Output is disabled; drive to pin is floating

bit 7-2 **Unimplemented:** Read as ‘0’

bit 1-0 **REFSEL<1:0>:** Reference Source Select bits[1,2,3]
11 = Positive reference voltage = AV_{DD}
10 = Positive reference voltage = 2 * internal band gap reference voltage (2 * 1.2V nominal)
01 = Positive reference voltage = External V_{REF+} pin
00 = No reference selected (no reference current consumption)

Note 1: To minimize DAC start-up output transients, configure the DACDAT<11:0>, DACOE, and REFSEL<1:0> bits prior to enabling the DAC (prior to making DACON = 1). Also, remember to wait T_{ON} time, after enabling the DAC. This time is required to allow the DAC output to stabilize. Refer to the **“Electrical Characteristics”** chapter in the specific device data sheet for the T_{ON} specification.

2: If the DACON bit is ‘0’, the reference source is disconnected from the internal resistor network.

3: Not all options are available on all devices. Refer to the **“Control Digital-to-Analog Converter (CDAC)”** chapter in the specific device data sheet to determine availability.

45.3 MODULE OPERATION

The CDAC module is based on a resistor network. The value available on the DACDAT<11:0> bits (DACCONx<27:16>) is presented as the analog voltage output, based on Equation 45-1.

Equation 45-1:

$$Analog\ Voltage\ Output\ =\ \frac{DACCONx\text{<27:16>}}{4095} \bullet Reference\ Voltage$$

The CDAC module outputs the value only when the DACON bit (DACCONx<15>) is set. When the CDAC output is available on the pin, the buffer can source/sink a current in excess of 1 mA over the full output range. Refer to the **"Electrical Characteristics"** chapter in the specific device data sheet for the exact electrical specifications. If the bit is cleared, the output of CDAC is set to high-impedance (tri-stated regardless of the state of DACOE).

The output of the CDAC module to the pin is controlled by the DACOE bit (DACCONx<8>). The output of CDAC is active on the pin only if the DACOE bit is set in conjunction with DACON bit. If this bit is cleared, the CDAC output is disconnected from the pin and the pin goes into a high impedance state regardless of the state DACON bit.

45.3.1 Reference Selection

The analog output voltage of CDAC depends on the reference voltage that is applied to the resistor network. There are four possible selections available for the reference voltage, which can be made using the REFSEL<1:0> bits (DACCONx<1:0>):

- `11` = AV_{DD}
- `10` = Positive reference voltage = 2 * internal band gap reference voltage (2 * 1.2V nominal)
- `01` = Positive reference voltage, from external $V_{REF}+$ pin.
- `00` = No reference is selected to the resistor network. This can be used to reduce power consumption by CDAC module, when it is not being used.

Note:	When the DACON bit (DACCONx<15>) = `0`, this is equivalent to the REFSEL<1:0> bits (DACCONx<1:0>) = `00`.

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Control Digital-to-Analog Converter (CDAC)

45.4 POWER-SAVING MODE OPERATION

45.4.1 Module Disabled

If the CDAC module is disabled (DACON bit (DACCONx<15>) = 0), regardless of the state of the DACOE bit (DACCONx<8>), all analog circuitry is disabled; however, the SFRs can still be accessed.

45.4.2 Power-Saving Modes

On devices that are equipped with Deep Sleep mode, DAC circuits are powered down and DAC outputs are tri-stated.

Note:	Deep Sleep mode is not available on all devices. Please refer to the specific device data sheet to determine availability.

The DAC outputs are not effected by Sleep, Idle, or Doze modes.

45.5 RELATED APPLICATION NOTES

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the PIC32 device family, but the concepts are pertinent and could be used with modification and possible limitations. The current application notes related to Control Digital-to-Analog Converter (CDAC) include the following:

Title	Application Note #
No related application notes at this time.	N/A

> **Note:** Please visit the Microchip web site (www.microchip.com) for additional application notes and code examples for the PIC32 family of devices.

45.6 REVISION HISTORY

Revision A (May 2015)

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