Ziheng Ding

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EDUCATION

University of Wisconsin-Madison

Master of Science, Electrical and Computer Engineering, Sep. 2023-Dec. 2024

Coursework: VLSI Systems Design(ECE 755,Grade A), Introduction to Computer Architecture(ECE 552,Grade A), Embedded Computing Systems, Digital Circuits and Components, Introducing Computer Science to K-12 Students

Hong Kong University of Science and Technology (HKUST)

Bachelor of Science, Computer Engineering, Sep. 2019-Jun. 2023

Coursework: Introduction to Embedded Systems, Operating Systems, Signals and Systems, Fundamentals of Artificial Intelligence

SKILLS

CAD: Verilog, Cadence Virtuoso, CubeMX, Hspice

Hardware: STM32, Arduino

Programming Languages: Python, JavaScript, Java, C++, C

Others: MATLAB

ACADEMIC

Graph Neural Network (GNN) implementation

- Implemented the Verilog code for a deep neural network (DNN) that will be embedded into a graph
- Implemented the Verilog code for a GNN that embeds the previous DNN and testing with given input
- Synthesized the GNN design using Design Compiler and verify the synthesized netlist.
- Performed automatic place-and-route (APR)
- Post-APR - export GDS, import the GDS into Virtuoso layout, and perform DRC/LVS on the final layout of the design.
- Estimated performance based on matrices of power, area and speed.
- Implemented 3 versions with different clock period and adopted the 1500ps one.

Multi-layer Perceptron Design for Human Activity Recognition

- The perceptron takes two inputs, does weighted sum with the input and output the sum.
- Do schematic design and customized layout with Virtuoso.
- Conduct DRC and LVS check.
- Extract netlist file using xACT 3D and simulate the design with Hspice.
- Work in team of four, undertake the part of implementing the schematic and layout for a transistor-level XOR gate.
- Taking modularized approach by implementing 3-bit adder, 3-bit 2-to-1 MUX and simplified multiplier

Design and implement a processor

- Designing and implementing a 16-bit pipelined processor with full data forwarding as well as cache on both instruction and data memory using Verilog.
- Functionality-wise, covered arithmetic, memory and branch instructions. Format-wise, covered R-type, I-type and J-type instructions.
- Memory access takes multiple cycles that requires synchronization.
- Taking modularized approaches, design and test each component separately before integration.

EXPERIENCE

Voluntary research May 27th – on going

- Worked in the team of designing accelerators for Mamba architecture
- Explored SRAM generator with different technologies and adopted OpenRAM
- Explored on systolic array architecture for synthesizable implementations
- Currently seeking systolic array based approaches of Mamba implementations

Community based learning

Introducing Computer Science to K-12 Students

- Work in team-of-3 to lead Computer Science clubs and workshops for K-12 students at sites in the Madison area.
- Design and lead activities based on Scratch to help K-12 students learn computational thinking and computer programming.