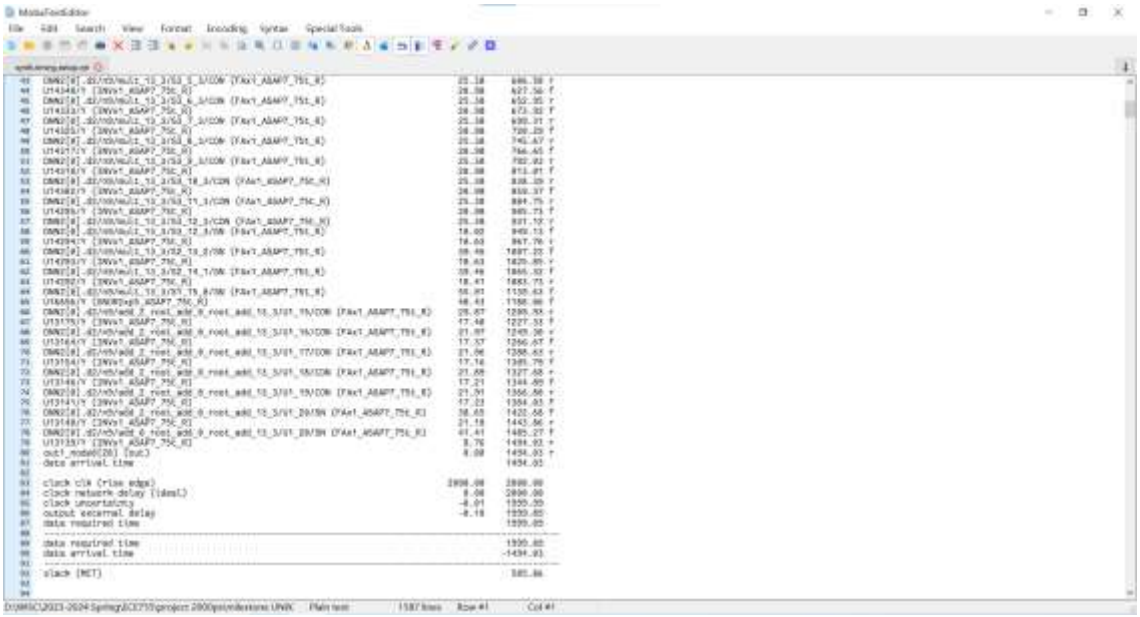
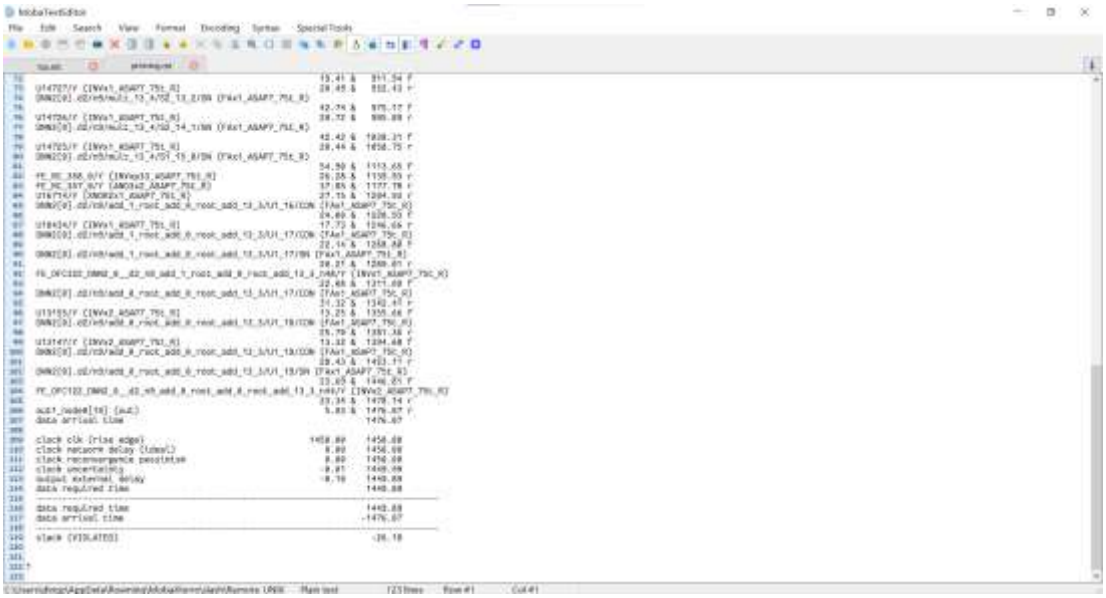
Designing a GNN Accelerator (SP24)

- We begin with the default 2000ps setup, which passes all phases successfully.
- Our initial optimization involves reducing the clock cycle to 1500ps. Upon reviewing the setup time report, we noticed more than 500 slack for each path, prompting us to cut 500ps from the clock.



- Subsequently, we aimed to push the circuit to its maximum speed by adjusting the constrain.tcl in milestone 3. Opting to start anew from milestone 3 instead of merely altering the clock in top.sdc was our choice because post-synthesis, the circuit's connections are fixed. While adjusting the clock can minimize slack, alternative structural changes might support higher frequencies. This approach led to a synthesis outcome supporting a 1200ps clock, with all other frequencies failing.
- Upon evaluating metrics, we determined that the 1500ps configuration was optimal. Although the 1200ps setup was the fastest, it compromised significantly on area and power. Comparing it with the original 2000ps setting, the area and power were similar, indicating that the speed increase did not trade off other aspects (see result tables for reference).



- Despite attempts to reduce the clock cycle by 50ps in the 1500ps case without re-synthesis, we encountered failure.
- We could further optimize by synthesizing with clock cycles of 1300 ps and 1400 ps, then comparing their statuses. Additionally, explicitly implementing multipliers and adders in Verilog at the hardware level could prove beneficial.
- We could improve by implementing pipelining.

The final results are shown below, we obtained the 1500ps one

Clock cycle (ps)	Cycle count	Frequency (MHz)	Area (Sq Microns)	Min latency (ns)	Power (mW)	Energy (pJ)	EDAP (pJns-mm2)
1500	40	666.67	99124.2256	60	3.29	4.935	29.3506832
2000	40	500.00	99124.2256	80	3.26	6.52	51.70319607

From the above result, we decided to keep the 1500 ps for better performance.

For comparison purposes we have explore different clock cycle.