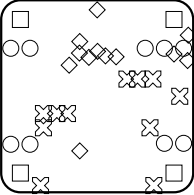


Drill Drawing View



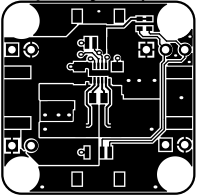
Drill Table

Symbol	Count	Hole Size	Plated	Hole Tolerance
○	9	1.00	Plated	
□	4	2.40	Non-Plated	
◇	12	0.30	Plated	
⊗	11	0.41	Plated	

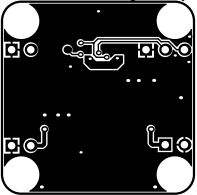
Layer Stack Legend

Material	Layer	Thickness	Dielectric Material	Type	Gerber
	Top Overlay			Legend	GTO
	Surface Material	0.03mm	SM-001	Solder Mask	GTS
PbSn	Top Surface Finish	0.02mm		Surface Finish	
CF-004	Top Layer	0.04mm		Signal	GTL
	Core	1.50mm	Core-043	Dielectric	
CF-004	Bottom Layer	0.04mm		Signal	GBL
PbSn	Bottom Surface Finish	0.02mm		Surface Finish	
Surface Material	Bottom Solder	0.03mm	SM-001	Solder Mask	GBS
	Bottom Overlay			Legend	GBO
Total thickness: 1.66mm					

Top Layer (Scale: 1:1)

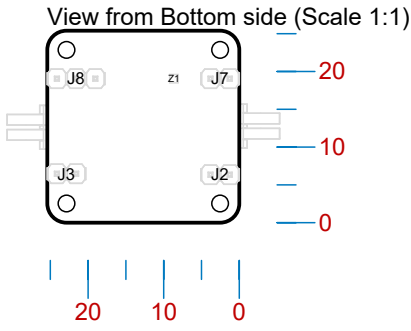
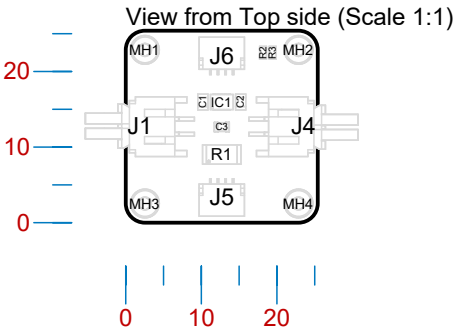


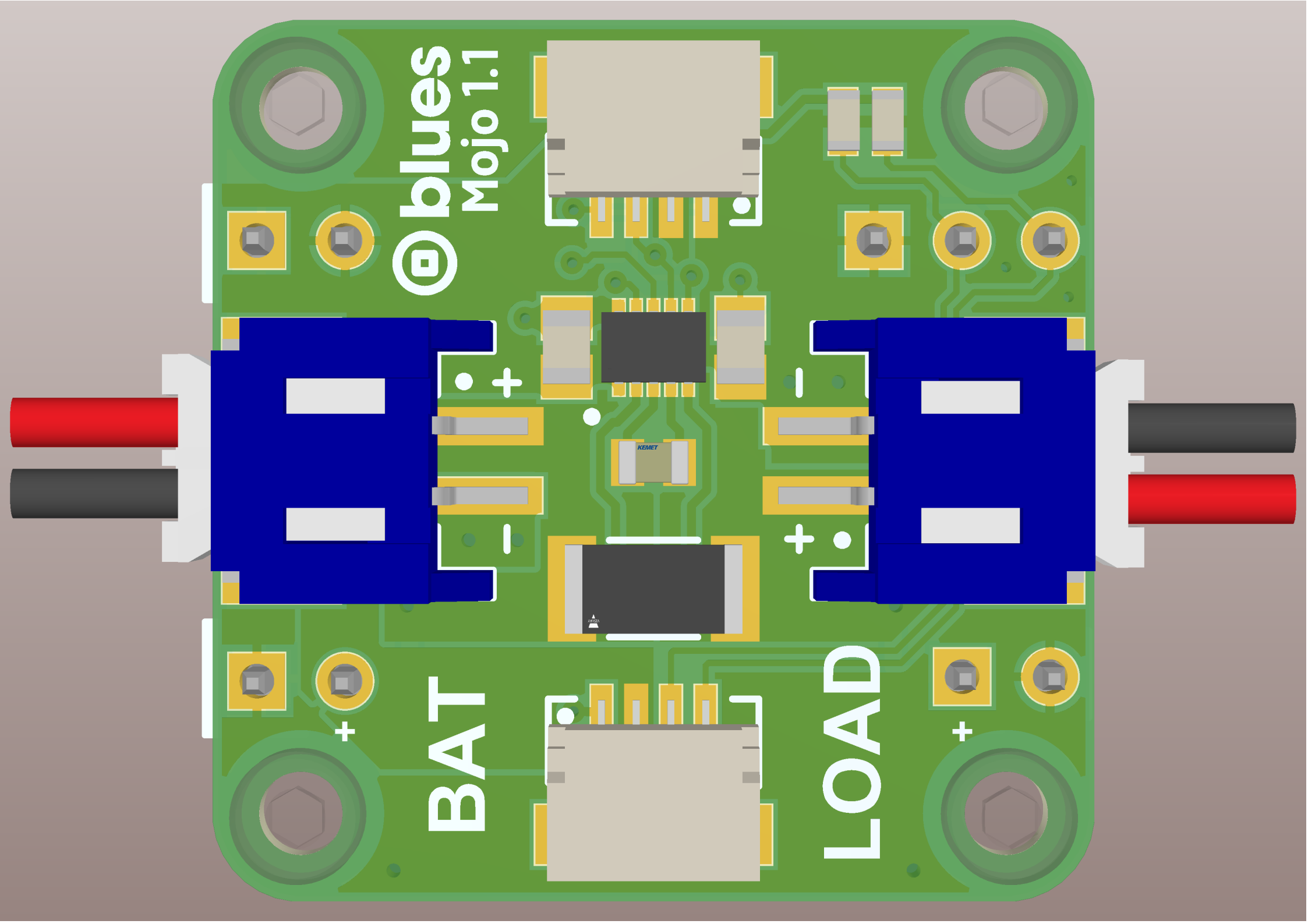
Bottom Layer (Scale: 1:1)



Bill Of Materials

Line #	Design Item Id	Designator	Name	Quantity	Supplier 1	Supplier Part Number 1	Layer	Center-X(mm)	Center-Y(mm)	Manufacturer Part Number 1
1	BAT-PH-ADAFRUIT-SMT-RA	J1, J4	20404	2			Top	4.856, 20.518	12.7	20404
2	CMP-1012-00659-3	R2, R3	RC0603FR-0722KL	2	Digikey	311-22.0KHRCT-ND	Top	18.161, 19.431	22.479	RC0603FR-0722KL
3	CMP-2007-00957-1	C1, C2	GRM216R61E105KA12D	2	Digikey	490-1700-1-ND	Top	10.2, 15.2	15.962	GRM216R61E105KA12D
4	CMP-2007-03659-2	C3	C0805C474K5RACTU	1	Digikey	399-C0805C474K5RAC7800CT-ND	Top	12.7	12.65	C0805C474K5RACTU
5	HEADER_AA_2	J2, J3, J7	Header 2-Pin, 0.100 in	3	Digikey	S1012E-02-ND	Bottom	2.54, 22.86	6.35, 6.477, 19.05	PEC02SAAN
6	HEADER_AA_3	J8	Header 3-Pin, 0.100 in	1	Digikey	S1012E-03-ND	Bottom	21.59	19.05	PEC03SAAN
7	LTC2959IDDB#TRMPBF	IC1	LTC2959IDDB#TRMPBF	1	Digikey	505-LTC2959IDDB#TRMPBFCT-ND	Top	12.7	15.962	LTC2959IDDB#TRMPBF
8	QWIIC_SM04B-SRSS	J5, J6	QWIIC SM04B-SRSS-TB(LF)(SN)	2	LCSC	C160404	Top	12.7	3.692, 21.708	SM04B-SRSS-TB(LF)(SN)
	RES_2020_0R250	R1	WSL2010R2500FEA	1	Digikey	WSLE-.25CT-ND	Top	12.7	9.017	WSL2010R2500FEA

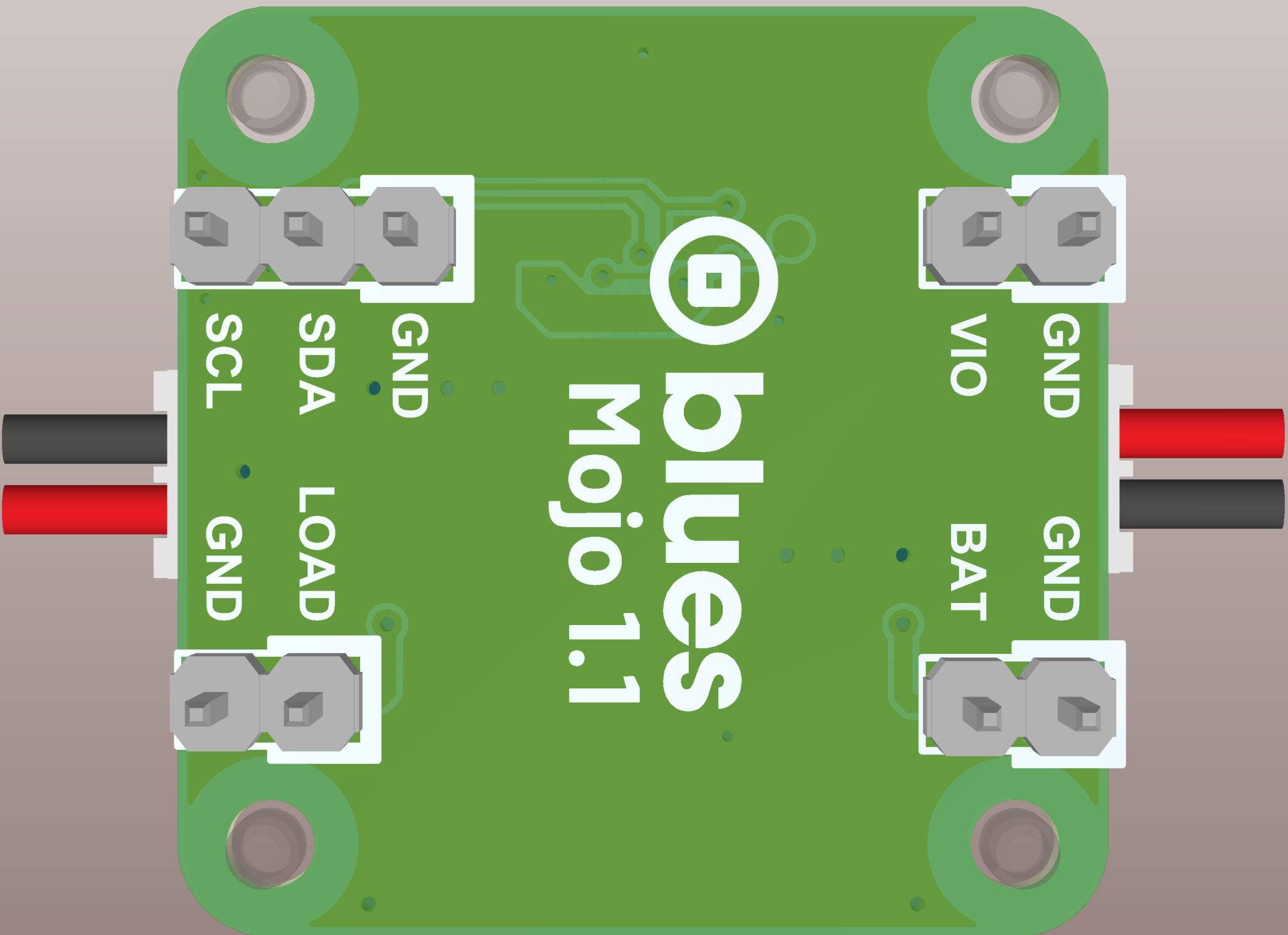




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# Blues Wireless

## Mojo 1.1

### v4

Version (Release Date) and Comments

- v1 (2024-03-11)

Initial Version
- v2 (2024-03-21)

Add 22K I2C SDA/SCL pullups  
3v3 labeled as "VIO" in serigraphy
- v3 (2024-04-15)

Changed sense resistor to 0R250.  
Reposition Vbat/Vout. Updated layout as needed.  
Moved GPIO test point to bottom and tented.  
Serigraphy changes.  
Updated battery connector to preferred supplier PN
- v4 (2024-06-07)

Made backside serigraphy bigger.

Variant Name	Description
Normal	Normal product configuration

+PROJECT ID

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