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Revision	Date	Author	Description
1	11/01/2023	S.KRAVITZ	First Draft
2	11/14/2023	S.KRAVITZ	Second Draft
3	1/3/2024	S.KRAVITZ	Third Draft - removed VIN, combined ideal diodes, all components on top Copied original project, now on Cygnet Feather v2
4	1/12/2024	S.KRAVITZ	PCB layout complete and ready for review
5	2/15/2024	S.KRAVITZ	Post design review, many changes
6	2/27/2024	S.KRAVITZ	PCB layout complete and ready for review
7	3/18/2024	S.KRAVITZ	Add "do not populate/ mount (DNM)" note to U4.8
8	4/4/2024	S.KRAVITZ	Change PU to PD and vv SWDIO/ SWCLK. Change PNs and footprints for J1, L1
9	4/15/2024	S.KRAVITZ	PU to +VIO change SWDIO
10	6/2/2024 - 7/11/2024	S.KRAVITZ	Various changes after manufacturing review

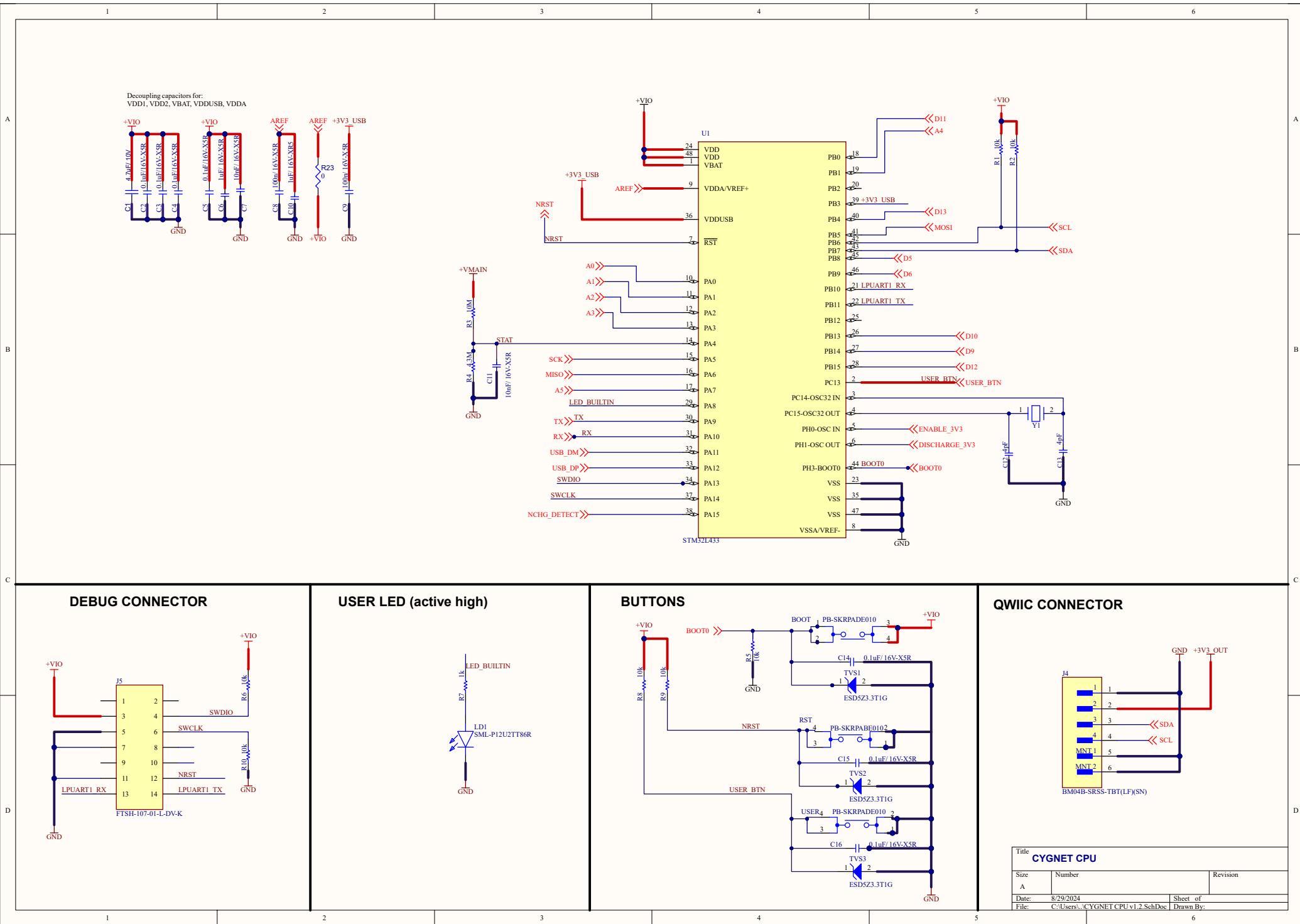


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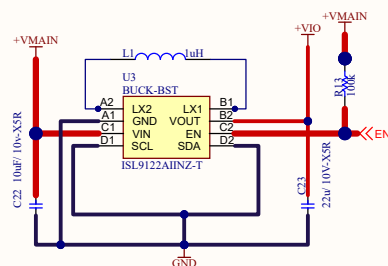
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CYGNET CPU		
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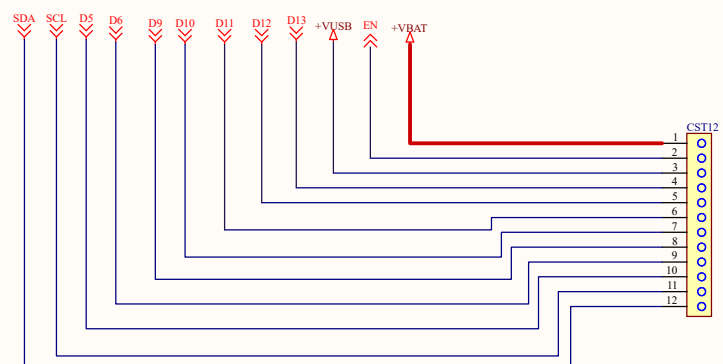
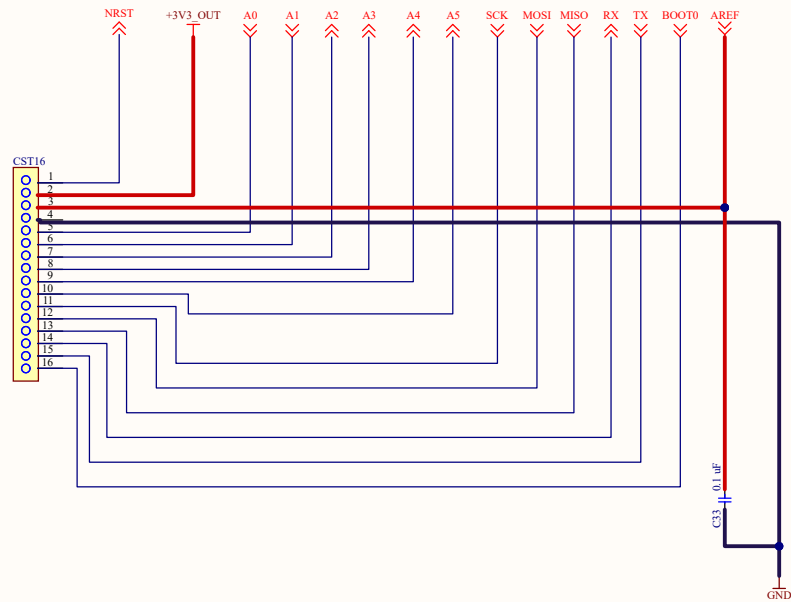
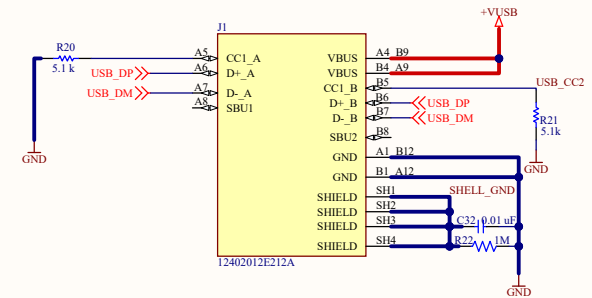
The schematic diagram illustrates the MCP73831-2ACI/MC circuit. It features a LiPo Battery (3.3V - 4.2V) connected to MP1 and MP2. The MCP73831-2ACI/MC (U5) is connected to +VBAT and +VUSB. The LD2 SML-P12WTT86R LED is connected to the output of the MCP73831-2ACI/MC. The circuit also includes capacitors C26 (4.7uF / 10V-XSR) and C27 (4.7uF / 10V-XSR), and resistors R17 (1k) and R18 (2.8k). The output of the circuit is labeled NCHG_DETECT.

AP2139AK-3.3TRG1

$I_{qmax}=1.5\mu A$
 $I_{sdmax}=1\mu A$
 $V_{EN-IH}=1.2V$
 $V_{EN-IL}=0.3V$
 $I_{PD-EN}=20\mu A$

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USB-C CONNECTOR



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CYGNET FEATHER CONNECTOR			
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