

# LMK00105 Ultra-Low Jitter LVC MOS Fanout Buffer and Level Translator With Universal Input

## 1 Features

- 5 LVC MOS Outputs, DC to 200 MHz
- Universal Input
  - LVPECL
  - LVDS
  - HCSL
  - SSTL
  - LVC MOS and LVTTL
- Crystal Oscillator Interface
  - Crystal Input Frequency: 10 to 40 MHz
- Output Skew: 6 ps
- Additive Phase Jitter
  - 30 fs at 156.25 MHz (12 kHz to 20 MHz)
- Low Propagation Delay
- Operates With 3.3 or 2.5-V Core Supply Voltage
- Adjustable Output Power Supply
  - 1.5 V, 1.8 V, 2.5 V, and 3.3 V for Each Bank
- 24-Pin WQFN Package (4.0 mm × 4.0 mm × 0.8 mm)

## 2 Applications

- LO Reference Distribution for RRU Applications
- SONET, Ethernet, Fibre Channel Line Cards
- Optical Transport Networks
- GPON OLT/ONU
- Server and Storage Area Networking
- Medical Imaging
- Portable Test and Measurement
- High-End A/V

## 3 Description

The LMK00105 is a high-performance, low-noise LVC MOS fanout buffer which can distribute five ultra-low jitter clocks from a differential, single-ended, or crystal input. The LMK00105 supports synchronous output enable for glitch-free operation. The ultra low-skew, low-jitter, and high PSRR make this buffer ideally suited for various networking, telecom, server and storage area networking, RRU LO reference distribution, medical and test equipment applications.

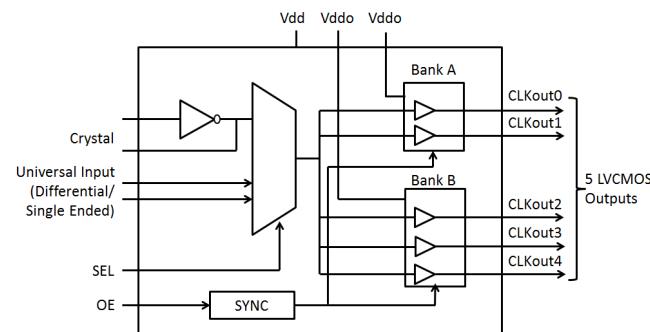
The core voltage can be set to 2.5 or 3.3 V, while the output voltage can be set to 1.5, 1.8, 2.5 or 3.3 V. The LMK00105 can be easily configured through pin programming.

### Device Information<sup>(1)</sup>

| PART NUMBER | PACKAGE   | BODY SIZE (NOM)   |
|-------------|-----------|-------------------|
| LMK00105    | WQFN (24) | 4.00 mm × 4.00 mm |

(1) For all available packages, see the orderable addendum at the end of the datasheet.

### Functional Block Diagram



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

## Table of Contents

|   |          |  |           |
|---|----------|--|-----------|
| <b>1 Features .....</b>                       | <b>1</b> | <b>8 Application and Implementation .....</b>                        | <b>12</b> |
| <b>2 Applications .....</b>                   | <b>1</b> | 8.1 Application Information.....                                     | 12        |
| <b>3 Description .....</b>                    | <b>1</b> | 8.2 Typical Applications .....                                       | 14        |
| <b>4 Revision History.....</b>                | <b>2</b> | <b>9 Power Supply Recommendations .....</b>                          | <b>20</b> |
| <b>5 Pin Configuration and Diagrams .....</b> | <b>4</b> | 9.1 Power Supply Filtering .....                                     | 20        |
| <b>6 Specifications.....</b>                  | <b>5</b> | 9.2 Power Supply Ripple Rejection.....                               | 20        |
| 6.1 Absolute Maximum Ratings .....            | 5        | 9.3 Power Supply Bypassing .....                                     | 21        |
| 6.2 ESD Ratings.....                          | 5        | <b>10 Layout.....</b>  | <b>21</b> |
| 6.3 Recommended Operating Conditions .....    | 5        | 10.1 Layout Guidelines .....   | 21        |
| 6.4 Thermal Information .....                 | 5        | 10.2 Layout Example .....  | 22        |
| 6.5 Electrical Characteristics.....           | 6        | 10.3 Thermal Management.....   | 22        |
| 6.6 Typical Characteristics .....             | 8        | <b>11 Device and Documentation Support .....</b>                     | <b>23</b> |
| <b>7 Detailed Description .....</b>           | <b>9</b> | 11.1 Documentation Support .....                                     | 23        |
| 7.1 Overview .....                            | 9        | 11.2 Trademarks .....  | 23        |
| 7.2 Functional Block Diagram .....            | 9        | 11.3 Electrostatic Discharge Caution .....                           | 24        |
| 7.3 Feature Description.....                  | 9        | 11.4 Glossary .....  | 24        |
| 7.4 Device Functional Modes.....              | 11       | <b>12 Mechanical, Packaging, and Orderable<br/>Information .....</b> | <b>24</b> |

## 4 Revision History

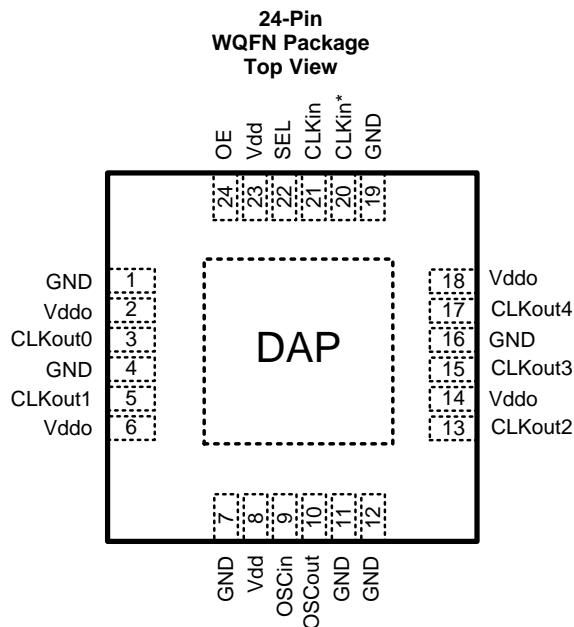
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision F (May 2013) to Revision G   | Page |
|--|------|
| • Added <i>Pin Configuration and Functions</i> section, <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section ..... | 1    |

| Changes from Revision E (February 2013) to Revision F   | Page |
|---|------|
| • Added device name to title of document .....  | 1    |
| • Changed all LLP and QFN packages to WQFN throughout document.....   | 1    |
| • Deleted optional from CLKin* pin description. And changed complimentary to complementary .....  | 4    |
| • Added max limit to Output Skew parameter and added tablenote to parameter in Electrical Characteristics Table.....  | 6    |
| • Changed typical value for both conditions of Propagation Delay in the Electrical Characteristics Table. ....  | 6    |
| • Added Min/Max limits to both conditions of Propagation Delay parameter in Electrical Characteristics Table. ....  | 6    |
| • Changed unit value for the first condition of Part-to-part Skew from ps to ns in the Electrical Characteristics Table. ....   | 6    |
| • Changed both Max values of each Part-to-part Skew condition in Electrical Characteristics Table.....  | 6    |
| • Changed the Typ value of each Rise/Fall Time condition in the Electrical Characteristics Table. ....  | 6    |
| • Deleted V <sub>IL</sub> table note .....  | 7    |
| • Added V <sub>I_SE</sub> parameter and spec limits with corresponding table note to Electrical Characteristics Table. ....   | 7    |
| • Added CLKin* column to <i>CLKin Input vs. Output States</i> table. Also added fourth row starting with Logic Low under CLKin column. ....   | 10   |
| • Changed table title from <i>CLKin input vs. Output States</i> to <i>OSCin Input vs. Output States</i> .....   | 10   |
| • Changed third paragraph in <i>Driving the Clock Inputs</i> section to include CLKin* and LVCMS text. Removed extra references to other figures. Revised to better correspond with information in Electrical Characteristics Table. .... | 12   |
| • Deleted Figure 10 ( <i>Near End termination</i> ) and Figure 11 ( <i>Far End termination</i> ) from <i>Driving the Clock Inputs</i> section....   | 12   |
| • Changed bypass cap text to signal attenuation text of the fourth paragraph in <i>Driving the Clock Inputs</i> section. ....   | 12   |
| • Changed <i>Single-Ended LVCMS Input, DC Coupling with Common Mode Biasing</i> image with revised graphic.....   | 13   |
| • Deleted sentence in reference to two deleted images. ....   | 13   |

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- Changed link from National packaging site to TI packaging site..... [22](#)
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## 5 Pin Configuration and Diagrams



### Pin Functions

| PIN     |                        | TYPE   | DESCRIPTION   |
|---------|------------------------|--------|---|
| NAME    | NO                     |        |   |
| DAP     | DAP                    | —      | The DAP should be grounded  |
| Vddo    | 2, 6                   | Power  | Power Supply for Bank A (CLKout0 and CLKout 1) CLKout pins.                       |
| CLKout0 | 3                      | Output | LVCMOS Output   |
| GND     | 1,4,7,11,<br>12, 16,19 | GND    | Ground  |
| CLKout1 | 5                      | Output | LVCMOS Output   |
| Vdd     | 8,23                   | Power  | Supply for operating core and input buffer  |
| OSCin   | 9                      | Input  | Input for Crystal   |
| OSCout  | 10                     | Output | Output for Crystal  |
| CLKout2 | 13                     | Output | LVCMOS Output   |
| Vddo    | 14,18                  | Power  | Power Supply for Bank B (CLKout2 to CLKout 4) CLKout pins                         |
| CLKout3 | 15                     | Output | LVCMOS Output   |
| CLKout4 | 17                     | Output | LVCMOS Output   |
| CLKin*  | 20                     | Input  | Complementary input pin   |
| CLKin   | 21                     | Input  | Input Pin   |
| SEL     | 22                     | Input  | Input Clock Selection. This pin has an internal pulldown resistor. <sup>(1)</sup> |
| OE      | 24                     | Input  | Output Enable. This pin has an internal pulldown resistor. <sup>(1)</sup>         |

(1) CMOS control input with internal pulldown resistor.

## 6 Specifications

### 6.1 Absolute Maximum Ratings<sup>(1)</sup>

|                  |                               | MIN  | MAX       | UNIT |
|------------------|-------------------------------|------|-----------|------|
| Vdd              | Core Supply Voltage           | -0.3 | 3.6       | V    |
| Vddo             | Output Supply Voltage         | -0.3 | 3.6       | V    |
| V <sub>IN</sub>  | Input Voltage                 | -0.3 | Vdd + 0.3 | V    |
| T <sub>L</sub>   | Lead Temperature (solder 4 s) |      | 260       | °C   |
| T <sub>J</sub>   | Junction Temperature          |      | 125       | °C   |
| T <sub>stg</sub> | Storage temperature           | -65  | 150       | °C   |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 6.2 ESD Ratings

|                    |                         | VALUE  | UNIT  |
|--------------------|-------------------------|--|-------|
| V <sub>(ESD)</sub> | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>              | ±2500 |
|                    |                         | Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup> | ±1000 |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.  
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

|                | MIN   | TYP | MAX  | UNIT |
|----------------|-------|-----|------|------|
| T <sub>A</sub> | -40   | 25  | 85   | °C   |
| Vdd            | 2.375 | 3.3 | 3.45 | V    |
| Vddo           | 1.425 | 3.3 | Vdd  | V    |

- (1) V<sub>ddo</sub> should be less than or equal to V<sub>dd</sub> (V<sub>ddo</sub> ≤ V<sub>dd</sub>)

### 6.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> | LMK00105                                     | UNIT |
|-------------------------------|--|------|
|                               | RTW  |      |
|                               | 24 PINS                                      |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance       | 46.7 |
| R <sub>θJC(top)</sub>         | Junction-to-case (top) thermal resistance    | 50.3 |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance         | 25.5 |
| Ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | 1.9  |
| Ψ <sub>JB</sub>               | Junction-to-board characterization parameter | 25.6 |
| R <sub>θJC(bot)</sub>         | Junction-to-case (bottom) thermal resistance | 13.6 |

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

## 6.5 Electrical Characteristics

( $2.375 \leq V_{dd} \leq 3.45$  V,  $1.425 \leq V_{ddo} \leq V_{dd}$ ,  $-40^\circ C \leq T_A \leq 85^\circ C$ , Differential inputs. Typical values represent most likely parametric norms at  $V_{dd} = V_{ddo} = 3.3$  V,  $T_A = 25^\circ C$ , at the Recommended Operation Conditions at the time of product characterization and are **not** ensured). Test conditions are:  $F_{test} = 100$  MHz, Load = 5 pF in parallel with  $50\ \Omega$  unless otherwise stated.

|   | PARAMETER   | TEST CONDITIONS  | MIN                   | TYP                   | MAX  | UNIT |
|---|---|--|-----------------------|-----------------------|------|------|
| <b>TOTAL DEVICE CHARACTERISTICS</b>         |   |  |                       |                       |      |      |
| Vdd   | Core Supply Voltage                                 |  | 2.375                 | 2.5 or 3.3            | 3.45 | V    |
| Vddo  | Output Supply Voltage                               |  | 1.425                 | 1.5, 1.8, 2.5, or 3.3 | Vdd  | V    |
| I <sub>Vdd</sub>                            | Core Current  | No CLKin   |                       | 16                    | 25   | mA   |
|   |   | V <sub>ddo</sub> = 3.3 V, F <sub>test</sub> = 100 MHz  |                       | 24                    |      |      |
|   |   | V <sub>ddo</sub> = 2.5 V, F <sub>test</sub> = 100 MHz  |                       | 20                    |      |      |
| I <sub>Vddo[n]</sub>                        | Current for Each Output                             | V <sub>ddo</sub> = 2.5 V,<br>OE = High, F <sub>test</sub> = 100 MHz  |                       | 5                     |      | mA   |
|   |   | V <sub>ddo</sub> = 3.3 V,<br>OE = High, F <sub>test</sub> = 100 MHz  |                       | 7                     |      |      |
|   |   | OE = Low   |                       | 0.1                   |      |      |
| I <sub>Vdd</sub> + I <sub>Vddo</sub>        | Total Device Current with<br>Loads on all outputs   | OE = High @ 100 MHz  |                       | 48                    |      | mA   |
|   |   | OE = Low   |                       | 16                    |      |      |
| <b>POWER SUPPLY RIPPLE REJECTION (PSRR)</b> |   |  |                       |                       |      |      |
| PSRR  | Ripple Induced<br>Phase Spur Level                  | 100 kHz, 100 mVpp<br>Ripple Injected on<br>V <sub>dd</sub> , V <sub>ddo</sub> = 2.5 V                              |                       |                       | -44  | dBc  |
| <b>OUTPUTS<sup>(1)</sup></b>                |   |  |                       |                       |      |      |
| Skew  | Output Skew <sup>(2)</sup>                          | Measured between outputs,<br>referenced to CLKout0   |                       | 6                     | 25   | ps   |
| t <sub>PD</sub>                             | Propagation Delay CLKin to<br>CLKout <sup>(2)</sup> | C <sub>L</sub> = 5 pF, R <sub>L</sub> = 50 Ω<br>V <sub>dd</sub> = 3.3 V; V <sub>ddo</sub> = 3.3 V                  | 0.85                  | 1.4                   | 2.2  | ns   |
|   |   | C <sub>L</sub> = 5 pF, R <sub>L</sub> = 50 Ω<br>V <sub>dd</sub> = 2.5 V; V <sub>ddo</sub> = 1.5 V                  | 1.1                   | 1.8                   | 2.8  | ns   |
| t <sub>PD, PP</sub>                         | Part-to-part Skew <sup>(2) (3)</sup>                | C <sub>L</sub> = 5 pF, R <sub>L</sub> = 50 Ω<br>V <sub>dd</sub> = 3.3 V; V <sub>ddo</sub> = 3.3 V                  |                       |                       | 0.35 | ns   |
|   |   | C <sub>L</sub> = 5 pF, R <sub>L</sub> = 50 Ω<br>V <sub>dd</sub> = 2.5 V; V <sub>ddo</sub> = 1.5 V                  |                       |                       | 0.6  | ns   |
| f <sub>CLKout</sub>                         | Output Frequency <sup>(4)</sup>                     |  | DC                    | 200                   | MHz  |      |
| t <sub>Rise</sub>                           | Rise/Fall Time                                      | V <sub>dd</sub> = 3.3 V, V <sub>ddo</sub> = 1.8 V, C <sub>L</sub> = 10 pF  |                       | 250                   |      | ps   |
|   |   | V <sub>dd</sub> = 2.5 V, V <sub>ddo</sub> = 2.5 V, C <sub>L</sub> = 10 pF  |                       | 275                   |      |      |
|   |   | V <sub>dd</sub> = 3.3 V, V <sub>ddo</sub> = 3.3 V, C <sub>L</sub> = 10 pF  |                       | 315                   |      |      |
| V <sub>CLKoutLow</sub>                      | Output Low Voltage                                  |  |                       | 0.1                   |      | V    |
| V <sub>CLKoutHigh</sub>                     | Output High Voltage                                 |  | V <sub>ddo</sub> -0.1 |                       |      |      |
| R <sub>CLKout</sub>                         | Output Resistance                                   |  |                       | 50                    |      | ohm  |
| t <sub>j</sub>                              | RMS Additive Jitter                                 | f <sub>CLKout</sub> = 156.25 MHz,<br>CMOS input slew rate ≥ 2 V/ns<br>C <sub>L</sub> = 5 pF, BW = 12 kHz to 20 MHz |                       | 30                    |      | fs   |

(1) AC Parameters for CMOS are dependent upon output capacitive loading

(2) Parameter is specified by design, not tested in production.

(3) Part-to-part skew is calculated as the difference between the fastest and slowest tPD across multiple devices.

(4) Specified by characterization.

## Electrical Characteristics (continued)

( $2.375 \text{ V} \leq V_{dd} \leq 3.45 \text{ V}$ ,  $1.425 \leq V_{ddo} \leq V_{dd}$ ,  $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$ , Differential inputs. Typical values represent most likely parametric norms at  $V_{dd} = V_{ddo} = 3.3 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ , at the Recommended Operation Conditions at the time of product characterization and are **not** ensured). Test conditions are:  $F_{test} = 100 \text{ MHz}$ , Load = 5 pF in parallel with  $50 \Omega$  unless otherwise stated.

|   | PARAMETER   | TEST CONDITIONS  | MIN  | TYP | MAX          | UNIT |
|---|---|--|------|-----|--------------|------|
| <b>DIGITAL INPUTS (OE, SEL0, SEL1)</b>                          |   |  |      |     |              |      |
| $V_{Low}$   | Input Low Voltage   | $V_{dd} = 2.5 \text{ V}$   |      |     | 0.4          | V    |
| $V_{High}$  | Input High Voltage  | $V_{dd} = 2.5 \text{ V}$   | 1.3  |     |              |      |
|   |   | $V_{dd} = 3.3 \text{ V}$   | 1.6  |     |              |      |
| $I_{IH}$  | High Level Input Current                                    |  |      |     | 50           | uA   |
| $I_{IL}$  | Low Level Input Current                                     |  | -5   |     | 5            |      |
| <b>CLKin/CLKin* INPUT CLOCK SPECIFICATIONS<sup>(5)(6)</sup></b> |   |  |      |     |              |      |
| $I_{IH}$  | High Level Input Current                                    | $V_{CLKin} = V_{dd}$   |      |     | 20           | uA   |
| $I_{IL}$  | Low Level Input Current                                     | $V_{CLKin} = 0 \text{ V}$  | -20  |     |              | uA   |
| $V_{IH}$  | Input High Voltage  |  |      |     | $V_{dd}$     | V    |
| $V_{IL}$  | Input Low Voltage   |  | GND  |     |              |      |
| $V_{CM}$  | Differential Input Common Mode Input Voltage <sup>(7)</sup> | $V_{ID} = 150 \text{ mV}$  | 0.5  |     | $V_{dd}-1.2$ | V    |
|   |   | $V_{ID} = 350 \text{ mV}$  | 0.5  |     | $V_{dd}-1.1$ |      |
|   |   | $V_{ID} = 800 \text{ mV}$  | 0.5  |     | $V_{dd}-0.9$ |      |
| $V_{LSE}$   | Single-Ended Input Voltage Swing <sup>(2)</sup>             | CLKinX driven single-ended (AC or DC coupled), CLKinX* AC coupled to GND or externally biased within $V_{CM}$ range                                    | 0.3  |     | 2            | Vpp  |
| $V_{ID}$  | Differential Input Voltage Swing                            | CLKin driven differentially  | 0.15 |     | 1.5          | V    |
| <b>OSCin/OSCout PINS</b>  |   |  |      |     |              |      |
| $f_{OSCin}$   | Input Frequency <sup>(4)</sup>                              | Single-Ended Input, OSCout floating  | DC   |     | 200          | MHz  |
| $f_{XTAL}$  | Crystal Frequency Input Range                               | Fundamental Mode Crystal ESR < $200 \Omega$ ( $f_{xtal} \leq 30 \text{ MHz}$ )<br>ESR < $120 \Omega$ ( $f_{xtal} > 30 \text{ MHz}$ ) <sup>(4)(8)</sup> | 10   |     | 40           | MHz  |
| $C_{OSCin}$   | Shunt Capacitance   |  |      | 1   |              | pF   |
| $V_{IH}$  | Input High Voltage  | Single-Ended Input, OSCout floating  |      |     | 2.5          | V    |

(5) See *Differential Voltage Measurement Terminology* for definition of  $V_{OD}$  and  $V_{ID}$ .

(6) Refer to application note AN-912 Common Data Transmission Parameters and their Definitions for more information.

(7) When using differential signals with  $V_{CM}$  outside of the acceptable range for the specified  $V_{ID}$ , the clock must be AC coupled.

(8) The ESR requirements stated are what is necessary in order to ensure that the Oscillator circuitry has no start up issues. However, lower ESR values for the crystal might be necessary in order to stay below the maximum power dissipation requirements for that crystal.

## 6.6 Typical Characteristics

Unless otherwise specified:  $V_{dd} = V_{ddo} = 3.3$  V,  $T_A = 20$  °C,  $C_L = 5$  pF, CLKin driven differentially, input slew rate  $\geq 2$  V/ns.

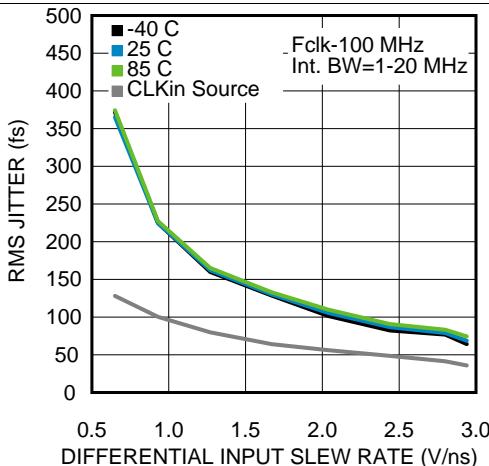


Figure 1. RMS Jitter vs. CLKin Slew Rate @ 100 MHz

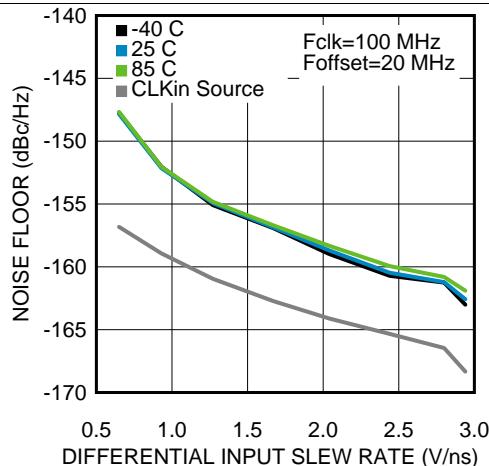
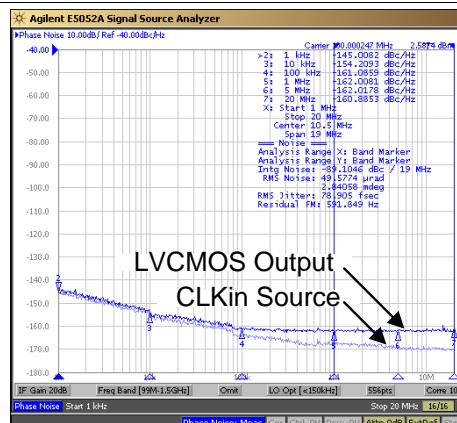


Figure 2. Noise Floor vs. CLKin Slew Rate @ 100 MHz



Test conditions: LVCMS Input, slew rate  $\geq 2$  V/ns,  $C_L = 5$  pF in parallel with  $50\ \Omega$ , BW = 1 MHz to 20 MHz

Figure 3. LVCMS Phase Noise @ 100 MHz

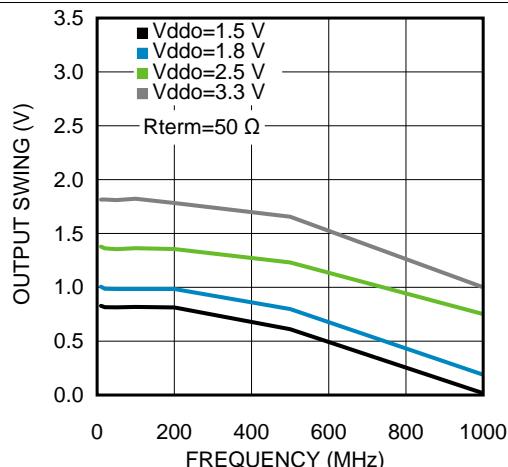


Figure 4. LVCMS Output Swing vs. Frequency

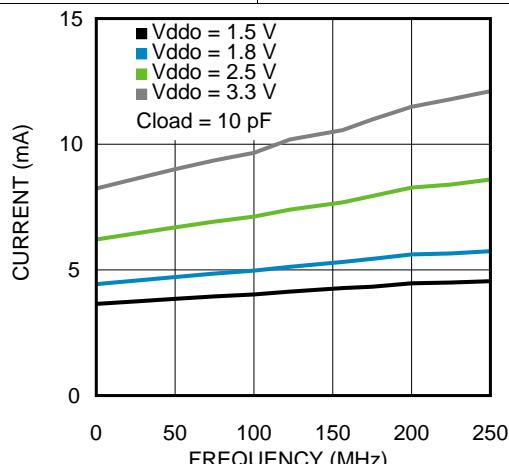


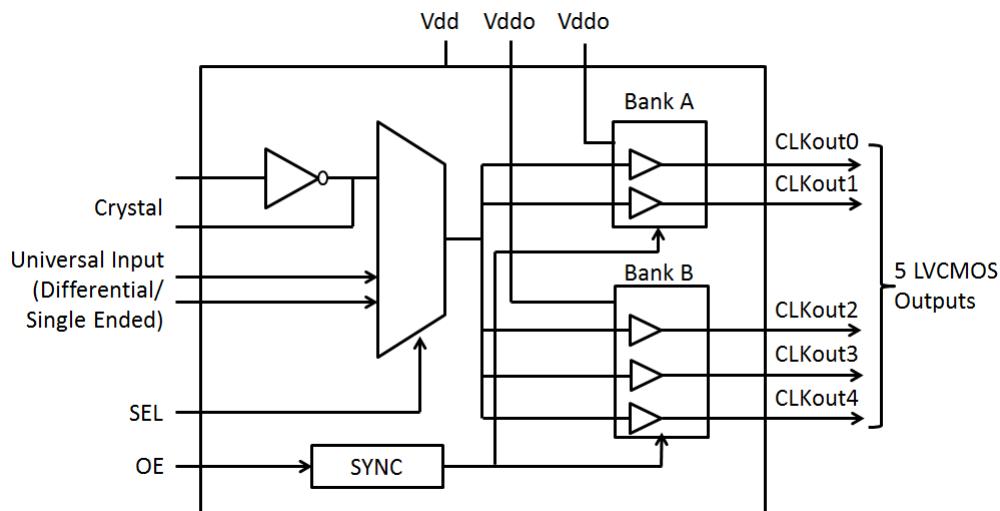
Figure 5. Iddo per Output vs Frequency

## 7 Detailed Description

### 7.1 Overview

The LMK00105 is a 5 output LVCMOS clock fanout buffer with low additive jitter that can operate up to 200 MHz. It features a 2:1 input multiplexer with a crystal oscillator input, single supply or dual supply (lower power) operation, and pin-programmable device configuration. The device is offered in a 24-pin WQFN package.

### 7.2 Functional Block Diagram



### 7.3 Feature Description

#### 7.3.1 $V_{dd}$ and $V_{ddo}$ Power Supplies

Separate core and output supplies allow the output buffers to operate at the same supply as the  $V_{dd}$  core supply (3.3 V or 2.5 V) or from a lower supply voltage (3.3 V, 2.5 V, 1.8 V, or 1.5 V). Compared to single-supply operation, dual supply operation enables lower power consumption and output-level compatibility.

Bank A (CLKout0 and CLKout1) and Bank B (CLKout2 to CLKout4) may also be operated at different  $V_{ddo}$  voltages, provided neither  $V_{ddo}$  voltage exceeds  $V_{dd}$ .

#### NOTE

Care should be taken to ensure the  $V_{ddo}$  voltage does not exceed the  $V_{dd}$  voltage to prevent turning-on the internal ESD protection circuitry.

**DO NOT DISCONNECT OR GROUND ANY OF THE  $V_{ddo}$  PINS** because the  $V_{ddo}$  pins are internally connected within an output bank.

#### 7.3.2 Clock Input

The LMK00105 has one differential input, CLKin/CLKin\* and OSCin, that can be driven in different manners that are described in the following sections.

##### 7.3.2.1 Selection of Clock Input

Clock input selection is controlled using the SEL pin as shown in [Table 1](#). Refer to [Clock Inputs](#) for clock input requirements. When CLKin is selected, the crystal circuit is powered down. When OSCin is selected, the crystal oscillator will start-up and its clock will be distributed to all outputs. Refer to [Crystal Interface](#) for more information. Alternatively, OSCin may be driven by a single ended clock, up to 200 MHz, instead of a crystal.

**Table 1. Input Selection**

| SEL | Input                |
|-----|----------------------|
| 0   | CLKin, CLKin*        |
| 1   | OSCin (Crystal Mode) |

### 7.3.2.1.1 CLKin/CLKin\* Pins

The LMK00105 has a differential input (CLKin/CLKin\*) which can be driven single-ended or differentially. It can accept AC or DC coupled 3.3V/2.5V LVPECL, LVDS, or other differential and single ended signals that meet the input requirements in [Electrical Characteristics](#) and when using differential signals with  $V_{CM}$  outside of the acceptable range for the specified  $V_{ID}$ , the clock must be AC coupled. Refer to [Clock Inputs](#) for more details on driving the LMK00105 inputs.

In the event that a Crystal mode is not selected and the CLKin pins do not have an AC signal applied to them, [Table 2](#) following will be the state of the outputs.

**Table 2. CLKin Input vs. Output States**

| CLKin      | CLKin*     | Output State |
|------------|------------|--------------|
| Open       | Open       | Logic Low    |
| Logic Low  | Logic Low  | Logic Low    |
| Logic High | Logic Low  | Logic High   |
| Logic Low  | Logic High | Logic Low    |

### 7.3.2.1.2 OSCin/OSCout Pins

The LMK00105 has a crystal oscillator which will be powered up when OSCin is selected. Alternatively, OSCin may be driven by a single ended clock, up to 200 MHz, instead of a crystal. Refer to [Crystal Interface](#) for more information. If Crystal mode is selected and the pins do not have an AC signal applied to them, [Table 3](#) will be the state of the outputs. If Crystal mode is selected an open state is not allowed on OSCin, as the outputs may oscillate due to the crystal oscillator circuitry.

**Table 3. OSCin Input vs. Output States**

| OSCin      | Output State |
|------------|--------------|
| Open       | Not Allowed  |
| Logic Low  | Logic High   |
| Logic High | Logic Low    |

### 7.3.3 Clock Outputs

The LMK00105 has 5 LVC MOS outputs.

#### 7.3.3.1 Output Enable Pin

When the output enable pin is held High, the outputs are enabled. When it is held Low, the outputs are held in a Low state as shown in [Table 4](#).

**Table 4. Output Enable Pin States**

| OE   | Outputs         |
|------|-----------------|
| Low  | Disabled (Hi-Z) |
| High | Enabled         |

The OE pin is synchronized to the input clock to ensure that there are no runt pulses. When OE is changed from Low to High, the outputs will initially have an impedance of about  $400\ \Omega$  to ground until the second falling edge of the input clock and starting with the second falling edge of the input clock, the outputs will buffer the input. If the OE pin is taken from Low to High when there is no input clock present, the outputs will either go high or low and stay at that state; they will not oscillate. When the OE pin is taken from High to Low the outputs will be Low after the second falling edge of the clock input and then will go to a Disabled (Hi-Z) state starting after the next rising edge.

### 7.3.3.2 Using Less than Five Outputs

Although the LMK00105 has 5 outputs, not all applications will require all of these. In this case, the unused outputs should be left floating with a minimum copper length to minimize capacitance. In this way, this output will consume minimal output current because it has no load.

---

#### NOTE

For best soldering practices, the minimum trace length should extend to include the pin solder mask. This way during reflow, the solder has the same copper area as connected pins. This allows for good, uniform fillet solder joints helping to keep the IC level during reflow.

---

## 7.4 Device Functional Modes

LMK00105 can be driven by a clock input or a crystal according to SEL pin. Refer to [Selection of Clock Input](#) for more information.

## 8 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

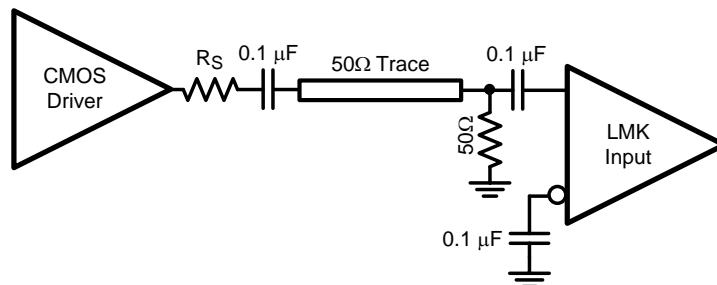
### 8.1 Application Information

#### 8.1.1 Clock Inputs

The LMK00105 has a differential input (CLKin/CLKin\*) that can accept AC or DC coupled 3.3V/2.5V LVPECL, LVDS, and other differential and single ended signals that meet the input requirements specified in [Electrical Characteristics](#). The device can accept a wide range of signals due to its wide input common mode voltage range ( $V_{CM}$ ) and input voltage swing ( $V_{ID}$ )/dynamic range. AC coupling may also be employed to shift the input signal to within the  $V_{CM}$  range.

To achieve the best possible phase noise and jitter performance, it is mandatory for the input to have a high slew rate of 2 V/ns (differential) or higher. Driving the input with a lower slew rate will degrade the noise floor and jitter. For this reason, a differential input signal is recommended over single-ended because it typically provides higher slew rate and common-mode noise rejection.

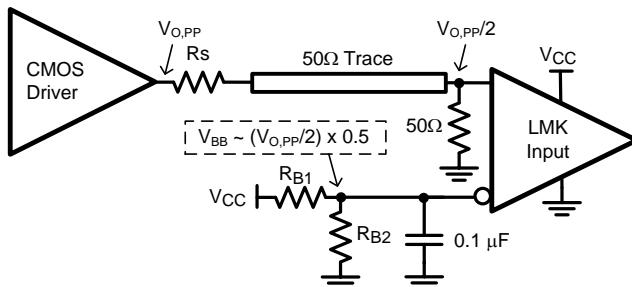
While it is recommended to drive the CLKin/CLKin\* pair with a differential signal input, it is possible to drive it with a single-ended clock provided it conforms to the Single-Ended Input specifications for CLKin pins listed in the [Electrical Characteristics](#). For large single-ended input signals, such as 3.3 V or 2.5 V LVCMS, a 50 Ω load resistor should be placed near the input for signal attenuation to prevent input overdrive as well as for line termination to minimize reflections. The CLKin input has an internal bias voltage of about 1.4 V, so the input can be AC coupled as shown in [Figure 6](#). The output impedance of the LVCMS driver plus  $R_s$  should be close to 50 Ω to match the characteristic impedance of the transmission line and load termination.



**Figure 6. Preferred Configuration: Single-Ended LVCMS Input, AC Coupling**

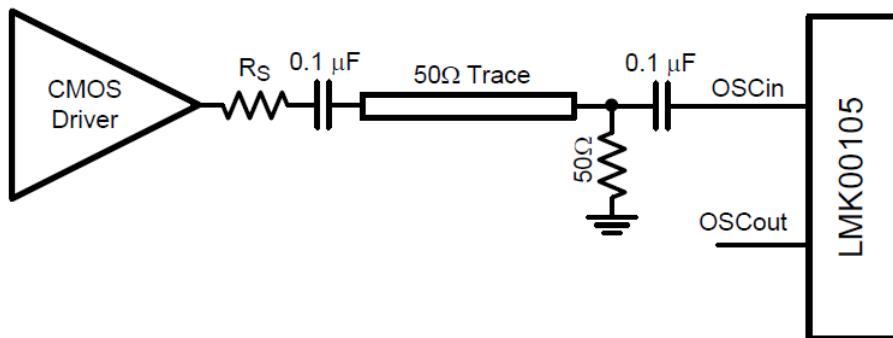
A single-ended clock may also be DC coupled to CLKin as shown in [Figure 7](#). A 50-Ω load resistor should be placed near the CLKin input for signal attenuation and line termination. Because half of the single-ended swing of the driver ( $V_{O,PP} / 2$ ) drives CLKin, CLKin\* should be externally biased to the midpoint voltage of the attenuated input swing ( $(V_{O,PP} / 2) \times 0.5$ ). The external bias voltage should be within the specified input common voltage ( $V_{CM}$ ) range. This can be achieved using external biasing resistors in the kΩ range ( $R_{B1}$  and  $R_{B2}$ ) or another low-noise voltage reference. This will ensure the input swing crosses the threshold voltage at a point where the input slew rate is the highest.

## Application Information (continued)



**Figure 7. Single-Ended LVCMOS Input, DC Coupling With Common Mode Biasing**

If the crystal oscillator circuit is not used, it is possible to drive the OSCin input with a single-ended external clock as shown in [Figure 8](#). The input clock should be AC coupled to the OSCin pin, which has an internally generated input bias voltage, and the OSCout pin should be left floating. While OSCin provides an alternative input to multiplex an external clock, it is recommended to use either differential input (CLKin) since it offers higher operating frequency, better common mode, improved power supply noise rejection, and greater performance over supply voltage and temperature variations.



**Figure 8. Driving OSCin With a Single-Ended External Clock**

### 8.1.2 Clock Outputs

The LMK00105 LVCMOS driver output impedance ( $R_o$ ) is nominally 50 ohms and well-matched to drive a 50 ohm transmission line ( $Z_0$ ), as shown as below. If driving a transmission line with higher characteristic impedance than 50 ohms, a series resistor ( $R_s$ ) should be placed near the driver to provide source termination, where  $R_s = Z_0 - R_o$ .

The LMK00105 has two output banks, Bank A and Bank B, which are separately powered by independent  $V_{ddo}$  supply pins. The  $V_{ddo}$  supply pins for Bank A and Bank B are not connected together internally, and may be supplied with different voltages. This allows the LMK00105 outputs to easily interface to multiple receivers with different input threshold or input supply voltage ( $V_{ddi}$ ) requirements without the need for additional voltage divider networks.

## Application Information (continued)

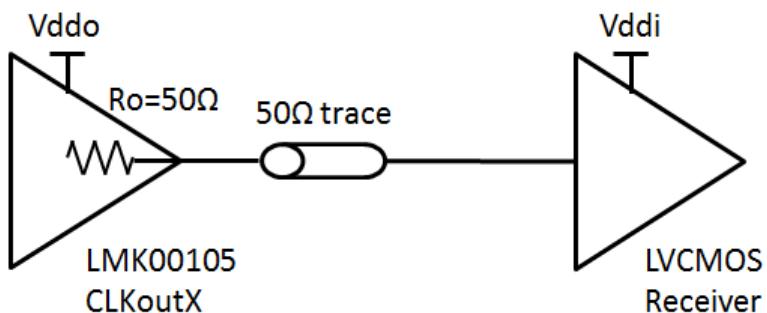


Figure 9. LMK00105 Output Termination

## 8.2 Typical Applications

### 8.2.1 Typical Application Block Diagram

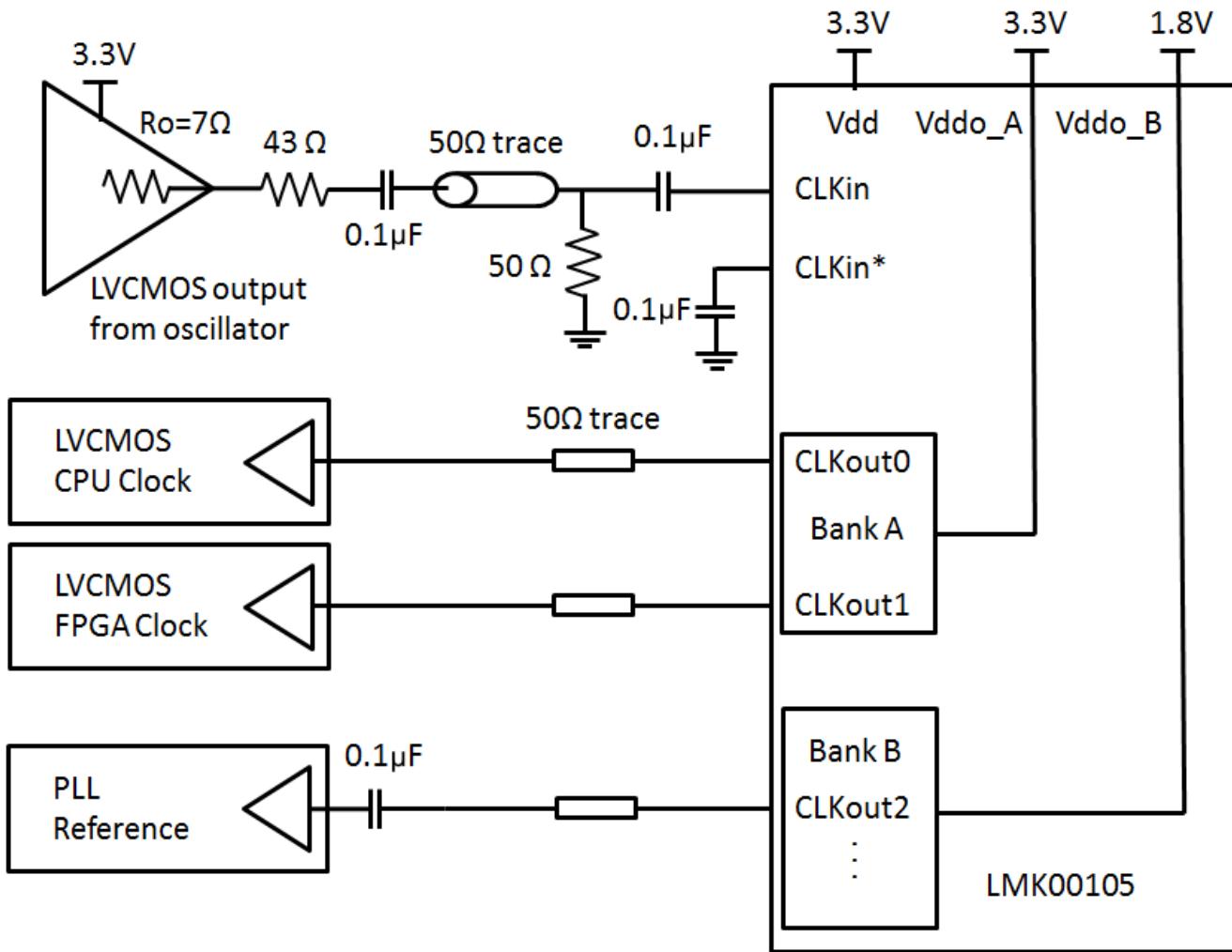


Figure 10. Typical Application Block Diagram

## Typical Applications (continued)

### 8.2.1.1 Design Requirements

In the example application shown in [Figure 10](#), the LMK00105 is used to fan-out a 3.3-V LVCMOS oscillator to three receiver devices with the following characteristics:

- The CPU input accepts a DC-coupled 3.3-V LVCMOS input clock. The LMK00105 has an internal 50- $\Omega$  series termination, thus the receiver is connected directly to the output.
- The FPGA input also requires a 3.3-V LVCMOS input clock, like the CPU.
- The PLL input requires a single-ended voltage swing less than 2 Vpp, so 1.8-V LVCMOS input signaling is needed. The PLL receiver requires AC coupling since it has internal input biasing to set its own common mode voltage level.

### 8.2.1.2 Detailed Design Procedure

Refer to [Clock Inputs](#) to properly interface the 3.3-V LVCMOS oscillator output to the CLKin input buffer of the LMK00105.

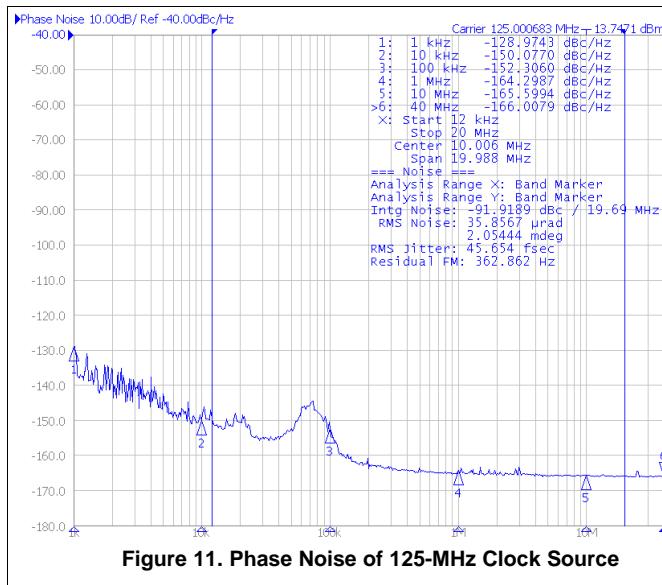
See [Figure 9](#) for output termination schemes depending on the receiver application. Since the CPU/FPGA inputs and PLL input require different input voltage levels, the LMK00105 output banks are supplied from separate Vddo rails of 3.3 V and 1.8 V for CLKout0/1 (Bank A) and CLKout2 (Bank B), respectively.

Unused outputs can be left floating.

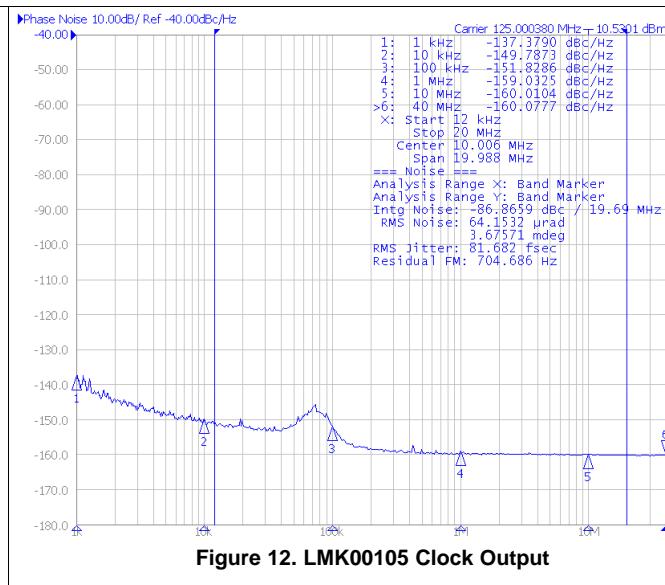
See [Power Supply Recommendations](#) for recommended power supply filtering and decoupling/bypass techniques.

### 8.2.1.3 Application Curves

The LMK00105 was tested using multiple low-jitter XO clock sources to evaluate the impact of the buffer's additive phase noise/jitter. The plots on the left show the phase noise of the clock source, while the plots on the right show the total output phase noise from LMK00105 contributed by both the clock source noise and buffer additive noise. Note that the phase noise "hump" around 80 kHz offset on the phase noise plots is correlated to the XO source, which is attributed to power supply noise at this frequency.



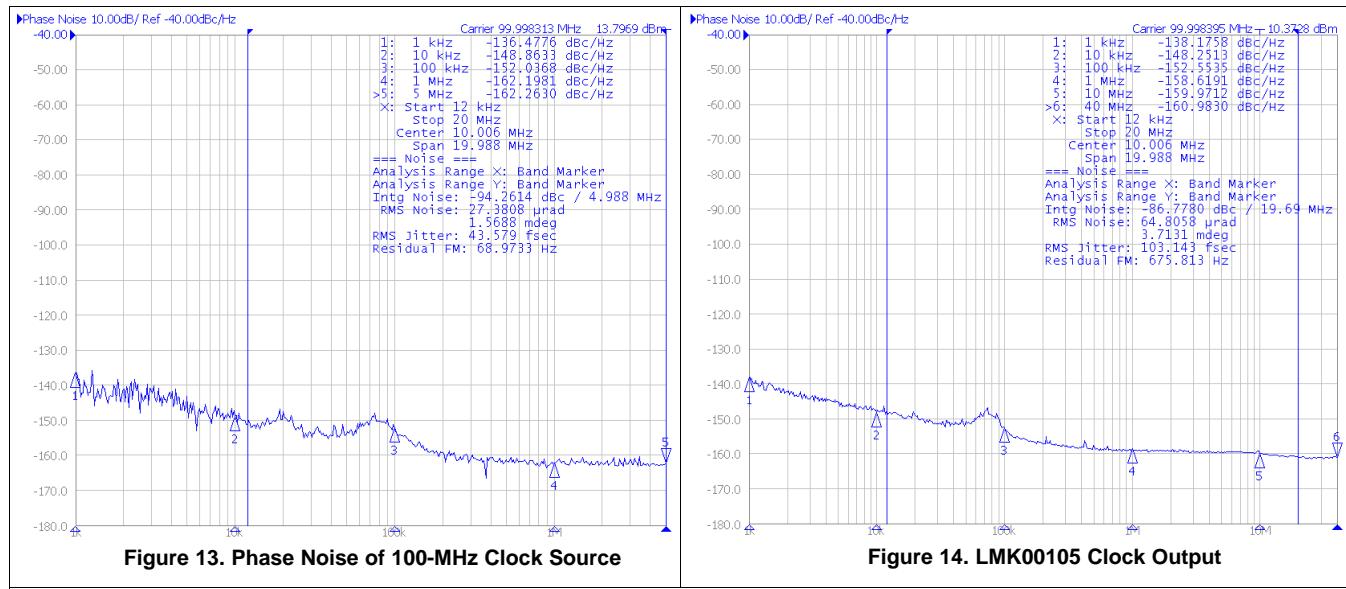
**Figure 11. Phase Noise of 125-MHz Clock Source**



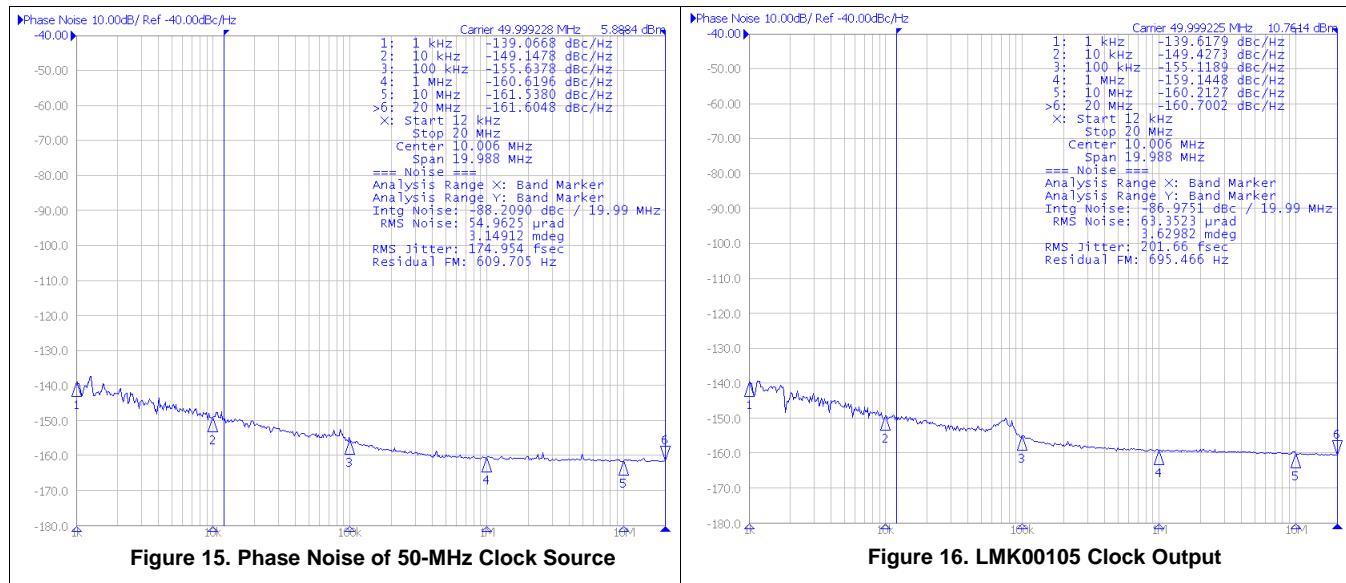
**Figure 12. LMK00105 Clock Output**

A low-noise 125 MHz XO clock source with 45.6 fs RMS jitter ([Figure 11](#)) was used to drive the LMK00105, resulting in a total output phase jitter of 81.6 fs RMS ([Figure 12](#)) integrated from 12 kHz to 20 MHz. The resultant additive jitter of the buffer is 67.7 fs RMS computed using the "Square-Root of the Difference of Squares" method.

## Typical Applications (continued)



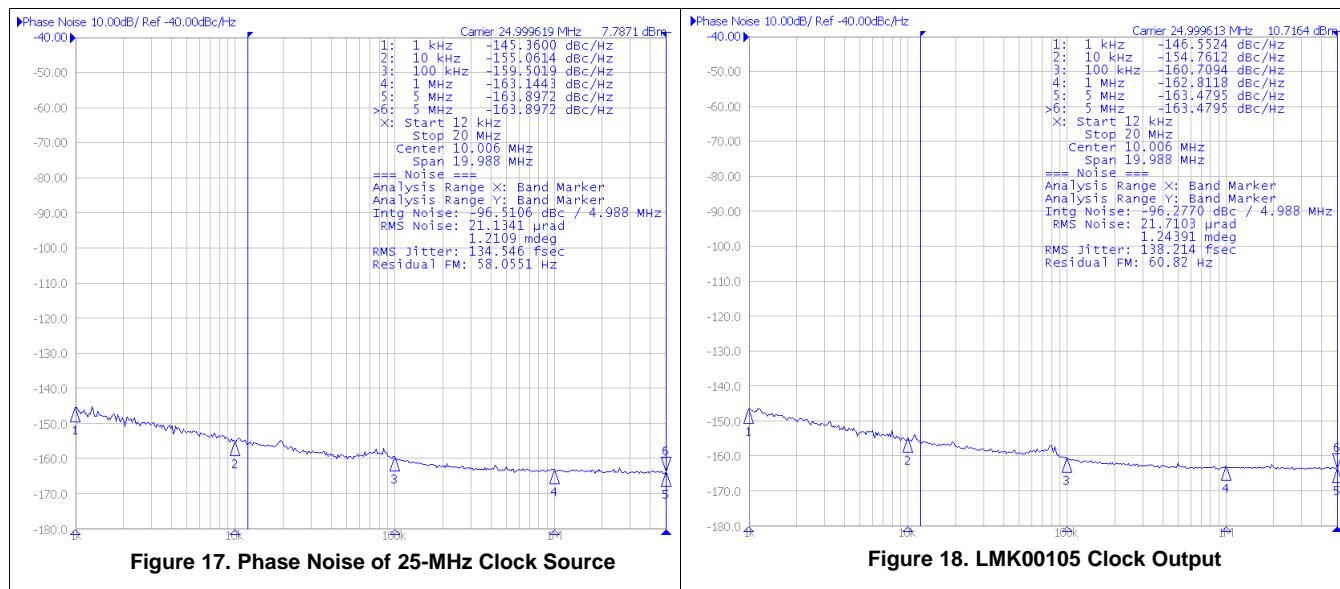
A low-noise 100 MHz XO clock source with 43.5 fs RMS jitter (Figure 13) was used to drive the LMK00105, resulting in a total output phase jitter of 103.1 fs RMS (Figure 14) integrated from 12 kHz to 20 MHz. The resultant additive jitter of the buffer is 93.4 fs RMS computed using the “Square-Root of the Difference of Squares” method.



A divide-by-2 circuit was used with the low-noise 100-MHz XO to generate a 50-MHz clock source with 174.9fs RMS jitter (Figure 15), resulting in a total output phase jitter of 201.6 fs RMS (Figure 16) integrated from 12 kHz to 20 MHz.

In this case, the total output phase noise/jitter is highly correlated to the clock source phase noise and jitter, which prevents us from computing the true additive jitter of the buffer using the “Square-Root of the Difference of Squares” method. To accurately specify the additive jitter of the buffer at this frequency, a clock source with lower noise (compared to the DUT) would be needed for this measurement.

## Typical Applications (continued)



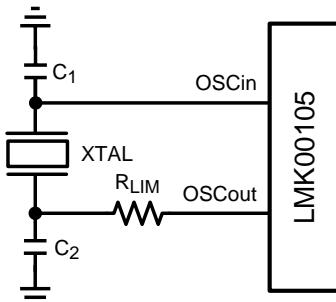
A divide-by-4 circuit was used with the low-noise 100 MHz XO to generate a 25-MHz clock source with 134.5 fs RMS (Figure 17), resulting in a total output phase jitter of 138.2 fs RMS (Figure 18) integrated from 12 kHz to 5 MHz.

In this case, the total output phase noise and jitter is highly correlated to the clock source phase noise and jitter, which prevents us from computing the true additive jitter of the buffer using the “Square-Root of the Difference of Squares” method. To accurately specify the additive jitter of the buffer at this frequency, a clock source with lower noise (compared to the DUT) would be needed for this measurement.

## Typical Applications (continued)

### 8.2.2 Crystal Interface

The LMK00105 has an integrated crystal oscillator circuit that supports a fundamental mode, AT-cut crystal. The crystal interface is shown in [Figure 19](#).



**Figure 19. Crystal Interface**

#### 8.2.2.1 Design Requirements

The value of capacitor and resistor depend on the crystal. Each crystal is specified with a load capacitance and resistor is used to avoid over driving the crystal.

The example crystal specifications are given in [Table 5](#).

**Table 5. Example 25-MHz Crystal Electrical Specifications**

| NO. | ITEM                         | SYMBOL         | ELECTRICAL SPECIFICATION |                |     |          |
|-----|------------------------------|----------------|--------------------------|----------------|-----|----------|
|     |                              |                | MIN                      | TYP            | MAX |          |
| 1   | Nominal Frequency            | F0             |                          | 25             |     | MHz      |
| 2   | Mode of Vibration            |                |                          | Fundamental    |     |          |
| 3   | Frequency Tolerance          | $\Delta F/F_0$ | -15                      |                | 15  | ppm      |
| 4   | Load Capacitance             | CL             |                          | 9              |     | pF       |
| 5   | Drive Level                  | DL             |                          | 100            | 300 | $\mu$ W  |
| 6   | Equivalent Series Resistance | R1             |                          | 9              | 50  | $\Omega$ |
| 7   | Shunt Capacitance            | C0             |                          | $2.1 \pm 15\%$ |     | pF       |
| 8   | Motional Capacitance         | C1             |                          | $9.0 \pm 15\%$ |     | fF       |
| 9   | Motional Inductance          | L              |                          | $4.6 \pm 15\%$ |     | mH       |
| 10  | Frequency Stability          | TC             | -20                      |                | 20  | ppm      |
| 11  | C0/C1 Rate                   |                |                          |                | 250 |          |

Based on the OSCin shunt capacitance and stray capacitance, C1 and C2 are chosen as 6.8 pF to make the load capacitance (CL) to be 9 pF. Suggested value of RLIM is 1.5 k $\Omega$ . Refer to [Detailed Design Procedure](#) for the derivation.

#### 8.2.2.2 Detailed Design Procedure

The load capacitance ( $C_L$ ) is specific to the crystal, but usually on the order of 18 to 20 pF. While  $C_L$  is specified for the crystal, the OSCin input capacitance ( $C_{IN} = 1 \text{ pF}$  typical) of the device and PCB stray capacitance ( $C_{STRAY} \sim 1 \text{ to } 3 \text{ pF}$ ) can affect the discrete load capacitor values, C1 and C2. For the parallel resonant circuit, the discrete capacitor values can be calculated as follows:

$$C_L = (C_1 * C_2) / (C_1 + C_2) + C_{IN} + C_{STRAY} \quad (1)$$

Typically,  $C_1 = C_2$  for optimum symmetry, so [Equation 1](#) can be rewritten in terms of C1 only:

$$C_L = C_1^2 / (2 * C_1) + C_{IN} + C_{STRAY} \quad (2)$$

Finally, solve for C1:

$$C_1 = (C_L - C_{IN} - C_{STRAY}) * 2 \quad (3)$$

*Electrical Characteristics* provides crystal interface specifications with conditions that ensure start-up of the crystal, but it does not specify crystal power dissipation. The designer will need to ensure the crystal power dissipation does not exceed the maximum drive level specified by the crystal manufacturer. Overdriving the crystal can cause premature aging, frequency shift, and eventual failure. Drive level should be held at a sufficient level necessary to start-up and maintain steady-state operation.

The power dissipated in the crystal,  $P_{XTAL}$ , can be computed by:

$$P_{XTAL} = I_{RMS}^2 * R_{ESR} * (1 + C_0 / C_L)^2 \quad (4)$$

Where:

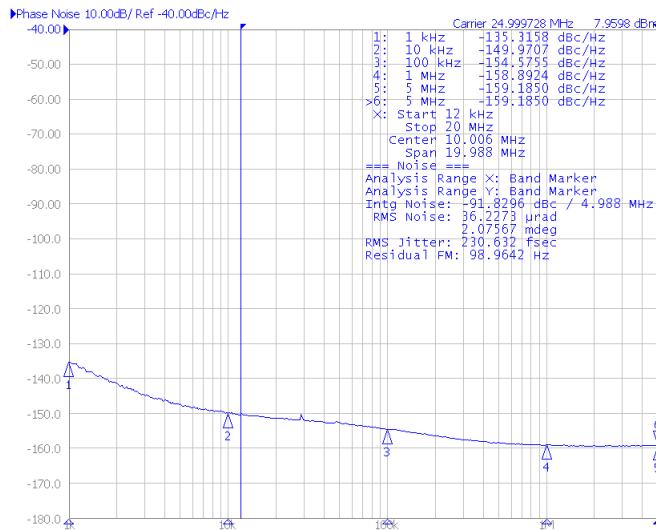
- $I_{RMS}$  is the RMS current through the crystal.
- $R_{ESR}$  is the maximum equivalent series resistance specified for the crystal.
- $C_L$  is the load capacitance specified for the crystal.
- $C_0$  is the minimum shunt capacitance specified for the crystal.

$I_{RMS}$  can be measured using a current probe (e.g. Tektronix CT-6 or equivalent) placed on the leg of the crystal connected to OSCout with the oscillation circuit active.

As shown in [Figure 19](#), an external resistor,  $R_{LIM}$ , can be used to limit the crystal drive level if necessary. If the power dissipated in the selected crystal is higher than the drive level specified for the crystal with  $R_{LIM}$  shorted, then a larger resistor value is mandatory to avoid overdriving the crystal. However, if the power dissipated in the crystal is less than the drive level with  $R_{LIM}$  shorted, then a zero value for  $R_{LIM}$  can be used. As a starting point, a suggested value for  $R_{LIM}$  is 1.5 kΩ.

[Figure 20](#) shows the LMK00105 output phase noise performance in crystal mode with the 25-MHz crystal specified in [Table 5](#).

### 8.2.2.3 Application Curves

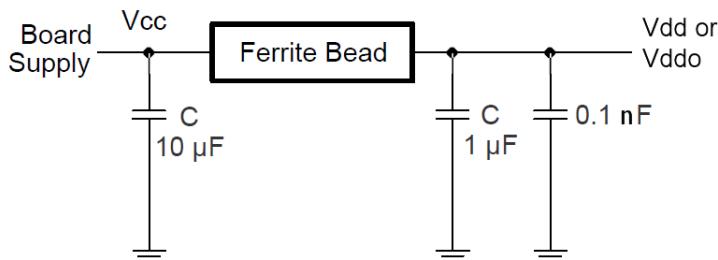


**Figure 20. Output Phase Noise in Crystal Mode with 25-MHz Crystal (230.6 fs RMS jitter, 12 kHz to 5 MHz)**

## 9 Power Supply Recommendations

### 9.1 Power Supply Filtering

It is recommended, but not required, to insert a ferrite bead between the board power supply and the chip power supply to isolate the high-frequency switching noises generated by the clock driver, preventing them from leaking into the board supply. Choosing an appropriate ferrite bead with very low DC resistance is important, because it is imperative to provide adequate isolation between the board supply and the chip supply. It is also imperative to maintain a voltage at the supply terminals that is greater than the minimum voltage required for proper operation.

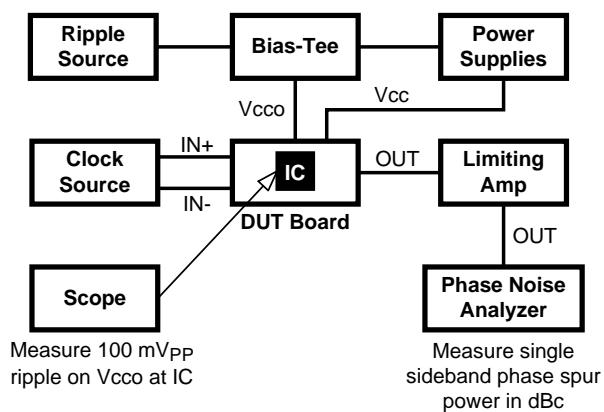


**Figure 21. Power-Supply Decoupling**

### 9.2 Power Supply Ripple Rejection

In practical system applications, power supply noise (ripple) can be generated from switching power supplies, digital ASICs or FPGAs, etc. While power supply bypassing will help filter out some of this noise, it is important to understand the effect of power supply ripple on the device performance. When a single-tone sinusoidal signal is applied to the power supply of a clock distribution device, such as LMK00105, it can produce narrow-band phase modulation as well as amplitude modulation on the clock output (carrier). In the singleside band phase noise spectrum, the ripple-induced phase modulation appears as a phase spur level relative to the carrier (measured in dBc).

For the LMK00105, power supply ripple rejection (PSRR), was measured as the single-sideband phase spur level (in dBc) modulated onto the clock output when a ripple signal was injected onto the  $V_{ddo}$  supply. The PSRR test setup is shown in [Figure 22](#).



**Figure 22. PSRR Test Setup**

A signal generator was used to inject a sinusoidal signal onto the  $V_{ddo}$  supply of the DUT board, and the peak-to-peak ripple amplitude was measured at the  $V_{ddo}$  pins of the device. A limiting amplifier was used to remove amplitude modulation on the differential output clock and convert it to a single-ended signal for the phase noise analyzer. The phase spur level measurements were taken for clock frequencies of 100 MHz under the following power supply ripple conditions:

## Power Supply Ripple Rejection (continued)

- Ripple amplitude: 100 mVpp on  $V_{ddo} = 2.5$  V
- Ripple frequency: 100 kHz

Assuming no amplitude modulation effects and small index modulation, the peak-to-peak deterministic jitter (DJ) can be calculated using the measured single-sideband phase spur level (PSRR) as follows:

$$DJ \text{ (ps pk-pk)} = [(2 * 10^{(PSRR/20)}) / (\pi * f_{clk})] * 10^{12} \quad (5)$$

## 9.3 Power Supply Bypassing

The  $V_{dd}$  and  $V_{ddo}$  power supplies should have a high frequency bypass capacitor, such as 100 pF, placed very close to each supply pin. Placing the bypass capacitors on the same layer as the LMK00105 improves input sensitivity and performance. All bypass and decoupling capacitors should have short connections to the supply and ground plane through a short trace or via to minimize series inductance.

# 10 Layout

## 10.1 Layout Guidelines

### 10.1.1 Ground Planes

Solid ground planes are recommended as they provide a low-impedance return paths between the device and its bypass capacitors and its clock source and destination devices. Avoid return paths of other system circuitry (for example, high-speed/digital logic) from passing through the local ground of the device to minimize noise coupling, which could induce added jitter and spurious noise.

### 10.1.2 Power Supply Pins

Follow the power supply schematic and layout example described in [Power Supply Bypassing](#).

### 10.1.3 Differential Input Termination

- Place input termination resistors as close as possible to the CLKin/CLKin\* pins.
- Avoid or minimize vias in the 50- $\Omega$  input traces to minimize impedance discontinuities. Intra-pair skew should be also be minimized on the differential input traces.
- If not used, CLKin/CLKin\* inputs may be left floating.

### 10.1.4 Output Termination

- Place series termination resistors as close as possible to the CLKoutX outputs at the launch of the controlled impedance traces.
- Avoid or minimize vias in the 50- $\Omega$  traces to minimize impedance discontinuities.
- Any unused CLKoutX output should be left floating and not routed.

## 10.2 Layout Example

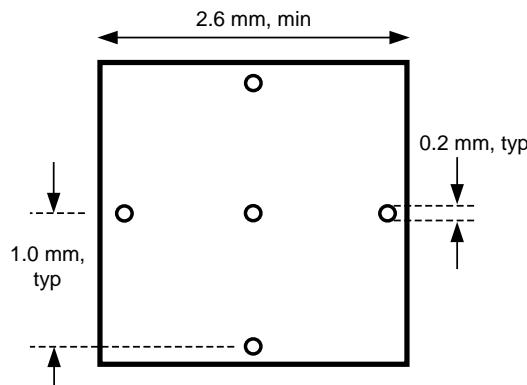


Figure 23. Recommended Land and Via Pattern

## 10.3 Thermal Management

For reliability and performance reasons the die temperature should be limited to a maximum of 125°C. That is, as an estimate, TA (ambient temperature) plus device power consumption times  $\theta_{JA}$  should not exceed 125°C.

The package of the device has an exposed pad that provides the primary heat removal path as well as excellent electrical grounding to a printed circuit board. To maximize the removal of heat from the package a thermal land pattern including multiple vias to a ground plane must be incorporated on the PCB within the footprint of the package. The exposed pad must be soldered down to ensure adequate heat conduction out of the package.

A recommended land and via pattern is shown in Figure 23. More information on soldering WQFN packages and gerber footprints can be obtained: [www.ti.com/packaging](http://www.ti.com/packaging).

To minimize junction temperature it is recommended that a simple heat sink be built into the PCB (if the ground plane layer is not exposed). This is done by including a copper area of about 2 square inches on the opposite side of the PCB from the device. This copper area may be plated or solder coated to prevent corrosion but should not have conformal coating (if possible), which could provide thermal insulation. The vias shown in Figure 23 should connect these top and bottom copper layers and to the ground layer. These vias act as “heat pipes” to carry the thermal energy away from the device side of the board to where it can be more effectively dissipated.

## 11 Device and Documentation Support

### 11.1 Documentation Support

#### 11.1.1 Differential Voltage Measurement Terminology

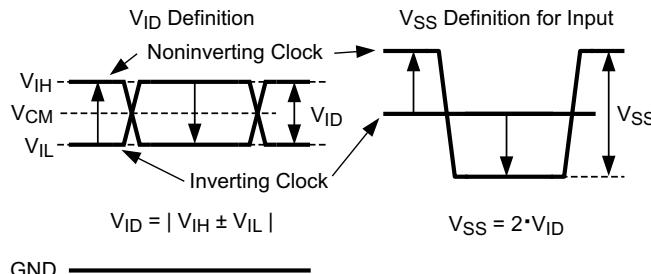
The differential voltage of a differential signal can be described by two different definitions causing confusion when reading datasheets or communicating with other engineers. This section will address the measurement and description of a differential signal so that the reader will be able to understand and discern between the two different definitions when used.

The first definition used to describe a differential signal is the absolute value of the voltage potential between the inverting and noninverting signal. The symbol for this first measurement is typically  $V_{ID}$  or  $V_{OD}$  depending on if an input or output voltage is being described.

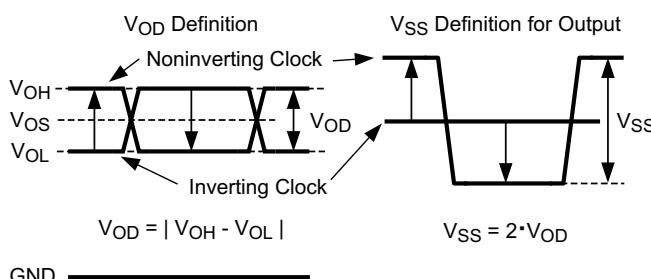
The second definition used to describe a differential signal is to measure the potential of the noninverting signal with respect to the inverting signal. The symbol for this second measurement is  $V_{SS}$  and is a calculated parameter. Nowhere in the IC does this signal exist with respect to ground, it only exists in reference to its differential pair.  $V_{SS}$  can be measured directly by oscilloscopes with floating references, otherwise this value can be calculated as twice the value of  $V_{ID}$  as described in the first section.

**Figure 24** illustrates the two different definitions side-by-side for inputs and **Figure 25** illustrates the two different definitions side-by-side for outputs. The  $V_{ID}$  and  $V_{OD}$  definitions show  $V_A$  and  $V_B$  DC levels that the noninverting and inverting signals toggle between with respect to ground.  $V_{SS}$  input and output definitions show that if the inverting signal is considered the voltage potential reference, the noninverting signal voltage potential is now increasing and decreasing above and below the noninverting reference. Thus the peak-to-peak voltage of the differential signal can be measured.

$V_{ID}$  and  $V_{OD}$  are often defined in volts (V) and  $V_{SS}$  is often defined as volts peak-to-peak ( $V_{PP}$ ).



**Figure 24.** Two Different Definitions for Differential Input Signals



**Figure 25.** Two Different Definitions for Differential Output Signals

### 11.2 Trademarks

All trademarks are the property of their respective owners.

## 11.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 11.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2)         | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples        |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|----------------|
| LMK00105SQ/NOPB  | ACTIVE        | WQFN         | RTW             | 24   | 1000        | Green (RoHS & no Sb/Br) | CU SN                   | Level-1-260C-UNLIM   | -40 to 85    | K00105                  | <b>Samples</b> |
| LMK00105SQE/NOPB | ACTIVE        | WQFN         | RTW             | 24   | 250         | Green (RoHS & no Sb/Br) | CU SN                   | Level-1-260C-UNLIM   | -40 to 85    | K00105                  | <b>Samples</b> |
| LMK00105SQX/NOPB | ACTIVE        | WQFN         | RTW             | 24   | 4500        | Green (RoHS & no Sb/Br) | CU SN                   | Level-1-260C-UNLIM   | -40 to 85    | K00105                  | <b>Samples</b> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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## PACKAGE OPTION ADDENDUM

8-Oct-2014

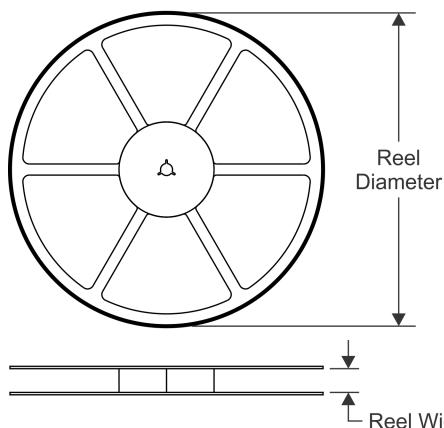
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continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

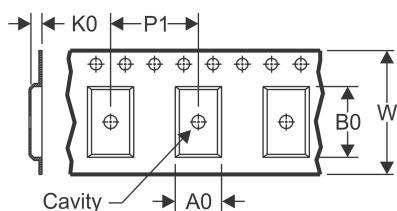
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## TAPE AND REEL INFORMATION

### REEL DIMENSIONS

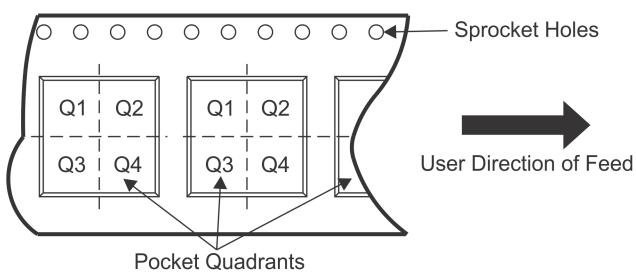


### TAPE DIMENSIONS



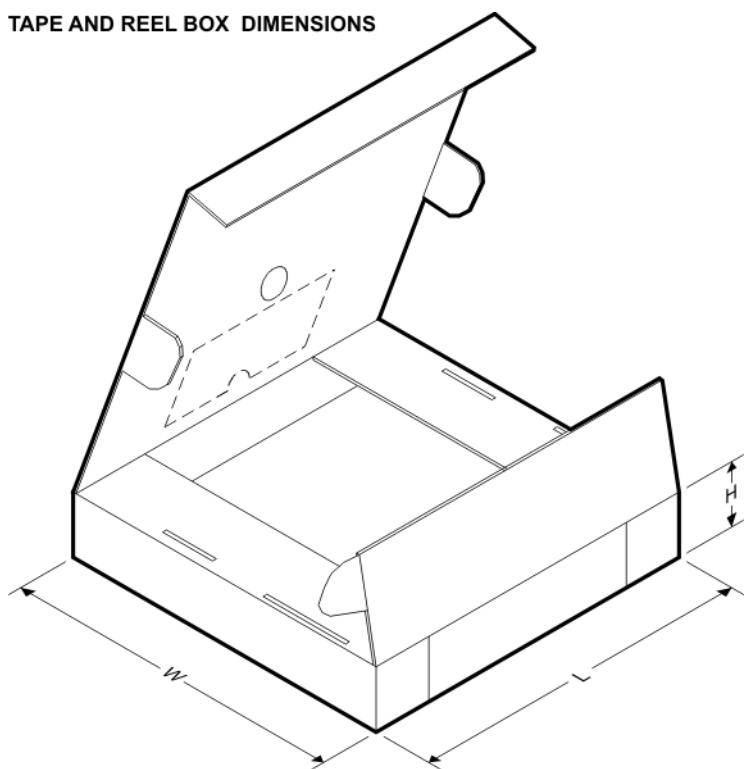
|    |   |
|----|---|
| A0 | Dimension designed to accommodate the component width     |
| B0 | Dimension designed to accommodate the component length    |
| K0 | Dimension designed to accommodate the component thickness |
| W  | Overall width of the carrier tape                         |
| P1 | Pitch between successive cavity centers                   |

### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

| Device           | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| LMK00105SQ/NOPB  | WQFN         | RTW             | 24   | 1000 | 178.0              | 12.4               | 4.3     | 4.3     | 1.3     | 8.0     | 12.0   | Q1            |
| LMK00105SQE/NOPB | WQFN         | RTW             | 24   | 250  | 178.0              | 12.4               | 4.3     | 4.3     | 1.3     | 8.0     | 12.0   | Q1            |
| LMK00105SQX/NOPB | WQFN         | RTW             | 24   | 4500 | 330.0              | 12.4               | 4.3     | 4.3     | 1.3     | 8.0     | 12.0   | Q1            |

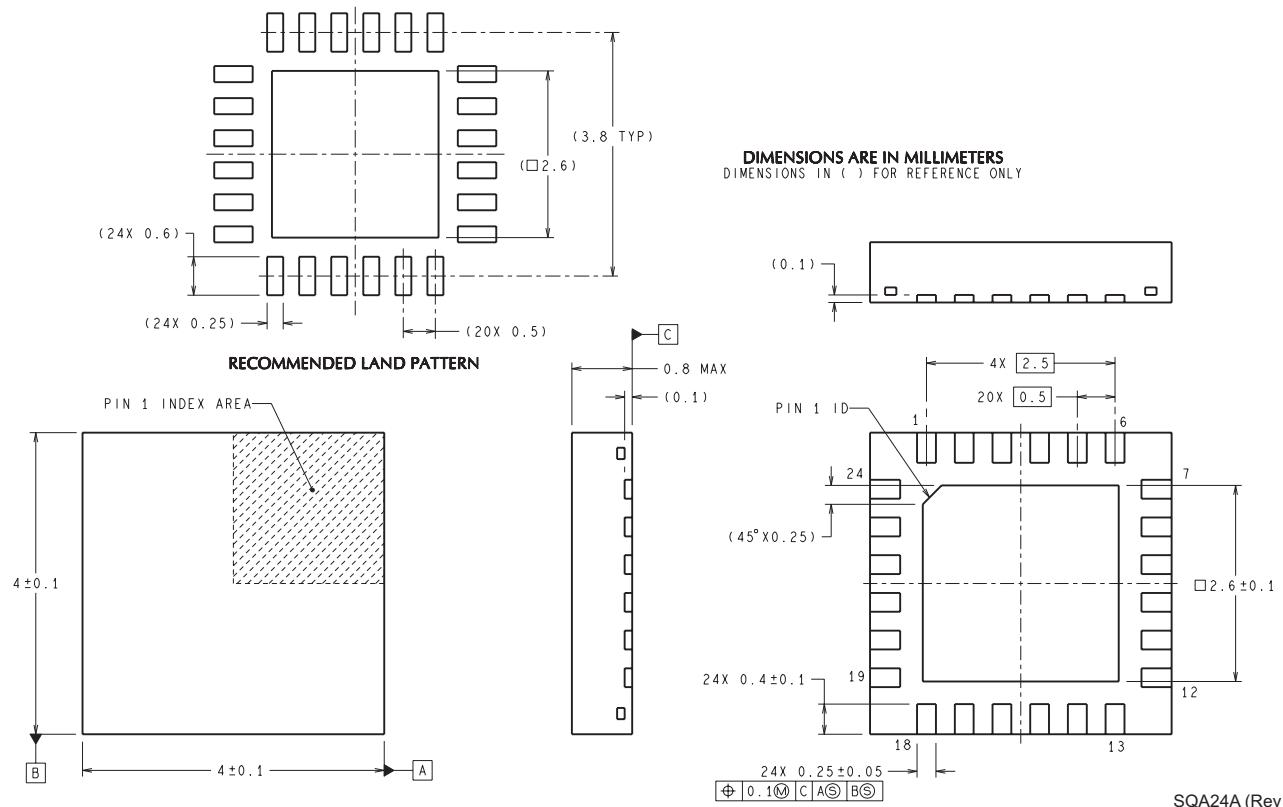
**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

| Device           | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| LMK00105SQ/NOPB  | WQFN         | RTW             | 24   | 1000 | 210.0       | 185.0      | 35.0        |
| LMK00105SQE/NOPB | WQFN         | RTW             | 24   | 250  | 210.0       | 185.0      | 35.0        |
| LMK00105SQX/NOPB | WQFN         | RTW             | 24   | 4500 | 367.0       | 367.0      | 35.0        |

## MECHANICAL DATA

RTW0024A



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