

# Chip Design 1

## Specification of Calculator Project Part 5: Top-level Design

Version: 1.0  
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# Introduction

After the IO control unit, the calculator control unit and the arithmetic logic unit have been coded and successfully tested in a simulation, they can be integrated into the top-level design. The top-level design is the topmost hierarchy level in the design which directly interfaces to the I/O pins of the FPGA. See the distance learning letter "Overview of Calculator Project" which includes a list of all ports of the top-level design. It is also worth having a look at the block diagram in order to understand how the interfaces of the sub-units need to be wired. A code skeleton of the top-level design is described in the following section.

## Code Skeleton of Top-level Design

```
-----
--
--          XXXXXXXX X      X XXXXXXXXXXXX X      X      XXXXXXXX XXXXXXXX
--          X      X      X      X      X      X      X      X      X      X
--          X      X      X      X      X      X      X      X      X      X
--          X      X      X      X      X      X      X      X      X      X
--          XXXXXXXX XXXXXXXX      X      X      X XXXXX XXXXXXXX X      X
--          X      X      X      X      X      X      X      X      X      X
--          X      X      X      X      X      X      X      X      X      X
--          X      X      X      X      X      X      X      X      X      X
--          X      X      X      X      X      X      XXXXXXXX XXXXXXXX
--
--          F A C H H O C H S C H U L E      -      T E C H N I K U M      W I E N
--
--          Embedded Systems Department
--
-----
--
--          Web:          http://www.technikum-wien.at/
--
--          Contact:      hoeller@technikum-wien.at
--
-----
--
--          Author:          Roland Höller
--
--          Filename:        calc_top_.vhd
--
--          Date of Creation: Sun Oct 20 12:17:48 2002
--
--          Version:         $Revision$
--
--          Date of Latest Version: $Date$
--
```

```
--      Design Unit:                Top-level Design of Calculator (Entity)
--
--      Description: This is the top-level design of the calculator project.
--                  It interconnects the sub-units 'IO control unit', 'calculator
--                  control unit' and 'arithmetic logic unit' and interfaces to
--                  the circuitry of the Digilent Basys3 FPGA board.
--
```

```
--
--      CVS Change Log:
--
--      $Log$
--
```

```
library ieee;
use ieee.std_logic_1164.all;
```

```
entity calc_top is
```

```
    port (clk_i      : in      std_logic;          -- 100 MHz system clock
          reset_i    : in      std_logic;          -- asynchronous reset
          ...);
```

```
end calc_top;
```

```
--
--      XXXXXXXX X      X XXXXXXXXXXXX X      X      XXXXXXXX XXXXXXXX      --
--      X      X      X      X      X      X      X      X      X      X      --
--      X      X      X      X      X      X      X      X      X      X      --
--      X      X      X      X      X      X      X      X      X      X      --
--      XXXXXXXX XXXXXXXX      X      X      X XXXXX XXXXXXXX X      X      --
--      X      X      X      X      X      X      X      X      X      X      --
--      X      X      X      X      X      X      X      X      X      X      --
--      X      X      X      X      X      X      X      X      X      X      --
--      X      X      X      X      X      X      XXXXXXXX XXXXXXXX      --
```

```
--      F A C H H O C H S C H U L E      -      T E C H N I K U M      W I E N      --
```

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--      Embedded Systems Department      --
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--      Web:                http://www.technikum-wien.at/      --
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```

```
--
--      Author:                Roland Höller
--
--      Filename:              calc_top_struct.vhd
--
--      Date of Creation:      Sun Oct 20 16:17:48 2002
--
--      Version:               $Revision$
--
--      Date of Latest Version: $Date$
--
--      Design Unit:           Top-level Design of Calculator (Architecture)
--
--      Description: This is the top-level design of the calculator project.
--                  It interconnects the sub-units 'IO control unit', 'calculator
--                  control unit' and 'arithmetic logic unit' and interfaces to
--                  the circuitry of the Digilent Basys3 FPGA board.
--
-----
--
--  CVS Change Log:
--
--  $Log$
--
-----

library ieee;
use ieee.std_logic_1164.all;

architecture struct of calc_top is

    component io_ctrl  -- component declaration of IO control unit
        port (clk_i      : in  std_logic;
              reset_i    : in  std_logic;
              swsync_o    : out std_logic_vector(15 downto 0);
              ...);
    end component;

    component calc_ctrl  -- component declaration of calculator control unit
        port (clk_i      : in  std_logic;
              reset_i    : in  std_logic;
              swsync_i    : in  std_logic_vector(15 downto 0);
              start_o     : out std_logic;
              ...);
    end component;

    component alu  -- component declaration of ALU
        port (clk_i      : in  std_logic;
              reset_i    : in  std_logic;
              start_i     : in  std_logic;
```

```

        ...);
end component;

signal swsync : std_logic_vector(15 downto 0);
signal start  : std_logic;
...

begin -- struct

    i_io_ctrl : io_ctrl -- instantiate IO control unit
    port map
        (clk_i    => clk_i,
         reset_i  => reset_i,
         swsync_o => swsync,
         ...);

    i_calc_ctrl : calc_ctrl -- instantiate calculator control unit
    port map
        (clk_i    => clk_i,
         reset_i  => reset_i,
         swsync_i => swsync,
         start_o  => start,
         ...);

    i_alu : alu -- instantiate ALU
    port map
        (clk_i    => clk_i,
         reset_i  => reset_i,
         start_i  => start,
         ...);

end struct;

```

## How to Proceed?

The next steps in the project are as follows:

- Write a VHDL entity for the top-level design, name the file, for example, “calc\_top.vhd” and store it in the “vhd” sub-folder of your project directory. The entity ports can be found in the distance learning letter “Overview of Calculator Project”.
- Write a VHDL architecture for the top-level design (see the previously described code skeleton), name the file, for example, “calc\_top\_struct.vhd” and store it in the “vhd” sub-folder of your project directory. Have a look at the block diagram (distance learning letter “Overview of Calculator Project”) in order to understand how the interfaces of the sub-units need to be wired.
- Create a VHDL configuration if you like to, but this is completely optional!

- Create a VHDL entity/architecture pair (and an optional configuration) for the testbench of the top-level design, name the files, for example, “tb\_calc\_top\_.vhd” and “tb\_calc\_top\_sim.vhd” and store them in the “tb” sub-folder of your project directory.
- Write “do”-scripts to compile and simulate the top-level design as described in the distance learning letter “Introduction to ModelSim-Intel FPGA Starter Edition” and store them in the “sim” sub-folder of your project directory.
- Simulate the top-level design using ModelSim and fix all bugs that you find. The top-level simulation is the most important type of simulation since it tests the complete design! Note, that bugs may appear even if the sub-blocks have been tested thoroughly, due to an incorrect wiring of the sub-components!
- If the top-level design was tested successfully, proceed with the last distance learning letter of the calculator project named “Part 6: Synthesis & Implementation”.

## Version

Version 1.0	Update to entire document for CHIP1

If you find mistakes or inconsistencies, please report them to the course supervisors via email.  
Thank you!