Introduction to VHDL VI

Finite State Machine – Railroad Crossing Example

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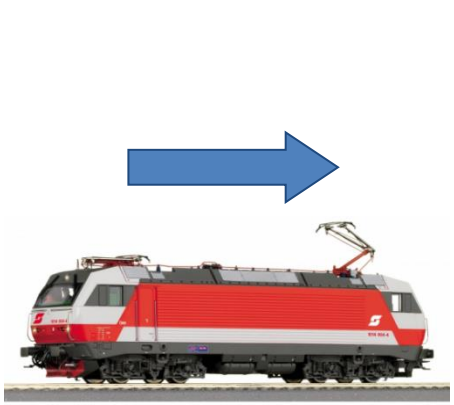
Class Example 2: Railroad Crossing FSM



Signal from Sensor:
“Train approaches”

Signal from Sensor:
“Train leaves crossing”

Class Example 2: FSM Specification (I)

- Design a FSM which controls a warning light and a gate on a railroad crossing
- The light can be turned on (logic 1) or off (logic 0) via a single signal
- The engine of the gate is operated by two signals ("up" and "down"). If the "down" signal is held at logic 1 for at least 4 seconds or longer, the gate is completely closed. Similarly, the gate is opened completely when the "up" signal is logic 1 for at least 4 seconds or longer. If “up” or “down” are held at logic 1 for less than 4 seconds, the gate will stay in an intermediate position (it can be completely opened or closed by subsequently setting “up” or “down” to logic 1 for an additional amount of time in such cases). If both, the "up" and the "down" signal are held at logic 1, the engine will not move.

Class Example 2: FSM Specification (II)

- Trains can pass the crossing from left to right only, as shown on Slide 2
- In the "open" state, the gate is open and the warning light is dark
- Once a train approaches, a one pulse with a duration t_D of $1 < t_D < 2$ seconds is generated on a signal coming from a sensor. This signal shall immediately (with a response time of 1 second) close the gate and enable the warning light to start blinking with a frequency of exactly 0.5 Hz.
- If the train leaves the crossing, a one pulse with a duration t_D of $1 < t_D < 2$ seconds is generated on another signal which shall open the gate. Once the gate is opened completely the warning light shall be turned off.

Class Example 2: FSM Specification (III)

- It takes 6 seconds at minimum for the fastest trains to pass the track between the “train approaches” and the “train leaves” sensor
- Once a train passes the “train approaches” sensor, an external safety mechanism (which is not part of this FSM) ensures that no other trains can enter the track between the “train approaches” and the “train leaves” sensor. This safety mechanism also makes sure that subsequent trains will enter the track at the “train approaches” sensor not earlier than 6 seconds after the preceding train passes the “train leaves” sensor.
- The frequency of the FSMs clock signal is 1 Hz
- The asynchronous reset signal (high active) should bring the application to a safe system state, independently of any previous actions or states

Class Example 2: Railroad Crossing FSM

- Draw a state diagram of the FSM
- Describe and simulate the VHDL code of the FSM