

Page:

Date:

Small \rightarrow AC

Large \rightarrow DC

$V_{in} > V_{out}$ \rightarrow linear

$V_{in} < V_{out}$ \rightarrow Saturation

V_{ds} \rightarrow AC small signal

V_{DS} \rightarrow DC

V_{DS} \rightarrow small + large

chap-1

Introduction of VLSI

VLSI (Very Large Scale Integration (> 10000))

- fabrication
- propagation delay
(interconnection between 500 pows. or 50 frows.)
 \downarrow PD less more \downarrow PD more
- In SSI (transistor \rightarrow ms) in VLSI (trans. \rightarrow ns)
interconnection \rightarrow ns inter. \rightarrow ns
 \downarrow can be ignored \downarrow can't be ignored

moore's law effectiveness double every after 18 months.

technology means channel length of mos or we can say that distance between source and drain.

- speed and power are tradeoff of VLSI at one time we can improve only one either speed or power.

Pros and cons of VLSI:

Pros:

- Smaller size
- Lower cost
- Lower power
- Higher reliability
- More functionality

Cons:

- Long design and fabrication time
- Higher risk to project

Terms:

Wafer

Die (Single IC having 4 gates)

Yield = Percentage of good die

Technology = min feature size

Scaling

Transistor density

TTM (Time to market) = 18 months

Design style:

(1) Full custom (ASIC → app. specification IC)

[larger TTM, performance max., size less]

(2) Programmable

PLD (Quick prototyping small TMT)

CPLD

FPGA

(3) Semicustom (less TTM, performance is less as compare to full custom)

- Gate array
- Standard cell based

⇒ Structure level

(4 bit counter using 1 bit @ counter, we don't bother about the 1 bit counter)

• Behavioural level domain

• Geometric domain

Design Approaches:

- Top down approach

(4 bit counter → 1 bit counter → adder → transistor)

- Bottom up approach

(Nand gate → counter → trans. → chip)

Design Hierarchy:

- regularity (regular pattern in design) cost is less
- modularity no of mask is less

- locality (avoid the no. of interconnection)

which element is generated is placed nearer to the module

Design Quality:

- Testability

- Yield and manufacturability

- Technology updateability (technology update to new design)

Testability:

- generate of good test vectors
- availability of reliable test fixtures at speed
- design of testable chips.

Yield & manufacturing:

100 chips are working that percentage is valid

functional
(not at speed testing)

parametric
(at speed testing)

manufacturing:

parametric yield estimation
" minimization
process variation minimization

CAD Tools:

- Synthesis tools (What is actual hardware \rightarrow logic design)
- layout tools (practical design)
- simulation & verification tools (P/I is given & O/P is checked)

company name: cadence & mentor graphics (for cad tools)

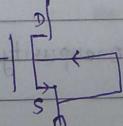
Chap-2

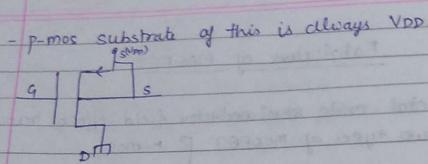
Fabrication of MOSFET

- metal oxide semiconductor field effect transistor
- two types of MOSFET
 - $n\text{-mos}$
 - $p\text{-mos}$
- power consumption (static = VI . I is dependent on size of mos, In CMOS current component is not there so consume = 0)
- dynamic $P = CV^2f$
- CMOS has property of scale down, that its follows the same VI characteristic.

Why CMOS?

- low cost of fabrication (25-26 mask are required in BJT, but 10 core required for made the mos.)
- low power consumption
- High speed
- High complexity
- placing both digital and analog circuits on the same chip.
- n-mos substrate of this is always ground and mobility of ee is high (speed is high)





In p-mos, we can't connect the transistor with multiple supply voltage on single chip, so we required multiple wafers \rightarrow cost issue.

Silicon wafers

as size increases, handling is difficult.

- N type $<111>$ (d_{1,4,2}) 45°

N type $<100>$ (1 direction) 180°

p-type $<111>$ only primary flat

p-type $<100>$ 90° Secondary & primary \rightarrow interference changes are less

substrate type: interference changes are 10 times higher in $<111>$ than in $<100>$ at the time of oxidation.

↓ ↓
 (at high voltage) (at low voltage we can work)

Fabrication steps:

① Wafer Cleaning

Class 1000 means only one impurity there in 1000 elements.

② Oxidation

Create a layer of SiO₂

Thin oxide
(between gate)

Thick oxide
(between two mosfet)

③ Photolithography

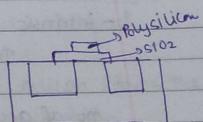
PR \rightarrow photo resist

Positive negative

UV light passes non-soluble
and soluble

④ Implantation

p or n-type diffusion



⑤ Etching

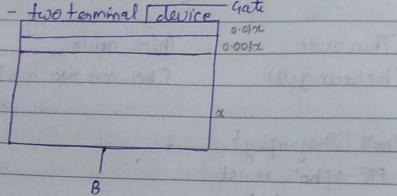
To remove the oxide layer, which are not required because of that n+ diffusion layer are not straight.

local oxidation of silicon, where we required silicon oxide layer whenever we have to make the layer of oxide by using nitride.

Chapter - 3

MOS

- Metal Oxide Semiconductor
- two terminal device



- Gate & B are ohmic contacts, but if we taken SiO_2 contact as terminal, that's not ohmic, so we do not take it.

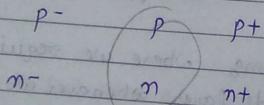
Intrinsic semiconductor

$$n_i = 1.45 \times 10^{10} \text{ cm}^{-3}$$

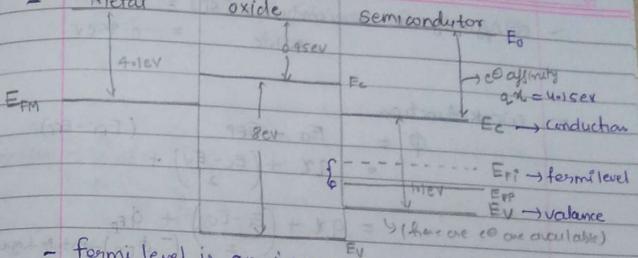
No. of acceptor NA in p-type substrate

$$n_p = \frac{N_A}{2} \rightarrow e\odot \text{ in p-type}$$

$$P_p = N_A \rightarrow \text{holes in p-type}$$



chosen for substrate



- Fermi level is an imaginary level, its separate the conduction and valence band.
- if we added ^(acceptor) holes, EFi down \rightarrow p-type substrate
- if holes = electrons, then Fermi level at the middle of conduction & valence band gap (forbidden gap)
- EFi \rightarrow Fermi level for intrinsic material.

for germanium energy gap is $<$ silicon, fasts the re and having the instability is high.

- $Eo \rightarrow$ free space
- for semiconductor: energy gap between Conduction band & free space \rightarrow electron affinity α_E
- for p-type EFi \rightarrow shifted to EFP (downward)
- n-type EFi \rightarrow to EFN (upward)

$Eo - EFP \rightarrow$ work function
energy required to $\text{e}\odot$ moves from fermi level to free space.

- electron affinity for semiconductor (Si) = 4.15 eV
oxide = 0.95 eV

- work function

$$\begin{aligned}\phi &= E_0 - E_{FP} \quad (E_Fi - E_Fp) \\ &= q\chi + \left(\frac{E_c - E_v}{2}\right) + \text{based on doping level} \\ &= q\chi + \left(\frac{E_c - E_v}{2}\right) + \phi_{Fp} \quad (-\phi_{Fn}) \rightarrow \text{in type logo, bcoz level shifted to up}\end{aligned}$$

Fermi potential

$$\phi_{Fp} = \frac{kT}{q} \ln \frac{n_i}{N_A} \quad (\text{for p-type})$$

T = 300 K

K = 1.38×10^{-23}

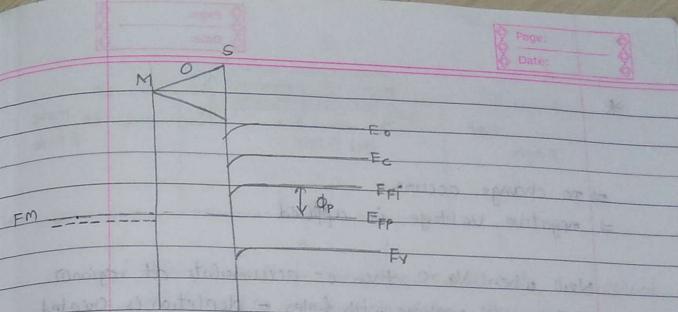
$$\phi_{Fn} = \frac{kT}{q} \ln \frac{N_D}{n_i} \quad (\text{for n-type})$$

$$\Rightarrow \text{if } \phi_{Fp} = 0.2 \text{ ; then } \phi = 4.15 + 1.1 + 0.2$$

Work done = 4.9 eV

$$\Rightarrow \phi_m = 4.1 \text{ eV}$$

$$\phi_s = 4.9 \text{ eV}$$

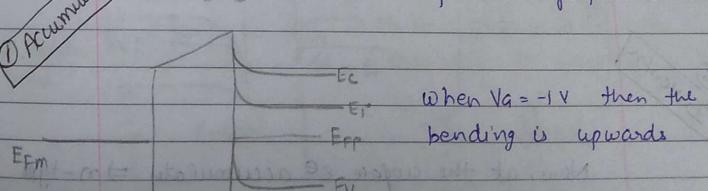


$$V_{FB} \rightarrow \text{flat band voltage} = \phi_m - \phi_s = V_{FB}$$

to remove the bending, 0.8 eV has to be applied

18-jcm

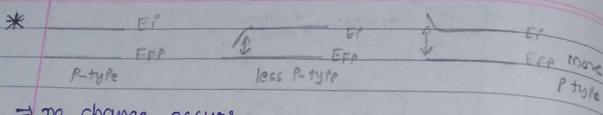
① Accumulation



When Vg = -1 V then the bending is upwards

This region ① in MOS is called accumulation.

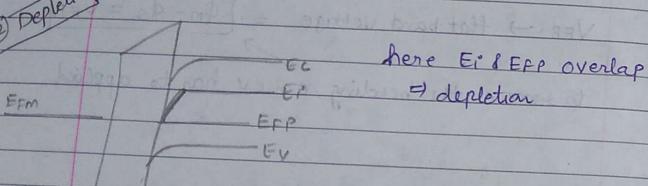
when gate is given voltage $< D$ then the holes from semiconductor collects on the surface as V_g is fixed more (-0.8 eV) \Rightarrow flattening takes place in graph.



- \Rightarrow no change occurs
- \Rightarrow negative voltage is applied.

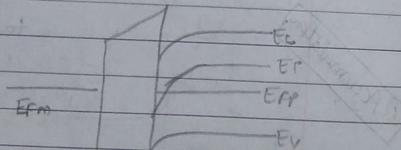
Now when $V_g > 0$ then e⁻ accumulate at region①
 \Rightarrow they will combine with holes \Rightarrow depletion is created
 (no holes & e⁻ are left) \Rightarrow no free carriers.

② Depletion



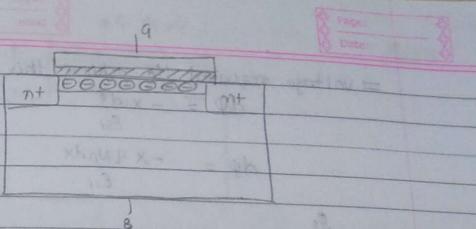
Now when V_g is made more the +ve ($V_g >> 0$) then
 e⁻ will accumulate at region① and will not combine
 with holes as no holes are left.

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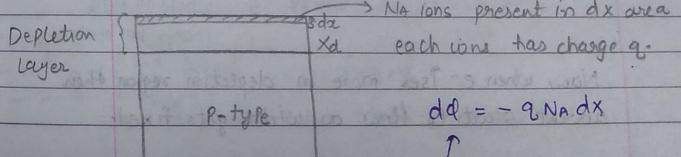
Now, at the surface e⁻ accumulate \Rightarrow n-type
 material is formed \Rightarrow Inversion takes place

③ Inversion



- Threshold voltage \Rightarrow voltage which is to be applied on gate for inversion to take place.
- Due to thin layer of oxide, so when $V_g >>> 0$ then this layer would break down, transistor stops working \Rightarrow no breakdown takes place in depletion as more V_g is required.

- There is no effect of n+ region because no oxide layer and metal is present on it. Secondly, as n+ type material is present \Rightarrow effect is negligible when inversion is done in p-type material.
- for p-type material we take p or p- not p+ bcoz Vg required by p+ will be very much high \Rightarrow oxide layer would break down before depletion layer is created.



$dQ = -qNa dx$

this much amount of charge is removed from this layer.

\Rightarrow Voltage required to achieve this is

$$d\psi = -x d\phi$$

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$$d\psi = -x \frac{q N_A dx}{\epsilon_s}$$

$$\downarrow \Phi_{FP} \quad \int_{\Phi_{FP}}^{\Phi_s} d\psi = \int_0^{X_d} x \frac{q N_A dx}{\epsilon_s}$$

$\Phi_{FP} \rightarrow$ initial potential diff b/w 2 fermi levels (present in
 $\phi_s \rightarrow$ surface potential (present only on whole matu
surface of material)

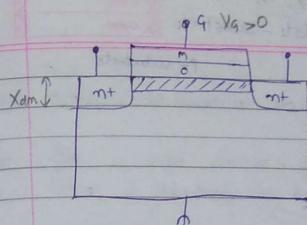
$$|\phi_s - \phi_F| = \frac{x_d^2 q N_A}{2 \epsilon_s}$$

$$x_d = \sqrt{\frac{2 \epsilon_s |\phi_s - \phi_F|}{q N_A}}$$

$$x_{dm} = x_{dmax} = \sqrt{\frac{2 \epsilon_s |\phi_s - \phi_F|}{q N_A}} \quad (\because \phi_s = -\phi_F)$$

at this point
whole P-type
change to n-type.

Now, when e- \uparrow s more in depletion region than
current starts to flow as width gets fixed.



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$V_{TO} \rightarrow$ shows that substrate is connected to ground.
 $V_{TH} \rightarrow$ logic threshold voltage (avg. voltage of high and low voltage)

Ex: for a mos structure substrate $N_A = 10^{16}/cm^3$ the
charge dens. gate is made up of polysilicon with charge density
 $N_D = 2 \times 10^{20}/cm^3$. find the flat band voltage
for the mos structure?

$$n_i = 1.45 \times 10^{10} cm^{-3} \quad K_T = 26 mV$$

$$N_A = 10^{16} cm^{-3}$$

$$\Phi_{FP} = \frac{K_T}{q} \ln \frac{n_i}{N_A}$$

$$= \frac{1.38 \times 10^{-23} \times 300}{1.6 \times 10^{-19}} \ln \left(\frac{1.45 \times 10^{10}}{10^{16}} \right)$$

$$= 26 \times 10^{-3} \ln \left(\frac{1.45 \times 10^{10}}{10^{16}} \right)$$

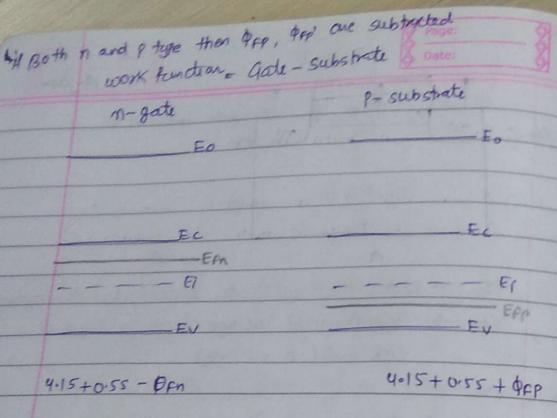
$$E_C = E_F + \frac{K_T}{q} \ln \left(\frac{1.45 \times 10^{10}}{10^{16}} \right)$$

$$= -0.349 eV$$

$$E_V = E_F + \frac{K_T}{q} \ln \left(\frac{1.45 \times 10^{10}}{10^{16}} \right) + 0.349$$

$$= 0.607 eV$$

$$|\Phi_{Fn}| = \frac{K_T}{q} \ln \frac{N_D}{N_A} = \frac{26 \times 10^{-3}}{1.6 \times 10^{-19}} \ln \left(\frac{2 \times 10^{20}}{1.45 \times 10^{16}} \right) = 0.607 eV$$



$$\text{then work done} = 0.956 \quad \text{--- (1)}$$

$$X_{dm} = \frac{2 \epsilon_s / 2\phi_f}{q N_A}$$

$\Rightarrow V_{th} \rightarrow \text{logic threshold}$

$V_t \rightarrow \text{voltage at which MOS diode is in cut off}$

$$V_t < V_{th}$$

V_{to}

in this four parameters are there:

i) V_{FB}

$V_{FB} = -\frac{Q_{BO}}{C_{OX}}$

nullify effect of diff b/w work function.

ii) create depletion

$$\frac{Q_{BO}}{C_{OX}} \rightarrow \text{depletion} \quad (V = q/C)$$

$C_{OX} \rightarrow \text{capacitance by oxide}$

iii) $2\phi_f \rightarrow \text{Inversion voltage}$

iv) $\frac{Q_{OX}}{C_{OX}} \rightarrow \text{to remove charges present on the surface of body and oxide.}$

$$V_{TO} = V_{FB} - 2\phi_f - \frac{Q_{BO}}{C_{OX}} - \frac{Q_{OX}}{C_{OX}} \quad \text{--- (A)}$$

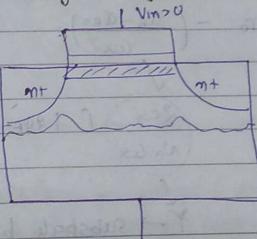
for p-type: $2\phi_f \rightarrow +ve$

$$Q_{BO}/C_{OX} \rightarrow +ve \quad \left. \begin{array}{l} Q_{OX}/C_{OX} \rightarrow +ve \\ V_{FB} \rightarrow +ve \end{array} \right\} V_{TO} \rightarrow -ve$$

$$Q_{OX}/C_{OX} \rightarrow +ve$$

$$V_{FB} \rightarrow +ve$$

\Rightarrow if body voltage is not zero $V_B \neq 0$



- $V_B < 0$ then V_{TO} is less as we calculated in eqn (A)

- $V_B > 0$ then V_{TO} is more as we calculated in eqn (A)

- If $V_B < 0$, then V_G required would be less as holes would get attracted to terminal B \Rightarrow e⁺ gets free easily.
- If $V_B > 0$, then V_G required would be more as holes would repel from terminal B and e⁺ would attract to terminal B.

$$Q_B = \frac{2\epsilon_0 (\beta\phi_F + V_{SB})}{N_A X_d^2}$$

$V_{SB} \rightarrow$ voltage applied to body

if V_{BS} is considered then it would be subtracted.

$$V_T = V_{FB} - \frac{2\phi_F}{C_{ox}} - \frac{Q_{BO}}{C_{ox}} - \frac{Q_B}{C_{ox}}$$

$$= V_{FB} - \frac{2\phi_F}{C_{ox}} - \frac{Q_{BO}}{C_{ox}} - \frac{Q_B - Q_{BO}}{C_{ox}}$$

$$V_T = V_{TO} - \left(\frac{Q_B - Q_{BO}}{C_{ox}} \right)$$

\downarrow

$$\frac{2\epsilon_0}{N_A C_{ox}} (12\phi_F + V_{SB} - 12\phi_F)$$

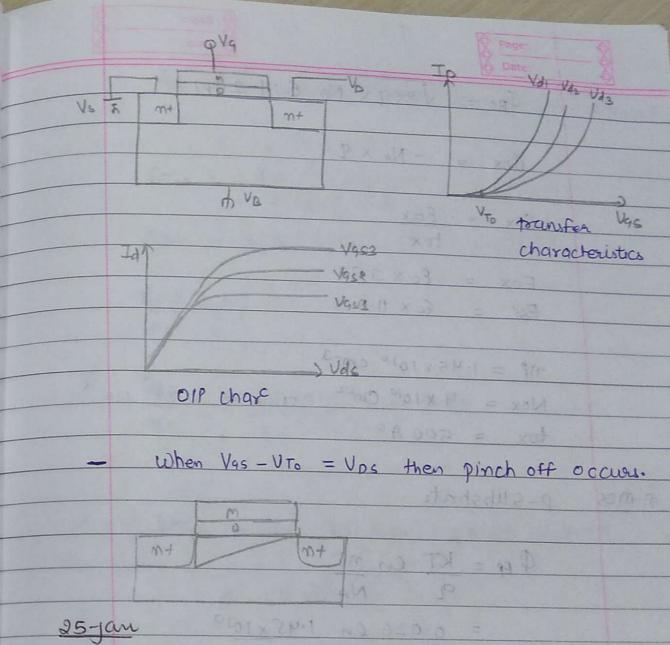
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\rightarrow Substrate bias coefficient

Even if body and source are connected to same potential then calculate V_{TO}

$V_{TO} \rightarrow$ level 0 design

$V_T \rightarrow$ level 1 design



Ex 8 Metal gate NMOS has substrate doping density of $10^{16}/cm^3$

thickness of oxide is 500 \AA . Oxide interface charges are $4 \times 10^{10}/cm^2$. Find out the threshold voltage for NMOS.

\rightarrow Substrate voltage bias = 0

Body grounded

$$V_{TO} = V_{FB} - \frac{2\phi_F}{C_{ox}} - \frac{Q_{BO}}{C_{ox}}$$

\approx

$$Q_{BO} = \sqrt{\epsilon_0 \times q \times N_A (\epsilon_{si} - 2\phi_F)}$$

$$Q_{ox} = -N_A \times q$$

$$C_{ox} = \frac{\epsilon_0}{t_{ox}}$$

$$\epsilon_{ox} = \epsilon_0 \times 3.97$$

$$\epsilon_{si} = \epsilon_0 \times 11.7$$

$$n_i = 1.45 \times 10^{10} \text{ cm}^{-3}$$

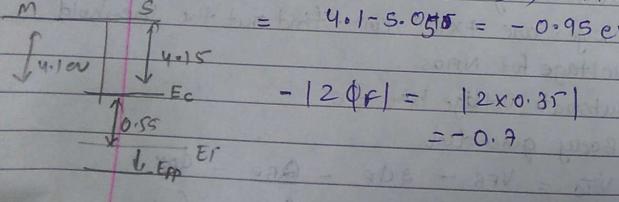
$$N_{ox} = 4 \times 10^{10} \text{ cm}^{-2}$$

$$t_{ox} = 500 \text{ Å}$$

n-mos p-substrate

$$\begin{aligned} \phi_F &= \frac{kT}{q} \ln \frac{n_i}{N_A} \\ &= 0.026 \ln \frac{1.45 \times 10^{10}}{10^{10}} \\ &= -0.395 \approx -0.35 \end{aligned}$$

$$V_{FB} = + (4.15 + 0.55 + 0.35) - 4.0 = \phi_m - \phi_s$$



$$Q_{BO} = \sqrt{q \times 1.6 \times 10^{-19} \times 10^{16} \times 8.85 \times 10^{-12} \times 11.7 \times 0.9}$$

$$= 0.48 \times 10^{-6}$$

$$C_{ox} = \frac{8.85 \times 10^{-12} \times 3.97}{500 \times 10^{-10}} = 0.07 \times 10^{-2}$$

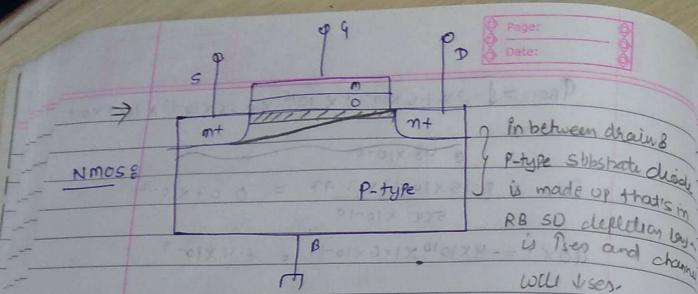
$$Q_{ox} = -4 \times 10^{10} \times 10^6 \times 10^{-19} = 6.4 \times 10^{-9}$$

$$Q_{ox} = -0.09$$

$$\frac{Q_{BO}}{C_{ox}} = \frac{0.48 \times 10^{-6}}{0.07 \times 10^{-2}} = 0.69$$

$$V_{TO} = -0.95 + 0.7 + 0.69 + 0.09$$

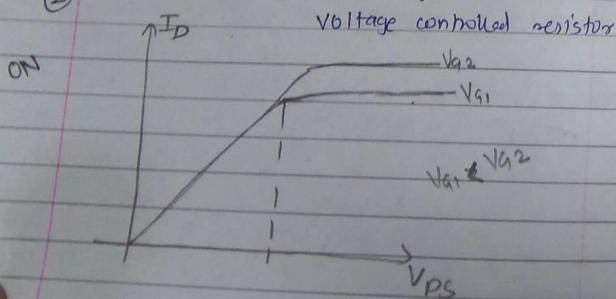
$$= 0.53 \text{ V}$$



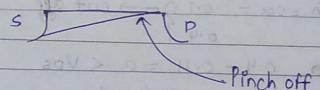
- When we apply V_D voltage and then there is no current flow.
- and if $V_G < 0 \rightarrow$ then also current will not flow. "accumulation"
- ① if $V_G > 0 \rightarrow$ "Depletion"; cut off

OFF $V_G < V_{T0} \rightarrow$ "cut off", no current will flow, channel is not there.

② $V_G > V_{T0} \rightarrow$ "linear region"

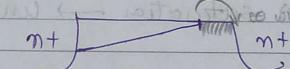


- ③ Channel voltage and drain voltage if same then depletion is more on the side of drain.



that voltage is called as "Pinch off" and region is "Saturation."

- $V_{DS} > V_{GS} - V_{TO}$
- When V_{DS} is also less, but at that time channel will jump will cut/break.



When channel is cut/break, then e⁺ will jump to the drain and that energy is comes from the $E = V/d$, d is very less, so current will increases due to high value of V_G & V_D voltage.

- Even after pinch off, breaking of channel at drain, if we bring the V_{DS} , the whole channel is breaks \rightarrow breakdown \rightarrow oxide damaged \rightarrow this condition is known as punch through.

* In MOSFET

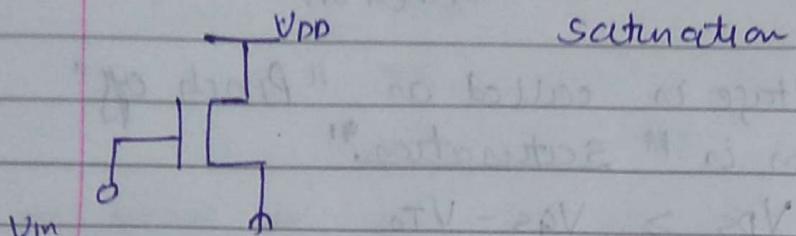
transistor starts in saturation and then it goes in linear region.

for ex8 $V_{DS} = V_{DD} = 2V$ cut starting we have do (4)

V_{GS} is slowly - 2 increases

$$V_{in} = V_{GS} = 0.1 \xrightarrow{0.4} \text{cut off}$$

$$0.4 - 0.4 = 0 < V_{DS}$$



* Cutoff \rightarrow saturation \rightarrow linear

then

to become in parallel, no drain stop now -
because there is no load will not go to zero
because there is no load will not go to zero
because there is no load will not go to zero
because there is no load will not go to zero