

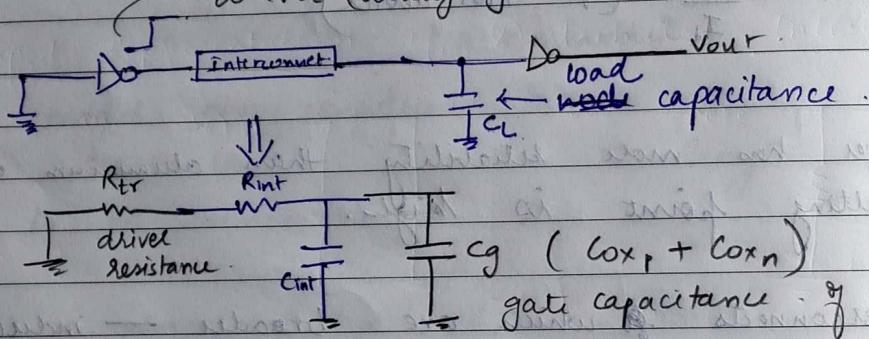
CHAPTER - 4

Electrical size of Interconnect (l_e) = $\frac{l}{\lambda}$ (physical length of interconnect)
 λ (wavelength of signal propagating)

$< 0.1 \rightarrow$ lumped RC model can be used

$> 0.1 \rightarrow$ RLC distributed model

\Rightarrow Lumped RC model for Interconnect



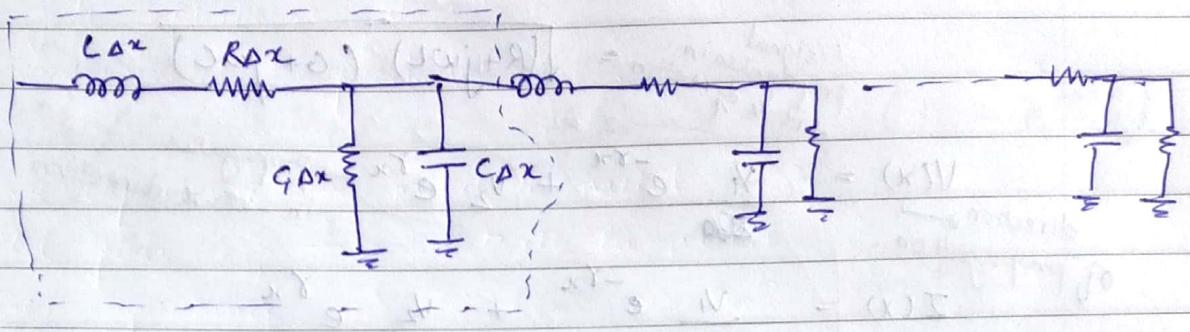
$$T_{RC} = (R_{drv} + R_{int}) (C_g + C_{int})$$

$$V_{out} = (1 - e^{-t/T_{RC}})$$

$$\text{Propagation delay} = 0.693 T_{RC}$$

- for wide interconnect, this model is not accurate

⇒ RLC Distributed Model



- Change in voltage and current

- $dV = -L \frac{dI}{dx} dx - RI dx$ —①

(Even sign bcoz voltage drop occurs)

- $dI = -c \frac{dV}{dx} dx - GV dx$ —②.

- from ① $\frac{dV}{dx} = -L \frac{dI}{dx} - IR$.

- from ② $\frac{dI}{dx} = -c \frac{dV}{dt} - VG$.

- $\frac{dV}{dx}(x,s) = -(R+SL) I(x,s)$

- $\frac{dI}{dx}(x,s) = -(G+SC) V(x,s)$

$R+SL = Z \rightarrow$ impedance per unit length

$G+SC = Y \rightarrow$ admittance per unit length.

$$\frac{dV^2}{dx^2}(x,s) = ZY V(x,s) = \gamma^2 V(x,s)$$

$$\frac{dI^2}{dx^2}(x,s) = ZY I(x,s) = \gamma^2 I(x,s)$$

$$\gamma = \sqrt{ZY}$$

$$\gamma(s) = \alpha + j\beta = \sqrt{Z_0}$$

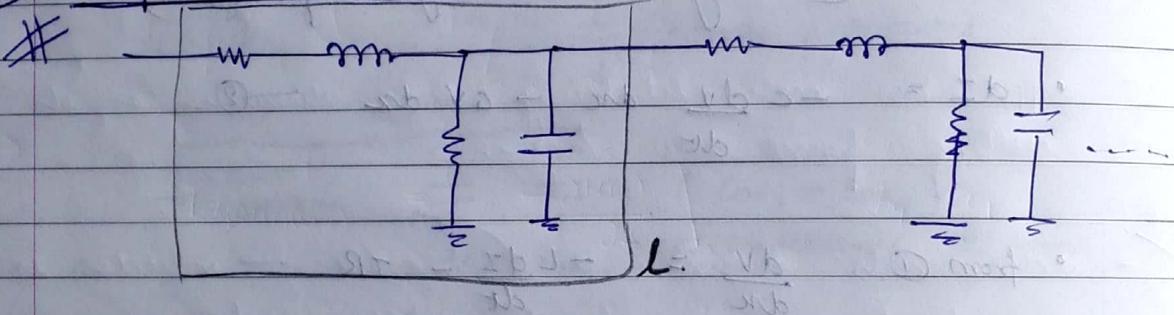
signal propagates in
+ve x-direction = $\sqrt{(R+j\omega L)(G+j\omega C)}$

$V(x) = \frac{V_1}{Z_0} e^{-rx} + \frac{V_2}{Z_0} e^{rx}$ → propagates
in -ve x-direction

$I(x) = \frac{V_1}{Z_0} e^{-rx} + \frac{V_2}{Z_0} e^{rx}$

$$Z_0 = \sqrt{\frac{R+j\omega L}{G+j\omega C}}$$

Q18. Lumped Representation of Distributed Interconnect.



Driver → [Interconnect] → Driver

$n \leftarrow$ no. of sections to be considered for a specific length of interconnect so that accuracy is not affected
 ↴ difference in delay is very less.

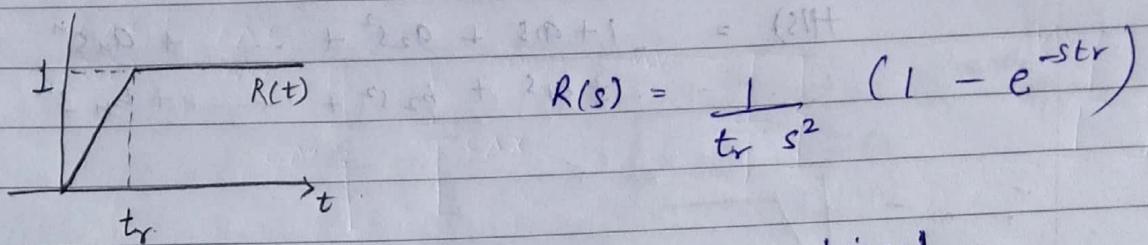
$$\text{Signal time } n \geq 5.6 \sqrt{Lc}$$

t_r → shortest rise time

l → length of interconnect

L, C → inductance & capacitance of Interconnect

Determining highest frequency of Interconnect.

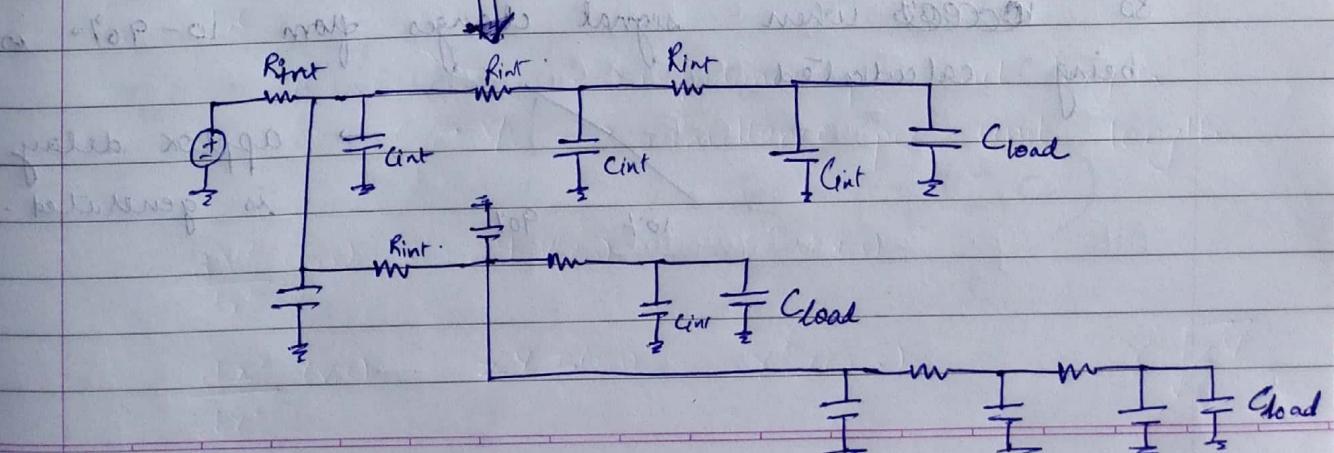
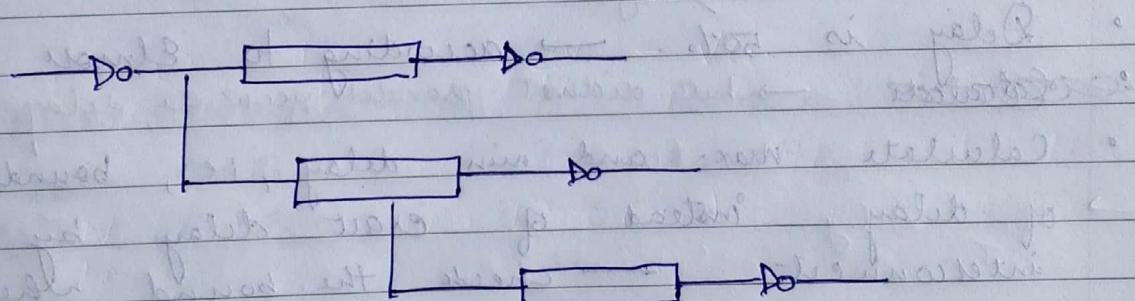


$$R(\omega) = \frac{tr}{2} \frac{[\sin \omega]}{\omega^2}$$

$$f_{\max} = \frac{0.24}{tr} \quad \text{or} \quad f_{\max} = \frac{0.35}{tr}$$

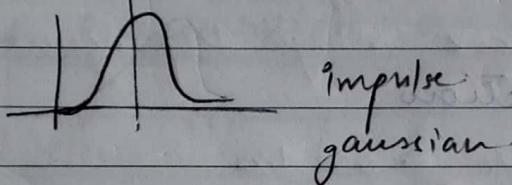
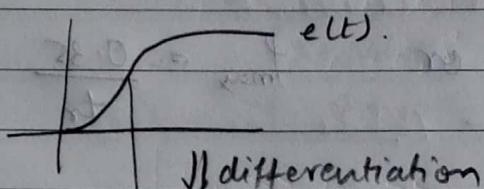
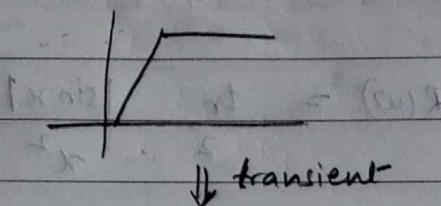
Model Order Reduction.

why required? → ① Large number of interconnects present on chip.
 ② complex nature



Elmore delay Model → tried to calculate accurate delay.

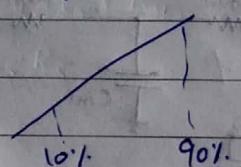
$$H(s) = \frac{1 + a_1 s + a_2 s^2 + \dots + a_n s^n}{1 + b_1 s + b_2 s^2 + \dots + b_n s^n}$$



$$T_{Elmore(\max)} = -\frac{\partial H(s)}{\partial s} \Big|_{s=0} = b_1 - a_1$$

- Delay is 50% → according to Elmore.
- ~~but didn't provide accurate delay~~
- Calculate max. and min delay, i.e., boundary of delay instead of exact delay by interconnect — check the bound whether accepted or not.

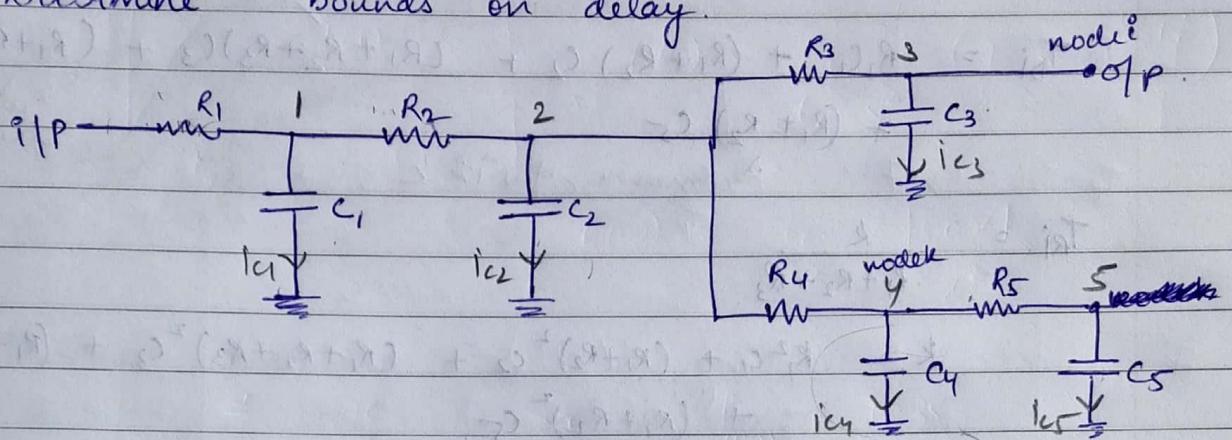
So ~~100%~~ when signal changes from $10-90\%$ is being calculated



→ approx delay is generated.

Algorithm by Penfield - Rubinsteain

Determine 'bounds' on delay.



i = Index refer to o/p node in RC tree

k = Index cover every capacitor within circuit

C_k = lumped capacitor at node k

R_{ii} = Resistance of unique path b/w i/p & o/p i

R_{kk} = " " " " " node k

R_{ik} = Resistance of portion i of unique path b/w i/p & o/p i that is common with unique path b/w o/p and node k.

$$R_{ii} = R_1 + R_2 + R_3 \quad R_{ik} \ll R_{kk}$$

$$R_{kk} = R_1 + R_2 + R_4 \quad R_{ik} \ll R_{ii}$$

$$R_{ik} = R_1 + R_2$$

$$T_p \rightarrow \text{upper bound} \quad T_p = \sum_k R_{kk} C_k$$

T_{di} → delay on i

T_{ri} → lower bound

$$T_{di} = \sum_k R_{ik} C_k$$

$$T_{ri} = \frac{\left(\sum_k R_k^2 C_k \right)}{R_{ii}}$$

$$T_p = R_1 C_1 + (R_1 + R_2) C_2 + (R_1 + R_2 + R_3) C_3 + (R_1 + R_2 + R_4) C_4 \\ + (R_1 + R_2 + R_4 + R_5) C_5$$

$$T_{di} = R_1 C_1 + (R_1 + R_2) C_2 + (R_1 + R_2 + R_3) C_3 + (R_1 + R_2) C_4 \\ + (R_1 + R_2) C_5$$

↓ common b/w 1 & 2

$$T_{ri} = \frac{k}{R_1 + R_2 + R_3}$$

$$k = R_1^2 C_1 + (R_1 + R_2)^2 C_2 + (R_1 + R_2 + R_3)^2 C_3 + (R_1 + R_2)^2 C_4 \\ + (R_1 + R_2)^2 C_5.$$

$$\boxed{T_{ri} \ll T_{di} \ll T_p}$$

Elmore's delay.

→ Voltage drop along the path.

$$1 - v_i(t) = \sum_k R_k i_k C_k \frac{d v_k}{dt}$$

node 3

$$1 - v_3(t) = (i_4 + i_{c2} + i_{c3} + i_{c4} + i_{c5}) R_1 + (i_{c2} + i_{c3} + i_{c4} + i_{c5}) R_2 \\ + (i_{c3} R_3)$$

→ Node Delay.

$$T_{d1} = (C_1 + C_2 + C_3 + C_4 + C_5) R_1$$

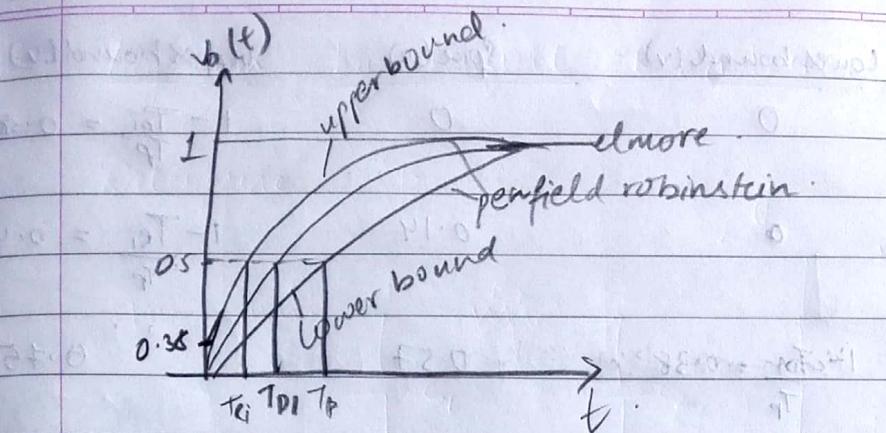
$$T_{d2} = T_{d1} + (C_2 + C_3 + C_4 + C_5) R_2$$

$$T_{d3} = T_{d2} + C_3 R_3$$

$$T_{d4} = T_{d2} + (C_4 + C_5) R_4$$

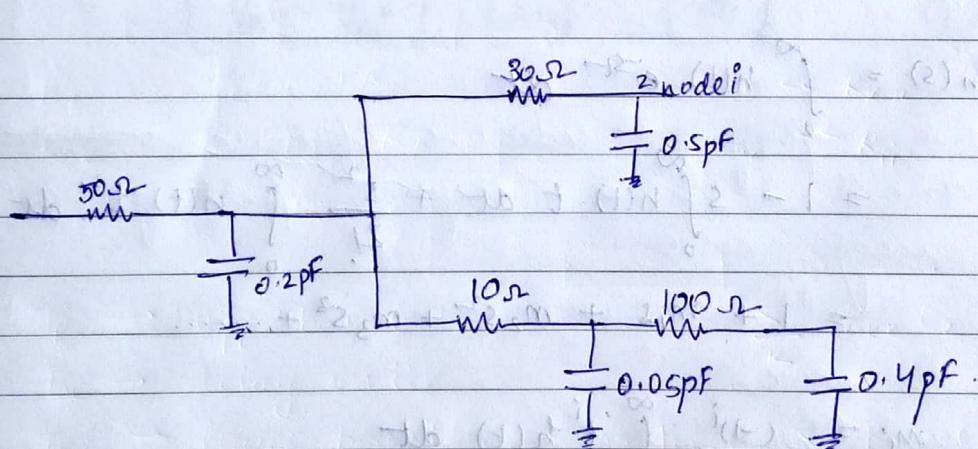
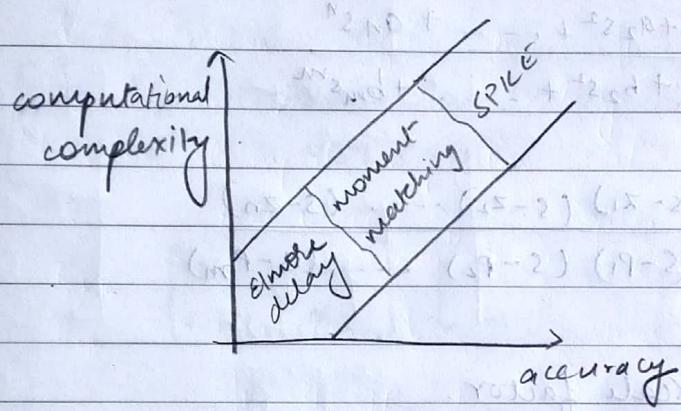
$$T_{d5} = T_{d4} + C_5 R_5$$

All cap. are in parallel



Moment matching

AWE - asymptotic wave evaluation



$$T_p = R_1 C_1 + (R_1 + R_2) C_2 + (R_1 + R_2 + R_3) C_3 + (R_1 + R_2 + R_3 + R_4) C_4 = 117 \times 10^{-12} \text{ s}$$

$$T_{Df} = R_1 (C_1 + C_2 + C_3 + C_4) + R_2 C_2 = 72.5 \times 10^{-12} \text{ s}$$

$$T_{ci} = \frac{R_1^2 C_1 + (R_1 + R_2)^2 C_2 + R_1^2 C_3 + R_1^2 C_4}{R_1 + R_2} = 60.3 \times 10^{-12} \text{ s}$$

Time (ps)	lower bound (v)	spine (v)	upper bound (v)
0	0	0	$1 - \frac{T_{D1}}{T_P} = 0.38$
$T_{D1} - T_{R1} = 12.2$	0	0.14	$1 - \frac{T_{E1}}{T_P} = 0.48$
$T_F - T_{R1} = 56.7$	$1 - \frac{T_{D1}}{T_P} = 0.38$	0.57	0.45

Moment Matching (AWE)

System Transfer function

$$H_n(s) = \frac{1 + a_1 s + a_2 s^2 + \dots + a_n s^n}{1 + b_1 s + b_2 s^2 + \dots + b_m s^m}$$

$$H_n(s) = K \frac{(s - z_1)(s - z_2) \dots (s - z_n)}{(s - p_1)(s - p_2) \dots (s - p_m)}$$

$K = \frac{a_n}{b_m}$ = scale factor.

Why?

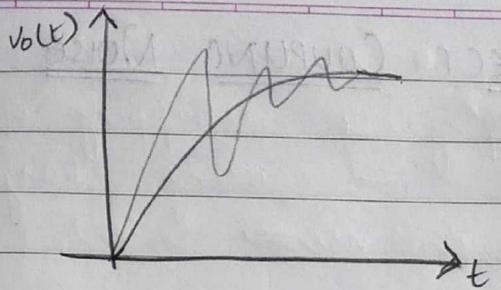
$$\begin{aligned} H_n(s) &= \int_0^\infty h(t) e^{-st} dt \\ &= 1 - s \int_0^\infty h(t) t dt + \frac{s^2}{2!} \int_0^\infty h(t) t^2 dt + \dots \\ &= 1 + m_1 s + m_2 s^2 + m_3 s^3 + \dots \end{aligned}$$

$$m_i = \frac{(-1)^i}{i!} \int_0^\infty t^i h(t) dt$$

$$H_n(s) = \frac{k_1}{s - p_1} + \frac{k_2}{s - p_2} + \dots + \frac{k_m}{s - p_m}$$

p_1, p_2, p_3, \dots — poles

k_1, k_2, k_3, \dots — residue of transfer funcⁿ.



e.g. AWE:

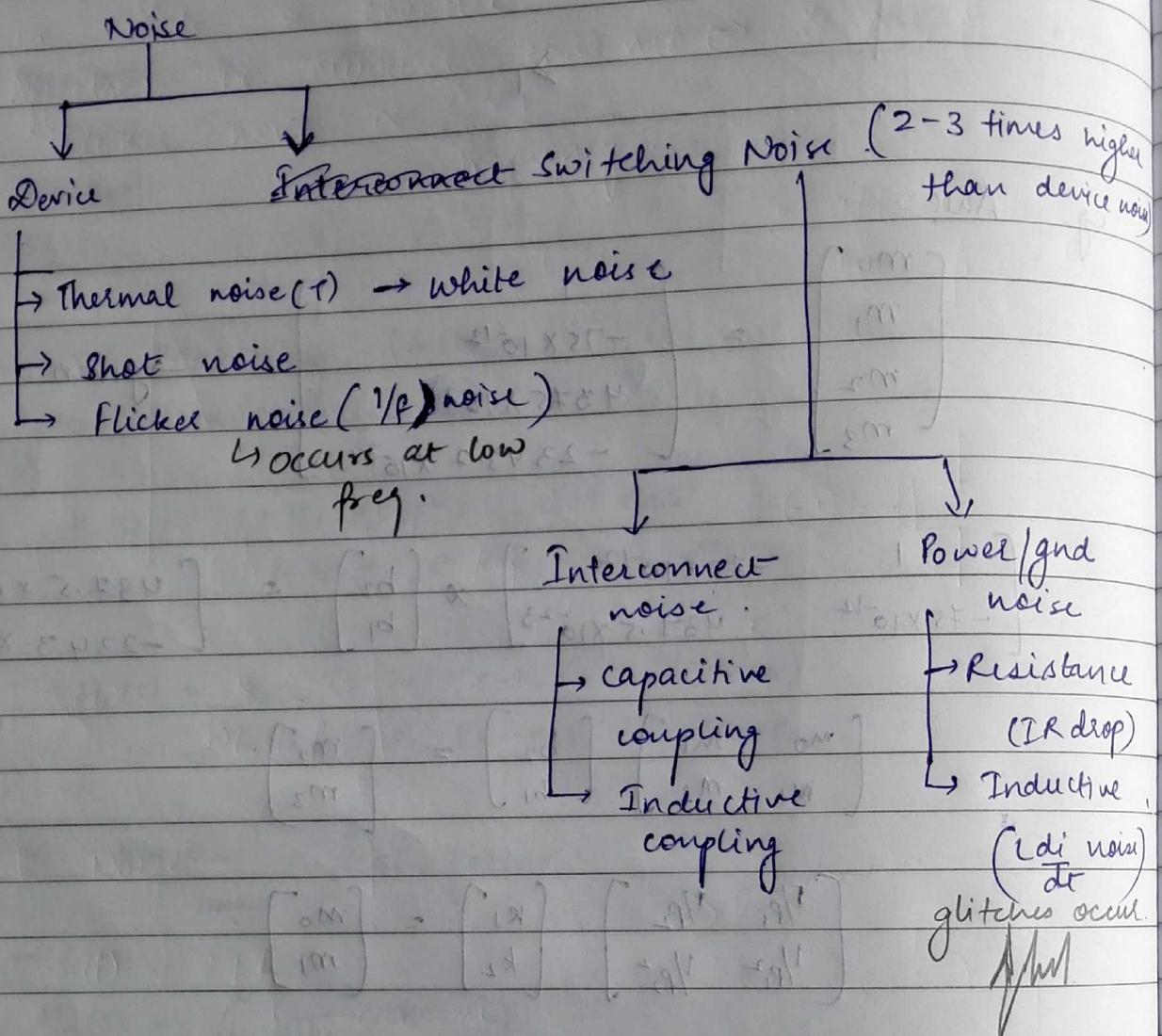
$$\begin{bmatrix} m_0 \\ m_1 \\ m_2 \\ m_3 \end{bmatrix} = \begin{bmatrix} \text{given values} & \rightarrow \text{given values} \\ -75 \times 10^{-12} & \rightarrow \text{given} \\ 437.5 \times 10^{-23} & \rightarrow \text{given} \\ -2343.7 \times 10^{-34} & \end{bmatrix}$$

$$\begin{bmatrix} 1 & -75 \times 10^{-12} \\ -75 \times 10^{-12} & 437.5 \times 10^{-23} \end{bmatrix} \times \begin{bmatrix} b_2 \\ b_1 \end{bmatrix} = \begin{bmatrix} 437.5 \times 10^{-23} \\ -2343.7 \times 10^{-34} \end{bmatrix}$$

$$\begin{bmatrix} m_0 & m_1 \\ m_1 & m_3 \end{bmatrix} \begin{bmatrix} b_2 \\ b_1 \end{bmatrix} = \begin{bmatrix} m_2 \\ m_3 \end{bmatrix}$$

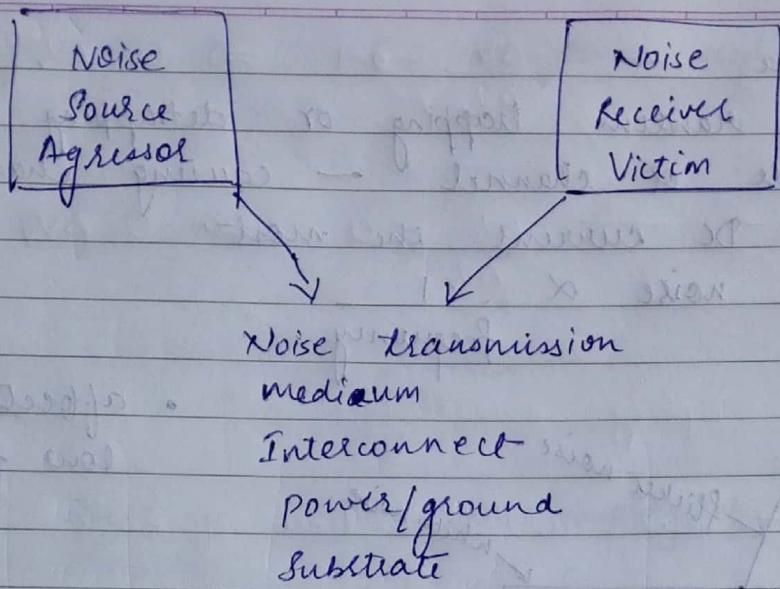
$$\begin{bmatrix} 1/p_1 & 1/p_2 \\ 1/p_2 & 1/p_1^2 \end{bmatrix} \begin{bmatrix} k_1 \\ k_2 \end{bmatrix} = \begin{bmatrix} m_0 \\ m_1 \end{bmatrix}$$

INTERCONNECT COUPLING NOISE



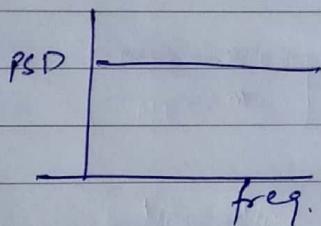
Inductive coupling — inductive effect in ~~interconnects~~
 interconnect causes magnetic field generation
 — causing noise.

- Due to noise
 - (1) interfere with the signal
 - (2) degrade system performance by increasing delay
 - (3) increase power generation



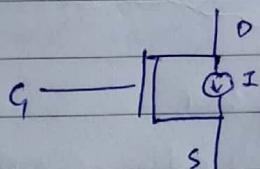
DEVICE NOISE.

(1) Thermal noise / white noise.



- Not frequency selective
- $4kT/R$ dependent

Resistance



$$S(f) = 4kT \frac{1}{R} g_m \rightarrow \text{transconductance of MOS}$$

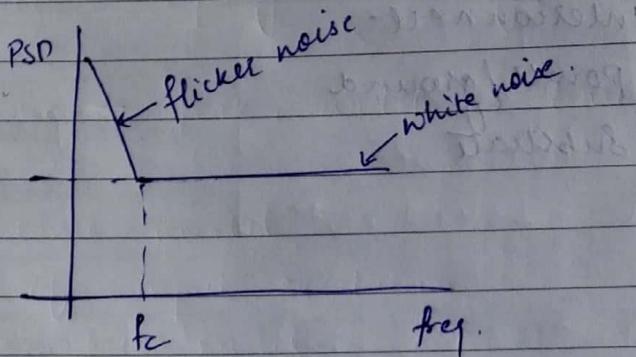
- depends on channel length
- it is a constant

- long channel = $2/3$
- short channel = $2-3$.

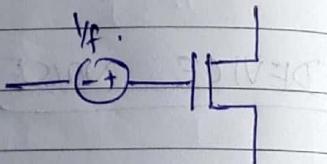
- Thermal noise \propto temp
- Random thermally excited vibrations of charge carriers

(2) Flicker Noise

- Due to random trapping or detrapping of carriers in oxide or channel — causing changes in I
- Affects DC current the most
- Flicker noise $\propto \frac{1}{\text{frequency}}$



- affects only low frequency



$$S_v(f) = \frac{k}{NLCo_x f}$$

(3) Shot Noise

$$S_i(f) = e g I$$

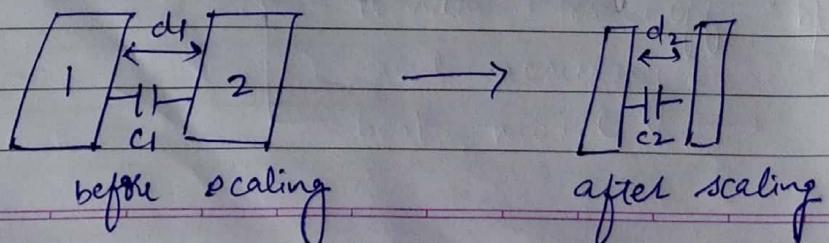
↑ current
charge of e

19.

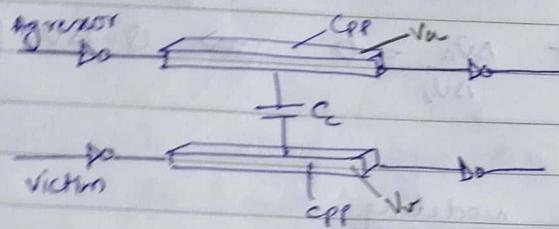
Aspect ratio \uparrow \Rightarrow device size \downarrow \Rightarrow device switching \uparrow

$$AR = \frac{T_{int}}{W_{int}}$$

Cases.



$d_1 > d_2 \Rightarrow C_1 < C_2 \Rightarrow$ device scaling causes coupling capacitance to \uparrow_{SC}



- | Signal | effective coupling cap. | Total cap. |
|---------------------|-------------------------|----------------|
| ① Int 1 switching | C_c | $C_c + C_{pp}$ |
| Int 2 non-switching | | |

$$I_v(t) = C_{pp} \frac{dV_a}{dt} + C_c \frac{d}{dt} (V_v - V_a)$$

- ② Int 1 switching $V_a \approx 0$ $I_v \approx C_{pp} \cdot \frac{dV_v}{dt}$
 Int 2 in phase

- ③ Int 1 switching $V_a \approx 2 \times C_c$ $C_{pp} + 2C_c$
 Int 2 out of phase
 (worst case)

- Signal goes into metastable state when coupling cap. is max. due to crosstalk

- Change of voltage because of charge coupling

$$\delta = \Delta V_v \left[C_c \left(1 - \frac{\Delta V_a}{\Delta V_v} \right) + C_{pp} \right]$$

indicates the amount of coupling

- In case-2 when interconnects switch in phase
 $\frac{\Delta V_a}{\Delta V_v} = 1 \Rightarrow \delta = \Delta V_v C_{pp}$

$$\text{In case - 3} \quad \frac{\Delta V_a}{\Delta V_v} = 0 \Rightarrow Q = \Delta V_v [2C_c + C_{pp}]$$

$$\text{In case - 1} \quad \frac{\Delta V_a}{\Delta V_v} = 0 \Rightarrow Q = \Delta V_v (C_c + C_{pp})$$

4/9

Capacitive coupling modeling.

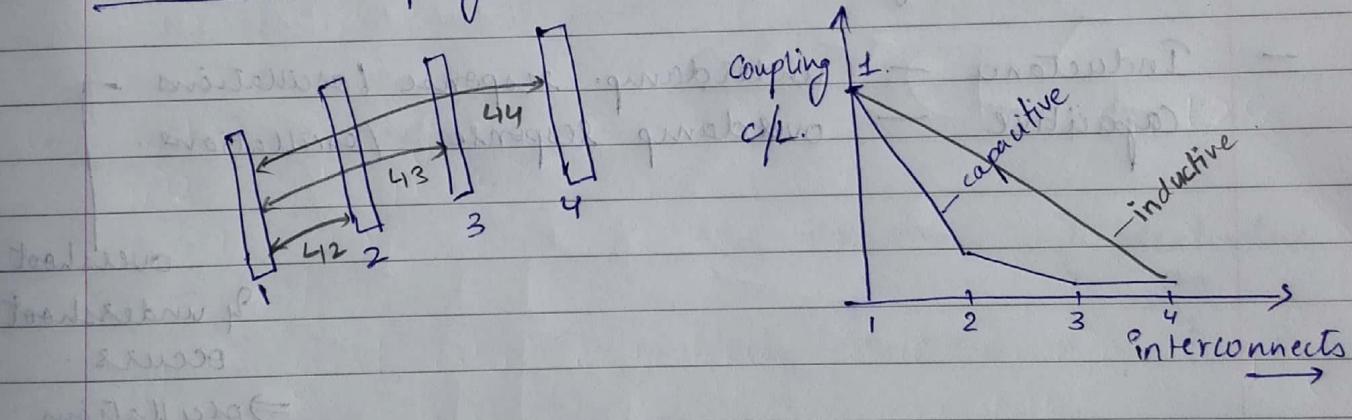
Noise — peak, width & time of noise

- ① Impedance model
- ② Type of input excitation
- ③ Interconnect model
- ④ Location & num number of aggressor

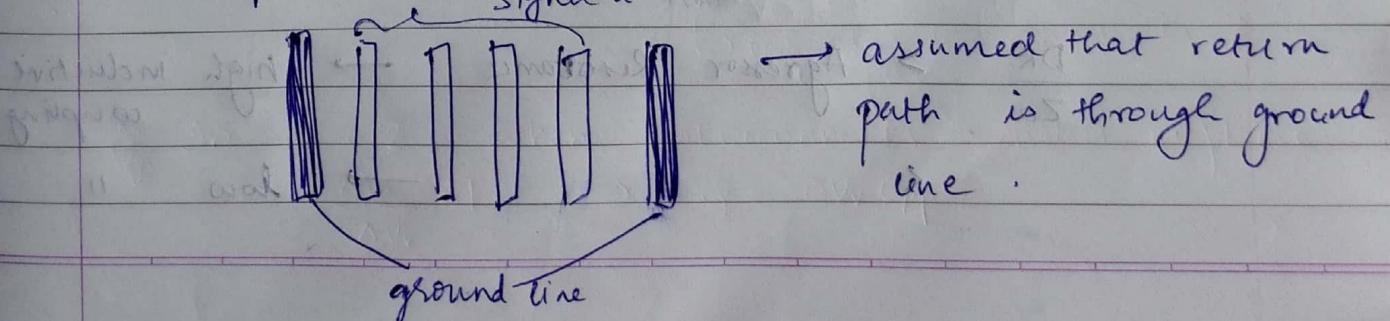
- Driver } — constant \Rightarrow high resistance
- victim } \uparrow (coupling)
- Driver } — small resistance \Rightarrow high coupling noise
- aggressor } (worst case)
- Type of Input Excitation to aggressor
 - ① Exponential $\quad \quad \quad$ computationally complex model
accurate
 - ② Step input $\quad \quad \quad$ computationally simple
 - ③ Saturated ramp $\quad \quad \quad$ error is high
(not accurate)
- Provides tradeoff b/w computations and accuracy
best model

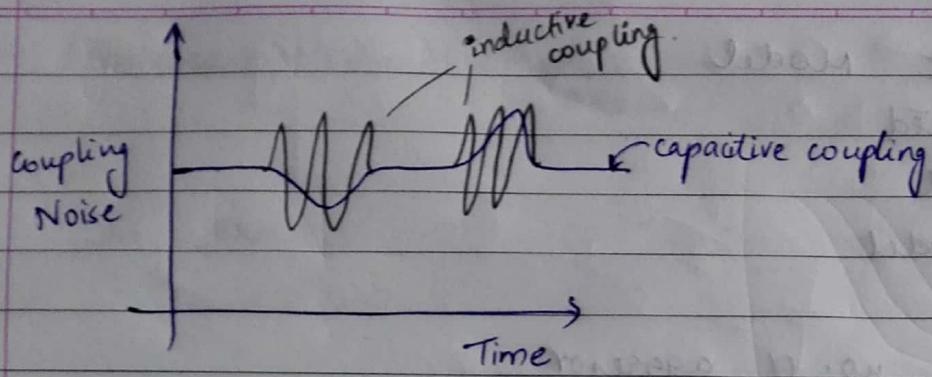
- Interconnect Model
 - distributed
 - lumped
 - Π - model
- Location & no. of aggressor
 - complex case.
 - many aggressor present practically
- Capacitive coupling effects nearby components depending upon distance b/w them
 But inductive coupling decreases very slightly if distance rises \Rightarrow it is more dangerous.

Inductive coupling

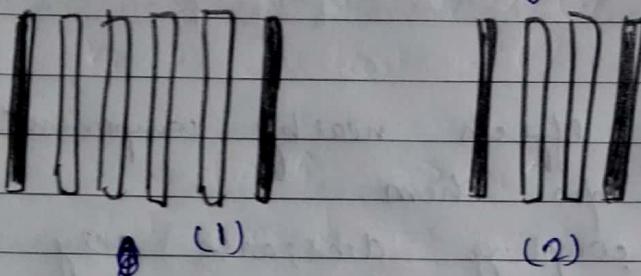


- Exact coupling inductance b/w interconnect cannot be calculated bcoz return path of current is to be known.
- So, partial inductance is predicted.





- Inductance is $\propto \alpha$ length of interconnect.



(1) will have higher inductance than (2) as the loop length of (1) is more than (2).

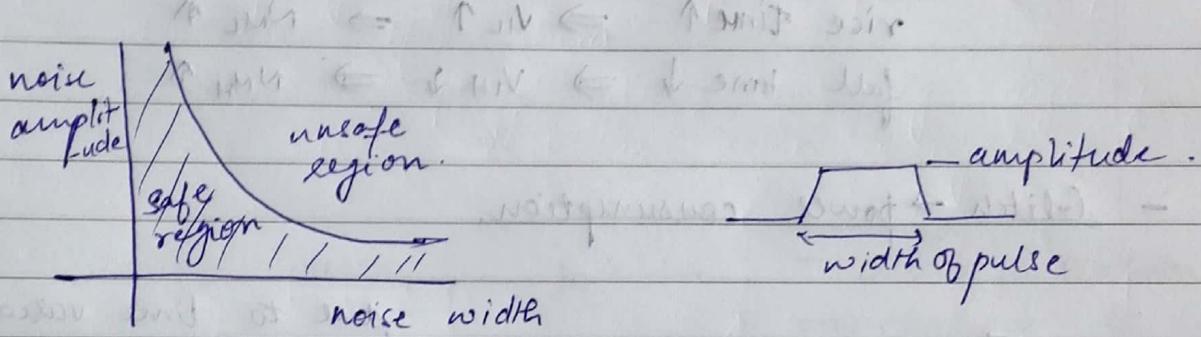
- Inductance — underdamp response / oscillations
- Capacitive — overdamp response / oscillations.

overshoot
if undershoot
occurs.
 \Rightarrow oscillations
generate

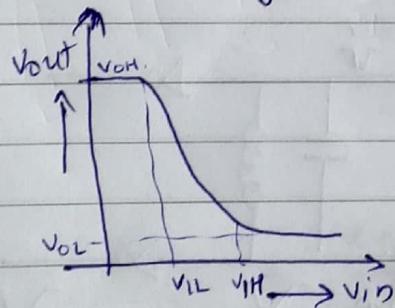
$$\text{Overall Impedance} = \frac{\text{drive resistance}}{\text{characteristic impedance}} = \frac{D.R}{Z_0}$$

$\frac{D.R}{Z_0} > \text{Agressor Resistance} \rightarrow$ high inductive coupling
 ↓ ↑ → low ↑

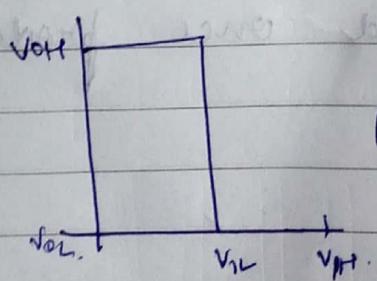
- Static and dynamic noise margin varies due to coupling noise.
- They should be constant.
- Due to noise, logic failure may occur and also glitches are produced \Rightarrow power dissipation \uparrow .
- ~~delay variation~~ delay variation due to crosstalk.
- Function failure: - noise tolerance of gate must be very high so that noise ^{at any node} within gate ~~is~~ does not change logical state of gate and parent gates.



Static Noise Margin

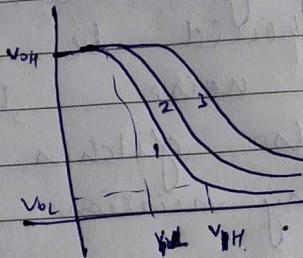
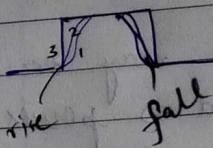


$$\left. \begin{aligned} NM_L &= V_{IL} - V_{OL} \\ NM_H &= V_{OH} - V_{IH} \end{aligned} \right\} \text{ideal value } \frac{V_{DD}}{2}$$



(ideal graph)

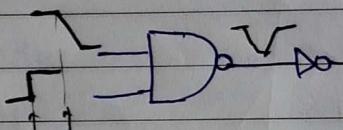
- Dynamic Noise Margin



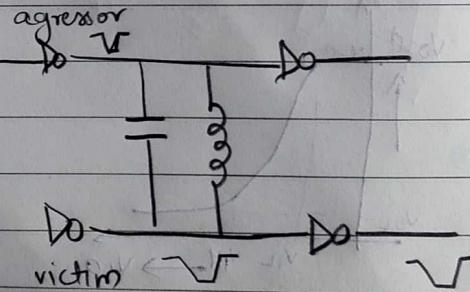
① is faster than ③
 V_{IL} is smallest in ①

rise time $\uparrow \Rightarrow V_{IL} \uparrow \Rightarrow N_{ML} \uparrow$
 fall time $\downarrow \Rightarrow V_{IH} \downarrow \Rightarrow N_{MH} \uparrow$

- Glitch \rightarrow power consumption



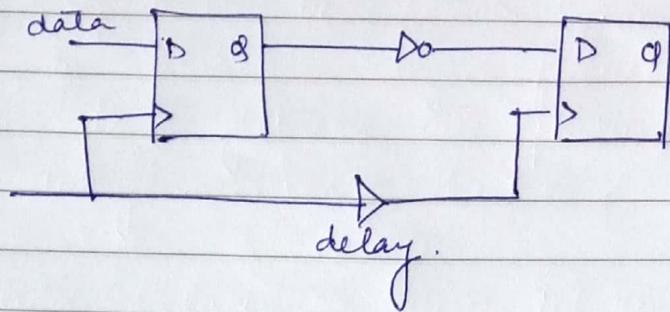
due to time variation
 in switching at i/p
 causes glitches



glitches propagate ahead once produced.

$$P_g = \frac{1}{2} f C V^2$$

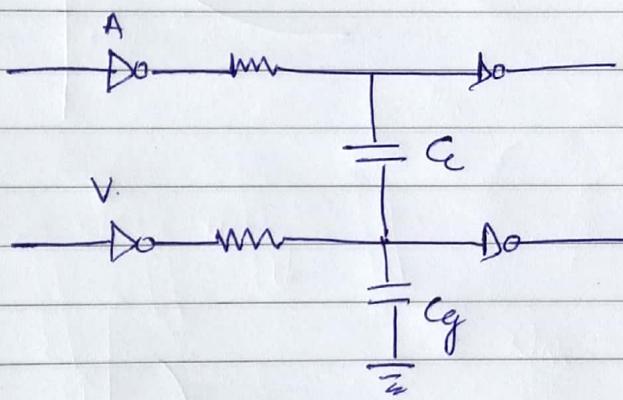
- Delay uncertainty



$$DV = t_{D\max} \text{ (max. delay)} - t_{D\min} \text{ (min. delay)}$$

(OR)

$$DV = \frac{t_{D\max}}{t_{D\min}}$$



- delay variation
may change ~~for~~ for
aggressor &
victim.

- delay changes
along the
interconnect
due to crosstalk.

$$\text{Delay} = C \times (R + R)$$

\uparrow constant.
 \uparrow varies