GLOBAL SIGNALING

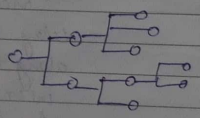
- Interconnect design methodology to meet — latency
  noise
  power dissipation
  physical area
  system reliability ⟶ depends on temp. & power dissipation

- Copper interconnects are used for global int.

⇒ Interconnect Topology Optimization

- wire sizing and shaping
- use of buffer to remove noise

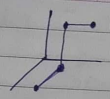
- Constructing Interconnect tree



- Manhattan distance — minimum spanning tree

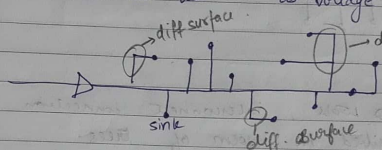
connected at right angles only
not important to connect a node to other node
length of wire reduces.

Graph theory



⊥ connection only permitted

- Via should be less — as voltage drop occurs



- Minimum distance b/w root and ~~stem~~ leaf nodes should be ~~as~~ present so that skew less.
- All clocks arriving at leaf nodes should be synchronized
- $T_{slack} = T_{req} - T_{delay}$

  Delay time should be less than the required time

  $= 4ps - 3ps = 1ps$ ✓

  $= 4pss - 5ps = -1ps.$ ✗

- ΔTree : a tree is formed where, all nodes are drawn with considering manhattan distance
- PTree : all permutation on sink nodes are arranged based on delay or delay area product
- C Tree : Clustred tree

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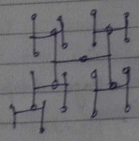
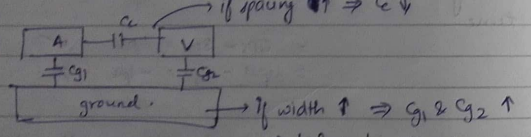
- H-Tree

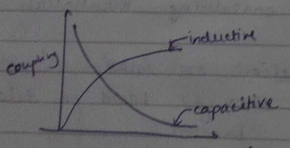


- To use CAD tools, interconnect connection are to be described in form of trees.

- Wire sizing, shaping, spacing helps in
  - ↓ noise — capacitive coupling
    inductive "
  - ↑ speed of signal.

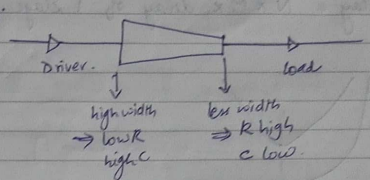
-





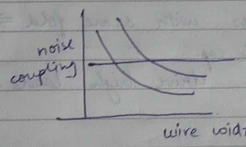
- A width ↑ V width ↓ ⇒ coupling ↓
- A width ↑ V width ↓ & ground wire width ↑
  ⇒ inductive coupling ↓.

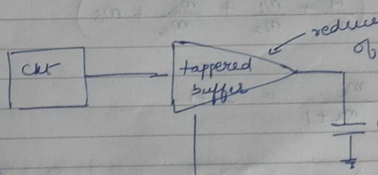
- Shaping.

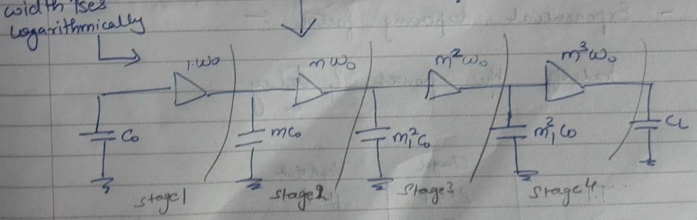


Tappered buffer

product of R and C remains constant
⇒ constant delay provided.





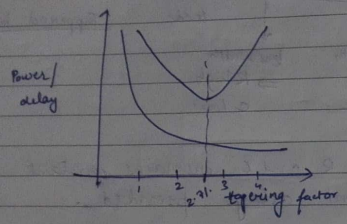


$\frac{C_L}{C_0} = M^N$ → tapering factor

$\frac{C_3}{C_2} = M$ ~~single stage delay~~

$N = \frac{\ln(C_L/C_0)}{\ln M}$ → no. of stages

Total delay = N × M × delay of 1 stage



- As width ↑es ⇒ current ↑es with same fold ⇒ high current is applied to C_L cap.
- Tappering buffer ⟶ used to drive high loads.
  C_g = 50μf, 100μf

$$t_p = t_{p0}\left(\frac{M}{m_1} + \frac{m_1}{m_2} + \frac{m_2}{m_3} + m_3\right)$$

$$F = \frac{m_k}{m_k + 1} = 2.71$$

- Exponential tapering factor :-

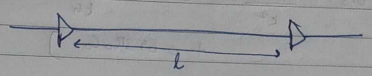
trade off b/w power & delay

	Jager	Veendrick
T.F	2.71	11.5
No. of Stages	5	2
delay	5.5 ns	6.5 ns
Power.	79 mW	16.5 mW

Repeater Insertion in RC Line

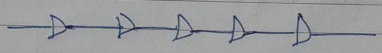
↓

inverting & non-inverting



delay = RCl^2

to reduce this divide into segments



delay = $\frac{RCl^2}{K}$

↓ no. of segments

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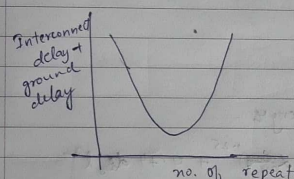
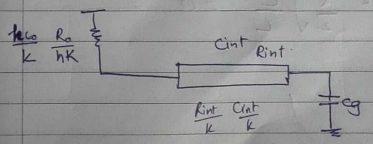
Optimum no. of repeater & size of repeater





$$T_{dRC} = 0.377 R_{int} C_{int} + 0.693 (R_0 C_0 + R_0 C_{int} + R_{int} C_0)$$

↑ 1 segment delay

$$T'_{dRC} = K T_{dRC}$$

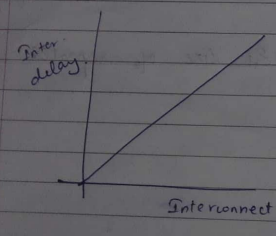
h – size of Repeater

$$k_{opt_{RC}} = \sqrt{\frac{R_{int}\, C_{int}}{2.3\, R_o C_o}}$$

$$T_{delay} = k\left[0.377\frac{R_{int}C_{int}}{k^2} + 0.693\frac{R_o C_{int}}{kh} + 0.693\frac{hR_{int}C_o}{k} + 0.693 R_o C_o\right]$$

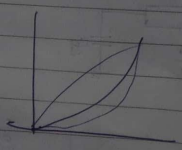
$$h_{opt_{RC}} = \sqrt{\frac{R_o\, C_{int}}{R_{int}\, C_o}}$$

- When freq. rises ⇒ inductive effect is considered.



$$T_{delay} = \sqrt{LC}\; e^{2.9\times(\alpha_{delay})^{1.25}} + 0.74\, d_{delay}\, l^2$$

$$\alpha_{delay} = \frac{R}{2}\sqrt{\frac{C}{L}} = 0.$$



$$k_{opt_{RLC}} = \sqrt{\frac{R_{int}\, C_{int}}{2.3 R_o C_o}} \times k'$$

$$h_{opt_{RLC}} = \sqrt{\frac{R_o\, C_{int}}{C_o\, R_{int}}} \times h'$$

$$k' = \frac{1}{\left[1 + 0.18\left(T_{L/K}\right)^3\right]^{0.3}}$$

$$h' = \frac{1}{\left[1 + 0.16\left(T_{L/R}\right)^3\right]^{0.24}}$$

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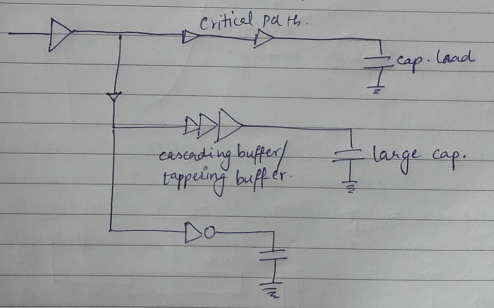
Repeater insertion in tree structure interconnect
- critical path
- large capacitance
- load with negative polarity



Gate Sizing.
- delay
- power dissipation

Signal Routing
- Global Routing
- Detail Routing.

- ↑e speed — at critical path ⇒ ↑se size of gate
  ⇒ power dissipation ↑ses.

  ⇓
  current ↑ses
  ⇓
  cap. charges fast.

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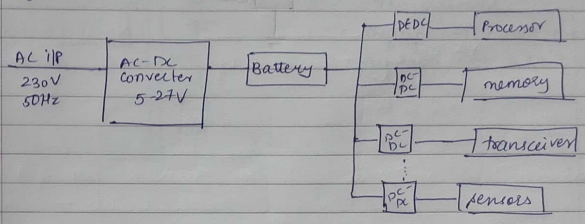
Power Generation

- P.S. scaled down
- ↑sed current load 100A at 1V

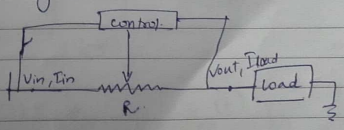
Regulated load voltage — 8.6V to 16.8V dc.

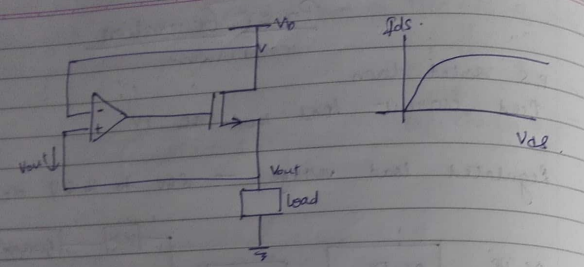


Power management
↓
Performance — speed
noise
power dissipation

Function of Voltage Regulation
isolate — Ic from fluctuations
convert — ↑ or ↓ voltage.
Regulate

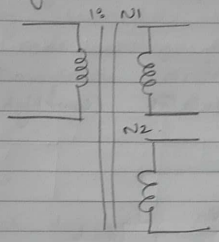
Linear Regulator.





Chapter - 7

- Power regulation & its formulas.
- voltage regulator → Linear, low dropout, switch cap.
- Switching dc-dc converter.

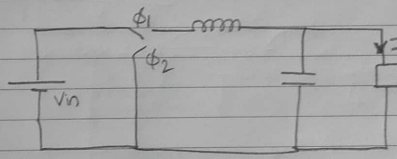


- isolation due to transformer
- Stepup → boost converter
  Stepdown → buck converter

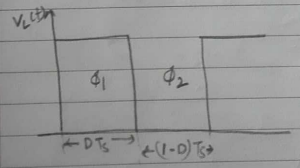
$\eta \propto 100\%$

∴

- Inductor based converter (Buck converter)



frequency of oscillation $(f_0) = \frac{1}{2\pi\sqrt{LC}}$ <<< $f_s = \frac{1}{T_s}$

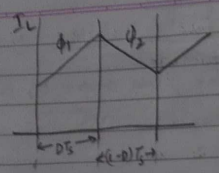


$V_{out} = \frac{1}{T}\int_0^{T_s} V_L(t)\,dt$

↓ voltage delivered to load

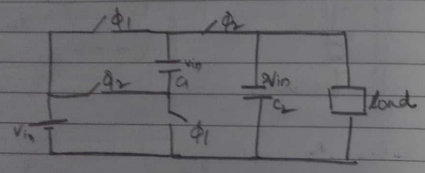
$= DV_{in}$

$V_{out}(s) = V_{out} + V_{ripple}(t)$



→ High power efficiency

- Switch capacitor voltage Regulator (Low + high converter)



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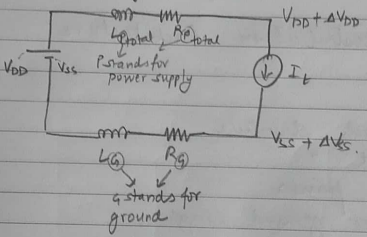
CHAPTER-8 POWER DISTRIBUTION NETWORK

- Functionality should be preserved
- Timing characteristics should satisfy
- Gate oxide reliability should be maintained
- Electromigration should not be violated.

} depends on physical layouts of chips.

— Power delivery & noise



$$\Delta V_{DD} = V_{DD}^{(noisy)} - V_{DD}^{(normal)}$$

$$\Delta V_{SS} = V_{SS}^{(noisy)} - V_{SS}^{(nominal)}$$

$$\Delta V_{DD} = -I(t) R_{P\,total} - L_{P\,total} \frac{dI}{dt}$$

$$\Delta V_{SS} = I(t) R_{g\,total} + L_{g\,total} \frac{dI}{dt}$$

$L\frac{dI}{dt}$ → SSN (simultaneous switching noise)

Page No.

skew → remains constant
jitter → varies

— Effect of Power supply Noise
- Noise margin degradation
- delay uncertainity
- clock jitter skew
- degrade gate oxide

— Scaling of Power Supply Noise
- $I \times R$
- $\frac{dI}{dt} \times L$

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— Power ground distribution System

— On-chip power distribution Architecture

(1) Routed n/w
(2) Irregular mesh structure
(3) Regular grid "
(4) Power ground planes
(5) Cascaded power ground rings
(6) Hybrid power ↓ n/w ground

— Types of On-chip decoupling capacitors

— CAD tools