

Introduction:

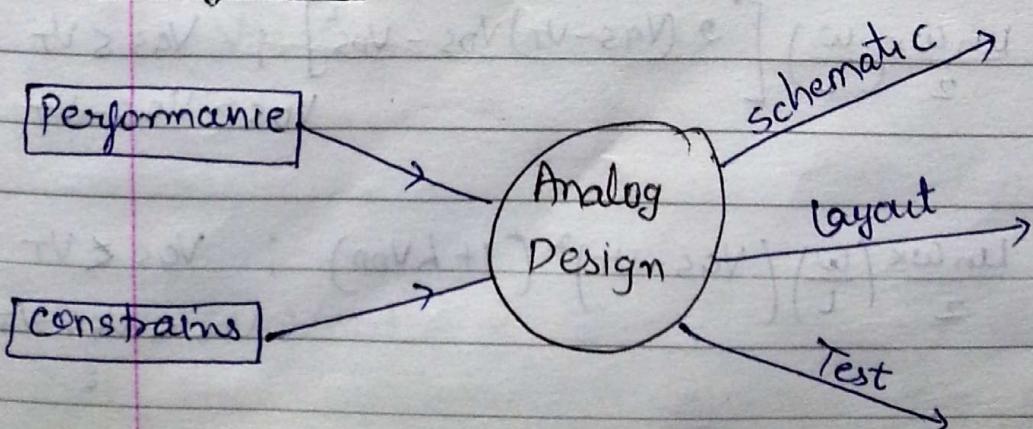
- BJT (high speed current controlled device)
- All real time signals are analog. digital signal will becomes analog due to noise, attenuation and distortion.

Ex: lossy cable
disc drive
wireless receiver
optical receiver

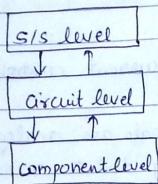
Why Integrated circuit (P)

- larger integration
- lower parasitics
- lower cost
- Higher speed
- larger complexity

Analog design:



levels of abstraction:



n-mos transistor:

$$\text{cut off} \quad I_D = 0 \quad ; \quad V_{GS} < V_T$$

$$\text{linear} \quad I_D = \frac{\mu n C_{ox} (\omega)}{2} \left[2(V_{GS} - V_T) V_{DS} - V_{DS}^2 \right] ; \quad V_{GS} > V_T \\ V_{DS} < V_{GS} - V_T$$

$$\text{saturation} \quad I_D = \frac{\mu n C_{ox} (\omega)}{2} \left[(V_{GS} - V_T)^2 (1 + k V_{DS}) \right] ; \quad V_{GS} \geq V_T \\ V_{DS} > V_{GS} - V_T$$

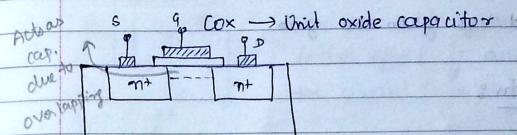
p-mos transistor:

$$\text{cut off} \quad I_D = 0 \quad ; \quad V_{GS} > V_T$$

$$\text{linear} \quad I_D = \frac{\mu n C_{ox} (\omega)}{2} \left[2(V_{GS} - V_T) V_{DS} - V_{DS}^2 \right] ; \quad V_{GS} < V_T \\ V_{DS} > V_{GS} - V_T$$

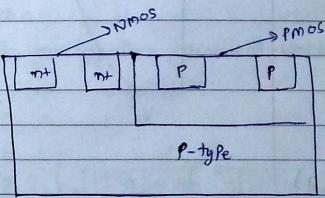
$$\text{saturation} \quad I_D = \frac{\mu n C_{ox} (\omega)}{2} \left[(V_{GS} - V_T)^2 (1 + k V_{DS}) \right] ; \quad V_{GS} \geq V_T \\ V_{DS} < V_{GS} - V_T$$

$$h = \left(\frac{\Delta f}{e} \right) / V_{DS} \text{ sat.}$$



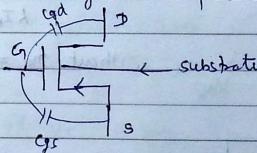
p-type

m-mos transistor



CMOS

All wafers are present in p-type.



$$\Rightarrow I_D = f(V_{GS}, V_{DS}, V_{BS})$$

V_{GS} (from the channel and gives the g_m)

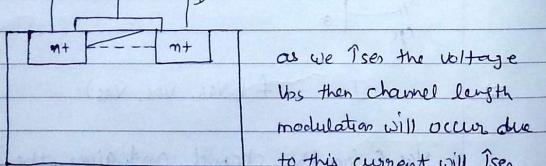
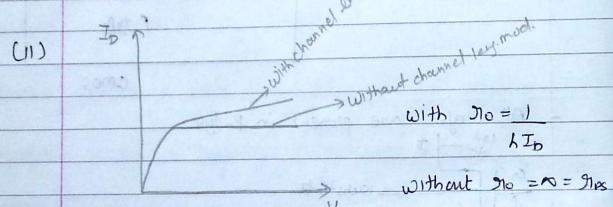
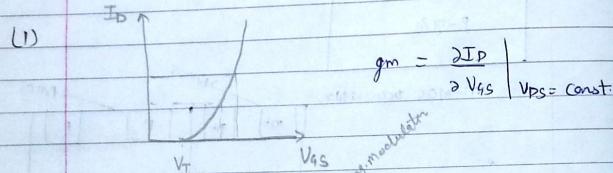
$$g_m = \frac{\partial I_D}{\partial V_{GS}} \Big|_{V_{DS} = \text{const.}}$$

combination of I_D & V_{DS} \rightarrow do the channel length modulation and Resistance is also either T_{ce}

for long channel length, CLM effect is not considered.

or ΔV_{DS}
and V_{DS} gives the gm.

char graphs:

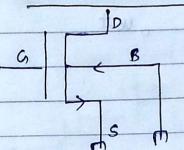


as we \uparrow the voltage V_{DS} then channel length modulation will occur due to this current will \uparrow and channel length \downarrow due to this current will flow through the depletion region.

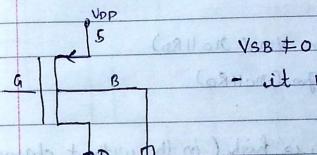
and current will flow through the depletion region.

$$g_{DS} = \frac{1}{r_{DS}} = \frac{\Delta ID}{\Delta VDS} \quad | \quad VDS = \text{const.}$$

III) Substrate bias effect:



when source is grounded then there is no effect of substrate taken in the circuit. ($V_{SB} = 0$)



$V_{SB} \neq 0$ - it modify the threshold voltage

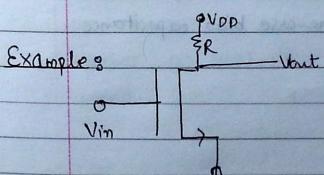
$$V_T = V_{TO} + \gamma \left(\sqrt{2|\phi_F| + V_{SB}} - \sqrt{2|\phi_F|} \right)$$

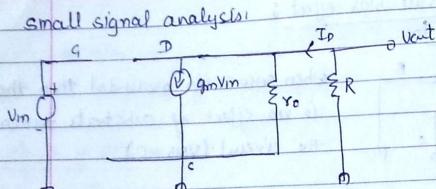
$\phi_F \rightarrow$ surface potential (channel inversion)

$$\begin{cases} \text{when } V_T \downarrow \text{ses} ; \quad V_{SB} < 0 \\ \text{when } V_T \uparrow \text{ses} ; \quad V_{SB} > 0 \end{cases}$$

* if V_T is less, ID is more and speed is also high.

$$g_{mB} = \frac{\Delta ID}{\Delta V_{SB}} \quad | \quad VDS, VGS \rightarrow \text{const.}$$



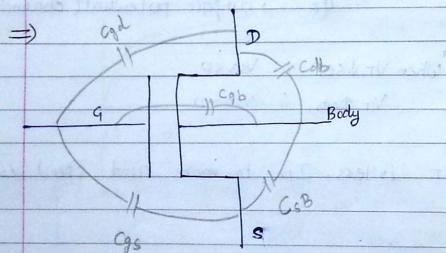


$$V_{out} = -g_m V_{in} (R_o || R_D)$$

$$\underline{V_{out}} = -g_m (g_{ol} R_D)$$

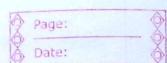
Vin

when g_0 is 1



CSB \rightarrow forward bias capacitance

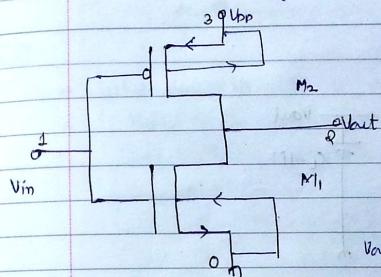
C_{dB} \rightarrow reverse bias capacitance



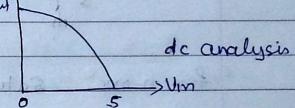
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Spice Code :

- it low level fabrication verification code.



mobility of $e\Theta$ (n-type)
is high as compare to
the mobility of holes in
p-type



code:

☆ ☆

MI 2 1 0 0 n-mos n-mos W=20 L=10
 M2 8 1 3 3 p-mos p-mos W=40 L=10

$$\text{model nmws } V_{TO} = 0.7 \quad KN = 110 \quad \text{Gamma} = 0.4 \quad \lambda = 0.04 \quad \text{PHI} = 0.7$$

model times -0.3 50 0.53 0.95 0.8

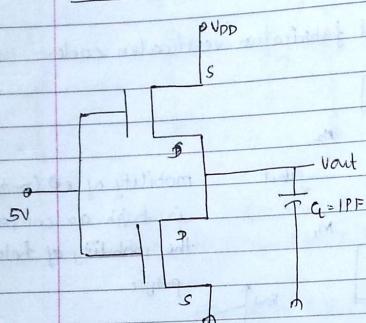
$$V_m = 1.0 \text{ m/s}$$

BC V+ 2 5 3

• DC V(3) 0 5

• sun

Cmos Inverter



for n-mos saturation $V_{out} > V_{in}$
 linear $V_{out} < V_{in}$

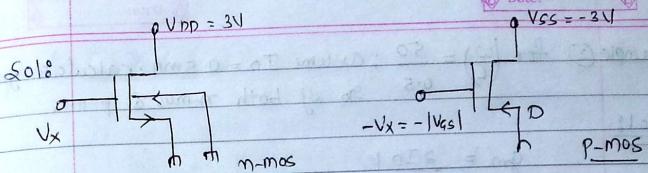
Example 1 for $\frac{W}{L} = \frac{5 \mu}{0.5 \mu}$, plot drain current of nmos & pmos as a func of V_{GS}

where V_{GS} varies from 0 to 3V; $|V_{DS}| = 3V$

level 1 parameter:

nMOS $V_{TO} = 0.7V$ $\Gamma = 0.45$ $\rho H = 0.9$ $K_n = 350 \times 10^{-6}$
 $\lambda_{MOS} = 0.1$

PMOS $V_{TO} = -0.8V$ $\Gamma = 0.4V$ $\rho H = 0.8$ $K_p = 100 \times 10^{-6}$
 $\lambda_{MOS} = 0.2$



$\text{when } V_{GS} = V_x = 0V ; V_{GS} < V_T \rightarrow I_D = 0, \text{ sat cutoff}$

$\text{then } V_{in} < V_{out} \rightarrow \text{saturation} ; V_{GS} = 1V > V_T$

$$I_D = \frac{C_{ox} \mu g \omega}{2(L)} (V_{GS} - V_T)^2 (1 + \lambda V_{DS})$$

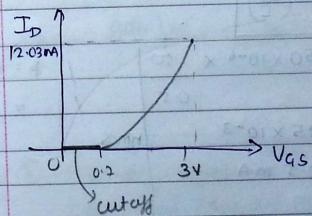
$$= \frac{1}{2} (3.50 \times 10^{-6}) \left(\frac{5}{0.5} \right) [V_{GS} - 0.7]^2 (1 + 0.1 \times 3)$$

$$= 2.02 \text{ mA} (V_{GS} - 0.7)^2$$

when $\rightarrow V_{GS} = 3V$, still device is in saturation

$$= 2.2 (3 - 0.7)^2$$

$$I_D = 1.58 \text{ mA} \quad 1.203 \text{ mA}$$

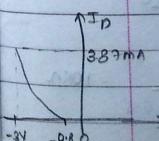


(p-mos) $\text{when } V_{GS} = 0 \rightarrow \text{cutoff} \quad V_{GS} > V_T \rightarrow \text{cutoff}$

$\text{when } V_{GS} = -1, -2, -3V$

$$I_D = \frac{100 \times 10^{-6}}{2} \times (10) [-3 + 0.8]^2 [1 + 0.2 \times 3]$$

$$= 3.87 \text{ mA}$$



Example ② for $\frac{W}{L} = 50$; assume $I_D = 0.5 \text{ mA}$; calculate g_m , g_o of both n-mos & p-mos

Sol:

$$g_m = \frac{\partial I_D}{\partial V_{GS}} \Big|_{V_{DS} = \text{const.}}$$

* g_m is higher in case of device is saturation mode.

$$I_D = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L} \right) (1 + \kappa V_{GS}) (V_{GS} - V_T)^2$$

$$\frac{\partial I_D}{\partial V_{GS}} = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L} \right) (1 + \kappa V_{GS}) 2(V_{GS} - V_T)$$

$$g_m = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L} \right) (1 + \kappa V_{DS}) (V_{GS} - V_T)$$

$$g_m = \sqrt{2 I_D \beta}$$

(Channel length modulation is not considering)

$$\beta = \mu_n C_{ox} \left(\frac{W}{L} \right)$$

$$\text{So, here } \beta = 350 \times 10^{-6} \times \frac{50}{0.5} = 35 \times 10^{-3} \quad \text{nmos}$$

$$\text{& } I_D = 0.5 \text{ mA}$$

$$\text{So } g_m = \sqrt{2 \times 0.5 \times 35 \times 10^{-6}}$$

$$= 5.91 \times 10^{-3}$$

$$g_m = \sqrt{2 \times 0.5 \times 10^{-6}}$$

$$= 10^{-3}$$

$$g_o = \frac{1}{\kappa I_D} = \frac{1}{0.1 \times 5.91} = 20.62$$

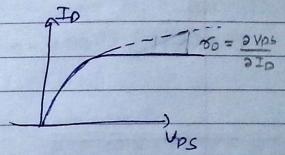
$$g_o = \frac{1}{0.2 \times 0.5} = 10 \text{ k}\Omega$$

proof: $g_o = \frac{1}{\partial I_D / \partial V_{DS}}$

$$\frac{\partial I_D}{\partial V_{DS}} = \frac{\mu_n C_{ox} (W/L)}{2} (V_{GS} - V_T)^2 (1 + \kappa V_{DS})$$

$$= I_D \cdot \kappa$$

$$g_o = \frac{1}{\kappa I_D}$$



$$\text{Intrinsic gain} = g_m g_o$$

$$\text{for nmos: gain} = \frac{5.91 \times 20.62 \times 10^{-3}}{= 118.2 \times 10^3 \times 10^{-3}} = 118.2$$

$$\text{gain}_{p\text{-mos}} = \frac{1 \times 10 \text{ k} \times 10^{-3}}{= 10 \times 10^3 \times 10^{-3}} = 10$$

Example ③ Derive expression for $g_m g_o$ in terms of I_D and (W/L) ?
Plot $g_m g_o$ is a func of L .

Rayav's Book

When $V_{SB} = \pm 1V$; $V_T = 0.78V$

$$V_{GS} = 1.2V > V_T$$

$$\& V_{GS} - V_T = 1.2 - 0.78 = 0.42 < V_{DS} = 2V$$

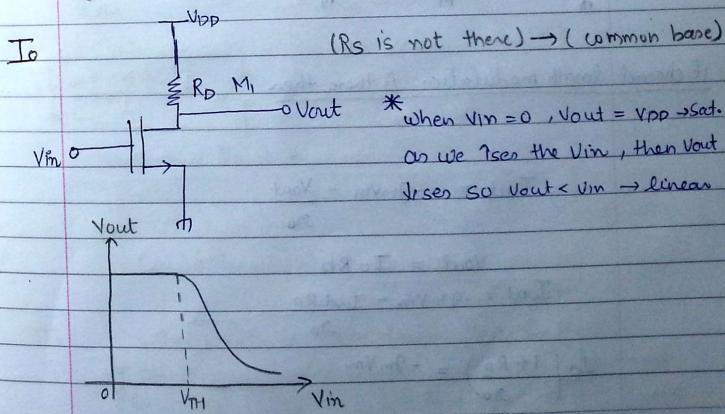
Saturation

$$I_D = \frac{350 \times 10^{-6}}{2} (10) (1.2 - 0.78)^2 (1 + 0.1 \times 2)$$

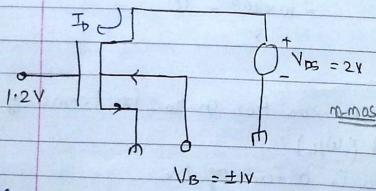
$$= 0.37 \text{ mA}$$

Single stage Amplifier

① Common Source topology:



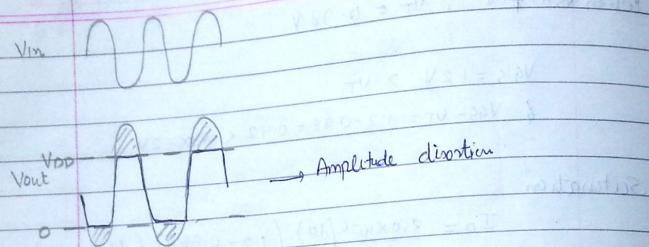
Example ④ If $V_{GS} = 1.2V$, $V_{DS} = 2V$, $V_{SB} = \pm 1V$, $V_{TH0} = 0.6V$, $\gamma = 0.4$, $|2\Phi_F| = 0.7V$, find $I_D = ?$



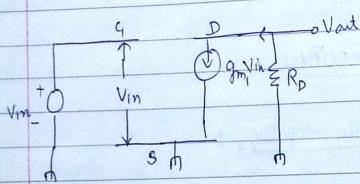
Sol:

$$V_T = V_{TH0} + \gamma (\sqrt{|2\Phi_F| + V_{SB}} - \sqrt{|2\Phi_F|})$$

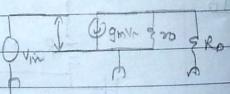
$$= 0.6 + 0.4 (\sqrt{0.7 + 1} - \sqrt{0.7})$$



Small signal analysis:



if channel length modulation is there then



$$I_{out} = -g_m V_{in} - \frac{V_{out}}{R_D}$$

$$V_{out} = I_{out} R_D$$

$$I_{out} = -g_m V_{in} - \frac{I_{out} R_D}{R_D}$$

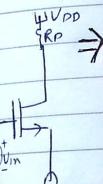
$$I_{out} \left(1 + \frac{R_D}{R_D} \right) = -g_m V_{in}$$

$$G_m = \frac{I_{out}}{V_{in}} = -g_m \cdot \frac{R_D}{g_m R_D + R_D}$$

$$V_{out} = G_m \cdot R_D$$

$$\boxed{V_{out} = -g_m \frac{R_D}{(g_m + R_D)} \approx -g_m (g_m + R_D)}$$

- if we want to work device as amplifier, then our device M1 must be in saturation. $V_{out} > V_{in}$ because g_m is very high in saturation mode.



$$V_{out} = V_{DD} - I_{out} R_D$$

$$= V_{DD} - \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (1 + \lambda V_{DS}) (V_{GS} - V_T)^2 \cdot R_D$$

(device in saturation)

$$V_{GS} = V_{in}$$

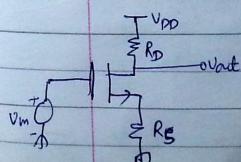
$$\frac{\partial V_{out}}{\partial V_{in}} = \frac{-1}{2} \mu_n C_{ox} \frac{W}{L} \cdot R_D (1 + \lambda V_{DS}) \cdot 2 (V_{in} - V_T)$$

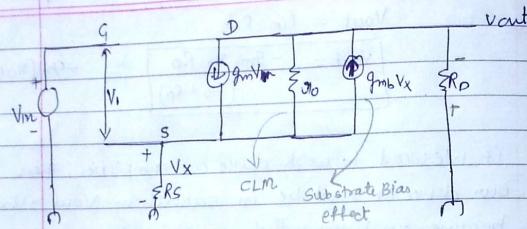
$$= -R_D g_m (1 + \lambda V_{DS})$$

$$R_{out} = R_D \parallel \infty$$

$$\infty = \frac{1}{h I_D}$$

II: when (R_S) is considered (neg feedback)





$$V_i = V_{in} - I_{out} R_s$$

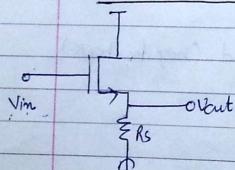
$$I_{out} = g_m V_i - g_{mb} V_x - \frac{I_{out} R_s}{g_{lo}}$$

$$I_{out} = g_m (V_{in} - I_{out} R_s) - g_{mb} I_{out} R_s - \frac{I_{out} R_s}{g_{lo}}$$

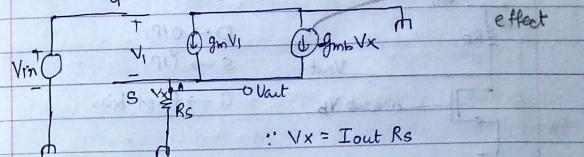
$$I_{out} \left[1 + R_s + g_{mb} R_s + g_m R_s \right] = g_m V_{in}$$

$$G_m = \frac{g_m R_s}{1 + R_s + g_{mb} R_s + g_m R_s}$$

② Source follower: (Common Drain)



Small signal analysis:



$$V_i = V_{in} - V_x$$

$$g_m V_{in} - g_{mb} V_x - g_m V_x$$

$$A_v = \frac{g_m R_s}{1 + (g_m + g_{mb}) R_s}$$

$$g_m V_{in} R_s = V_{out}$$

$$\text{at node A} \quad g_m V_i - g_{mb} V_x - \frac{V_{out}}{R_s} = 0$$

$$g_m V_{in} - g_m V_x - g_{mb} V_x - \frac{V_{out}}{R_s} = 0$$

$$V_x = V_{out}$$

$$g_m V_{in} = (g_m + g_{mb} + \frac{1}{R_s}) V_{out}$$

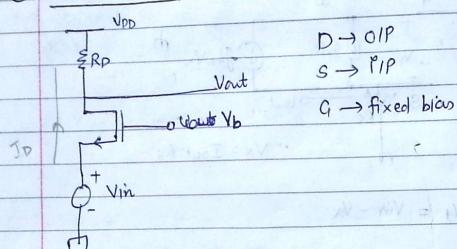
$$\frac{g_m R_s}{(g_m + g_{mb}) R_s + 1} = \frac{V_{out}}{V_{in}} = A_v$$

$$\text{When } g_m \gg g_{mb} \gg 1$$

then $A_v \approx 1$, source follower follows the inputs.

Voltage Buffer \rightarrow application (current amplified, $V_{out} = V_{in}$)

③ Common Gate :



Device must be in saturation region:

$$V_{out} = V_{DD} - I_D R_D$$

$$= V_{DD} - \frac{1}{2} m \cosh \left(\frac{V_b - V_{in} - V_{th}}{L} \right) (V_b - V_{in} - V_{th})^2 \cdot R_D$$

$$\therefore V_{GS} = V_b - V_{in}$$

$$\frac{\partial V_{out}}{\partial V_{in}} = \frac{(-1 + \frac{1}{2} m \cosh(\frac{V_b - V_{in} - V_{th}}{L}))}{2} R_D (-1 - \frac{\partial V_{th}}{\partial V_{in}})$$

$$= \frac{\partial V_{th}}{\partial V_{in}}$$

Due to substrate bias effect b/c S is not grounded

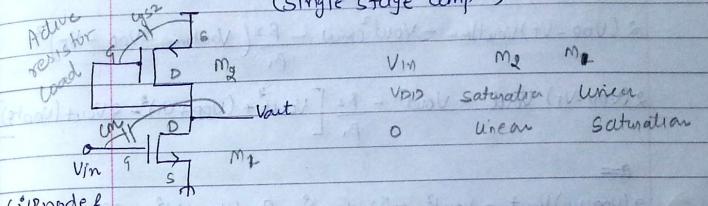
$$= \frac{1}{2} m \cosh \left(\frac{V_b - V_{in} - V_{th}}{L} \right) (1 + \frac{1}{2} m) R_D$$

$$= g_m (1 + \frac{1}{2} m)$$

- it can also used as voltage amplifier

Ch-5 (16B Page No) (E-book)

① Common Source with different load (Single stage amp)



O/P node are (IP node & Miller capacitor) $V_{GS} = V_{DS}$

$$V_{DS} = V_{DD}$$

- When in saturation then Drain & source V_{th} , voltage drop is occur. But in linear, drop = 0.

dc analysis:

$$\text{When } V_{in} = 0; \quad V_{out} = V_{DD} - V_{TP}$$

$$V_{in} = V_{DD}; \quad V_{out} = 0$$

$$V_{out} \text{ min} =$$

$$I_{D1} = I_{D2} \quad V_{GS} = V_{DD}$$

$$I_{D1} = \frac{B_1}{2} \left[2(V_{DD} - V_{Tn})V_{out} - V_{out}^2 \right] \quad (\text{min})$$

$$I_{D2} = \frac{B_2}{2} \left(\frac{V_{out}}{V_{DD} - V_{TP}} \right)^2$$

$$- 2(V_{DD} - V_{Tn})V_{out} \text{ min} + V_{out}^2 \text{ min} + \frac{B_2}{2} \left(\frac{V_{out}}{V_{DD} - V_{TP}} \right)^2 = 0$$

$$V_{out} \text{ min} = \frac{2(V_{DD} - V_{Tn}) \pm \sqrt{4(V_{DD} - V_{Tn})^2 - 4 \frac{B_2}{P_1} (V_{DD} + V_{TP})^2}}{2 \frac{B_2}{P_1}}$$

$$V_{out, min} = (V_{DD} - V_{TN}) \pm \sqrt{(V_{DD} - V_{TP})^2 - \frac{\beta_2}{\beta_1} (V_{DD} + V_{TP})^2}$$

$$2(V_{DD} - V_T)V_{out, min} - V_{out, min}^2 - \frac{\beta_2}{\beta_1} (V_{out, min} - V_{DD} - V_T)^2$$

$$2(V_{DD} - V_T) V_{out} - V_{out}^2 - \frac{\beta_2}{\beta_1} \left[V_{out} + (V_{DD} + V_T)^2 - 2V_{out}(V_{DD}) \right]$$

$$2(V_{D0}-V_r)V_{out} - V_{out}^2 - \frac{\beta_2}{\beta_1} V_{out}^2 - \frac{\beta_2}{\beta_1} (V_{D0}+V_r)^2 + \frac{2\beta_2 V_{out}}{\beta_1} = 0$$

$$\left(\frac{1+\beta_2}{\beta_1} \right) V_{out}^2 - 2 V_{out} \left[(NDD - VT) + \frac{\beta_2 (V_{DD} + VT)}{\beta_1} \right] + \frac{\beta_2 (V_{DD} + VT)^2}{\beta_1} = 0$$

$$V_{out} = \frac{Q}{2C} \left[(V_{DD} - V_T) + B_2 I_B (V_{DD} + V_T) \right] \pm \left[\left(\frac{1}{2} \right)^2 - 4 (1 + B_2 I_B) C \right]$$

$$V_{out/min} = (V_{DD} - V_T) - (V_{DD} - V_T) \sqrt{1 + \beta_2 / \beta_1}$$

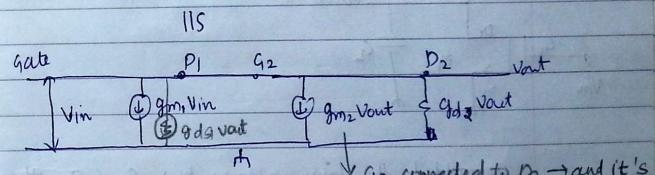
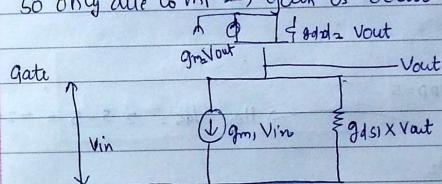
from the dc analysis we are carried out the

Voltage swing is poor at the O/P side.

Small gain & BCW

$$B_{\text{W}0} = \frac{1}{R_{\text{out}} C_{\text{out}}}$$

- V_{in} is only connected to m_1 , $M_2 \rightarrow$ load
so only due to $m_1 \rightarrow$ gain is occurs.



$$g_m V_{in} + g_{ds1} V_{out} + g_{m2} V_{out} + g_{ds2} V_{out} = 0$$

$$\frac{V_{out}}{V_{in}} = \frac{-g_{m1}}{g_{ds1} + g_{ds2} + g_{m2}} \stackrel{\text{Circuit}}{=} C_m R_{out}$$

$$R_{out} = \frac{1}{g_{d1} + g_{d2} + g_{m2}}$$

due to Miller effect BW is \downarrow sen.

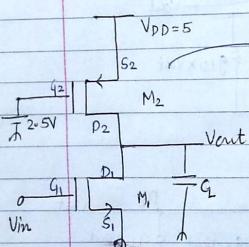
$$C_{out} = C_{gd1} + C_{gs2} + C_{db1} + C_{db2} + C_L$$

\downarrow \downarrow \downarrow \downarrow

C_{gd1} is connected to G_0 , to C_L

Qm bcoz D_2 is shorted to G_2 to C_{GS2} is in pic

② \Rightarrow



we added the bias voltage b/w g_2 & D_2 then

$$V_{out})_{max.} = V_{DD}$$

DC Analysis:

- When $V_m = 0$; $M_1 \rightarrow$ saturation
 $M_2 \rightarrow$ linear

its holding in linear region, so M_2 acts as the voltage series resistor.

- When $V_{IN} = V_{DD}$; $M_1 \rightarrow$ linear
 $M_2 \rightarrow$ saturation because

Page: _____
Date: 20-Jan

$V_{GS} = -2.5$, & we assumed $V_{out}^D = 1V \Rightarrow V_{DS} = 1 - 5 = -4V$
 $V_{GS} > V_{DS}$ ($V_{in} > V_{out}$)
then device in saturation region

$$V_{out})_{min} =$$

$$I_{D1} = \frac{\beta_1}{2} \left[2(V_{DD} - V_T) V_{out_{max}} - V_{out}^2 \right]$$

$$I_{D2} = \frac{\beta_2}{2} \left[(Vg - V_{DD} - V_T)^2 \right]$$

$$\frac{I_{D1}}{I_{D2}} = \frac{V_{out} - (V_{DD} - V_T)}{(Nq - V_{DD} - V_T)^2}$$

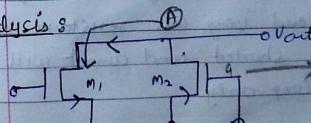
$$V_{out})_{\min} = \frac{-b \pm \sqrt{b^2 - 4ac}}{2a}$$

$$= \frac{2(v_{BD} - v_t) \pm \sqrt{4(v_{BD} - v_t)^2 - 4(v_g - v_{BD})^2}}{2}$$

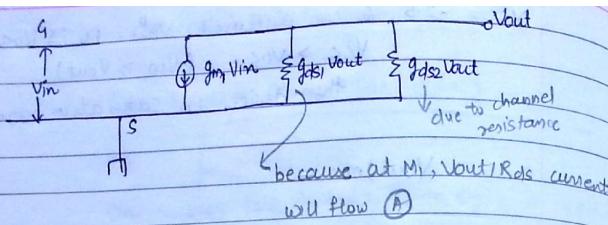
$$= (V_{DD} - V_T) \pm \sqrt{(V_{DD} - V_T)^2 - (V_G - V_{DD} - V_T)^2 \frac{\beta_2}{\beta_1}}$$

$$V_{out} = \frac{(V_{DD} - V_T)}{R_{in}} \left[1 - \frac{\left\{ 1 - \frac{(V_G - V_{DD} - V_T)^2 B_2}{(V_{DD} - V_T)^2 B_1} \right\}^{1/2}}{1} \right]$$

AC analysis :



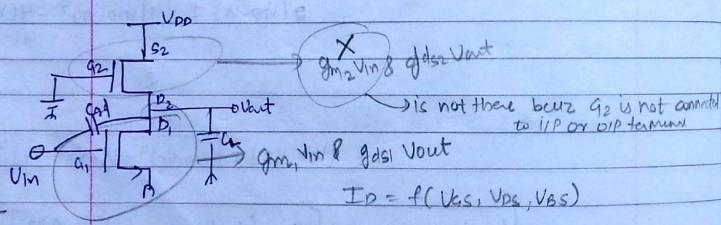
it does not get
any Ti^3 or Cl^-
(Ti^3 & Cl^- make one not
connected to cage), so
 Ti^3 behaved as R and
there is many
pm]



$$g_m1 V_{in} + g_{ds1} V_{out} + g_{ds2} V_{out} = 0$$

$$V_{out} = \frac{-g_m1}{(g_{ds1} + g_{ds2})}$$

$$R_{out} = \frac{1}{g_{ds1} + g_{ds2}}$$

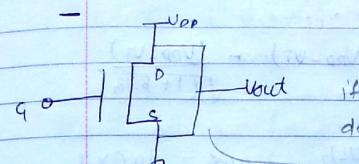


- Miller capacitor \rightarrow using the Bandwidth.
- C_{gd} consider in the ac analysis, at high freq. C_{gd} offered very less resistance due to this G & D are shorted and current will through in this loop only

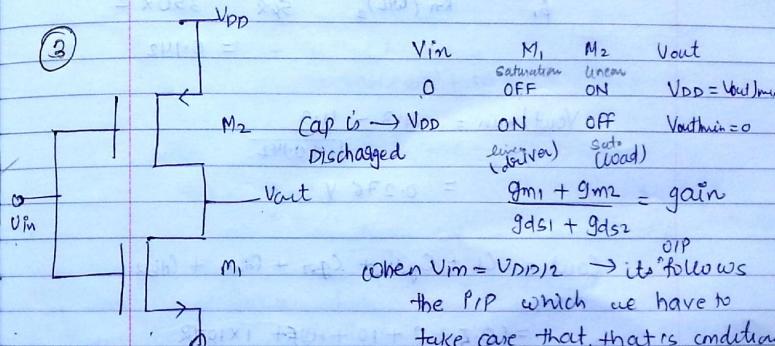
$$C_{out} = C_{gd1} + C_{db1} + C_{db2} + C_{gd2} + C_L$$

Main load $\rightarrow P_F$

interconnection load $\rightarrow f_F$



③



25 - Jan

will flow and losses will occurs

Example: Calculate the o/p swing limits for $V_{DD} = 5V$ for diode control PMOS load inverter:

$$(\frac{V_o}{V_{DD}})_1 = \frac{0.5}{1} ; \quad (\frac{V_o}{V_{DD}})_2 = \frac{1}{1} ; \quad C_{gd1} = 0.5 \text{ fF} , \quad C_{gd2} = 0.5 \text{ fF} ;$$

$$C_{bd1} = C_{bd2} = 10 \text{ fF} ; \quad C_L = 1 \text{ pF} ; \quad I_{D1} = I_{D2} = 100 \text{ mA}$$

Date: 25-Jan

Q10

$$\text{① CKT. } V_{out(\max)} = V_{DD} - V_{TP} \\ = 5 - 0.3 \\ = 4.3 \text{ V}$$

$$V_{out(\min)} = (V_{DD} - V_T) - \frac{(V_{DD} - V_T)}{\sqrt{1 + \beta_2/\beta_1}}$$

$$\frac{\beta_2}{\beta_1} = \frac{k_p(w/L)_2}{k_n(w/L)_1} = \frac{110 \times 100 \times 1}{50 \times 350 \times 2} \\ = 0.142$$

$$V_{out(\min)} = \frac{4.3 - 4.3}{\sqrt{1 + 0.142}} \\ = 0.276 \text{ V}$$

$$C_{out} = C_L + C_{gds1} + C_{gds2} + C_{db1} + C_{db2} \\ = (0.8 + 2 + 10 + 10) \text{ fF} + 1 \times 10^{-12} \\ = 22.5 \times 10^{-15} + 10^{-12} \\ = 1.02 \text{ pF}$$

$$R_{out} = \frac{1}{g_{me} + g_{ds1} + g_{ds2}}$$

$$V_{out} = -g_{m1} \cdot R_{out}$$

$$g_{m1} = \sqrt{2 I_D \beta} \\ = \sqrt{2 \times 100 \times 10^{-6} \times 350 \times 10^{-6} \times 2} \\ = 374 \times 10^{-3}$$

$$g_{m2} = \sqrt{2 \times 100 \times 10^{-6} \times 100 \times 10^{-6} \times 1} \\ = 141 \times 10^{-3}$$

*
$$\begin{cases} g_{ds1} = h_n \times 100 \text{ mA} \\ g_{ds2} = h_p \times 100 \text{ mA} \end{cases} = 0.1 \times 100 = 10 \text{ k} \Omega$$

$$S_o; R_{out} = \frac{1}{0.141 \times 10^{-3} + 10 \times 10^{-6} + 20 \times 10^{-6}}$$

$$= 5.84 \text{ k} \Omega$$

$$\text{then } g_{gain} = -374 \times 10^{-3} \times 5.84 \times 10^3 \\ = -2.18$$

$$BW = \frac{1}{2\pi R_{out} C_{out}}$$

$$= \frac{1}{2 \times 3.14 \times 5.84 \times 1.02 \times 10^{-12} \times 10^3}$$

$$= 26.71 \text{ MHz}$$

③ CMOS Inverter:

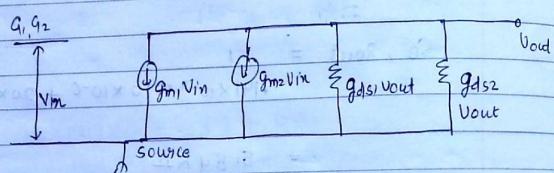
$$V_{out, max} = V_{DD}$$

$$V_{out, min} = 0$$

$$\frac{V_{out}}{V_{in}} = \frac{-(g_{m1} + g_{m2})}{g_{d1} + g_{d2}}$$

$$R_{out} = g_{d1} + g_{d2}$$

$$C_{out} = C_{gd1} + C_{gd2} + C_{bd1} + C_{bd2} + C_L$$



Width of nmos = (2-2.5) width of Pmos

bcz mobility of e^- > mobility of holes

and in CMOS both currents due to holes & e^- are same
so to equate we have to take care
that $W_1 = 2-2.5 W_2$

Example In CMOS ③

$$V_{DD} = 5V; I_{D1} = I_{D2} = 300 \text{ mA}, (W/L)_1 = 1$$

$$(W/L)_2 = 4$$

$$g_{m1} = \sqrt{2 I_D B_1} = \sqrt{2 \times 350 \times 300 \times 10^{-6} \times 10} = 458.25 \times 10^{-6}$$

$$g_{m2} = \sqrt{2 I_D B_2} = \sqrt{2 \times 100 \times 300 \times 10^{-6} \times 2} = 346.41 \times 10^{-6}$$

$$g_{d1} = h_N \times 300 \text{ MA} = 0.1 \times 300 = 30 \text{ M}$$

$$g_{d2} = h_P \times 300 \text{ MA} = 0.2 \times 300 = 60 \text{ M}$$

$$\text{then gain} = - \frac{(458.25 + 346.41)}{30 + 60} = -8.94$$

$$BW = \frac{1}{2\pi R_{out} C_{out}}$$

$$C_{out} = 1.02 \text{ PF}$$

$$\Rightarrow R_{out} = \frac{1}{(30 + 60 + 346.41) \times 10^{-6}} = 9.2 \text{ k}\Omega$$

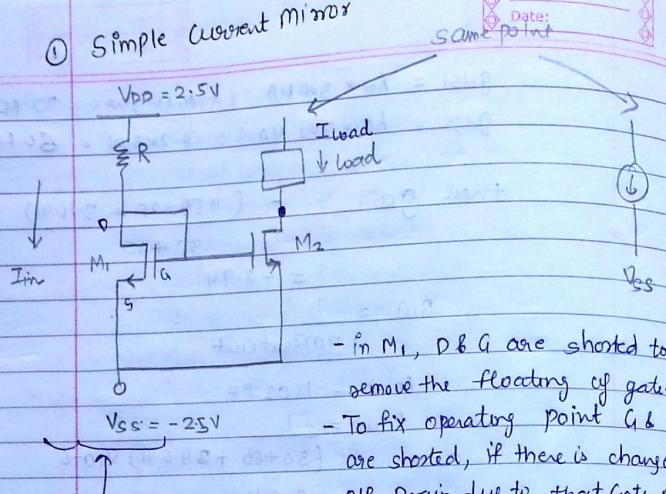
$$BW = 70.92 \text{ rad/s}$$

27-Jan

Current Mirror

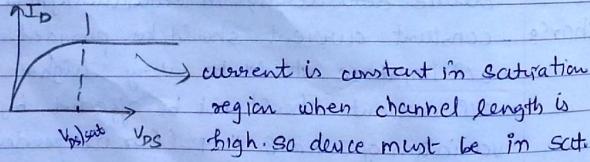
- Constant current source & sink
- device also always in saturation (g_m is higher)
- charge - constant current should be provided.
- output impedance should be very high.
- output current should not be affected by the variation of V_{DD} & temp (or independent to V_{DD} bias voltage & temp)
- current generated / current used with isolation.
- M_1 & M_2 must be biased in saturation bcz of const. current

① Simple Current Mirror



$$I_{in} = \frac{V_{DD} - V_{GS1} + V_{SS1}}{R}$$

$$\beta = k_n (w/L) = n \mu C_o x (w/L)$$



$$I_{D1} = k_n (w/L_1) [V_{GS1} - V_T]^2$$

$$I_{D2} = k_n (w/L_2) [V_{GS2} - V_T]^2$$

V_T is same as M_1 & M_2

Chp-20 "Current source & sinks" part III CMOS Analog circuits

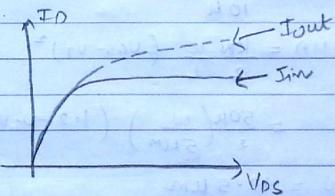
$$\frac{I_{out}}{I_{in}} = \frac{I_{D2}}{I_{D1}} = \frac{(w/L)_2}{(w/L)_1}$$

same technology is used in M_1 & M_2 : $L_1 = L_2$

$$\frac{I_{out}}{I_{in}} = \frac{w_2}{w_1} \quad \text{--- (1)}$$

$V_{DS} > V_{DS1\text{sat}}$ → for getting the current constant and eqn (1) is only applicable when $V_{DS} \geq V_{DS1\text{sat}}$

bcz of channel length modulation we don't get the o/p charc as we want



$$\text{O/P Impedance } Z_{in} = 1/k_n I_{out} \\ = 1/0.04 (10mA) \\ = 2.50 M\Omega$$

O/P impedance is also very poor and channel length is 1 μm which is very less bcz of this channel length modulation is there. So we don't get $I_{out} \rightarrow \text{constant}$.

So if uses the channel length $L = 5 \mu\text{m}$ then area is also $5 \mu\text{m}^2$, which is not reliable. general design rule is set to the length of most used in analog app. to two to five times the min.



drawn gate length.

Example 8 Design a current sink $V_{DD} = -V_{SS} = 2.5V$ to sink a current of $10mA$. Estimate the min. voltage across the current source and O/P resistance.

Sol: let assume $V_{GS} = \frac{V_{DD}}{2} = 1.25V$

$$R = \frac{V_{DD} - V_{GS} + V_T}{I}$$

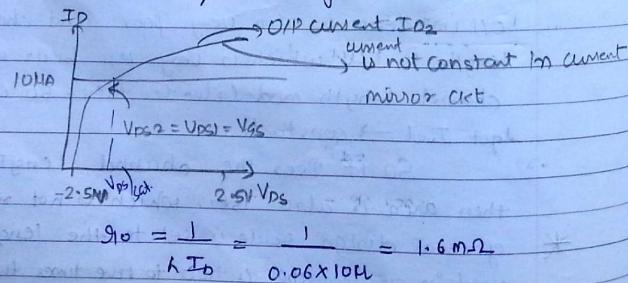
$$= \frac{2.5 - 1.25 + 0.5}{10 \mu A} = 380 k\Omega$$

$$I_{D2} = 10mA = \frac{K_N W}{2L} (V_{GS} - V_T)^2$$

$$= \frac{50 \mu A}{2} \left(\frac{W}{5 \mu m} \right) (1.25 - 0.5)^2$$

$$W = 12.5 \mu m$$

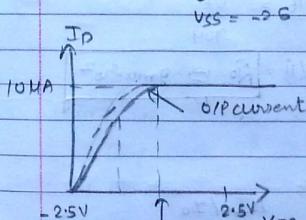
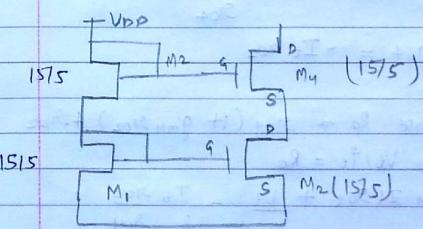
technology \rightarrow diff' doping profile gives diff. mobility of e⁺ & holes \rightarrow so we get diff' value of K_P & K_N .



g_o is very less in current mirror source, so we are using Cascode connection.

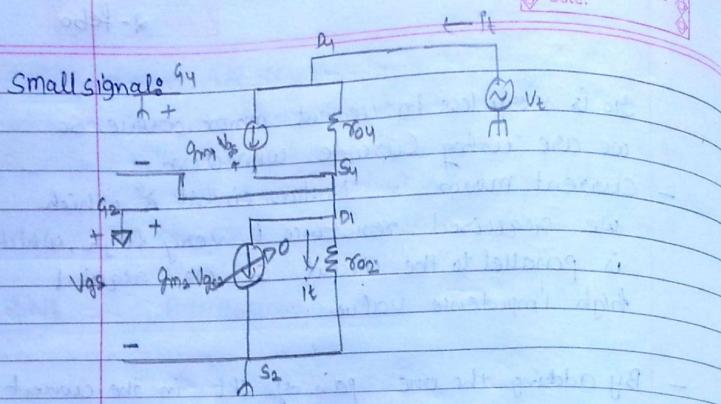
- Current mirror is Norton circuit in which we required resistance is very high, which is parallel to the circuit, so we required high impedance value.

- By adding the one pair of ckt in the current mirror source, o/p impedance will be $1/g_{os}$ at the o/p node.



$2V_{DS(\text{sat})} \rightarrow$ because two devices must be in saturation, for constant the value of current

$V_{GS} - V_T \rightarrow$ voltage fed from



$$i_t = g_{m4} V_{gs4} + \frac{V_t - (-V_{gs4})}{g_{104}}$$

$$V_{gs4} = -i_t g_{102}$$

$$O/P \text{ impedance } R_o = g_{104} (1 + g_{m4} g_{102}) + g_{102}$$

$$V_t/i_t = R_o$$

$$i_t = -g_{m4} I_t g_{102} + \frac{V_t}{g_{104}} - \frac{I_t g_{102}}{g_{104}}$$

$$(1 + g_{m4} g_{102} + g_{102}) i_t = \frac{V_t}{g_{104}}$$

$$V_t/i_t = R_o \approx g_{m4} g_{102}^2$$

Sensitivity Analysis:

$$S_{V_{DD}}^{i_o} = \lim_{\Delta V_{DD} \rightarrow 0} \frac{\Delta i_o / i_o}{\Delta V_{DD} / V_{DD}}$$

$$= \frac{V_{DD}}{I_o} \frac{\Delta I_o}{\Delta V_{DD}}$$

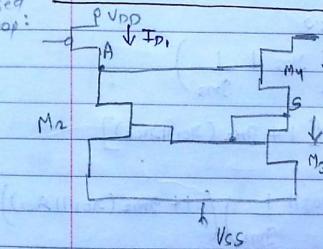
$$S_{V_{DD}}^{i_o} = \frac{V_{DD}}{I_o} \cdot \frac{1}{R}$$

$$\frac{\Delta I_o}{I_o} = S_{V_{DD}}^{i_o} \cdot \frac{\Delta V_{DD}}{V_{DD}}$$

- thickness of oxide is changes, V_t is also changes
Due to that variation in speed of device will occur \rightarrow that's known as "Corner Analysis"
- In cascode connection, o/p impedance is I_{ses} , but current is constant and voltage headroom also I_{ses} .

3-feb

Wilson Current Mirror:



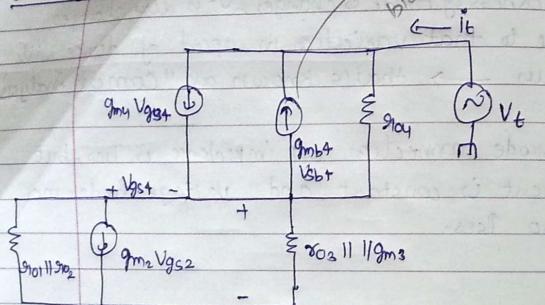
- I_{D1} is constant
- so due to that V_A \downarrow ses
- feedback is M_3 & M_2

in any case if I_o is I_{ses} , so current through the M_3 is I_{ses} due to that b/c of current mirror current through M_2 is also I_{ses} \rightarrow at node A, voltage is \downarrow ses which is V_{gs} for M_4 , that's \downarrow ses and due to that current I_o take (get) its new value and change is not there \rightarrow that is

- Current mirror can be improved with negative feedback.

• Current feedback:
(feedback \rightarrow current minor)
x) Substrate (bottom)
select MA

Small signal analysis:



$$V_{SB4} = V_{95\%}$$

$$Vgs2 = it \left(\frac{g_{m3}}{g_{m2}} \parallel \frac{1}{g_{m3}} \right)$$

$$Vgs4 = -Vgs2 \left[1 + g_{m2} (g_{o1})_1 g_{o2} \right]$$

$$= -\dot{t} \left(\frac{g_{103} || 1}{g_{m_3}} \right) \left(1 + g_{m_2} (g_{10}) || g_{20} \right)$$

$$I_t = g_{my} V_{gs4} - g_{mb4} V_{sb4} + \underline{V_t - V_{gs2}}$$

$$903 \parallel \frac{1}{9m_3} \stackrel{\sim}{=} \frac{1}{9m_3}$$

$$R_{out} = g_{m1} \left[1 + g_{m2} (g_{o1} || g_{o2}) + g_{mb4} \left(\frac{1}{g_{m3}} \right) + \frac{1}{g_{o4} g_{mb3}} \right]$$

$$\therefore g_{m3} = g_{mb} +$$

$$\begin{aligned}
 R_{out} &= \pi \rho \left[1 + g_{m2} \frac{g_{10}}{2} + \frac{g_{m3}}{g_{m2}} + \frac{1}{\pi \rho g_{m3}} \right] \\
 &= \pi \rho \left[1 + g_{m2} \frac{g_{10}}{2} + \frac{1}{\pi \rho g_{m3}} \right] \\
 &= \frac{0.5 \rho + g_{m2} \frac{g_{10}^2}{2}}{g_{m2}} + \frac{1}{g_{m2}}
 \end{aligned}$$

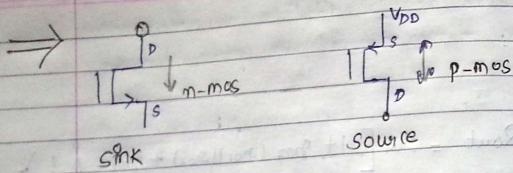
$$R_{out} \approx r_0 + g_{me} \frac{r_0^2}{2}$$

Current shunt

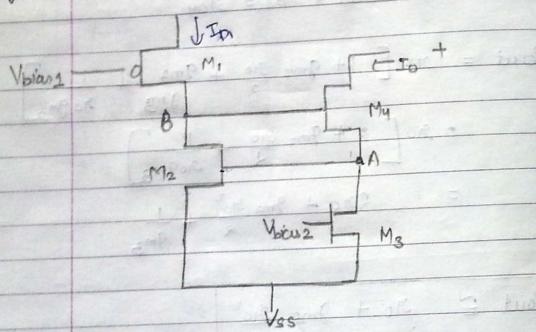
drawback

* (Cascade) \rightarrow (Wilson)

- in cascade, current is not stabilize as much as wilson current mirror is done. because cascade is ideally design of ckt, but we can say that wilson is practically current mirror ckt.



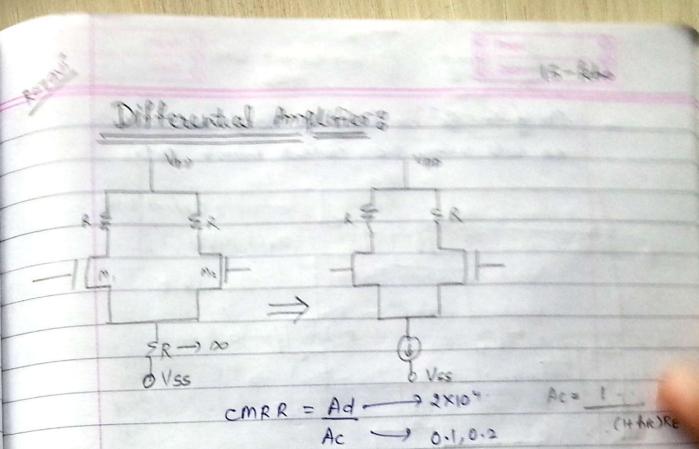
Regulated cascode current sink



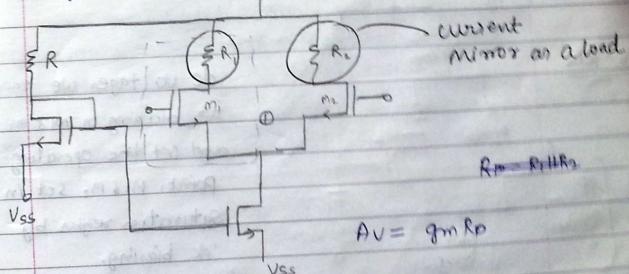
if we increase the $I_o \rightarrow V_A$ is also increased ($M_2 \rightarrow$) current through M_2 increases \rightarrow Voltage at B would increase \rightarrow so it compensates the increasing amount of current $I_o \rightarrow$ so stabilize the current.

- feedback is M_3

$$R_{\text{out}} = \frac{g m^2 g_0}{e^3}$$



$R \rightarrow \infty$, to improve the CMRR, that not possible with the R . So we are using cement ^{minor} source which provide the resistance in M_2 , which is very high.



When we applied diff voltage V_{DS} to M_1, M_2 and M_3, M_4 , then current will flow due to that

- So input common mode voltage must be in range b/w $V_1 \rightarrow V_2$ & also it must be stable.

O/P CM model

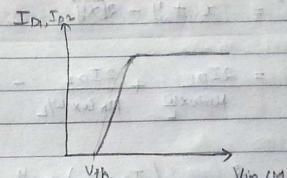
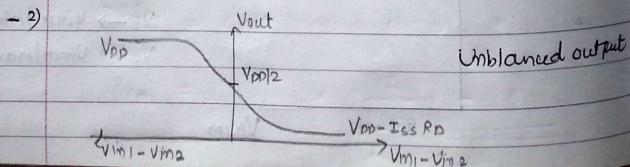
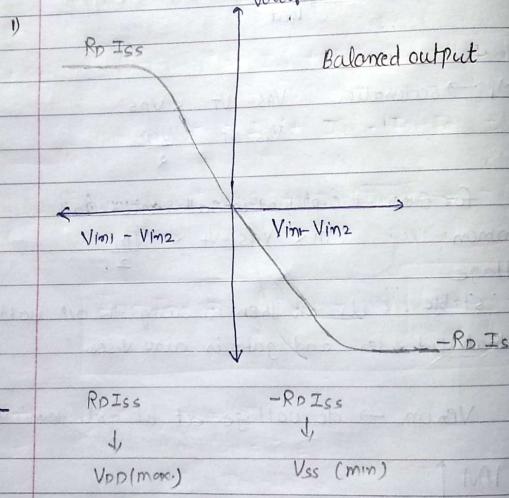
(dc voltage)

$$V_{out1} = V_{DD} - I_{D1} R_D$$

$$V_{out2} = V_{DD} - I_{D2} R_D$$

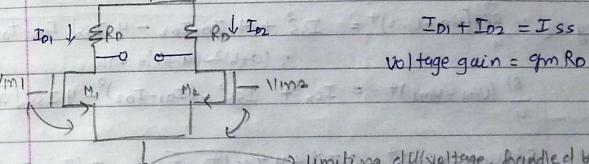
$$V_{out1} - V_{out2} = (I_{D2} - I_{D1}) R_D$$

$$V_{out1} - V_{out2}$$



② Diff' input handling capacity

Differential Voltages which can be handled by the diff' amp is limited by the I_{SS}



limiting diff/voltage, bounded by the I_{SS}

$$V_{in1} - V_{in2} = V_{GS1} - V_{GS2}$$

$$\therefore V_{GS} - V_{TH} = \sqrt{\frac{2 I_D}{\mu n \omega L}}$$

$$V_{in1} - V_{in2} = \sqrt{\frac{2 I_{D1}}{\mu n \omega L}} - \sqrt{\frac{2 I_{D2}}{\mu n \omega L}} - 0$$

$$V_{out} = I_{D1} R_D - I_{D2} R_D$$

$$= R_D (I_{D1} - I_{D2})$$

$$\text{In eqn ① } (V_{in1} - V_{in2})^2 = (\sqrt{I_{D1}} - \sqrt{I_{D2}})^2$$

$$(V_{in1} - V_{in2})^2 = x + y - 2\sqrt{xy}$$

$$= \frac{2I_{D1}}{\mu_n C_o x w/L} + \frac{2I_{D2}}{\mu_n C_o x w/L} - 2 \sqrt{\frac{2I_{D1}}{\mu_n C_o x w/L} \frac{2I_{D2}}{\mu_n C_o x w/L}}$$

$$= \frac{2}{\mu_n C_o x w/L} (I_{D1} + I_{D2}) - \frac{4}{\mu_n C_o x w/L} \sqrt{I_{D1} I_{D2}}$$

$$= \frac{2}{\beta} (I_{D1} + I_{D2} - 2\sqrt{I_{D1} I_{D2}})$$

$$\frac{\beta}{2} (V_{in1} - V_{in2})^2 = (I_{SS} - 2\sqrt{I_{D1} I_{D2}})$$

$$\text{By sq: } \frac{\beta^2}{4} (V_{in1} - V_{in2})^4 = I_{SS}^3 + 4 I_{D1} I_{D2} - 4 I_{SS} \sqrt{I_{D1} I_{D2}}$$

$$\therefore (a+b)^2 - (a-b)^2 = 4ab$$

$$\frac{\beta^2}{4} (V_{in1} - V_{in2})^4 = I_{SS}^3 + I_{SS}^2 - (I_{D1} + I_{D2})^2 - 4 I_{SS} \sqrt{I_{D1} I_{D2}}$$

$$\frac{\beta^2}{4} (V_{in1} - V_{in2})^4 - 2 I_{SS}^2 + 4 I_{SS} \sqrt{I_{D1} I_{D2}} = -(I_{D1} - I_{D2})^2$$

$$I_{D1} - I_{D2} = \frac{\beta}{2} (V_{in1} - V_{in2}) \sqrt{\frac{4 I_{SS}}{\mu_n C_o x w/L} - (V_{in1} - V_{in2})^2}$$

When $V_{in1} = V_{in2}$

then $I_{D1} = I_{D2}$

$$\Delta I_o = I_{D1} - I_{D2} \quad \Delta V_{in} = V_{in1} - V_{in2}$$

$\frac{\partial I_{D1}}{\partial V_{in}}$ = diff transconductance

ΔV_{in}

$$G_m = \frac{1}{2} \frac{\mu_n w/L}{C_o} \frac{4 I_{SS}}{\mu_n C_o x w/L} - \frac{2}{\mu_n C_o x w/L} \Delta V_{in}^2$$

$$\Delta V_{in} \rightarrow 0$$

$$G_m = \frac{\mu_n w/L}{2} \cdot I_{SS}$$

G_m is dependent of I_{SS} .

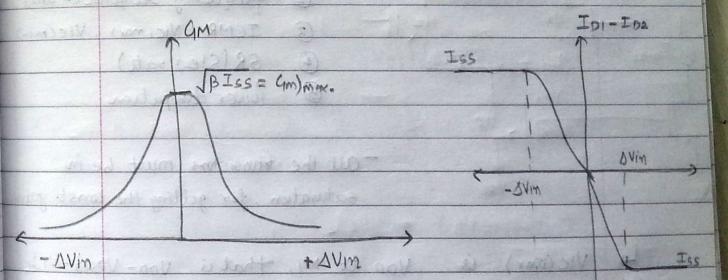
- if $V_{in1} \ll V_{in2}$, I_{D1} is set in such a way that $I_{D1} = I_{SS}$, then I_{D2} must be zero, bcoz its limited by the diff. amplifier.

* I_{SS} → Bandwidth

→ Power dissipation

→ Slew rate

$$\Delta V_{in} = \sqrt{\frac{2 I_{SS}}{\mu_n C_o x w/L}}$$



↑ this range of voltage
can be handled
by the diff. amp.

for Differential comp:

$$V_{id} = V_1 - V_2$$

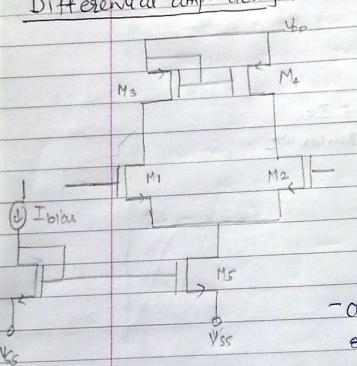
$$V_{cm} = \frac{V_1 + V_2}{2}$$

$$CMRR = \frac{A_d}{A_{cm}}$$

$$V_{out} = A_d V_{id} \pm A_{cm} V_{cm}$$

Allen-Hover's Bias

Differential comp design:



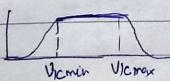
specifications:

- ① Small Signal gain A_v
- ② frequency response (-3dB)
- ③ ICMR ($V_{IC(max)}$, $V_{IC(min)}$)
- ④ SR (Slew rate)
- ⑤ Power dissipation

All the transistors must be in saturation, for getting the const. gain

↳ $V_{IC(max)}$ is V_{DD} to M_1 , that is $V_{DD} - V_{DS3} - V_{T1}$
↳ $V_{IC(min)} = -V_{SS} - V_{DS1} - V_{T1}$

- output is linearly changes by changing the I_{IP} & gain will remain constant, which we required in b/w $V_{IC(max)}$ to $V_{IC(min)}$ gain is constant.



We have to design the diff. ampr (for that we have to find out the W/L ratio for all the transistors)

Design Equations:

$$1) A_v = g_m R_{out} = g_m (g_{ds2} || g_{ds4}) \\ = g_m \\ g_{ds2} + g_{ds4}$$

$$2) -3 \text{ dB frequency} = \frac{1}{2\pi R_{out} C_{out}} \\ R_{out} = \frac{1}{g_{ds2} + g_{ds4}}$$

$$3) V_{IC(min)} = V_{DD} - V_{DS3} + V_T \rightarrow \text{DC voltage range b/w V_{IC}}$$
$$V_{IC(max)} = V_{DS1} + V_{SS} \rightarrow \text{V_{IC(max)} to V_{out}}$$

$$4) \text{Slew rate} = \frac{I_S}{C_L} \rightarrow \text{changes}$$

$$5) \text{power dissipation} = (V_{DD} + V_{SS}) I_S$$

Design steps:

① choose I_S to satisfy 1) SR
2) PD

$$\left\{ \begin{array}{l} \text{If Power rating is } = 1 \text{ mW} \\ 1 \text{ mW} = 5 \times I_S \\ I_S = 200 \text{ mA} \end{array} \right. \rightarrow I_S = \frac{10 \text{ V}}{5 \text{ U}_F} = 70 \text{ mA}$$

To current must be $70mA < I_S < 200mA$

② check Rout from freq. response

③ Design w/L_3 & w/L_4 from I_{CMRmax} .

$$V_{ICmax} = V_{DD} - V_{SD} + V_T$$

↓ we know
given

V_{SD} , we can find that.

& current is $I_S/2$ from the M_3

$$I_D = \mu_n C_o x \frac{w}{L} \left(\frac{V_{GS} - V_T}{V_{DS}} \right)^2$$

we know that

we have finding

so we can find the w/L ratio.

$$g_m = \sqrt{2 I_D \beta}$$

} — when g_m, V_{GS}, V_{DS} are given
we can easily find out the
 w/L ratio.

$$w/L_3 = w/L_4$$

④ Design w/L_1 & w/L_2 to satisfy the Av.

$$Av = g_m R_{out} = g_m$$

given

$$g_{ds} = I_D K$$

$g_m = \sqrt{2 I_D \beta}$ — from this we can able to
find the value of w/L_1 & w/L_2

$$V_{GS} = \sqrt{2 I_D \beta} \quad V_{DS} = \sqrt{\frac{2 I_D}{\beta}}$$

Page: 23 feb
Date: $I_D = \frac{P}{V_{DS}} = \frac{P}{(V_{DS})^2}$

⑤ Design w/L_5 from the V_{ICmin}

$$V_{ICmin} = V_{DS} + V_{GS}$$

— current flowing from M_5 is I_S and
current flowing through the M_1, M_2, M_3, M_4 is I_S .

$$I_{DS} = \frac{\mu_n C_o x \left(\frac{w}{L} \right)_5 (V_{DS})^2}{2}$$

23 feb

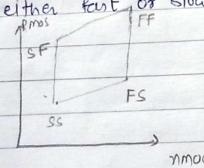
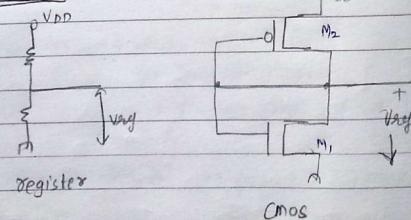
Voltage Reference:

Ref. Ckt: A ref. ckt. is an independent current and voltage source which has a high degree of precision and stability.

- independent of power supply
- independent of temp
- independent of processing variations.
 - LTL (lot to lot) due to manufacturing
 - WTW (wafer to wafer)
 - DTD (die to die)
 - DWD (die within die)

due to change in oxidizing layer, speed of mos will affected either fast or slow.

design corner

Voltage Divider:

Q & D are shorted in M₁ & M₂, so its act as resistor
Both are in saturation

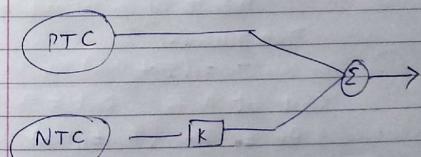
$$I_{D2} = \frac{\beta_2}{2} (V_{DD} - V_{T_{H,P}} - V_{T_{H,N}})^2 \quad (1)$$

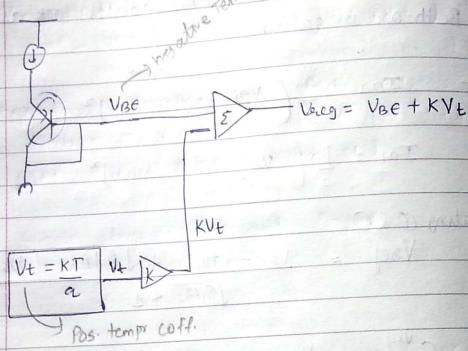
$$I_{D1} = \frac{\beta_1}{2} (V_{ref} - V_{SS} - V_{T_{H,N}})^2 \quad (2)$$

By equating (1) & (2)

$$V_{ref.} = \frac{V_{DD} - V_{T_{H,P}} + \sqrt{\beta_1/\beta_2} (V_{SS} + V_{T_{H,N}})}{\sqrt{\beta_1/\beta_2} + 1}$$

Variation in $\frac{V_{ref.}}{V_{DD}}$ = $\frac{V_{DD}}{(V_{DD} - V_{T_{H,P}}) + \sqrt{\beta_1/\beta_2} (V_{SS} + V_{T_{H,N}})}$

Bandgap reference:



Chapter-7 Noise

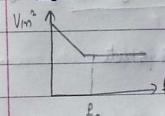
① Thermic noise \rightarrow represented as parallel current at the output or as voltage at output.

$$V_{in}^2 = 4KT \left(\frac{2}{3} g_m \right) V_o^2 = I_o^2 \frac{V_o^2}{R_o}$$

② flicker noise \rightarrow presented as series voltage on gate.

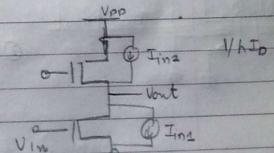
$$V_{in}^2 = \frac{K}{Cox \omega L} \frac{1}{f}$$

also known as 1/f noise.



① Single stage common source amplifier

for \uparrow gain
represented by
single MOSFET



- if we \uparrow the gain then noise is \downarrow so then what we do for \uparrow gain then \uparrow $\frac{I_{se}}{I_{D1}}$ ratio or \uparrow I_{D1} current

In noise ckt made up of resistance & noise.
 signal to noise ratio at 1/f & 0/f

$$V_{in} \text{ equivalent 1/f noise on } M_1 \text{ gate:}$$

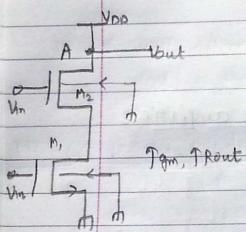
$$V_{in}^2 = MKT \left(\frac{2}{3} g_{m1} + \frac{2}{3} g_{m2} \right) \left(g_{o1} || g_{o2} \right)^2 \text{ d}f$$

- expands with resistance and flicker noise: finds the flicker noise in the gate of M_1 & M_2 , find the flicker noise in the ckt. 7.36. (common source 2/2)

② Single stage common gate Amps

* Cascade amplifier :- 2 - Stage Amps

CS stage followed by + CG stage



① \rightarrow we place the n-mos and upper side. also place n-mos. Then Rout at point A is

$$R_{out} = g_m$$

② \rightarrow If substrate of M_1 is tied but substrate of M_2 is not grounded

Then gain is

$$g_{12} = (g_{m1} g_{mb}) g_{m2} g_{mr}$$

Rout at A is $R_{out} = g_m g_{m2}^2$
& $A_v = g_{m1} (R_{out} || R_o)$

- if change resistance R_o & put with current source I_o

conducting in single stage amp \rightarrow final $A_v = A_{v1} \cdot A_{v2} \cdot A_{v3}$

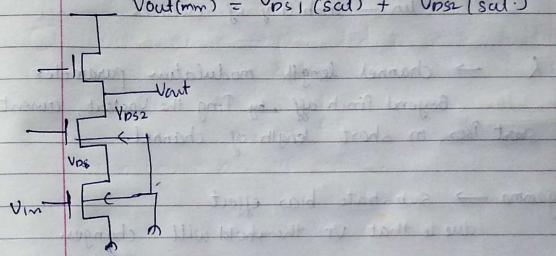
$$I_{DQ} \rightarrow V_{in} \rightarrow V_{out}$$

biasing condition in large signal amp

$$① V_{DS1} = V_{GS1} - V_{T1}$$

$$② V_{DS2} = V_b - V_{DS1} - V_{T2}$$

$$V_{out(\text{mm})} = V_{DS1}(\text{sat}) + V_{DS2}(\text{sat})$$



Tie V_{GS1} with V_{GS2} and V_{GS3} with V_{DS1} and V_{DS2} with V_{DS3}

then $V_{GS1} = V_{GS2} = V_{GS3}$

then $V_{DS1} = V_{DS2} = V_{DS3}$

then $V_{out1} = V_{out2} = V_{out3}$

then $A_v1 = A_v2 = A_v3$

then $A_v = A_v1 \cdot A_v2 \cdot A_v3$

Page: 23 Date: 9-March-2023

9-March

MOS Transistor theory (say 10 min)

* $V_t \rightarrow$ threshold Voltage is required to channel inversion (means p-channel converted into n-channel)

$K_m = \mu_n C_{ox} \rightarrow$ C_{ox} - oxide capacitor
 μ_n - mobility of electrons

$\lambda \rightarrow$ channel length modulation parameter

Beyond pinch off, by increasing the V_{ds} , current will short rise in short length of channel.

$\gamma \rightarrow$ substrate bias effect
due to that V_t threshold will changes.

Model will define the behaviour of the MOSFET. SPICE tool is the circuit solver.

MOS Capacitance Model:

C_{sb} & C_{db} are the reverse bias diode capacitor in the capacitor model. Due to capacitor and parasitic resistance delay will occur in OIP, which is digital.

- short channel/weak inversion / substrate conduction

Page: _____ Date: _____

Mobility degradation and Velocity saturation:

dropping V_{ds} \rightarrow velocity V_{ds} \rightarrow I_d current I_{ds}

Gate induced drain current

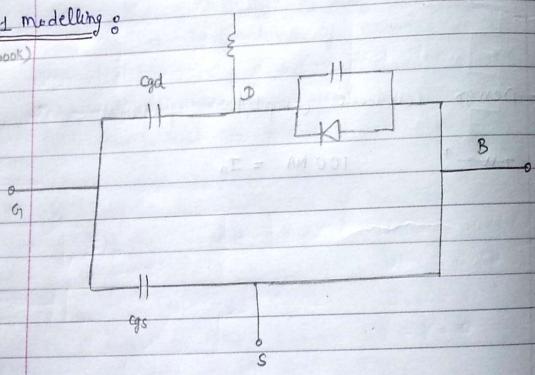
Ex- Design cascode amplifiers (from book)

Ans $100 \text{ mA} = I_d$

- charge based modelling is done now a days.
- for simulation or define the V-I char' of mosFET circuit, we required some constants and capacitor values (which are calculated in small signal analysis) which are define in model. So model defines the behaviour of mosFET.

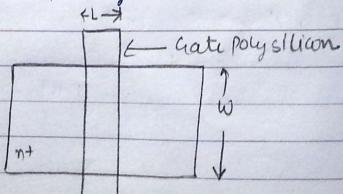
level 1 modelling :

(from book)



In level 1 we defined V_{TO} , L , Γ , γ , k_p

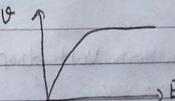
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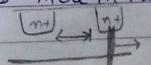
- current is dependent on channel area
- By doing scaling of W , L , tox , X_j \rightarrow depth of
- 1μ technology means, length of mos or length of channel $L = 1\mu$, which is the min length of the channel and we can't decrease that but we can used that by doing scaling.
- According to moore, after every 18 months technology will double half and package density (no. of transistor) will 1.5 times. So we can say that for a particular length of channel or technology life tym is only 18 months.
- Scaling factor $S = \sqrt{2}$

$$\begin{matrix} 1\mu \\ \downarrow \\ 0.5\mu \\ \downarrow \\ 0.35\mu \end{matrix}$$

- In full scaling we scaled down the W , L , tox , V_{DD} and I_D By S .
- Constant voltage Scaling, Electric field rises due to that second order effect will occurs - that is
 - velocity saturation & leakage

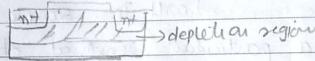


① IBL \rightarrow drain induced barrier lower, due to that leakage is there in mos



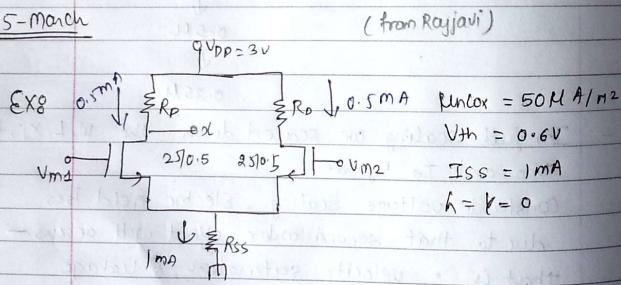
- mobility degradation
 - mobility \propto doping (if doping I_{DS} , then mobility is less, bcoz of temp)
 - * velocity is prop. to the drain current.

- punch through \rightarrow
 - when charges are merge from the depletion region of source and drain, then our mos will damaged that's known as punch through.



when depletion region of source and drain are mix \rightarrow punch through.

15-March



i) Calculate g_{mP} cm level when volt. drop across R_{DS} is 0.5V

ii) Calculate R_D

So,

design \rightarrow LN Haulburg

$$I_{D1} = I_{D2} = 0.5 \text{ mA}$$

$$V_{GS1} = V_{GS2} = \sqrt{2 I_{D1} \mu_{nCOX} w/L} + V_{th}$$

$$= \sqrt{\frac{2 \times 0.5 \times 0.5}{50 \times 10^{-3} \times 25}} + 0.6$$

$$V_{GS} = 1.23 \text{ V}$$

$$V_{in,cm} = V_{GS1} + \text{Voltage drop across the } R_{DS}$$

$$= 1.23 + 0.5$$

$$= 1.73 \text{ V}$$

$$R_{DS} = \frac{10^3 B \times 0.5}{1 \text{ mA}} = 500 \Omega$$

ii)

$$g_m = \sqrt{2 \mu_{nCOX} (w/L) I_D}$$

$$= \sqrt{2 \times 50 \times 10^{-6} \times \frac{25}{0.5} \times 0.5 \times 10^{-3}}$$

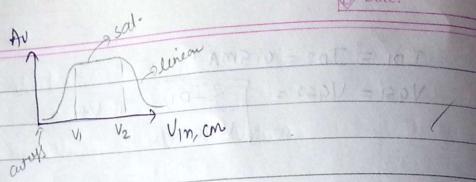
$$= 15.81 \times 10^{-4}$$

$$\text{Gain} = 5 = \frac{g_m R_D}{R_D}$$

$$50, R_D = \frac{5}{g_m} = 3.16 \text{ k}\Omega$$

$$\text{OIP bias voltage level} = V_{DD} - I_{D1} R_D$$

$$= 3 - 0.5 \times 3.16 = 1.42 \text{ V}$$



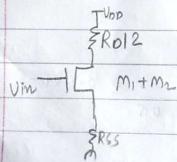
- (c) What happens at the OIP if $V_{in, cm}$ level is 50mV higher than the value calculated in (a)

$$V_{in, cm} = 1.73 + 50 \text{ mV} = 1.78 \text{ V}$$

$$A_{v, cm} = \frac{V_{out}}{V_{in, cm}}$$

$$A_{v, cm} = \frac{R_{D12}}{R_{SS} + \frac{1}{2g_m}}$$

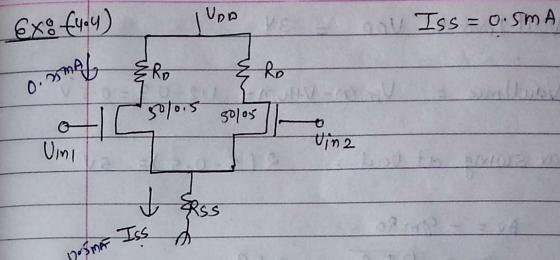
- When V_{in1} & V_{in2} are shorted $R_{D1}||R_D \rightarrow R_{D12}$



$$(d) |\Delta V_{x,y}| = |\Delta V_{in, cm}| \frac{R_{D12}}{R_{SS} + 1/2g_m}$$

$$= 50 \text{ mV} \times 1.94$$

$$= 96.8 \text{ mV}$$



- (a) What is max. allowable OIP voltage swing if $V_{in, cm} = 1.2 \text{ V}$

- (b) What is the voltage gain under this cond.

$$I_{D1} = I_{D2} = 0.25 \text{ mA}$$

$$V_{in, cm} = 1.2 \text{ V}$$

$$R_{SS} = 0.5/0.5 \text{ mA} = 1 \text{ k}\Omega$$

$$R_D = 5/g_m$$

$$g_m = \sqrt{2 I_{D1} \beta}$$

$$= \sqrt{2 \times 0.25 \times 10^{-3} \times \mu_{n,COX} \times \frac{50}{0.5}}$$

$$= 15.81 \times 10^{-4} \quad (\mu_{n,COX} = 50 \text{ NAm}^{-2})$$

$$R_D = 5/15.81 = 3.16 \text{ k}\Omega$$

$$V_{DD} - I_{D1}R_D = 3 - 0.25 \times 3.16 = 2.21 \text{ V}$$

$$A_v(\text{gain}) = \frac{R_{D12}}{R_{SS} + 1/2g_m}$$

$$= \frac{3.16 \text{ k}\Omega}{1 \text{ k}\Omega + 1/(2 \times 15.81 \times 10^{-4})} = 2.4$$

$$(a) V_{out\ max} = V_{DD} = 3V$$

$$V_{out\ min} = V_{in, CM} - V_{th, m} = 1.2 - 0.7 = 0.5V$$

$$\text{max. swing at } V_{out} = 2(3 - 0.5) = 5V$$

$$(b) A_v = -g_m R_o$$

$$g_m = \sqrt{2 I_{DSS} \beta} = 2.59$$

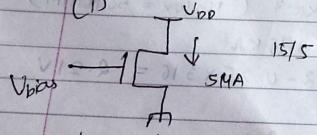
$$\text{to get max. swing } R_o I_{SS} = \frac{V_{out\ max} - V_{out\ min}}{2} = 1.25 \text{ m}$$

$$R_o = \frac{1.25 \times 2}{I_{SS}} = 5k\Omega$$

$$A_v = g_m R_o = -2.59 \times 5k = -13$$

16-March

Ex 8 - Design a ckt to bias the mos fet below:



When it is in sat:

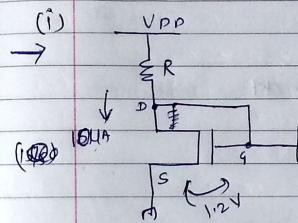
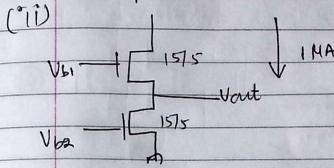
$$5mA = \frac{10mA}{2} \times \frac{15}{5} \left[V_{bias} - V_{th} \right]^2$$

$$5mA = \frac{10mA}{2} \times \frac{15}{5} = \left(V_{bias} - 0.7 \right)^2$$

$$V_{bias} =$$

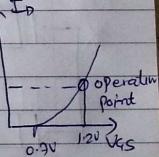
for biasing the ckt. current mirror is used

Ex :- Design a ckt

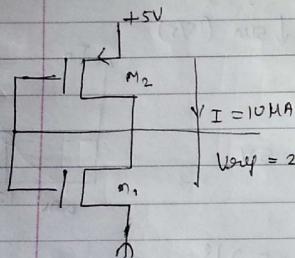


let assume $V_{DD} = 5V$

$$10mA = \frac{5}{2} \times \frac{15}{5} \left(V_{bias} - 0.7 \right)^2$$



(iii) Design a Volt. reference ckt.



$$I_{D2} = \frac{B_2}{2} \left(V_{DD} - V_{th,P} - V_{reg} \right)^2$$

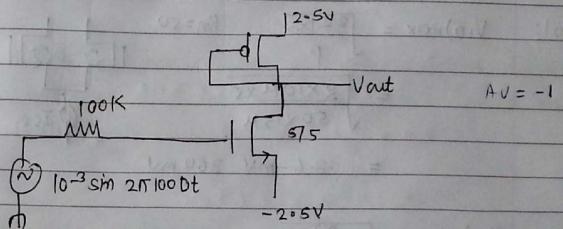
$$I_{D1} = \frac{\beta_1}{2} (V_{ref} - V_{th,n})^2$$

$$\mu_{n(\omega)x} p \left(\frac{\omega}{L}\right)_2 \left[5 + 0.8 - 2 \right]^2 = \left(\frac{\omega}{L}\right)_1 \mu_{n(\omega)x} \eta \left[2 - 0.7 \right]^2$$

$$100 \left(\frac{\omega}{L}\right)_2 \left[3.8 \right]^2 = 350 \left(\frac{\omega}{L}\right)_1 \left[1.3 \right]^2$$

$$\frac{w/L)_2}{w/L)_1} = 0.40$$

$\omega/L)_1$



find V_{out} voltage.

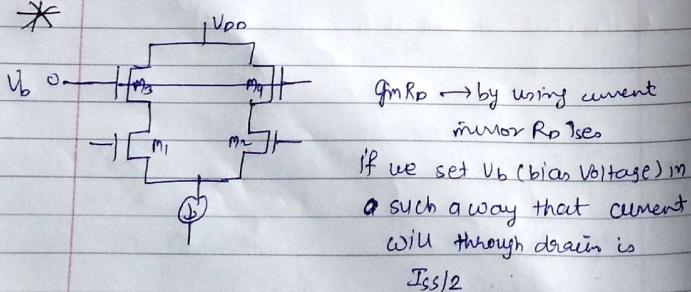
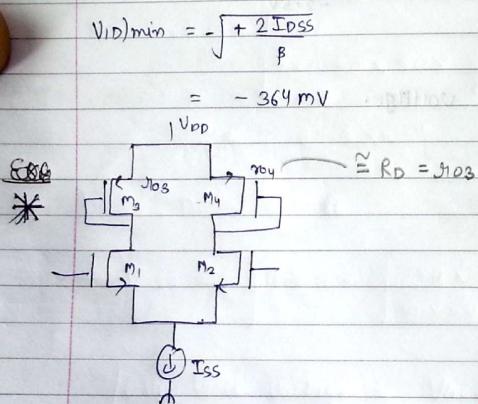
Sol:

Ex: (1) In a diff. amp. $I_{SS} = 10 \mu A$, $W_1 = W_2 = 15 \mu m$, $L_1 = L_2 = 5 \mu m$. determine $V_{ID(max)}$?

Sol: $V_{ID(max)} = \sqrt{\frac{2I_{DSS}}{\beta}} \quad K_n = 50$

$$= \sqrt{\frac{2 \times 10 \times 15}{50 \times 15}} \quad \text{MOSFET symbol}$$

$$= 3.6 \text{ mV} \quad 364 \text{ mV}$$

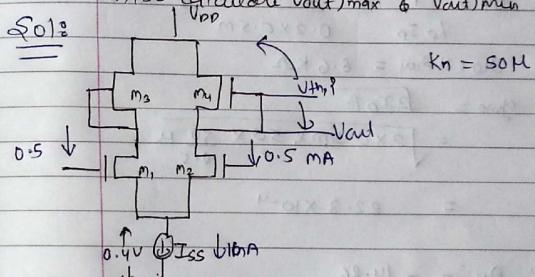


- amplitude distortion, when gm is changes by changing the input. So gm must be constant.

Ex: for a diff pair calculate differential gain if $I_{SS} = 1 \mu A$, $W/L_{1,2} = \frac{50}{0.5}$, $W/L_{3,4} = \frac{50}{1}$

what is min allowable common mode voltage $V_{cm} = ?$, if volt drop across I_{SS} is 0.4 V

Also calculate $V_{out(max)}$ & $V_{out(min)}$



i) $V_{GS1} = \sqrt{\frac{2I_D}{\beta}} + V_{th,n}$

$$= \sqrt{\frac{2 \times 0.5 \times 0.5}{50 \times 10^{-6} \times 50}}$$

$$= 0.44 + 0.7 = 1.14 \text{ V}$$

$V_{cm} = V_{GS1} + 0.4 = 1.5 \text{ V}$

$V_{out(min)} = 1.5 - 0.9 = 0.6 \text{ V}$

$V_{out(max)} = V_{DD} - V_{th} = 3 - 0.8 = 2.2 \text{ V}$

$V_{out(min)} = V_{cm} - V_{th} = 1.5 - 0.8 = 0.7 \text{ V}$

then swing = $2(0.7 - 0.6) = 0.4 \text{ V}$

$V_{out(min)} = V_{DD} - V_{GS1} = 3 - 0.98 = 2.02 \text{ V}$

$0.18 \text{ swing} = 0.36 \text{ V}$

Overdrive voltage $\rightarrow V_{GS}$, Volt required to keep the MOS in saturation

(iii) Voltage gain

$$A_V = -g_{m2} (g_{o2} || g_{o4})$$

$$g_{o2} = \frac{1}{h_F I_D} = \frac{1}{0.1 \times 0.5 \text{ mA}} = 20 \text{ k}\Omega$$

$$g_{o4} = \frac{1}{h_F I_D} = \frac{1}{0.2 \times 0.5 \text{ mA}} = 10 \text{ k}\Omega$$

$$g_{o2} || g_{o4} = 6.6 \text{ k}\Omega$$

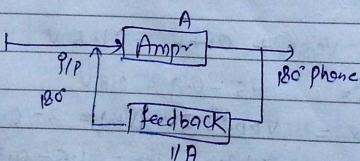
$$g_{m2} = \frac{2 I_D \beta}{2 \times 0.5 \text{ mA} \times 50 \times \frac{50}{0.5} \mu} = 22.3 \times 10^{-4}$$

$$\text{So, } A_V = -14.86$$

$$- V_{GS3} = \sqrt{\frac{2 I_D}{\beta}} = \sqrt{\frac{2 \times 0.5}{50 \times 50}} = 0.02$$

Overdrive voltage = $V_{GS} - V_{th}$

(Volt required to keep MOS in saturation)



total Phase shift = 360°
 $g_{m1} = 1$; g_{o1} oscillates

Hansberg (Chp-6)

CMOS Operational Amplifier

Page: _____ Date: 8-4-march

- When we have to design Amps, if we design multistage Amps, so there is chance that ckt can work as oscillator. So to remove that we have to add some phase shift, so over ckt will work as Amplifier.

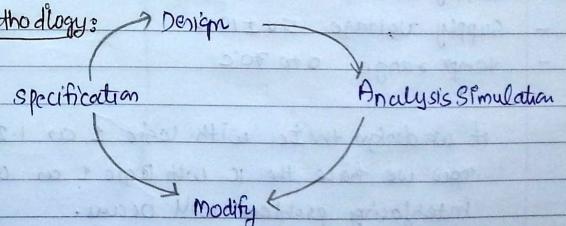
(2 stage Amps \rightarrow 360° phase shift \rightarrow oscillator)

So we have to add or compensate that we used "compensation ckt."

- Capacitors \rightarrow current is provided, then cap. start charging and then voltage across the cap is lagging 90° by the current.

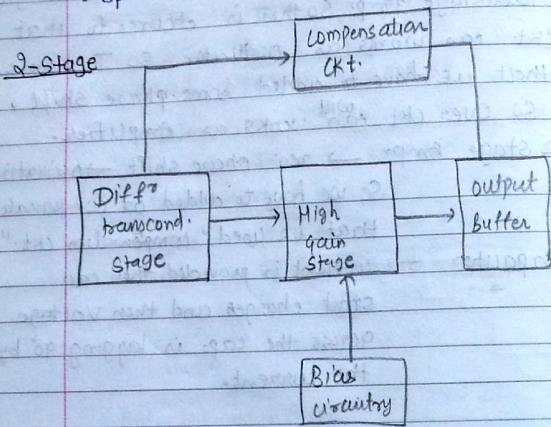
- Bode plot (at x-axis freq. and y-axis gain) is the frequency response.

Design methodology:



for MOSFET $\xrightarrow{\text{design}}$ 7 to 8 months are required

Tradeoff
 { Speed and power dissipation
 { Speed and area



Boundary conditions/constraints

- Supply current 100mA
- Supply voltage $5\text{V} \pm 10\%$
- Temp range 0 to 70°C

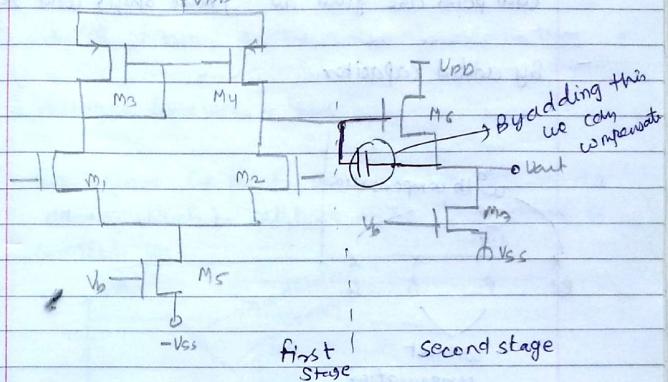
If we design the IC with logic 1 as 1.25V and now we have the IC with logic 1 as 0.75V then interfacing problem will occurs.

- $\text{Gain} > 80\text{dB}$

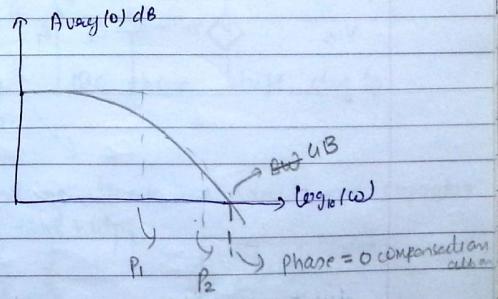
$$\text{Gain-BW} \geq 10\text{MHz} \quad (1\text{M to } 10\text{MHz})$$

$$\text{SR} \geq 1\text{V}/\mu\text{sec} \quad (0: 1\text{V}/\mu\text{sec} \text{ to } 10\text{V}/\mu\text{sec})$$

- at gain-BW , $\text{BW} \text{ curren} = 0\text{dB}$, that means operational amplifier starts to oscillate.



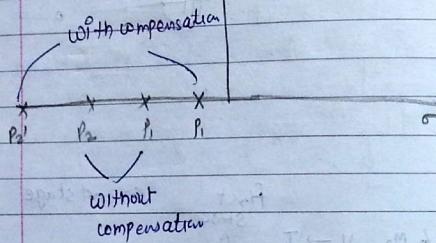
Boode plot



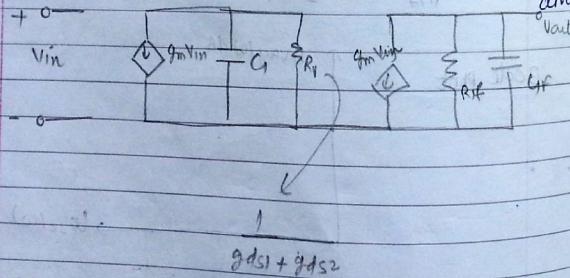
$|P_1| \rightarrow$ shifted origin beyond ω_B
 $|P_2| \rightarrow$ shift to (after) ω_B to compensate the oscillation effect

We have done this by using the capacitor in the two stage diff. Amplifier. Each poles are given 90° phase shift, and 20dB/decade.

- By added capacitor



- two stage Amp = differential amp + Normal

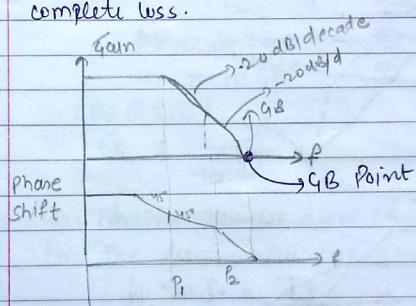


due to capacitance, we get poles, which gives the 20dB/decade down.

in the phase margin = 0 so output will swing or not constant or oscillate.

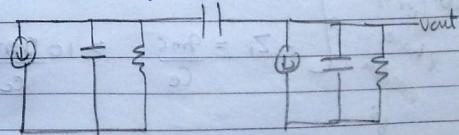
- at GB point gain = 0dB, means $\frac{V_{out}}{V_{in}} = 1$ (Voltage follower)

- So before GB point we seen we get 40dB down which is shows that our signal is complete loss.



Here we get 180° phase shift due to the poles.

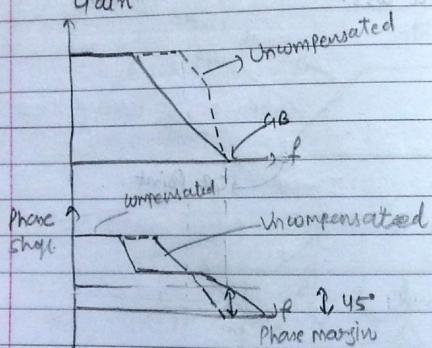
- for compensation that we added one capacitor



for compensating the phase shift, we added cap. at the output of the first diff. amp. and b/w input of the 2nd amp.

- To achieve the stable output we have to compromise with the (3dB freq) cut off freq. b/w to shift the pole P_1 to the origin, 3dB freq. will be very poor.

P_1 & P_2 are beyond the GB point



$$GB = \frac{g_{m2}}{C_e} = \frac{g_{m1}}{C_e}$$

Condition for getting phase margin $\{ P_2 \geq 2.2 GB \text{ for phase margin} = 60^\circ \}$

$$Z_1 = \frac{g_{mC}}{C_e} > 10 \frac{g_{m2}}{C_e}$$

Example: (for phase shift = 60°)

- $G_{\text{clim}} \text{ BW Product is always constant.}$
- $C_{\text{B}} = 5 \text{ MHz}$ (means at that freq. $g_{m1} = 1$)
- SR and Pdiss is decided our biasing current.

$$\Rightarrow \frac{g_{m2}}{C_e} = 0 \quad ; \quad \frac{g_{mC}}{C_L} = P_2$$

$$Z_1 = \frac{g_{mC}}{C_e} \quad ; \quad G_B = \frac{g_{m1}}{C_e}$$

$$P_2 > 2.2 G_B \quad \text{--- (1)}$$

$$Z_1 > 10 G_B \quad \text{--- (2)}$$

(By (1) & (2))

$$C_e = \frac{2.2}{10} C_L$$

Design steps for compensated amp (two stage):

- ① find the compensated capacitor
- ②

Ex 8

Calculate small signal diff. gain g_{m2} & A_v for n-channel diff. Amp. when $I_{SS} = 100\text{mA}$

$$i) \frac{w_1}{L_1} = \frac{w_2}{L_2} = \frac{w_3}{L_3} = \frac{w_4}{L_4} = 1, L_1 = L_2 = L_3 = L_4 = 1\text{m}$$

$$ii) \text{also } \frac{w_1}{L_1} = \frac{w_2}{L_2} = 10, \frac{w_3}{L_3} = 10, \frac{w_4}{L_4} = 10$$

So 10

$$i) g_{m2} = \sqrt{2 \times 50 \times 100 \times 1} = 104.88 \times 10^{-6} = 104.88 \mu$$

$$g_{ds2} = h_n I_D = 0.04 \times 50 = 2 \mu$$

$$g_{ds4} = h_p I_D = 0.05 \times 50 = 2.5 \mu$$

$$A_v = \frac{104.88}{2 + 2.5} = 33.30$$

$$ii) g_{m2} = \sqrt{2 \times 50 \times 110 \times 10} = 331.66 \mu$$

$$g_{ds2} = h_n I_D = 2 \mu$$

$$g_{ds4} = h_p I_D = 2.5 \mu$$

$$A_v = 73.70$$

for p-channel

$$(i) g_{m2} = \sqrt{2 \times 50 \times 50 \times 1} = \sqrt{2 \times 50 \times 50 \times 1} = 70.71 \mu$$

$$A_v = 15.71$$

In p-mos gain is less compare to n-mos and its

gives the low noise

Ex8 If all the devices in the diff' amp are saturated find the worst case i/p offset voltage. Assume the model parameters. $10 \left(\frac{w}{L} \right)_4 = 10 \left(\frac{w}{L} \right)_3 = \frac{w}{L_2} = \frac{w}{L_1} = \frac{10 \mu}{10 \mu} ; V_{thn} = 0.7V ; V_{thp} = -0.7V$

$$I_{SS} = 100 \text{ mA} \Rightarrow I_{D1} = I_{D2} = I_{SS}/2$$

$$V_{OS} = |V_{GS1} - V_{GS2}|$$

$$I_D = \frac{K_n}{2} (V_{GS} - V_{th})^2$$

$$I_{SS} = \mu_n C_o x K_n (V_{GS} - 0.7)^2$$

$$V_{GS1} = 1.65V \quad M_1 = 1M\Omega$$

$$I_D = \frac{K_p}{2} (V_{GS2} - V_{th})^2$$

$$I_{SS} = \mu_n C_o x K_p (V_{GS2} - V_{th})^2$$

$$V_{GS2} = 3.7V$$

$$V_{GS1} = \frac{\sqrt{I_{SS}}}{\beta} + V_{th}$$

$$V_{GS2} = \frac{\sqrt{2I_D}}{\beta} + V_{th}$$

If $I_{D1} \neq I_{D2}$

$$V_{OS} = |V_{th1} - V_{th2}| + \sqrt{\frac{2I_{D1}}{\beta}} - \sqrt{\frac{2I_{D2}}{\beta}}$$

When M_1 & M_2 are not mismatching in terms of current and threshold voltage.

$$\text{Assume } I_{D1} = 50 \text{ mA}$$

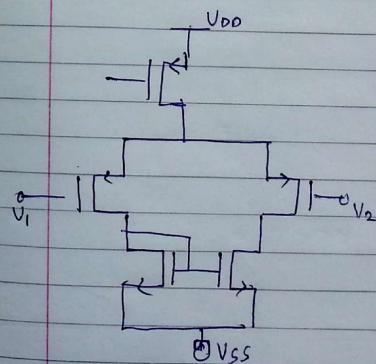
$$I_{D2} = 49 \text{ mA}$$

$$V_{th1} = 0.7V$$

$$V_{th2} = 0.71V$$

$$\text{then } V_{OS} = 0.019V$$

P-MOS diff' amp



Ex8

A 2-stage Miller compensated n/w find $\omega_{1,2,6}$ and C_C if $G_B = 1 \text{ MHz}$

$$\omega/L_6 = 12.33, \omega/L_{1,2} = 10$$

$$33.3 \text{ pF} = C_C$$

Page: _____
Date: 5-April

$|P_2| = 5 \text{ GB}, Z_1 = 3 \text{ GB}, C_L = 20 \text{ pF} = C_2$
Bias current through M_5 is $40 \mu\text{A}$ and
 M_7 is $320 \mu\text{A}$.

Sol:

$$C_C = \frac{2.2}{10} C_L$$

$$= \frac{2.2 \times 20 \text{ pF}}{10}$$

$$C_C = 4.4 \text{ pF}$$

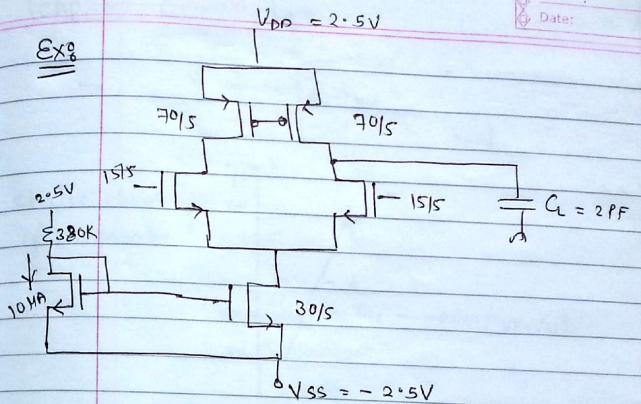
$$g_{mc} = Z_1 \cdot C_C = 3 \times 4.4 \times 10^{-12} = 13.2 \text{ p}$$

$$g_{mi} = G_B \cdot C_C = 10^6 \times 4.4 \times 10^{-12} = 4.4 \text{ M}$$

$$V_{DD} = 2.5 \text{ V}$$

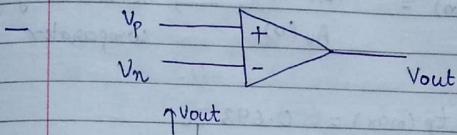
Page: _____
Date: _____

Ex:

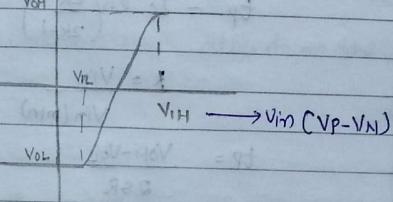


find the specifications of the circuit at -3 dB freq,
CMRR,

Allen Hawbaker
(chp-8) Comparators



static charc
of comparators



$V_p > V_n$; $V_{out} = +V_{sat}$ $\rightarrow 1$ logic

$V_p < V_n$; $V_{out} = -V_{sat}$ $\rightarrow 0$ logic

$$\text{open loop gain} = \frac{V_{thH} - V_{thL}}{V_{thH} - V_{thL}} = A_{v(0)} \rightarrow \text{dc gain}$$

propagation Delay \rightarrow time delay b/w provided input and getting the o/p

$$A_{vcc} = \text{closed loop gain} = \frac{A_{v(0)}}{S/\omega_c + 1}$$

$$= \frac{A_{v(0)}}{S/\omega_c + 1} \quad \rightarrow -3\text{dB freq.}$$

$\omega_c \rightarrow -3\text{dB frequency}$

resolution time \rightarrow resolution of the comp. means the minimum voltage difference b/w the input which can be detected by the comparator.

Resolution: $V_{in(min)} = \frac{V_{OH} - V_{OL}}{Av(0)}$ → sensitivity of the comparator

Propagation delay: $t_p(max) = 0.693 \tau_c$

$$t_p = \tau_c \ln\left(\frac{2K}{2K-1}\right)$$

$$K = \frac{V_{in}}{V_{in(min)}}$$

$$t_p = \frac{V_{OH} - V_{OL}}{2SR}$$

Ex: find the propagation delay for open loop comparator that has dominant pole at 10^3 rad/s, dc gain 10^4 , SR = 1 V/μs, binary O/P swing is $\pm 1V$. Assume i/p voltage = 10 mV.

Sol:

$$t_p = \frac{V_{OH} - V_{OL}}{2SR} \quad \tau_c = \frac{1}{10^3 \text{ rad/s}}$$

$$= \frac{10^{-6}}{10^{-4}} = 0.5 \text{ μsec}$$

$$\text{resolution} = \frac{1V}{10^4} = \frac{V_{OH} - V_{OL}}{Av(10)} = V_{in(min)}$$

$$\text{Or } t_p = \tau_c \ln\left(\frac{2K}{2K-1}\right)$$

$$K = \frac{10 \text{ mV}}{10^{-4}} = 10^2$$

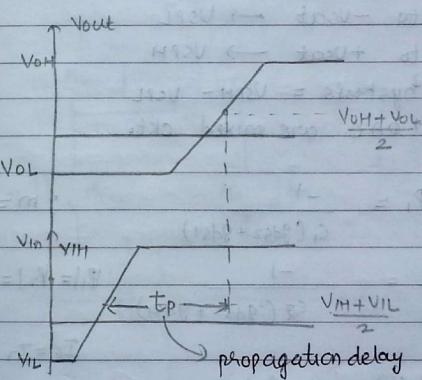
$$\tau_c = 10^{-3}$$

$$t_p = 0.5 \text{ μs}$$

$$t_p = 0.693 \tau_c$$

$$\text{max.} = 0.693 \cdot 10^{-3} \text{ ms}$$

- propagation delay depends on the \rightarrow actual i/p and min i/p provided or detectable resolution



- Two stage open-loop comparator

- advantage of CMOS $V_{OH} = V_{DD} \rightarrow \text{logic 1}$
 $V_{OL} = 0 \rightarrow \text{logic 0}$

and power dissipation is very less

- low speed

- Higher noise margin

Comparators in acme are CMOS, But till its not strong for logic 1 but strong for logic 0
 $V_{OH} = V_{DD} - (V_{DD} - V_{GS(\text{min})} - V_{TP}) \left[1 - \frac{2I_2}{R_2(V_{DD} - V_{TH} - V_{GS})} \right]$
 $V_{OL} = V_{SS}$

$$Av(0) = \left(\frac{g_{m1}}{g_{ds2} + g_{ds4}} \right) \left(\frac{g_{m2}}{g_{ds6} + g_{ds7}} \right)$$

- Zero crossing detector $V_{SPH} = V_{SPL}$
- $\{ +V_{SPL} \text{ to } -V_{SPL} \rightarrow V_{SPL}$
- $\{ -V_{SPL} \text{ to } +V_{SPL} \rightarrow V_{SPH}$
- $\text{hysteresis} = V_{SPH} - V_{SPL}$
- ADC and DAC are mixed ckt.

$$P_1 = \frac{-1}{C_1(g_{ds2} + g_{ds4})} \quad ; \quad m = \frac{P_2}{P_1}$$

$$\frac{I_2}{I_1} = \frac{2C_1}{C_2} \quad P_2 = \frac{-1}{C_2(g_{ds2} + g_{ds4})} \quad |P_1| = |P_2| = \frac{1}{2P_1\sqrt{mK}}$$

$$Av(s) = \frac{Av(0)}{(sP_1 + 1)(sP_2 + 1)} \quad I_2 = P_1 C_1$$

Based on propagation delay

linear
(non-slew)

$$t_p = \frac{2C \ln(2K)}{eK-1}$$

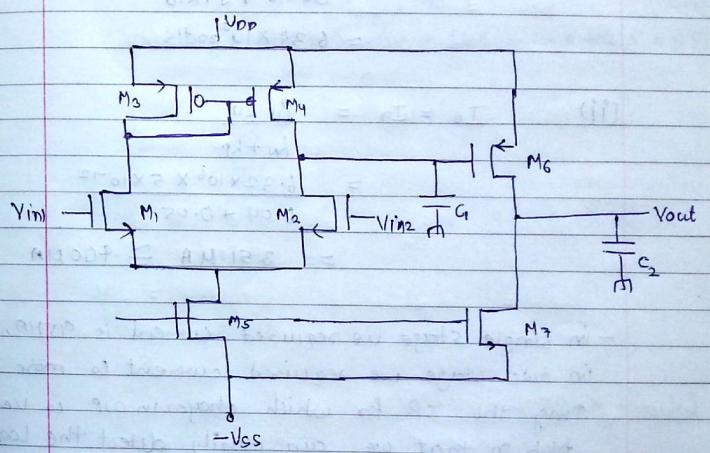
slew

I/P is changing at
very high speed then

Page: _____
 Date: _____
 6 - April

OIP changes does not
changes that much and
OIP changes exponentially
 $\Sigma p = \frac{V_{OH} - V_{OL}}{2SR}$

Two-Stage comparator with linear response



Ex: design a comp $t_p = 50\text{ns}$, $V_{DD} = 2.5\text{V}$,
 $V_{SS} = -2.5\text{V}$, $V_{OH} = 2\text{V}$, $V_{OL} = -2.5\text{V}$,
 $V_{in1\text{min}} = 1\text{mV}$, $V_{ICMR} = 2\text{V}$, $V_{OCMR} = -1.25\text{V}$
 $M = 1 \& K = 10$, dc Volt. gain $Av(0) = 4000$
 $C_1 = 0.2\text{ pF}$, $C_2 = 5\text{ pF}$

Sol: Non-inverting comparator (open loop)

$$m = \frac{P_2}{P_1} = 1$$

$$|P_1| = |P_2| = \frac{1}{t_p \sqrt{mK}}$$

$$|P_1| = |P_2| = \frac{1}{50 \times 10^{-6} \sqrt{1 \times 10}} = 6.32 \times 10^6 \text{ rad/s}$$

$$(ii) I_G = I_2 = \frac{P_{11} C_{11}}{h_n + h_p} = \frac{6.32 \times 10^6 \times 5 \times 10^{-12}}{0.04 + 0.05} = 351 \text{ mA} \approx 400 \text{ mA}$$

- in single stage we required current is 95mA, but in two stage we required current is more for turning the SR for which change in OIP is very high so that we can easily detect the logic 1 and 0.

$$(iii) \frac{w}{L}_6 = \frac{2 I_G}{K_p' (V_{DS6})^2} \text{ (sat. current for } M_6) = \frac{2 \times 400 \times 10^{-6}}{50 \times 10^{-6} (0.5)^2} = 64$$

($V_{GS} - V_T = V_{DS} \rightarrow bcoz$)

(VII)
for M_3 :

V_{GS3} using $ICMR$

$$V_{GS3} = V_{DD} + V_{TH} - V_{CM}$$

$$(V_{DD} = V_{DS3} + V_{DS1})$$

$$= 2.5 - 2 + 0.7$$

$$= 1.2 \text{ V}$$

$$I_3 = \frac{I_5}{2} = 20 \text{ mA}$$

$$\frac{2 \times 20 \text{ mA}}{50 \times (V_{GS3} - V_T)^2} \frac{w}{L}_3 = \frac{w}{L}_4 = 3.2 \approx 4$$

$$(1.2 - 0.7)$$

$$V_{DS6} = V_{out} - V_{DD}$$

$$= V_{OH} - V_{DD} = 2 - 2.5 = 0.5 \text{ V}$$

(max output volt is V_{OH})

$$\frac{w}{L}_7 = \frac{2 I_7}{K_n (V_{DS7})}$$

$$= \frac{2 \times 400 \times 10^{-6}}{110 \times 10^{-6} (0.5)^2} = 7.2 \approx 8$$

$$V_{DS7} = V_{OH} - V_{OL} - V_{SS} = -2 + 2.5 = 0.5 \text{ V}$$

$$\frac{w}{L}_7 = \frac{2 C_1}{C_{11}}$$

$$I_{S7} = \frac{400 \text{ mA} \times 2 \times 0.2}{5} = 32 \text{ mA} \approx 40 \text{ mA}$$

V_{GS3} using $ICMR$

$$V_{GS3} = V_{DD} + V_{TH} - V_{CM}$$

$$(V_{DD} = V_{DS3} + V_{DS1})$$

$$= 2.5 - 2 + 0.7$$

$$= 1.2 \text{ V}$$

$$I_3 = \frac{I_5}{2} = 20 \text{ mA}$$

$$\frac{2 \times 20 \text{ mA}}{50 \times (V_{GS3} - V_T)^2} \frac{w}{L}_3 = \frac{w}{L}_4 = 3.2 \approx 4$$

$$(1.2 - 0.7)$$

$$(VII) A_v(0) = \frac{g_m}{(g_{ds2} + g_{ds4})} \cdot \frac{g_m}{(g_{ds6} + g_{ds2})}$$

$$g_{m1} = \frac{I_{D1} \beta}{2 \times 400 \mu \times 50 \times 64 \times 10^{-6}} = 1.6 \times 10^{-3}$$

$$g_{ds6} = k_p I_6 = 0.05 \times 400 \mu = 20 \mu$$

$$g_{ds2} = k_p I_2 = 0.04 \times 20 \mu = 0.8 \mu$$

$$g_{ds4} = k_p I_4 = 20 \mu \times 0.05 = 1 \mu$$

$$4000 \times \frac{(1.6) \mu (36 \mu)}{1.6 \times 10^{-3}} = g_{m1}$$

$$g_{m1} = 1.6 \times 10^{-3}$$

$$g_{m2} = 2 I_1 k_p \left(\frac{w}{l}\right)$$

$$(1.6)^2 \times 10^{-6} = 2 \times 20 \mu \times 110 \times \left(\frac{w}{l}\right) \times 10^{-6}$$

$$\left(\frac{w}{l}\right)_1 = \frac{1.6 \times 10^{-3} \times 10^6}{2 \times 20 \mu \times 110} \approx 6$$

$$\begin{aligned} V_{DSS} &= V_{CM} - V_{GS1} - V_{SS} \\ &= -1.25 - 0.24 + 2.5 = 1.0 \text{ V} \\ V_{GS1} &= \sqrt{\frac{2 I_1}{\beta}} \\ &= \sqrt{\frac{2 \times 20 \mu}{110 \times 10^6 \times 6}} = 0.24 \text{ V} \end{aligned}$$

$$\begin{aligned} \text{So, } \frac{w}{l}_5 &= \frac{2 I_5}{k_n' \times (V_{DS})^2} \\ &= \frac{2 \times 40 \mu}{110 \times (1.0)^2 \times 10^{-6}} \\ &= 0.71 \end{aligned}$$

Tripp point \rightarrow Voltage at which logic 1 \rightarrow logic 0

$$V_{TRP} = V_{TN} + \sqrt{\frac{k_n(\omega L)_7}{k_p(\omega L)_6} (V_{DD} - V_{BIAS} - V_{TP1})}$$

$$\begin{aligned} (VII) V_{TRP} &= 0.7 + \sqrt{\frac{110 \times 0.9}{50 \times 64} (2.5 - 0.7)} \\ &= 0.49 \text{ V} \end{aligned}$$

Example

Calculate the performance of the comparator

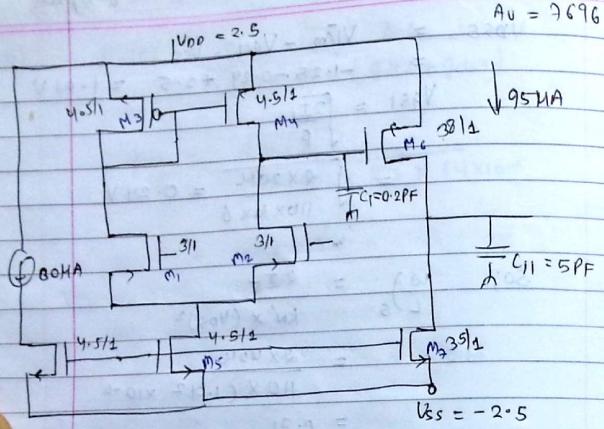
Calculate $A_v(0)$

$$C_1 = 0.2 \text{ pF}$$

$$C_2 = 5 \text{ pF}$$

$$t_p, V_{OH},$$

$$V_{OL}$$



$$\begin{aligned}
 & \text{assume } V_{G6} = 0 \\
 \text{So } V_{OH} &= V_{DD} - (V_{DD} - V_{G6} - |V_{TP1}|) \left[1 - \sqrt{1 - \frac{2I_1}{B_6 (V_{DD} - V_{G6} - |V_{TP1}|)}} \right] \\
 V_{OH} &= 2.5 - (2.5 - 0 - 0.4) \left[1 - \sqrt{1 - \frac{2 \times 95}{50 \times \frac{33}{1} (2.5 - 0.7)^2}} \right] \\
 &= 2.049 \text{ V}
 \end{aligned}$$

$$\text{ii) } \text{VOL} = \text{VOS} = -2.5V$$

$$111) F_{v(0)} = \frac{g_{m1} \cdot g_{m6}}{(g_{ds2} + g_{ds4}) (g_{ds6} + g_{ds7})}$$

assume $A(0) = 10^4$

$$p_1 = \frac{-1}{c_1(gds_2 + gds_4)}$$

$$P_2 = \frac{-1}{C_{11}(g_{elSG} + g_{AS2})}$$

$$q_{m1} = \sqrt{2 I_B P_1}$$

$$= \sqrt{2 \times 15 \text{ mA} \times 110 \text{ V}}$$

$$g_{m6} = \sqrt{2 I_B \beta_6} = \sqrt{2 \times 95 \times 50 \times 38} = 600.8 \text{ } \mu$$

$$g_{DS2} = k_n I_2 = 0.04 \times B_0 H = 0.6 H$$

$$gdsy = k_p I_y = 0.05 \times 15 \mu = 0.75 \mu$$

$$gds6 = h_p I_G = 0.05 \times 95 M = 0.75 M$$

$$gds7 = h_p I_7 = 0.04 \times 95 M = 3.8 M$$

$$SO, \quad p_1 = \frac{-1}{0.2 \times 10^{-12} (0.6 + 0.75) \times 10^{-6}}$$

$$P_{11} = \frac{-1}{5 \times 10^{-12} (4.95 + 3.8) \mu} =$$

$$\text{and } V_{in(\text{mm})} = \frac{V_{OH} - V_{OL}}{2}$$

$$= \frac{2.42 + 2.5}{7696} = 0.64 \text{ mV}$$

$$P_1 = 6.75 \times 10^6$$

$$P_{11} = 1.21 \times 10^6$$

Z_C is the dominant pole
which is appear first

$$m = \frac{P_2}{P_1}$$

(i) for diff input define calculate $t_p = ?$
 $V_{in} = 10mV, 100mV, 1V \rightarrow t_p = ?$

If $V_{in\min} = 0.64mV$

$$\frac{V_{in}}{V_{in\min}} = K = \frac{10mV}{0.64mV}$$

$$t_p = Z_C \ln \left(\frac{2K}{2K-1} \right)$$

i) non
slew rate
 $V_{in} = 10mV$

$$K = \frac{100mV}{0.64mV}$$

$$t_p = Z_C \ln \left(\frac{2K}{2K-1} \right)$$

ii) Skew rate
 $V_{in} = 1V$

$$t_p = \frac{V_{OH} - V_{OL}}{2SR} = \frac{4.92}{2 \times 19 \times 10^6} = 0.12 \mu s$$

$$SR = \frac{I_E}{C_{11}} = \frac{95 \mu A}{5pF} = 19 \times 10^6$$

in this if voltage is very much higher than the $V_{in\min}$ so our comparator will operate in the slew rate type and t_p is decided by the slew rate.

$$V_{TRP} = V_{TN} + \sqrt{\frac{K_n(\omega/L) + (V_{DD} - V_{TH})}{K_p(\omega/L)G}}$$

$$= 0.7 + \sqrt{\frac{110 \times 35}{50 \times 38}} (2.5 - 0.7)$$

$$= 3.26 V$$

12-April

Baker (Chp 26)

Comparator with hysteresis

↳ hysteresis

$$V_{in1} = V_{in2}$$

$$V_{SPL} = V_{SPH}$$

hysteresis loss = 0

switching point

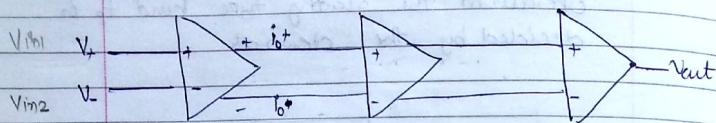
- if $V_{in1} = 2.5V$ AC sine wave

$V_{in2} = 3V$ dc value



then ckt will look as
amplifier, clipping part of some signal
is there.

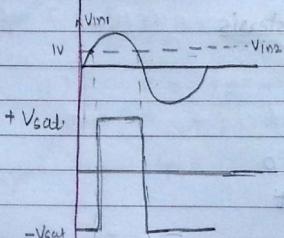
Three Stage Comparator



Be-
amplification
(differ voltage
converted into
differ current
with the help of
differ ampr)

Decision
circuit
(Positive
feedback)

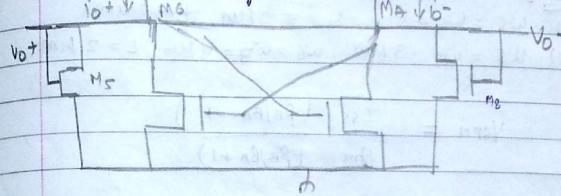
Post
amplification



- $V_{in1} > V_{in2} \rightarrow +V_{sat}$
- $V_{in1} < V_{in2} \rightarrow -V_{sat}$

- Switching is occur (means output change its logic state) when $V_{in1} = V_{in2}$, $i_{o+} = i_{o-}$

Decision making circuit



- if $i_{o+} > i_{o-}$ ($V_{o+} > V_{o-}$), then M_6 is in cut off & M_7 is in saturation region.
- this decide our switching point
if all the transistors M_5, M_6, M_7, M_8 having same W/L ratio, hysteresis = 0

$$V_{SPH} = V_+ - V_- = \frac{I_{SS}}{g_m} \frac{\frac{\beta_B}{\beta_A} - 1}{\frac{\beta_B}{\beta_A} + 1} \quad \beta_B \gg \beta_A$$

$$V_{SPL} = -V_{SPH}$$

$$i_{o-} = \frac{\beta_B}{2} (V_{o+} - V_{thn})^2 = \frac{\beta_B}{\beta_A} i_{o+}$$

- When $i_{o+} > i_{o-}$ ($M_6 \rightarrow$ cut off
 $M_5 \rightarrow$ ON
 $M_7 \rightarrow$ saturation
 $M_8 \rightarrow$ OFF)

- if $V_{SPH} \neq 0$, $V_{SPL} = -V_{SPH}$, then its having two slop points and with hysteresis

Example : Calculate the S/I Point.

- (i) $w_5 = w_6 = w_7 = w_8 = 3 \mu m$, $L = 2 \mu m$
 (ii) $w_5 = w_8 = 3 \mu m$, $w_6 = w_7 = 4 \mu m$, $L = 2 \mu m$

Sol:

$$V_{SPH} = \frac{I_{SS} (\beta_B/\beta_A - 1)}{g_m (\beta_B/\beta_A + 1)}$$

$$\text{i) When } \beta_B = 312$$

$$\beta_A = 312$$

$$V_{SPH} = 0$$

$$V_{SPL} = 0$$

$$\text{ii) } \beta_B = 412 ; I_{SS} = 20 \mu A$$

$$\beta_A = 312 ; g_m = 71 \mu A/V$$

$$V_{SPH} = \frac{I_{SS} \left(\frac{413 - 1}{413 + 1} \right)}{g_m}$$

$$= \frac{I_{SS}}{g_m} \left(\frac{413}{413} \right)$$

$$= \frac{1}{7} \left(\frac{20}{71} \right) = 40 \text{ mV}$$

$$V_{SPL} = -40 \text{ mV}$$

$$g_m = \frac{2 I_B}{w_L} = \frac{2 \times 50 \mu A \times 10}{2} \times 10 \mu A$$

- for tolerating the noise, we are using the comparator with hysteresis.

Example Design a Comparator, with $V_{RF} = 100 \text{ mV}$

$$I_{SS} = 20 \mu A$$

$$g_m = 71 \mu A/V$$

$$V_{SPH} = \frac{20}{71} \left(\frac{\beta_B/\beta_A - 1}{\beta_B/\beta_A + 1} \right) = 100 \text{ mV}$$

$$\frac{\beta_B/\beta_A - 1}{\beta_B/\beta_A + 1} = 355 \left(\frac{\beta_B}{\beta_A} + 1 \right)$$

$$(1 - 355) \frac{\beta_B}{\beta_A} = 356$$

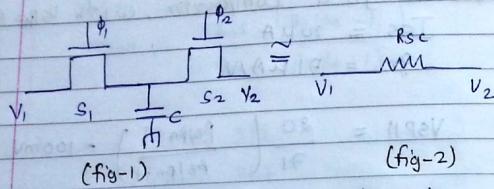
$$\frac{\beta_B}{\beta_A} = 1.005$$

13-April

Switched Capacitor

Page: _____
Date: _____
(Baker) (329)

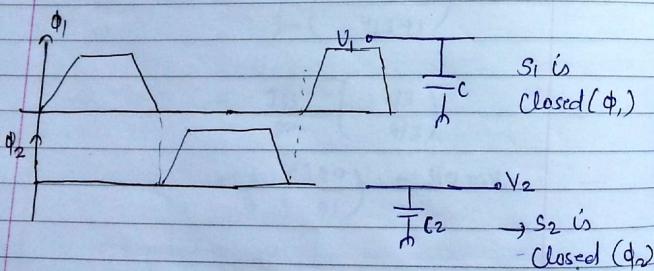
- two SW and one capacitor \rightarrow resistors and they are discrete in nature.



non-overlapping clocks are ϕ_1 & ϕ_2

- When Resistor are using:- can chip)

- size will \propto τ_{res} (device)
- Power loss is there (I^2R), bcoz \propto τ_{res} . So continuous supply powers the current
- temp will \propto τ_{res} .



$$q_1 = CV_1$$

$$q_2 = \frac{1}{2} C V_2$$

$$q_1 - q_2 = C(V_1 - V_2)$$

$$(fig-1) \quad I_{avg.} = \frac{dq}{dt} = \frac{C(V_1 - V_2)}{T} \quad \text{--- (1)}$$

$$(fig-2) \quad I_{avg.} = \frac{V_1 - V_2}{R_{sc}} \quad \text{--- (2)}$$

$$\Rightarrow R_{sc} = \frac{T}{C}$$

$T \rightarrow 1/f_{clk} \rightarrow$ Clock freq.

$$R_{sc} = \frac{1}{C f_{clk}}$$

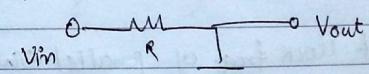
$\left\{ \begin{array}{l} \text{continuous time ckt.} \rightarrow \text{discrete time ckt.} \\ R_{sc} \rightarrow 2 \text{ SW} + 1 \text{ cap.} \end{array} \right.$

$f_{clk} \geq 10$ fsignal

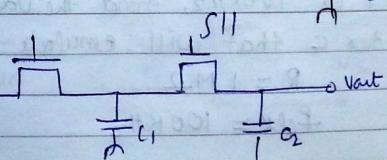
Freq. of information signal

Example:

$RC = 1 \text{ ms}$; 3dB freq. of V_{out}/V_{in} is 159 Hz. By using SW capacitor, implement the ckt.



Sol:-



$$RC_2 = \frac{C_2}{C_1 \cdot f_{CLK}}$$

$$R = \frac{1}{C f_{CLK}}$$

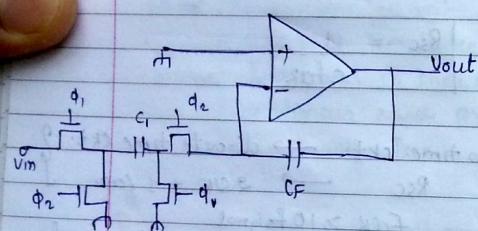
$$C = \frac{1}{R \cdot f_{CLK}}$$

$$= \frac{1}{10^6 \times 100 \times 10^3}$$

$$= 10^{-11}$$

$$C = 10 \text{ pF}$$

⇒ Switched capacitor integrators



$$\frac{V_{out}}{V_{in}} = \frac{1/j\omega C_F}{R_{sc}} = \frac{1}{j\omega \left(\frac{C_F \cdot 1}{C_1 \cdot f_{CLK}} \right)}$$

Ex: If clock freq. of parallel SW cap. equivalent resistor is 100 kHz, find the value of the capacitor C that will emulate 1 MΩ resistor.

Sol:

$$R = 1 \text{ M}\Omega$$

$$f_{CLK} = 100 \text{ kHz}$$

if $R = 10 \text{ k}\Omega$

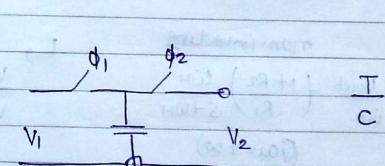
$$C = \frac{1}{10 \times 10^3 \times 10^5}$$

$$= 10^{-10}$$

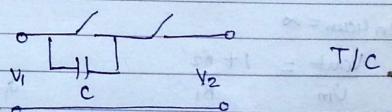
$$= 100 \text{ pF}$$

⇒

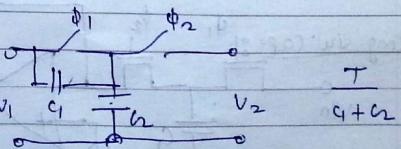
① parallel

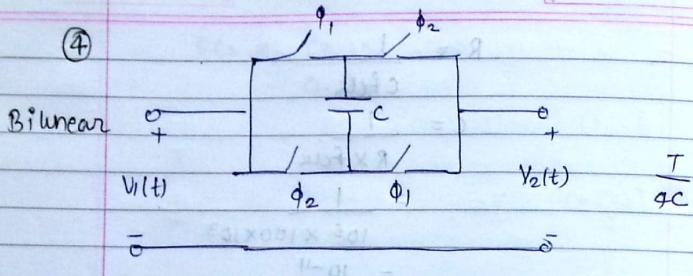


② series



③ series-parallel



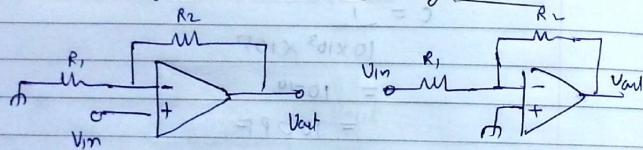


feedback (+ve) \rightarrow Smitch trigger
u (-ve) \rightarrow amplifier

$$H(z) = -\frac{C_1}{C_2} (e^{-j\omega t})$$

$$= -\frac{C_1}{C_2} z^{-1}$$

\Rightarrow Inverting and non-inverting amplifier



non-inverting

$$\frac{V_{out}}{V_{in}} = \left(1 + \frac{R_2}{R_1}\right) \frac{W_H}{S + W_H}$$

(Gain $\neq \infty$)

inverting

$$\frac{V_{out}}{V_{in}} = -\left(\frac{R_2}{R_1}\right) \frac{W_H}{S + W_H}$$

($G_B = \infty$, Gain $\neq \infty$)

When $G_{out} = \infty$

$$\frac{V_{out}}{V_{in}} = 1 + \frac{R_2}{R_1}$$

$$\frac{V_{out}}{V_{in}} = -\frac{R_2}{R_1}$$

