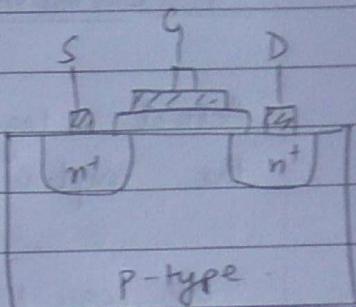
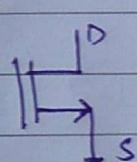


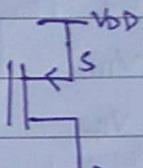
3/17
NMOS transistor \rightarrow n-channel
enhancement n-channel MOS
depletion " "



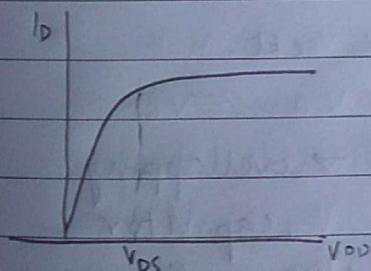
pMOS transistor \rightarrow p-channel



Sinking current



Source current



$w \& L \rightarrow$ depends on technology

cutoff
linear

$$I_D = 0$$

$$I_D = \frac{\mu_n C_{ox}}{2} \left(\frac{W}{L} \right) [2(V_{GS} - V_T) V_{DS} - V_{DS}^2]$$

$$V_{GS} < V_T$$

$$V_{GS} \geq V_T$$

$$V_{DS} < V_{GS} - V_T$$

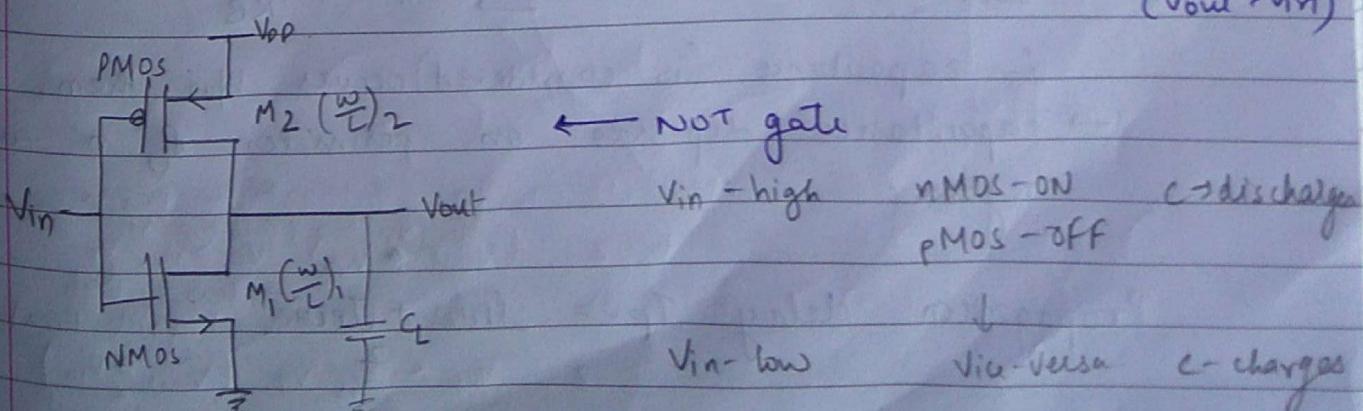
$$(V_{out} < V_{in})$$

Saturation

$$I_D = \frac{\mu_n C_{ox}}{2} \left(\frac{W}{L} \right) (V_{GS} - V_T)^2 (1 + dV_{DS}) \quad V_{GS} \geq V_T$$

$$V_{DS} \geq V_{GS} - V_T$$

$$(V_{out} > V_{in})$$



7 COMBINATIONAL LOGIC CIRCUITS

Actual logic 1 & logic 0 - of the values in
the implemented Transistor level logic circuit.

city logo 1 - York

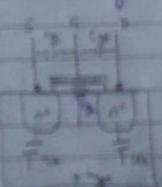
at large 0 - 100

3.16 logic 1 = via

~~After~~ ~~long~~ 0 = Vile

$$\text{NMM} = V_{10} - V_{20}$$

More white margin → better logic etc

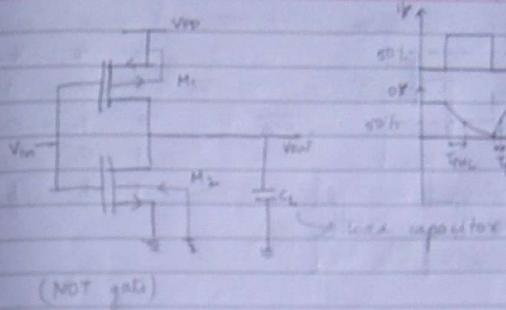


$C_{\text{S}} \subseteq C_{\text{A}} \rightarrow$ overlapping
capacitor

$C_{ab}, C_{ba} \rightarrow$ bulk capacitor

Parasitic bacteria are now created by
cause to multiply and again by synthesis
→ when bacteria conduct

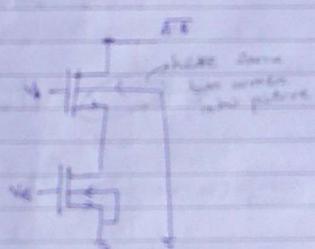
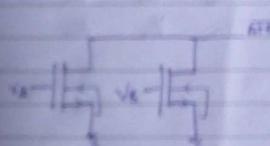
source - quadrupole Alode \rightarrow source in FB
 due to it \rightarrow " " " " \rightarrow FB
 i.e. capacitive (as considered) current flows there
 \rightarrow Inductance depends on parameter θ of same region



$$T_{\text{rise}} = \frac{C_{\text{load}} \times (V_{\text{out}} - V_{\text{sat}})}{I_{\text{avg rise}}}$$

→ 2 中 NER GATE

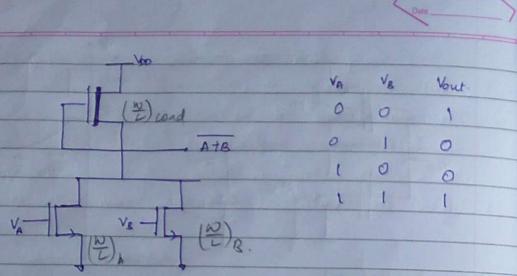
depiction in MS. as a lead



$$Y_1 = Y_{\text{obs}} + \mathbf{Y} \left(\frac{\text{true value} - \text{observed}}{\sqrt{\text{true variance}}} \right)$$

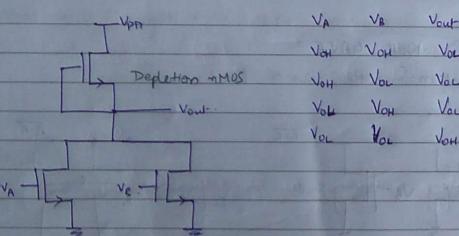
334

卷之三

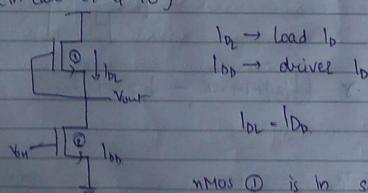


V_A	V_B	V_out
0	0	1
0	1	0
1	0	0
1	1	1

$$K_R = \frac{k_{n\text{driver}}}{k_{n\text{load}}}$$



case-1 (in case $V_A > V_{DS} & V_A < V_DDS$)



nMOS ① is in saturation region
bcz $(V_{out} > V_{DS}) \quad V_{DS} > V_{GS} - V_T$

nMOS ② is in linear region
bcz $V_{DS} < V_{GS} - V_T \quad (V_{out} > V_{DS})$

$$\begin{aligned} \text{load} \quad I_{DL} &= \frac{1}{2} k_n C_o x \left(\frac{W}{L} \right)_L (V_{GS} - V_T)^2 \\ &= \frac{k_n C_o x}{2} \left(\frac{W}{L} \right)_L V_T^2 \quad (\because V_{GS} = 0) \quad \text{--- ①} \end{aligned}$$

$$\begin{aligned} \text{driver} \quad I_{D_D} &= \frac{k_n C_o x}{2} \left(\frac{W}{L} \right)_D [2(V_{GS} - V_T)V_{DS} - V_{DS}^2] \\ &= \frac{k_n C_o x}{2} \left(\frac{W}{L} \right)_D [2(V_{GS} - V_T)V_{DS} - V_{DS}^2] \quad \text{--- ②} \end{aligned}$$

$$I_{D_D} = I_{DL}$$

$$\left(\frac{W}{L} \right)_D V_T^2 = \left(\frac{W}{L} \right)_D [2(V_{GS} - V_T)V_{DS} - V_{DS}^2]$$

$$\left(\frac{W}{L} \right)_D V_T^2 + V_{DS}^2 - 2(V_{GS} - V_T)V_{DS} = 0.$$

$$x = -b \pm \sqrt{b^2 - 4ac} \quad a = 1 \quad b = -2(V_{GS} - V_T) \quad c = \left(\frac{W}{L} \right)_D V_T^2$$

$$V_{DS} = \frac{-b \pm \sqrt{(V_{GS} - V_T)^2 - 4 \left(\frac{W}{L} \right)_D V_T^2}}{2 \left(\frac{W}{L} \right)_D}$$

$$V_{DS} = (V_{GS} - V_T) \pm \sqrt{(V_{GS} - V_T)^2 - \left(\frac{W}{L} \right)_D V_T^2}$$

If $\left(\frac{W}{L} \right)_D V_T^2 \rightarrow$ should be as small as possible

then $V_{DS} = 0$ (required value)

[when (-) is considered]

$\left(\frac{w}{l}\right)_L = \left(\frac{w}{l}\right)_D \rightarrow$ will provide strong 0, i.e., the value V_{OL} will be more nearer to 0.

- CMOS logic has high noise margin so advisable even though more no. of transistors are required.

Case-2 when $V_A = V_{OH}$ $V_B = V_{OL}$

$$\text{then } I_{OL} = I_{O1} + I_{O2}$$

$$V_{OL} = (V_{OH} - V_T) - \sqrt{(V_{OH} - V_T)^2 - \left(\frac{w}{l}\right)_L V_T^2} / \left(\frac{w}{l}\right)_D + \left(\frac{w}{l}\right)_D$$

$\left(\frac{w}{l}\right)_L = \left(\frac{w}{l}\right)_D = \left(\frac{w}{l}\right)_B \rightarrow V_{OL}$ will be nearer to 0.

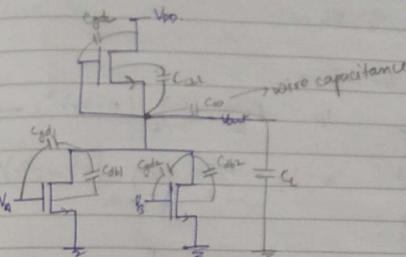
Case-3 when $V_A = 0$ $V_B = 0$

then load transistor is in saturation region.

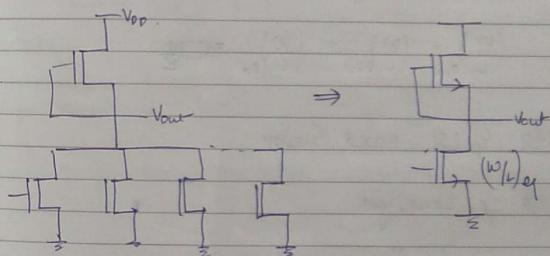
TRANSIENT ANALYSIS

→ Wire capacitance → occurs in IC's where the wire used to connect transistors can cause capacitance b/w two wires taking air as dielectric.

$$C_{off} = C_w + C_{gd1} + C_{gd2} + C_{gdL} + C_{db1} + C_{db2} + C_{sbL} + C_L$$



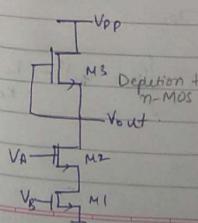
2 i/p NOR gate \rightarrow n i/p NOR gate



$$\left(\frac{w}{l}\right)_{eq} = \sum_{n=1}^k \left(\frac{w}{l}\right)_n$$

$C_{eq} = n k L$,
if all nmos
has same $(w/l) = k$

NAND



V_A	V_B	V_{out}	$0 - V_{OH}$
0	0	1	$1 - V_{OH}$
0	1	1	
1	0	1	
1	1	0	

when $V_A = V_S = V_{OH}$

$$I_{D1} = I_{D2} = I_{DL}$$

$$I_{D1} = \frac{k_{unox}}{2} \left(\frac{W}{L} \right)_{D1} (0 - V_T)^2 \quad \text{--- 1.}$$

$$I_{D1} = I_{D2} = \frac{k_{unox}}{2} \left(\frac{W}{L} \right)_{D1=D2} \left[2(V_{OH} - V_T)V_{OL} - V_{OL}^2 \right] \quad \text{--- 2.}$$

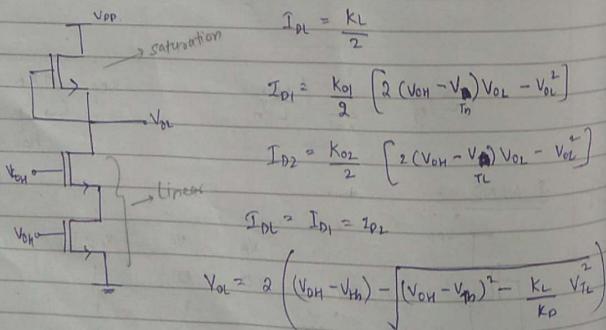
$$\therefore V_{OL} = (V_{OH} - V_T) - \sqrt{(V_{OH} - V_T)^2 - \left(\frac{W}{L} \right)_{D1=D2} V_T^2}$$

For n i/p NAND gate

$$\left(\frac{W}{L} \right)_{D1} = \left(\frac{W}{L} \right)_{D2} = \dots = \left(\frac{W}{L} \right)_{Dn}$$

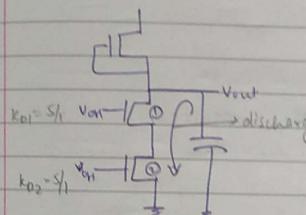
MSI & LSI Based Design.

& I_P NAND gate



$$I_P = \frac{I_{D1} + I_{D2}}{2}$$

Here, V_{OH} is given to both the transistors so there will be some variations in I_P due to it. \Rightarrow average is taken when discharging current is considered.



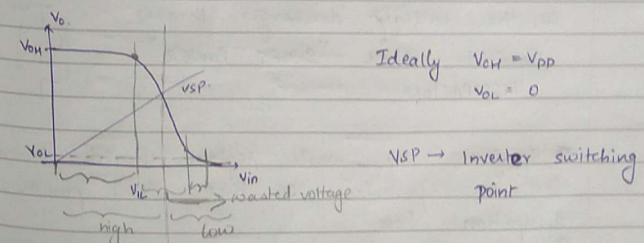
$$I_D = \frac{k_D}{4} (2(V_{DD} - V_T)V_{OL} - V_{OL}^2)$$

Also $V_{DS1} = V_{OL}$
 $V_{DS2} \rightarrow$ will be different.

$$\Rightarrow K_{eq} = \frac{k_D}{2} = \frac{2.5}{1} \quad (\frac{W}{L}) = K_D \rightarrow \text{driver ratio / aspect ratio.}$$

for n i/p nand gate $\rightarrow K_{eq} = \frac{k_D}{n}$

n i/p nor gate $\rightarrow K_{eq} = n K_D$



Ideally $V_{OH} = V_{DD}$
 $V_{OL} = 0$

VSP \rightarrow Inverter switching point

$$N_{ML} = V_{IL} - V_{OL}$$

$$N_{MH} = V_{OH} - V_{IH}$$

Noise Margin is \Leftarrow whole range of \Leftarrow $N_{ML} = N_{MH} = \frac{V_{DD}}{2}$ (while designing)
I/P is useful
(provided by \Rightarrow)

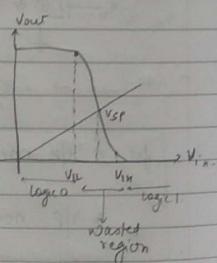
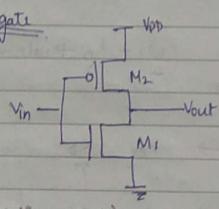
- Noise margin should be high
- This is achieved when the transition from high to low is steep (or a vertical line)

14/2

CMOS LOGIC

- $V_{OH} = V_{DD}$ \rightarrow logic 1
- $V_{OL} = 0$ \rightarrow logic 0
- Double no. of transistors required.

NOT gate



At V_{SP} , $V_{out} = V_{in}$
↑ not required.

↳ bcoz all the transistors are in saturation.

So, the battery discharges through $\frac{V_{DD}}{2}$ this path.
This is called "SHORT POWER DISSIPATION".

Therefore, the waste region should be as less as possible so that short power dissipation \downarrow .

Secondly, the noise margin \uparrow when waste region \downarrow .

$$NML = V_{IL} - V_{OL} = \frac{V_{DD}}{2}$$

$$NMH = V_{OH} - V_{IH} = V_{DD} - \frac{V_{DD}}{2} = \frac{V_{DD}}{2}$$

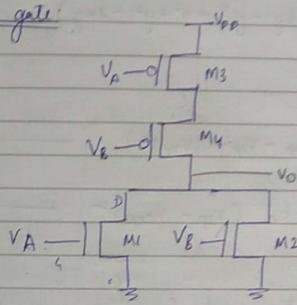
TB Notation:

$$f \rightarrow K$$

$$V_{SP} \rightarrow V_{th}$$

- Slope of curve should be as steep as possible to achieve these conditions.
 $\Rightarrow V_{sp} \approx V_{DD}/2$

NOR gate:



$$V_{eq} = w_1 + w_2 = 2w \quad (w_1 = w_2)$$

$$\Rightarrow \beta_1 + \beta_2 = 2\beta \quad (\beta_1 = \beta_2)$$

$$\beta = \mu_n C_o \frac{W}{L} \quad (\text{Transconductance})$$

When $L \downarrow \beta \downarrow$, i.e., $I_{eq} = L_3 + L_4 = 2L$
 $\Rightarrow \beta$ becomes half.

$$I_D = I_{D1} + I_{D2}$$

$$I_{D3} = I_{D4} \rightarrow \text{current gets half}$$

$$I_D = \frac{I_{D1} + I_{D2}}{2}$$

- Assume $V_A = V_{SP}$ $V_B = V_{SP} \Rightarrow V_O = V_{SP}$

M_1 and M_2 are in saturation.

$$\therefore I_{D1} = I_{D2} = \frac{k_p}{2} (V_{SP} - V_{THN})^2$$

M_3 in linear and M_4 in saturation

$$I_{D3} = \frac{k_p}{2} [2(V_{DD} - V_{SP} - |V_{TFL}|) V_{SP} - V_{SP}^2]$$

$$I_{D4} = \frac{k_p}{2} [V_{DD} - V_{SP} - |V_{TFL}| - V_{SP}]^2$$

$$\text{Let } x = V_{DD} - V_{SP} - |V_{TFL}|$$

$$y = V_{SP}$$

$$I_D = \frac{I_{D1} + I_{D2}}{2}$$

$$= \frac{k_p/2 (2xy - y^2) + k_p/2 (x-y)^2}{2}$$

$$= \frac{k_p}{4} (2xy - y^2 + x^2 + y^2 - 2xy)$$

$$= \frac{k_p}{4} x^2$$

$$I_D = \frac{k_p}{4} (V_{DD} - V_{SP} - |V_{TP}|^2) \quad \text{--- (1)}$$

$$I_D = I_{D1} + I_{D2} = k_n (V_{SP} - V_{THN})^2 \quad \text{--- (2)}$$

$$(1) = (2)$$

$$k_n (V_{SP} - V_{THN})^2 = \frac{k_p}{4} (V_{DD} - V_{SP} - |V_{TP}|^2)^2$$

$$(V_{SP} - V_{THN})^2 = \frac{k_p}{4k_n} (V_{DD} - V_{SP} - |V_{TP}|^2)^2$$

$$V_{SP} - V_{THN} = \sqrt{\frac{k_p}{4k_n}} (V_{DD} - V_{SP} - |V_{TP}|)$$

$$V_{SP} + \sqrt{\frac{k_p}{4k_n}} V_{SP} = V_{THN} + \sqrt{\frac{k_p}{4k_n}} (V_{DD} - V_{TP})$$

(for 2 input $\rightarrow N=4$,
i.e. n input $\rightarrow N$)

\rightarrow no of inputs.

$$V_{SP} + \sqrt{\frac{k_p}{N^2 k_n}} V_{SP} = V_{THN} + \sqrt{\frac{k_p}{N^2 k_n}} (V_{DD} - |V_{TP}|)$$

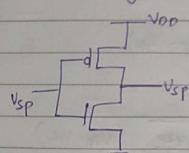
$$V_{SP} = V_{THN} + \sqrt{\frac{k_p}{N^2 k_n}} (V_{DD} - |V_{TP}|)$$

$$1 + \sqrt{\frac{k_p}{N^2 k_n}}$$

For NAND gate

$$V_{SP} = V_{THN} + \frac{\sqrt{\frac{k_p N^2}{k_n}} (V_{DD} - |V_{TP}|)}{1 + \sqrt{\frac{k_p N^2}{k_n}}}$$

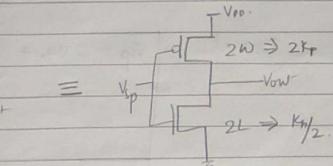
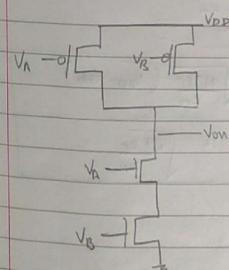
For NOT gate



$$\frac{k_n}{2} (V_{SP} - V_{THN})^2 = \frac{k_p}{2} (V_{DD} - |V_{TP}| - V_{SP})^2$$

$$V_{SP} = V_{THN} + \frac{\sqrt{\frac{k_p}{k_n}} (V_{DD} - |V_{TP}| - V_{SP})}{1 + \sqrt{\frac{k_p}{k_n}}}$$

Cmos NAND gate.

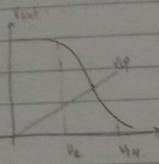


$$\therefore \frac{k_p}{k_n} = \frac{2k_p}{kn/2} = \frac{4k_p}{kn}$$

$$I_{DN} = \frac{k_n}{4} (V_{SP} - V_{TH})^2$$

$$I_{DP} = \frac{2k_p}{2} (V_{DD} - V_{SP} - V_{TH})^2$$

$$\frac{I_{Dn}}{I_{Dp}} = \frac{V_{Dp} - V_{Th}}{V_{Dp} - V_{Th} + 2(V_{DD} - V_{Dp})}$$



$$\text{Transconductance} = \frac{I_D}{V_{GS}}$$

$$I_D \propto W$$

$$(V_{Dp} - V_{Th}) = \sqrt{\frac{4kT}{kn}} (V_{DD} - V_{Dp} - V_{Th})$$

$$V_{Dp} \left(1 + \sqrt{\frac{4kT}{kn}} \right) = V_{Th} + \sqrt{\frac{4kT}{kn}} (V_{DD} - V_{Th})$$

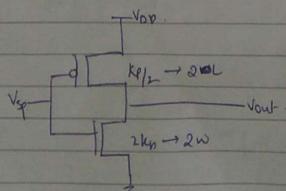
$$\therefore V_{Dp} = \frac{V_{Th} + \sqrt{\frac{4kT}{kn}} (V_{DD} - V_{Th})}{1 + \sqrt{\frac{4kT}{kn}}}$$

general

$$V_{Dp} = V_{Th} + \frac{N^2 kT}{kn} (V_{DD} - V_{Th})$$

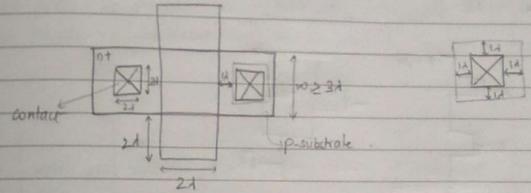
$$1 + \sqrt{\frac{N^2 kT}{kn}}$$

NOR



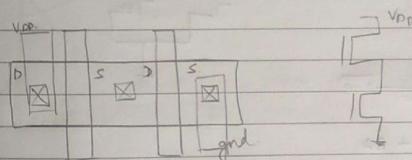
(equivalent ckt of NOR).

Layout of CMOS logic

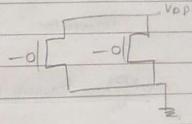
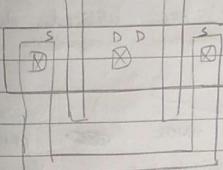


$L = \frac{d}{2}$ → Technology minimum feature size

$$d = \frac{0.18 \mu}{2} \quad (\text{lambda Rule})$$



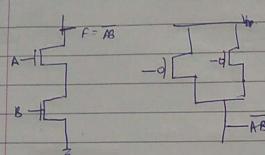
n-well.



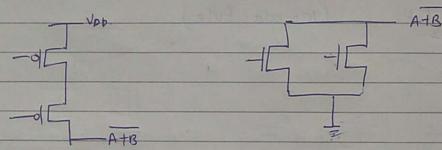
Capacitive effect in CMOS

CMOS Complex gate

$\rightarrow \bar{A}\bar{B}$



$\rightarrow \bar{A} + B$

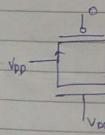


$\rightarrow F = \bar{A}\bar{B} + BA$

2/2/19

Euler's Path \rightarrow A common path in nMOS and pMOS transistors such that area utilized decreased.

CMOS transmission gate



nMOS ~~V_{DD}~~

$$V_{DSn} = V_{DD} - V_{out}$$

$$V_{GSn} = V_{DD} - V_{out}$$

$\therefore V_{GSn} = V_{DSn}$

\Rightarrow nMOS is in saturation when $(V_{out} = 0)$

pMOS

$$V_{DSp} = V_{out} - V_{DD}$$

$$V_{GSp} = -V_{DD}$$

pMOS in saturation when $(V_{out} = 0)$

nMOS

$$V_{GS} > V_T$$

$$V_{DS} \geq V_{GS} - V_T \rightarrow \text{sat.}$$

$$V_{DS} < V_{GS} - V_T \rightarrow \text{linear}$$

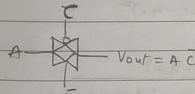
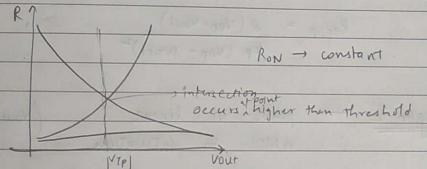
pMOS

$$V_{GS} < V_T$$

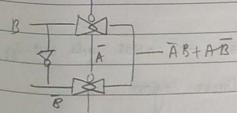
$$V_{DS} > V_{GS} - V_T \rightarrow \text{linear}$$

$$V_{DS} \leq V_{GS} - V_T \rightarrow \text{sat.}$$

R1	R2	R3	
nMOS	nMOS-sat	nMOS	
pMOS in saturation	pMOS-linear	- v_{offb}	
		pMOS	
		- linear	
			$V_{DD} = 5V$
	1V	4V	5V
			V_{out}



$$\bar{A} + A\bar{B}$$



$$K_n > (0.25 K_p)$$

$$\begin{aligned} R_{eq,n} &= \frac{V_{DD} - V_{out}}{I_{DS,n}} \\ R_{eq,p} &= \frac{V_{DD} - V_{out}}{I_{DS,p}} \end{aligned}$$

} → large signal resistance

Region-1 → pMOS and nMOS in saturation region

$$R_{eq,n} = \frac{2(V_{DD} - V_{out})}{k_n (V_{DD} - V_{out} - V_{t,n})^2}$$

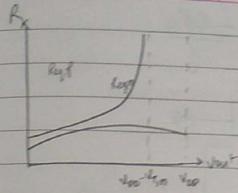
$$R_{eq,p} = \frac{2(V_{DD} - V_{out})}{k_p (V_{DD} - V_{out})^2}$$

Region-2 → pMOS in linear
nMOS in saturation ($V_{out} > V_{t,p}$)

$$R_{eq,n} = \frac{2(V_{DD} - V_{out})}{k_n (V_{DD} - V_{out} - V_{t,n})^2}$$

$$\begin{aligned} R_{eq,p} &= \frac{2(V_{DD} - V_{out})}{k_p [2(V_{DD} - |V_{t,p}|) (V_{DD} - V_{out}) - (V_{DD} - V_{out})^2]} \\ &= \frac{2(V_{DD} - V_{out})}{k_p [2(V_{DD} - V_{t,p}) - (V_{DD} - V_{out})]} \end{aligned}$$

Region-3 → let $V_{DD} = 5V$.
 $V_{out} > 4.75V \Rightarrow$ nMOS gate cut-off
pMOS in linear region



C Complementary Pass-transistor logic (CPL)

Only nMOS are used.

All i/p's are in complementary form.

- Static power dissipation for CMOS logic is zero as when i/p is 0 → PMOS is on and when i/p is 1 → nMOS is on ⇒ never short circuit occurs, i.e., when V_{in} and V_{out} is connected directly ⇒ no leakage current.

Whereas in CPL → power dissipation occurs.

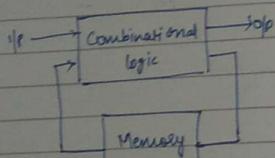
In CPL → area required is less

logic 1 and 0 are not ideal, i.e.,

$V_{out} = V_{DD}$ but $V_{out} \neq 0$ instead it is 0.02...

while in CMOS V_{out} and V_{in} values are ideal.

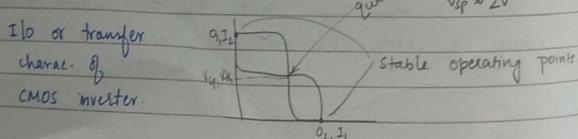
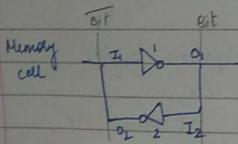
Sequential Logic



Present IP depends on -
 → present IP
 → reg. of previously stored IP

Sequential Logic

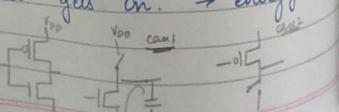
bistable Monostable Asymmetrical



$$\text{loop gain} = \frac{\partial P_1}{\partial P_1} \times \frac{\partial P_2}{\partial P_2} = \frac{1}{0} \times \frac{0}{1} = 0.$$

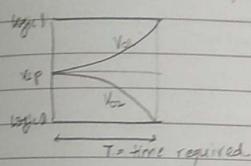
⇒ Loop gain at stable operating point is very low.

- V_{DD} to ground path is not shorted as at any instant only one cell gets on. → energy consumption is low.

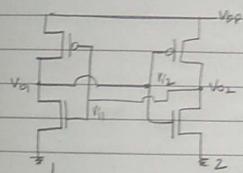


$$\text{if } V_{DD} = 2.5 \text{ then } \overline{S} = 0.5$$

A small deviation from 3.5 will cause change in IP.



$$\begin{aligned} 1^{\text{st}} \text{ IP rise} &\rightarrow 1^{\text{st}} \text{ IP } \downarrow \\ 2^{\text{nd}} \text{ IP fall} &\rightarrow 2^{\text{nd}} \text{ IP } \downarrow \end{aligned}$$



$$\begin{aligned} V_{D1} &= V_{d1} & V_{D2} &= V_{d2} \\ V_{g1} &= V_{i1} & V_{g2} &= V_{i2} \\ V_{D1} &= g_m V_{g1} & V_{D2} &= g_m V_{g2} \end{aligned}$$

$$V_{g1} = \frac{q_1}{C_g} \quad V_{g2} = \frac{q_2}{C_g}$$

$$I_{d1} = g_m V_{g1}, \quad I_{d2} = g_m V_{g2}$$

$$I_{d1} = I_{g2}, \quad I_{d2} = I_{g1}$$

$$\therefore I_{g1} = g_m V_{g2} = g_m \left(\frac{q_2}{C_g} \right)$$

$$I_{g2} = g_m V_{g1} = g_m \left(\frac{q_1}{C_g} \right)$$

$$I_{g1} = C_g \frac{dV_{g1}}{dt}, \quad I_{g2} = C_g \frac{dV_{g2}}{dt}$$

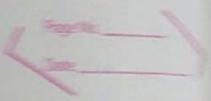
$$g_m V_{g2} = C_g \frac{dV_{g1}}{dt}$$

$$g_m V_{g1} = C_g \frac{dV_{g2}}{dt}$$

$$g_m \frac{q_2}{C_g} = C_g \frac{d(q_1/C_g)}{dt}$$

$$g_m \frac{q_1}{C_g} = \frac{d q_2}{dt}$$

$$g_m \frac{q_2}{C_g} = \frac{d q_1}{dt}$$



CMOS has speed compared to NMOS.

- area occupation is high
- noise margin is high

SCALING IN MOSFET

Ex:

Practically $\alpha = 1$, its not always fixed.
not can scale by any factor.

Constant field scaling (full scaling)

Ex: If E_x and E_y field will be constant

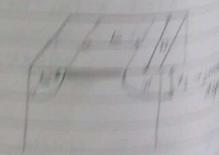
$$\frac{E_x}{E_x} = \frac{L_x}{L_x} = \frac{t_x}{t_x}$$

$$\frac{E_y}{E_y} = \frac{L_y}{L_y} = \frac{t_y}{t_y}$$

$$\text{constant } \left(\frac{E_x}{E_x} \right) = \frac{t_x}{t_x} \quad \text{constant } \left(\frac{E_y}{E_y} \right) = \frac{t_y}{t_y}$$

$E_y = k E_x$
that represents effect just after
of change in effect

Power would scale down by 8



$$C_{xy} = \frac{\epsilon_0}{t_x} = \frac{\epsilon_0 A_x}{t_x} \quad \text{more charge can be stored.}$$

$$T_{ch} = \frac{V_{DD}}{2} \times \frac{1}{2} \left(t_{DD} - t_x - t_y \right) \quad t_{DD} = \frac{2V_{DD}}{f}$$

$$T_{ch}' = \frac{V_{DD}}{2} \times \frac{1}{2} \left(t_{DD} - t_x \right)^2 = \frac{T_{ch}}{8}$$

$$\frac{\text{Static}}{\text{Initial}} = \frac{P'}{P} = \frac{1}{8} = \frac{1}{k^2} = \frac{1}{8}$$

$$C_y = \frac{\epsilon_0}{t_y} = \frac{\epsilon_0 A_y}{t_y} \quad \text{more charge can be stored.}$$

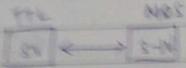
$$\left(\frac{P_{ch}}{P} \right) = \frac{P_{ch}}{P_{ch}} = \frac{8}{8} = 1 \quad \text{constant scaling for each.}$$

$$\text{Power } \left(\frac{P}{P} \right)' = \frac{V_{DD}}{t_{DD}} = \frac{P}{P} \quad \text{constant power for each cell.}$$

- 1. As t_x increases \Rightarrow charging & discharging time \propto time of capacitor \propto speed \propto
- 1. Power \propto time \Rightarrow more becomes less power density.
- 1. Scaling of t_x and t_y will have effect on power but no effect there is no effect time \propto power is not present in formula.
- 1. t_y remains same \Rightarrow Power is not effected \propto t_x \propto t_y \propto t_x

Advantages:
heat dissipation \downarrow
power dissipation \downarrow
switching speed \uparrow

DEMONSTRATION

Typical mapping becomes difficult as more circuits are required to make them compatible.

 \Rightarrow lower & hardware fix

So we need to keep voltage constant \Rightarrow this mapping problem won't occur.

I Constant voltage scaling

$\frac{V_D}{V_S}$

$$N_D = S^2 N_D$$

$$N_S = S^2 N_S$$

$$n^2 = \frac{N_D}{N_S}$$

$$C = 4/S$$

$$L_D = 4S^2/S$$

$$X_D = 8S^2/S$$

scaled by S^2 so that
 \in current change

$$C_{D'} = S^2 C_D \quad C_S = C_S/S \rightarrow S^2 \text{ less as S is less}$$

$$I_{D'} = S I_D$$

$$I_S = S I_S$$

$\therefore I_{D'} \leq I_D$ \Rightarrow speed ↑

$$P = S^2$$

$$B_D = S^2 B_D \quad \Rightarrow \text{more heat is generated}$$

$$B_S = S^2 B_S \quad \Rightarrow \text{relaxing time come in}$$

constant with generation and

$\frac{V_D}{V_S}$

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- Normally, people are using constant field scaling. \Rightarrow in 1 wafer whole ckt is built
- Constant voltage scaling is used when many devices are used and they work at different V_{DD}.

e.g. For a MOSFET device, scaling is to be performed. The power density of the scaled device is 8 unit which was 2 unit before scaling. If the saturation current was 3mA and substrate doping density was 10^{16} pec/cm³, then find out saturation drain current and substrate doping density after scaling of device

$$\left(\frac{P}{A}\right) = 8 \quad \left(\frac{P}{A}\right) = 2 \quad I_D = 3\text{mA}$$

$$\left(\frac{P}{A}\right)' = S^3 \left(\frac{P}{A}\right) \Rightarrow S = 3\sqrt[3]{4}$$

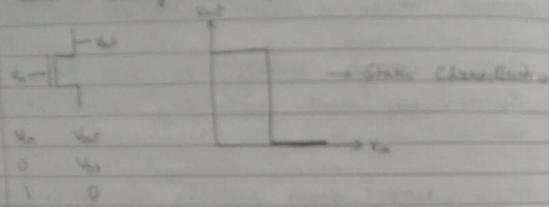
$$\therefore I_D' = \frac{3\text{mA}}{3\sqrt[3]{4}} \quad N_D' = S^2 N_D \\ = (3\sqrt[3]{4})^2 N_D$$

$$I_{D'} = \frac{W L_0}{2} \left(\frac{V_D - V_S}{S} \right) [2(V_{DS} - V_T) V_{DS} - V_{DS}^2]$$

$$I_S = \frac{W L_0}{2} \left(\frac{V_D}{S} \right) [(V_D - V_S)^2]$$

Since \rightarrow constant \Rightarrow scaling

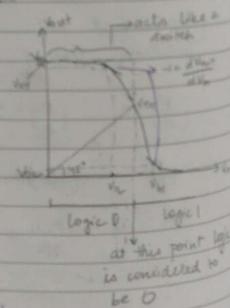
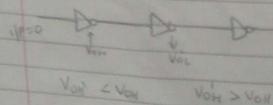
VTC - Voltage Transfer Characteristics



We want to design an inverter which has same VTC as this one is idle.

So, graph required:

- $V_{in} = \text{Highest when logic '1'}$
(highest value of i/p when logic=1)
- $V_{in} = \text{lowest when logic '0'}$
(lowest value of i/p when logic=0)
- i/p remains between V_{in} & V_{DD}
- $V_{IL} = \text{maximum i/p when logic '0'}$
- $V_{IH} = \text{minimum i/p within logic '1'}$
- $V_T = \text{logic threshold} \rightarrow \text{particularly cannot be achieved}$



If noise is more than $V_{in} - V_{IH}$ noise in clk
This is known as Noise Margin

$V_{in} - V_{in} \rightarrow \text{Noise Margin at logic 0} \rightarrow \text{noise allowed in the clk when logic 0}$

Allowed noise margin of any switch:

$$V_{in} - V_{in} = N_{M0}$$

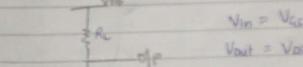
$$V_{in} - V_{in} = N_{M1}$$

What we want?

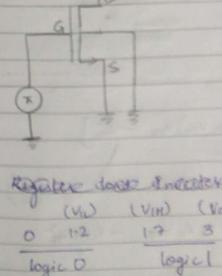
$$V_{in} = V_{DD} \quad V_{IL} = V_{IH} = V_{in} = V_{in}$$

$$V_{in} = 0 \quad N_{M0} = N_{M1}$$

REGISTER LOAD INVERTER



Anywhere where source is connected is called Drive



i/p o/p operation regions
0 V_{in} cut-off
V_{IL} < V_{in} saturation
V_{IH} > V_{in} linear (i/p)
V_{DD} > V_{in} linear

When Input logic 0
 \Rightarrow o/p logic 1
 \rightarrow inverter.

$$V_T = 0.4$$

If $i/p > o/p \Rightarrow \text{linear} \quad V_{in} > V_{IH} \rightarrow \text{linear}$
If $i/p < o/p \Rightarrow \text{saturation}$

\rightarrow In case of $\boxed{R_L}$

$$\text{Current through } R_L = I_L = \frac{V_{DD} - V_D}{R_L} = I_0$$

$$(I_0 > 0) \rightarrow V_D > V_{DD}$$

\rightarrow $V_{DD} > V_D \rightarrow$ for R-L inverter

leakage current flow \rightarrow but negligible

\rightarrow If $I_0 = \boxed{0}$ \rightarrow last case

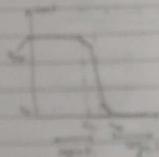
$$I_0 = \frac{V_{DD} - V_D}{R_L}$$

$$\frac{V_{DD} - V_D}{R_L} = \frac{\text{pulse}}{L} \left[2(V_{DD} - V_{DD})V_{DD} - V_D^2 \right]$$

\Rightarrow

$$V_{DD} = V_{DD} + V_{DD}$$

$$V_{DD} = V_{DD} - V_{DD}$$



$$\frac{V_{DD} - V_D}{R_L} = \frac{L}{2} \left[2(V_{DD} - V_D)V_{DD} - V_D^2 \right]$$

without loss of generality $\frac{V_{DD} - V_D}{R_L} = \frac{1}{2}$

$$V_{DD} - V_D = \frac{1}{2} (V_{DD} - V_D) L \frac{1}{R_L} \rightarrow R_L V_{DD} = \frac{1}{2} L V_{DD}$$

$$L \frac{1}{R_L} (V_{DD}) = (V_{DD} - V_D) L \frac{1}{R_L} \rightarrow V_{DD} = V_D = 0$$

$$V_D = \frac{1}{2} (V_{DD} - V_D) L \frac{1}{R_L} \rightarrow V_{DD} = V_D = 0$$

($L \neq 0$)

$$V_{DD} = \left(V_{DD} - V_D + \frac{1}{R_L L} \right) = \sqrt{\left(V_{DD} - V_D + \frac{1}{R_L L} \right)^2 - \frac{2 V_{DD}}{R_L L}}$$

\rightarrow sign considered here. We should be as least as \checkmark $\frac{1}{R_L L}$ possible

$$V_{DD} \leq \frac{1}{R_L L} \rightarrow$$
 to get $V_D = 0 \rightarrow R_L = \infty, L = 0$

$\text{but } + I_0 = \frac{\text{pulse}}{L} \rightarrow$ here $L=0$ and $I_0=0$ is not possible

$\rightarrow R_L = \infty$ not possible since $R_L = 0$ means open circuit \rightarrow not possible

\therefore to get $V_D = 0$ R_L should be very high

$\rightarrow \boxed{0} \rightarrow$ saturation region

$$\frac{V_{DD} - V_D}{R_L} = \frac{L}{2} \left[(V_{DD} - V_D)^2 \right] \quad \left(R_L = \frac{\text{pulse}}{L} \right)$$

Differentiating w.r.t. V_D

$$\frac{d}{dV_D} \left(\frac{V_{DD} - V_D}{R_L} \right) = R_L \left[V_D - V_{DD} \right]$$

$$V_D = \frac{1}{2} R_L \approx V_{DD}$$

$V_D = \frac{1}{2} R_L$ with all the other unknown about the value of V_D is not possible since V_D will give this result

$\rightarrow V_{IH}$ \rightarrow linear region

$$\frac{V_{DD} - V_0}{R_L} = \frac{k_n}{2} [2(V_{IH} - V_{TO})V_0 - V_0^2] \quad \text{--- (1)}$$

$$\frac{1}{R_L} (-i) = \frac{k_n}{2} [2V_0 + 2(V_{IH} - V_{TO})(-i) + 2V_0]$$

$\therefore \text{GND} \parallel R_L \parallel V_{DD} \parallel V_{TO}$

$$\frac{1}{R_L k_n} = V_0 - 2(V_{IH} - V_{TO}) + 2V_0$$

$$\frac{1}{R_L k_n} = V_0 - V_{IH} + V_{TO} + V_0$$

$$V_{IH} = V_{TO} + 2V_0 - \frac{1}{k_n R_L}$$

Here, we don't know the value of V_0
so put the eqn of V_{IH} or V_{out} in eqn (1)

$$V_{out} = \sqrt{\frac{2}{3}} \frac{V_{DD}}{k_n R_L} \leftarrow \text{we get this if we substitute } V_{in} = V_{IH} \text{ in eqn (1).}$$

$$\therefore V_{IH} = V_{DD}$$

$$V_{OL} \propto \frac{1}{k_n R_L}$$

$$V_{IL} \propto \frac{1}{k_n R_L}$$

$$V_{IH} \propto \frac{1}{k_n R_L}$$

Now, to get $V_{OL} \approx 0$; R_L is kept very high
 $\Rightarrow V_{IL}$ will also be very less \Rightarrow noise margin \downarrow

\Rightarrow V_{IH} also rises but we require V_{IH} to be high.

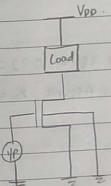
If R_L is kept high then
Power dissipation $\propto I^2$
 $\propto R$

Size \uparrow rises.

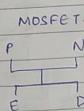
4RKT Bn \leftarrow Thermal Noise \uparrow rises

VTC is not proper

\therefore We cannot use Register-Load Inverter for Digital Design.



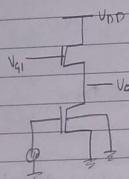
- L and C are reactance
 \Rightarrow cannot transfer power.
 \Rightarrow impedance matching does not occur.
- MOS, JFET, diode, BJT
 \Rightarrow many fabrication steps.



- If Enhancement nMOS used as load
 - Load MOS \rightarrow is in saturation region
 $V_G - V_T \leq V_D$ ($V_G = V_D$)
 - When Transistor operates in sat. there is always a drop of V_T .
 $\therefore V_O = V_{DD} - V_T$.
 - Secondly there will be high power dissip.

$$\text{Minimum value of } k_n \geq 2 \\ \mu_n C_{ox} \left(\frac{W}{L} \right) \quad L < W$$

So we can run load transistor in linear by providing gate some external supply.
 \Rightarrow no. of supplies required increases.



Q13.

eg Design a resistive load inverter with $V_{OH} = 5V$
 $V_{OL} = 0.147V$ noise margin low = $0.78V$ $V_{TO} = 0.8V$

$$N_{ML} = V_{OL} - V_{IL}$$

$$V_{IL} = V_{OL} + N_{ML} = 0.147 + 0.78 = 0.927.$$

Assume $k_n = 2$.

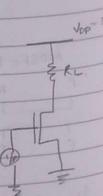
$$V_{DD} = V_{OH} = 5V.$$

$$V_{IL} = \frac{1}{2k_n R_L} + V_{TO}$$

$$0.927 = \frac{1}{2k_n R_L} + 0.8$$

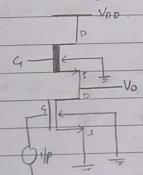
$$\frac{1}{k_n R_L} = 0.127$$

$$R_L = \frac{1}{k_n (0.127)}$$



$$\text{Practically } \mu_n = 10^{-4} \\ C_{ox} = 10^{-3}$$

Considering depletion nMOS in load.



$$\text{for load} \\ V_T = V_{TO} + r \left(\sqrt{12\phi_F + V_{SB}} - \sqrt{12\phi_F} \right)$$

Here $V_{SB} = V_S - V_B$, where $V_B = 0$ $V_S = V_O$
 $\Rightarrow V_{SB}$ depends on V_O
 $\Rightarrow V_T$ depends on V_O value

Depletion Load Driver: every time \rightarrow as effects V_T value of load
Enhancement Driver: every time \rightarrow as effects V_T value of load

- As we require load to be ON every time so when $i_D = 0 \Rightarrow V_O = 5V \Rightarrow V_T \text{ becomes } \Rightarrow V_S \text{ not greater than } V_T \rightarrow \text{load nMOS gets OFF}$

- In depletion nMOS $V_{TO} < 0$ bcoz V_{TO} is the voltage at which the depletion region gets removed.
 $V_{FB} + 2\phi_F + \frac{\theta}{C}$
this is $-ve$ and $> (2\phi_F + \phi_F)$

- $V_{GS} = V_{DD} \rightarrow$ as it gets into saturation
 $V_{GS} > V_{DS} \rightarrow$ it goes into cut-off (considering the case when $V_O = 5V$).

$V_{GS} = V_O \rightarrow V_O = V_S \Rightarrow V_{GS} = 0 \Rightarrow V_{GS} > V_{TO}$
But here it can operate in saturation or linear region \rightarrow so if while calculating V_{OT} \rightarrow nMOS required to be in linear \rightarrow if this condition is achieved then fine

$V_{IL} > V_{TO} \rightarrow$ always

Driver	Load
$V_{DS} = V_{IN}$	$V_{DS} = 0$
$V_{DS} = V_0$	$V_{DS} = V_{DD} - V_0$
V_{TO}	V_T in breakdown $V_T(V_{OUT})$ means V_T funct of V_{OUT}

i/p	o/p	Driver	Load
0	V_{OH}	Cut-off	linear $\frac{V_{DS}-V_T}{2} \rightarrow V_{DS} = V_{DD} - V_{OUT} = 0$
V_{IL}	$\approx V_{OH}$	sat.	linear $V_{OUT} < V_{IN}$
V_{IH}	$\approx V_{OL}$	linear	sat.
V_{DD}	V_0	linear	sat.

\therefore at $V_{OIP} = V_{OH} \rightarrow$ load is not in saturation \Rightarrow genl

$|V_{OH}|$

$$I_B = 0$$

$$\frac{k_{nL}}{2} [2(-V_T)(V_{DD}-V_0) - (V_{DD}-V_0)^2] = 0$$

Here $V_T \neq 0 \Rightarrow (V_{DD}-V_0)$ has to be 0

$$\therefore V_{DD}-V_0 = 0$$

$$\boxed{V_{DD} = V_0 = V_{OH}}$$

$|V_{OL}|$

$$I_D = \frac{k_{nL}}{2} [2(-V_T)(V_{DD}-V_0)]$$

$$I_{DQ} = \frac{k_{nL}}{2} (-V_T)^2$$

$$I_{DQ} = \frac{k_{nL}}{2} [2(V_{DS}-V_T)V_0 - V_{DS}^2]$$

$$= \frac{k_{nL}}{2} [2(V_{DD}-V_{TO})V_{OL} - V_{OL}^2]$$

$$I_{DQ} = I_{DL}$$

$$\frac{k_{nL}}{2} [2(V_{DD}-V_{TO})V_{OL} - V_{OL}^2] = \frac{k_{nL}}{2} V_{T(V_{OUT})}^2$$

$$2(V_{DD}-V_{TO})V_{OL} - V_{OL}^2 = \frac{k_{nL}}{k_{nD}} V_{T(V_{OUT})}^2$$

$$V_{OL}^2 - 2(V_{DD}-V_{TO})V_{OL} + \frac{k_{nL}}{k_{nD}} V_{T(V_{OUT})}^2 = 0$$

$$V_{OL} = \frac{2(V_{DD}-V_{TO}) \pm \sqrt{4(V_{DD}-V_{TO})^2 - 4\frac{k_{nL}}{k_{nD}} V_{T(V_{OUT})}^2}}{2}$$

$$\boxed{V_{OL} = (V_{DD}-V_{TO}) - \sqrt{(V_{DD}-V_{TO})^2 - (\frac{k_{nL}}{k_{nD}} V_{T(V_{OUT})})^2}}$$

$|V_{IL}|$

$|V_{IL}|$

$$\frac{dV_{OUT}}{dV_{IN}} = -1$$

$$I_{DL} = \frac{k_{nL}}{2} [2(-V_T)(V_{DD}-V_{OUT}) - (V_{DD}-V_{OUT})^2]$$

$$I_{DD} = \frac{k_{nD}}{2} (V_{IN}-V_{TO})^2$$

$$I_{OL} = I_{DP} = \frac{k_{nL}}{2} [2(-V_T)(V_{DD}-V_{OUT}) - (V_{DD}-V_{OUT})^2] = \frac{k_{nL}}{2} (V_{IN}-V_{TO})^2$$

Differentiate

$$\frac{k_{nL}}{2} [2(-V_T) \left(\frac{-dV_{OUT}}{dV_{IN}} \right) + 2(V_{DD}-V_{OUT}) \left(\frac{dV_T}{dV_{IN}} \right) + 2(V_{DD}-V_{OUT}) \frac{dV_{OUT}}{dV_{IN}}] = \frac{k_{nL}}{2} 2(V_{IN}-V_{TO}) \frac{dV_{IN}}{dV_{IN}} = -1$$

$\frac{1}{n} \cdot \frac{1}{m}$ = $\frac{1}{n+m}$ \rightarrow $n > m$ \rightarrow $n+m > n$
 \rightarrow $\frac{1}{n+m} < \frac{1}{n}$
 \rightarrow $\frac{1}{n+m} < \frac{1}{n}$

$$\frac{1}{n+m} = \frac{1}{n} \cdot \frac{1}{(n+m)-n}$$

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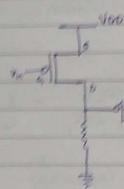
③ $\frac{1}{n+m} = \frac{1}{n}$ \rightarrow $n > m$ \rightarrow $n+m > n$
 \rightarrow $\frac{1}{n+m} < \frac{1}{n}$

④ $\frac{1}{n+m} = \frac{1}{n}$ \rightarrow $n > m$ \rightarrow $n+m > n$
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eg. find V_{DS} for resistive load p-mos inverter



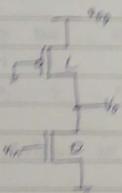
\rightarrow acts as attenuator
 \rightarrow substrate-bias effect
 comes in picture. As body is connected to V_D , while source is not connected to V_S .



$V_{GS} > V_{TO}$ cut off.
 $V_{GS} - V_{TO} \geq V_{OS}$ sat.
 $V_{GS} = V_{TO} < V_{OS}$ linear.

$V_{DS} \approx V_{IN} - V_{OS}$ for $V_{IN} \gg 0$, resistance used
 $V_{DS} \approx V_{OUT} - V_{OS}$ should be high

Power enhancement as load



$$V_{DS} = V_G - V_D = 0 = V_{DD} = -V_{SD}$$

In load will always be in saturation

As we don't require load to be in sat. always \rightarrow we give another supply to gate of pmos
 \Rightarrow no of supplies increases.

= So use depletion type pMOS. \rightarrow same as depletion NMOS.

when
 depletion
 occurs
 in pMOS
 $\left. \begin{array}{l} \text{depletion type pMOS as load} \rightarrow \text{substrate-bias effect doesn't} \\ \text{occur.} \\ " " \text{ NMOS } " " \rightarrow \text{speed is best} \\ (\text{most popular}) \end{array} \right\}$

$$\rightarrow V_{TC} \quad V_{DD} = V_{DD}$$

$$V_{OL} = 0$$

$$V_{IL} = V_{IH} = V_{TH} = \frac{V_{DD}}{2}$$

has to be improved

Noise Margin

Area

Power dissipation

Thermal Noise

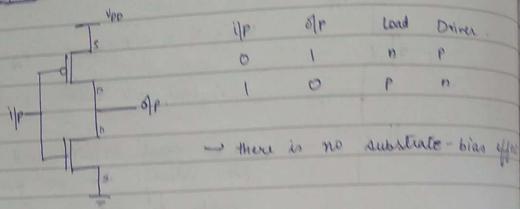
\rightarrow already improved

\rightarrow has to be improved

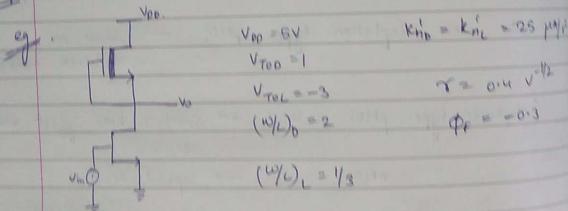
\rightarrow already improved

This is achieved till now \uparrow

CMOS

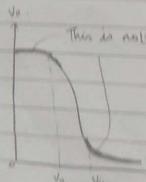


16/3



$$\rightarrow V_{OH} = V_{ON} = 5V$$

$$\rightarrow V_{OL} = V_{DN} - V_{TO} = \sqrt{(V_{DD} - V_{TO})} = \frac{k_n}{k_p} \sqrt{T(V_{DD})}$$



So $V_{IL} \neq V_{OL}$ $V_{IL} \approx V_{OL}$
 $V_{IH} \neq V_{OH}$ $V_{IH} \approx V_{OH}$

$$V_T = V_{TO} + T (\sqrt{|2\phi_F|} + V_{SB} - \sqrt{|2\phi_F|})$$

$$= -3 + 0.4 (\sqrt{0.6 + 0} - \sqrt{0.6})$$

$V_{SB} = V_S - V_B$ here source of pMOS is connected to Vout & body is connected to ground

$$\therefore V_{SB} = V_{out} - 0 = V_{out}$$

as we are unaware about the value of Vout and ideally we know that $V_B = 0$
 $\therefore V_B = 0$ standard is considered.

$$\therefore V_T = V_{TO} \approx -3V$$

$$\therefore V_{OL} = \sqrt{5 - 1} = \sqrt{(5-1)^2 + V_B (-3)^2} = 0.192$$

$$V_T = V_{TO} + T (\sqrt{0.6 + 0.192} - \sqrt{0.6})$$

$$= -2.98V$$

This is found back earlier $V_{SB}=0$ was assumed but value of V_{out} to get V_{in} consider $V_{out} = 0.192$ & find V_T again

$$\therefore V_{OL}' = (5-1) = \sqrt{4^2 + V_B (-2.95)^2} = 0.186$$

As the difference b/w V_{OL} & V_{OL}' is very small as compared to V_{DD} \Rightarrow effect of variation is very less

$$\boxed{\begin{aligned} V_{OL} &= 0.186 \\ \text{for } V_T &= -2.95 \end{aligned}}$$

$$\rightarrow V_{IL} = V_{IN} + \frac{V_o}{R_o} (-V_T - V_{IN} + V_T)$$

for V_{IL} : $V_{IN} = 5V$ but its exact value is not known $\Rightarrow V_{IN} = 5V$ is assumed for

$$V_T = V_{IN} + \sqrt{0.6 + 5} - 1.36$$

$$\therefore V_L = 4 + \frac{1}{6} (2.36 - 5 + V_o) \quad \begin{matrix} \text{This do not assume} \\ \text{all remaining } V_T \\ \text{do not change w.r.t} \\ \text{variation in } V_o \text{ do} \\ \text{it's reasonable b/c} \\ \text{will be many?} \end{matrix}$$

$$V_o = 6V_{IL} - 3.36$$

Substitute V_o value in eqⁿ when $I_{OL} = I_{OB}$ is done before differentiating

$$\frac{k_m}{2} [2(-V_T)(V_{OB} - V_{OUT}) - (V_{OB} - V_{OUT})^2] = \frac{k_m}{2} (V_{IL} - V_o)$$

$$\frac{1}{6} [2(2.36)(5 - (6V_{IL} - 3.36)) - (5 - (6V_{IL} - 3.36))^2] = (V_{IL} - 1)^2$$

\therefore we get $V_{IL} = 1.36$ and 0.63

Now as $V_o > V_{OB}$, i.e., $V_o = 0.63$ is not possible

Q DRCG

$$V_o = 6(1.36) - 3.36 = 4.81$$

$$\boxed{V_{IL} = 1.36}$$

$$\boxed{V_o = 4.81}$$

As using $V_o = 4.81V$ in V_T find V_{IL} keeping V_{IN} as it is
 $\Rightarrow V_{IL}$ eqⁿ comes again and
find V_{IL} and $4.81V$.

$$\rightarrow V_{IL} = 2V_{IN} + V_{oP} + \frac{V_o}{R_o} \quad \begin{matrix} \text{from} \\ \text{eq n} \end{matrix}$$

as $V_{IN} = V_o$ which we have found earlier \Rightarrow so for the corresponding V_o is also found.

$$\therefore V_{IL} = 0.185$$

$$V_T = 2.95$$

$$\frac{dV_T}{dV_{out}} = \frac{\frac{1}{2} \frac{1}{2(2.95) + 5}}{2} = \frac{0.4}{2 \sqrt{0.6 + 5}} = 0.451 = 0.4205$$

$$V_{IL} = 2(0.4205) + 1 + \frac{1}{6} (-2.95) (0.4205)$$

$$V_{IL} = 2V_o + 1 + \frac{1}{6} (-2.95) (0.4205)$$

$$V_{IL} = 2V_o + 0.778$$

$$V_o = \frac{V_{IL} - 0.778}{2}$$

Substitute V_o value in eqⁿ

$$\frac{k_m}{2} [2(V_{IL} - V_{oP}) V_{IL} - V_{oP}^2] = \frac{k_m}{2} (-V_T)^2$$

$$[2(V_{IL} - 1) \left(\frac{V_{IL} - 0.778}{2}\right) - \left(\frac{V_{IL} - 0.778}{2}\right)^2] = \frac{1}{6} (2.95)^2$$

$$\frac{2}{2} V_{IL}^2 - 0.778 V_{IL} - V_{IL} + 0.778 - \frac{V_{IL}^2}{4} - 1.556 V_{IL} + 0.605 = 1.45$$

$$-0.75 V_{IL}^2 - 2.147 V_{IL} + 1.45 = 0$$

$$\boxed{V_{IL} = 1.91}$$

$$\boxed{V_o = 0.345}$$

