

Ex: For a Mosfet device scaling to be performed, the power density of scaled device is 8 unit which was 2 unit before scaling. If the sat. current was 3mA and substrate doping density was $10^{16}/\text{cm}^3$. Then find out sat drain current and substrate doping density after scaling of the device.

Sol:

$$(P/A)' = S^3 (P/A)$$

$$8 = S^3 (2)$$

$$S^3 = 4$$

$$S = 1.58$$

$$\begin{aligned} I_D' &= S I_D \\ &= 1.58 \times 3 = 4.762 \text{ mA} \end{aligned}$$

$$N_d' = S^2 N_d$$

$$= 10^{16} \times (1.58)^2$$

$$= 2.51 \times 10^{16} / \text{cm}^3$$

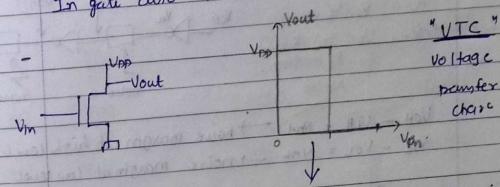
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Static Charc of MOS

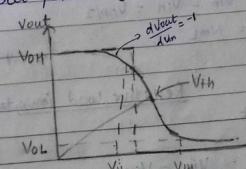
as change in input voltage / current, output voltage / current will not change \rightarrow static

- for all digital circuits basic element is gate and In gate also NOT is most basic component



its ideal response of an inverter

But practically we get diff VTC



\$V_{OH} \rightarrow\$ Highest o/p voltage when logic '1'

\$V_{OL} \rightarrow\$ lowest o/p voltage when logic '0'

\$V_{IL} \rightarrow\$ Max. input voltage which logic '0'

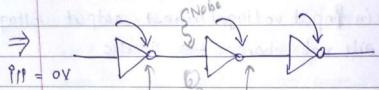
\$V_{IH} \rightarrow\$ min. input voltage which logic '1'

\$V_{th} \rightarrow\$ Logic threshold

- logic threshold is not stable, it continuously changes

$V_{th} \rightarrow$ is high value 2-3 V

$V_T, V_{IO} \rightarrow 0.5 - 0.7 V$



$V_{OH} \approx V_{OL}$

$V_{OH}' > V_{OL}$

By adding

Noise

$V_{OH} - V_{IH} = N_{MH}$

$V_{IL} - V_{OL} = N_{ML}$

\rightarrow noise margin at high level
 $V_{IL} - V_{OL} = N_{ML} \rightarrow$ noise margin at low level

For $V_{OH} = V_{DD}$

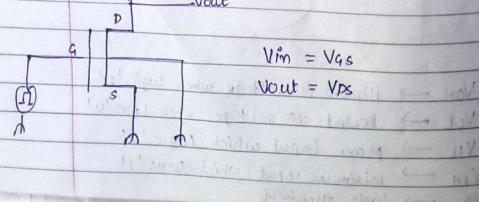
$$\left\{ \begin{array}{l} V_{OH} = V_{DD} \\ V_{OL} = 0 \\ V_{IL} = V_{th} = V_{IH} = V_{DD}/2 \end{array} \right.$$

$$N_{MH} = N_{ML}$$

(P/N 18)

\Rightarrow

"Resistive load inverter"



$$V_{in} = V_{gs}$$

$$V_{out} = V_{ds}$$

$$V_{in} = V_{ds}$$

- where i_P voltage is step applied, that's known as driver.

- drain & bias voltage are connected with the help of metal, so some resistance always present there.

	i_{IP}	i_{OP}	i_{OT}
I)	0	V_{OH}	Cut off
II)	V_{IL}	$\approx V_{OH}$	Saturation
III)	V_{IH}	≈ 0	Linear
IV)	V_{OD}	V_{OL}	Linear

$$\begin{matrix} 0 & 10^2 & 10^3 & 3 \\ | & | & | & | \\ V_{IL} & V_{IH} & V_{OD} & V_{OP} \end{matrix} \quad VT = 0.4$$

logic 0 logic 1

$V_{OH} \approx$

cutoff:

$$I_R = \frac{V_{DD} - V_O}{R}$$

$$I_D = 10$$

$$\frac{V_{DD} - V_O}{R} = 0 \Rightarrow V_O = V_{DD}$$

$$V_{OH} = V_{DD}$$

Vol

Linear region

$$V_{DD} - V_O = \frac{I_R}{R}$$

→ ①

$$I_O = \frac{K_n C_o}{2} \left[\frac{1}{L} (V_{DD} - V_{TO}) V_{OL} - V_{O}^2 \right] \rightarrow ②$$

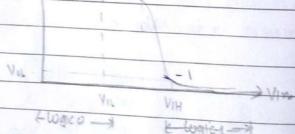
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$$N_{MH} = V_{OH} - V_{IH}$$

$$N_{ML} = V_{IL} - V_{OL}$$

Vout

$$-1 = \frac{dV_{out}}{dV_{in}}$$



from ① & ②

$$\frac{V_{DD} - V_{OL}}{R_L} = K_n \left[\frac{1}{2} (V_{DD} - V_{TO}) V_{OL} - V_{OL}^2 \right]$$

$$\text{where } K_n = \frac{K_n C_o}{2} \left(\frac{W}{L} \right)$$

$$V_{DD} - V_{OL} = \frac{1}{2} (V_{DD} - V_{TO}) V_{OL} + K_n R_L V_{OL}^2$$

$$K_n R_L V_{OL}^2 - \frac{1}{2} (V_{DD} - V_{TO}) K_n R_L + V_{OL}^2 = 0$$

$$V_{OL} = \frac{-b \pm \sqrt{b^2 - 4ac}}{2a}$$

$$V_{OL} = \left(V_{DD} - V_{TO} + \frac{1}{K_n R_L} \right) - \sqrt{\left(V_{DD} - V_{TO} + \frac{1}{K_n R_L} \right)^2 - \frac{4V_{DD}}{K_n R_L}}$$

check this

- -ve sign considered bcz Vol should be as less as possible.

$$V_{OL} \propto \frac{1}{K_n R_L} \Rightarrow \text{to get } V_{OL} = 0 \Rightarrow K_n = \infty \quad R_L = \infty$$

but $\Rightarrow K_n = \frac{K_n C_o}{2} \left(\frac{W}{L} \right)$ → here $W = \infty$ and $L = 0$ is not possible

$\Rightarrow K_n = \infty$ not possible

$\Rightarrow R_L = \infty$ is not possible bcz $R_L = \infty$ means open circuit → not possible.

∴ To get very less R_C should be very high.

VIL

⇒ Saturation region

$$\frac{V_{DD} - V_{OL}}{R_L} = K_n (V_{IL} - V_{TO})^2$$

$$\left\{ K_n = \frac{K_n C_o}{2} \left(\frac{W}{L} \right) \right\}$$

$$\therefore \left(\frac{dV_{out}}{dV_{in}} = -1 \right)$$

$$\text{differentiating w.r.t } V_{in} \\ -1 (-1) = K_n (V_{IL} - V_{TO})$$

$$\frac{R_L}{V_{IL}} = \frac{1}{K_n R_L} + V_{TO}$$

$V_{IL} \times \frac{1}{R_L}$ \Rightarrow as we are unaware about the value of V_{IH} so we can't predict about V_{IL} from this cond.

(\approx) \Rightarrow linear region

$$\frac{V_{DD} - V_0}{R_L} = \frac{K_n}{2} \left[2(V_{in} - V_{T0}) V_0 - V_0^2 \right] \quad (1)$$

differentiating

$$\frac{-1}{R_L} (-1) = \frac{K_n}{2} [2V_0 + 2(V_{in} - V_{T0})(-1) + 2V_0]$$

$$\frac{1}{R_L K_n} = V_0 - (V_{in} - V_{T0}) + V_0$$

$$\frac{1}{R_L K_n} = V_0 - V_{IH} + V_{T0} + V_0$$

$$V_{IH} = V_{T0} + 2V_0 - \frac{1}{R_L K_n}$$

here, we don't know the value of V_0 . so put the eqⁿ of V_{IH} or V_{out} in eqⁿ (1)

$$V_{out} = \sqrt{\frac{2}{3} \frac{V_{DD}}{K_n R_L}} \quad \text{we get this if we substitute } V_{in} = V_{IH} \text{ in eqⁿ 1}$$

$$\therefore V_{IH} = V_{DD}$$

$$V_{IL} \times \frac{1}{R_L}$$

$$V_{IL} \times \frac{1}{R_L}$$

$$V_{IH} \times \frac{1}{R_L}$$

Now, to get $V_{IL} > 0$; R_L is kept very high
 $\Rightarrow V_{IL}$ will also be very less \Rightarrow noise margin \downarrow
 $\Rightarrow V_{IH}$ also goes but we require V_{IH} to be high.

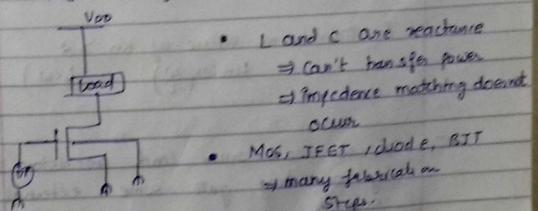
If R_L is kept high then
(1) power dissipation $\propto I^2$
 $\propto R$

(2) Size issue

(3) $4 \pi k T B_m \rightarrow$ thermal noise \uparrow

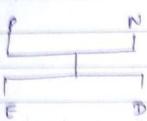
(4) VTC is not proper
 $- P_{dc}(\text{avg.}) = \frac{V_{DD}}{2} \left(\frac{V_{DD} - V_{out}}{R_L} \right)$

\therefore we cannot use Register-load inverter for Digital Design.



- L and C are reactance
- \Rightarrow can't transfer power
- \Rightarrow impedance matching doesn't occur
- Mos, JFET, diode, BJT
- \Rightarrow many fabrication steps

MOSFET



(PN-16) If enhancement nmos used as load



* lead mos \rightarrow is in sat. region

$$V_{ds} = V_D - V_B \quad (V_D = V_0)$$

* when transistor operates in sat. there is always a drop of V_T .

$$V_D = V_{DD} - V_T$$

- Secondly there will be high power dissipation

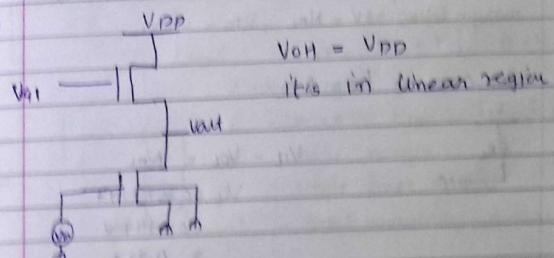
C Minimum value of $k_n > 2$

$$\min(k_n) \quad (\text{LSD})$$

So we can run load transistor in linear region by providing gate some external supply.

\Rightarrow no. of supplies required 2

(ii)



$$V_{OH} = V_{DD}$$

It is in linear region

Both types of inverters ext. suffer from relatively high stand-by (DC) power dissipation. Hence enhancement-load nMOS inverters are not used in any large-scale digital application.

Ex:- Design resistive load inverter with $V_{OH} = 5V$, $V_{OL} = 0.147V$, $V_{TL} = \text{noise margin below } 0.78V = NM_L$, $V_{TD} = 0.8V$.

Sol:-

let assume $k_N = 2$



$$\begin{aligned} V_{IL} &= V_{DD} - V_{OL} = NM_L \\ V_{IL} &= 0.78 + 0.147 \\ &= 0.927V \end{aligned}$$

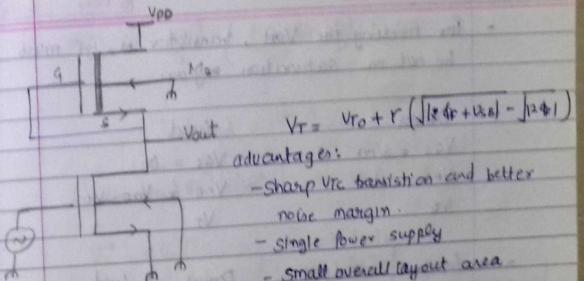
$$\begin{aligned} V_{IL} &= V_{DD} + \frac{1}{k_N R_L} \\ k_N R_L &= V_{DD} - V_{IL} \\ 2 \times 0.8 &= 5 - 0.927 \\ 0.927 - 0.8 &= \frac{1}{2 R_L} \\ R_L &= 3.93\Omega \end{aligned}$$

$$\begin{aligned} k_N &= 2 \\ k_N C_{ox} W/L &= 2 \\ 10^{-3} &= 2 \end{aligned}$$

So here $W/L \rightarrow 10^3$ that's not practically possible. So we have to take $W/L = 2$. So we have to take the value of R_L is very high as possible.

(P-N-P) Depletion type n-mos as load:

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advantages:

- sharp V_{TC} transition and better noise margin.
- single power supply
- small overall layout area

- as if P is changes output is also changes as off is changes V_T is also changes due to source of M_2 is not grounded
- $V_{GS} > V_T$
when $V_{out} = 0$, then for M_2 is in ON condition.
But when $V_{out} = V_{DD}$, then M_2 is in cut off

for enhancement type: V_{DS} voltage for which required to create a channel $V_{DS} = 0.8V$

depletion type: V_{DS} voltage which required to remove the channel, k_{D2} channel is already there. $V_{DS} < 0$

- Gate of M_2 would be connected to source
 - ↳ $V_{GS} = 0 > V_{TO}$ → in ON
 - ↳ if gate is grounded $V_{GS} = -5 < V_{TO}$ → cut off
 - ↳ If gate is connected to V_{DD} , then also M_2 is in saturation region.

- for finding the V_{OH} , transistor is in must be not in saturation region.

- Driver \rightarrow Load

$$V_{GS} = V_{in} \quad V_{GS} = 0$$

$$V_{DS} = V_o \quad V_{DS} = V_{DD} - V_o$$

$$V_T \quad V_T$$

Input	Output	Driver	Load
0	V_{OH}	Cut off	linear
V_{IL}	$\approx V_{OH}$	Saturation	linear
V_{IH}	$\approx V_o$	linear	Saturation
V_{DD}	V_{OL}	linear	Saturation

- $V_{OH} \approx$

$I_D = 0 \rightarrow$ Driver is in cut off

$$K_n L \left\{ \alpha (V_T) (V_{DD} - V_o) - (V_{DD} - V_o)^2 \right\} = 0$$

$$V_{DD} - V_o = 0$$

$$\boxed{V_{DD} = V_o = V_{OH}}$$

- $V_{OL} \approx$

$$I_D = \frac{K_n}{2} \left(\alpha (V_{DD} - V_T) V_o - V_o^2 \right)$$

$$I_D(L) = \frac{K_n}{2} L \left((V - V_T)^2 \right)$$

$$I_D(\text{load}) = I_D(\text{driver})$$

$$2[V_{in} - V_{TO}] - [V_o^2] = V_T^2 \cdot \frac{K_n L}{K_n D}$$

$$V_o^2 - 2V_o(V_{in} - V_{TO}) + V_T^2 \cdot \frac{K_n L}{K_n D} = 0$$

$$\boxed{V_{OL} = (V_{DD} - V_{TO}) - \left[(V_{DD} - V_{TO})^2 - \frac{K_n L (V_T)^2}{K_n D} \right]}$$

$$- \frac{V_{IL}}{I_D(\text{sat})} = \frac{K_n}{2} L \left[\alpha (V_{in} - V_T)^2 \right]$$

$$I_D(\text{line}) = \frac{K_n}{2} L \left[\alpha (0 - V_T)(V_{DD} - V_o) - (V_{DD} - V_o)^2 \right]$$

$$K_n D (V_{in} - V_{TO})^2 = -2(V_{DD} - V_o) V_T - (V_{DD} - V_o)^2$$

$$K_n D \cdot 2(V_{in} - V_{TO}) = -2V_T (0 - V_{DD}) + 2(V_{DD} - V_o)$$

$$-2(V_{DD} - V_o) 2V_T = \frac{2V_D}{2V_{in}}$$

$$\frac{\partial V_T}{\partial V_{in}} \rightarrow 0, \text{ because change in input voltage is very less } V_{in} = V_{IL}$$

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$V_{in} = V_{IL}$
 $\frac{\partial V_{out}}{\partial V_{in}} = -1$
 $\frac{\partial V_{in}}{\partial V_{in}}$

$Kn)_D (V_{IL} - V_{to}) = Kn)_L \left[\frac{2(-V_T)(1) + \varrho(V_{DD} - V_0)}{(V_{DD} - V_0)^2} \right] + \frac{1}{2}(V_{DD} - V_0)$

$Kn)_D (V_{IL} - V_{to}) = Kn)_L \left[-2V_T - 2V_{DD} + 2V_0 \right]$

$Kn)_D (V_{IL} - V_{to}) = Kn)_L (V_0 - V_{DD} - V_T)$

$V_{IL} = \frac{Kn)_L}{Kn)_D} (V_0 - V_{DD} - V_T) + V_{to}$

$I_{load} = I_D = \frac{1}{2} Kn_L \cos(\omega) \left(V_{to} - V_{th,n} \right)^2$

Driver: $I_D \text{ linear} = \frac{Kn)_D}{2} \left(\varrho (V_{in} - V_{th,D}) V_0 - V_0^2 \right)$

By diff'g $\frac{Kn)_L}{Kn)_D} \cdot V_{th,n} \frac{\partial V_{th,n}}{\partial V_{in}} = \frac{2(1 - \varrho V_{in})}{\sqrt{2(V_{in} - V_{th,n})}} V_0 + \frac{\varrho V_{out}}{\sqrt{2(V_{in} - V_{th,n})}}$
 $- \frac{\varrho V_0 \cdot \frac{\partial V_{out}}{\partial V_{in}}}{\sqrt{2(V_{in} - V_{th,n})}}$

$V_T = V_{to} + \varrho \left(\sqrt{2(V_{in} - V_{th,n})} - \sqrt{2(V_{in} - V_{th,D})} \right)$

$\frac{\partial V_T}{\partial V_{in}} = \frac{\partial V_T}{\partial V_{SB}} \frac{\partial V_{SB}}{\partial V_{in}} = V_{SB} = V_{out}$

$= \frac{\partial V_T}{\partial V_{out}} \frac{\partial V_{out}}{\partial V_{in}}$

$\frac{\partial V_T}{\partial V_{out}} = \frac{K}{2 \sqrt{2(V_{in} - V_{th,n})} + V_{out}}$

So, $\frac{Kn)_L}{Kn)_D} \frac{V_{th,n} \cdot K}{2 \sqrt{2(V_{in} - V_{th,n})} + V_{out}} \frac{\partial V_{out}}{\partial V_{in}} = \frac{(1 - \varrho V_{in})}{2 \sqrt{2(V_{in} - V_{th,n})} + V_{out}} \frac{\partial V_{out}}{\partial V_{in}}$
 $V_{out} + \frac{\varrho V_{out}}{\sqrt{2(V_{in} - V_{th,n})}} - \frac{\varrho V_{out} \cdot \frac{\partial V_{out}}{\partial V_{in}}}{\sqrt{2(V_{in} - V_{th,n})}}$

$\Rightarrow \frac{Kn)_L}{Kn)_D} \frac{V_{th,n} \cdot K}{2 \sqrt{2(V_{in} - V_{th,n})} + V_{out}} - (-1) = V_{out} + (V_{to} - V_{in}) + V_{out}$

$$- \frac{K_n j_L}{K_n j_D} V_{THN} \cdot \frac{dV_T}{dV_{out}} = 2V_{out} + V_{TO} - V_{in}$$

$$V_{in} = V_{IH} = \frac{2V_{out} + V_{TO} + K_n j_L V_T}{K_n j_D} \frac{dV_T}{dV_{out}}$$

$$\text{So, } V_{OH} = V_{DD}$$

$$V_{OL} \propto \frac{K_L}{K_D} = \frac{(W/L)_L}{(W/L)_D}$$

$$V_{IL} \propto \frac{K_L}{K_D}$$

$$V_{IH} \propto \frac{K_L}{K_D}$$

$$\text{where } K_L = \mu n \text{ox} (W/L)_L$$

$$K_D = \mu p \text{ox} (W/L)_D$$

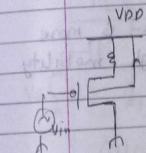
n-mos are using cas code load and an driver so
 $\mu n \text{ox} (W/L)_L = \mu p \text{ox} (W/L)_D$ & if same technology
 $(W/L)_L = (W/L)_D$
then $(W/L)_L < (W/L)_D$

for ^{tiny} driver larger than the load

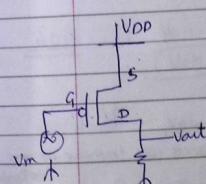


Resistive load	Size P _{DS}	mos depletion load
✓	✓	✓
✓	✓	✓
✓	✓	✓

Ex8- for p-mos resistive load ckt.



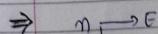
Substrate & source are not at same potential due to R, so we don't do that to remove the substrate bias effect.



$V_{GS} > V_{TO} \rightarrow \text{cutoff}$
 $V_{GS} - V_{TO} \geq V_{DS} \rightarrow \text{saturation}$
 $V_{GS} - V_{TO} \leq V_{DS} \rightarrow \text{linear}$

$$V_{GS} = V_{in} - V_{DD}$$

$$V_{DS} = V_{out} - V_{DD}$$

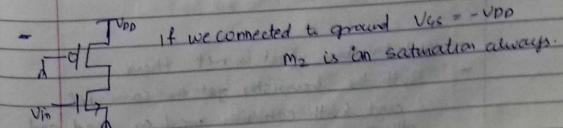


n → E

p → E

D → n-mos

D → p-mos



- if PMOS as load in NMOS driven then there is no substrate bias effect.
- and NMOS enhancement & depletion is more used becoz in NMOS speed is high, mobility is high.

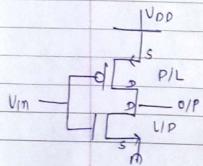
$\circ \Rightarrow V_{OH} = V_{DD}$

$$V_{DL} = 0$$

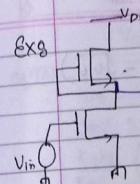
$$V_{IL} = V_{IH} = V_{DD}$$

{ VTC
 NM
 Area (MOS are used as load then area will improve as in Power)
 Thermal noise (By using MOS as load, TN will 0)

CMOS (Complementary metal oxide)



- Substrate bias effect is not there.
- Both the transistors get the same I/P and both can be used as load and driver \rightarrow CMOS



$$\begin{aligned} V_{DD} &= 5V \\ V_{T0,D} &= 1 \\ V_{T0,L} &= -3 \\ W/L_D &= 2 \\ W/L_L &= 1/3 \end{aligned}$$

calculate V_{OH} , V_{OL} , V_{IH} & V_{IL}

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2018 i) $V_{OH} = V_{DD}$

$$V_{OH} = 5V$$

$$\begin{aligned} ii) V_{OL} &= (V_{DD} - V_{T0}) - \frac{(V_{DD} - V_{T0})^2 - K_m L}{K_m D} V^2(V_{out}) \\ &= (5-1) - \frac{(5-1)^2 - 1}{6} \end{aligned}$$

$$\begin{aligned} V_T(V_{out}) &= V_{T0,L} + \gamma \sqrt{2\phi_F + V_{SB} - \sqrt{2\phi_F}} \\ &= -3 + 0.4 \left(\sqrt{0.6+0} - \sqrt{0.6} \right) \end{aligned}$$

here V_{SB} = source is connected to Vout & Body is connected to ground

here we don't know $V_{SB} \rightarrow$ let assume $V_{SB}=0$

$$V_{IL} \rightarrow V_{T0,L}$$

$$\begin{aligned} \text{So, } V_{OL} &= (5-1) - \sqrt{(5-1)^2 - 1/(6(3))^2} \\ &= 0.192V \end{aligned}$$

$$\text{In eqn (1)} \quad V_{SB} = V_{OL} = 0.192$$

$$V_T = -3 + 0.4(\sqrt{0.6 + 0.192} - \sqrt{0.6})$$

$$= -2.95 \text{ V}$$

So, when $V_{T,L} = -2.95$

then

$$V_{OL} = (5-1) - \sqrt{(5-1)^2 - \frac{1}{6}(-2.95)^2}$$

$$\checkmark V_{OL} = 0.186 \text{ V}$$

$$\checkmark V_{T,L} = -2.95 \text{ V}$$

$$\text{iii) } V_{IL} = \frac{k_n L}{k_n D} [V_0 - V_{DD} - V_{T,L}] + V_{TO,0}$$

$$\Rightarrow \frac{k_n D}{k_n L} (V_{IN} - V_{TO})^2 = -2(V_{DD} - V_0) V_T - (V_{DD} - V_0)^2 - \theta$$

$$V_T = V_{TO} + k' (\sqrt{1.2 \cdot 0.6 + V_{SB}} - \sqrt{1.2 \cdot 0.6})$$

fixe $V_{SB} = V_{OH} = 5 \text{ V}$

$$= -3 + 0.4 (\sqrt{0.6 + 5} - \sqrt{0.6})$$

$$= -2.36 \text{ V}$$

$$\text{so, } V_{IL} = 1 + \frac{1}{6} (V_0 + 2.36 - 5)$$

$$V_{IL} = 1 + \frac{1}{6} V_0 - 0.44$$

$$= -0.56 + 0.16 V_0$$

$$V_0 = 6 V_{IL} - 3.36$$

$$V_{IN} = V_{IL}$$

$$V_{OUT} = 6 V_{IL} - 3.36$$

$$\frac{k_n D}{k_n L} (V_{IL} - V_{TO})^2 = -2 [V_{DD} - 6 V_{IL} + 3.36] V_T - (V_{DD} - 6 V_{IL} + 3.36)^2$$

$$6(V_{IL} - 1)^2 = -2(5 - 6 V_{IL} + 3.36)(-2.36) - (5 - 6 V_{IL} + 3.36)^2$$

$$6(V_{IL} - 1)^2 = 39.45 - 28 \cdot 3.8 V_{IL} - (8 \cdot 6 V_{IL})^2$$

$$6 V_{IL}^2 + 6 - 12 V_{IL} = 39.45 - 28 \cdot 3.8 V_{IL} - 64 - 36 V_{IL}^2 + 96 V_{IL}$$

$$42 V_{IL}^2 - 79.68 V_{IL} + 30.55 = 0$$

$$\checkmark V_{IL} = 1.36, 0.53 \text{ V}$$

V_{IL} is the value when transistor is ON, $V_{TO} = 1 \text{ V}$

$$\text{so, } V_{IL} = 1.36 \text{ V}$$

$$\text{so, } V_{OUT} = 4.8 \text{ V}$$

$$\text{now, } V_T = -3 + 0.4 (\sqrt{0.6 + 4.8} - 1.36)$$

$$= -2.38 \text{ V}$$

$$\text{iv) } V_{IH} = \frac{2V_0 + V_{TO} + \frac{k_n L}{k_n D} V_T}{\frac{dV_{out}}{dV_{out}}}$$

$$\frac{dV_T}{dV_{out}} = \frac{k'}{2\sqrt{1.2 \cdot 0.6 + V_{out}}}$$

$$V_{out} \geq V_{OL}$$

$$\frac{dV_T}{dV_L} = \frac{0.4}{2(0.6 + 0.18)}$$

$$= 0.56 \text{ V} \times 0.4 = 0.224 \text{ V}$$

$$V_{TL} = -2.95 \text{ V}$$

$$V_{IH} = 2V_{OL} + 1 + \frac{1}{2}(-2.95)(0.4)$$

$$V_{IH} = 2V_{OL} + 0.92$$

$$V_{OL} = 0.5 V_{IH} = 0.46 \text{ V}$$

$$\Rightarrow \frac{1}{6} [(1)^2] = 2(V_{IH}-1)(0.5V_{IH}-0.36) - (0.5V_{IH})^2$$

$$0.166 = 2(0.5V_{IH} - 0.36V_{IH} - 0.5V_{IH}^2 + 0.36) - (0.5V_{IH})^2 + 2(0.5)(0.36)V_{IH}$$

$$0 = 0.25V_{IH}^2 - 1.36V_{IH} + 0.42$$

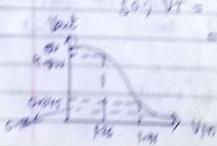
$$V_{IH} = 1.41, 0.39 \text{ V}$$

$$\text{So, } V_{out} = 0.5(1.41) - 0.36$$

$$V_{out} = 0.34 \text{ V}$$

$$\text{So, } V_T = -2 + 0.4[(0.5 + 0.34) - 1.41]$$

$$= -2.92 \text{ V}$$

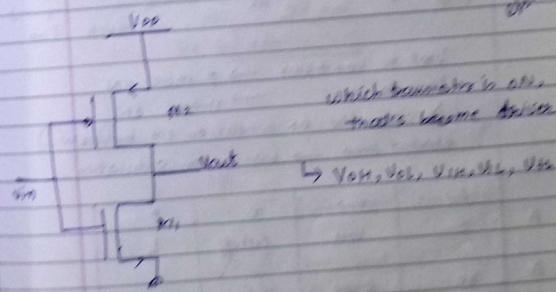


Chp-5 Static char

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CMOS 8

- Power Dissipation
- Noise margin (V_{TC}) → There two noise margins are determined by the transistors
- Area / Size
- Noise



$$V_{GS} = V_{in} - V_{DD}$$

$$V_{DS} = V_{DD} - V_{out}$$

$$V_{GS} > V_{Thn}, V_{GS} < V_{Thp}$$

$$V_{GS} - V_{Thp} < V_{DS} \rightarrow sat$$

$$V_{in} - V_{Thp} + V_{DD} \rightarrow sat$$

$$V_{in} - V_{Thp} > V_{DS} \rightarrow CFE$$

$$V_{GS} - V_{Thp} > V_{DS} \rightarrow small$$

$$V_{GS} - V_{Thp} > V_{DS} \rightarrow CFE$$

$$V_{out} \approx V_{OL}$$

$$\frac{dV_T}{dV_{out}} = \frac{0.4}{2\sqrt{0.6+0.186}} = 0.56 \text{ V} \times 0.4 = 0.225 \text{ V}$$

$$V_{TL} = -2.95 \text{ V}$$

$$V_{IH} = 2V_{out} + 1 + \frac{1}{6}(-2.95)(0.56)$$

$$V_{IH} = 2V_{out} + 0.72$$

$$V_{out} = 0.5 V_{IH} - 0.36$$

$$\Rightarrow \frac{1}{6}[(1)^2] = 2(V_{IH}-1)(0.5V_{IH}-0.36) - (0.5V_{IH}-0.36)^2$$

$$0.166 = 2(0.5V_{IH}^2 - 0.36V_{IH} - 0.5V_{IH} + 0.36) - (0.5V_{IH})^2 - (0.36)^2 + 2(0.5)(0.36)V_{IH}$$

$$0 = 0.75V_{IH}^2 - 1.36V_{IH} + 0.42$$

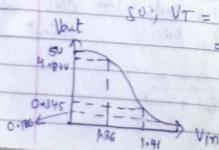
$$V_{IH} = 1.41, 0.39 \text{ V}$$

$$\text{so, } V_{out} = 0.5(1.41) - 0.36$$

$$V_{out} = 0.345$$

$$\text{so, } V_T = -3 + 0.4(\sqrt{0.6+0.345} - \sqrt{0.6})$$

$$= -2.92 \text{ V}$$



Chp-5 Static charc

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CMOS 8

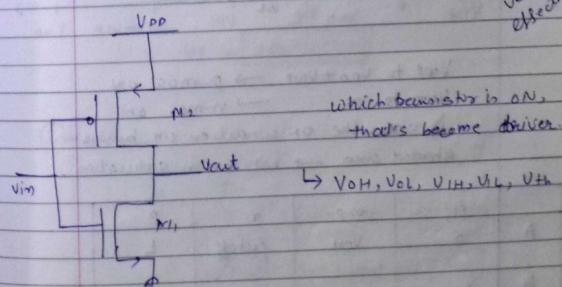
- Power Dissipation

- Noise Margin (V_{TC})

- Area / size

- Noise

There two problems are solved by the CMOS very effectively.



M₁

$$V_{GS} = V_{in}$$

$$V_{DS} = V_{out} - V_{DD}$$

$$V_{GS} > V_{Th}, V_{GS} < V_{Th} \text{ cutoff}$$

$$V_{GS} - V_{Th} < V_{DS} \rightarrow \text{sat.}$$

$$V_{in} - V_{th} < V_0 \rightarrow \text{sat.}$$

M₂

$$V_{GS} = V_{in} - V_{DD}$$

$$V_{DS} = V_{out} - V_{DD}$$

$$V_{GS} < V_{Th}, V_{GS} > V_{Th} \text{ on off}$$

$$V_{in} - V_{DD} < V_{Th} \rightarrow \text{on}$$

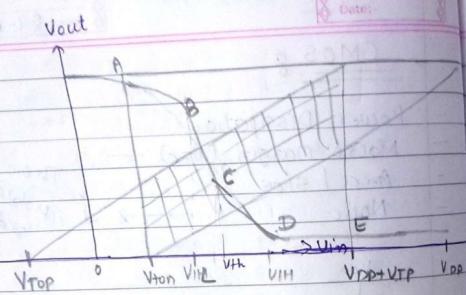
$$V_{in} < V_{Th} + V_{DD} \rightarrow \text{off}$$

$$V_{GS} - V_{Th} > V_{DS} \rightarrow \text{sat.}$$

$$V_{in} - V_{Th} > V_0 \rightarrow \text{sat.}$$

$$V_{GS} - V_{Th} > V_{DS} \rightarrow \text{off}$$

$$V_{in} - V_{Th} > V_0 \rightarrow \text{off}$$



V_{TOP} to $V_{DD} + V_{TP}$ \rightarrow p-mos ON
 V_{TH} to ∞ \rightarrow n-mos ON
 △ shows the ON condition on behavior
 Shaded area \rightarrow both are in saturation.

	P_{IP}	O_{IP}	n	p
A	0	V_{OH}	cutoff	L
B	V_{IL}	$\approx V_{OH}$	sat.	L
C	V_{TH}	V_{TH}	Sat.	S
D	V_{IH}	$\approx V_{OL}$	linear	S
E	V_{DD}	V_{OL}	linear	cutoff

- When both mos are in the saturation region, that's difficult to achieve.

① V_{OH} (first row)

$$I_n = I_p$$

$$I_p = 0 \rightarrow (I_n \text{ cut off})$$

$$I_p = \frac{Kp}{2} \left[g(V_{IN} - V_{DD} - V_{TO,p})(V_o - V_{DD}) - (V_o - V_{DD})^2 \right] = 0$$

$$V_o = [V_{DD} = V_{OH}]$$

② V_{OL} (last row)

$$I_p = I_n$$

$$I_n = \frac{Kn}{2} \left[g(V_{IN} - V_{TH,n})V_{out} - V_{o^2} \right]$$

$$= \frac{Kn}{2} \left[g(V_{DD} - V_{TH,n})V_o - V_{o^2} \right]$$

$$I_p = 0 \rightarrow \text{cut off}$$

$$I_n = 0 \leftarrow I_p$$

$$V_o = 0$$

$$[V_{OL} = 0]$$

③ V_{IL} (second row)

$$I_p = \frac{Kp}{2} \left[g(V_{IN} - V_{DD} - V_{TO,p})(V_o - V_{DD}) - (V_o - V_{DD})^2 \right]$$

$$I_n = \frac{Kn}{2} \left[g(V_{IN} - V_{TH,n})^2 \right]$$

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$I_p = I_n$

$K_p \left[g(V_{in} - V_{DD} - V_{to,p}) (V_o - V_{DD}) - (V_o - V_{DD})^2 \right] = K_n (V_{in} - V_{DD})$

by diff $\frac{dV_{out}}{dV_{in}}$

$K_p \left[g(V_o - V_{DD}) (V_{in} - V_{DD} - V_{to,p}) \frac{dV_{out}}{dV_{in}} - g(V_o - V_{DD}) \frac{dV_{out}}{dV_{in}} \right] = K_n \cdot g (V_{in} - V_{to,n})$

$\frac{dV_{out}}{dV_{in}} = \frac{K_n}{K_p} \left[g(V_{in} - V_{to,n}) - g(V_{in} - V_{to,p}) \right]$

$\frac{K_p}{K_n} \left[(V_o - V_{DD}) - V_{in} + V_{to,p} + V_{o,p} + V_{o,p} - V_{DD} \right] = g(V_{in} - V_{to,n})$

$\frac{K_p}{K_n} \left[g(V_o - V_{DD}) - V_{in} + V_{to,p} \right] = V_{in} - V_{to,n}$

$V_{in} = V_{IL}$

$-V_{DD} \frac{K_p}{K_n} + \frac{K_p}{K_n} (2V_o) - \frac{(V_{IL}) K_p}{K_n} + \frac{K_p}{K_n} V_{to,p} = V_{IL} - V_{to,n}$

$V_{IL} \left(1 + \frac{K_p}{K_n} \right) = \frac{K_p}{K_n} (2V_o + V_{to,p}) + V_{to,n}$

$V_{IL} = \frac{K_p}{K_n} \left[\frac{g(V_o + V_{to,p})}{-V_{DD}} + V_{to,n} \right] \quad (1 + K_p/K_n)$

(4) V_{IH} (fourth row)

$I_p = \frac{K_p}{2} \left[V_{in} - V_{DD} - V_{tp} \right]^2$

$I_n = \frac{K_n}{2} \left[g(V_{in} - V_{tn}) V_{out} - V_{out}^2 \right]$

$\frac{K_p}{K_n} \left[V_{in} - V_{DD} - V_{tp} \right]^2 = g(V_{in} - V_{tn}) V_{out} - V_{out}^2$

$\frac{K_p}{K_n} \left[V_{in} - V_{DD} - V_{tp} \right] = g(V_{in} - V_{tn}) \frac{dV_{out}}{dV_{in}} + 2V_{out}$

$\frac{K_p}{K_n} \left[V_{in} - V_{DD} - V_{tp} \right] = -g(V_{in} - V_{tn}) + 4V_{out}$

$K_p (V_{in} - V_{DD} - V_{tp}) = -g(V_{in} - V_{tn}) + 4V_{out}$

$K_p (V_{in} - V_{DD} - V_{tp}) = -g(V_{in} + V_{tn} + 2V_{out})$

$V_{in} = V_{IH}$

$\frac{K_p}{K_n} (V_{IH} - V_{DD} - V_{tp}) = -g(V_{in} + V_{tn} + 2V_{out})$

$\frac{K_p}{K_n} (V_{IH} - V_{DD} - V_{tp}) = \frac{K_n}{K_p} (V_{tn} + 2V_{out}) + V_{DD} + V_{tp}$

$V_{IH} = \frac{g(V_{out} + V_{tn} + K_p/K_n (V_{DD} + V_{tp}))}{(1 + K_p/K_n)}$

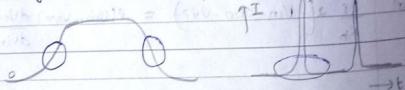
Conclusion:

- O size is reduced

② static power dissipation = $VI = V(I) = 0$
 bcoz in any input $\downarrow V_{DD}$ and ground are shorted.
 $(V_{in}=0, V_{DD})$

- When both the transistor are ON, then we get spikes in the current vs time graph when $V_{in} = V_{th}$, $V_{out} = V_{th}$

$$\text{dynamic power dissipation} = CV^2f$$



- ③ Note is very lesser than the resistor load
 VTC & NM
- ✓ $V_{OH} = V_{DD}$
 - ✓ $V_{OL} = 0$
 - ✓ $V_{IL} = V_{th} - \frac{V_{DD}}{2} = V_{th}$ (we don't getting this)

to getting this

$$④ V_{in} = V_{th}, V_{out} = V_{th}$$

$$I_P = \frac{K_P}{2} \left[2(V_{in} - V_{DD} - V_{top})(V_o - V_{DD}) - (V_o - V_{DD})^2 \right]$$

$$I_{in} = \frac{K_n}{2} \left[2(V_{in}) - V_{th} \right] V_o - V_o^2$$

$$V_{th} = V_{th,m} + \frac{\sqrt{K_P}}{\sqrt{K_n}} \left(V_{DD} - V_{top} \right) \quad ①$$

$$K_R = \frac{K_n}{K_P}$$

$$\left(1 + \frac{\sqrt{K_P}}{\sqrt{K_n}} \right) V_{th} = V_{th,m} + \frac{\sqrt{K_P}}{\sqrt{K_n}} (V_{DD} - V_{top})$$

$$\frac{\sqrt{K_P}}{\sqrt{K_n}} V_{th} - \frac{\sqrt{K_P}}{\sqrt{K_n}} V_{DD} = V_{th,m} - V_{th} - \frac{\sqrt{K_P}}{\sqrt{K_n}} V_{top}$$

$$\frac{\sqrt{K_P}}{\sqrt{K_n}} (V_{th} - V_{DD}) = V_{th,m} - V_{th} - \frac{\sqrt{K_P}}{\sqrt{K_n}} V_{top}$$

$$\frac{\sqrt{K_P}}{\sqrt{K_n}} (V_{th} - V_{DD} + V_{top}) = V_{th,m} - V_{th}$$

$$\frac{1}{K_R} = \frac{K_P}{K_n} = \left(\frac{V_{th,m} - V_{th}}{(V_{th} - V_{DD} + V_{top})} \right)^2$$

$$\frac{1}{K_R} = \left(\frac{V_{th,m} - V_{DD}/2}{V_{DD}/2 - V_{DD} - V_{top}} \right)^2 = 1$$

$$\text{so; } \frac{K_n}{K_P} = 1$$

$$\frac{\mu_n \text{cox} (W/L)_n}{\mu_p \text{cox} (W/L)_p} = 1$$

$(W/L)_n = \frac{\mu_p}{\mu_n}$ → mobility of holes
 $(W/L)_p = \frac{\mu_n}{\mu_p}$ → mobility of electrons

$$\frac{\mu_n}{\mu_p} = \frac{(W/L)_p}{(W/L)_n} = 2.5$$

$$w_p = 2.5 w_n$$

then our inverter is ideal inverter
 so for that we are getting

$$V_{IL} = V_{IH} = V_{Th} = V_{DD}$$

$$N_{ML} = V_{IL}$$

$$N_{MM} = V_{IL}$$

$V_{TO,P} = V_{TO,N}$ → for ideal inverter

By putting this into the eqn of V_{IH}

$$V_{IH} = \frac{2V_0 + V_{TO,N} + K_P k_N (V_{DD} + V_{TO,P})}{1 + (K_P k_N)}$$

$$= \frac{2V_0 + \frac{1}{2}V_{TO,N} + (V_{DD} + V_{TO,P})}{1 + 1}$$

$$V_{IH} = \frac{V_0 + V_{TO} + V_{DD}}{2}$$

$$Ex - V_{DD} = 3.3V, V_{TO,N} = 0.6, V_{TO,P} = -0.7$$

$$k_N = 200, K_P = 80 HA/V^2$$

find out $V_{OH}, V_{OL}, V_{IH}, V_{IL} = ?$

Sol:

$$i) V_{OH} = 3.3V$$

$$ii) V_{OL} = 0$$

$$iii) V_{IL} = \frac{80}{200} \left(2V_0 + (-0.7) - 3.3 \right) + 0.6 \\ 1 + (8/20)$$

$$V_{IL} = \frac{0.4 (8V_0 - 4)}{1.4} + 0.6$$

$$\frac{1}{0.4} (1.4 V_{IL} - 0.6) = 2V_0 - 4$$

$$\frac{1}{0.4} (1.4 V_{IL} - 0.6) + \frac{4}{2} = 8V_0$$

$$2 \times 0.4 V_0 = 1.25 + 1.75 V_{IL}$$

in current eqn:

$$2 \left[2(V_{IL} - 3.3 + 0.7)(V_0 - 3.3) - (3.3 + 4.6)^2 \right] = 5 \\ (V_{IL} - 0.6)^2$$

$$2(V_{IL} - 2.6)(1.25 - 3.3 + 1.75 V_{IL}) - (1.25 - 3.3 + 1.75 V_{IL})^2 \\ = 2.5(V_{IL} - 0.6)^2$$

$$2(V_{IL} - 2.6)(1.75 V_{IL} - 2.05) - (1.75 V_{IL} - 2.05)^2 \\ = 2.5(V_{IL} - 0.6)^2$$

$$V_{IL}^2 - 13.2V_{IL} + 10.66 - 3.06V_{IL}^2 - 4.20 + 3.15 \\ = 2.5V_{IL}^2 + 0.9 - 3V_{IL}$$

$$- 3.06V_{IL}^2 - 3.05V_{IL} + 5.36 = 0$$

$$\begin{aligned} V_{IL} &= 1.06 \\ V_{IL} &= 2.15 \end{aligned}$$

$\therefore V_{out} = 1.35V_{IL} + 1.05 \\ = 3.105 \text{ V Ans.}$

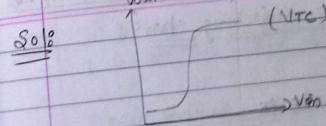
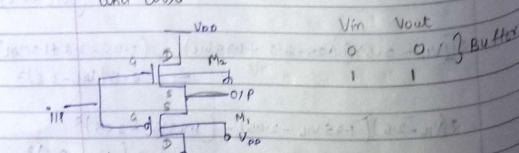
iv) $V_{IH} = 1.39 \text{ V}$

$V_o = 0.2 \text{ V}$

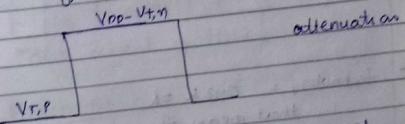
its not ideal inverter bcoz $V_{IH} \neq V_{IL}$

- for ideal inverter $V_{IH} = V_{IL}$ must be.
- if $V_{IH} = V_{o,p}$, then $V_{IL} = V_{IH} \leftarrow$ ideal inverter.

Ex: Draw the IIP , OIP waveform for given CKT and also



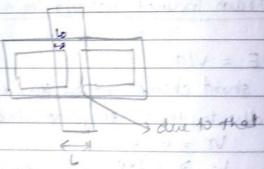
When $Vin = 0$, $M_1 \rightarrow \text{ON}$ & $M_2 \rightarrow \text{cut off}$
 $V_{out} = 0$, then M_1 is in sat. region
so V_T voltage drop is there that
is $V_T > V_{o,p}$
 $V_{DD} - V_{T,n}$



When $Vin = V_{DD}$, $M_1 \rightarrow \text{off}$, $M_2 \rightarrow \text{sat}$
so $V_{T,n}$ voltage drop across the device is
always there.

① - Overlap capacitance

A_{ov} , when distance is less than d , overlapped cap is there.



② junction Capacitance

③ Volt. diff

④ When there is no channel, then cap. b/w gate (neutral) and body \rightarrow mos in cut-off

- mos is in ~~linear~~ ^{linear} ~~cut-off~~ ^{cut-off} ~~saturation~~ ^{saturation} \rightarrow so there is no cap. b/w due to substrate but due to channel (n) there is two capacitances source to gate and drain to gate we are divided.

⑤ mos is in sat \rightarrow channel to gate capacitance

	Cut-off	Linear	Saturation
C_{gb}	$C_{ox}WL$	0	0
C_{gd}	$C_{ox}WL + \frac{1}{2}C_{ov}$	$C_{ox}WL$	$C_{ox}WL$
C_{gs}	$1C_{ox}WL$	$\frac{1}{2}C_{ox}WL + C_{ov}$	$\frac{2}{3}C_{ox}WL + C_{ov}$

$C_{ox}WL_0 \rightarrow$ overlap capacitance

- b/w drain and source no capacitance is there bcz channel is there that is conducting so there is no insulation b/w them.

\hookrightarrow caps connected to source are not present bcz in nmos & pmos substrate bias effect is not there \Rightarrow C_{SD} is not present

C_{DS} is π cap \rightarrow so not considered as effect on off resistance

If WL of pmos & nmos is same \Rightarrow current is different and pmos is slower due to mobility of ee is less \Rightarrow current in pmos is less.

Proposed value
 $t_{PHL} \rightarrow$ time taken to go from low to 50%
 $t_{PLH} \rightarrow$ " " " High to 50%
 \rightarrow defined cost to 0.1P as 1P is assumed to be perfect pulse.

- $V_{DD} \rightarrow V_{OL} + (\text{Highest } K_A 10\%)$
 $V_{DD} \rightarrow V_{OL} + (\text{Highest } K_A 90\%)$

$$\begin{aligned} Q &= CV \\ I &= \frac{dQ}{dt} = CV \end{aligned}$$

$$T = \frac{CV}{I}$$

- The eqn in "slide-11" of avg. current can be used to calculate time delay because current T_{se} & I varies exponentially. So taking half of value for avg. does not give exact avg., in fact its an very rough estimate.

- (Slide-13) Pdn

↳ bcoz current flows from cap to mms while discharging.

Propagation time depends on net capacitive and interconnection of length.

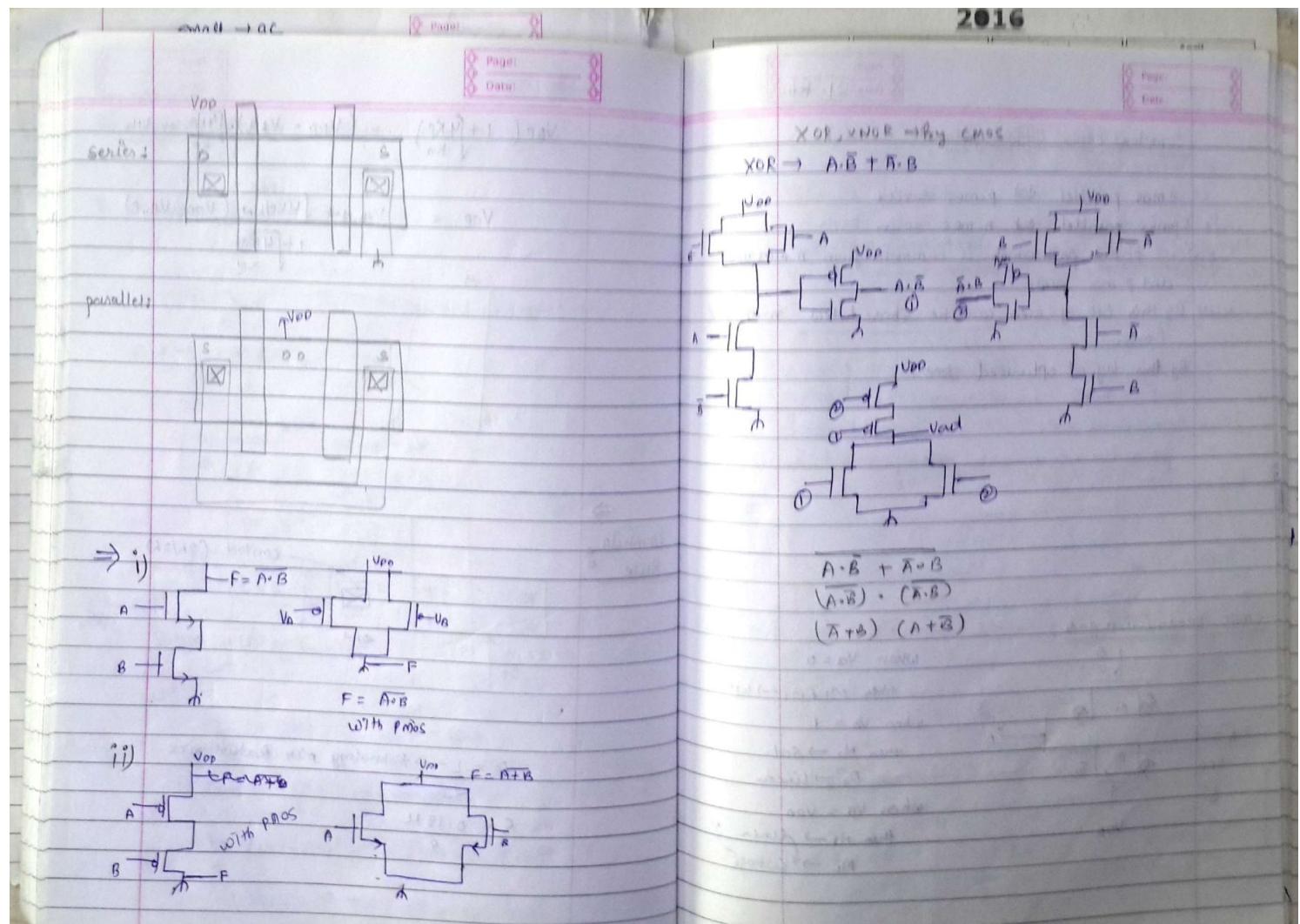
Cload does not changes much

\Rightarrow propagation delay is independent.

$$C_{load} = 2\pi \rightarrow \text{normally used}$$

$$\tau = \frac{1}{f} = \frac{1}{2\pi T_p}$$

avg no of inversions



small \rightarrow ac

Page:

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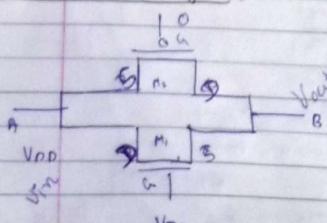
Complex CMOS logic gates

- * n-mos parallel \Leftrightarrow p-mos series
 - * p-mos parallel \Leftrightarrow n-mos series
- Euler's path: path which is common from n-mos n/w and p-mos n/w.
- By this lot of area can be shared b/w n-mos & p-mos.
 - By this layout optimised done.

CMOS transmission gate

- V_{ds} as 2kΩ, then cut off resistance.

CMOS transmission gate



When V_B = 0

then M₁ & M₂ \rightarrow sat.

when V_B = 1

then M₁ \rightarrow Sat.

M₂ \rightarrow linear

when V_B = V_{DD}

then M₁ \rightarrow linear

M₂ \rightarrow cutoff

n-mos

$$V_{DSN} = V_{DD} - V_{out}$$

$$V_{GSN} = V_{DD} - V_{out}$$

n-mos saturation

$$V_{DD} - V_{t,n} > V_{out} \rightarrow \text{sat.}$$

$$V_{DD} - V_{t,n} < V_{out} \rightarrow \text{turned off}$$

R₁

R₂

p-mos

$$V_{DSP} = V_{out} - V_{DD}$$

$$V_{GSP} = -V_{DD}$$

p-mos saturation

$$V_{out} < |V_{t,p}| + \text{sat.}$$

$$V_{out} > |V_{t,p}| \rightarrow \text{linear}$$

n-mos

p-mos

n-mos — sat.

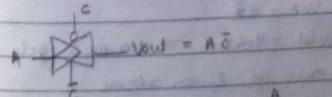
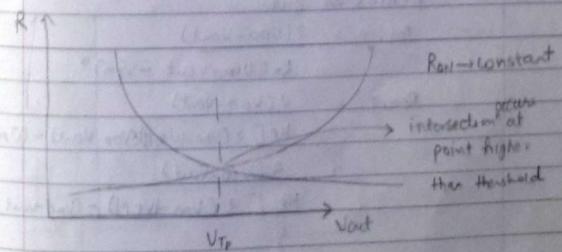
p-mos — linear

n-mos — cutoff

p-mos — linear

saturation

1V 4V 5V



$$\bar{A}B + A\bar{B}$$

$$= A\bar{B} + A\bar{B}$$

$$= AB + A\bar{B}$$

$$= A$$

$$= \bar{A}$$

$$= B$$

$$= \bar{B}$$

$$= C$$

$$= \bar{C}$$

$$= A$$

$$= \bar{A}$$

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$$= \bar{B}$$

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Small \rightarrow ac

08-Feb-08

$$k_n > (0.25) K_p$$

$$\text{Req. } n = \frac{V_{DD} - V_{out}}{I_{os,n}}$$

$I_{os,n}$

$$\text{Req. } p = \frac{V_{DD} - V_{out}}{I_{os,p}}$$

$I_{os,p}$

Large signal
resistance

Region-1 \rightarrow p-mos & n-mos in sat.

$$\text{Req. } n = \frac{2(V_{DD} - V_{out})}{K_n(V_{DD} - V_{out} - V_{Tn})^2}$$

$$K_n(V_{DD} - V_{out} - V_{Tn})^2$$

$$\text{Req. } p = \frac{2(V_{DD} - V_{out})}{K_p(V_{DD} - V_{out})^2}$$

$$K_p(V_{DD} - V_{out})^2$$

Region-2 \rightarrow p-mos in linear

n-mos in sat.

$$\text{Req. } n = \frac{2(V_{DD} - V_{out})}{K_n(V_{DD} - V_{out} - V_{Tn})^2}$$

$$K_n(V_{DD} - V_{out} - V_{Tn})^2$$

$$\text{Req. } p = \frac{2(V_{DD} - V_{out})}{K_p(V_{DD} - V_{out})^2}$$

$$K_p[(2(V_{DD} - V_{T,p}))V_{DD} - V_{out}] - (V_{DD} - V_{out})^2$$

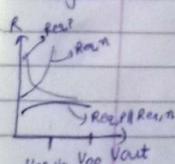
$$= \frac{2(V_{DD} - V_{out})}{K_p[(2(V_{DD} - V_{T,p})) - (V_{DD} - V_{out})]}$$

$$K_p[(2(V_{DD} - V_{T,p})) - (V_{DD} - V_{out})]$$

Region-3 \rightarrow let $V_{DD} = 5V$

$$V_{out} > 4.5V$$

\Rightarrow n-mos gets cut off



$$\text{Req. } p =$$

$$K_p \left[\frac{2(V_{DD} - V_{T,p}) - (V_{DD} - V_{out})}{V_{DD} - V_{out}} \right]$$

$$K_p \left[\frac{2(V_{DD} - V_{T,p}) - (V_{DD} - V_{out})}{V_{DD} - V_{out}} \right]$$

2016

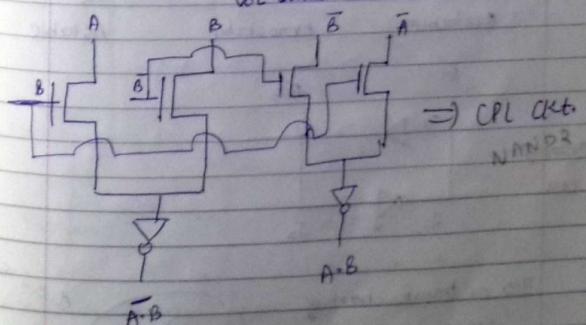
Complementary pass-transistor logic (CPL)

- Only n-mos are used
- All i/p's are in complementary form.
- static power dissipation for CMOS logic is zero as when i/p is 0 \rightarrow p-mos is on when i/p is 1 \rightarrow n-mos is on \Rightarrow never short ckt occurs i.e., when V_{DD} and ground is connected directly \Rightarrow no leakage current.

Whereas in CPL \Rightarrow power dissipation occurs

In CPL \rightarrow area required is less

logic 1 and 0 are not ideal, i.e.,
 $V_{OH} = V_{DD}$ but $V_{OL} \neq 0$ instead its
0.1 to 0.2 ... while in CMOS V_{OH} &
 V_{OL} values are ideal.



- as p-mos are not associated here, speed will be slow

2016

Sequential logic

present o/p depends on

- present i/p
- seq. of previously stored o/p

Sequential logic

```

graph TD
    S[Sequential logic] --> B[Bistable]
    S --> P[Pronestable]
    S --> A[Astable]
    
```

Bistable

Pronestable

Astable

I/O or transfer char. of CMOS inverter

V_{DD} V_{SS}

3rd stable point
stable operating point

loop gain = $\frac{\partial P_1}{\partial V_{DD}} \times \frac{\partial V_{DD}}{\partial P_1} = \frac{1}{0} \times 0 = 0$

⇒ loop gain at stable operating point is very low.

- V_{DD} to ground path is not shorted as at an instant only one cell gets on → energy consumption is low.

Logic 1

Logic 2

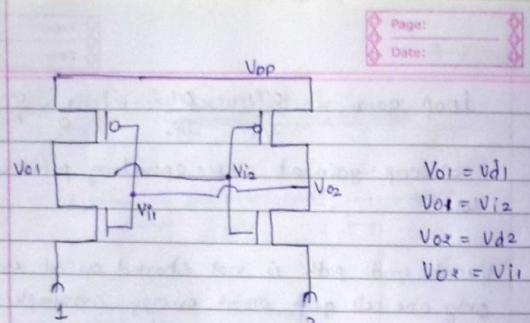
Logic 3

If $V_{DD} = 2.8$, $V_{DD}/2 = 1.4$
then $\Delta t = \Delta t_1$
A small deviation from 2.8×1.4
cause change in SLP

1st i/p $V_{DD} \rightarrow 1st\ o/p$
2nd i/p $V_{DD} \rightarrow 2nd\ o/p$

T-time required

small \rightarrow ac



$$C_g \gg C_d$$

$$V_{g1} = \frac{q_1}{C_g}$$

$$V_{g2} = \frac{q_2}{C_g}$$

$$i_{d1} = g_m V_{g2}$$

$$i_{d2} = g_m V_{g1}$$

$$i_{d1} = i_{d2}$$

$$i_{d2} = i_{d1}$$

$$\therefore i_{d1} = g_m V_{g2} = g_m \left(\frac{q_2}{C_g} \right)$$

$$i_{g1} = g_m V_{g1} = g_m \left(\frac{q_1}{C_g} \right)$$

$$i_{g1} = C_g \frac{dV_{g1}}{dt}$$

$$i_{g2} = C_g \frac{dV_{g2}}{dt}$$

$$g_m V_{g2} = C_g \frac{dV_{g1}}{dt}$$

$$g_m V_{g1} = C_g \frac{dV_{g2}}{dt}$$

$$g_m \frac{q_2}{C_g} = C_g \frac{d(q_1/C_g)}{dt}$$

$$g_m \frac{q_1}{C_g} = \frac{dq_2}{dt}$$

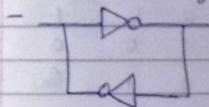
$$g_m \frac{q_2}{C_g} = \frac{dq_1}{dt}$$

2016

14 - March

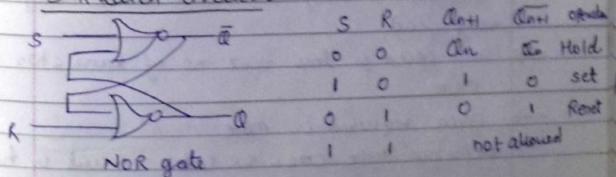
Behaviour of bistable elements:

- S-RAM memory

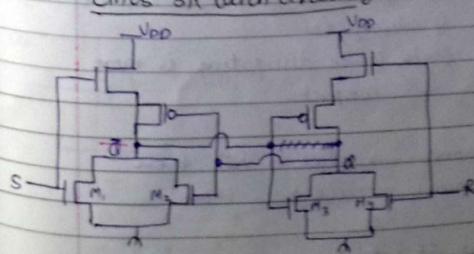


- two identical cross-coupled inverter

S-R latch circuit:



CMOS SR latch circuit:



Small \rightarrow ac

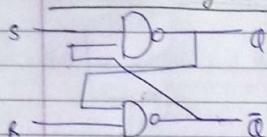
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2016

Month: April

Page: _____ Date: _____

SR latch using NANDs

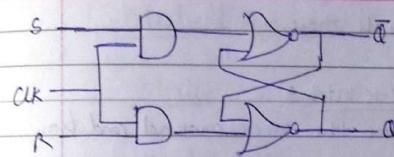


S	R	Q	Q-bar	Condition
0	0	Not allowed		
0	1	1	0	Set
1	0	0	1	Reset
1	1	Qn	Qn	Memory

- static power dissipation in CMOS is very low (bcz in CMOS VDD to ground is not shorted in any case)
- static power dissipation = 0
- So for ^{CMOS} SR latch using NOR and N-NAND, static power dissipation is very low and noise margin is very good.
- and speed is less bcz no of transistors is more.
- area required is more
- depletion type CMOS SR latch circuit is having
 - noise margin is poor
 - leakage is always there bcz depletion type transistors is always ON
 - static power dissipation is more
 - it's compact

Asynchronous \rightarrow clock is not there
Synchronous \rightarrow clock is there

Clocked SR latch:



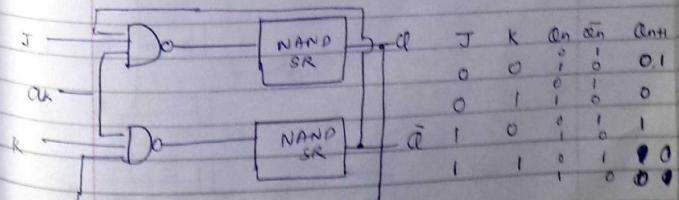
- When CLK = 0

- i/p signal not influence upon the ckt response
- O/P holds its current state

- When CLK = 1

- when S=1, Q=1
- R=1; Q=0

Clocked JK latch:



J	K	Q	Q-bar	Condition
0	0	1	0	0, 1
0	1	0	1	0, 1
1	0	1	0	1, 0
1	1	0	1	1, 0

J	K	Q	Q-bar	Condition
0	0	1	0	Hold
0	1	0	1	Reset
1	0	1	0	Set
1	1	0	1	Toggle

Small \rightarrow a.C

Page: 2

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Date: _____

- Race around will there

Master Slave J-K latch :

- To overcome the race around condition.

D-F/F :

2016

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Date: 11-April

Static & Dynamic logic :

Static

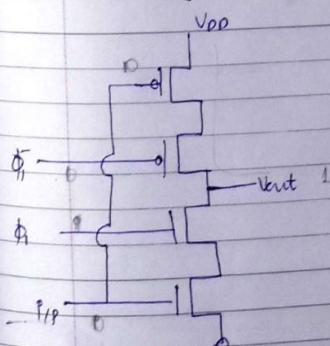
- no need of clock
- O/P are gen'ed in response to i/p voltage level after a time delay

Dynamic

- Clock is required
- operation depends on temporary storage of charge in parasitic node capacitances.
- less dynamic power
- smaller silicon area
- synchronise

18-April

- CMOS dynamic



When $\phi_1 = 0$, then capacitor is charged through the V_{DD}
↓
Precharge (when $\phi_1 = 0$)
When $i_{IP} = 1$, $\phi_1 = 1$
(evaluate)

→ P.E. Gate

- Precharge (ϕ_1 - Clock is low)
- Evaluation (Clock ϕ_1 is High)
(O/P is only available when clock is high)

- By using PE gate propagation delay will reduce or not there. And When OIP is high, node is already charged through the VDD
- floating node, which is not connected to ground and VDD. (floating \rightarrow High impedance)
- Domino logic gate \rightarrow first stage \rightarrow NOT gate \rightarrow second stage

$$T = \frac{CV}{I}$$

- The eqn in "slide-11" of avg. current can be used to calculate time delay because current I_{se} & I_{ce} exponentially. So taking half of value for avg. does not give exact avg., in fact its an very rough estimate.
- (Slide-13) I_{dn}
When current flows from cap to nMOS while discharging.

Propagation time depends on net capacitance and interconnection of length.
 C_{load} does not charges much
 \Rightarrow propagation delay is independent.

$$C_{load} = 2H \rightarrow \text{normally used}$$

$$f = \frac{1}{T_p} = \frac{1}{2nT_p}$$

avg. T_p of invertors

- transistor is having its own resistor and capacitor
- resistance may be neglected.

Estimation of interconnection Parameters:

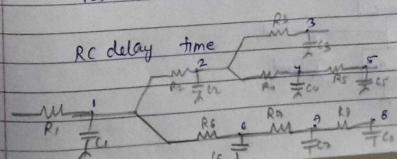
- interconnection having R, L, C
- distributed components: throughout the length resistance is diff' at high speed.
- lumped components: throughout the length resistance value is same.
- $T_{rise} (\Sigma R_{all}) < 2.5 \left(\frac{l}{v} \right)$ \Rightarrow (transmission-line modelling)
 then we have to used distributed parameters.
- $2.5 \left(\frac{l}{v} \right) < T_{rise} < 5 \left(\frac{l}{v} \right)$ \Rightarrow (either transmission-line or lumped modeling)

- thicker the oxide, lesser the capacitance

$$\text{RC time constant: } V_{out}(t) = V_{DD} (1 - e^{-(t/RC)})$$

$$V_{DDOL}(t) = V_{DD} (1 - e^{-tPHL/RC})$$

for transistor we only consider the capacitors



"elmost delay"

for at 8

$$R(t)_{eq} = R_1 C_1 + (R_1 + R_6) (C_6 + (R_1 + R_6 + R_2) C_9 + (R_1 + R_6 + R_2 + R_8) C_4 + R_1 C_2 + R_1 C_3 + R_1 C_4 + R_1 C_5)$$

for at 2

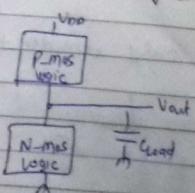
$$R(t)_{eq} = R_1 C_1 + (R_1 + R_6) (C_6 + R_1 + R_2 + R_6) C_7 + R_1 C_8 + R_1 C_2 + C_3 + C_4 + C_5$$

for at 5

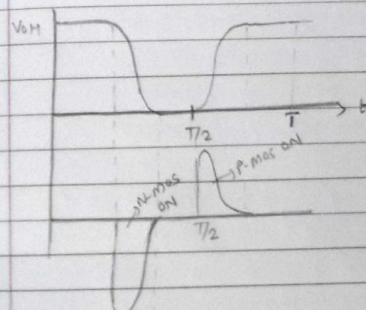
$$R(t)_{eq} = R_1 C_1 + (R_1 + R_2) C_2 + (R_1 + R_2 + R_4) C_4 + (R_1 + R_2 + R_4 + R_5) C_5 + (R_1 + R_2) C_3 + R_1 C_6 + C_7 + C_8$$

$$T_D = \sum_{j=1}^n C_j \sum_{k=1}^l R_k$$

Slow Power of CMOS inverter:



n-mos (on) \rightarrow cap. is discharged (-I current)
p-mos (on) \rightarrow " " charged (+I current)



$$\begin{aligned} P_{avg.} &= \frac{1}{T} \int_0^T V(t) I(t) dt \\ &= \frac{1}{T} \left[\int_0^{T/2} V_{out} \left(-C_{load} \frac{dV_{out}}{dt} \right) dt + \int_{T/2}^T (V_{DD} - V_{out}) \left(C_{load} \frac{dV_{out}}{dt} \right) dt \right] \end{aligned}$$

$$= \frac{1}{T} C_{load} V_{DD}^2$$

$$P_{avg.} = C_{load} \cdot f \cdot V_{DD}^2$$

- speed is high \rightarrow dynamic power dominate

$$P = VI + \underset{\text{Static}}{\downarrow} C_{load} \cdot f \cdot V_{DD}^2 \quad \underset{\text{Dynamic}}{\downarrow}$$