Laboratory Report # 1

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Laboratory Exercise Title: Design Flow of Digital Systems

Target Course Outcomes:

CO1: Create descriptions of digital hardware components such as in combinational and sequential circuits using synthesizable Verilog HDL constructs.

CO2: Verify the functionality of HDL-based components through design verification tools.

Exercise 1C:

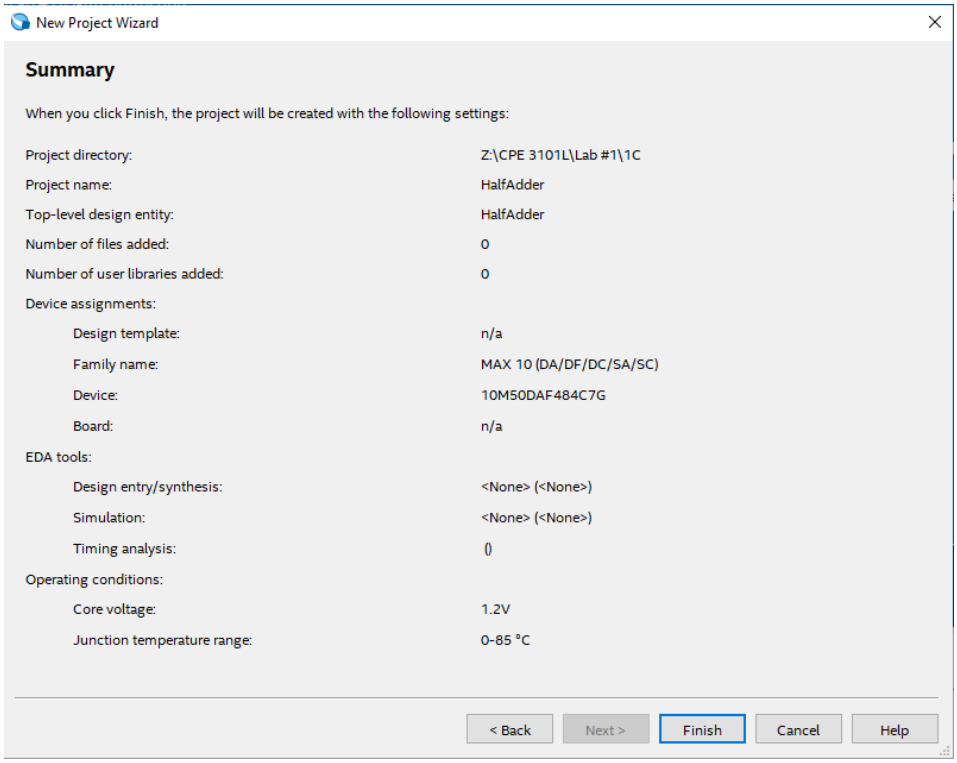

Figure 1: Project Settings Summary of HalfAdder

The project made use of DE-10 Lite board with an Intel Max 10 10M50DAF484C7G FPGA.

HalfAdder.v

```
1   // Machacon, Zach Riane I.
2   // CPE 3101L (Group 2) F 11:00AM - 2:00PM
3   // Verilog HDL code for a half adder circuit
4   //
5   module HalfAdder (x, y, C, S);
6
7       input    x, y;
8       output   C, S;
9       xor      X1 (S, x, y);
10      and      A1 (C, x, y);
11
12  endmodule
```

Figure 2: Design Entry for HalfAdder in Verilog HDL

As indicated by the code, there will be 2 inputs and 2 outputs, along with the use of 1 XOR and 1 AND gate.

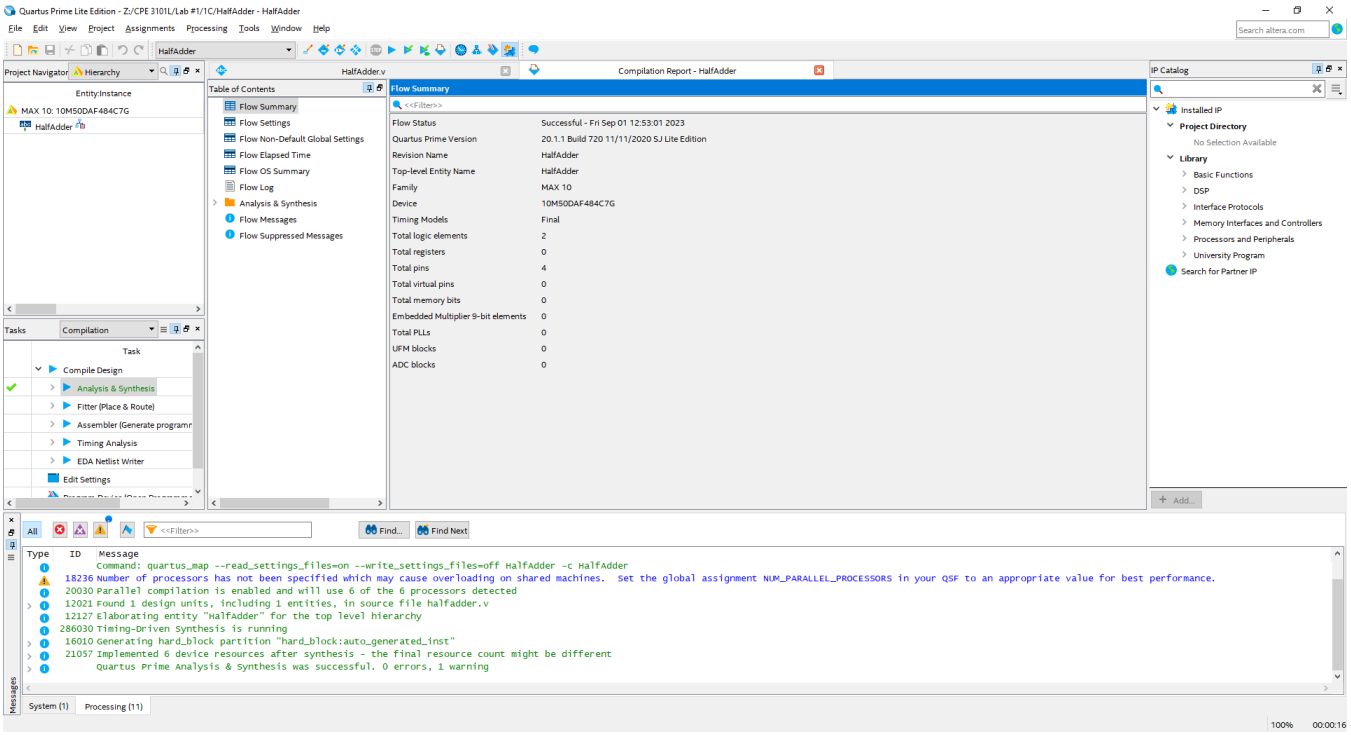

Figure 3: Compilation Report for the Flow Summary of HalfAdder

According to the compilation report, 2 logic elements and 4 total pins are needed. Quartus also found 1 warning, however, it is negligible and does not interfere with the synthesis process.

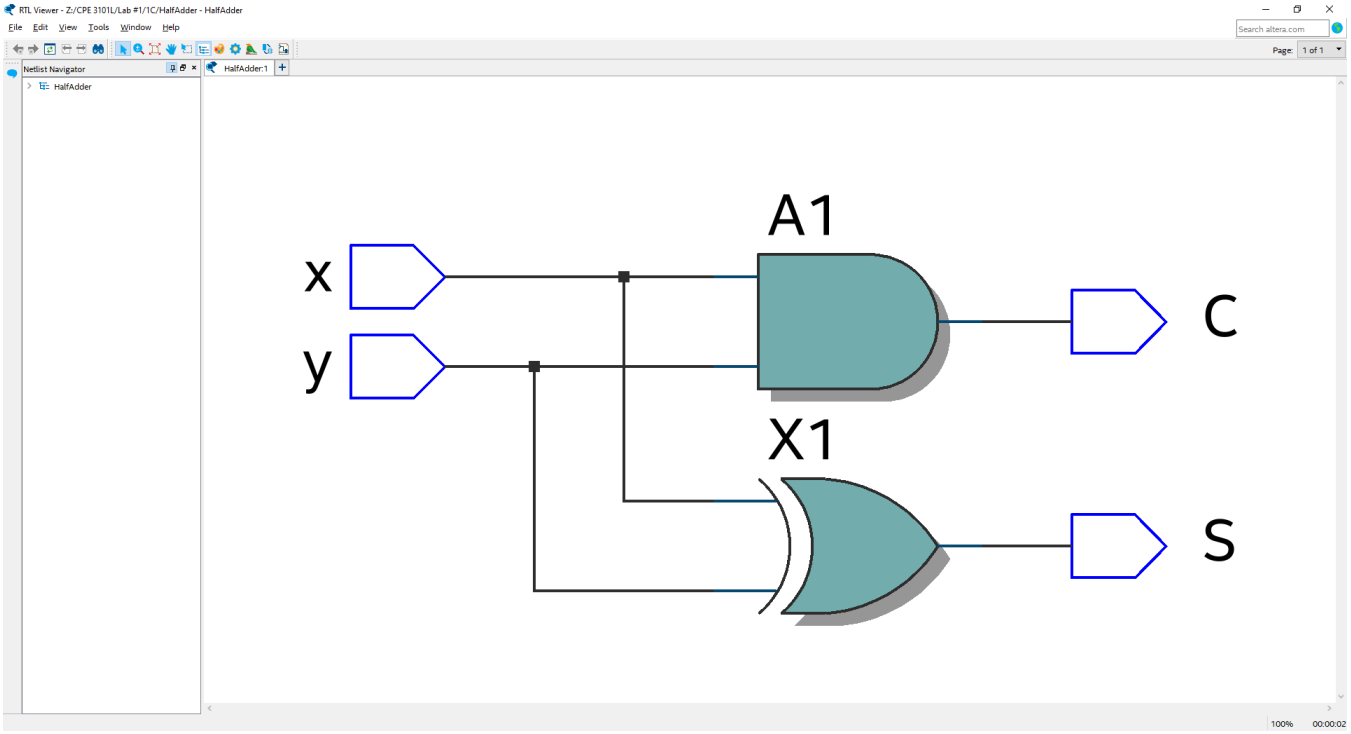

Figure 4: Schematic Diagram of Synthesized Circuit from HalfAdder Project

As expected, a half adder circuit was constructed from the design entry. 2 inputs, x and y, are put into both the XOR and AND gates. The result of the AND gate is the CARRY, and the result of the XOR gate is the SUM.