

## Laboratory Report # 1

**Name:** Machacon, Zach Riane I.

**Date Completed:** September 1, 2023

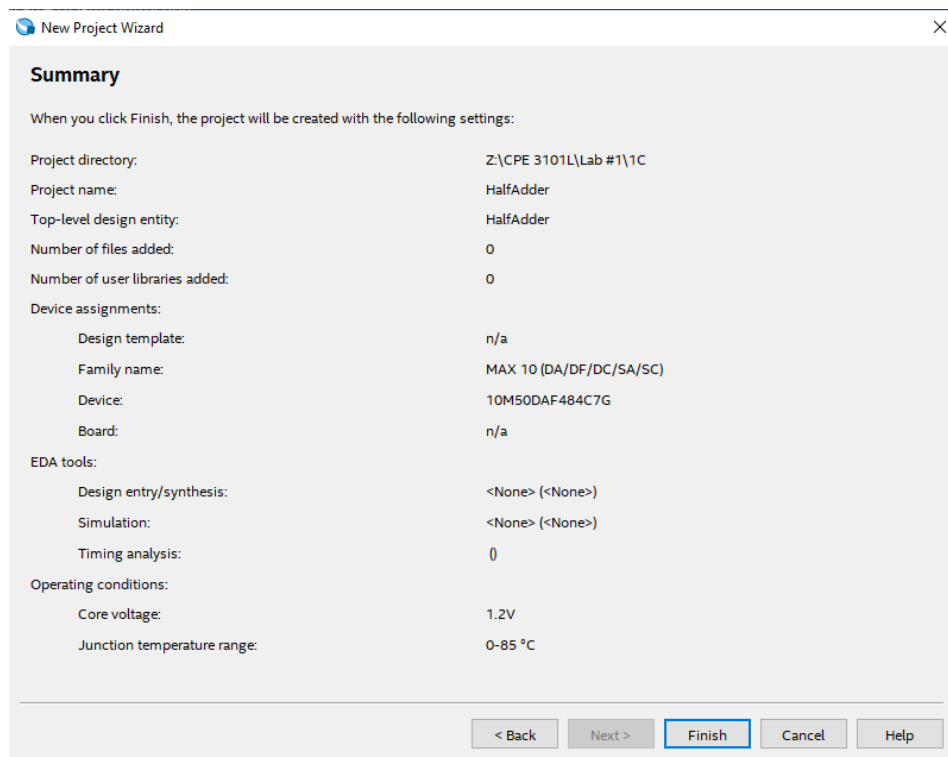
**Laboratory Exercise Title:** Design Flow of Digital Systems

### Target Course Outcomes:

**CO1:** Create descriptions of digital hardware components such as in combinational and sequential circuits using synthesizable Verilog HDL constructs.

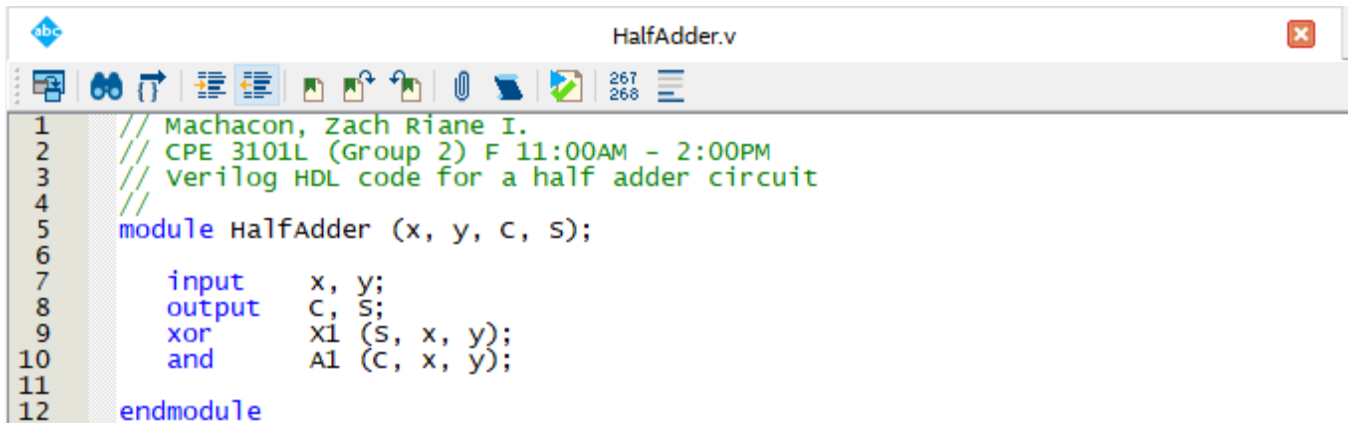
**CO2:** Verify the functionality of HDL-based components through design verification tools.

### Exercise 1C:



**Figure 1: Project Settings Summary of HalfAdder**

The project made use of DE-10 Lite board with an Intel Max 10 10M50DAF484C7G FPGA.

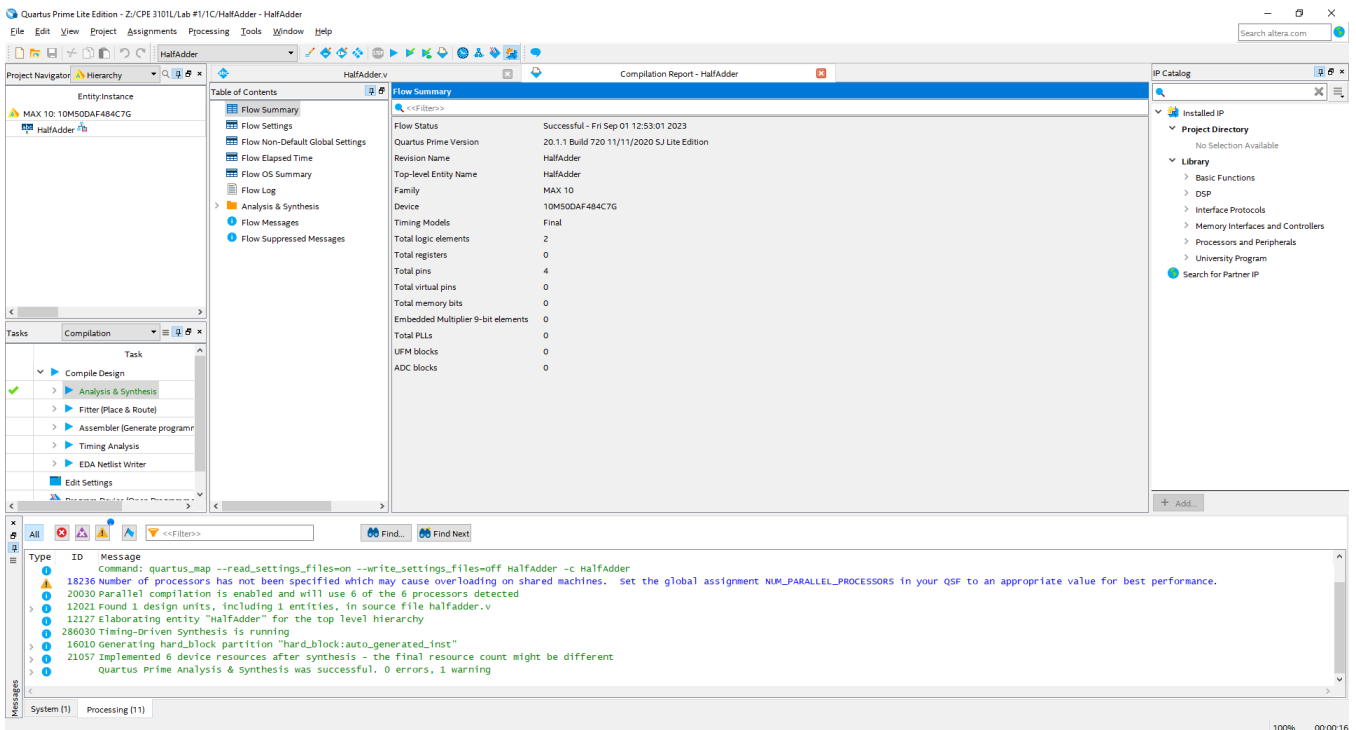


```

1 // Machacon, Zach Riane I.
2 // CPE 3101L (Group 2) F 11:00AM - 2:00PM
3 // Verilog HDL code for a half adder circuit
4 //
5 module HalfAdder (x, y, c, s);
6
7     input    x, y;
8     output   c, s;
9     xor      x1 (s, x, y);
10    and      a1 (c, x, y);
11
12 endmodule
  
```

**Figure 2: Design Entry for HalfAdder in Verilog HDL**

As indicated by the code, there will be 2 inputs and 2 outputs, along with the use of 1 XOR and 1 AND gate.



The screenshot shows the Quartus Prime Lite Edition interface with the 'Flow Summary' report open. The report details the compilation process for the 'HalfAdder' project. Key information includes the successful completion of the synthesis, the use of 2 logic elements and 4 total pins, and a warning about the number of processors.

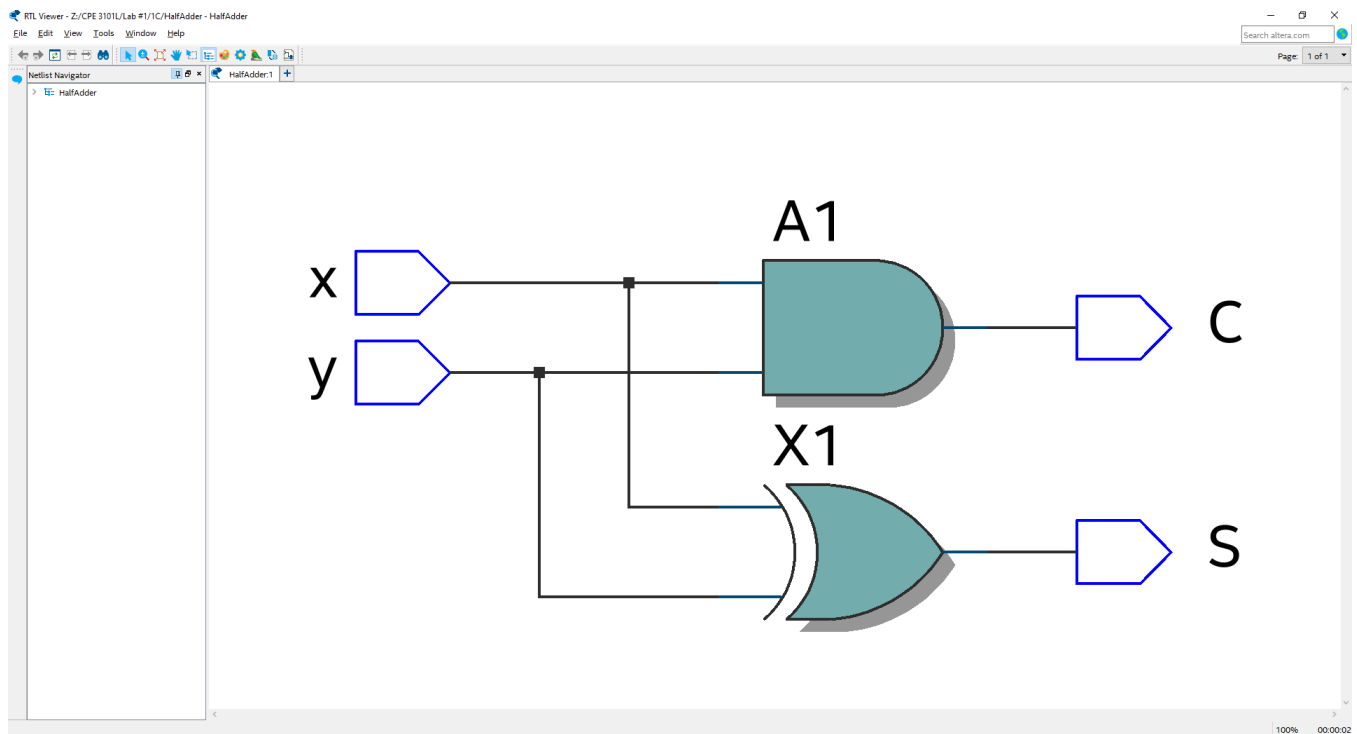
Flow Status	Successful - Fri Sep 01 12:53:01 2023
Quartus Prime Version	20.1.1 Build 720 11/11/2020 SJ Lite Edition
Revision Name	HalfAdder
Top-level Entity Name	HalfAdder
Family	MAX 10
Device	10M50DAF484C7G
Timing Models	Final
Total logic elements	2
Total registers	0
Total pins	4
Total virtual pins	0
Total memory bits	0
Embedded Multiplier 9-bit elements	0
Total PLLs	0
UFM blocks	0
ADC blocks	0

**Messages:**

- Command: quartus\_map --read\_settings\_files=on --write\_settings\_files=off HalfAdder -c HalfAdder
- 18236 Number of processors has not been specified which may cause overloading on shared machines. Set the global assignment NIM\_PARALLEL\_PROCESSORS in your QSF to an appropriate value for best performance.
- 20030 Parallel compilation is enabled and will use 6 of the 6 processors detected
- 12021 Found 1 design units, including 1 entities, in source file halfadder.v
- 12127 Elaborating entity "HalfAdder" for the top level hierarchy
- 286030 Timing-Driven Synthesis is running
- 16010 Generating hard\_block partition "hard\_block:auto\_generated\_inst"
- 21057 Implemented 6 device resources after synthesis - the final resource count might be different
- Quartus Prime Analysis & Synthesis was successful. 0 errors, 1 warning

**Figure 3: Compilation Report for the Flow Summary of HalfAdder**

According to the compilation report, 2 logic elements and 4 total pins are needed. Quartus also found 1 warning, however, it is negligible and does not interfere with the synthesis process.



**Figure 4: Schematic Diagram of Synthesized Circuit from HalfAdder Project**

As expected, a half adder circuit was constructed from the design entry. 2 inputs, x and y, are put into both the XOR and AND gates. The result of the AND gate is the CARRY, and the result of the XOR gate is the SUM.