Laboratory Report # 4

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Laboratory Exercise Title: Dataflow Modeling of Combinational Circuits

Target Course Outcomes:

CO1: Create descriptions of digital hardware components such as in combinational and sequential circuits using synthesizable Verilog HDL constructs.

CO2: Verify the functionality of HDL-based components through design verification tools.

Exercise 3A:

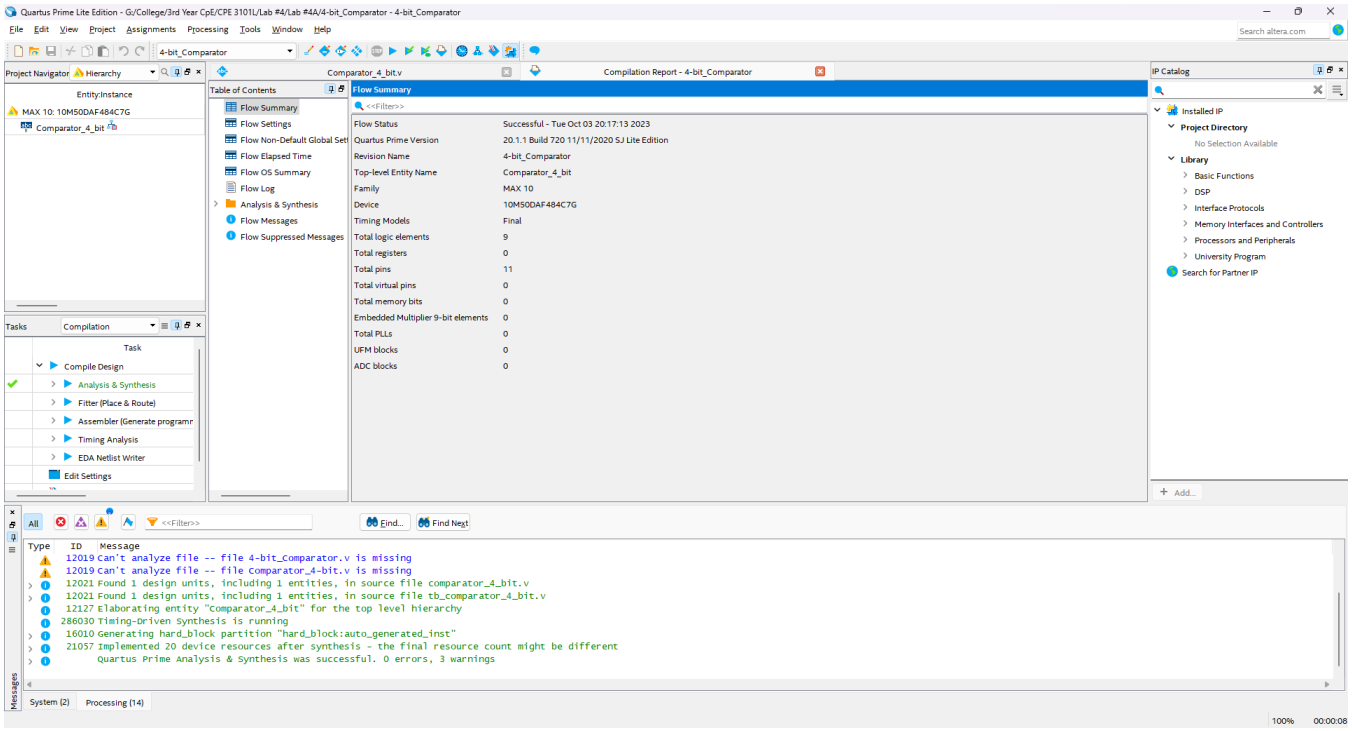

Figure 1: Proof of Successful Design Synthesis of 4-bit Comparator

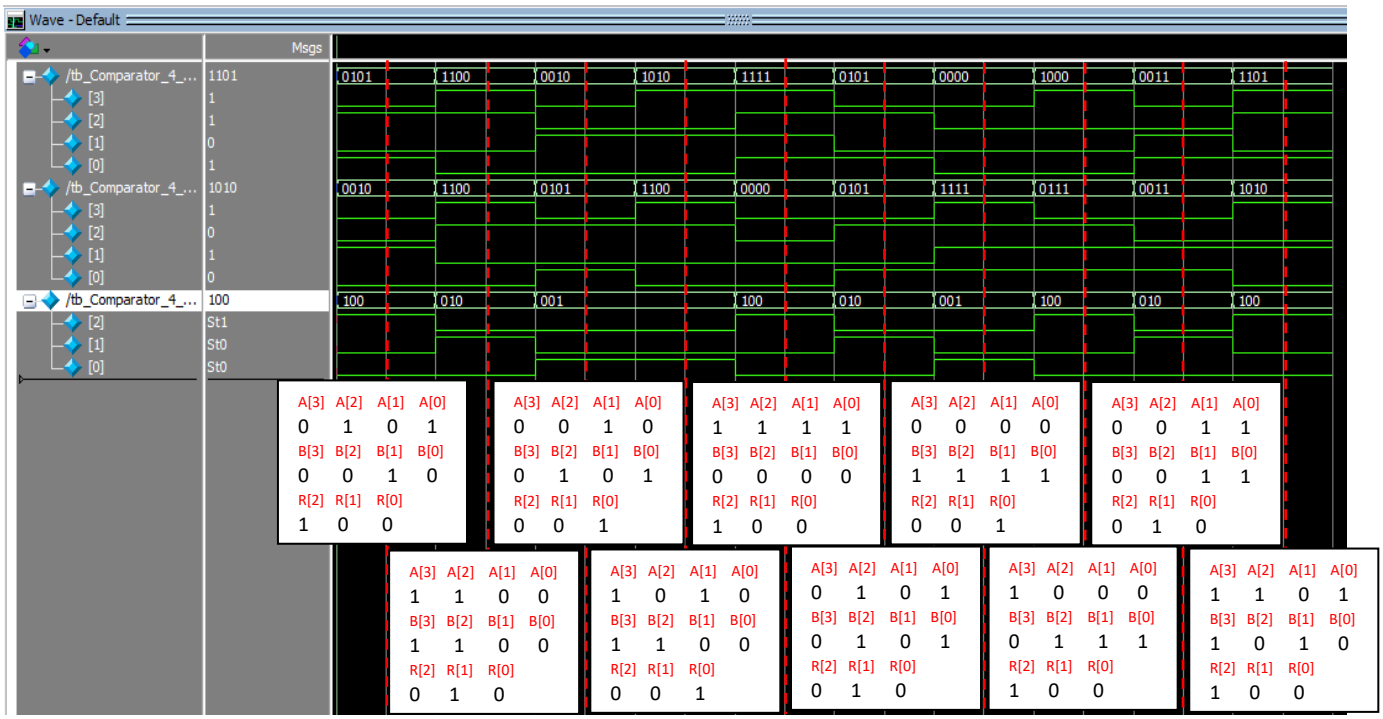

Figure 2: Proof of Successful Simulation Results of 4-bit Comparator

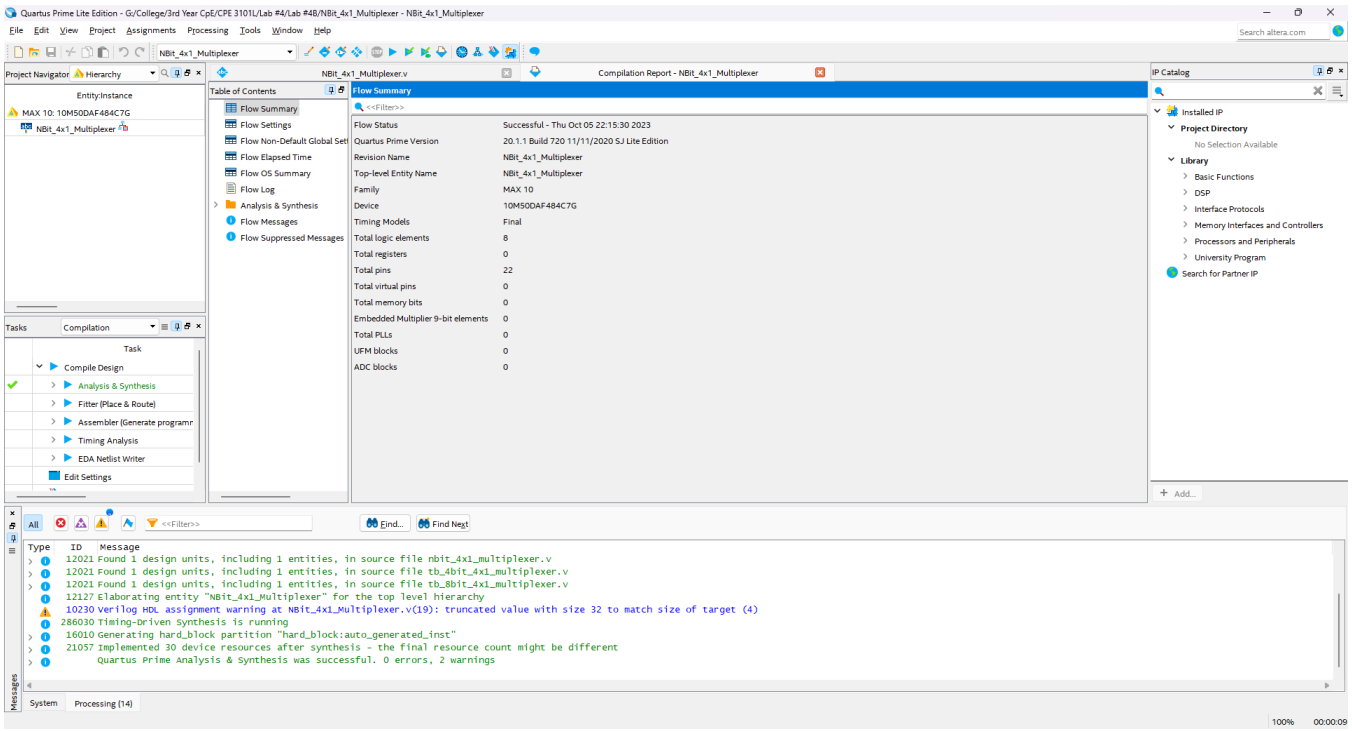

Figure 3: Proof of Successful Design Synthesis of n-Bit 4-to-1 Line Multiplexer

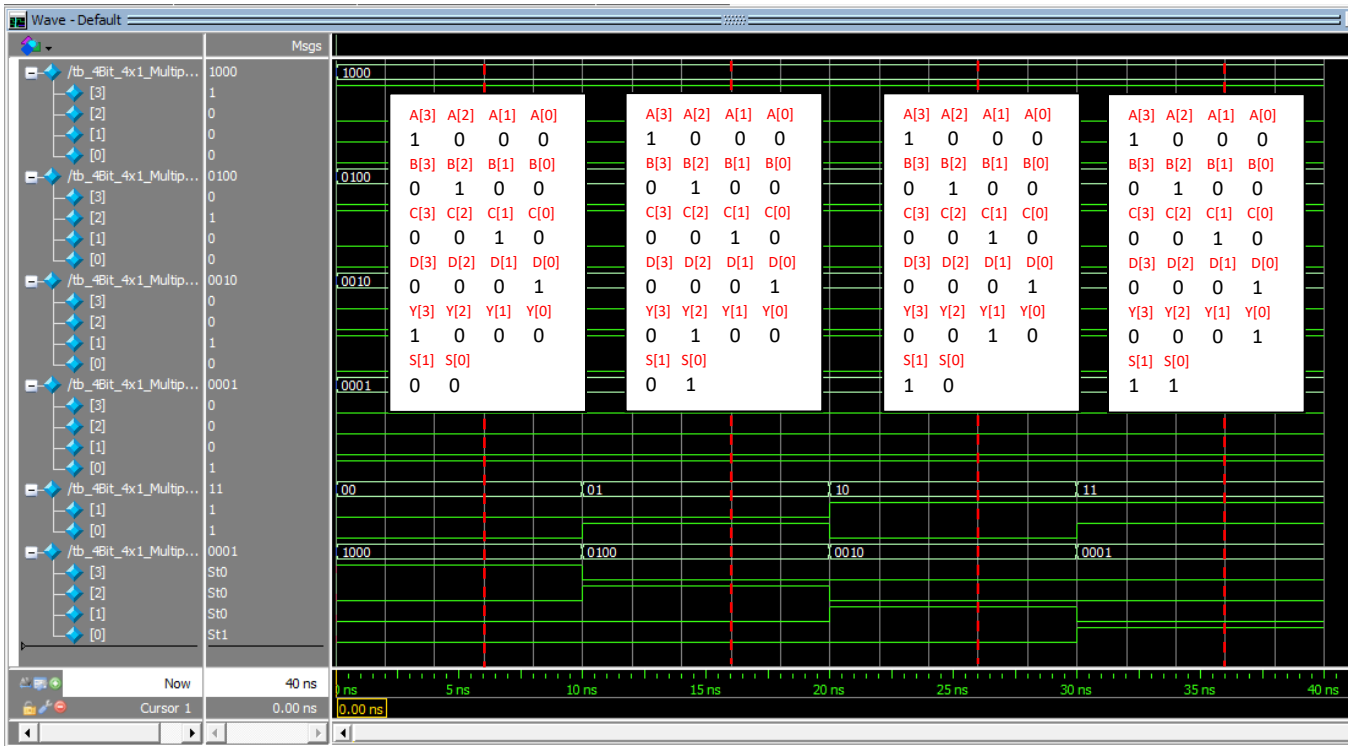

Figure 3: Proof of Successful Simulation Results of 4-Bit 4-to-1 Line Multiplexer

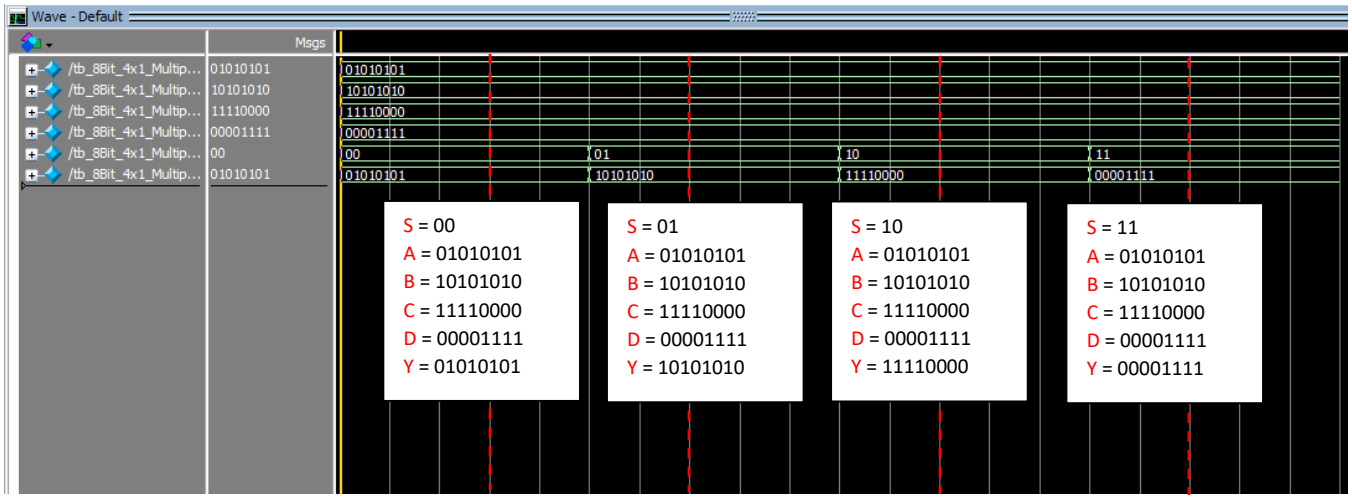

Figure 4: Proof of Successful Simulation Results of 8-Bit 4-to-1 Line Multiplexer