Laboratory Report # 3

Name: Machacon, Zach Riane **Date Completed:** September 22, 2023

Laboratory Exercise Title: Structural Modeling of Combinational Circuits

Target Course Outcomes:

CO1: Create descriptions of digital hardware components such as in combinational and sequential circuits using synthesizable Verilog HDL constructs.

CO2: Verify the functionality of HDL-based components through design verification tools.

Exercise 3A:

Solution:

Truth Table for 2x4 Decoder

E	**A_1**	**A_0**	**D_3**	**D_2**	**D_1**	**D_0**
0	0	0	0	0	0	0
0	0	1	0	0	0	0
0	1	0	0	0	0	0
0	1	1	0	0	0	0
1	0	0	0	0	0	1
1	0	1	0	0	1	0
1	1	0	0	1	0	0
1	1	1	1	0	0	0

Boolean Expressions:

$D_3 = A_1A_0E \quad D_0 = A_1'A_0'E$

$D_2 = A_1A_0'E$

$D_1 = A_1A_0'E$

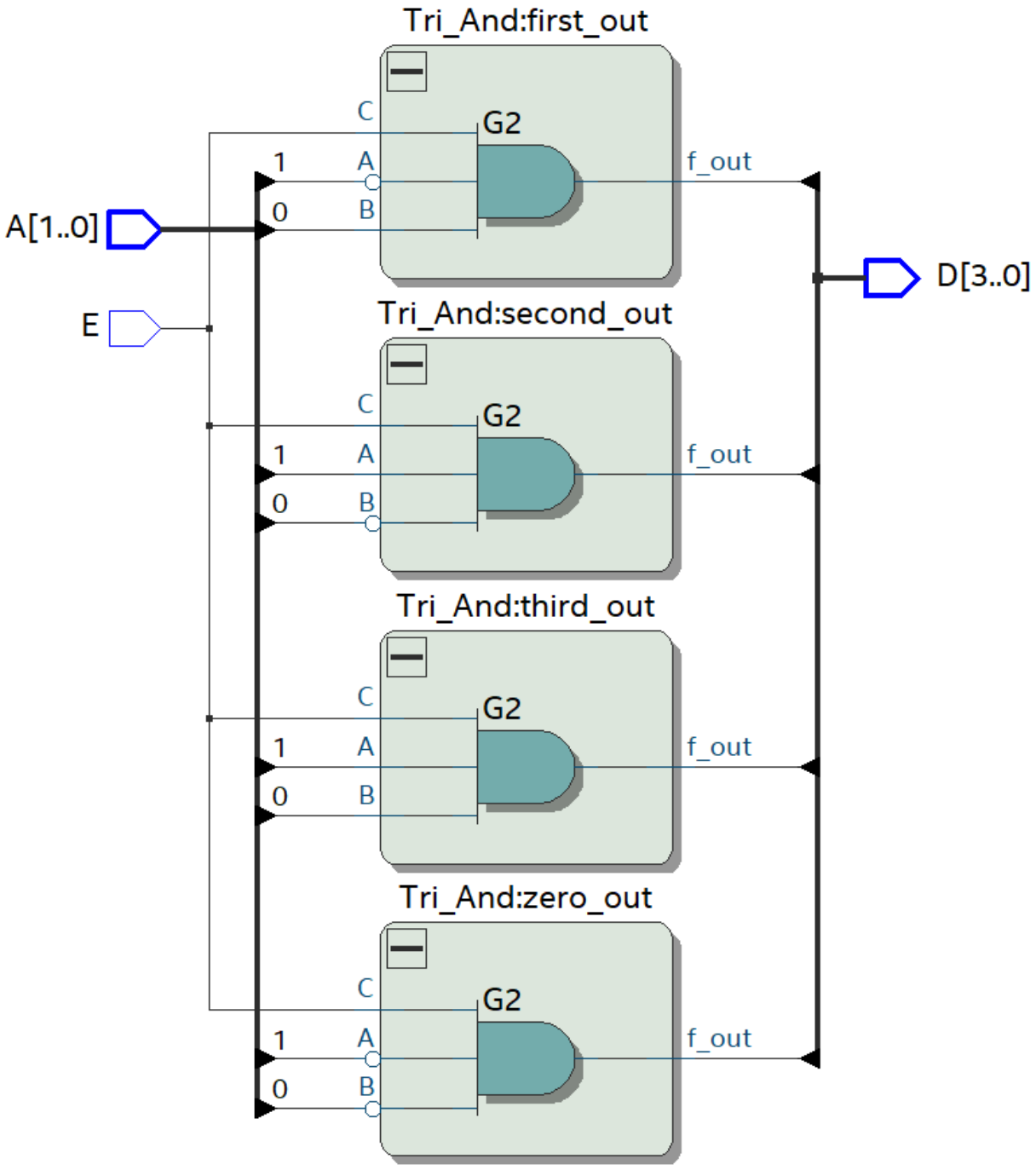

Figure 1: Logic Diagram with Labels of Decoder_2x4

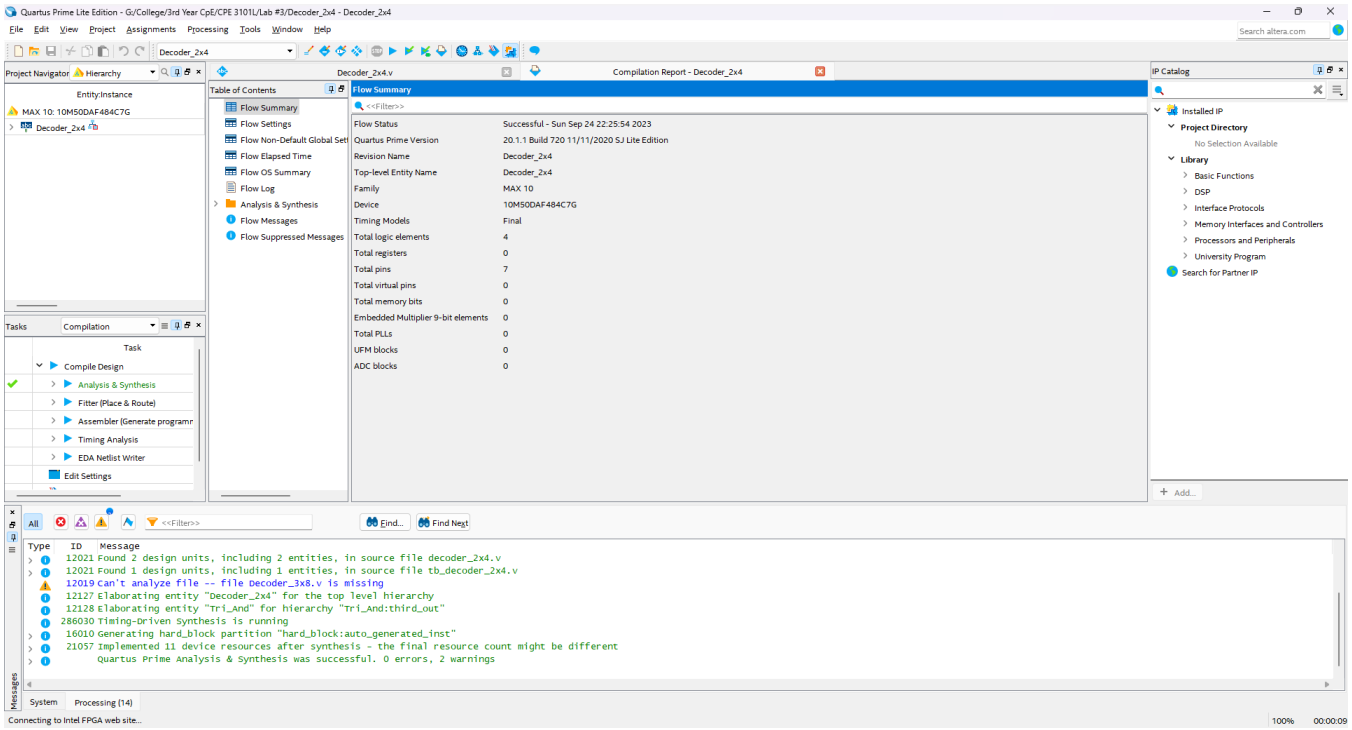

Figure 2: Successful Design Synthesis of Decoder_2x4

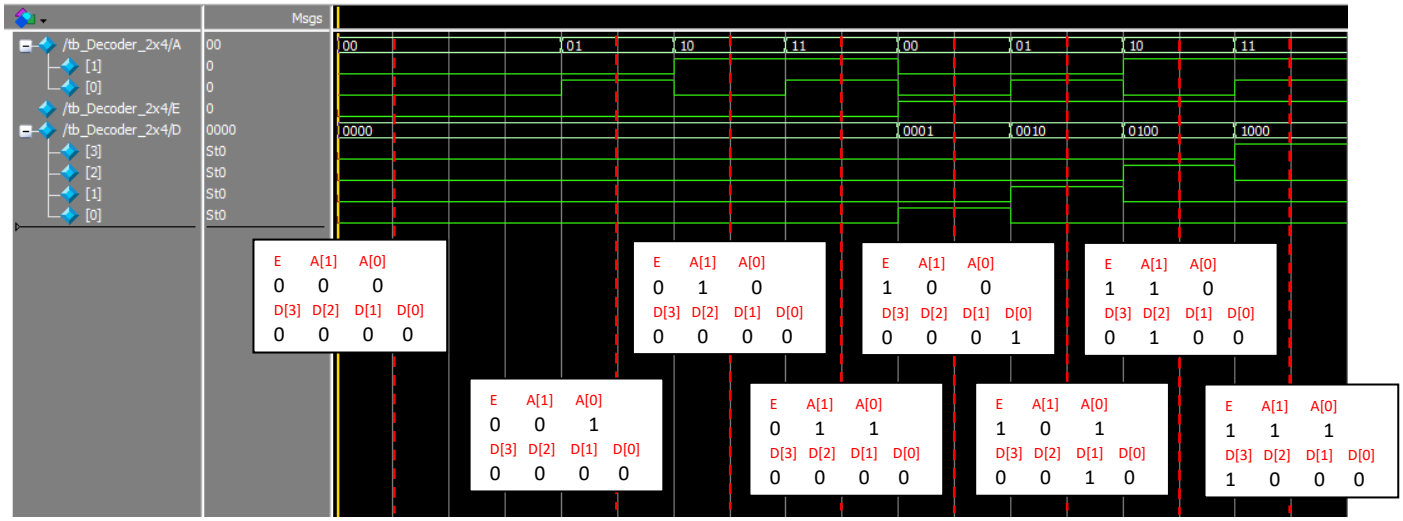

Figure 3: Successful Simulation Results of Decoder_2x4

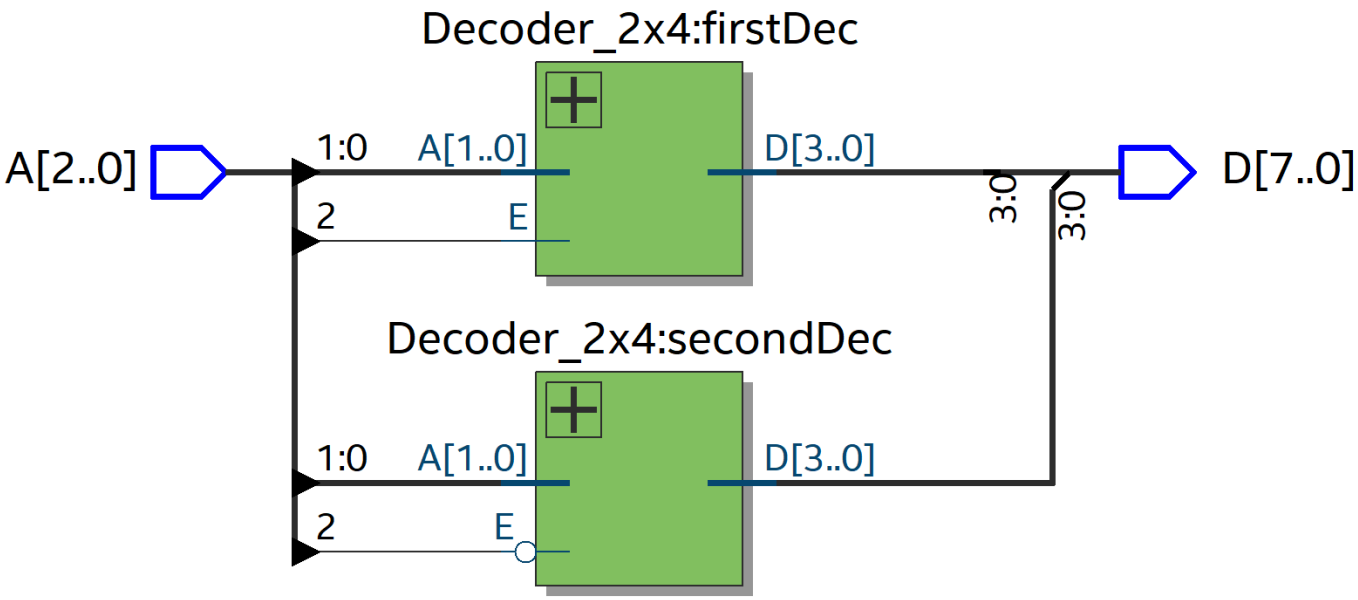

Figure 4: Internal Block Diagram of Decoder_3x8

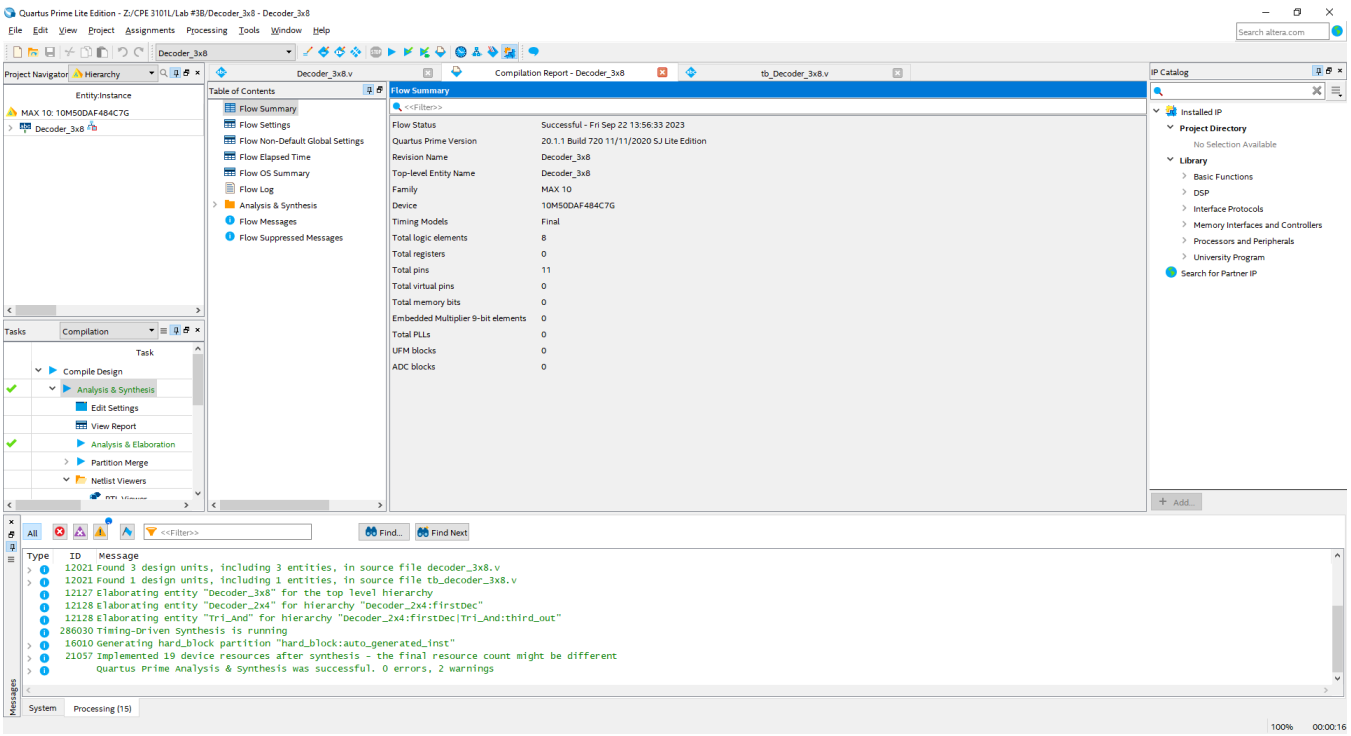

Figure 5: Successful Design Synthesis of Decoder_3x8

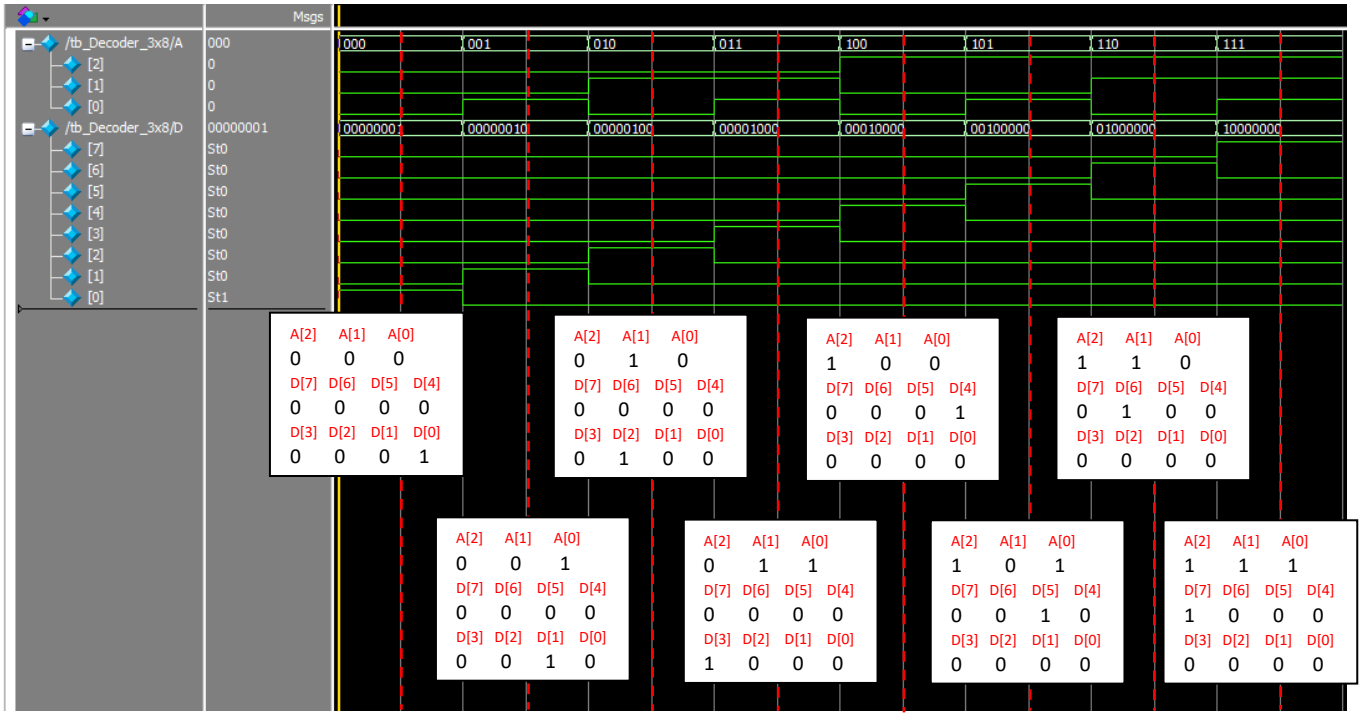

Figure 6: Successful Simulation Results of Decoder_3x8