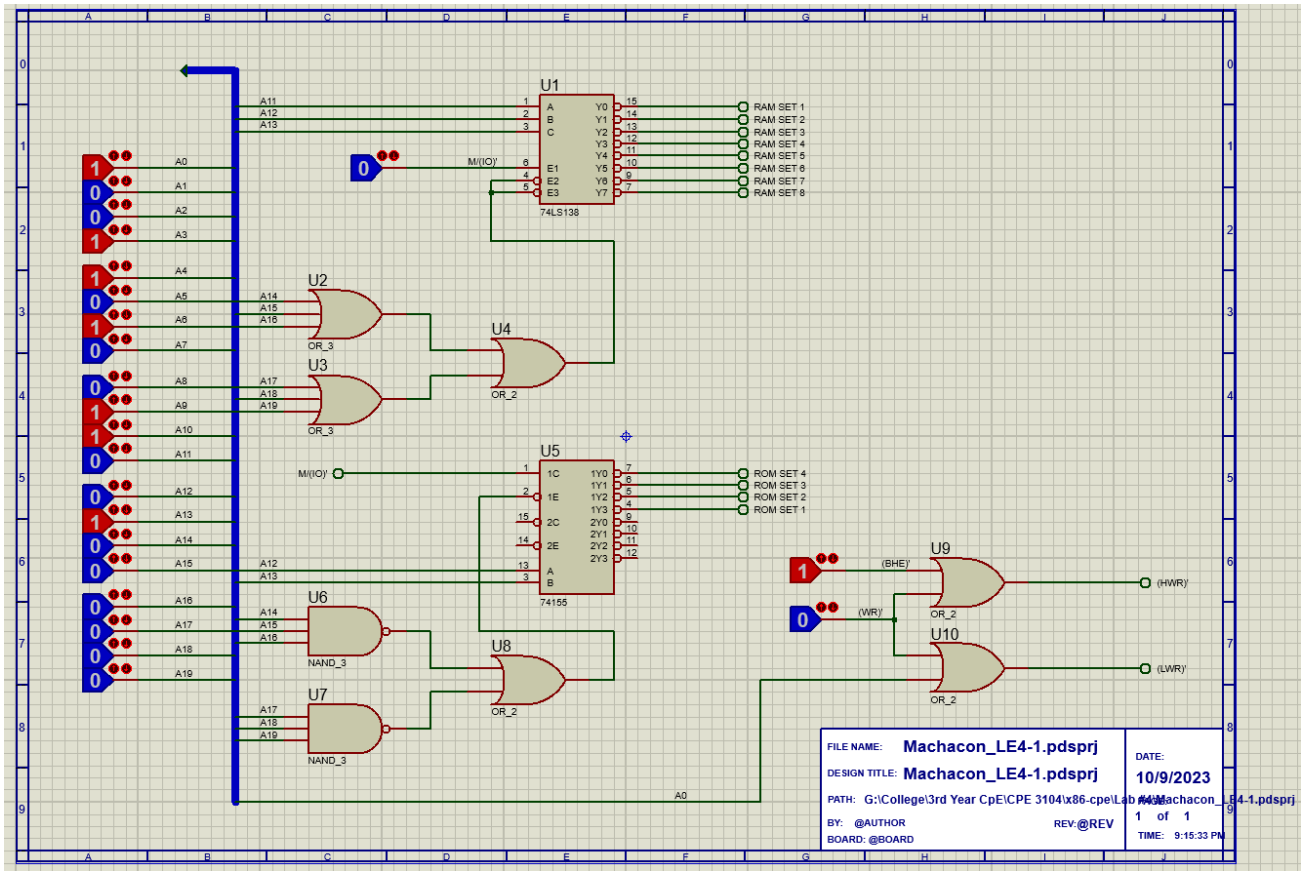
Laboratory Report

Laboratory Exercise No.:	4	**Date Performed:**	October 7, 2023
Laboratory Exercise Title:	Memory Interfacing (with Addressing Decoding)		
Name of Student:	Zach Riane Machacon	**Document Version:**	1.0

Activity #1

Circuit Diagram:



Simulated address decoding and RAM write/read data:

Address (A_{19}…A_0)		$M/\overline{IO}$	$\overline{WR}$	$\overline{BHE}$	**Memory Set Enabled**	$\overline{HWR}$	$\overline{LWR}$	**Observations**
0000 0000 1111 0000 0001	00F01H	1	0	0	RAM Set 2	0	1	high bank 8-bit transfer (write)
1111 1100 0110 1000 0010	FC680H	1	0	1	ROM Set 4	1	0	low bank 8-bit transfer (write)
0000 0101 1010 0111 1100	05A7CH	1	1	0	none	1	1	address out of range
1111 1111 0000 0000 0010	FF002H	0	0	0	none	0	0	Access is isolated since M/IO is logic-0.
0000 0001 1111 1111 1111	01FFFH	1	1	1	RAM Set 4	1	1	No bank enabled; Read operation done
0000 0000 0000 0000 0001	00001H	1	1	0	RAM Set 1	1	1	No bank enabled; Read operation done
1111 1011 1111 0000 0011	FBF03H	1	0	0	none	0	1	high bank 8-bit transfer (write)
0000 0000 1111 1100 1110	00FCEH	0	1	1	none	1	1	Access is isolated since M/IO is logic-0.

0000 0100 0000 0000 0000	04000H	1	0	0	none	0	0	Address is out of range
0000 0010 0110 0101 1001	02659H	1	0	1	RAM Set 5	1	1	No bank enabled

a. How many RAM and ROM chips are used?

ROM: 4 sets * 2 banks = 8 chips

RAM: 8 sets * 2 banks = 16 chips

b. What is the chip size of the RAM and ROM?

RAM: $2^{11} = 2048$ = 2k x 8

ROM: $2^{12} = 4096$ = 4k x 8

c. Determine the address range of the RAM and ROM.

RAM: 00000H - 03FFFH

ROM: FC000H - FFFFFH

d. Based on the number of chips and chip size, calculate and determine the address range (start and end) of each chip sets for both RAM and ROM.

RAM: 007FFH (0 -> 2047)

Set	Start Address	End Address	Address Range
1	00000H	00000H + 007FFH = 007FFH	00000H - 007FFH
2	007FFH + 1 = 00800H	00800H + 007FFH = 00FFFH	00800H - 00FFFH
3	00FFFH + 1 = 01000H	01000H + 007FFH = 017FFH	01000H - 017FFH
4	017FFH + 1 = 01800H	01800H + 007FFH = 01FFFH	01800H - 01FFFH
5	01FFFH + 1 = 02000H	02000H + 007FFH = 027FFH	02000H - 027FFH

6	027FFH + 1 = 02800H	02800H + 007FFH = 02FFFH	02800H - 02FFFH
7	02FFFH + 1 = 03000H	03000H + 007FFH = 037FFH	03000H - 037FFH
8	037FFH + 1 = 03800H	03800H + 007FFH = 03FFFH	03800H - 03FFFH

ROM: 00FFFH (0 -> 4095)

Set	**Start Address**	**End Address**	**Address Range**
1	FFFFFH - 00FFFH = FF000H	FFFFFH	FF000H - FFFFFH
2	FEFFFH - 00FFFH = FE000H	FF000H - 1 = FEFFFH	FE000H - FEFFFH
3	FDFFFH - 00FFFH = FD000H	FE000H - 1 = FDFFFH	FD000H - FDFFFH
4	FCFFFH - 00FFFH = FC000H	FD000H - 1 = FCFFFH	FC000H - FCFFFH

e. Suggest an actual RAM (static RAM) and ROM (EPROM) integrated circuit (IC) with the same size as determined in (b).

RAM: CY7C128A

ROM: 2732

Activity #2

Address Ranges:

RAM: 00000H - 03FFFH (0 -> 16383)

ROM: FC000H - FFFFFH (0 -> 16383)

Sets:

RAM: $\frac{16k}{8k} \cdot 2\ banks = $ **4 RAM chips**

$\frac{4\ RAM\ chips}{2\ banks} =$ **2 RAM sets**

ROM: $\frac{16k}{8k} \cdot 2\ banks = $ **4 ROM chips**

$\frac{4\ ROM\ chips}{2\ banks} =$ **2 ROM sets**

Address Decoding:

RAM: 01FFFH (0 -> 8191)

Set	Start Address	End Address	Address Range
1	00000H	00000H + 01FFFH = 01FFFH	00000H - 01FFFH
2	01FFFH + 1 = 02000H	02000H + 01FFFH = 03FFFH	02000H - 03FFFH

RAM Chip Selection:

Set 1: 0000 0000 0000 0000 0000

0000 0001 1111 1111 1111

Set 2: 0000 0010 0000 0000 0000

0000 0011 1111 1111 1111

^ Chip Selection (A_{13})

ROM: 01FFFH (0 -> 8191)

Set	Start Address	End Address	Address Range
1	FFFFFH - 01FFFH = FE000H	FFFFFH	FE000H - FFFFFH
2	FDFFFH - 01FFFH = FC000H	FE000H - 1 = FDFFFH	FC000H - FDFFFH

ROM Chip Selection:

Set 1: 1111 1110 0000 0000 0000

1111 1111 1111 1111 1111

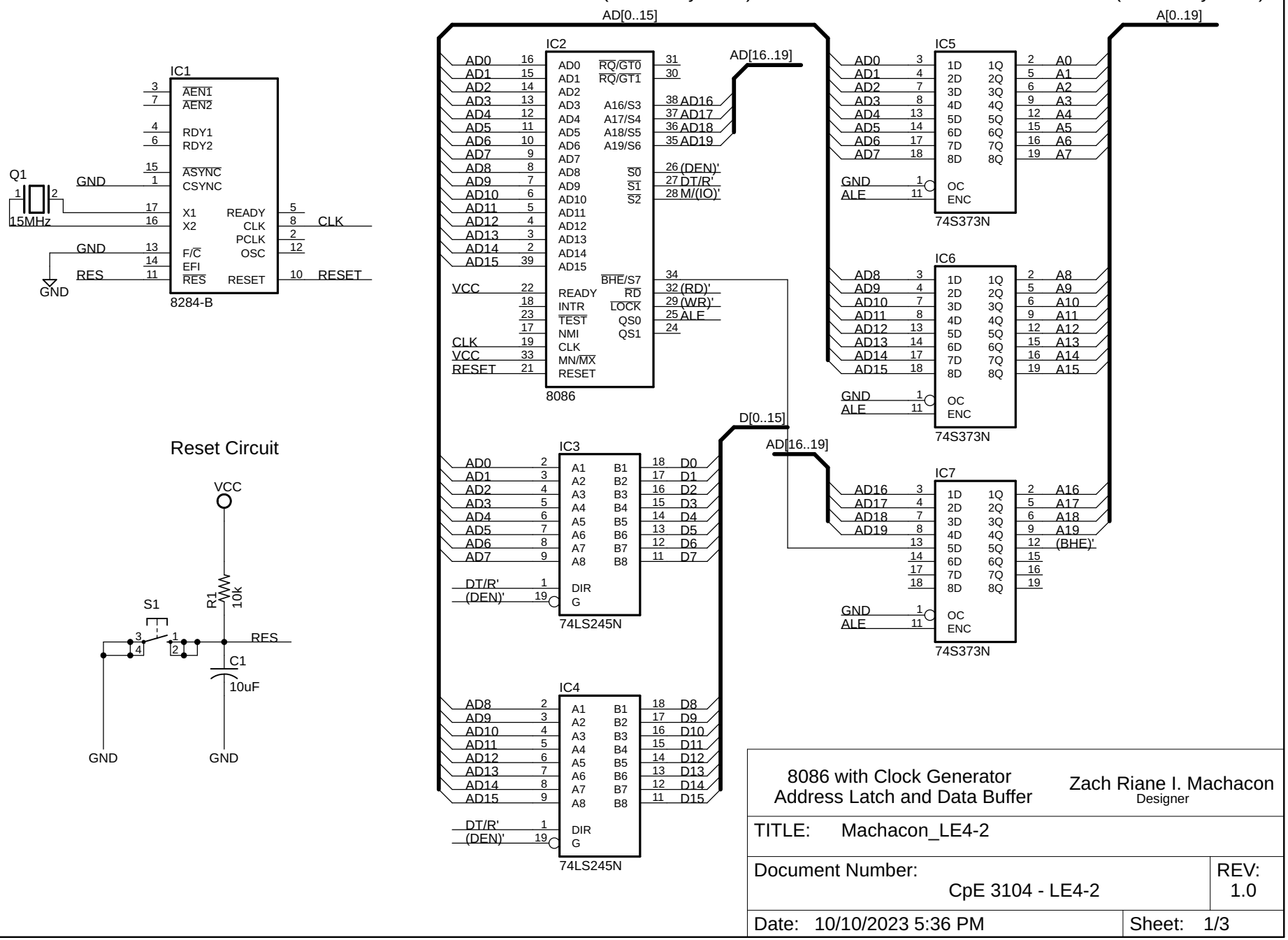
Set 2: 1111 1100 0000 0000 0000

1111 1101 1111 1111 1111

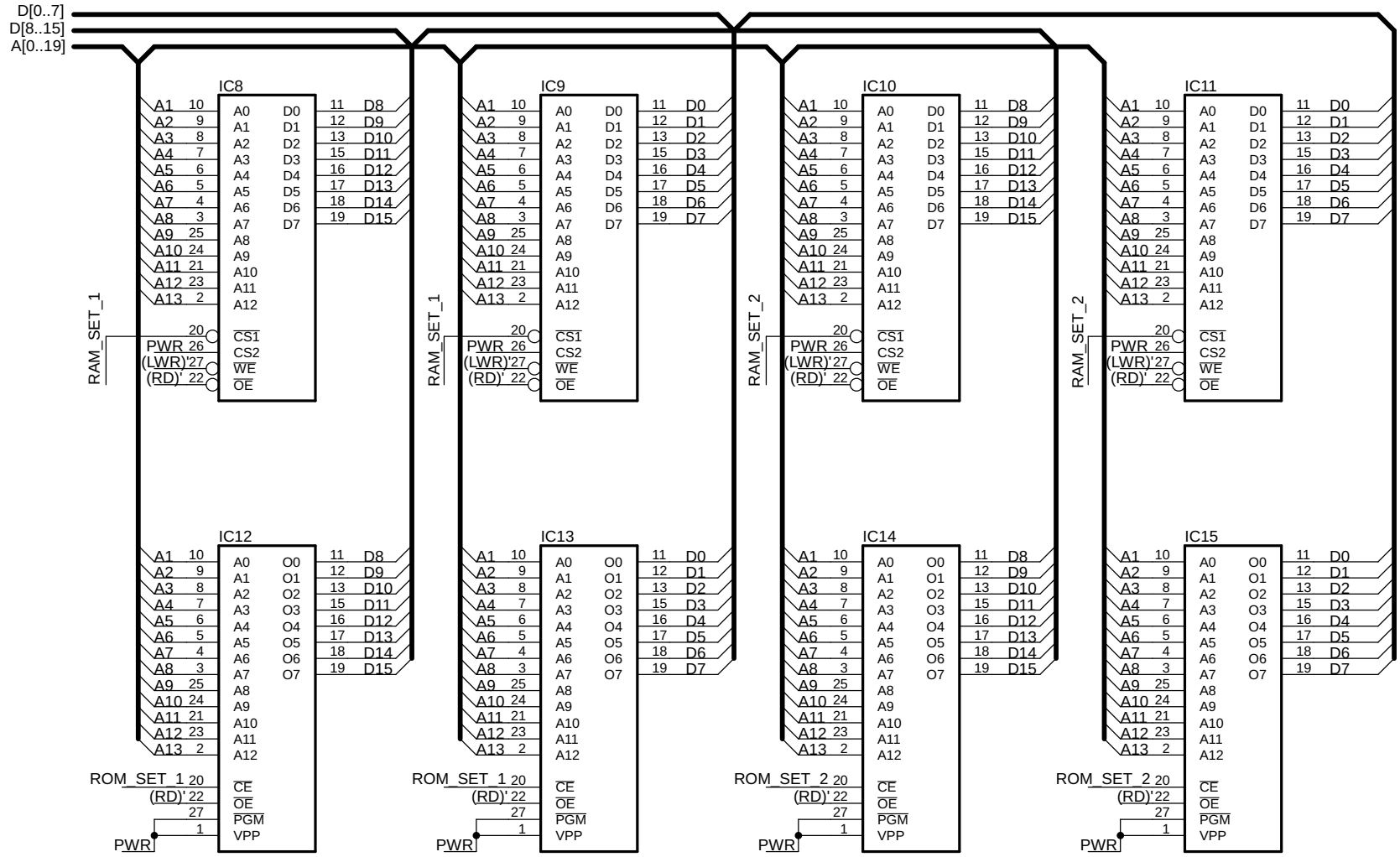
^ Chip Selection (A_{13})

References

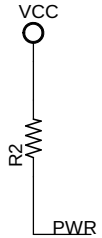
N/A


Clock Generator
Data Bus (to memory & I/O)
Address Bus (to memory & I/O)
IC1
8284-B
Q1
15MHz
GND
RES
CLK
RESET
Reset Circuit
S1
R1
10k
C1
10uF
VCC
AD[0..15]
AD[16..19]
A[0..19]
D[0..15]
IC2
8086
IC3
74LS245N
IC4
74LS245N
IC5
74S373N
IC6
74S373N
IC7
74S373N
8086 with Clock Generator
Address Latch and Data Buffer
Zach Riane I. Machacon
Designer
TITLE: Machacon_LE4-2
Document Number:
CpE 3104 - LE4-2
REV:
1.0
Date: 10/10/2023 5:36 PM
Sheet: 1/3

16K x 16 RAM w/ 4 8K x 8 2063 CMOS SRAM

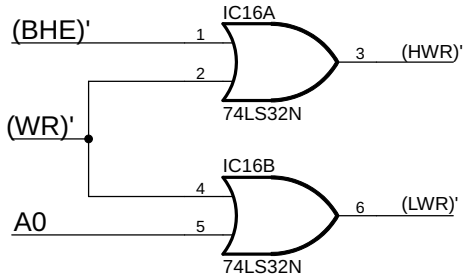


16K x 16 ROM w/ 4 8K x 8 2764 NMOS UV EPROM

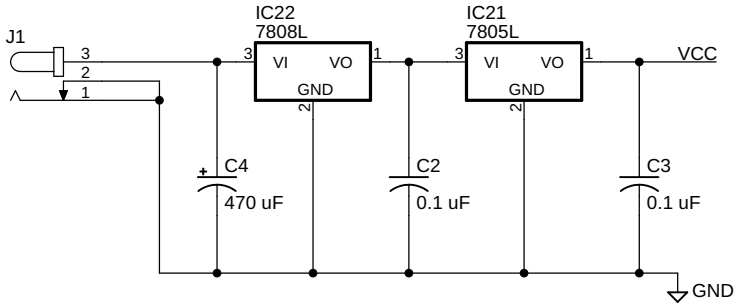


8086 with Clock Generator Address Latch and Data Buffer	Zach Riane I. Machacon Designer	
TITLE: Machacon_LE4-2		
Document Number: CpE 3104 - LE4-2		REV: 1.0
Date: 10/10/2023 5:36 PM	Sheet: 2/3	

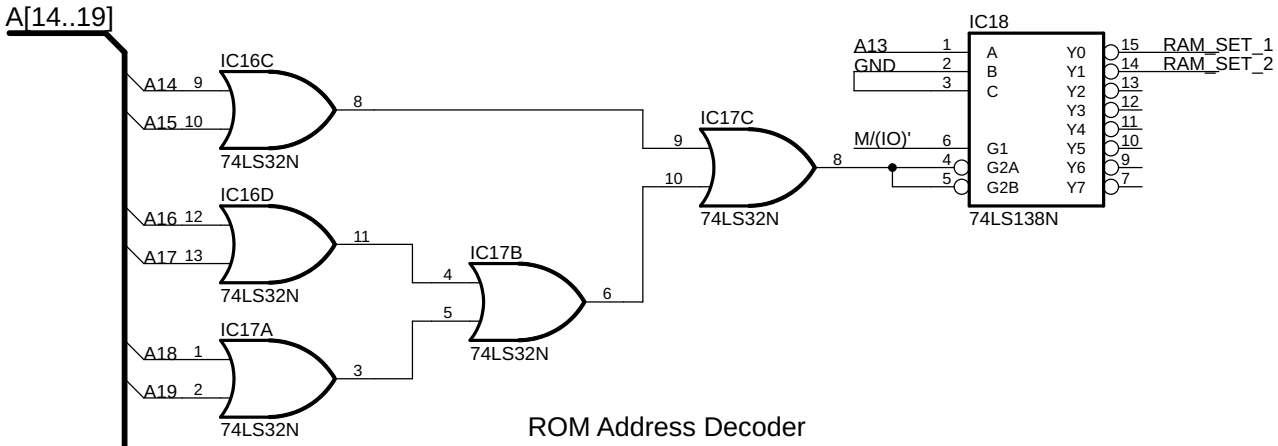
Bank Select Circuit



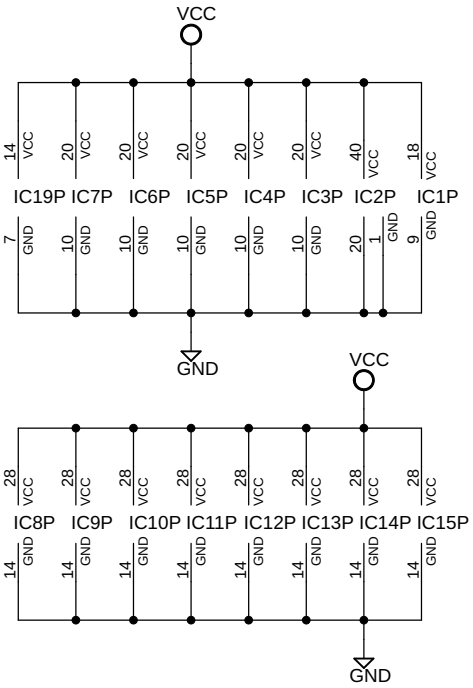
Power Supply with Regulator



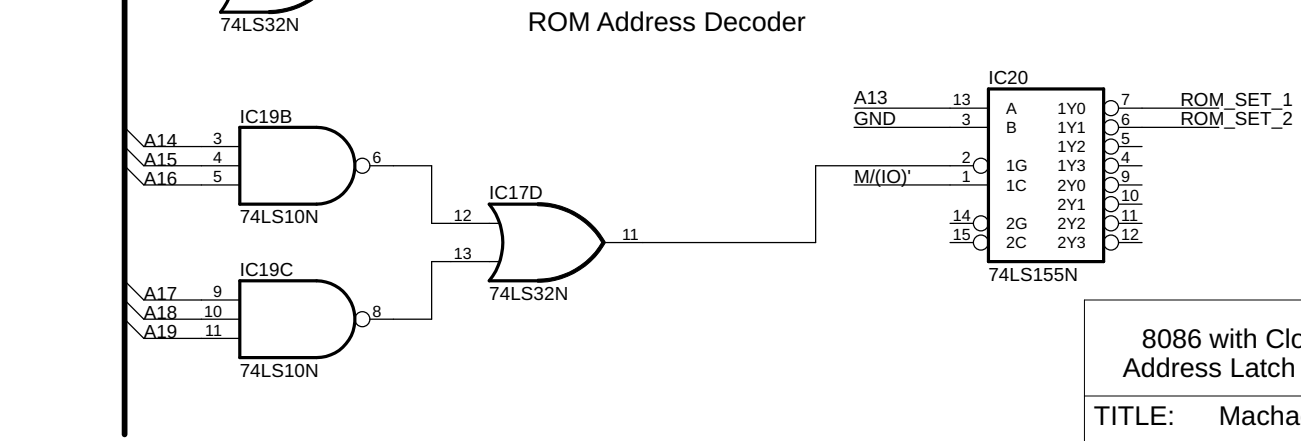
RAM Address Decoder



Gate and IC Supply



ROM Address Decoder



8086 with Clock Generator Address Latch and Data Buffer	Zach Riane I. Machacon Designer
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Document Number: CpE 3104 - LE4-2	REV: 1.0
Date: 10/10/2023 5:36 PM	Sheet: 3/3