

#### LED Driver Control / Keyboard Scan ASIC TM1650

Datasheet from http://www.titanmec.com/index.php/en/product/lists/typeid/59/p/3.html

http://www.titanmec.com/index.php/en/project/download/id/309.html

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### Feature description

The TM1650 is a dedicated LED (Light Emitting Diode Display) drive control circuit with a keyboard scan interface. MCU integrated inside

Input and output control digital interface, data latch, LED driver, keyboard scan, brightness adjustment and other circuits. TM1650 performance is stable and qualitative

Reliable and anti-interference ability, it can be applied to applications with long-term continuous operation for 24 hours.

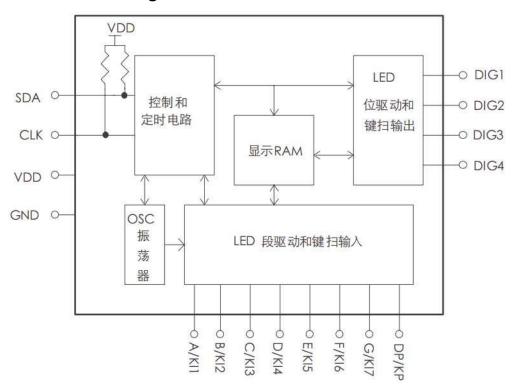
#### **Features**

- $\square$  Two display modes: 8 segments  $\times$  4 bits and 7 segments  $\times$  4 bits
- ☐ Segment drive current is greater than 25mA, bit drive current is greater than 150mA
- ☐ Provide 8 levels of brightness control
- ☐ Keyboard scanning: 7×4bit internal integrated triode driver
- ☐ High-speed two-wire serial interface
- ☐ Built-in clock oscillation circuit
- ☐ Built-in power-on reset circuit
- ☐ Support 2.8V-5.5V power supply voltage
- ☐ Available in DIP16 and SOP16 packages

#### Applicable fields:

Display of household appliances such as set-top boxes, air conditioners, DVD/VCD, etc.

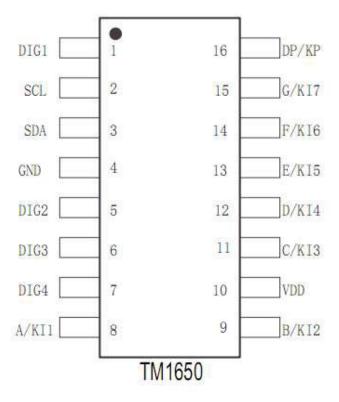
### Internal block diagram



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### Pin information



### Pin function

Port		I/O	Functional description
Name	Name Pin		Functional description
DIG1	1	О	LED Segment Drive Output 1 / Keyboard Scan Output 1
DIG2	5	О	LED Segment Drive Output 2 / Keyboard Scan Output 2
DIG3	6	О	LED Segment Drive Output 3 / Keyboard Scan Output 3
DIG4	7	О	LED segment drive output 4 / keyboard scan output 4
SCL	2	I	clock input
SDA	3	O/I	data input/output
A/KI1	8	O/I	LED segment drive output A/key scan input KI1
B/KI2	9	O/I	LED segment drive output B/key scan input KI2
C/KI3	11	O/I	LED segment drive output C/key scan input KI3
D/KI4	12	O/I	LED segment drive output D/button scan input KI4
E/KI5	13	O/I	LED segment drive output E/key scan input KI5
F/KI6	14	O/I	LED segment drive output F/key scan input KI6
G/KI7	15	O/I	LED segment drive output G/key scan input KI7
DP/KP	16	0	LED segment output DP/keyboard flag output KP
GND	4	ı	Logically
VDD	10	-	Logic Power Supply

In the dry season or dry use environment, it is easy to generate a large amount of static electricity, and electrostatic discharge may damage the integrated circuit. Tianwei Electronics recommends taking one Proper IC prevention and treatment measures, if improper operation and soldering, may cause ESD damage or performance degradation, the chip can not normal work.



#### **Protocol**

The TM1650 communicates using a 2-wire serial transfer protocol.

#### 1: start signal (START) / end signal (STOP)

Start signal: keep SCL at "1" level, SDA jumps from "1" to "0", which is considered to be the start signal. Such as (Figure 3) segment A;

End signal: keep SCL at "1" level, SDA jumps from "0" to "1", which is considered to be the end signal. Such as (Figure 3) segment E;

#### 2: ACK signal

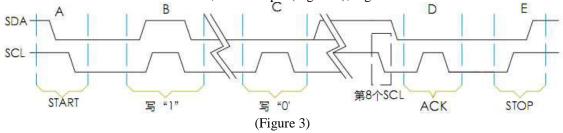
If the communication is normal and the chip is on the 8th clock falling edge of serial communication, the TM1650 actively pulls SDA low. Until check

It is detected that SCL has a rising edge and SDA is released as an input state (for the chip), as in (Figure 3) segment D.

### 3: Write "1" and write "0".

Write "1": keep SDA at "1" level, SCL jumps from "0" to "1", then jumps from "1" to "0", it is considered to be written "1"; For example (Figure 3), segment B.

Write "0": keep SDA at "0" level, SCL jumps from "0" to "1", then jumps from "1" to "0", it is considered to be written "0"; For example (Figure 3), segment C.



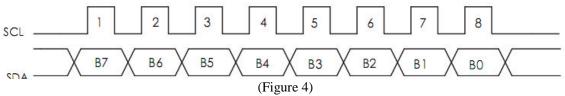
#### 4: One byte data transfer format

The transmission format of one byte of data is shown in Figure 4. When the data is sent, the MSB is in the front and the LSB is in the back. Microprocessor data passes through a two-wire bus

The interface communicates with the TM1650. When SCL is high when inputting data, the signal on SDA must remain unchanged; only on SCL

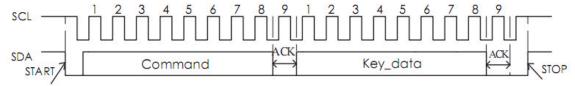
When the clock signal is low, the signal on the SDA can be changed. The start condition of the data input is that SDA is changed from high to high when SCL is high.

Low; the end condition is when SCL is high and SDA changes from low to high.



#### 5: Read button data timing

When reading data, the falling edge of SCL, the data is output from the TM1650 SDA pin.



Command: Send a read button command. Key\_data: The scanned keyboard scan code.



## Keyboard scan code

TM1650 corresponds to the keyboard scan code:

Addressing	DIG4	DIG3	DIG2	DIG1
A/KI1	47H	46H	45H	44H
B/KI2	4FH	4EH	4DH	4CH
C/KI3	57H	56H	55H	54H
D/KI4	5FH	5EH	5DH	5CH
E/KI5	67H	66H	65H	64H
F/KI6	6FH	6EH	6DH	6CH
G/KI7	77H	76H	75H	74H

Note: When reading the button, DIG and KI are connected in series with 2K resistors. Combination keys are not supported.

### **Control commands**

#### 1. data command settings

B7	<b>B6</b>	B5	<b>B4</b>	В3	<b>B2</b>	B1	B0	Description
0	1	0	0	1	0	0	0	Mode command
0	1	0	0	1	×	×	1	Read button data command

Note: The bit of  $\times$  can be 1 or 0, and it is recommended to write 0. Others must be fixed values.

#### 2. display command settings

MSB LSB

<b>B7</b>	<b>B6</b>	B5	<b>B4</b>	В3	<b>B2</b>	<b>B1</b>	<b>B</b> 0	Features	Description
×	0	0	0		×	X			Brightness level 8
×	0	0	1		×	×			Brightness level 1
×	0	1	0		×	×			Brightness level 2
×	0	1	1		×	×		Brightness setting	Brightness level 3
×	1	0	0		×	×		Drightness setting	Brightness level 4
×	1	0	1		×	×			Brightness level 5
×	1	1	0		×	×			Brightness level 6
×	1	1	1		×	×			Brightness level 7
×				0	×	X		7/8 segment display	8-segment display mode
×				1	×	×		control bit	7-segment display mode
×					×	×	0	Turn display bit	Display off
×					×	X	1	on/off	Display on

Note: The bit of  $\times$  can be 1 or 0, and it is recommended to write 0.



## Memory address:

This register stores data transferred from the external device to the TM1650 through the serial interface, a total of 4 byte units, respectively, with the chip

A/KI~DP/KP corresponds to the LED light connected to the DIG pin, and is assigned as shown below: When writing the LED display data, it operates from the high to the low of the data byte from the high to the low of the data address.

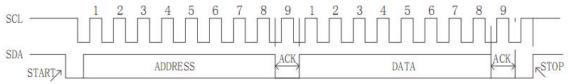
	DP/KP	G/KI7	F/KI6	E/KI5	D/KI4	C/KI3	B/KI2	A/KI1		
	h four)	xHU (hig	ow four) x	xxHL (le	xxHL (low four)					
	B7	В6	B5	B4	В3	B2	B1	В0		
DIG1		BHU	68			HL	68]			
DIG2		MU	6A		6AHL					
DIG3		CHU	60		6CHL					
DIG4		EHU	6E			HL	6E			

#### 1: Memory address command:

LSB MSB **B7 B6 B5 B4 B3 B2 B1 B**0 Memoryaddress 0 0 0 0 0 1 1 1 68H 0 1 1 0 1 0 1 0 6AH 0 1 0 0 0 6CH 0 0 0 1 1 1 6EH

Note: This command is used to set the address of the display register.

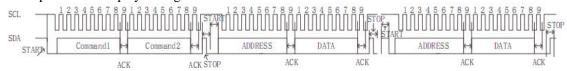
#### 2: Timing of writing data to the memory address:



ADDRESS: Write memory address to TM1650

DATA: Write the data to be displayed to the TM1650.

#### A complete write display timing:



Command1: Data command: 48H.

Command2: On display, showing the brightness level.

ADDRESS: Memory address.

DATA: Display data



### Absolute maximum rating range (1) (2)

	Paramete	Range	Unit	
VDD	logic supply voltage		-0.5 to +7.0	V
VIN	logic input voltage range	SDA, SCL	$-0.5 \sim VDD + 0.5V$	V
Topr	operating temperature rang	ge	-40 to +85	°C
Tstg	storage temperature range		-55 to +125	°C
ESD	Human Body Model (HBM	3000	V	
ESD	Machine mode (MM)		200	V

<sup>(1)</sup> In these levels, the chip may cause permanent damage to the device under long-term use conditions, which may reduce the reliability of the device. Tianwei Electronics does not build Under any other conditions, the chip works beyond these extreme parameters.

## Recommended working conditions

Parameter		Test				
		Conditions	Minimum	Typical	Maximum	unit
		Conditions	value	value	value	
VDD	Supply voltage	-	2.8	5.0	7.0	V
VIH	High Level Input Voltage	-	0.7VDD	-	VDD	V
VIL	Low level input voltage	-	0	-	0.3VDD	V
TA	Operating temperature range	-	-40		+85	°C
TJ	Working junction temperature range	-	-40		+125	°C

### Electrical characteristics

(At VDD=3.0V~5.5V and -40°C~+85°C, (test voltage is VDD=5.0V and TA=+25°C) unless otherwise stated

		Test				
	Parameter	Conditions	Minimum	Typical	Maximum	unit
		Conditions	value	value	value	
VDD	voltage		2.8	5.0	7.0	V
IDD	supply current			0.2	150	mA
ICS	quiescent current	SCL, SDA, KP are high		0.2		mA
VIL	low level input voltage			2.8		V
VIH	high level input voltage			2.8		V
VOH	high level output voltage		VDD-0.4		VDD	V
VOL	low level output voltage			0.3		V
VOLdig	DIG pin low level output	IDIG= -200mA	-		1.3	V
	voltage					
VOLdig	DIG pin low output voltage	IDIG= -100mA			0.9	V
VOHdig	DIG pin high output voltage	IDIG= 5mA	4.5			V
VOLki	KI pin low level output voltage	IKI= -20mA			0.2	V
VOLki	KI pin low level output voltage	IKI= 20mA			0.5	V
IDN1	KI pin input pull-down current	VKI=5.0V	85			mA
VR	Default voltage threshold for power-on reset			2.5		V

<sup>(2)</sup> All voltage values are tested relative to the network.



## Internal timing parameters

(test conditions:  $Ta = 25 \,^{\circ} \text{C}$ , VDD = 5V)

Parameter	symbol	minimum	typical	maximum	Unit
Reset time generated by power-on detection	TPR	10	30	60	ms
Display scan period	TP		7		ms
Keyboard scan interval, button response time	TKS		40		ms

Note: The timing parameters of this watch are multiples of the built-in clock cycle, and the built-in clock frequency decreases as the power supply voltage decreases.`

## Interface timing parameters

(test conditions:  $Ta = 25 \,^{\circ} \text{C}$ , VDD = 5V)

Parameter	symbol	min.	typical	max.	Unit
SDA falling edge start signal setup time	TSSTA	100			ns
SDA falling edge start signal hold time	THSTA	100			ns
SDA rising edge stop signal settling time	TSST0	100			ns
SDA rising edge stop signal hold time	THST0	100			ns
Low level width of the SCL clock signal	TCLOW	100			ns
High level width of the SCL clock signal	TCHIG	100			ns
SDA input data settling time for SCL rising edge	TSDA	40			ns
SDA input data hold time for SCL rising edge	THDA	10			ns
SDA output data is valid for the delay of the falling	TAA	2			ns
edge of SCL					
SDA output data is invalid. Delay on SCL falling edge	TDH	2			ns
Average data transfer rate	Rate			4M	bps

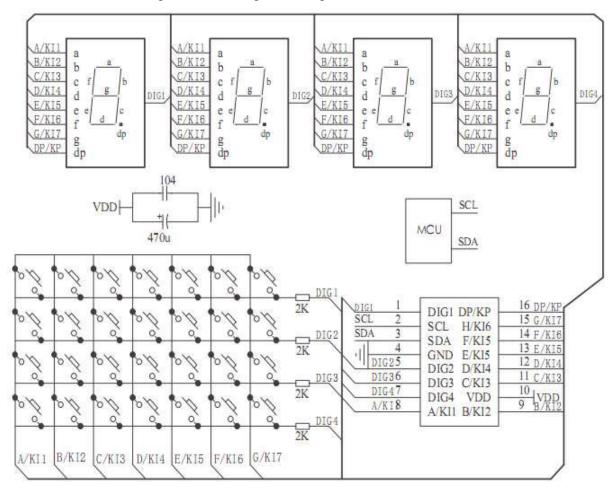
Note: The unit of measurement in this table is 10<sup>-9</sup> in nanoseconds. If the maximum value is not specified, the theoretical value can be infinite.

V1.0



## Typical application circuit

TM1650 driver common digital screen wiring circuit diagram:

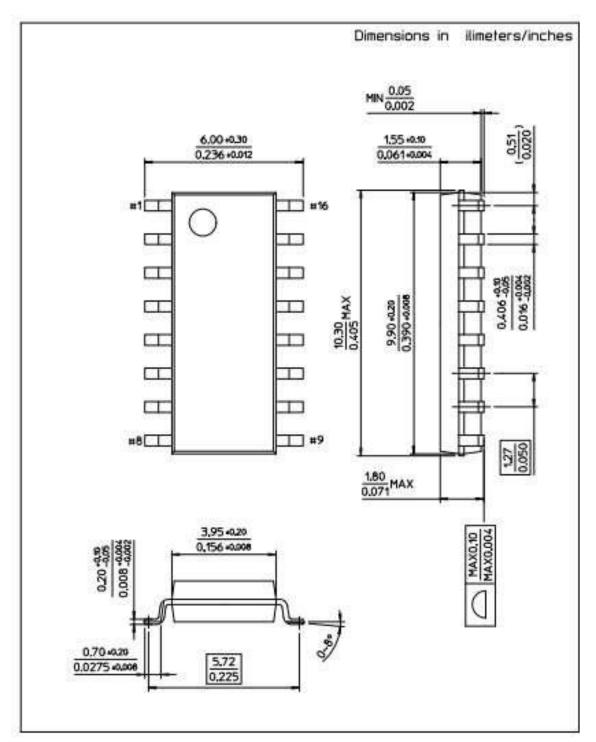


#### Remarks:

- 1) The filter capacitor of the chip should be placed as close as possible to the TM1650 pin during the layout to enhance the filtering effect.
- 2) The chip power and the network of the ground should be as wide as possible when the line is at the line.
- 3) Since the turn-on voltage drop of the Blu-ray digital tube is about 3.0V, the TM1650 power supply should be 5.0V.

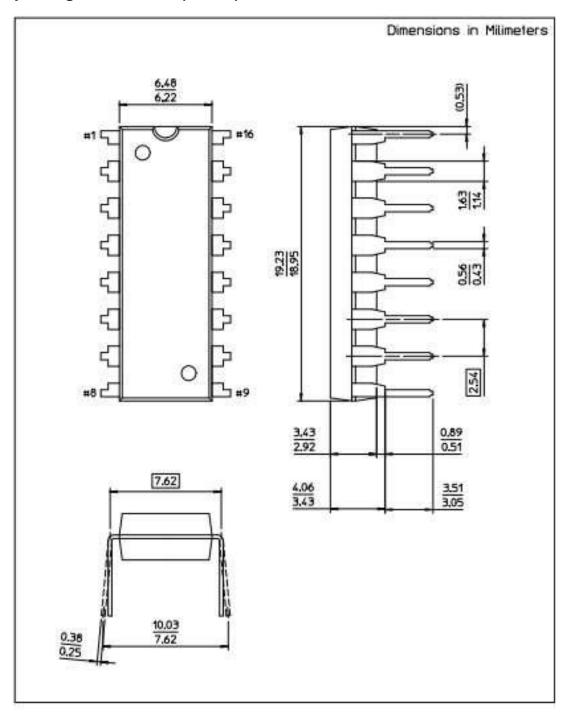


# IC package schematic (SOP16):





## IC package schematic (DIP16):



All specs and applications shown above subject to change without prior notice. (The above circuits and specifications are for reference only, if the company makes amendments without prior notice)