

# **BK3211**

# **Specifications**

Beken Internal Data — Signed NDA Required for Distribution

Single Chip for Bluetooth

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 $Disclaimer: Descriptions\ of\ specific\ implementation\ are\ for\ illustrative\ purpose\ only,\ actual\ hardware\ implementation\ may\ differ.$ 



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## 1. General Description

The BK3211 chip is a highly integrated singlechip Bluetooth device. It integrates the highperformance transceiver and rich features baseband processor, which is compliant with Bluetooth 2.1 + EDR specification.

The BK3211 is available in 32-pin 4x4 mm QFN packages.

#### 1.1. Features

#### 1.1.1. Radio Features

- On-chip TX/RX switch
- Polar modulation transmitter architecture with very low power consumption and high TX performance
- Near-Zero IF receiver architecture with -91dBm sensitivity
- Support for class 1, class 2 and class 3 transmitting power requirement
- Fully integrated synthesizer without external loop filter component

#### 1.1.2. Baseband Features

- Fully compliant with Bluetooth 2.1 + EDR specification
- Support Bluetooth Piconet and Scatternet
- Support up to 3Mbps high speed UART interface
- Support Sniff mode, hold mode and park mode
- Support A-law, μ-law and CVSD digitize audio CODEC in PCM interface
- Provide I2C interface

#### 1.1.3. Device Features

- Enhanced support for WLAN/BT Coexistence
- Standby and sleep modes to minimize power consumption
- Support share handset system reference clock

### 1.2. Applications

- Mobile handset
- MP3, MP4 player and PMP
- Other portable devices



## 2. Pin Definition

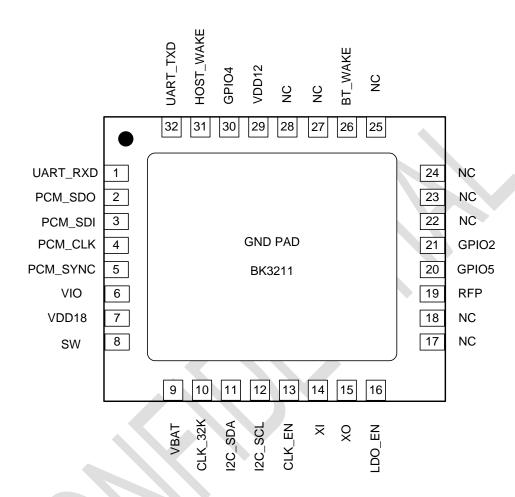


Figure 1 BK3211 PIN Definition Diagram

**Table 1 Pin Definition** 

Package Pin#	Name	Description
1	UART_RXD	UART RX data input
2	PCM_SDO	PCM data output
3	PCM_SDI	PCM data input
4	PCM_CLK	PCM data clock
5	PCM_SYNC	PCM data sync
6	VIO	IO power supply
7	VDD18	1.8V voltage output, connected with 1uF decoupling cap.
8	SW	Internal buck regulator output
9	VBAT	VBAT LDO input, connected with 1uF decoupling cap.
10	CLK_32K	32.768 kHz clock input



## BK3211 Datasheet

v 1.2

11	I2C_SCL	I2C Clock signal
12	I2C_SDA	I2C Data signal
13	CLK_EN	Request source clock active
14	XI	Crystal input or oscillator input.
15	XO	Crystal output.
16	LDO_EN	System power on/off control
17	NC	Not connect
18	NC	Not connect
19	RFP	RF input and output
20	GPIO5	General purpose input/output
21	GPIO2	General purpose input/output or Bluetooth Priority signal
22	NC	Not connect
23	NC	Not connect
24	NC	Not connect
25	NC	Not connect
26	BT_WAKE	To wakeup BT. Input from host.
27	NC	Not connect
28	NC	Not connect
29	VDDD12	Power supply for digital
30	GPIO4	General purpose input/output or WLAN Active signal
31	HOST_WAKE	To wakeup host. Output to host.
32	UART_TXD	UART TX data output



## 3. Functional Description

## 3.1. Block Diagram

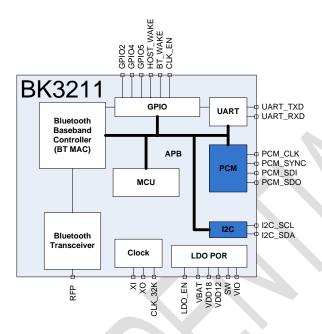


Figure 2 BK3211 Block Diagram

As shown in the **Figure 2**, the BK3211 integrates the Bluetooth transceiver, Bluetooth baseband controller and MCU etc. The Bluetooth transceiver integrates the low-IF single conversion RX and Polar loop modulation TX. The Bluetooth baseband controller carries out the baseband protocols and other low-level link routines such as modulation/demodulation, packets processing, bit stream processing, frequency hopping and so on.



### 4. Electrical Characteristics

## 4.1. Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings

Parameter	Description	MIN	TYP	MAX	Unit
VBAT	Battery Regulator Supply Voltage			4.8	V
$P_{RX}$	RX Input Power	-	10	-	dBm
T <sub>STR</sub> Storage Temperature Range		-40	-	150	$^{\circ}\!\mathbb{C}$
Vcc	Input Voltage	-0.3	-	3.6	V

## 4.2. Recommended Operating Conditions

Table 3 Recommended Operating Conditions

Parameter	Description	MIN	TYP	MAX	Unit
VBAT	Battery Regulator Supply Voltage	3.3	4	4.2	V
$T_{OPR}$	Operation Temperature Range	-20	-	60	$^{\circ}\!\mathbb{C}$
$V_{\mathrm{IL}}$	CMOS Low Level Input Voltage	0	-	0.3*VIO	V
$V_{\mathrm{IH}}$	CMOS High Level Input Voltage	0.7*VIO	-	VIO	V
$V_{TH}$	CMOS Threshold Voltage		0.5*VIO		V

Notes:

1. VIO=1.8~3.3V

## 4.3. Typical Power Consumption

**Table 4 Typical Power Consumption** 

State	Description	MIN	TYP	MAX	Unit
Shut Down			8		uA
Sleep			600		uA
Only HCI Active			5		mA
DH1/DM1			42		mA
DH3/DM3			46		mA
DH5/DM5			47		mA

### 4.4. RX AC Characteristics

#### 4.4.1. Basic Data Rate mode RX AC Characteristics

Table 5 Basic Data Rate mode RX AC Characteristics

(VBAT = 3.6 V,  $T_{OPR} = 27 \, \text{C}$ , unless otherwise specified)

Parameter	Condition	MIN	TYP	MAX	Unit
Input Frequency	2402~2480	2402	-	2480	MHz
RXSENS	BER=0.001	-	-89	-	dBm



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Bluetooth

Maximum Received Signal	BER=0.001	0	-	-	dBm
C/ICO		-	10	-	dB
C/IIST	F = F0 + 1MHz	-	0	-	dB
	F = F0 - 1MHz	-	0	-	dB
C/I2ND	F = F0 + 2MHz	-	-15	-	dB
	F = F0 - 2MHz		-24	-	dB
C/I3RD	F = F0 + 3MHz	-	-30	-	dB
CISKD	F = F0 - 3MHz	-	-40	-	dB
C/I Image Channel	F = Fimage	-	-15	1	dB
	30MHz-2000MHz	-10	-	-	dBm
Out-of-Band Blocking	2000MHz-2400MHz	-27	-	-	dBm
Performance	2500MHz-3000MHz	-27	-	-	dBm
	3000MHz-12.5GHz	-10	-	-	dBm
Intermodulation		-	-37	_	dBm

#### 4.4.2. Enhanced Data Rate mode RX AC Characteristics

### Table 6 Enhanced Data Rate mode RX AC Characteristics

 $(VBAT = 3.6 \text{ V}, T_{OPR} = 27 \text{ C}, \text{ unless otherwise specified})$ 

Parameter	Condition	MIN	TYP	MAX	Unit
π/4 DQPSK					
RXSENS	BER=0.0001	-	-91	-	dBm
BER Floor	BER=0.00001	-	-85	-	dBm
Maximum Received Signal	BER=0.001	0	-	-	dBm
C/ICO		-	11	-	dB
C/I1ST	F = F0 + 1MHz	-	-11	-	dB
CHSI	F = F0 - 1MHz	-	-11	-	dB
C/I2ND	F = F0 + 2MHz	-	-15	-	dB
C/12ND	F = F0 - 2MHz	-	-27	-	dB
C/IODD	F = F0 + 3MHz	-	-32	-	dB
C/I3RD	F = F0 - 3MHz	-	-40	-	dB
C/I Image Channel	$F = F_{image}$	-	0	-	dB
8DPSK					
RXSENS	BER=0.0001	-	-83	-	dBm
BER Floor	BER=0.00001	-	-78	-	dBm
Maximum Received Signal	BER=0.001	0	-	-	dBm
C/ICO		-	20	-	dB
C/I1ST	F = F0 + 1MHz	-	-5	-	dB
CHSI	F = F0 - 1MHz	-	-5	-	dB
C/I2ND	F = F0 + 2MHz	-	-10	-	dB
C/12ND	F = F0 - 2MHz	-	-22	-	dB
C/I2DD	F = F0 + 3MHz	-	-30	-	dB
C/I3RD	F = F0 - 3MHz	-	-30	-	dB
C/I Image Channel	$F = F_{image}$	-	4	-	dB



### 4.5. TX AC Characteristics

#### 4.5.1. Basic Data Rate mode TX AC Characteristics

#### Table 7 Basic Data Rate mode TX AC Characteristics

(VBAT = 3.6 V,  $T_{OPR} = 27 \, \text{C}$ , unless otherwise specified)

Parameter	Condition	MIN	TYP	MAX	Unit
Maximum RF Transmit Power		-	8	9	dBm
RF Power Control Range		-	15	-	dB
20dB Band Width		-	0.9	-	MHz
ACP1ST	F = F0 + 1MHz	-	-	-	dBm
ACPIST	F = F0 - 1MHz	-		-	dBm
A CDAND	F = F0 + 2MHz	-	-30	-	dBm
ACP2ND	F = F0 - 2MHz	-	-30	-	dBm
A CID 2DD	$F = F0 + \ge 3MHz$	-	-40	-	dBm
ACP≥3RD	$F = F0 - \ge 3MHz$	-	-40	-	dBm
	30MHz to 1GHz, Operating Mode	-	-36	-	dBm
Out-of-Band Spurious	1GHz to 12.75GHz, Operating Mode	-	-30	-	dBm
Emission	1.8GHz to 1.9GHz, 5.15GHz to 5.3GHz	-	-47	-	dBm
Δflavg Maximum Modulation		1	160	1	KHz
Δf2max Minimum Modulation		ı	120	ı	KHz
∆f2avg/∆f1avg		-	0.9	-	-
Initial Carrier Frequency Tolerance		-	5	-	KHz
Drift Rate		-	7	-	KHz/50us
Drift (1 slot packet)		-	8	-	KHz
Drift (3 slot packet)		-	8	-	KHz
Drift (5 slot packet)		-	10	-	KHz

#### 4.5.2. Enhanced Data Rate mode TX AC Characteristics

#### Table 8 Enhanced Data Rate mode TX AC Characteristics

(VBAT = 3.6 V,  $T_{OPR} = 27 \, \text{C}$ , unless otherwise specified)

Parameter	Condition	MIN	TYP	MAX	Unit
Maximum RF Transmit Power		-	4	6	dBm
Relative Transmit Power		-	-4	-	dB
$\pi/4$ DQPSK Max Carrier Frequency Stability $w_0$		-	2	-	kHz
π/4 DQPSK Max Carrier Frequency Stability w <sub>i</sub>		-	3	-	kHz
$\pi/4$ DQPSK Max Carrier Frequency Stability $ w_i+w_0 $		-	1.5	-	kHz



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Bluetooth

8DPSK Max Carrier Frequency Stability w <sub>0</sub>		-	2	-	kHz
8DPSK Max Carrier Frequency Stability w <sub>i</sub>		-	3	-	kHz
8DPSK Max Carrier Frequency Stability  w <sub>i</sub> + w <sub>0</sub>		-	1.5	-	kHz
π/4 DQPSK Modulation Accuracy	RMS DEVM	-	7	-	%
	99% DEVM	-	-	20	%
	Peak DEVM	-	15	-	%
8DPSK Modulation Accuracy	RMS DEVM	-	9	-	%
	99% DEVM	-	-	20	%
	Peak DEVM	-	17	-	%
ACP1ST	F = F0 + 1MHz	-	-14	-	dBm
	F = F0 - 1MHz	-	-13	-	dBm
ACP2ND	F = F0 + 2MHz	-	-20	-	dBm
	F = F0 - 2MHz	-	-20		dBm
ACP>3RD	$F = F0 + \ge 3MHz$	-	-40	-	dBm
ACr≥3ND	$F = F0 - \ge 3MHz$	-	-40	-	dBm
EDR Differential Phase Coding		-	100	-	%



## 5. Application Schematic

The compatible design for BK3211 and BK3511, which inside the square brackets are BK3511 Pin names or component values  $\frac{1}{2}$ 

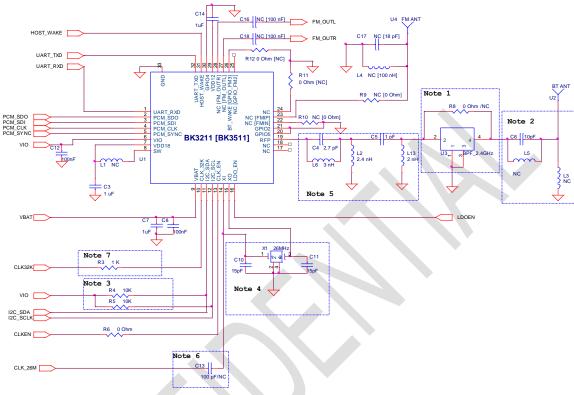


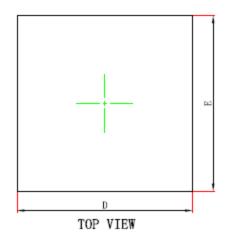
Figure 3 BK3211 Application Diagram

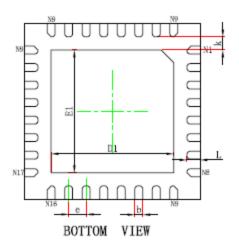
The detail schematic design please refers to the hardware design reference.



## 6. Package Information

QFNWB4×4-32L-A (PO. 40TO. 75/O. 85) PACKAGE OUTLINE DIMENSIONS





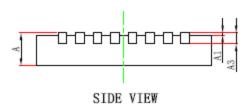


Figure 4 QFN 4x4 32 Pin Package diagram

Table 9 QFN 4x4 32 Pin Package dimensions

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
Α	0.700/0.800	0.800/0.900	0.028/0.031	0.031/0.035
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008REF.	
D	3.924	4.076	0.154	0.160
E	3.924	4.076	0.154	0.160
D1	2.700	2.900	0.106	0.114
E1	2.700	2.900	0.106	0.114
k	0.200MIN.		0.008MIN.	
b	0.150	0.250	0.006	0.010
е	0.400TYP.		0.016	STYP.
L	0.224	0.376	0.009	0.015



## 7. Solder Reflow Profile

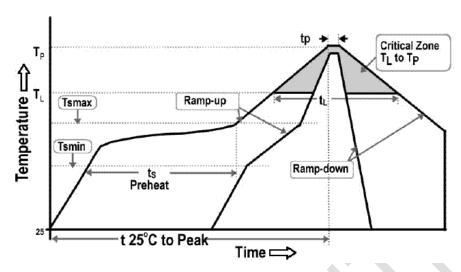


Figure 5 Classification Reflow Profile

Table 10 Solder Reflow Profile

Profile Feature		Specification
Average Ramp-Up Ra	te (tsmax to tp)	3 ℃/second max.
	Temperature Min (Tsmin)	150 ℃
Pre_heat	Temperature Max (Tsmax)	200 ℃
	Time (ts)	60-180 seconds
Time Maintained	Temperature (TL)	217 ℃
above	Time (tL)	60-150 seconds
Peak/Classification Te	emperature (Tp)	260 ℃
Time within 5 °C of A	ctual PeakTemperature (tp)	20-40 seconds
Ramp-Down Rate 6		6 ℃/second max.
Time 25 °C to Peak Te	emperature 8	8 minutes max.

## 7.1. RoHS Compliant

The product does not contain lead, mercury, cadmium, hexavalent chromium, PBB&PBDE content in accordance with directive 2002/95/EC(RoHS).

## 7.2. ESD Sensitivity

Integrated circuits are ESD sensitive and can be damaged by static electricity. Proper ESD techniques should be used when handling these devices.



# **Revision History**

Rev.	Date	Author(s)	Remark
1.0	5/7/2012	YMHUANG	Initial release
1.1	05/24/2012	LFBAO	Updated application schematic; updated electrical characteristics, Specially change the serial resistance from 0 to 1K at 32.768K clock path
1.2	06/19/2012	YMHUANG	Updated application schematic to improve the GSM suppression