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Model Name: ELZE1

File Name: LA-G611P

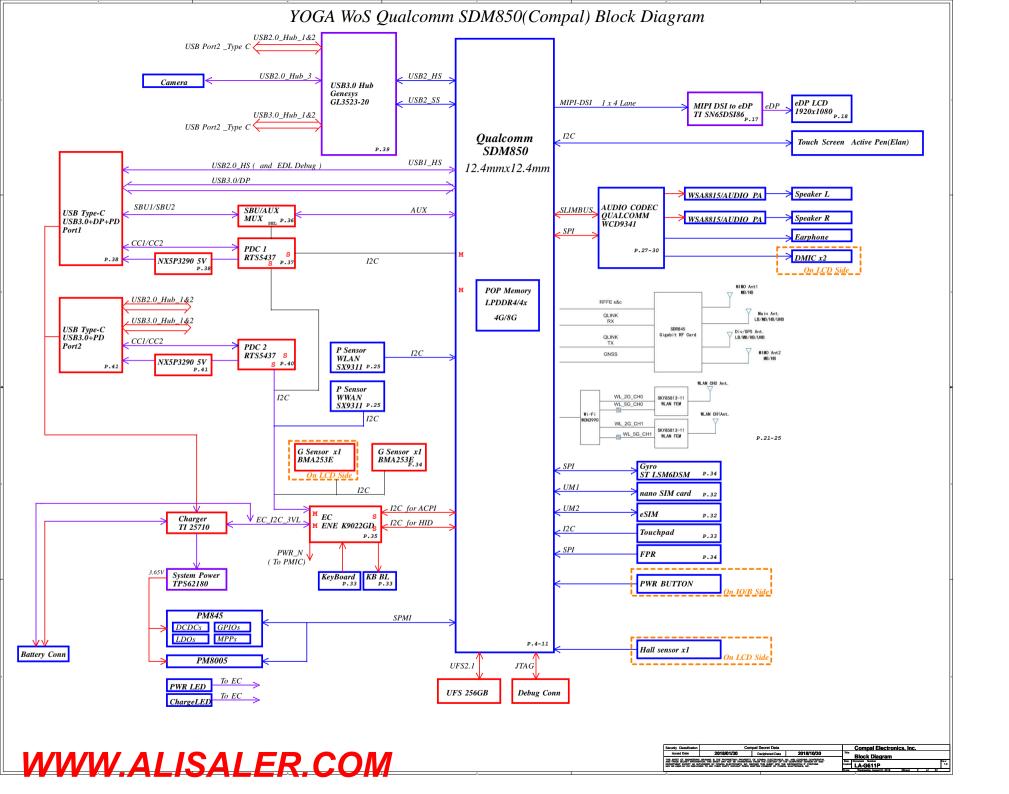
# **Compal Confidential**

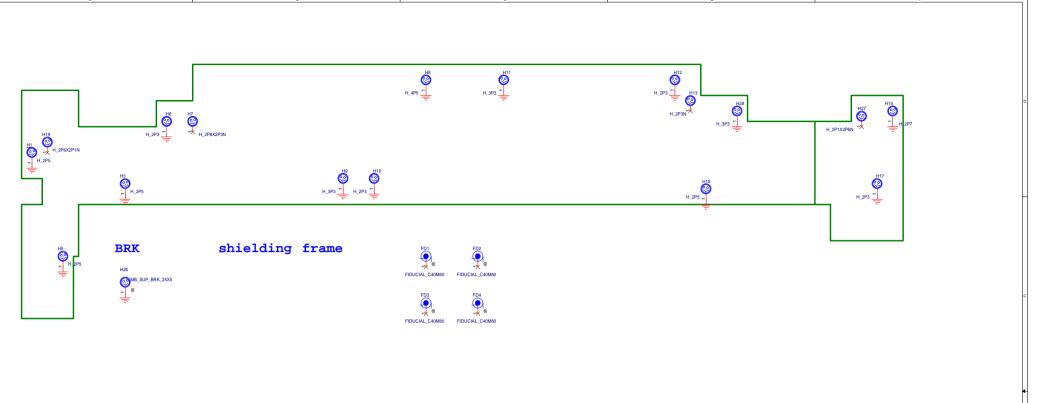
WOS M/B Schematics Document

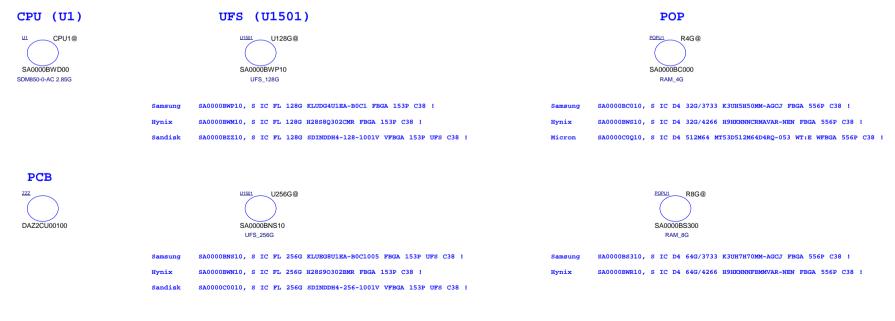
Qualcomm SDM850 with LPDDR4

Rev. 1.0

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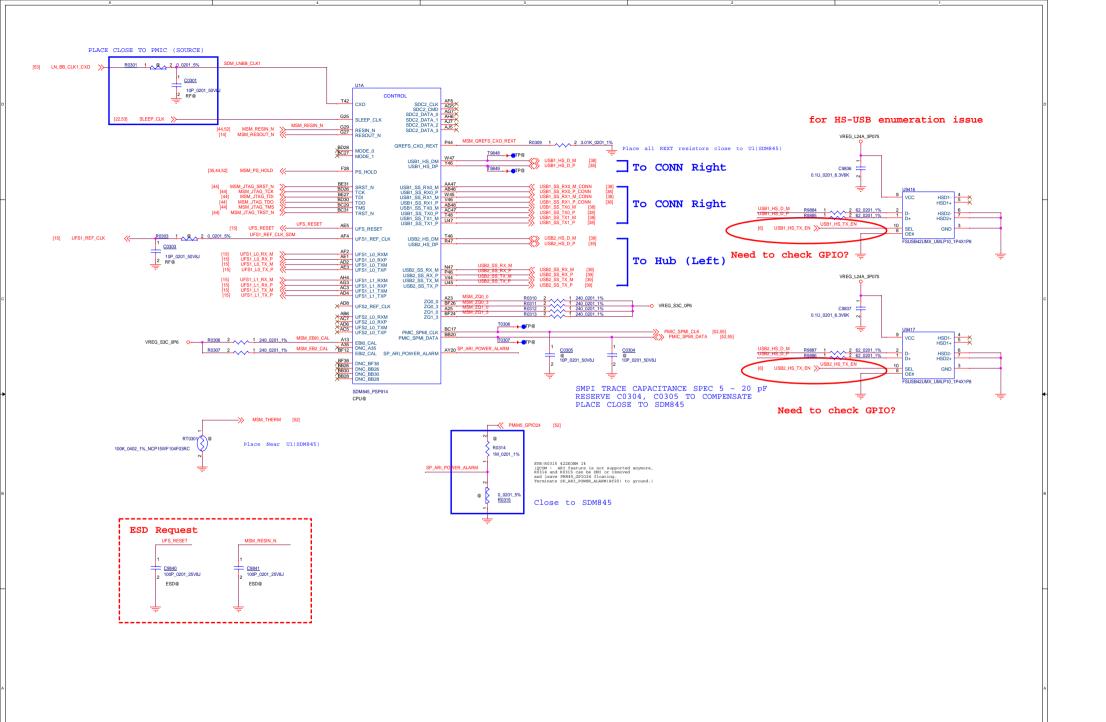
Security Classification

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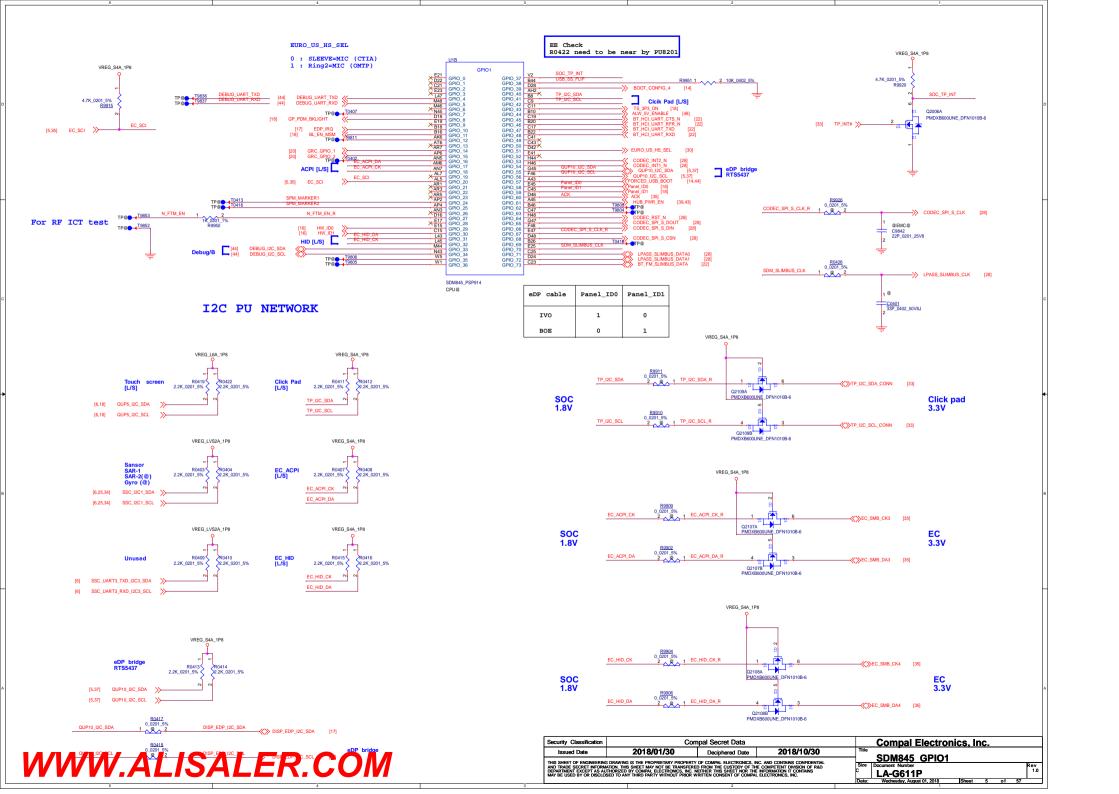
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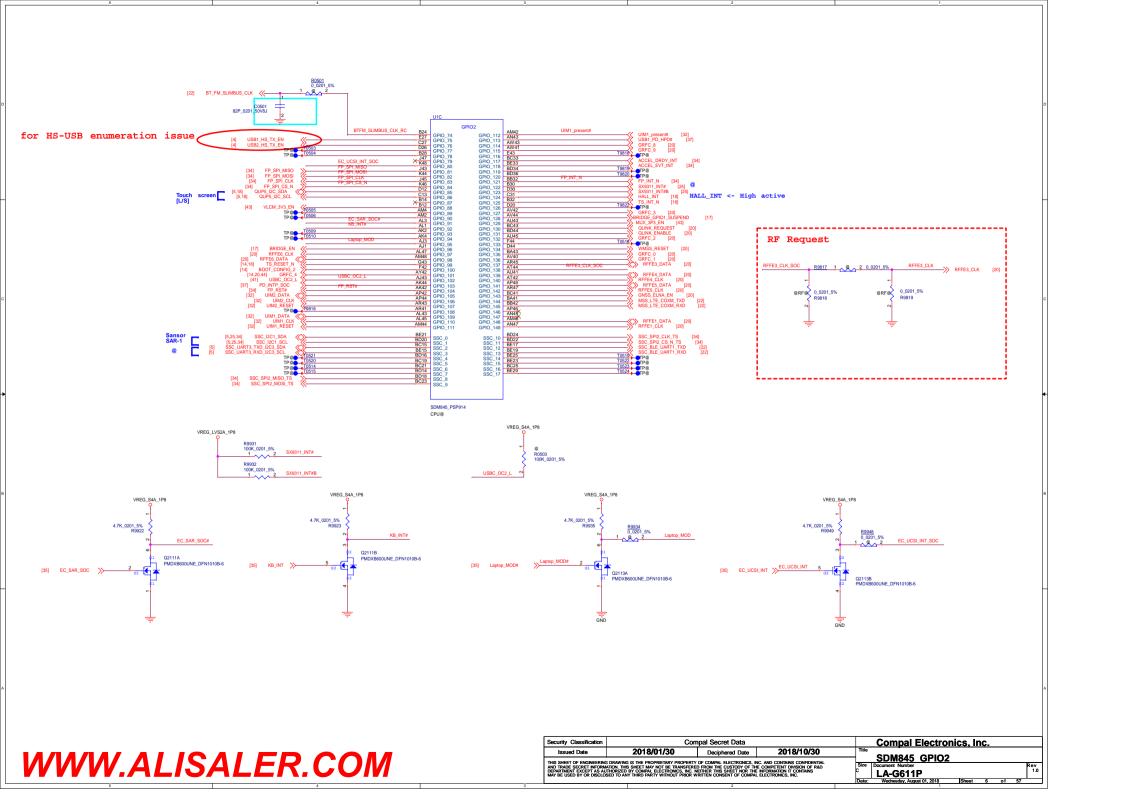
Compal Electronics, Inc.

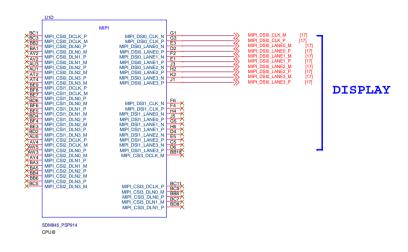
Notes List Document Number LA-G611P

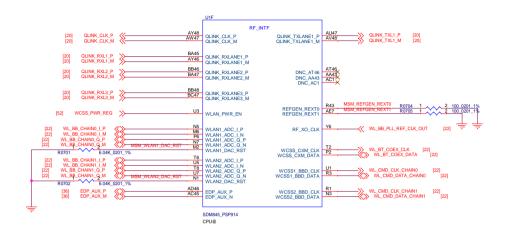


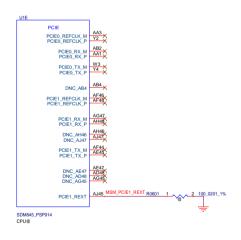
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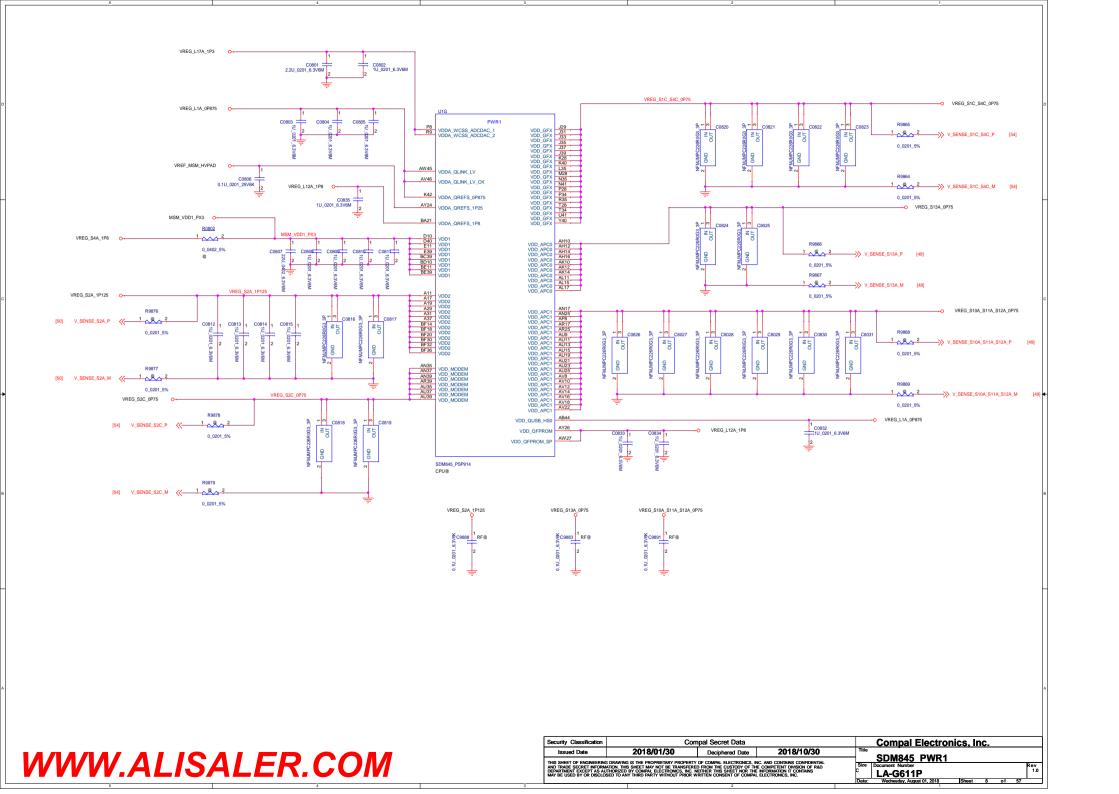


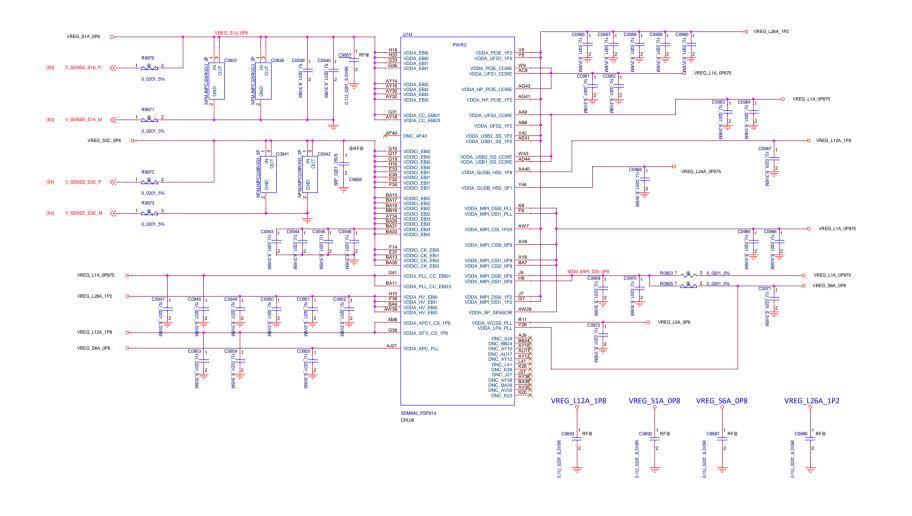




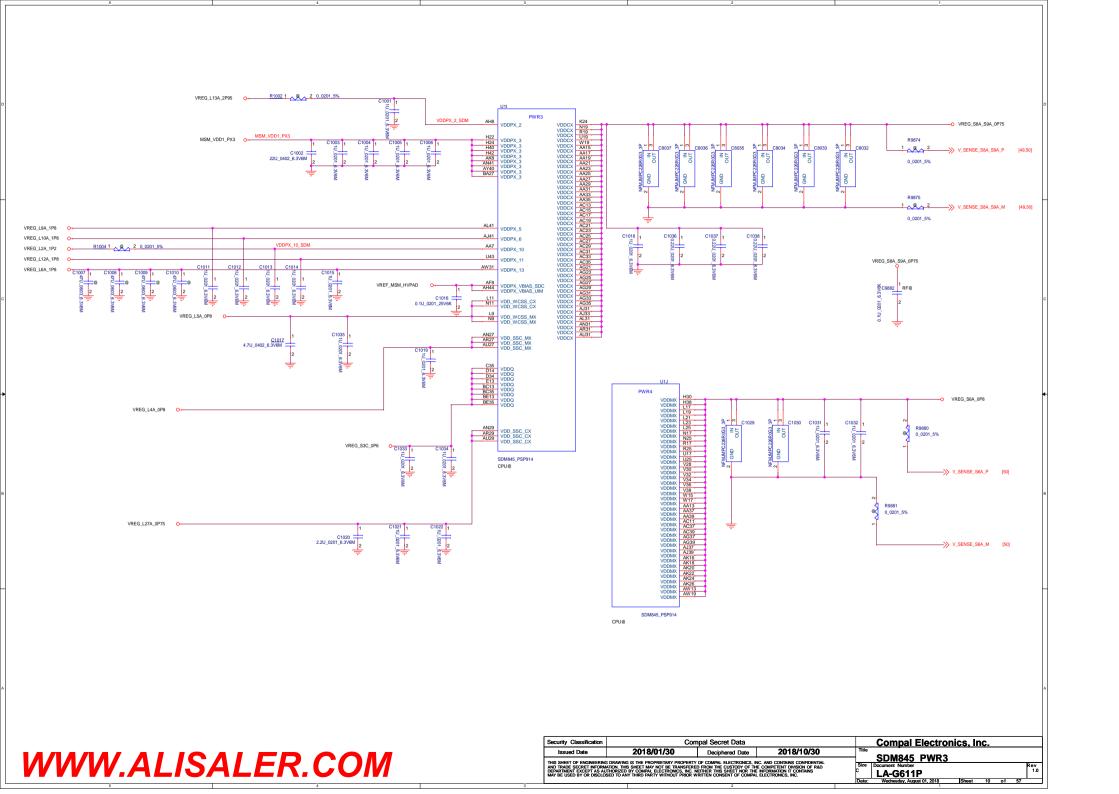


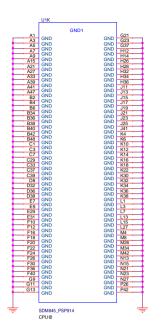
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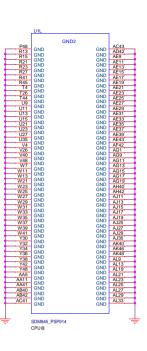


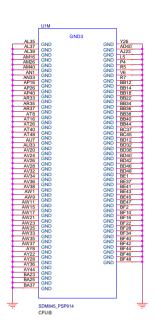


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#### SoC\_I2C

Channel	Dev.	Address	Level
GPIO_17/18	EC_ACPI	0 <b>x</b> 60	3.3(L/S)
GPIO_31/32	EC_HID		3.3(L/S)
GPIO_41/42	Click pad	0X2C (Synaptics) 0X15 (ELAN)	3.3(L/S)
GPIO_85/86	Touch screen	0x10	3.3(L/S)
SSC_0/1	Sar-1_Wlan	0 <b>x</b> 28	1.8
GPIO 53/54	eDP Bridge	0 <b>x</b> 2C	1.8
GF10_53/54	PDC1_5437	0xBC	3.3(L/S)

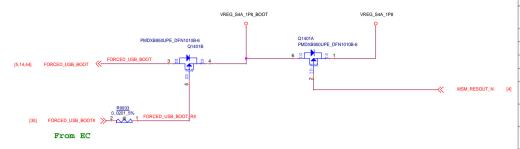
#### EC\_I2C

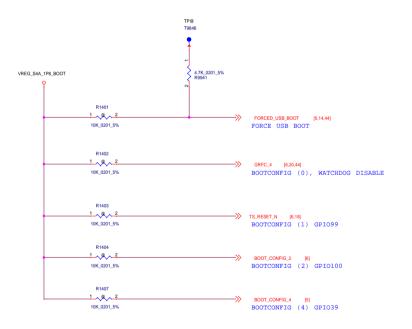
Channel	Dev.	Address	Level
	PDC1_5437	0xBC	3.3
	PDC2_5437	0xBE	3.3
EC_SMB_2	G-Sensor(MB)	0011000b(0x18)	3.3
	G-Sensor(Panel)	0011001b(0x19)	3.3
	Sar-2_LTE	0x28	3.3

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Boot	Pin	Do	not	use	for	PU.	/PI

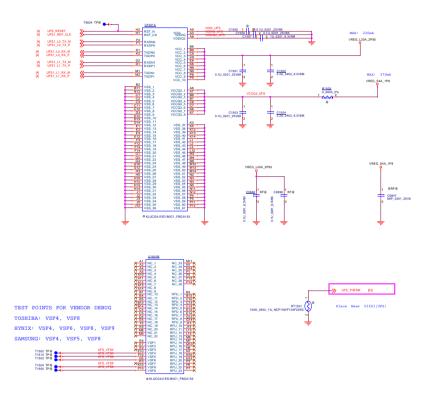
Boot configuration #	GPIO#	Function	Bit values			
BOOT_CONFIG_0 GPIO_101 WDOG disable		WDOG disable	1 – Disables WDOG 0 – Enables WDOG			
BOOT_CONFIG_1	BOOT_CONFIG_1 GPIO_99 Fast boot bit 0		Selects external boot device.			
BOOT_CONFIG_2	GPIO_100	Fast boot bit 1				
BOOT_CONFIG_3	GPIO_133	Fast boot bit 2				
BOOT_CONFIG_4	GPIO_39	Fast boot bit 3				
BOOT_CONFIG_10	GPIO_148	Use serial number	Serial number is not used for authentication.     All segments of serial number used for authentication.			
BOOT_CONFIG_11	GPIO_146	MSA PK hash in fuse	0 – Hash of MSA root is in the apps boot ROM. 1 – Hash of MSA root is in the OEM PK hash.			
BOOT_CONFIG_12	GPIO_141	MSA authentication enable	O – Disables MSA authentication.     1 – Enables MSA authentication.			
BOOT_CONFIG_13	GPIO_136	Apps PK hash in fuse	0 – Hash of apps root is in the apps boot ROM. 1 – Hash of apps root is in the OEM PK hash.			
BOOT_CONFIG_14	GPIO_132	Apps authentication enable	Disables apps authentication.     Enables apps authentication.			
BOOT_CONFIG_15	OOT_CONFIG_15 GPIO_116 Force MSA authentication enable		O – Disables force MSA authentication.     Enables force MSA authentication.			
FORCE_USB_BOOT GPIO_57 Force USB download		Force USB download	d 0 – Releases USB download mode. 1 – Enables USB download mode.			

			GF	PIO		
	FAST_BOOT	39	133	100	99	Boot device/comments
Default	0000	0	0	0	0	UFS (1) Then SD card on SDC2 (2) Then SS/HS/FS USB on USB 3.1 (3)
	0001	0	0	0	1	SD card on SDC2 (1)  Then UFS (2)  Then SS/HS/FS USB on USB 3.1 (3)
	0010	0	0	1	0	SD card on SDC2 (1) Then SS/HS/FS USB on USB 3.1 (2)
	0011	0	0	1	1	SS/HS/FS USB on USB 3.1 (1)
	0100	0	1	0	0	Quad SPI (1) Then SS/HS/FS USB on USB 3.1 (2)
	0101	0	1	0	1	Single SPI (1) Then SS/HS/FS USB on USB 3.1 (2)

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#### UFS MEMORY (SR)



#### [Table 7] Power mode and MIPI UniPro and M-PHY power state

UFS power mode	UniPro Power Mode	M-PHY Power Mode	VCC Power	Description
ACTIVE	FAST_STATE	HS-BURST	On	(3)
IDLE	SLEEP_STATE	STALL	On	(6)
IDLE21)	HIBERNATE_STATE	Hibem8	On	See the Chapter 2.4.1
SLEEP	HIBERNATE_STATE	Hibern8	Off	(2)
POWER DOWN	OFF_STATE	UNPOWERED	Off	(4)

NOTE:

1) Samsung specific power mode for saving the IDLE power. Host shall issue 'enter hilbern8' for this power mode.

#### [Table 3] Supply voltage for operating

Parameter	Symbol	Min	Тур.	Max	Unit
Supply Voltage	VCC	2.7	3.3	3.6	V
Supply Voltage	VCCQ2	1.7	1.8	1.95	V

#### [Table 17] Power Consumption

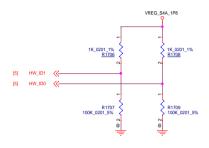
			HS Gear3	x 1Lane	HS Gear3	x 2Lane	
Power	Density	NAND Type	VCCQ2(1.8V)	VCC(3.3V)	VCCQ2(1.8V)	VCC(3.3V)	Unit
Active			320	230	370	230	mA
IDLE2	64 GB	128Gb MLC x 4	450	70	450	70	uA
Sleep			450	01)	450	01)	uА

#### ITable 21 153 FBGA Ball Information

Name	Type	Description
VCC	Supply	Supply voltage for the memory devices
VCCQ2	Supply	Supply voltage used typically for the PHY interface and the memory controller and any other internal low voltage block
VDDiQ	Input	Input terminal to provided bypass capacitor for VCCQ internal regulator typically related to the memory controller
VDDiQ2	Input	Input terminal to provide bypass capacitor for VCCQ2 internal regulator, typically related to memory IF
VDDi	Input	Input terminal to provide bypass capacitor for VCC internal regulator
VSS	Supply	Ground
RST_n	Input	Input hardware reset signal. This is an active low signal
REF_CLK	Input	Input reference clock. When not active, this signal shall be pull-down or driven low by the host SoC.
RXDP0 / RXDP1		
RXDN0 / RXDN1	Input	Downstream data lane(1st and 2nd lane) : differential input signals into UFS device from the host
TXDP0 / TXDP1		
TXDN0 / TXDN1	Output	Upstream data lane(1st and 2nd lane) : differential output signals from the UFS device to the host
NC		Not Connected. NC pins can be connected to ground or left floating
RFU	-	Reserved for Future Use. RFU pins must be left floating.
VSFn	5	Vendor Specific Function. VSFn(n=1-9) pins must be left floating. Each vendor is able to use these pins during manufacturing

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Date: Wednesday, August 01, 2018 Sheet 15 of 57	_

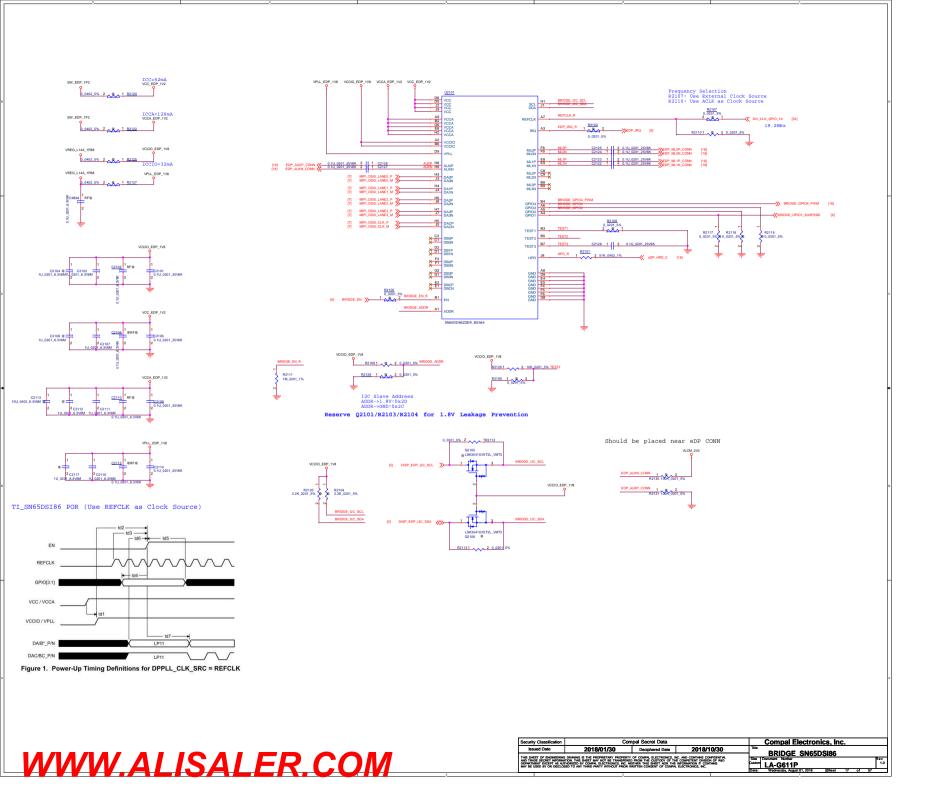
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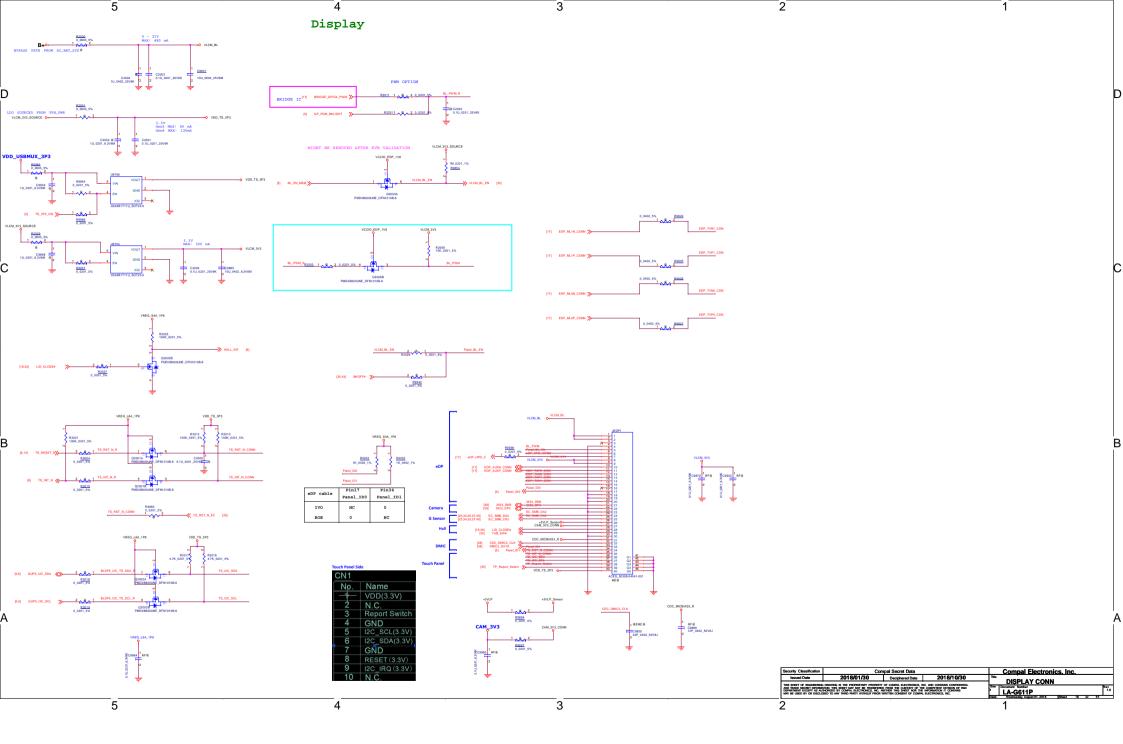


#### PCB ID (1,0)

PCB Ver.	Value	Phase
0.1	00	SDV
0.2	01	FVT
0.3	10	SIT
1.0	11	SVT

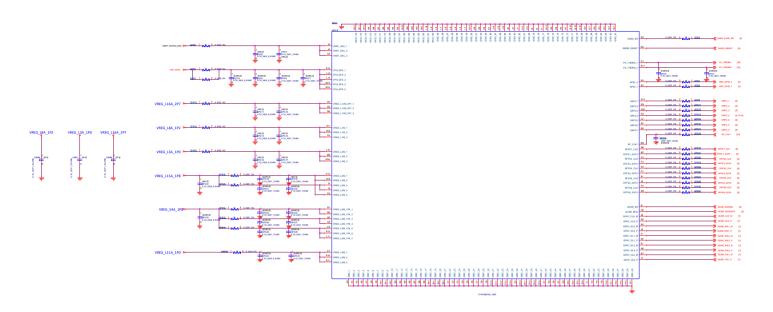
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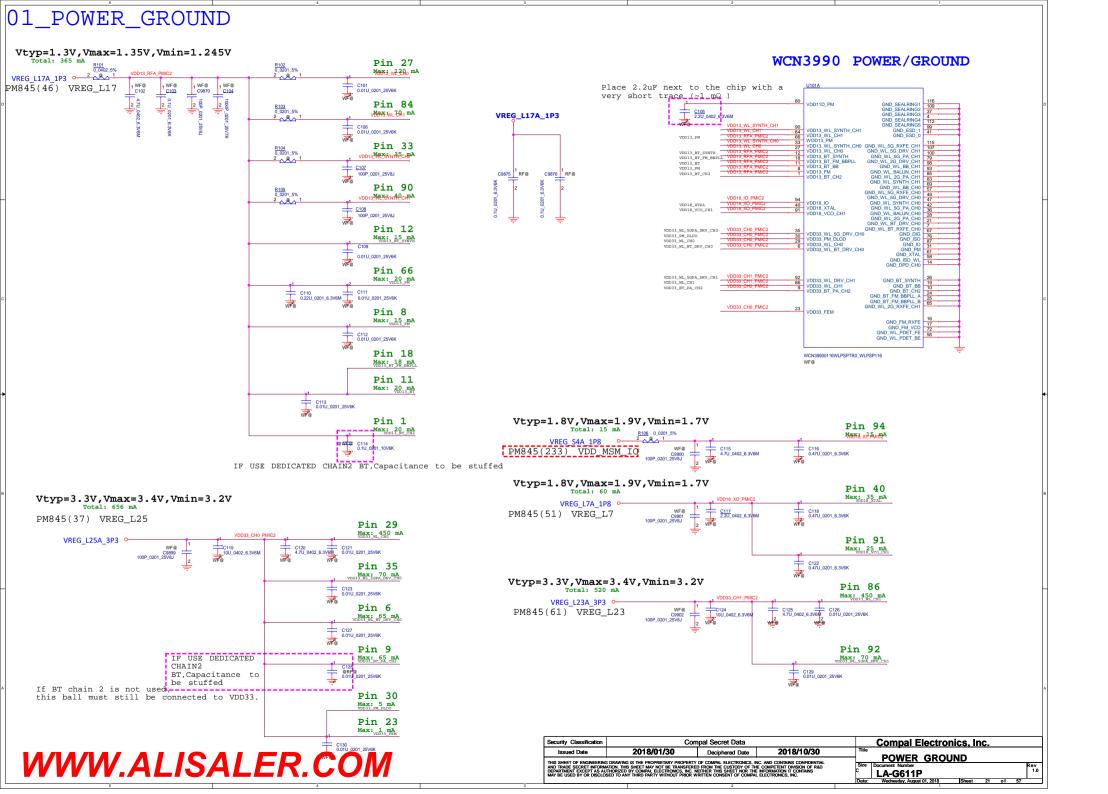






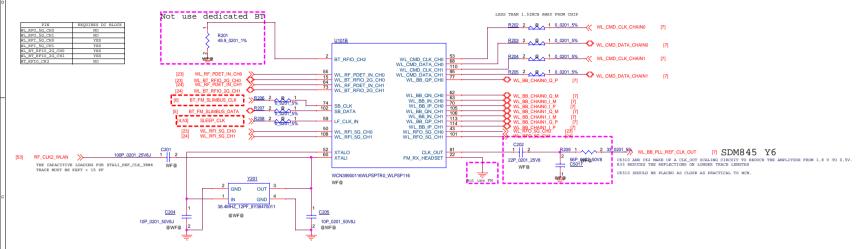
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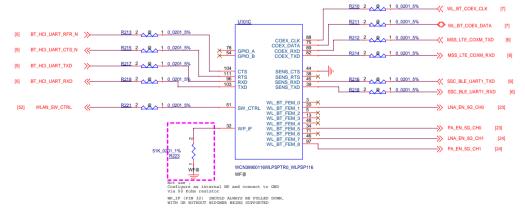
### 02\_RF\_INTERFACES

#### WCN3990 RF/CONTROL



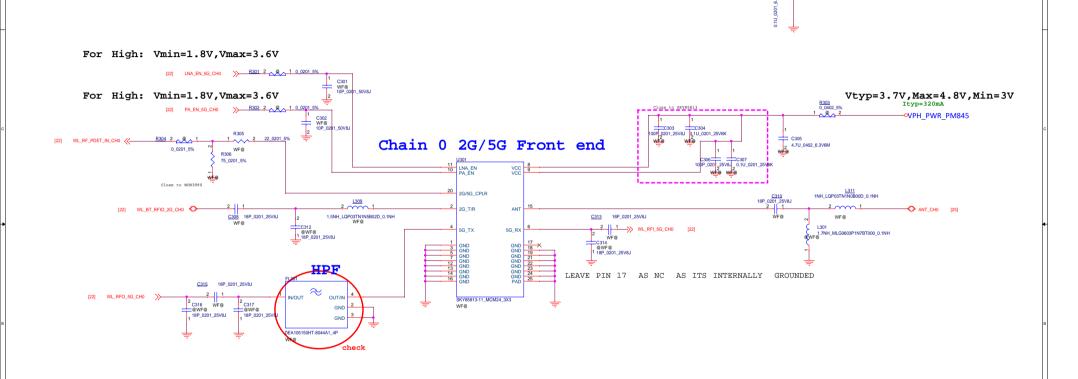
NOTE: CRYSTAL BACKUP STUFF OPTION CAN BE USED FOR IMPROVING EVM PERFORMANCE IN DESIGNS THAT HAVE PMIC/CLOCK LAYOUT ISSUES.IF USING XTAL OPTION INSERT Y1, C27, C19, AND DNI C40

#### WCN3990 RF/IO



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### 03\_RFFE\_CHAIN0\_2G\_IPA\_5G\_FEM\_NON\_ANTENNA SHARING



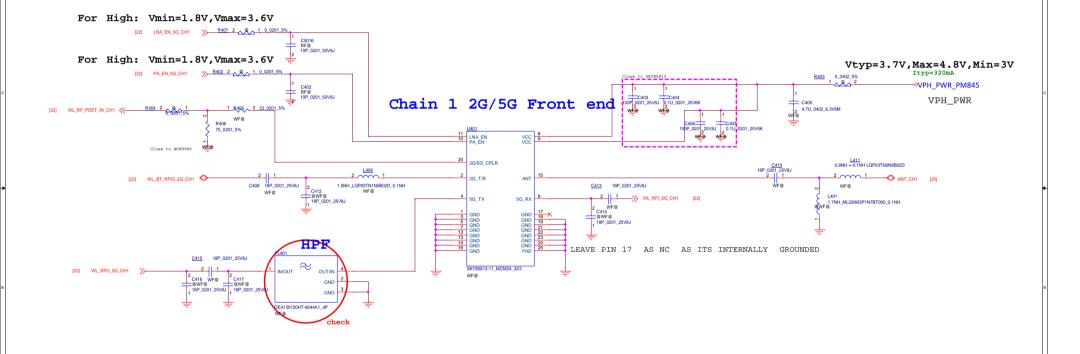
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VPH PWR PM845

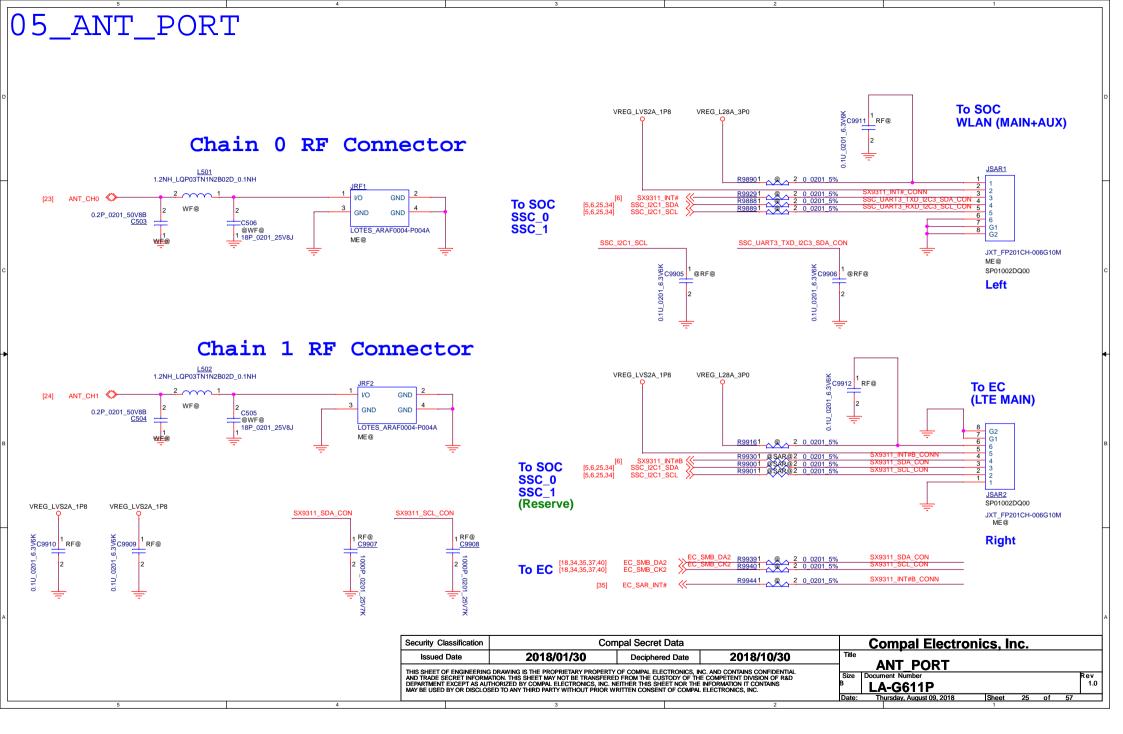
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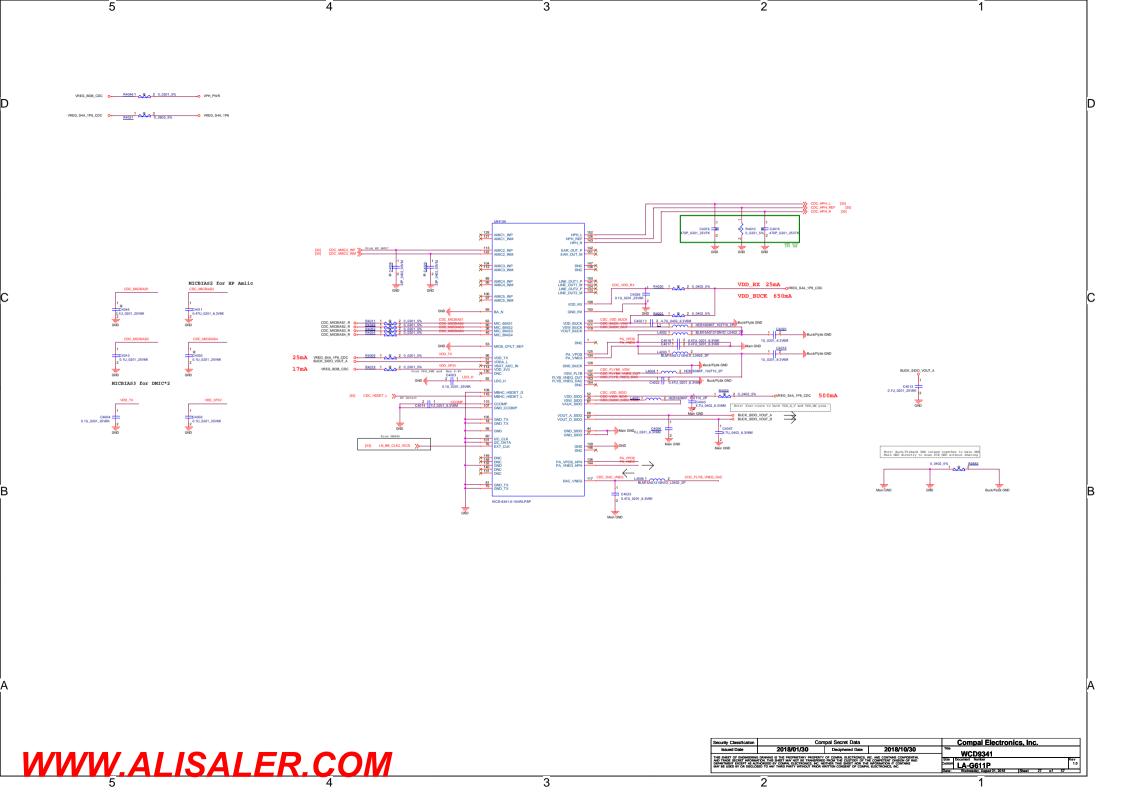
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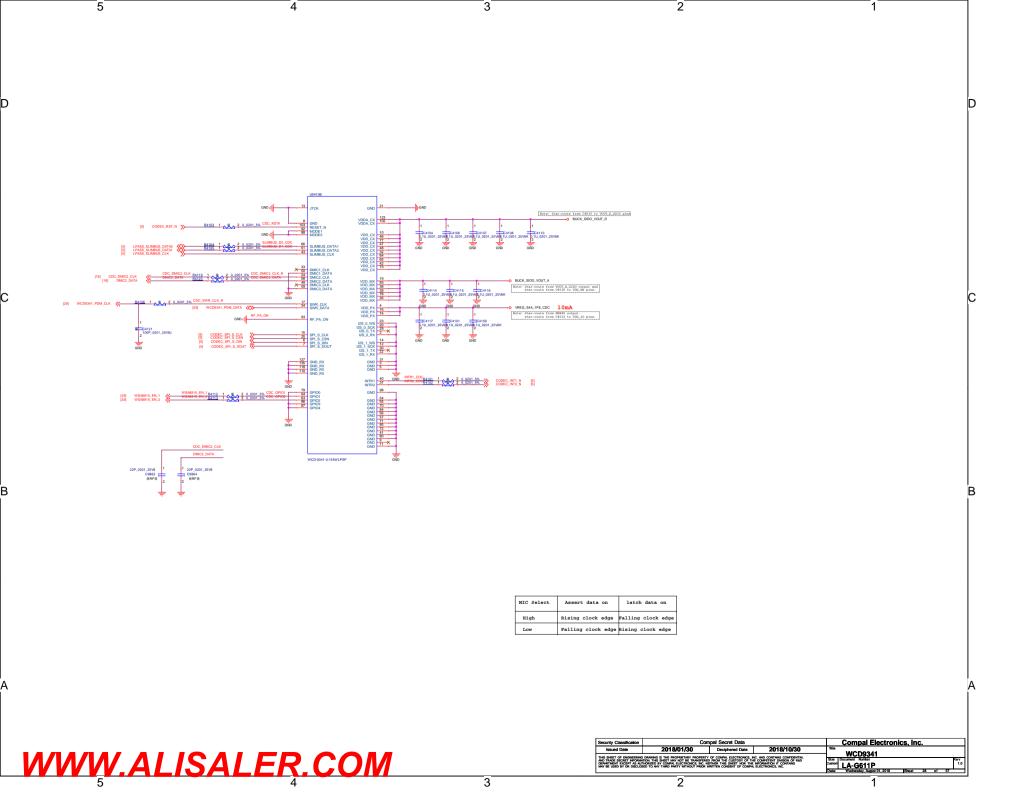
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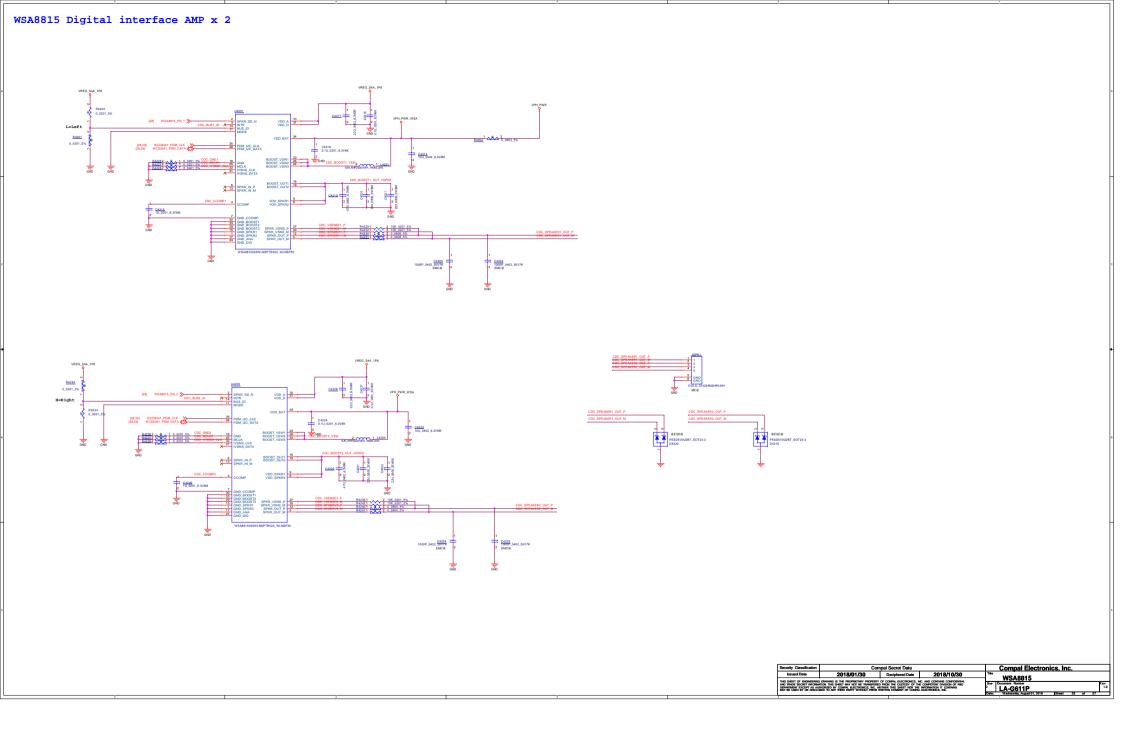


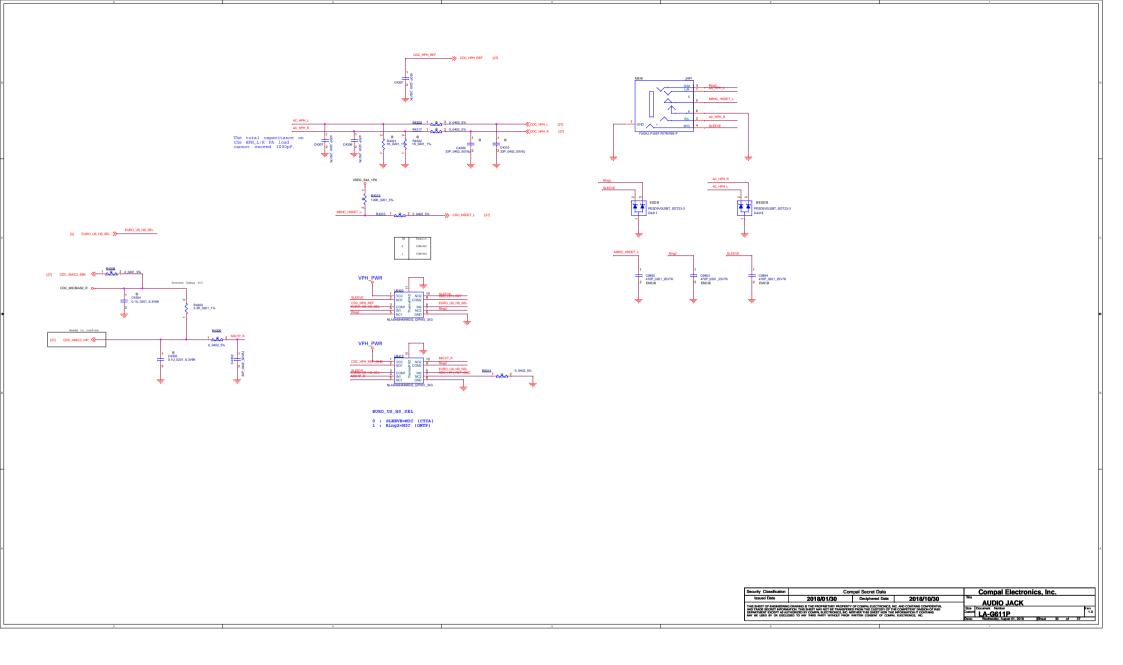


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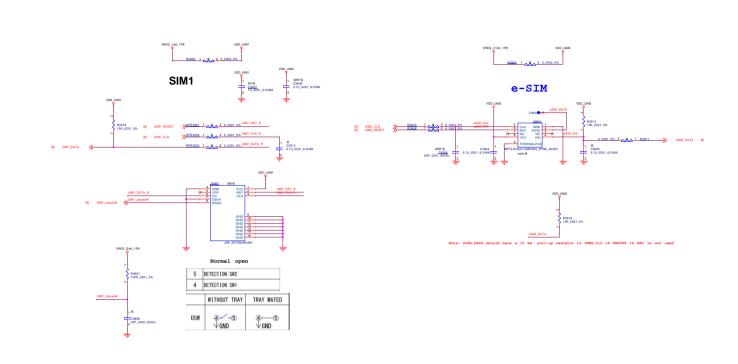






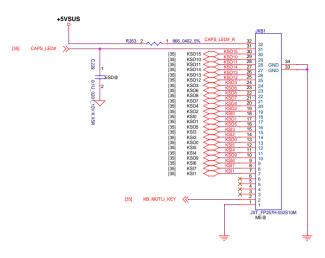


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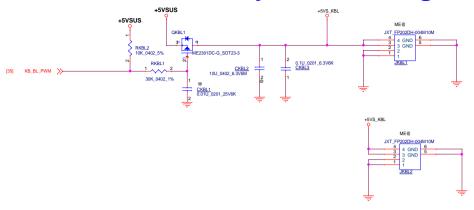


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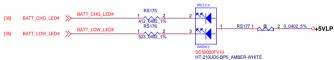
### **Keyboard**



### **Keyboard Backlight**

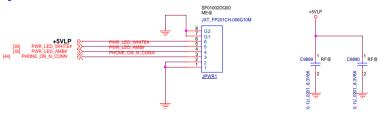


### **BATT LED**

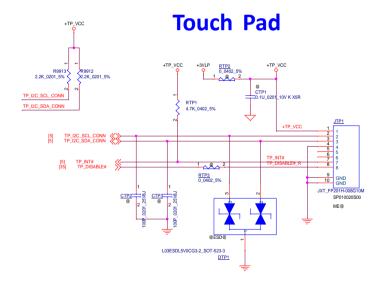


## SC50000FV10 HT-210UD5-BP5\_AMBER-WHITE

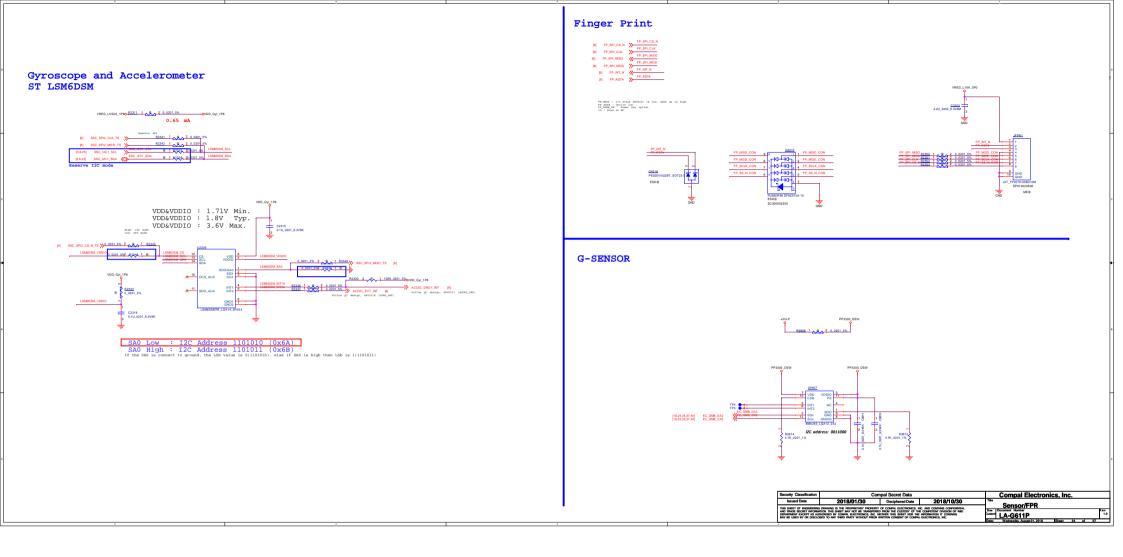
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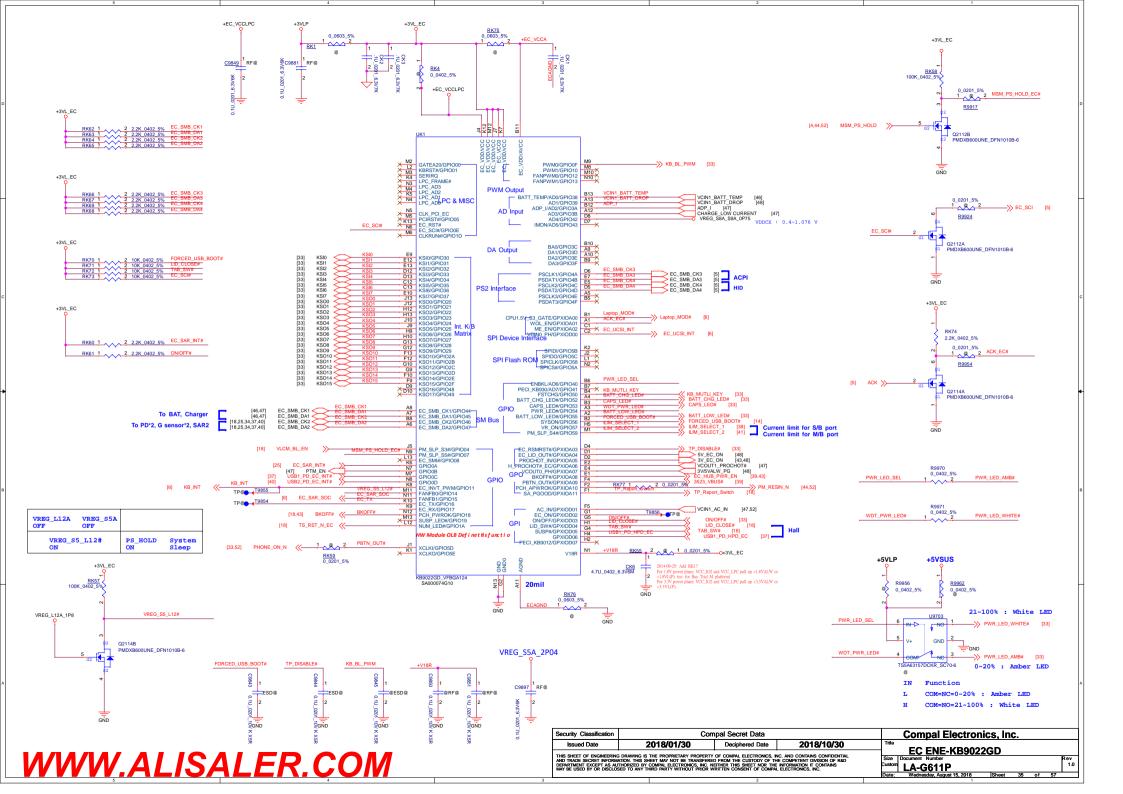


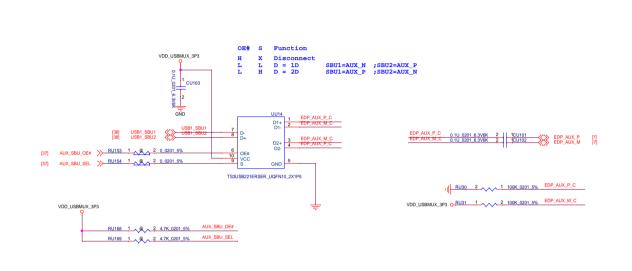




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1				Date:	Monday, August 13, 2018	Sheet	33	of	57

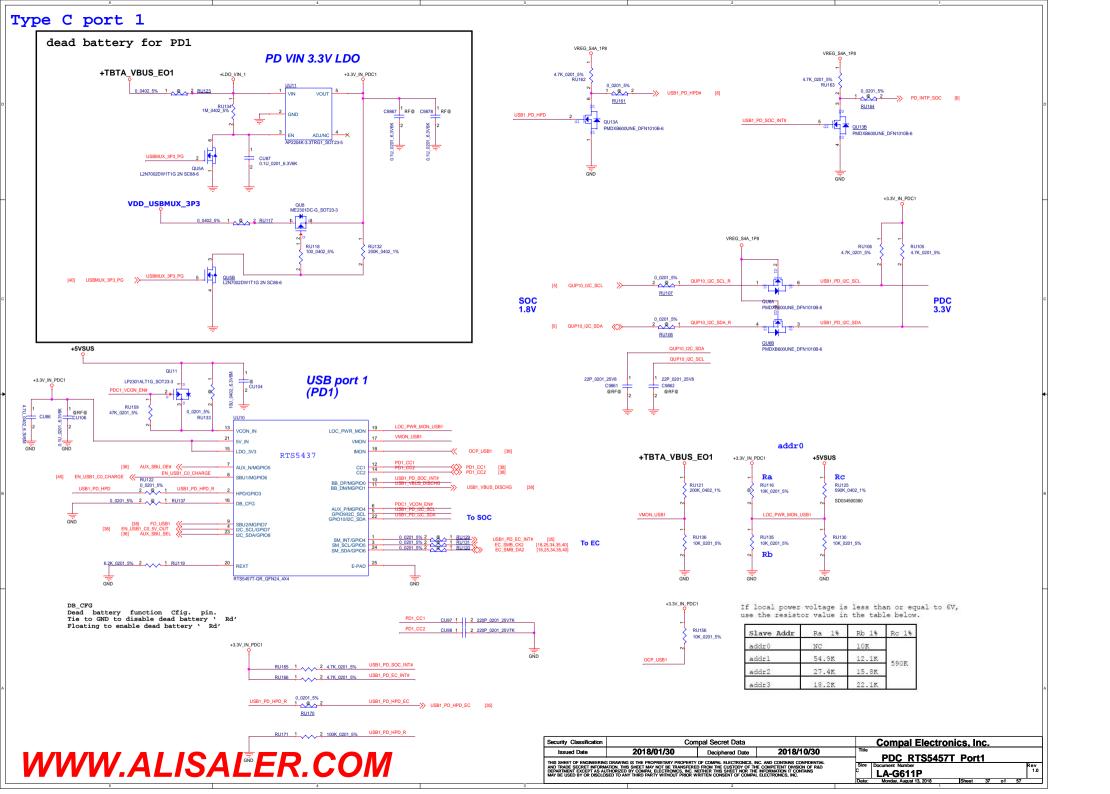


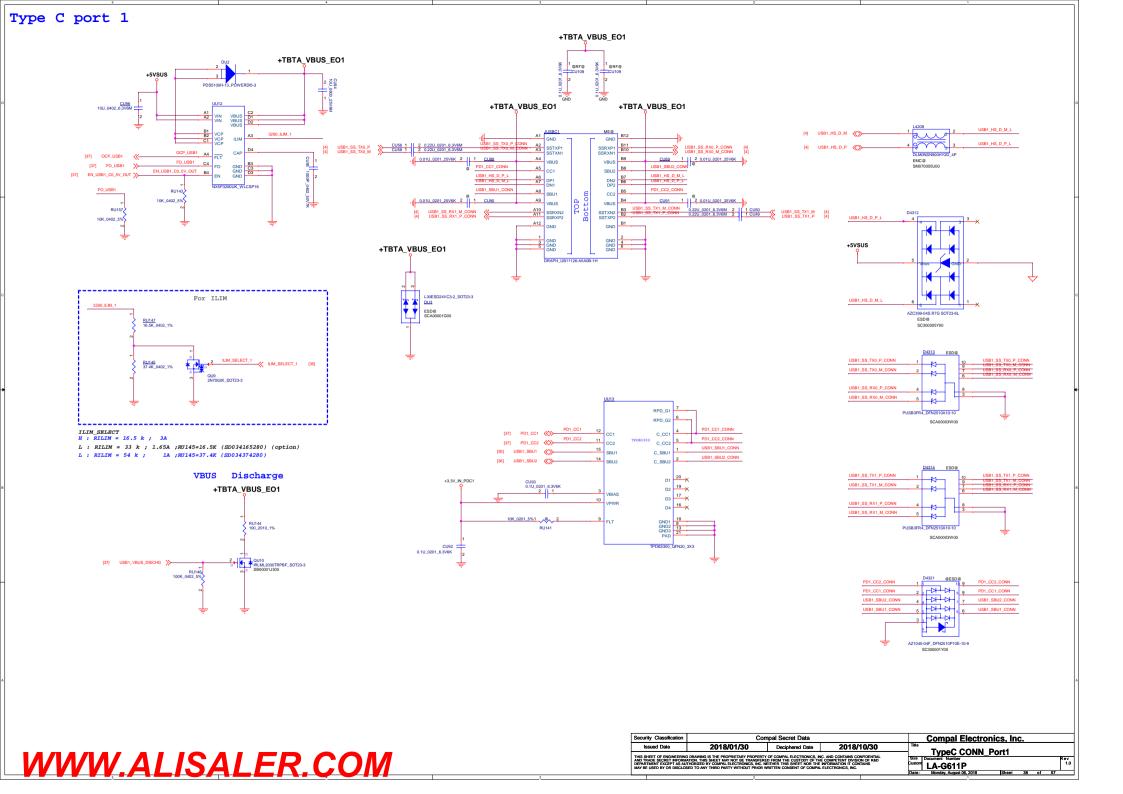


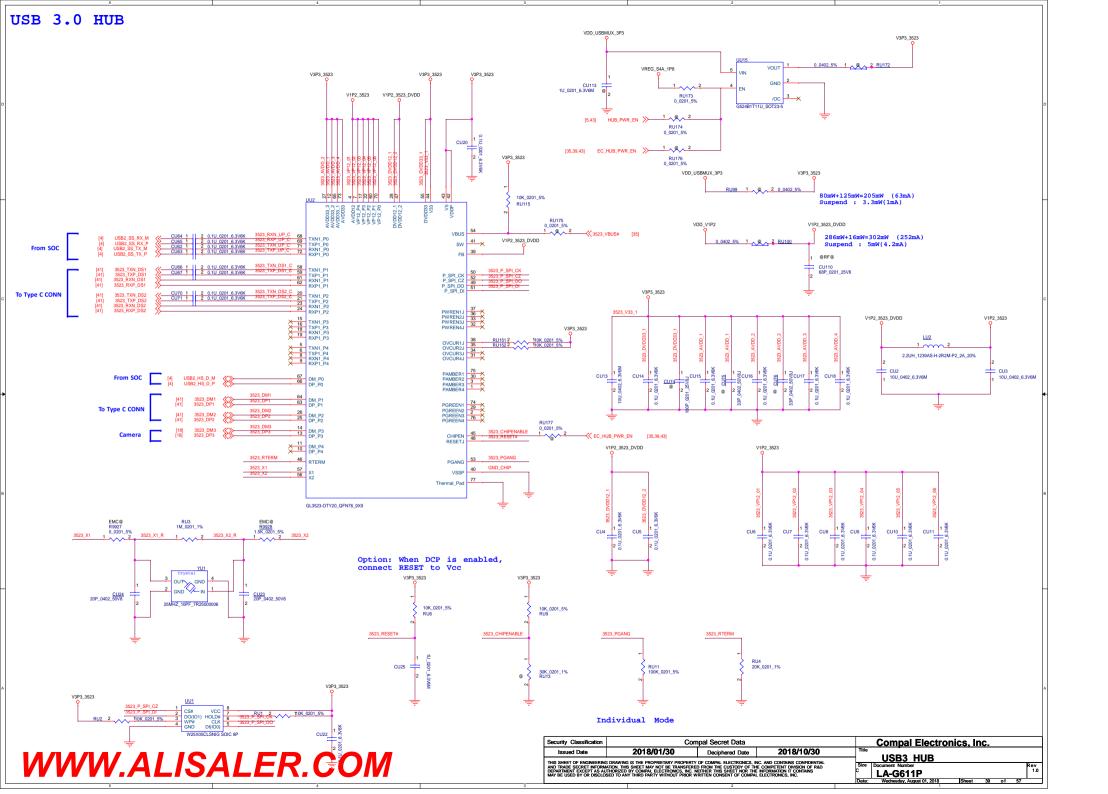


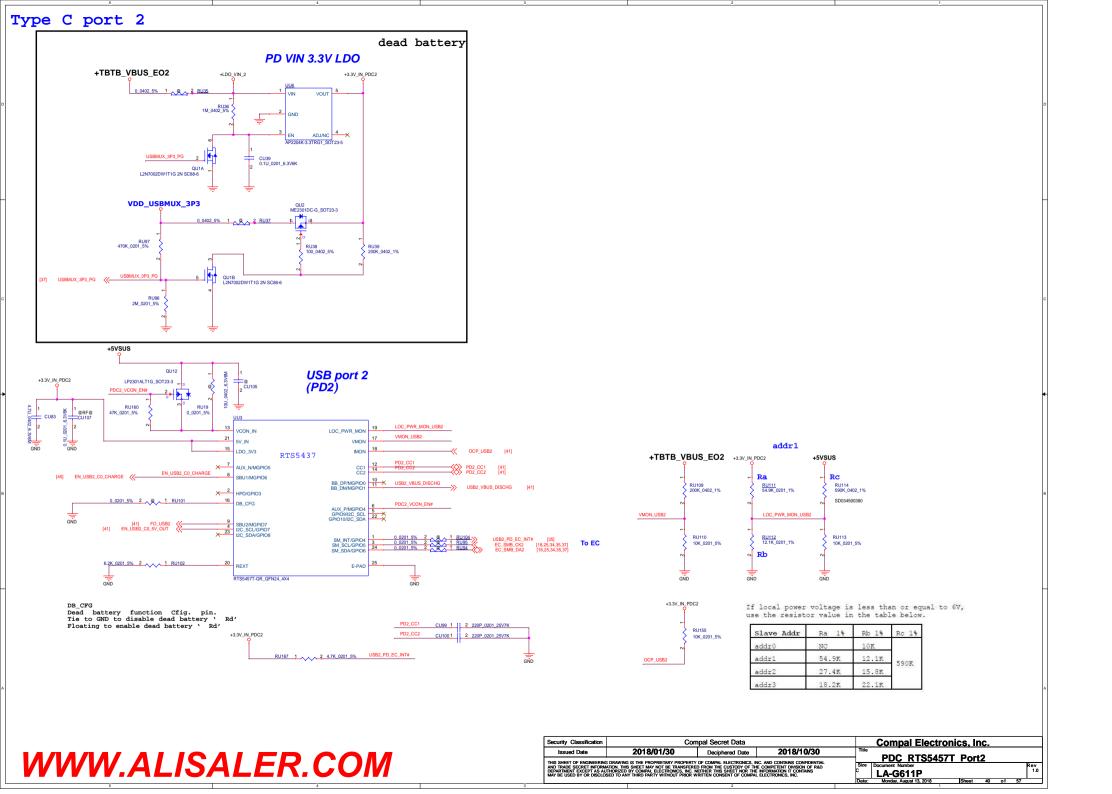
AUX/SBU for port 1

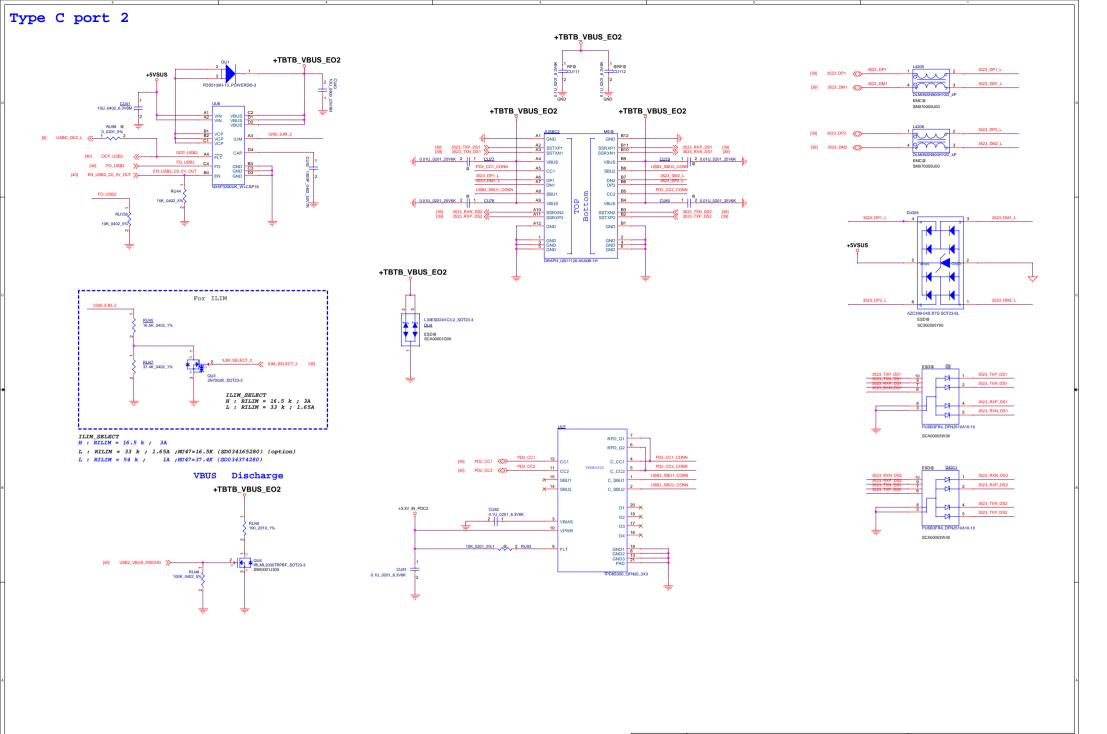
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				Date:	Wednesday, August 01, 2018 Sheet 36	of 57











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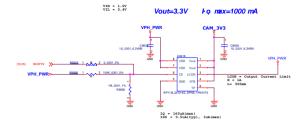
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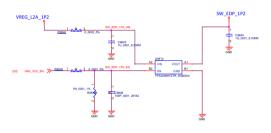
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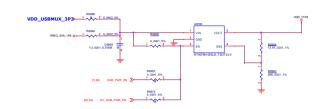
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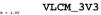
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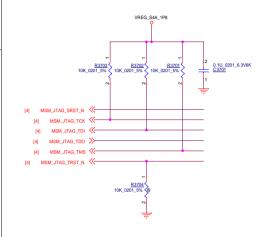


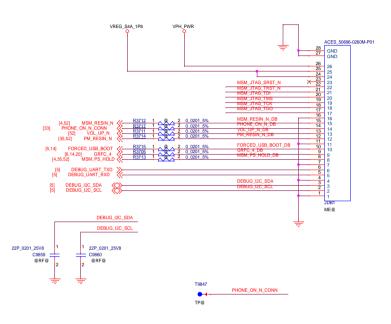




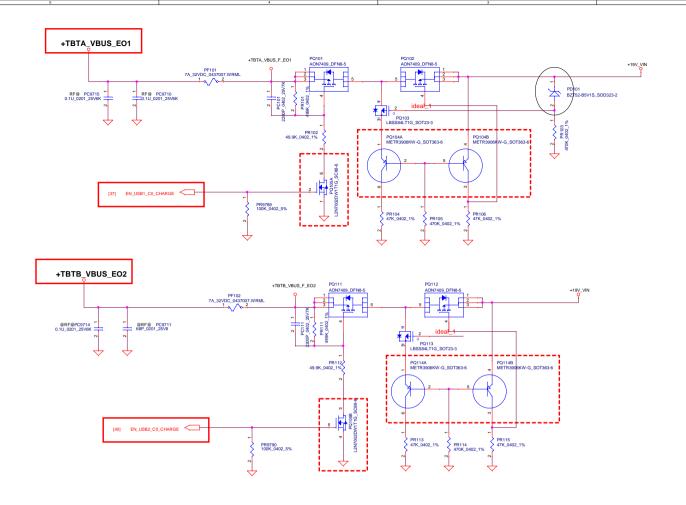
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				Date:	Tuesday, August 14, 2018	Sheet	43	of	57	

#### DEBUG CONNECTOR

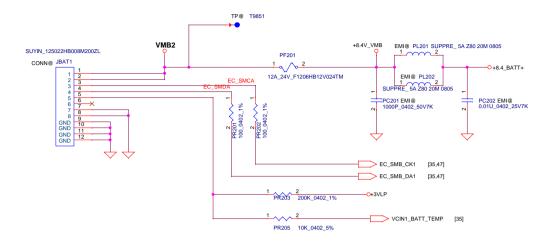




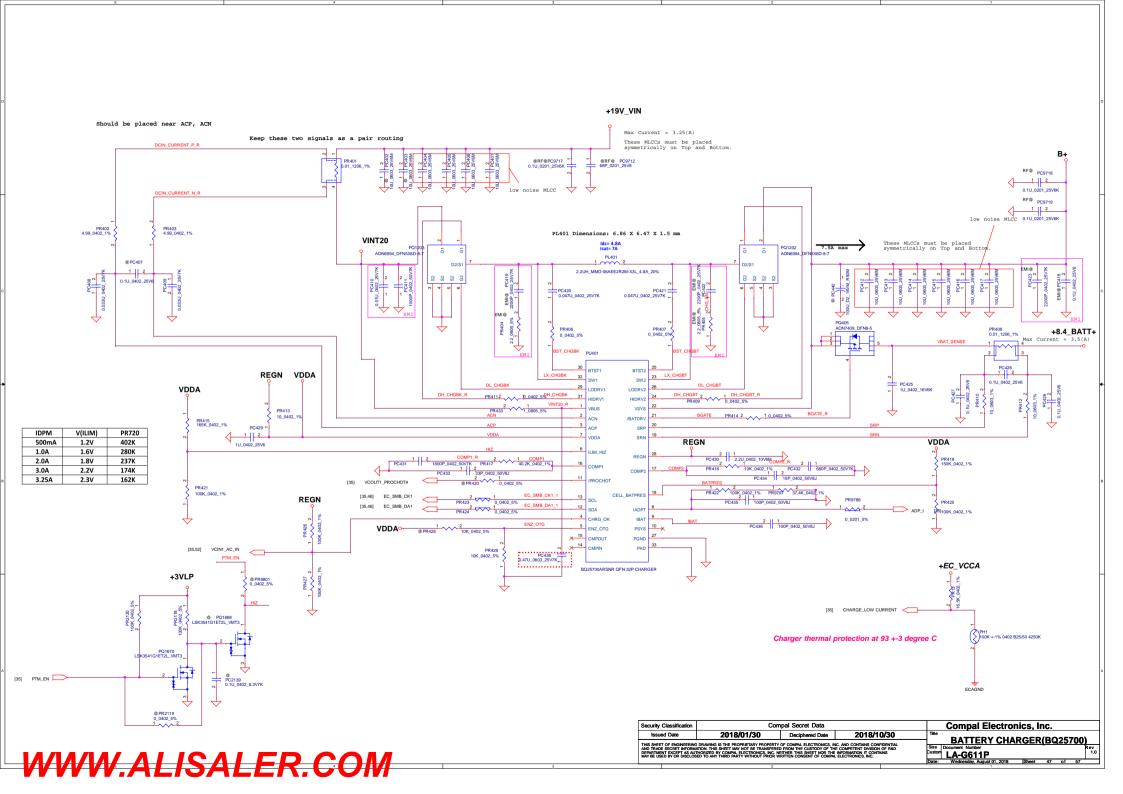
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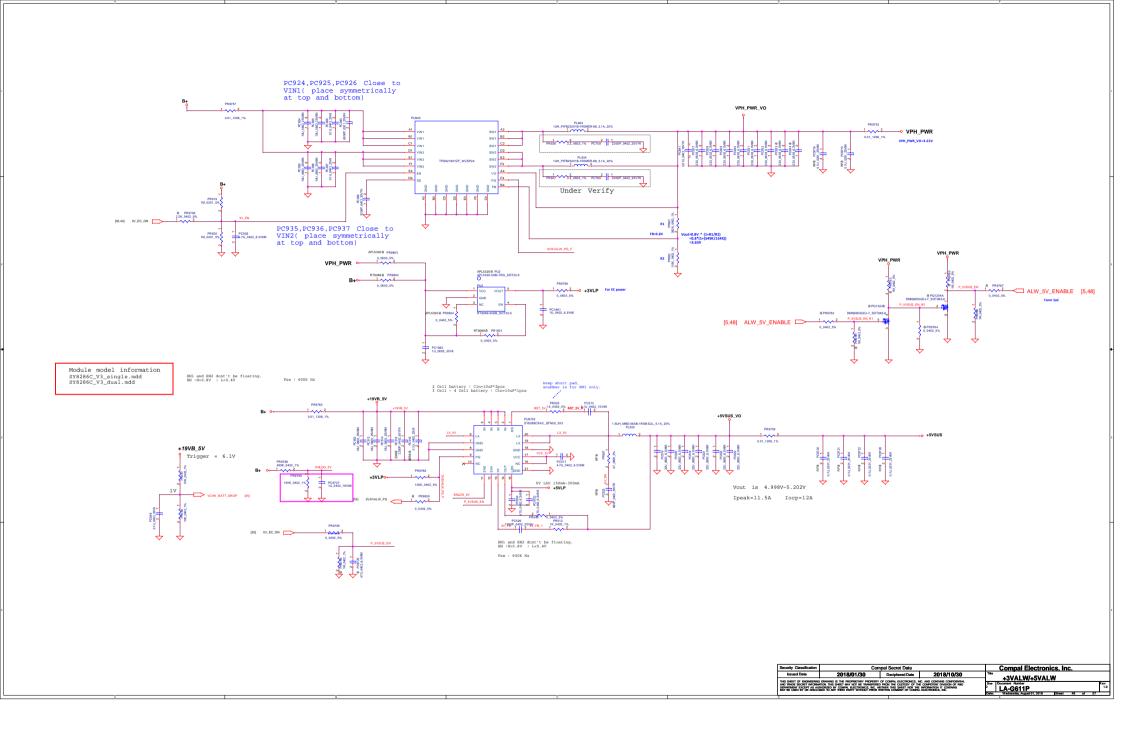


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					Date:	Wednesda	y, August 01, 2018	Sheet	46	of	57	





#### 84\_PMIC\_PM845\_BUCK1

PM84	5 Regula	ator
Regulator	I_rated(mA)	Voltage(\
S1	2000	0.8
S2	2500	1.128
S3	2500	1.352
S4	2850	1.8
S5	1100	2.04
S6	4000	0.8
S7	3600	1.028
S8	4000	0.752
S9	4000	0.752
S10	4000	0.756
S11	4000	0.752
S12	4000	0.752
S13	4000	0.752

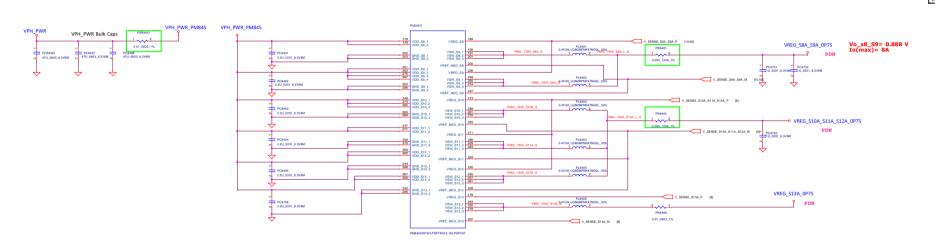
Regulator	I_rated(mA)	Voltage(V)
L1	600	0.88
L2	300	1.2
L3	1200	1
L4	300	0.8
L5	1200	0.8
L6	50	1.856
L7	150	1.8
L8	1200	1.2
L9	150	1.808
L10	150	1.8
L11	1200	1
L12	300	1.8
L13	150	2.96
L14	300	1.8
L15	300	1.8
L16	300	2.704

PM845 Regulator

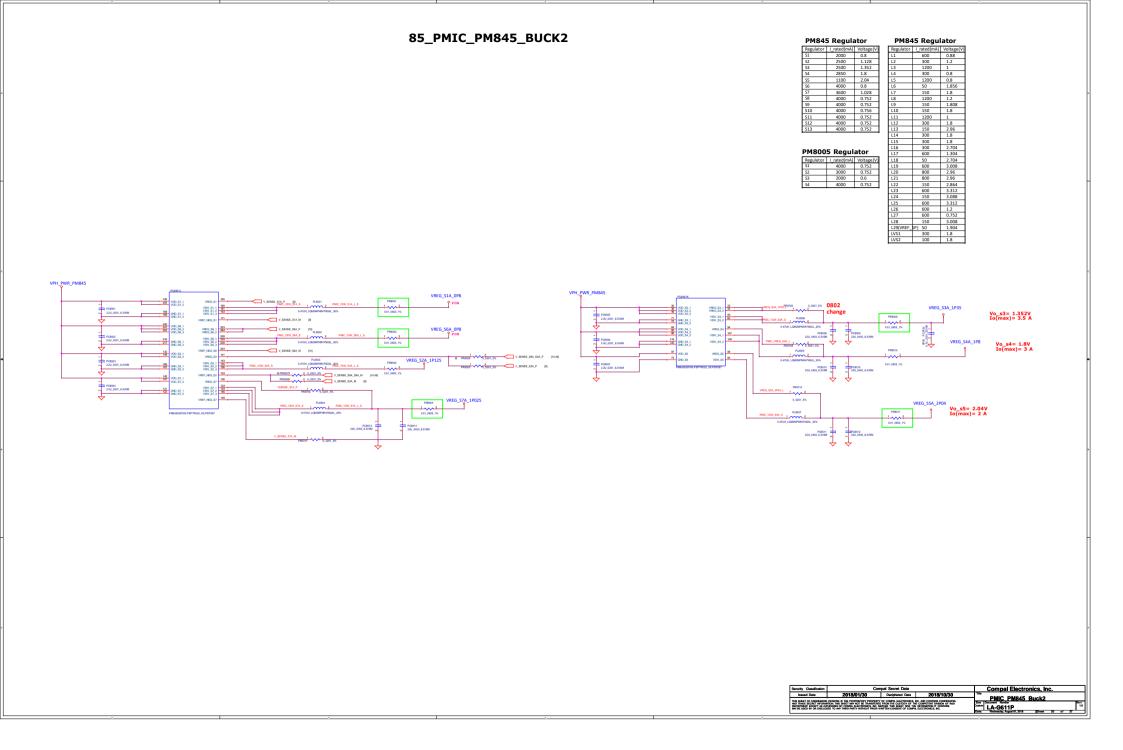
#### PM8005 Regulator

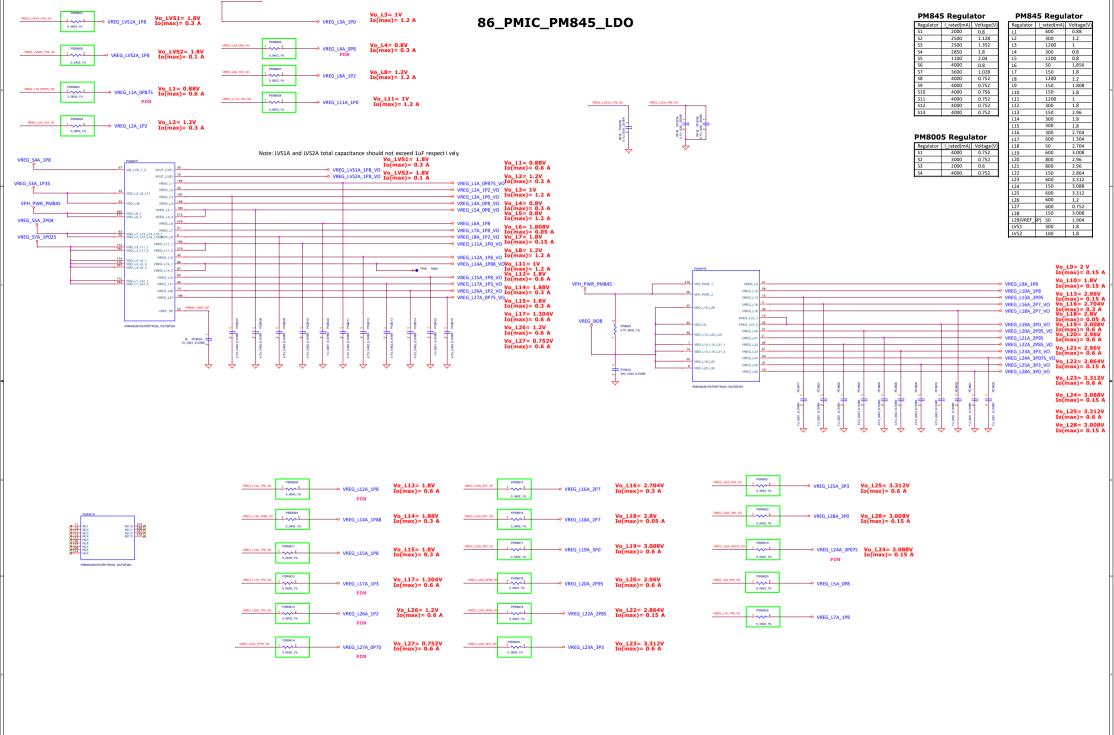
	Regulator	I_rated(mA)	Voltage
1	S1	4000	0.752
	S2	3000	0.752
	S3	2000	0.6
	S4	4000	0.752

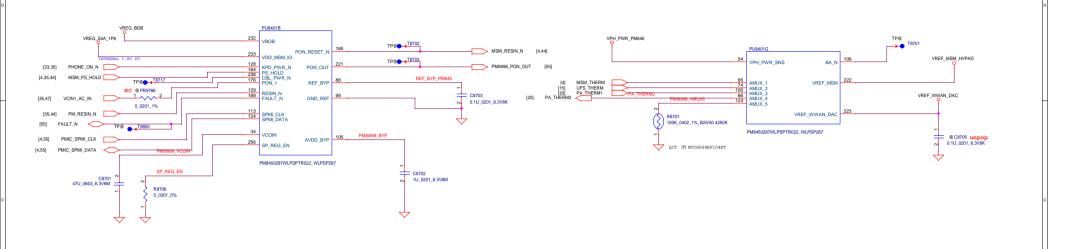
300	1.8
300	1.8
300	2.704
600	1.304
50	2.704
600	3.008
800	2.96
800	2.96
150	2.864
600	3.312
150	3.088
600	3.312
600	1.2
600	0.752
150	3.008
SP) 50	1.904
300	1.8
100	1.8
	300 300 600 50 600 800 800 150 600 150 600 600 600 600 600 5P) 50

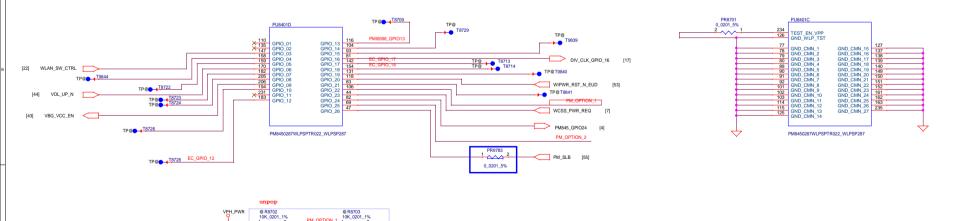


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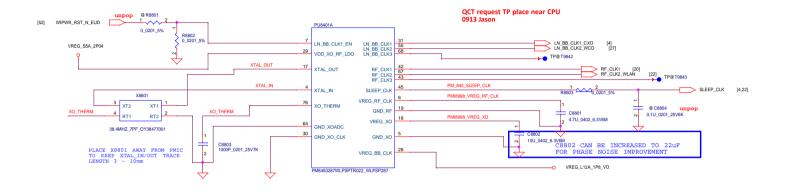






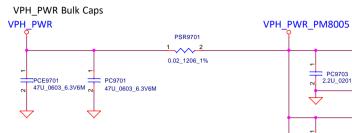


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				Date:	Wednesday, August 01, 2018	Sheet	53 of	57	

### **97\_PMIC\_PM8005\_BUCK**



### PM845 Regulator

Regulator	I_rated(mA)	Voltage(V)		
S1	2000	8.0		
S2	2500	1.128		
S3	2500	1.352		
S4	2850	1.8		
S5	1100	2.04		
S6	4000	0.8		
S7	3600	1.028		
S8	4000	0.752		
S9	4000	0.752		
S10	4000	0.756		
S11	4000	0.752		
S12	4000	0.752		
S13	4000	0.752		

#### PM8005 Regulator

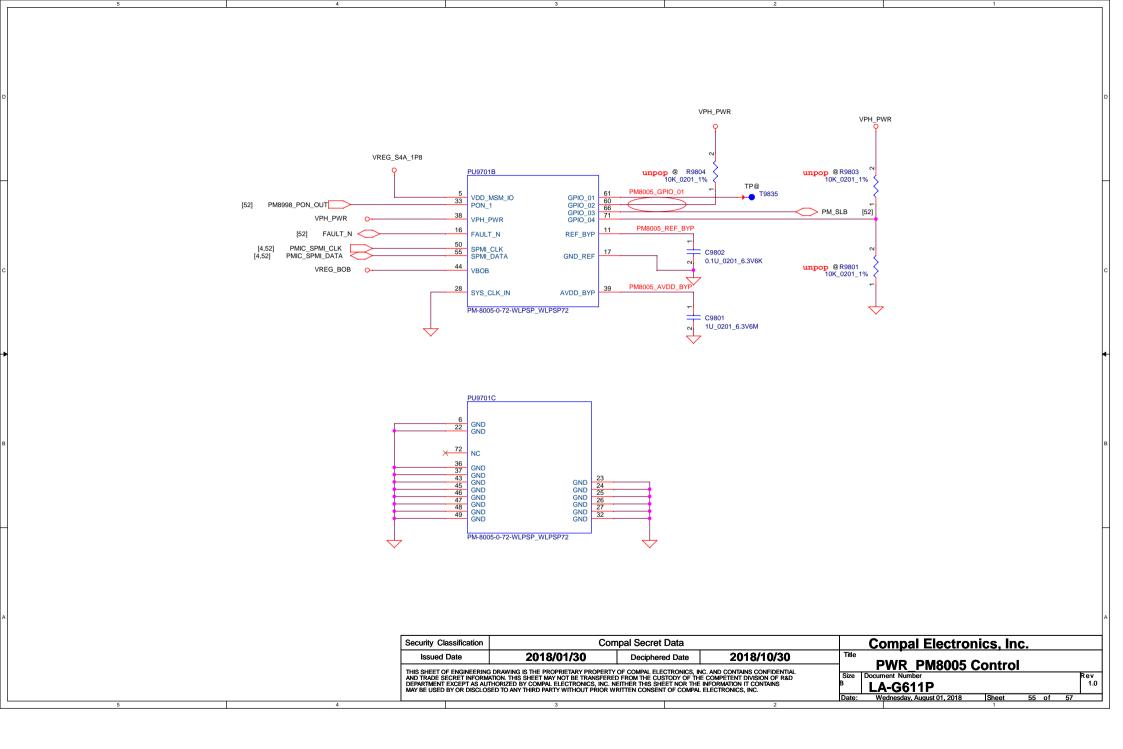
Regulator	I_rated(mA)	Voltage(V)	
S1	4000	0.752	
S2	3000	0.752	
S3	2000	0.6	
S4	4000	0.752	

#### PM845 Regulator

Photo Regulator		
Regulator	I_rated(mA)	Voltage(V)
L1	600	0.88
L2	300	1.2
L3	1200	1
L4	300	0.8
L5	1200	0.8
L6	50	1.856
L7	150	1.8
L8	1200	1.2
L9	150	1.808
L10	150	1.8
L11	1200	1
L12	300	1.8
L13	150	2.96
L14	300	1.8
L15	300	1.8
L16	300	2.704
L17	600	1.304
L18	50	2.704
L19	600	3.008
L20	800	2.96
L21	800	2.96
L22	150	2.864
L23	600	3.312
L24	150	3.088
L25	600	3.312
L26	600	1.2
L27	600	0.752
L28	150	3.008
L29(VREF_	SP) 50	1.904
LVS1	300	1.8
LVS2	100	1.8

_PWR_PM8005	PU9701A	V_SENSE_S1C_S4C_P	[8] Vo_s1.s4 = 0.752 V Io(max)= 8 A
PC9703 2.2U_0201_6.3V6M 8 19	VDD_S1 VREG_S1 VDD_S1 VDD_S1 VDD_S1 VSW_S1 VSW_S1 VSW_S1 VSW_S1	2 PW_VSW_S1C_S 1 PL9701 2 PW_VSW_S1C_LS 13 0.47UH_LQM2MPNR47NG0L_30%	VREG_S1C_S4C_0P75 PR9701 1
56 62 67	GND_S1	35 V_SENSE_S1C_S4C_M	Vo_s2= 0.752 V Io(max)= 3 A  VREG S2C 0P75
PC9704 52 2.2U_0201_6.3V6M 63	VDD_S2 VREG_S2  GND_S2 VSW_S2 GND_S2 VSW_S2 VSW_S2	51 PW_VSW_S2C_S 1 PL9702 PW_VSW_S2C_LS	PR9702 PDN 2
58 64 69	VSW_S2  - VDD_S3	40 V_SENSE_S2C_M [8] 41 V_SENSE_S3C_P [9]	VREG_S3C_0P6
PC9705 54 2.2U_0201_6.3V6M 65	GND_S3 VSW_S3 GND_S3 VSW_S3 VSW_S3	70 0.47011_EQM/2/WF/NR47/NGUE_5076	1
3 9 14	VDD_S4	42	IO(IIIAX)— Z M
PC9706 21 2.2U_0201_6.3V6M	VSW_S4   GND_S4 VSW_S4   GND_S4 VSW_S4   VREF_NEG_S4	15 0.47UH_CQM2MPNR47NG0L_30% 20 31 V_SENSE_S1C_S4C_M	
<b>\( \frac{1}{2} \)</b>	PM-8005-0-72-WLPSP_WLPSP72		

Compal Electronics, Inc. Security Classification Compal Secret Data 2018/01/30 2018/10/30 Issued Date PWR\_PM8005\_BUCK **LA-G611P** 



Item	Version change list Reason for change,	P <i>G#</i>	Page 1 of 3  Modify List	Date	Phase
1	For energy star	47	Add PC2139, PQ1668, PQ1670, PR2118, PR2119, PR2120 for charger PTM (Pass Through Mode)	20180423	SDV
2	For ME height restrict area	47	PC438 change to 0.68u_0603_25V size	20180423	SDV
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l			Security Classification Compal Secret Data  Issued Date 2018/01/30 Decimporal Date 2018/10/30 Title		ctronics, Inc.
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