Bitan Mallik

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Education

Cornell University (College of Engineering) **2025 – 2026**
Master of Engineering (M.Eng) in Engineering Management *Ithaca, New York*

Dresden University of Technology (TU Dresden) **2015 – 2018**
Master of Science (M.Sc) in Nanoelectronic Systems; GPA: 3.73/4.00 *Dresden, Germany*

West Bengal University of Technology **2009 – 2013**
Bachelor of Technology (B.Tech) in Electronics and Communication Engineering; GPA: 3.76/4.00 *Kolkata, India*

Experience

Renesas Electronics **Nov 2023 – Aug 2025**
Senior Engineer - Analog Mixed-Signal Design *Bingen, Germany*

- Led requirements analysis for industrial Ethernet; created product spec in Polarion; achieved CDR, SDR, LDR gates.
- Designed analog transmitter on 40 nm TSMC for Ethernet PHY IP; verified chip top; simulated package and signed-off.
- Ran cross-team design, layout, and verification reviews across 3 groups; passed compliance test; got first silicon success.

Apple **Mar 2022 – Oct 2023**
ICT3 Engineer - AMS Layout Design *Munich, Germany*

- Led a team of 4 engineers to develop PMU using FinFET for Cellular RF SoC; delivered megacell ahead of schedule.
- Managed third-party vendors; organized daily stand-ups, distributed tasks, accomplished goals, and provided feedback.
- Introduced Innovus PnR for AMS blocks and used ParagonX to minimize parasitics; reduced critical-net RC by 20%.

Fraunhofer IIS **Nov 2018 – Feb 2022**
Research Engineer - Analog Mixed-Signal Design *Erlangen, Germany*

- Designed a CDR circuit operating at 8 GHz using 22nm GF FDX for ASA-compliant automotive infotainment SoC.
- Designed multiple ROICs on 180nm XFAB/TowerJazz for ToF imaging, smoke detection, & smart farming applications.
- Mentored over 3 research assistants for master thesis; formally reviewed journal, presentation, & research papers.

Technical Skills

EDA/IC Cadence Virtuoso (ADE Assembler, Spectre, AMS), Innovus, Quantus/QRC, Calibre (DRC/LVS), PEX.
Digital Verilog (RTL), MATLAB/Simulink, C, Java, Shell, OS(Linux, Windows).
Workflow Polarion, Confluence, JIRA, Git, LaTex.

Academic Projects

M.Sc. Thesis | *Title: Fast-start-up SerDes transmitter for Neuromorphic Hardware Systems.* | *TU Dresden* **2017 – 2018**

- Developed a fast start-up SerDes transmitter for neuromorphic system; modeled and verified architecture in simulation.
- Extracted key metrics e.g. power, performance, area, & wake-up time; documented & presented results; defended thesis.

M.Sc. Project | *Topic: Low latency SerDes link for high-speed communication systems.* | *TU Dresden* **2016 – 2017**

- Designed 2.5 GHz SerDes link and burst-mode CDR (RTL); verified architecture using mixed-mode (AMS) simulation.
- Achieved optimum power efficiency, low latency, and reduced link initialization delay; documented & presented results.

Certifications

- Phase Locked Loops - Practical & Advanced Design - Prof. Woogeun Rhee (Certificate of Completion) - 2024
- Practical Design of Data Converters - MEAD Course at EPFL, Switzerland (Certificate of Completion) - 2021
- Verification and Test of Integrated Circuits - Practical training at eecy-ic gmbH (Acquired by BOSCH) - 2020

Languages

- English (Fluent)
- German (Advanced)
- Hindi (Fluent)
- Bengali (Native)

Honors and Awards

- GFF an der TU Dresden Scholarship for research contribution during Master's Thesis at chair HPSN - 2017
- DAAD Scholarship for ranking in the top 5% and delivering exceptional project work at TU Dresden - 2016