DIGITAL ELECTRONICS PROJECT

Front-End Acquisition

—

F. BONY -- J. PERCHOUX -- D. RAMBAUD

Project description

The goal of this project is to design a **front-end acquisition** and an associated **digital signal processing**.

The signal is generated by an optical sensor that produces “sawtooth-like” fringes (periodic signal with slowly increasing ramp followed by a **sharp edge**).

By the end of the project your system shall be capable to display the **fringes frequency** on the FPGA extension board.

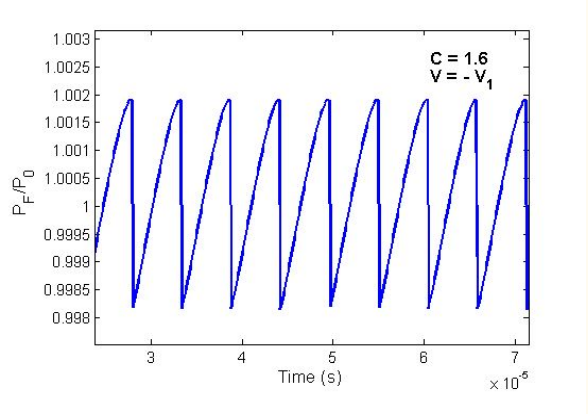


FIG. 1: Signals from the sensor

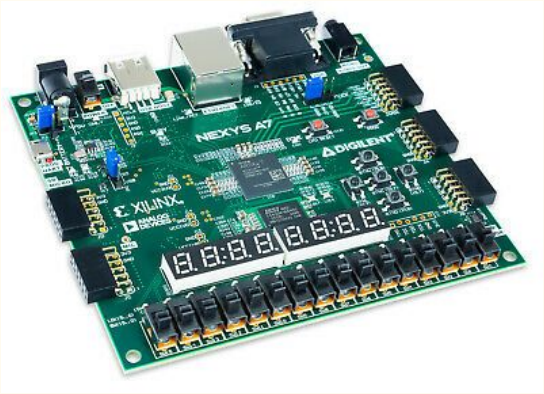
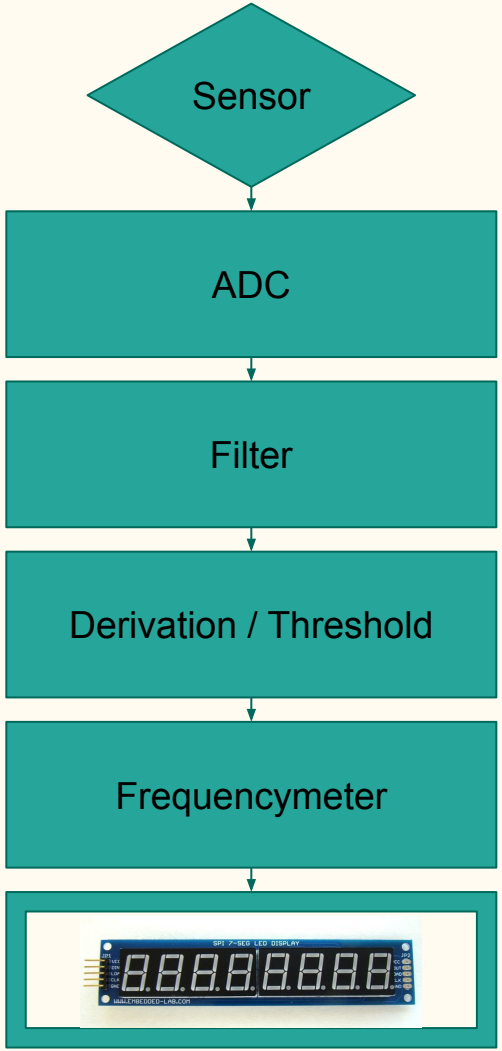


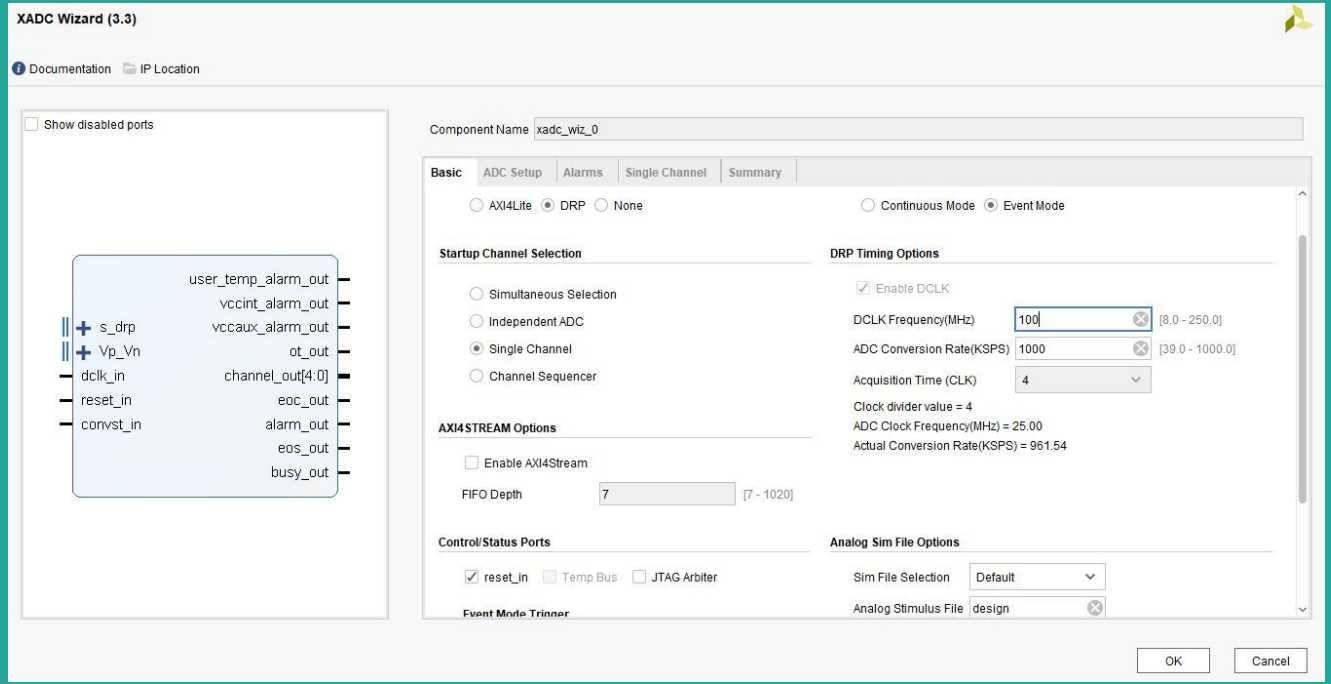
FIG. 2: Digilent Artix-7

Project description (2)

1. The signal is first **acquired** using a **12 bits ADC** that is native to the FPGA at a sampling frequency of 1MHz.
2. The signal is then **filtered** (high-pass) before being **derived** which enhance the sharp edge.
3. A threshold is set to automatically detect the sharp edge.
4. A frequencymeter allows then to measure the fringe frequency which is displayed with a 4 digit resolution.



ADC

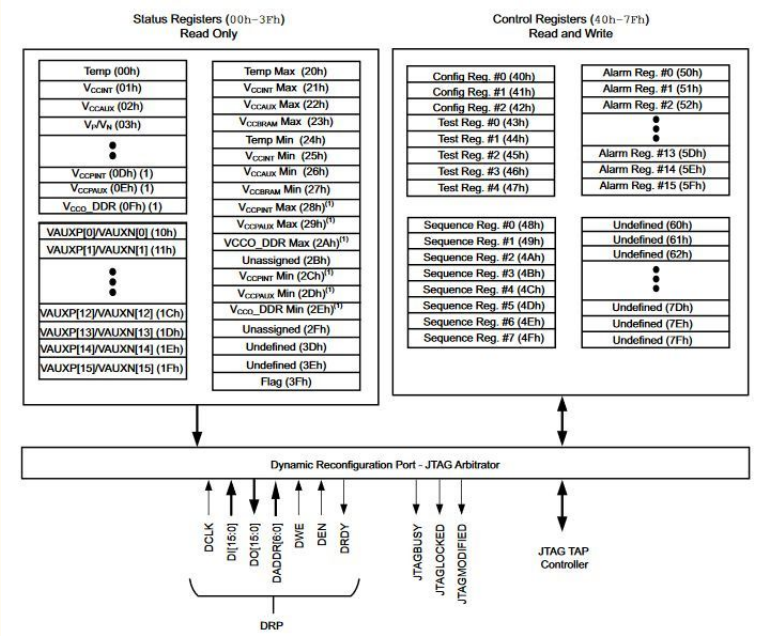

XADC Wizard (3.3)
Documentation
IP Location
Show disabled ports
s_drp
Vp_Vn
dclk_in
reset_in
convst_in
user_temp_alarm_out
vccint_alarm_out
vccaux_alarm_out
ot_out
channel_out[4:0]
eoc_out
alarm_out
eos_out
busy_out
Component Name
xadc_wiz_0
Basic
ADC Setup
Alarms
Single Channel
Summary
AXI4Lite
DRP
None
Continuous Mode
Event Mode
Startup Channel Selection
Simultaneous Selection
Independent ADC
Single Channel
Channel Sequencer
DRP Timing Options
Enable DCLK
DCLK Frequency(MHz)
100
[8.0 - 250.0]
ADC Conversion Rate(KSPS)
1000
[39.0 - 1000.0]
Acquisition Time (CLK)
4
Clock divider value = 4
ADC Clock Frequency(MHz) = 25.00
Actual Conversion Rate(KSPS) = 961.54
AXI4STREAM Options
Enable AXI4Stream
FIFO Depth
7
[7 - 1020]
Control/Status Ports
reset_in
Temp Bus
JTAG Arbiter
Event Mode Trigger
Analog Sim File Options
Sim File Selection
Default
Analog Stimulus File
design
OK
Cancel

XADC

The ADC component is included in the FPGA. It is called XADC and it can be driven using the XADC Wizard that generates a dedicated IP.

The full documentation is available here (PDF), the one of the wizard can be found here (PDF).

The IP generates a memory where acquired signals will be stored. Some of the options you need to set are listed below:



- ❏ Interface : DRP
- ❏ Timing mode : Event mode
- ❏ Startup channel option : Single channel
- ❏ DRP timing options : DCK : 100MHz ; ADC Conversion Rate : 1000 K/samples
- ❏ Control Status Ports : Reset_in
- ❏ Event Mode Trigger : convst_in

You shall use the Vaux3 analog input!!

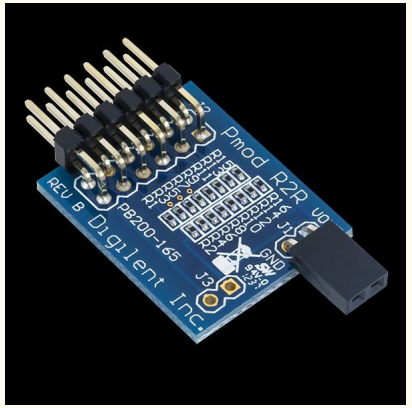
Validation of the ADC

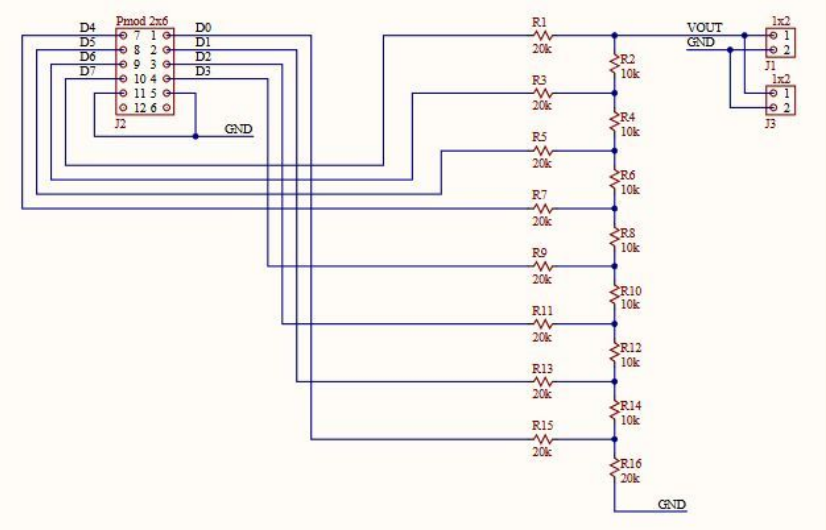
In order to test the ADC, the best solution is to implement a DAC.

You will use a R2R ladder structure that is connected on one of the PMOD connectors.

This type of DAC is very easy to implement, as it is passive and you just need to feed the converter with digital data refreshed at the good rate (ideally the one of the ADC).

Validate first the DAC by feeding it with a ramp, before connecting the ADC outputs to the DAC inputs to validate the ADC.





Filtering

The filter to be designed is a high-pass of first order with a cutoff frequency of 10kHz.

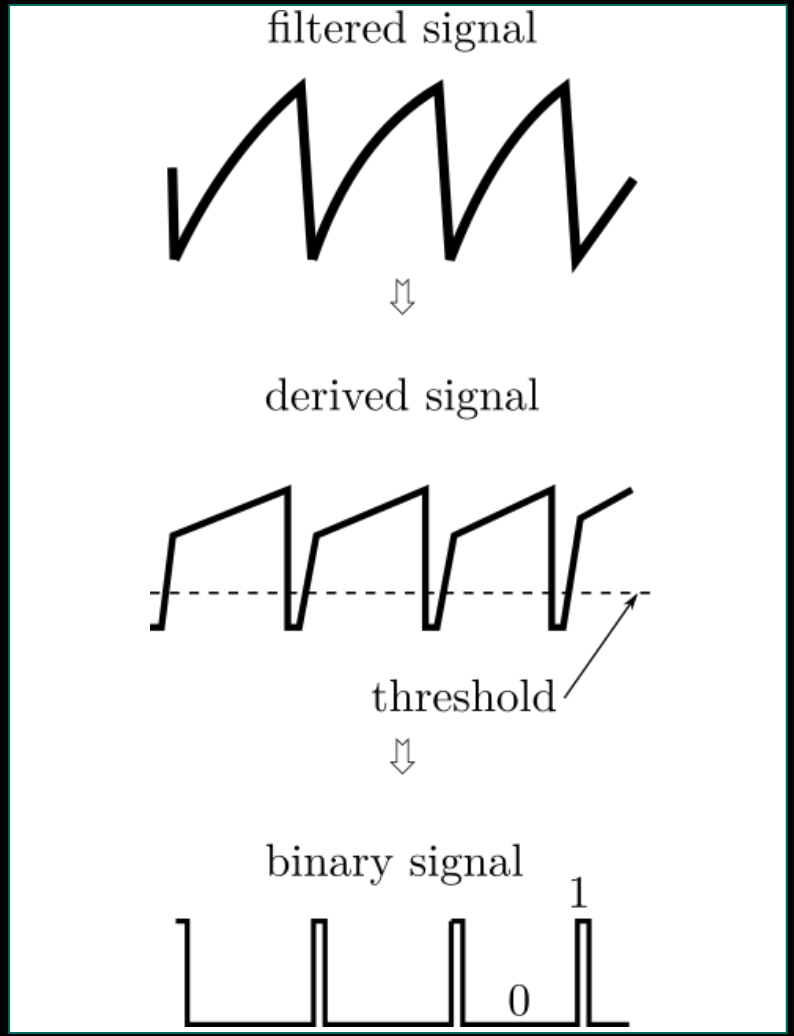
The design uses a fixed point and the sampling frequency F_S of the ADC.

Calculation of the filter

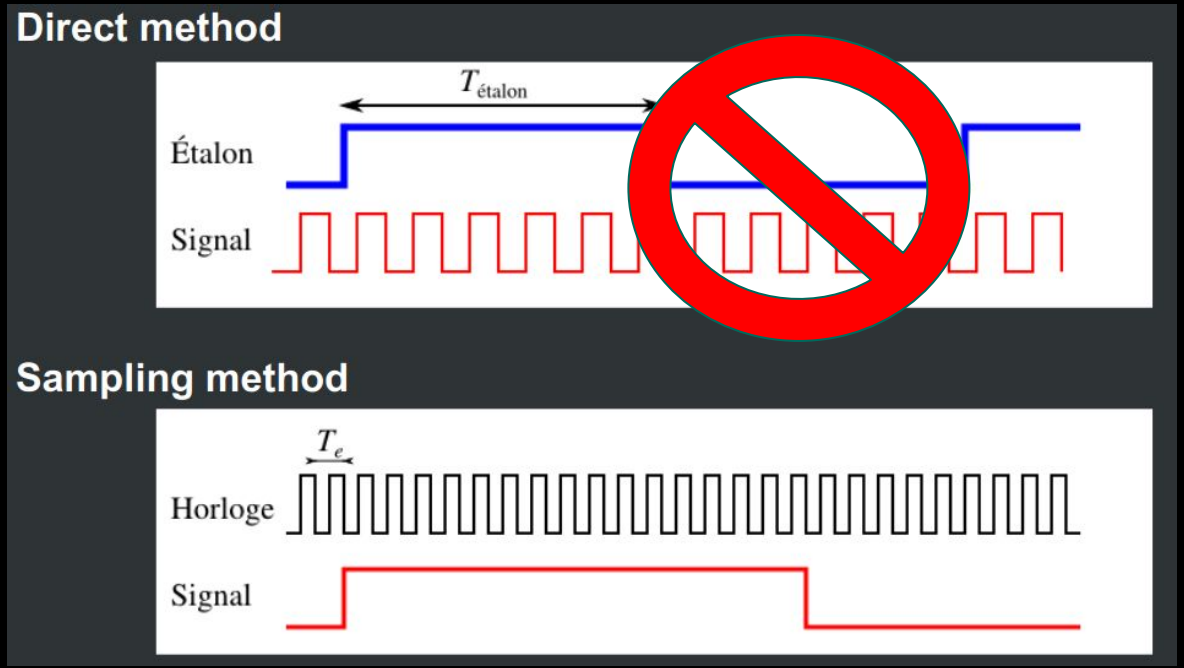
- Express the transfer function between input $x(p)$ and output $y(p)$ in the Laplace domain
- Apply Euler's approximation to express y_k as a function of y_{k-1}, x_k and x_{k-1}
- Design the filter with mathematical operators blocs and appropriate truncatures of vectors

Derivation

The derivation enhance the sharp edges of the signals.
Then by setting a threshold, a binary (single bit) signal can be generated which frequency is the one of the fringes.



Frequencymeter



Frequencymeter requirements

Performances

- Refresh rate : 100 ms
- Resolution: Minimum 4 significant digits
- Range of operation : minimum [100Hz - 200 kHz]

Display

- Automated range display (Hz, kHz) on LEDs or using a 7 segment display.
- Automated placement of the decimal separator : X.XXX, XX.XX or XXX.X