CS351 Computer Systems Engineering Project

Network Switch Design on FPGAs

Specification

1611586

I. Problem Statement

Networking is an important area of Computing, and as network sizes and average complexity of projects have increased, the need for network connections with very low latency has also increased.

Using FPGAs to conduct switching logic can result in a switch with a very high throughput, since this switching logic will be implemented in hardware. The look-up tables (LUTs) on an FPGA can be used to store MAC addresses, allowing an FPGA based switch to theoretically determine the appropriate port to direct a packet to in a single clock cycle. Unlike ASICs, FPGAs are also able to be reconfigured on the fly, so MAC address tables can dynamically updated while still being implemented in hardware. For all of these reasons, FPGA-based network switches should be able to be used to create networks with a much higher throughput than traditional networking hardware, and investigation into FPGA-based switches may reveal further opportunity for other FPGA-based networking hardware, such as routers or firewalls.

The NetFPGA [1] platform is intended to be used for this project. The NetFPGA is an "open source hardware and software platform designed for research and teaching" [2]. Of the four hardware plaforms available, the NetFPGA 1G [3] is the most suitable for this project. The NetFPGA 1G is based around a *Xilinx Virtex-II Pro 50* [4] which contains 53,136 logic cells and 4kb block RAM. In addition, the NetFPGA 1G contains four Gigabit Ethernet networking ports, 4.5MB of SRAM, and 64MB of DDR2 DRAM. It has a standard PCI form factor, and so is compatible with most consumer motherboards.

II. Requirements

In order to measure the success of this project and to clearly define the work to be done, the following requirements have been written. These requirements are subject to change over the course of the project, and are more intended to lay out one available route that the project could take rather than serve to restrict the bounds of the project. They have been written using the MoSCoW method.

A. Functional Requirements

These requirements define the technical detail of the system produced over the course of the project, as well as the data to be analysed for the final report.

F1:

F2: y

B. Non-Functional Requirements

NF1: x

NF2: y

- Research networking concepts (such as the OSI network model)
- Research the NetFPGA platform [1]
- Research the packet switching language P4 [5]
- Implement a packet analyser on a NetFPGA
- Implement a packet switcher on a NetFPGA

- Test throughput and latency of switching packets using the NetFPGA packet switcher
- Test throughput and latency of switching packets using a conventional network switch
- Compare performance of NetFPGA packet switcher to conventional network switch
- Write up performance comparison

III. Project Management

A. Methods

This project will use an agile methodology so that it can adapt to changes which arise during the project. Since the research and implementation stages of the project will contribute to confirming the direction the project will take, this flexibilty is important. In addition, git [6] will be used to track changes in both written documents and any code developed for the project, such as any P4 or Verilog code. Repositories will be set up in git for the different areas of the project, and these repositories will be stored primarily on an online GitHub [7] server and will be backed up regularly. A Gantt chart (shown in figure 1) has been constructed to show an outline of the project timetable, and is intended to be flexible to changes arising during the course of the project.

B. Timetable

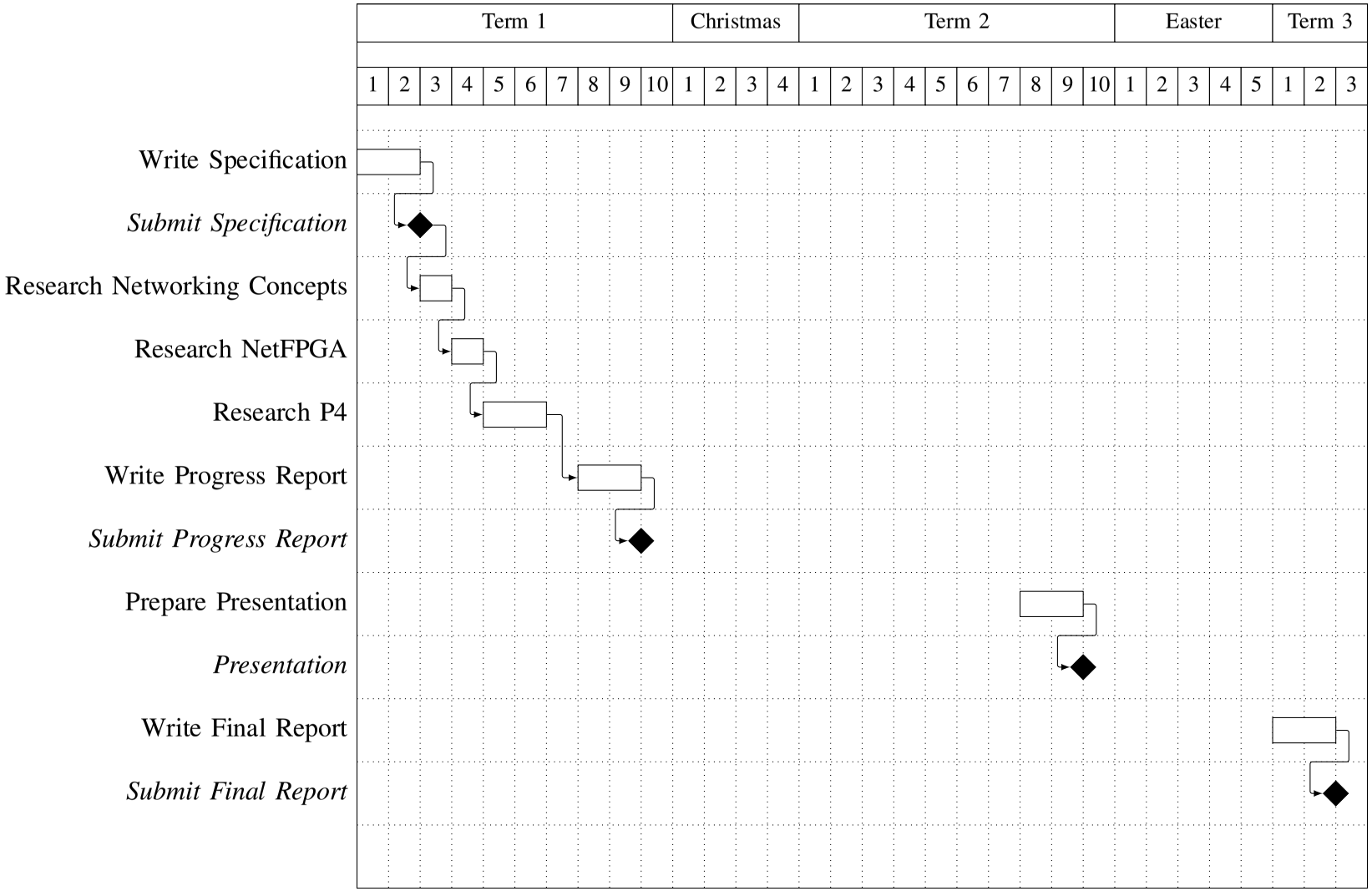

Figure 1: Gantt Chart of Project Timetable

IV. Related Work

https://netfpga.org/site/#/publications/

V. Resources

This project will use a number of different resources, including hardware, software, and languages. These are listed below.

- git [6]
- GitHub [7]
- NetFPGA [1]
- P4 [5]
- LaTeX
- Atom

VI. Glossary

- **FPGA**: Field-Programmable Gate Array
- **ASIC**: Application-Specific Integrated Circuit
- **LUT**: Look-Up Table

References

[1] ”netfpga.org”, “Netfpga.” https://netfpga.org/, Jul 2010. Accessed: 2018-10-08.
[2] ”netfpga.org”, “Netfpga - about.” https://netfpga.org/site/#/about/, Jul 2010. Accessed: 2018-10-09.
[3] ”netfpga.org”, “Netfpga - netfpga 1g.” https://netfpga.org/site/#/systems/4netfpga-1g/details/, Jul 2010. Accessed: 2018-10-09.
[4] Xilinx, *Virtex-II Pro and Virtex-II Pro X Platform FPGAs*, 5 2011. v5.0.
[5] ”p4.org”, “P4 language consortium.” https://p4.org/, Sep 2014. Accessed: 2018-10-08.
[6] ”git scm.com”, “git.” https://git-scm.com/, May 2012. Accessed: 2018-10-08.
[7] ”github.com”, “Github.” https://github.com/, Sep 2009. Accessed: 2018-10-09.