9-Stage Pipeline

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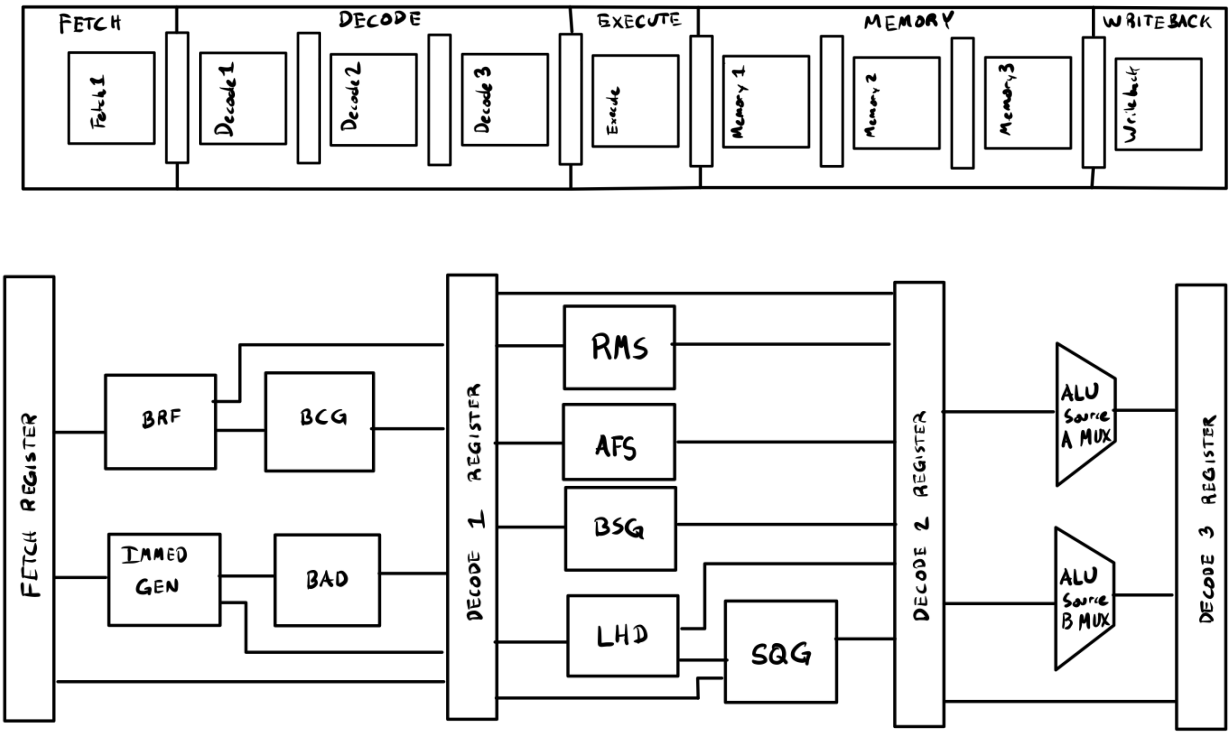

Figure: Basic layout of the 3 stages in the decoder superstage. The module abbreviations shown are as follows:

- **BRF:** Register Forwarder
- **IMMED GEN:** Immediate value generator
- **BAD:** Branch address generator
- **BCG:** Branch condition generator
- **RMS:** Register Multiplexor Select
- **AFS:** ALU Function Select
- **BSG:** Branch Source Generator
- **LHD:** Load Hazard Detector
- **SQG:** Squash Generator

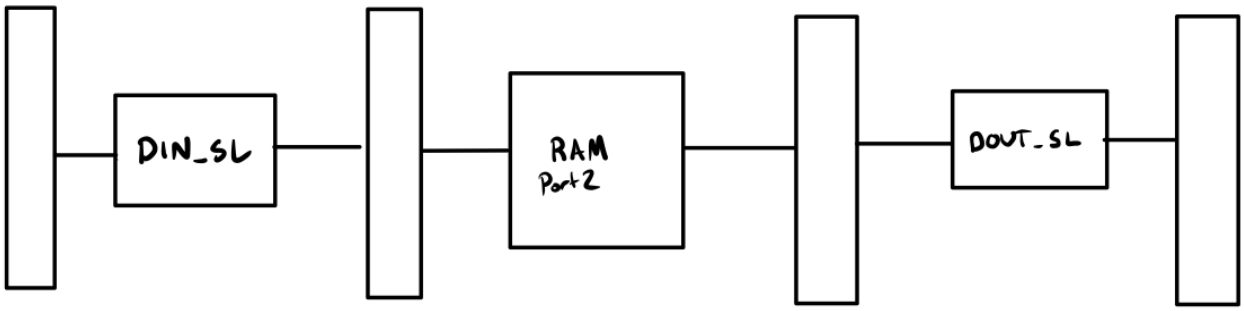

Figure: The 3 stages of the memory superstage in the new design. Not shown is the additional path for the instruction port (port 1), which is essentially not part of the “memory” superstage, though it is technically contained in the module.