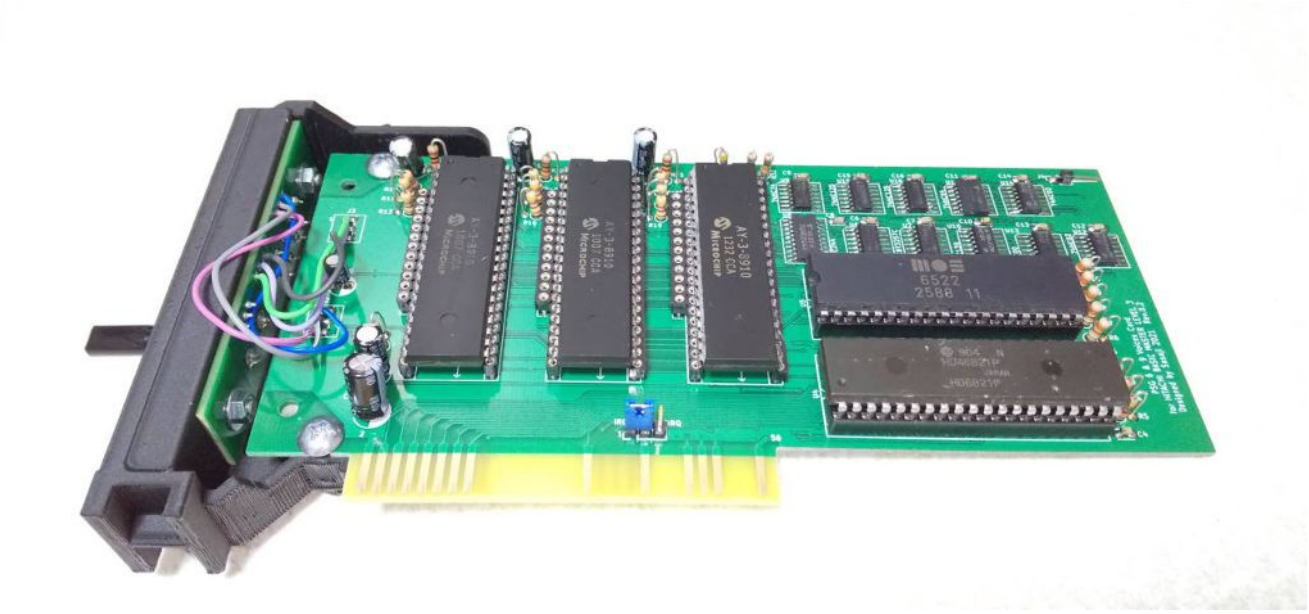
PSG6&9Voices Card for HITACHI BASIC MASTER LEVEL3

Designed by Sasaji 2021 Rev. 0.2

This is an extension card for HITACHI BASIC MASTER LEVEL3, markII and mark5. This is equipped with 3 PSGs and you can play with up to 9 voices.



Implementation

Installation

This card has two modes to control PSG via PIA and to do it via VIA.

PIA mode	This control two PSGs. You can play up to 6 voices. Supported games: Destroy Alien, The Cockpit
VIA mode	This control three PSGs. You can play up to 9 voices. Supported games: Skipper

You can toggle these modes using a I/O port by software, or buttons on the back side.

When specify from BASIC:

PIA: `POKE &HFF34,0`
VIA: `POKE &HFF34,&H81`

I/O Ports

PIA Register

Address	D7	D6	D5	D4	D3	D2	D1	D0	R/W	
$FF30	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0	R/W	PIA Data Register A Write to PSG
$FF31									R/W	PIA Control Register A
$FF32	x	x	x	x	x	SEL	BDIR	BC1	R/W	PIA Data Register B PSG Bus Control
$FF33									R/W	PIA Control Register B

When BDIR = 1 and BC1 = 1, latch register number on PSG.
When BDIR = 1 and BC1 = 0, write data to PSG.
When BDIR = 0 and BC1 = 1, read data from PSG.
SEL : Select PSG1 = 0, Select PSG2 = 1

PIA/VIA Select

Address	D7	D6	D5	D4	D3	D2	D1	D0	R/W	
$FF34 ($FF35)	CLK	x	x	x	x	x	x	V/P	R/W	

V/P … “0”:Select PIA, “1”:Select VIA
CLK … Select clock on PSG “0”: 1MHz “1”:2MHz

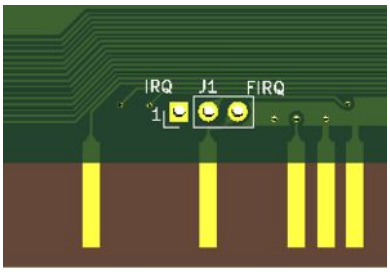
VIA Register

Address	D7	D6	D5	D4	D3	D2	D1	D0	R/W	
$FF70	x	x	x	PSG3	PSG2	PSG1	BC1	BDIR	R/W	ORB PSG Bus Control
$FF71	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0	R/W	ORA Write to PSG
$FF72 ~ $FF7F										VIA Register See datasheet of VIA for details.

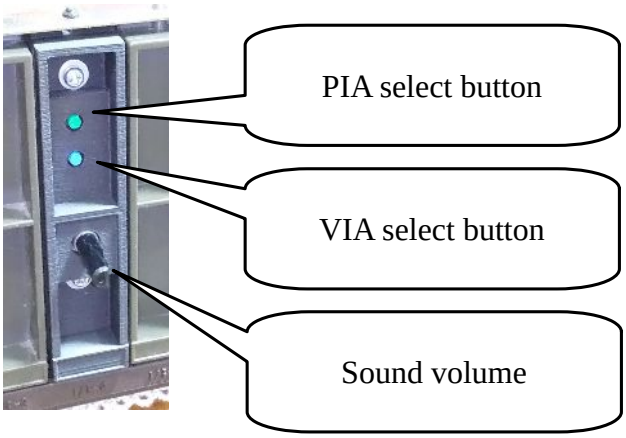
When BDIR = 1 and BC1 = 1, latch register number on PSG.
When BDIR = 1 and BC1 = 0, write data to PSG.
When BDIR = 0 and BC1 = 1, read data from PSG.
PSG1:Select PSG1=1
PSG2:Select PSG2=1
PSG3:Select PSG3=1

Jumper Pin

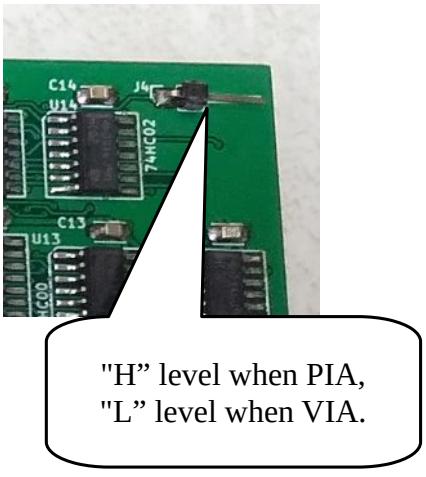
This connect the interrupt signals from PIA and VIA to the CPU side.
Normally, short the IRQ side (1-2).



The back cover



Extended terminal



Attention

- You cannot adjust the sound using the volume on the main board. Please use it on the back cover.
- The Kanji ROM card and VIA address are duplicated. When select the VIA side, don’t read from Kanji ROM or VIA port.
- This board is a prototype. No consideration is given to noise generated during use and deterioration over time.

No warranty

We are not responsible for any damage caused by this card.

You use this card at your own risk.

Web

This document and CAD data are opened on the web.

GitHub(https://github.com/bml3mk5/L3PSG6n9Voices)

or

http://s-sasaji.ddo.jp/bml3mk5/l3psg6n9.htm#board

Sasaji (sasaji@s-sasaji.ddo.jp)
http://s-sasaji.ddo.jp/bml3mk5/
(Twitter: https://twitter.com/bml3mk5)